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Architectures for Sheet-of-Light Range Imaging

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Abstract (150 words):

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Our new image sensor design incorporates the concept of Near Sensor Image Processing (NSIP) where the individual sensor operation is an integrated part of the signal processing algorithm. This architecture can provide range images with very high frame rates. The limit is set by the integration time in the sensor. The NSIP design is automatically adaptive to different light intensities since the utilized integration time for each cell depends on the incoming light. There is no transfer of analog data; each sensor cell output is binary and thus there is no signal degradation in the image readout. Concurrent with the range image, the chip can also produce a grey level reflectance image.

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Range image acquisition can be made in many different ways. In active range imaging a light source is used in cooperation with the sensor and in passive range imaging no special lighting is used. In this paper we concentrate on active range imaging where sheet-of-light illuminates the scene. We present and compare both new and previously reported smart sensor architectures.

Our new image sensor design incorporates the concept of Near Sensor Image Processing (NSIP) where the individual sensor operation is an integrated part of the signal processing algorithm. This architecture can provide range images with very high frame rates. The limit is set by the integration time in the sensor. The NSIP design is automatically adaptive to different light intensities since the utilized integration time for each cell depends on the incoming light. There is no transfer of analog data; each sensor cell output is binary and thus there is no signal degradation in the image readout. Concurrent with the range image, the chip can also produce a grey level reflectance image.

1 Introduction

1.1 Active range imaging

Range imaging is used in many applications, e.g. road surface surveys [8] and industrial robots. In active range imaging the scene is illuminated with structured light, for instance spot illumination, a sheet-of-light or gray coded light. A thorough discussion on the different methodologies can be found in [3], [10] and [11].

In single point illumination one data point (rangel) is acquired for each position of light, and thus $N \times N$ integrations have to be made to obtain a $N \times N$ image. In sheet-of-light illu-

mination one row of rangels is acquired at each light position and thus N integrations are needed for a $N \times N$ image. When using gray-coded light the scene is illuminated with $\log N$ patterns and therefore $\log N$ integrations are needed to form one image.

The gray-coded light technique would then seem to have a speed advantage. However, to get the same signal-to-noise ratio, the over-all illumination level must be increased proportionally. Also, it is difficult to make a projector which can switch between patterns as fast as the sensor can integrate images. Hence, the bottle-neck is in the projector design rather than the sensor.

When using sheet-of-light the projection can be made with a scanning mirror which is considerably simpler than a shutter design. In other applications the sheet-of-light is not swept, but the apparatus or scene is moving and thus no moving parts are needed.

1.2 Range imaging with sheet-of-light

In a sheet-of-light system range data is acquired with triangulation, see Figure 1a. The offset position of the reflected light on the sensor depends on the distance from the light source to the object. To make a sheet-of-light the laser light is passing a cylindrical lens, see Figure 1a-b. For each position of the sheet-of-light a one dimensional range image is acquired, see Figure 1c. Two dimensional images can be obtained in at least three ways: by moving the apparatus over a static scene (in a road survey vehicle), by moving the scene (conveyor belt) or by sweeping the sheet-of-light with a mirror over the static 3 D-scene. In the two first cases the distance can be computed from the offset position in each line with a simple lookup table. In the latter case the direction of the emitted sheet-of-light changes so that a full triangulation computation has to be made to obtain the distance to the objects in the image.

In any case, for each illumination position (and sensor integration) the output from the 2D image sensor should be reduced to a 1D-array of offset values.

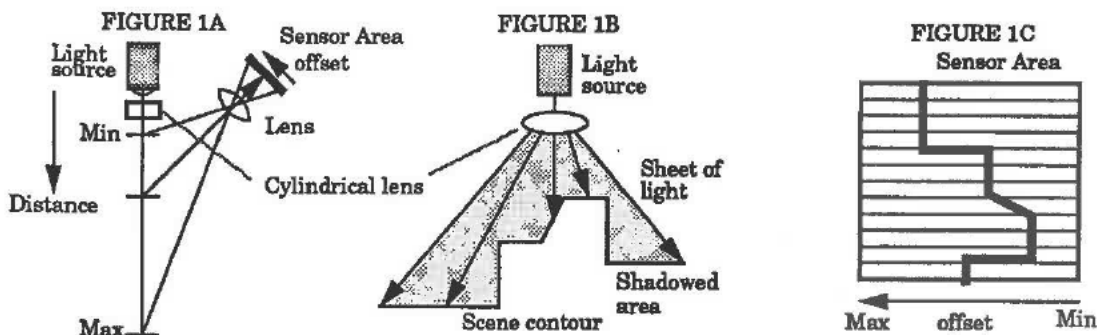


FIGURE 1. A range camera using sheet-of-light. Figure 1a shows the illumination with the sheet-of-light perpendicular, Figure 1b parallel to the plane of the paper. Figure 1c shows a snapshot of the sensor area.

2 Architectures with Smart Sensors

2.1 Video Camera

A standard video camera have poor performance when it is used for sheet-of-light range imaging since the frame rate is set at 50 or 60 Hz, and only one row of rangels are obtained from each video frame. If a 256x256 image is required this result in a range image rate of 0.2 Hz. When using smart sensors which combine sensing and processing on the same chip, shorter integration times can be utilized and considerably faster range imaging obtained.

2.2 Position Sensitive Devices

A one dimensional Position Sensitive device, PSD, is the lateral photo diode shown schematically in Figure 2. The incoming light produces a current in the diode and by measuring the difference of the currents flowing in the different halves of the diode the position of the centroid of the incoming light can be obtained. A summation of the currents give a value proportional to the total intensity of the incoming light.

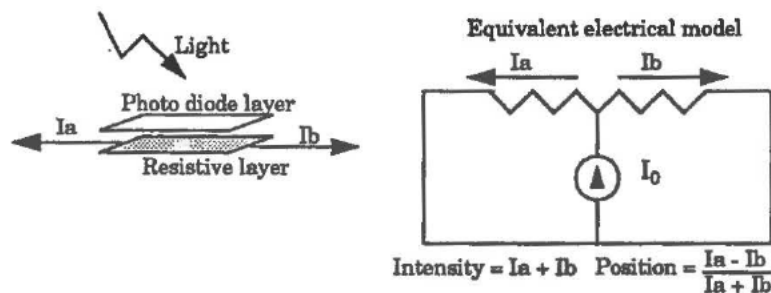


FIGURE 2. A PSD 1-D photo diode.

A range finder based on multiple use of 1D PSD, Position Sensitive Devices, has been presented by Araki et al [7], and it can be seen in Figure 3. An array of 128 PSD's output range images at 32 Hz with a reported accuracy within 0.3%. Besides the problem of designing the array itself, a possible drawback is that the output is an analog value of the centroid of the incoming light. If the background light intensity is high in parts of the picture, the centroid is moved from the position of the peak value, see Figure 4.

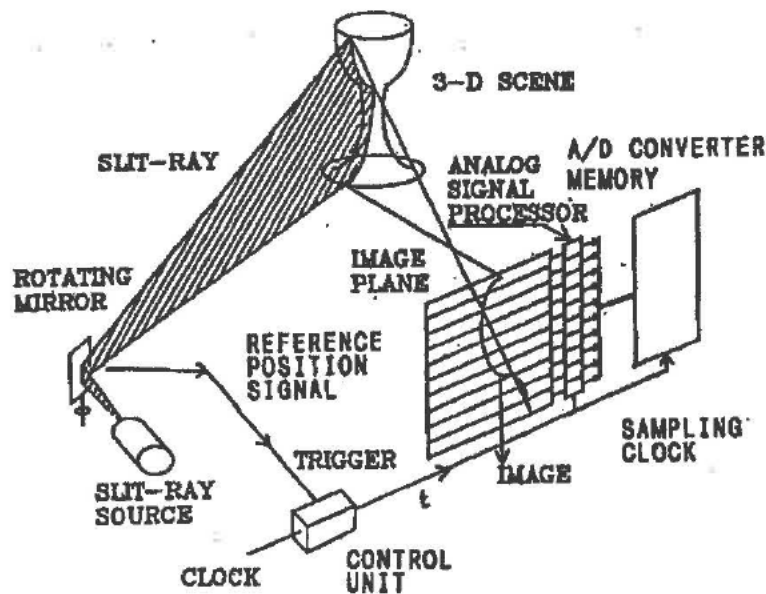


FIGURE 3. A range finder architecture from Araki et al [7]. This figure also illustrate the rotating mirror technique for sheet-of-light imaging.

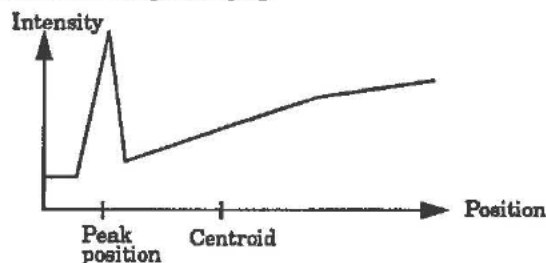


FIGURE 4. Center of gravity when the background light intensity is high.

2.3 Analog Processing Sensor Cells (Kanade)

The sensor design proposed by Kanade [6] has analog processing in each sensor cell. Peak detection and time when the peak occurred is derived within each sensor cell, see Figure 5. The sensor area is integrated as the sheet-of-light sweeps the entire scene and the analog value which hold the sawtooth value for the peak corresponds to the instant of maximum intensity. This point of time gives the direction of the transmitted light. A triangulation is then made using this direction and the position in the sensor image which corresponds to the direction of the incoming light. The peak amplitude is used for the intensity image.

Each sensor integration gives one complete range image. Hence every pixel in the 2D sensor must be read out in-between integrations. The use of a whole light sweep during each integration make the architecture cannot be used with a moving scene or apparatus since in such cases the one-to-one mapping between offset position (direction of incoming light) and time (direction of transmitted light) does not hold. In Figure 1 for instance, if the

scene is one-dimensional along the axis of movement the light will be projected onto the same line during the whole integration.

Due to the extensive hardware in each cell this design is very hard to implement in standard VLSI. An undocumented recent report mentions a fabricated 32x32 array.

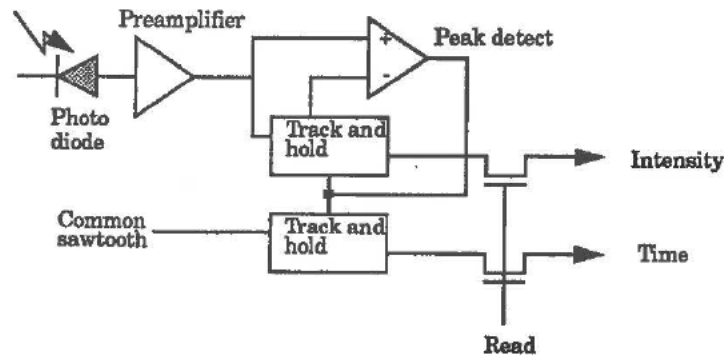


FIGURE 5. Sensor cell due to Kanade.

2.4 Peak Detection with column read-out

This architecture was originally described briefly in [2]. The principle is that after integration of one light position the analog values are read out column-wise, and the maximum and its position are obtained, see Figure 6. The peak detection circuits are somewhat similar to those described above in Figure 5.

An apparent disadvantage with this circuit is that it is impossible to do the light integration and the max detection in parallel without analog storage capabilities in the sensors (i.e. an analog shiftregister).

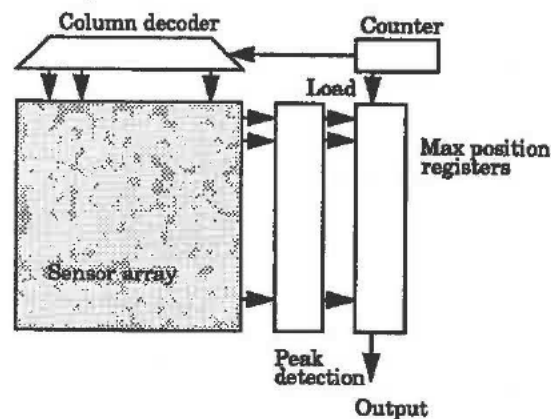


FIGURE 6. Column by column readout with peak detection.

The max detection circuits consists of a column of comparators which compare each row output with the previously recorded maximum intensity. If a new maximum is found, the analog value is saved in an analog register and the column position is saved in a max position register. This is showed in Figure 7. To obtain the intensity maximum value a D/A converter is connected to the comparator instead of the row output so that the maximum value found is compared with a ramp (staircase) signal. When the ramp signal reaches the value of the max register the counter value is loaded to a shiftregister as seen in Figure 7.

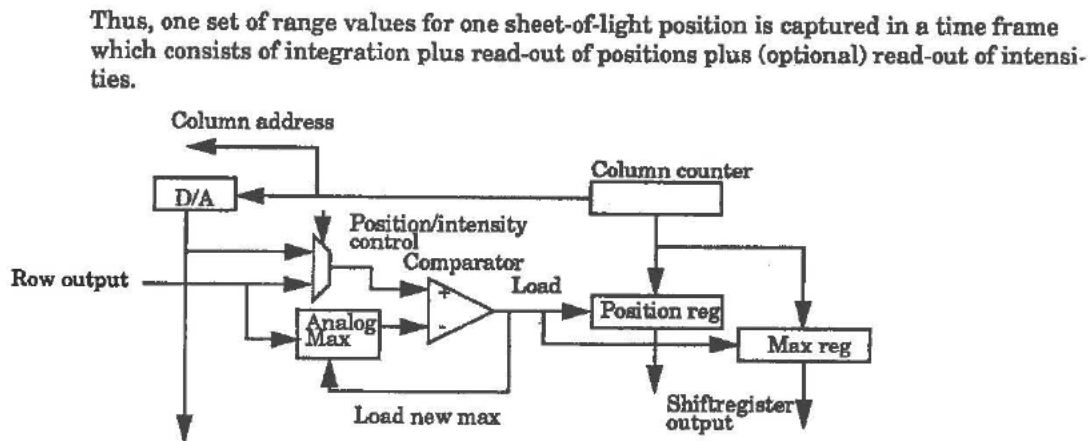


FIGURE 7. One peak detection circuit with maximum value output.

2.5 A row by row architecture

This architecture utilizes row-by-row readings of analog sensor data, see Figure 8. For each row of output we find the position median of the incoming light profile. The reason that this architecture measures the median rather than the maximum position is that it compares two sums of pixel values. The analog values from the sensor output are multiplexed and summed to one or the other of the two inputs of a comparator. The output of the comparator controls a sequential network of type successive approximation which moves the position median left or right. To get the output for a N bit row the network has to do $\log N$ approximations.

This design suffer from the same problem with sensitivity to background light as the PSD solution presented in section 2.2. Sensor integration and read-out can take place in parallel.

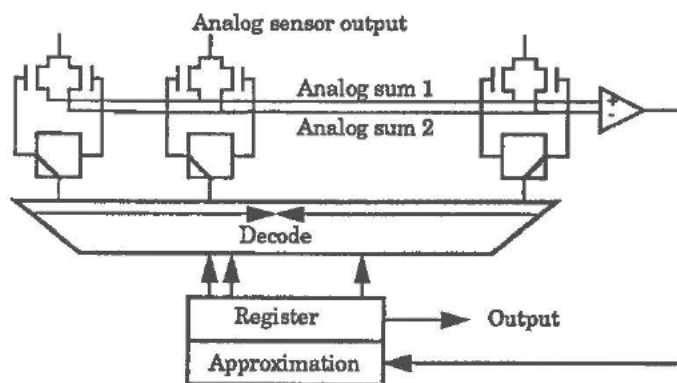


FIGURE 8. Row-by-row read-out with analog/digital processing to find the median position.

2.6 MAPP as a Range Image Sensor

In the MAPP2200, see [12], the sensor array is read one row at the time and the position of the maximum can be determined with a kind of successive approximation using all data from one row at the same time, see Figure 9. The relatively simple added off-chip hardware consists of the approximation logic. Initially, at time $t = 0$, the approximation register, i.e. the reference voltage, is set to $1000000_2 = 128_{10}$. If there is at least one position with a voltage over 128, the Global-OR will go high. If the Global-OR was high the next reference voltage will be set to $1100000_2 = 196_{10}$, otherwise the voltage will be set to $0100000_2 = 64_{10}$. Table 1 shows these steps for each t , where G_i stands for the Global-OR at time i . This procedure takes $O(b)$ cycles for a b bit digital output. If the special approximation hardware is used this figure is $2b+O(1)$. The intensity value is found in the approximation register after $t=8$.

The comparator output data is now a single *one* or (possibly several *ones*) representing the position of the peak amplitude. To obtain the leftmost *one* (a discussions on which signal to choose is found in section 3.3) the built in GLU, Global Logic Unit, functions *lfill* and *count* are used. The function *lfill* fill all registers to the right of the leftmost *one* with *ones*, and the function *count* counts the total number of *ones* in the registers.

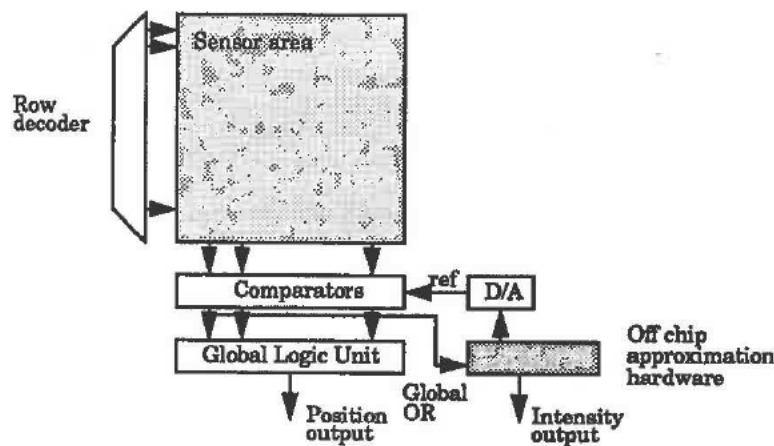


FIGURE 9. Using MAPP for sheet-of-light range imaging.

t	X7	X6	X5	X4	X3	X2	X1	X0
0	1	0	0	0	0	0	0	0
1	G0	1	0	0	0	0	0	0
2	G0	G1	1	0	0	0	0	0
3	G0	G1	G2	1	0	0	0	0
4	G0	G1	G2	G3	1	0	0	0
5	G0	G1	G2	G3	G4	1	0	0
6	G0	G1	G2	G3	G4	G5	1	0
7	G0	G1	G2	G3	G4	G5	G6	1
8	G0	G1	G2	G3	G4	G5	G6	G7

TABLE 1. The successive approximation scheme used with MAPP for sheet-of-light range imaging. X7 is the msb of the approximation and X0 is the lsb.

3 Near Sensor Image Processing

3.1 The basic Element

In Near Sensor Image Processing [1] (NSIP), the individual sensor operation is an integrated part of the signal processing algorithm. The basic NSIP element is shown in Figure 10A. The incoming light will induce a current, proportional to the intensity, in the diode. The time from the precharge of the diode to the time the diode voltage passes the reference voltage of the comparator is inversely proportional to the light intensity, see Figure 10B.

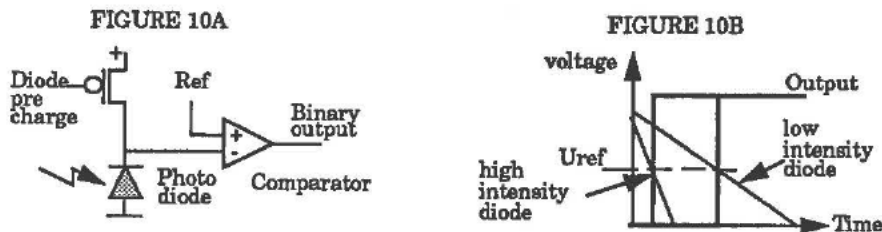


FIGURE 10. The NSIP design. Figure 10a shows the schematic of the diode and comparator. Figure 10b shows the output as a function of time and intensity.

3.2 The sensor cell

The design of a complete individual sensor cell for the sheet-of-light application can be seen in Figure 11. Please note that this is a principal sketch and not a complete circuit drawing. The sensor area consists of a two-dimensional array of sensor cells who are interconnected via inhibit and output buses. The output bus is horizontal or vertical depending on if data is read-out one column or one row at the time.

The integration starts after the photo diode has been precharged. As mentioned, it is then discharged proportionally to the incoming light intensity. When the first photo diode in the row is discharged to the point where the value goes below the reference voltage, the comparator switches, and the inhibit bus goes low from its precharged high. Thus, at this moment all sensors in the row are forced to freeze their potentials at C. Interpreted as binary signals these values are zero except for the cell with the highest intensity (and which took command over the inhibit bus). When the transfer transistors are enabled the output data are moved from the first inverter to the second, and a new integration can begin in the photo diodes. The readout is then made one row or column at a time concurrent with the next integration cycle in the sensors.

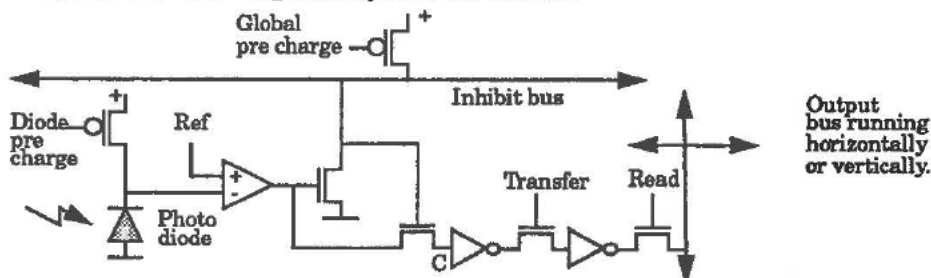


FIGURE 11. A complete single cell in the sensor array. The inhibit bus is precharged high. The output bus is vertical or horizontal depending on if row-wise or column-wise read-out is incorporated.

3.3 Global architecture

The presentation of the global architecture is divided into three parts. The first two describe two possible implementations for the range data readout from the sensor while the last part describes the logic to obtain intensity images.

The problem with several sensor cells in one row set to one is a difficult one. In three different solutions the output is reduced to the leftmost position, the median, and the centroid respectively. Which version is the most appropriate have not been thoroughly investigated. For now the global logic is assumed to take the leftmost position. This decision logic also has to handle the case when no output is found, i.e. when the scene is shadowed.

Column read-out

A global architecture with column-by-column readout is showed in Figure 12. In the read-out the columns are addressed one at the time and if a *one* is found the column address is saved in a shiftregister for that row. If several *ones* are found the last (leftmost) will be saved in the register. Thus, when all columns have been addressed the position registers will contain the addresses for the maximum intensity positions for each row. The problem with no sensor output can be solved by pre-loading the max position registers with a special code. The registers are set up as pairs to enable full concurrency. After each complete column read-out the data are copied to the second pair of registers and then shifted during the next column readout.

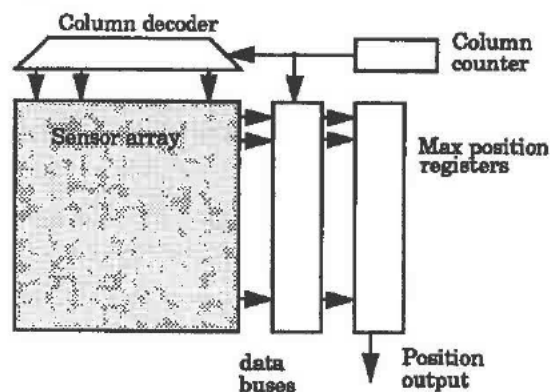


FIGURE 12. A global architecture with column readout.

Row read-out

A global architecture with row-by-row readout of position data is showed in Figure 13. From the 2D-array of sensors, binary data is read one row at a time, and the binary code of the position of the single *one* is obtained with an encoder. The encoder work by letting each signal from the sensor control an enable signal to switch the appropriate address to the output bus. This hardware also has to handle the case when more than one sensor position is set to one, and this is done in the *multiple-ones-blocking-circuit*, which inhibits all but the leftmost one. The case when no single position is set also has to be treated, and this can be done by having a dummy output last which always is one, and which is interpreted as no signal by the following signal processing.

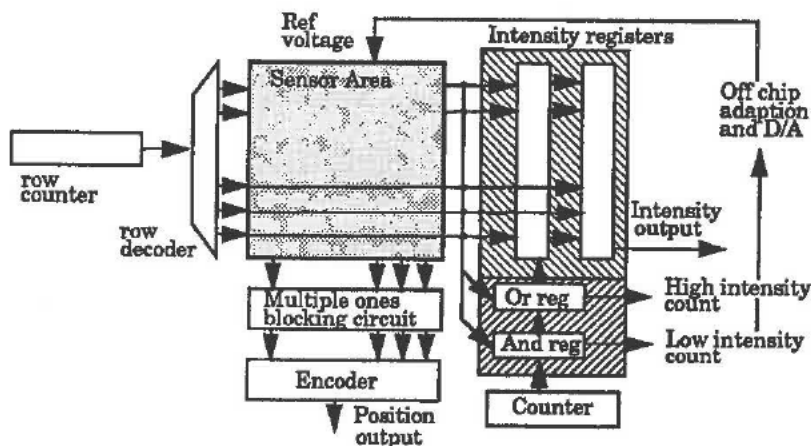


FIGURE 13. The global architecture for row read-out. The area marked by down-slanting lines is the intensity image circuit, and the area marked by up-slanting lines is the circuits for adaption to different light levels.

Intensity image logic

The time from the start of the integration to the activation of the inhibit bus is inversely proportional to the light intensity in the maximum intensity position. This intensity depends on the reflectance (brightness) of the surface swept by the sheet-of-light. A full reflectance map, an intensity image, can be obtained as follows by the area which is marked by down-slanting lines in Figure 13. A counter is started when the sensors are activated, and when the inhibit bus of a certain row is triggered the corresponding register is loaded with the counter value. These registers are then addressed simultaneously with the row output so that both the position and its intensity value are output concurrently. To be able to use this design concurrent with the integration, the registers have to be doubled so that one set of registers can be loaded from the inhibit bus while the other set is used for output.

To facilitate automatic adaption of the reference voltage (integration time) extra hardware is incorporated in the design shown in the area which is marked by up-slanting lines in Figure 13. The adaption is based on the integration times for the first and last row to reach the reference voltage. These can be detected by taking a *Global-OR* and *Global-AND*, respectively, of the inhibit bus signals. The OR function will react for the first transition, the AND function for the last. To get the best signal-to-noise ratio, the integration times should be as long as possible. This means that for optimization, the reference voltages should be lowered as much as possible without missing a row with a low but still significant illumination.

3.4 Sensor cell variations

Clocking the sensor output

To get a discrete digital behavior from the sensor output, clocking can be applied on the inhibit bus control as seen in Figure 14. By clocking ϕ_1 before ϕ_2 it is always insured that data have time to reach the memory cell before the hold transistor can switch off.

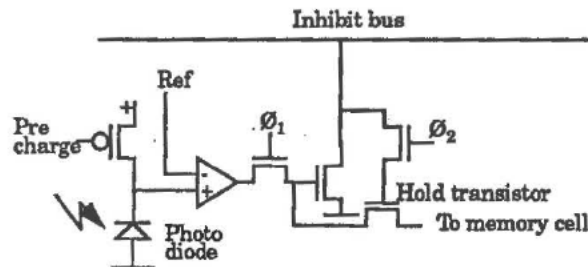


FIGURE 14. A clocked version of the sensor cell. The clock is two phase non-overlapping.

The comparator design

The comparator can be realized as in Figure 15. The bias voltage come from a global transistor, and the comparator is a current mirror sense amplifier with an inverter output. The inverter amplifies the signal level.

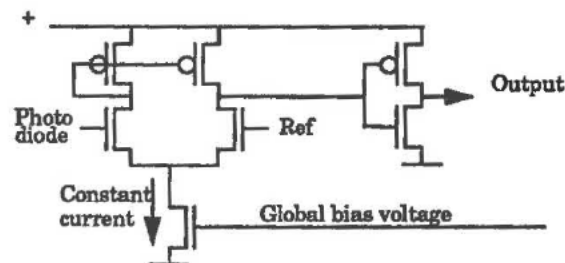


FIGURE 15. A current mirror comparator, with reservation for the polarity of the output.

The sensor cell can be implemented without a comparator which is interesting since the comparator is large and has high power consumption. The major power dissipation in the comparator comes from the constant bias current flowing in the current mirror. To overcome this, the current mirror is removed and the threshold is controlled indirectly by charging the photo diode to different values and using a fixed threshold.

A design using a precharged/clocked inverter switch is shown in Figure 16. This switch works by sensing the photo diode voltage in each clock cycle, and if the diode voltage has sunk below the threshold of the switch transistor it will charge the output to high when the clock goes low. This implies that the following circuits also be adapted to a precharge situation. The output will always be precharged to low.

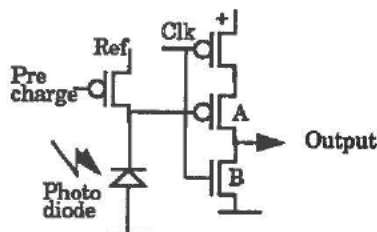


FIGURE 16. A comparator with a clocked inverter.

Inhibit bus design

The inhibit bus suffers from problems with large capacitive load and thus long switching times. One way to obtain sufficient speed is to use a double bus structure as seen in Figure 17. This architecture is from page 363 in Principles of CMOS VLSI design [9] and is designed for fast memory readout. The idea is to use a global sense amplifier to detect inhibition, amplify the signal, and feed it back to all sensor cells in the row.

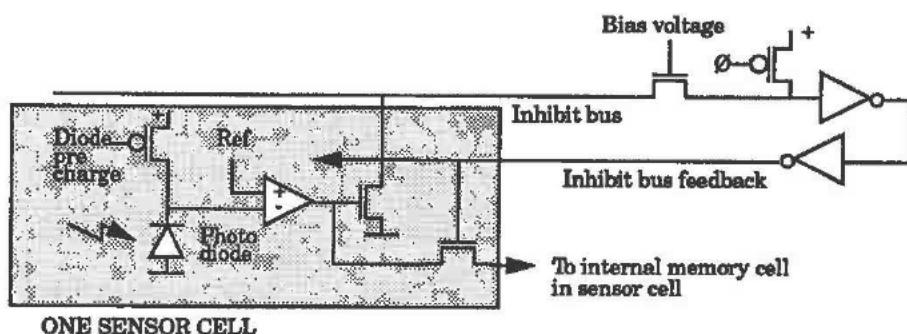


FIGURE 17. Realization of the inhibit bus with memory logic readout.

3.5 Size estimations

With 20 transistors in each cell, a 128x128 implementation would give 330 000 transistors, which is feasible. A 128x128 realization on a 10x10 mm chip would leave approximately 80x80 μm for each cell. In the currently available CMOS process, with $\lambda = 0.8 \mu\text{m}$, the sensor diode takes up approximately 25x25 μm and the comparator 60x160 μm (Values from MAPP [12]). Transposed to a quadratic cell this give approximately 100x100 μm , and a total area of 13x13 mm. The digital parts can be made very small since most of these can be implemented with minimum sized transistors.

4 Increasing the aperture

All smart sensors have problems to utilize the whole sensor area for light absorption. The percentage of active sensor area should be maximized to get a good signal to noise ratio. A radical but difficult solution is to bury the processing circuitry below the sensors in a 3-D structure.

Another way to utilize the whole sensor cell area effectively for light absorption is to apply a micro lens over each sensor cell, see Figure 18. A micro lens collects the incoming light over the whole cell area and concentrates it onto the photo diode. This design is used by Sony in their video camera design and the lens is made by SiO_2 as a part of the total VLSI process. A micro lens structure should also be possible to apply to the chip after the VLSI process.

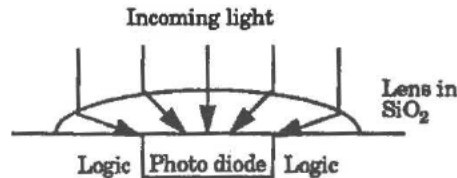


FIGURE 18. A micro lens cell architecture.

5 Comparisons

5.1 Speed

The architectures which can integrate and output data simultaneously can obtain higher frame rates than those who cannot. Both the row-by-row architecture and MAPP use a standard photo diode sensor array that can integrate light in parallel with readout but the row samples will get skewed in time, see Figure 19. The PSD solution will also result in skewed samples. Time skewed samples result in an image which will be skewed when presented without interpolation of the light direction since the direction of the transmitted light varies over the range image row. Only the NSIP design can do non interlaced integration and simultaneous image readout. Furthermore, the NSIP design has the sensor integration time and not the signal processing as a speed bottleneck.

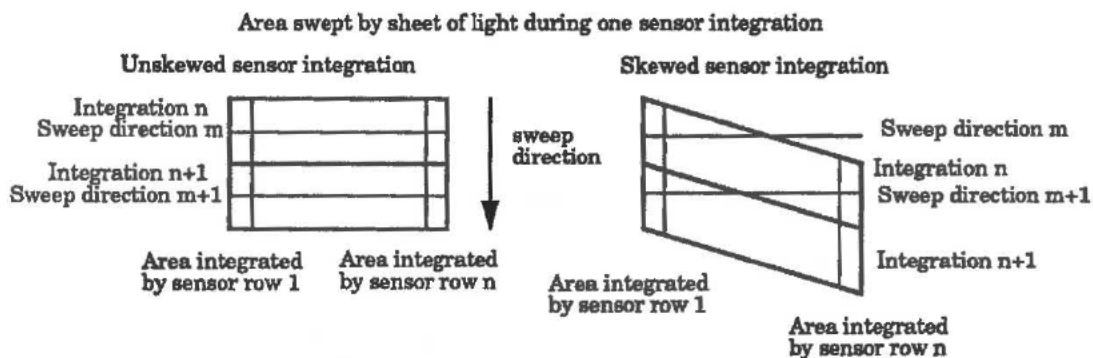


FIGURE 19. Integration scheme, unskewed compared with skewed. The light is considered illuminating a flat surface to simplify the figure.

5.2 Noise sensitivity

The NSIP architecture have digital data transports which is less noise sensitive at high clock frequencies than the analog transfers in the other designs. Both the PSD and the row-by-row readout architectures compute the center of gravity of the incoming light rather than the position of the maximum. This should make them sensitive to background illumination. The NSIP design automatically adapts for different light intensities and the risk of sensor saturation is very low.

5.3 Complexity

The architecture proposed by Kanade is the most complex one with the double analog registers in each sensor cell. The NSIP design is also quite complex but we believe that it is possible to fabricate working sensors with standard CMOS VLSI design. Furthermore, the NSIP design does not need any analog hardware outside of the sensor area which makes it rather VLSI friendly.

5.4 Versatility

The NSIP architecture, the Kanade architecture, the Peak Detection architecture and MAPP can all output grey level reflectance images concurrently with the range data. Theoretically, the PSD architecture can output reflectance maps, but no reports of this are available. Intensity information is very useful for light adaption. The NSIP architecture automatically saves the minimum and maximum intensity values. As shown in Figure 13, they are primarily intended for control of the Ref voltage. However, in a more controlled environment they can be used to adjust the illuminator as well.

6 Conclusions

We have presented a new high speed solution for range imaging with sheet-of-light, and we have shown that it is competitive to previously reported designs. The key point is the row-wise max detector. We believe this solution is much simpler than most other designs e.g. the one suggested by T. Kanade [6]. We estimate that, using a CMOS process with $\lambda = 0.8\mu\text{m}$, 128x128 cells of the type shown in Figure 11 should fit on a 10x10mm chip. An image integration time of 50 μs gives a data readout of 2.5 M rangels per second. If a full range image is assumed to consist of 128x128 data points (rangels) these should be possible to acquire in 6.5ms, i.e. at a frame rate of 150Hz.

Our implementation efforts will focus on the sensor circuitry, especially the comparator, which poses a size reduction problem. Naturally, the area percentage of the sensor diodes must be kept as large as possible.

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