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Smart Vision Sensors

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Abstract

Smart Vision Sensors represent a niche in machine vision where high performance in terms of frame rates, processing speed, and flexibility is the most essential feature. With the integration of photosensitive devices with processing elements on one and the same substrate it is possible to reach high performance at low complexity and low cost. The MAPP2500 from IVP represents state-of-art in this development of CMOS imaging and on-chip processing.

1. Background

A Smart vision sensor can be defined by the integration of photosensitive devices with processing elements, usually on one and the same substrate, in such a way that the image processing technique is significantly influenced by this architecture.

In 1987 IVP Integrated Vision Products AB released such a device commercially, [1]. This was a 128 pixel line sensor with built-in SIMD processor. It was characterized by having a separate processor element for each pixel. Those processor elements were connected into a programmable single-instruction multiple-data (SIMD) array. This device was followed in 1991 by the two-dimensional MAPP2200-device, [2], characterized by a 256x256 photo-diode sensor and an array of 256 processing elements, one for each column. Later on the family of Smart Vision Sensors were extended with a 512 pixel line sensor and a 512 X 32 multi-linear sensor, all of them characterized by the same basic SIMD architecture.

During these 10 years of existence, IVP's CMOS-based Smart Vision Sensors have found their use in numerous applications, from sorting of potatoes to space applications. The technology has shown its power particularly in high-speed applications, in low power applications and in harsh environments.

2. MAPP2500 - A 512 X 512 Smart Vision Sensor

Scheduled for release in 4Q98, the latest development along these lines, the MAPP2500 represents state-of-art, with regard to CMOS sensing and SIMD processing architecture. With its 512 X 512 photo-diode matrix it can be used in virtually all machine vision applications as well as for surveillance, and image communication systems. Compared to traditional system concepts based on CCD sensing and separate signal or PC processor the new component enables higher performance in a smaller package and at considerably lower power levels.

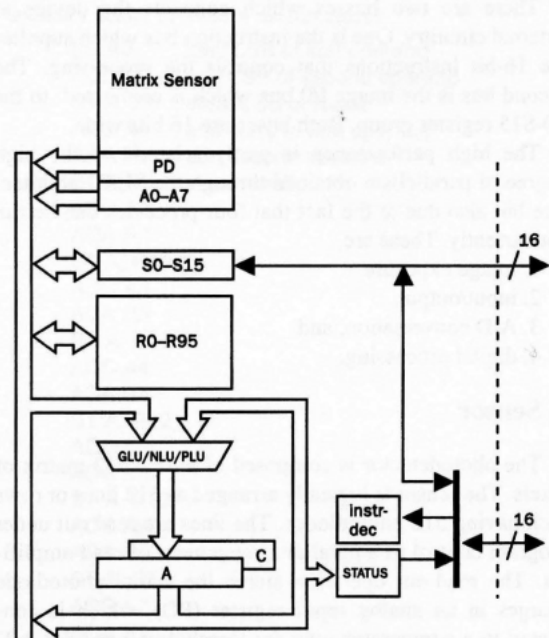


Figure 1. Architecture of the MAPP2500 Smart Vision Sensor.

3. Architecture

The architecture of MAPP2500 is shown in figure 1. The sensor array is connected to read-out circuitry and to an A/D-converter which performs parallel conversion of one image row in 4-16 microseconds depending on the selected gray-level resolution (1-8 bits). Image information can be internally stored in one of the 96 general purpose registers (R0-R95) or the group of specific registers (S0-S15). All of these registers have a length of 512 bits to allow one bit-plane of a complete image row to be handled in parallel. Operations on register data can be done with point, neighborhood or global operators through dedicated logical units (PLU, NLU, GLU). The result of such an operation is placed in the accumulator A and/or the register C, and can be stored in any of the registers or used for subsequent operations.

After each operation the number of set positions of the accumulator is updated. This number, called COUNT, is available in the status register.

The special register group is used also for input and output. In this mode 16 registers are altered simultaneously to produce or receive a 16 bit word at a given position along the line.

There are two busses which connects the device to external circuitry. One is the instruction bus which supplies the 16-bit instructions that controls the processing. The second bus is the image I/O bus which is connected to the S0-S15 register group. Both busses are 16 bits wide.

The high performance is partly related to the high degree of parallelism obtained through the SIMD architecture but also due to the fact that four processes can be run concurrently. These are,

1. image exposure,
2. input/output,
3. A/D conversion, and
4. digital processing.

4. Sensor

The photodetector is composed of a 512x512 matrix of pixels. The sensor is logically arranged as 512 lines or rows each having 512 photodiodes. The lines are read out under program control to a parallel arrangement of read amplifiers. The read-out operation stores the actual photodiode charges in an analog input register (PD), which is connected to a comparator used for thresholding and for A/D conversion.

The design of the read amplifiers is shown in Figure 2. Each amplifier serves a column of 512 photodiodes via a common busline. The specific photodiode row is defined by instructions or an auto-increment option. Once a specific row is defined, the analog operations are performed

simultaneously on all photodiodes in that row. The operations are defined by the various combinations of switch settings in the read-circuitry. The four basic combination options are, see Figure 2,

- reset on and pon off resets the input register PD
- reset on and pon off resets the input register and the photodiodes
- integ on and pon on transfers the charge from the photodiode to the input register
- integ on and pon off holds the charge in the input register

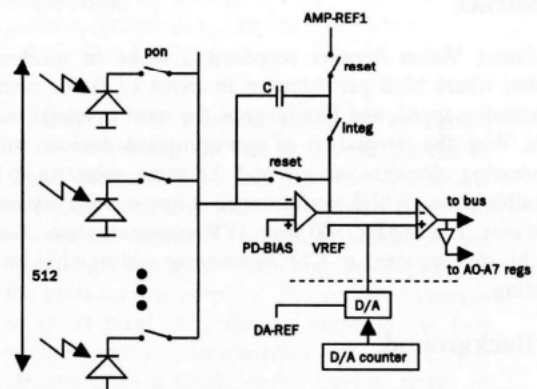


Figure 2. Image sensor architecture; photodiodes and read-out circuitry.

Once a specific row is defined, the analog operations are performed simultaneously on all photodiodes in that row.

With this setup the resulting charge after exposure may be read out to the charge amplifier or accumulated with previous read-outs to perform analogue preprocessing before digitization. Since also the addressing of sensor rows can be done in any order, it is possible to use different exposure-times for different groups of rows.

The spectral sensitivity follows the characteristic curve for silicon with a peak sensitivity at a wavelength of 750 nm.

5. Instruction set

The instruction set comprises some 80 different instructions. All of them operates on complete lines and, except the eight GLU instructions, completes in one clock cycle. The GLU instructions uses two cycles. A special instruction format controls the sensor and read-out circuitry.

The arithmetic is performed by the three logical units PLU, NLU, and GLU. The PLU instructions are bitwise boolean algebra operators executed on data local to each pixel.

In the NLU the pixel values are processed in a way determined by the pixel's nearest neighbors such as template matching or filtering operations which reduce noise

or enhance edges. Each position in the input register is compared with a 3-element mask. A logical one (1) in a specific position of the output picture indicates neighborhood agreement between the input picture and the mask. Since 1's and 0's as well as X's (don't care) are valid mask values, there are 27 possible mask combinations. For example, the left edge of a binary image line can be detected using the mask (01x). Figure 3 shows the input and resulting output of this NLU operation which has been named LEDGE.

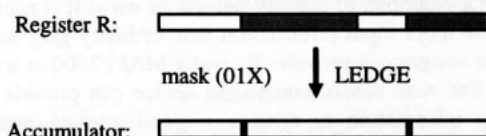


Figure 3. NLU operator example; detection of left edges.

An example of a common operator for binary image processing is the MARK instruction shown in figure 4. This operator will compare two image lines and extract those "objects" (represented in black) in register A, the accumulator, that has at least one corresponding object pixel in register R. Thus, this operator checks for "vertical" connectivity between objects in two image lines.

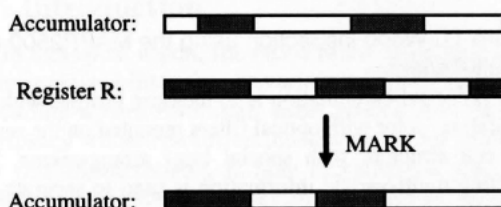


Figure 4. GLU operator example; marking of connected components.

Another very useful GLU operation is LFILL. This instruction fills the array with ones from the leftmost object towards the right. See Figure 5.

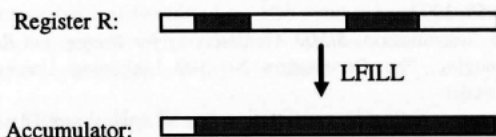


Figure 5. LFILL Instruction. The accumulator is filled with ones from the leftmost object to the right border.

The power of the logical units can be illustrated by a simple program for run-length coding depicted in Figure 6. The program uses the PLU, NLU, and GLU instructions exemplified above.

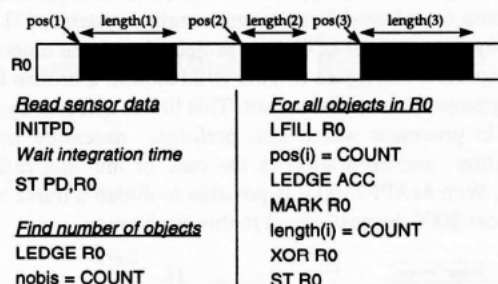


Figure 6. Processing example showing run-length coding of binary objects.

Processing of gray-level information is performed through bit-serial arithmetic which uses groups of registers to hold the operands. Figure 7 shows the routine to add two image rows, each digitized with 8-bit resolution. As is shown, 25 cycles are needed to perform the 512 additions along the line, leading to an "architecture advantage" of more than a factor of 20 for this type of operation over ordinary scalar processor architectures.

```
LD A0 ; load LSB of first operand
ADD R0 ; add LSB of second operand
ST A, R8 ; store LSB of result
ADC A1 ; add carry to first operand
ADA R1 ; add second operand
ST A, R9 ; store result
ADC A2
ADA R2
ST A, R10
ADC A3
ADA R3
ST A, R11
ADC A4
ADA R4
ST A, R12
ADC A5
ADA R5
ST A, R13
ADC A6
ADA R6
ST A, R14
ADC A7
ADA R7
ST A, R15
ST C, R16; Store carry
```

Figure 7. Addition of two 8-bit grayscale numbers.

6. Applications

6.1. 3D Profiling

Among the many application areas, the new sensor is believed to enhance laser range imaging systems, [3]. In such systems a sheet-of-light is projected onto the object to be inspected, see figure 8. This will result in a broken line being projected onto the sensor. This line is detected by the built-in processor which also performs necessary noise reduction and arbitration in the case of multiple reflections. With MAPP2500 it is possible to obtain a frame rate of about 2000 frames/second in this application.

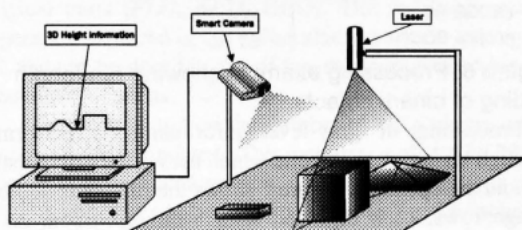


Figure 8. 3D-profiling application.

By assuming that the laser line position on the sensor is represented by the centroid of the binary input image a complete profiling algorithm can be implemented using only 4 instructions and two status register readouts of the MAPP2500 per range pixel. See Figure 9. Each processed frame results in one 512-element height profile.

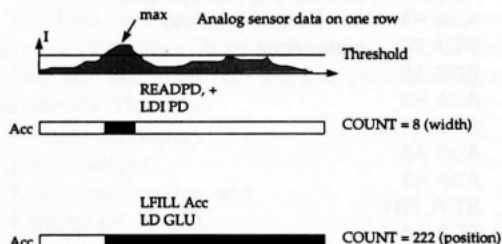


Figure 9. Algorithm for 3D-profiling

As illustrated in Figure 10 this algorithm can easily be extended with an error detection feature. By utilizing the LEDGE instruction it is possible to obtain the number of peaks found on each sensor row.

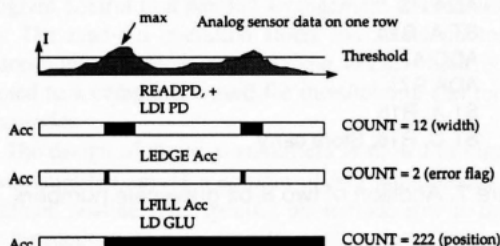


Figure 10. 3D-profiling with multiple peak detection.

6.2. Multi-sensor

Another possibility which opens up is to use the device in "multi-sensor" applications. Specifically called for in the wood inspection industry. Here different areas of the sensor is used for different purposes. Thus, a group of image lines are used for range imaging while another group is used for color-separated sensing etc. This means that one and the same camera is able to perform several different tasks, something that will considerably lower the price of an inspection system.

For example, to classify defects in wood it is necessary to use more input information than ordinary gray scale or color images can provide. By using MAPP2500 as a multiple line scan sensor one single device can provide sufficient information to achieve a good grading result on different types of boards.



Figure 11. Wood inspection using the MAPP2500 as a multi-sensor.

A powerful combination is to measure profiles with triangulation, color with optical filters mounted on the sensor and cell structure with special laser arrangements. The resulting multi-variate information is used to separate dirt from knots and to detect defects previously not possible to classify, [4].

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