

Petition for *Inter Partes* Review of U.S. Patent 7,523,373  
Claims 1-13 and 15-16

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Filed on behalf of Intel Corporation

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UNITED STATES PATENT AND TRADEMARK OFFICE

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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Intel Corporation  
Petitioner

v.

VLSI Technology LLC  
Patent Owner

Case IPR2020-00158

**PETITION FOR *INTER PARTES* REVIEW OF  
U.S. PATENT NO. 7,523,373  
CHALLENGING CLAIMS 1-13, 15, and 16  
UNDER 35 U.S.C. § 312 AND 37 C.F.R. § 42.104**

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## **I. INTRODUCTION**

Intel Corporation (“Intel” or “Petitioner”) respectfully requests *inter partes* review of claims 1-13 and 15-16 of U.S. Patent No. 7,523,373 (the “’373 patent”) (Ex. 1001) pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42.1 *et seq.*

## **II. MANDATORY NOTICES**

### **A. Real Party-in-Interest**

Intel Corporation is the real party-in-interest.

### **B. Related Matters**

VLSI Technology LLC (“VLSI” or “Patent Owner”) has asserted the ’373 patent against Intel in *VLSI Technology LLC v. Intel Corporation*, Case No. 1-19-cv-00254-ADA (consolidated as 1-19-cv-00977) (W.D. Tex.). That case is currently pending.

### **C. Counsel**

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Claims 1-13 and 15-16

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Petitioner consents to email delivery on lead and backup counsel.

### **III. CERTIFICATION OF GROUNDS FOR STANDING**

Petitioner certifies pursuant to Rule 42.104(a) that the patent for which review is sought is available for *inter partes* review and that Petitioner is not barred or estopped from requesting an *inter partes* review challenging the patent claims on the grounds identified in this Petition.

### **IV. OVERVIEW OF CHALLENGE AND RELIEF REQUESTED**

Pursuant to Rules 42.22(a)(1) and 42.104(b)(1)-(2), Petitioner challenges claims 1-13 and 15-16 of the '373 patent.

#### **A. Prior Art Patents and Printed Publications**

The following references are pertinent to the grounds of unpatentability explained below:<sup>1</sup>

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<sup>1</sup> The '373 patent issued from a patent application filed prior to enactment of the America Invents Act ("AIA"). Accordingly, the pre-AIA statutory framework applies.

Petition for *Inter Partes* Review of U.S. Patent 7,523,373  
Claims 1-13 and 15-16

1. U.S. Patent No. 5,867,719 (“Harris”) (Ex. 1003), which issued on February 2, 1999, is prior art under at least 35 U.S.C. § 102(b).
2. U.S. Patent Application Publication No. 2006/0259840 (“Abadeer”) (Ex. 1004), filed on May 12, 2005, and published on November 16, 2006, is prior art under at least 35 U.S.C. § 102(e).
3. U.S. Patent Application Publication No. 2003/0122429 (“Zhang”) (Ex. 1005), published on July 3, 2003, is prior art under at least 35 U.S.C. § 102(b).
4. U.S. Patent No. 7,702,935 (“Cornwell”) (Ex. 1006), filed on January 25, 2006, and issued on April 20, 2010, is prior art under at least 35 U.S.C. § 102(e).
5. U.S. Patent Application Publication No. 2005/0188230 (“Bilak”) (Ex. 1007), published on August 25, 2005, is prior art under at least 35 U.S.C. § 102(b).

**B. Grounds for Challenge**

Petitioner requests cancellation of claims 1-13, 15, and 16 of the ’373 patent as being unpatentable under 35 U.S.C. § 103. This Petition, supported by the declaration of Dr. Adit Singh (Ex. 1002),<sup>2</sup> Professor of Electrical Engineering at

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<sup>2</sup> This Petition is also supported by the declaration of Dr. Sylvia Hall-Ellis (Ex. 1027) demonstrating the public availability of certain exhibits cited herein.

Auburn University, demonstrates that there is a reasonable likelihood that Petitioner will prevail with respect to cancellation of at least one challenged claim and that each challenged claim is not patentable. *See* 35 U.S.C. § 314(a). The grounds for challenge are:

	Ground	References	Challenged Claims
1.	§103	Harris in view of Abadeer and Zhang	1-7, 9-11, 13, 15-16
2.	§103	Harris in view of Abadeer, Zhang, and Cornwell	2, 11-12
3.	§103	Harris in view of Abadeer, Zhang, and Bilak	8

**V. DISCRETION UNDER 35 U.S.C. §314(a) AND §325(d)**

The '373 patent is one of 21 patents asserted by VLSI against Intel in five cases spanning three venues: *VLSI Technology LLC v. Intel Corporation*, Nos. 6-19-cv-00254, -255, -256 (W.D. Tex.), 18-966-CFC (D. Del.), and 5-17-cv-05671 (N.D. Cal.). More specifically, the '373 patent is asserted in 19-cv-00254, one of three parallel cases consolidated until trial (as 1-19-cv-00977) in the Western District of Texas.

Intel is diligently pursuing its defenses, including invalidity, in the district court; however, *inter partes* review is a more efficient and expedient forum in which to adjudicate validity. **First**, the '373 patent involves the technical subject matter of integrated circuits and electrical engineering, and is thus well-suited to

the expertise of the specialized patent judges at the PTAB. **Second**, VLSI is currently asserting at least 12 claims of the '373 patent against Intel. Compared to the PTAB, a jury trial is necessarily a more difficult forum for presenting a detailed obviousness case for this number of asserted claims, especially for the multi-reference obviousness combinations presented herein. **Third**, the three Western District of Texas actions are currently set for jury trials starting the same day (October 5, 2020) before the same Court, even though they have not been consolidated for purposes of trial. Therefore, it is unclear which of these trials (and patents) will proceed on October 5, 2020, and what the schedule for the other two trials might be. **Fourth**, even following a jury verdict, the time required for briefing and resolution of post-trial motions could easily result in a Final Written Decision before the district court's final appealable judgment is docketed. **Finally**, this Petitioner was diligent in timely filing this Petition. The statutory bar date is more than four months away, and Petitioner diligently filed this Petition within six weeks of VLSI's October 9, 2019, unauthorized service of amended Preliminary Infringement Contentions, in which VLSI first charted seven additional claims (4, 5, 9, and 11-14) against Petitioner's products, and within two weeks after VLSI



filed a motion to amend its infringement contentions to add those new claims to its infringement contentions.<sup>3</sup>

Petitioner respects the limited resources of the Board, but because *inter partes* review would be a more effective and efficient alternative to litigation under the present circumstances, and because Petitioner has been diligent in pursuing this relief, and in light of the substantive grounds discussed below, Petitioner requests that the Petition be granted. Petitioner may request additional briefing if Patent Owner urges the Board to exercise its discretion to deny this Petition under 35 U.S.C. §§ 314(a) or 325(d).

## **VI. BRIEF DESCRIPTION OF TECHNOLOGY**

The '373 patent relates to a purported improvement in providing regulated voltages to a memory. Ex. 1002, ¶ 29.

### **A. Common Components of an Integrated Circuit**

Integrated circuits containing processors and memory have been known in the art for decades. Ex. 1008. Such circuits integrate “the major functional elements of a complete end-product into a single chip or chipset.” *Id.*, 3. In such circuits, the processors execute instructions whereas the memory stores data. Ex.

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<sup>3</sup> The deadline to file “Final Infringement Contentions” is not until January 31, 2020.

1009, 372-390. For example, memory can store data that a processor uses to execute its instructions. *Id.* Memory can be volatile or nonvolatile. Nonvolatile memory continues to retain information after being powered down; volatile memory does not. A fuse is an example of nonvolatile memory. Dynamic random access memory (DRAM) and static random access memory (SRAM) are examples of volatile memory. Ex. 1002, ¶ 30.

### **B. Operating Voltages of an Integrated Circuit**

Long before the '373 patent, the concepts described therein were well-known. It was known to vary voltages provided to different elements (e.g., processor and memory) within integrated circuits. Ex. 1010, ¶ 0047. For example, U.S. Patent Application Publication No. 2005/0077919 ("Sowden") describes varying the voltage to different elements in an integrated circuit, often called "dynamic voltage scaling," and explains that by varying the voltage, the frequency (clock speed) of the elements in the integrated circuit can also be varied. *Id.*, ¶ 0006. Increasing the voltage to an element allows that element to operate faster (but uses more power) when higher performance is needed, whereas reducing the voltage to an element slows operation (but reduces power consumption) when faster processing is not needed. Sowden explains that reducing supply voltage to different elements reduces energy consumed, significantly enhancing battery life. *Id.* Ex. 1002, ¶ 31.

It was also known long before the '373 patent that different elements in an integrated circuit may have different ranges of operational voltages. The lowest voltage at which an element can effectively operate is sometimes referred to as its “minimum operating voltage.” Ex. 1011, Abstract. This was nothing new in the early 2000s. In fact, circuit designers had been aware of minimum operating voltages of elements such as memory since at least 1980. For example, U.S. Patent No. 4,461,003 explains that a “read-write memory is usually arranged to be disabled before the power voltage drops below the minimum operating voltage of the memory.” Ex. 1012, 1:45-50. It was also well-known that different elements may have different minimum operating voltages. For example, it was known that memory could have a different minimum operating voltage than a processor. *See* Ex. 1010, ¶ 0024 (constraint on the voltage supplied to the memory is higher than the voltage supplied to the processor). Ex. 1002, ¶ 32.

Given the conventional understanding of “minimum operating voltage” of memory, it was also known long before the '373 patent that while power can be saved by reducing the memory’s voltage in an integrated circuit, the voltage should remain at least as great as the memory’s minimum operating voltage. In fact, by the 1990s, a well-known technique for saving power involved reducing voltage supply to a memory circuit to its minimum operating voltage to (1) consume the least amount of power, while (2) ensuring that the memory functioned correctly.

For example, U.S. Patent No. RE37,593 explains that the voltage provided to the memory can be “reduced to a necessary and minimum value” to both retain data and reduce power consumption. Ex. 1013, 3:28-43. Similarly, U.S. Patent No. 4,709,202 discloses a battery-powered system that maintains a minimum voltage for the memory such that data is retained even if the central processing unit is not able to operate. Ex. 1014, 5:44-59. Ex. 1002, ¶ 33.

**C. Testing the Integrated Circuit to Determine its Minimum Operating Voltages**

Circuit designers had also known decades before the '373 patent that manufacturing variability may cause the minimum operating voltages on integrated circuits to vary from one integrated circuit to the next. Accordingly, the need to test each integrated circuit to determine its individual minimum operating voltage has long been known. For example, U.S. Patent No. 4,553,225, which claims priority to 1981, taught adjusting a power-supply voltage to determine “a minimum data-holding limit voltage” for the memory in an integrated circuit. Ex. 1015, Abstract. Likewise, U.S. Patent No. 6,697,978, discloses performing voltage (“minimum Vdd”) testing in processors to “test for minimum operating conditions.” Ex. 1016, 9:8-11. Ex. 1002, ¶ 34.

Further, by at least the 2000s, techniques for testing memory to determine its memory-specific minimum operating voltage were well-known. U.S. Patent No.

7,142,996, for example, discloses “executing a test sequence ... on said integrated circuit ... [and] *identifying a lowest test voltage* ... for which said test sequence was successfully executed.”<sup>4</sup> Ex. 1017, 1:37-46, 8:53-59. And U.S. Patent No. 7,276,925 discloses testing the memory in an integrated circuit to determine a “measured voltage [that] may be *the lowest measurable voltage that results in correct operation.*” Ex. 1018, 4:3-11. Accordingly, these concepts were well-known long before the ’373 patent. Ex. 1002, ¶ 35.

Finally, it was also well-known to store the minimum operating voltages of an integrated circuit, including the minimum operating voltage of the memory in non-volatile memory. For example, Abadeer discloses a “solution for determining minimum operating voltages” for various components in an integrated circuit and storing those minimum operating voltages in non-volatile memory, such as fuses. Ex. 1004, Abstract, ¶¶ 0045-0046. Ex. 1002, ¶ 36.

## VII. OVERVIEW OF THE ’373 PATENT

The ’373 patent describes “a minimum memory operating voltage technique.” Ex. 1001, 1:6-8. As described below, however, the claimed technique was obvious by 2006. Ex. 1002, ¶ 37.

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<sup>4</sup> All emphasis added unless otherwise noted.

**A. The Alleged Problem in the Prior Art**

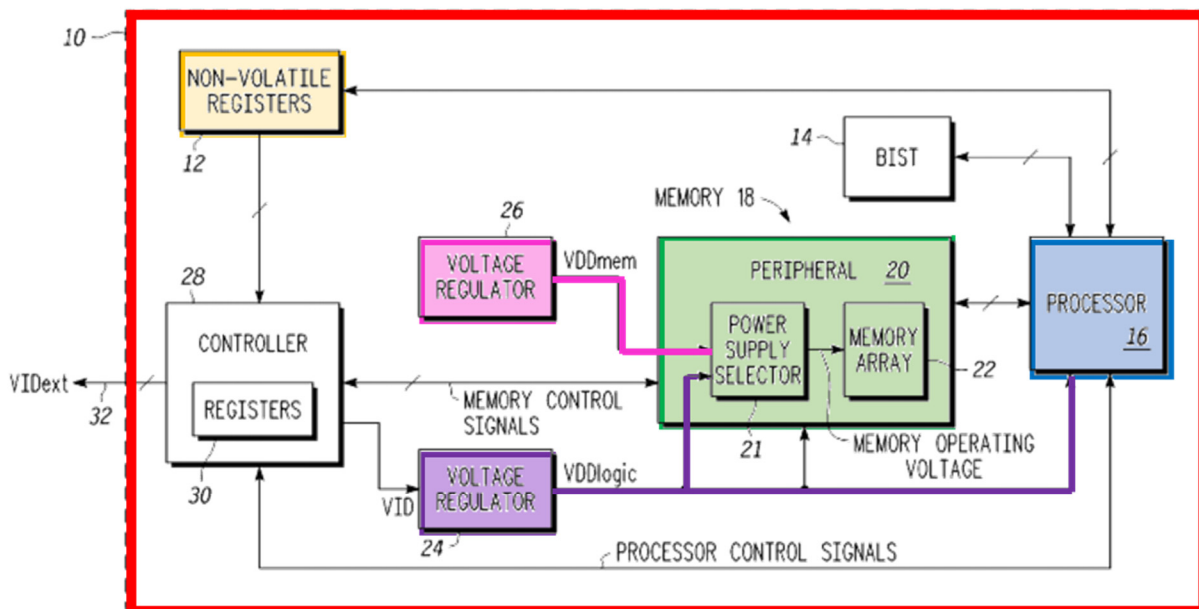
The '373 patent purports to address the well-known challenge of “tradeoffs between performance and power,” by operating processors “at maximum voltage and frequency when peak performance is required,” and “at a low voltage and frequency to reduce power consumption” at other times. Ex. 1001, 1:12-20. The patent discusses the allowable ranges in which these voltages may fluctuate: “different types of circuitry within a data processing system may have different ranges of allowable operating voltages.” *Id.*, 1:23-25. Further, “the processor may be able to operate at a lower voltage than is possible for the memory.” *Id.*, 2:5-7. The '373 patent also recognizes the well-known concept that “the minimum operating voltage for a memory varies across parts, such that one integrated circuit (IC) may tolerate one minimum operating voltage while another IC may be able to tolerate even a lower operating voltage.” *Id.*, 2:17-22. Ex. 1002, ¶ 38.

**B. The Alleged Invention of the '373 Patent**

The '373 patent claims are directed to two basic concepts: (1) determining and storing a memory's minimum operating voltage; and (2) ensuring that the voltage provided to the memory does not fall below that minimum operating voltage, even when the voltage provided to logic (e.g., a processor) fluctuates below that threshold. *E.g.*, Ex. 1001, 9:5-67, Fig. 4. More specifically, a first regulated voltage may be provided to *both* the logic and the memory. *Id.*, 3:21-29.

If, however, that voltage falls below the memory's minimum operating voltage, then a higher, second regulated voltage is provided to the memory so that the memory's minimum operating voltage is met, while the lower first regulated voltage is still provided to the logic. *E.g., id.*, Abstract, 3:21-45, claims 1 and 16. Ex. 1002, ¶ 39.

Figure 1 of the '373 patent, annotated below, illustrates a data processing system 10 with a memory 18, a processor 16, and non-volatile registers 12. Ex. 1001, 2:38-42. Figure 1 also shows “a power supply selector 21 which receives VDDmem and VDDlogic and provides *one* of these to memory array 22 as the memory operating voltage.” *Id.*, 2:52-57. Ex. 1002, ¶ 40.



**FIG. 1**

As shown in Figure 1, the regulated voltage from voltage regulator 24, **VDDlogic**, is *always* provided to **processor 16**. Ex. 1001, 3:23-27. On the other hand, the regulated voltage provided to **the memory array 22** will *either* be **VDDlogic or VDDmem**. *Id.*, Abstract, 2:6-10. According to the patent, **VDDmem** is greater than **VDDlogic**. *Id.*, 3:27-29, Claims 1, 16. Ex. 1002, ¶ 41.

The '373 patent describes the following steps. **First**, the integrated circuit is tested to determine the memory's minimum operating voltage, and that minimum operating voltage is stored in non-volatile memory. Ex. 1001, 6:33-36, Fig. 4. **Second**, during operation, a first regulated voltage (**VDDlogic**) is provided to **both** the processor and the memory. *Id.*, 3:23-29. **Third**, when that first regulated voltage (**VDDlogic**) falls *below* the memory's minimum operating voltage, the memory is provided with a second regulated voltage (**VDDmem**), which is greater than the first regulated voltage (**VDDlogic**). *Id.*, 3:30-39. Ex. 1002, ¶ 42.

### C. Summary of Prosecution History

The '373 patent issued from U.S. Application No. 11/468,458, filed on August 30, 2006. Ex. 1001, cover. Several claims were rejected as being anticipated or obvious in view of (1) U.S. Patent No. 6,772,379 (Ex. 1019) ("Camera"); (2) the combination of U.S. Patent No. 5,086,501 ("DeLuca") (Ex. 1011) and U.S. Patent No. 6,975,551 ("Iwata") (Ex. 1020); and/or (3) the combination of DeLuca in view of Iwata in view of U.S. Patent Application



Publication No. 2007/0174642 (“Cornwell Publication”) (Ex. 1021). August 19, 2008 Office Action (Ex. 1022), 3-14.

The applicants amended original independent claims 1, 11, and 20 (issued claims 1, 9, and 16) to add limitations (among others) from original dependent claims 5, 12, and 21. November 13, 2008 Response (Ex. 1023), 1-6. The applicants distinguished DeLuca and Iwata by arguing that neither reference discloses that “the second regulated voltage is greater than the first regulated voltage and that while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the functional circuit.” *Id.*, 8.

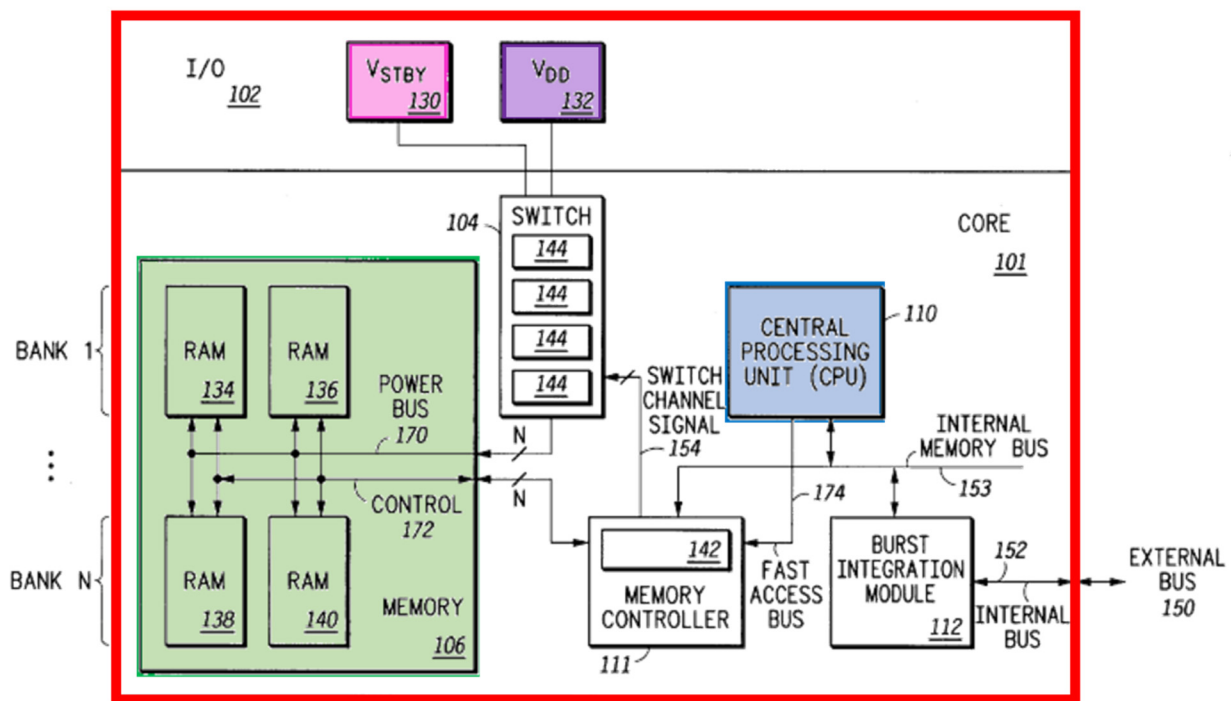
## **VIII. OVERVIEW OF THE PRIOR ART REFERENCES**

The challenged claims of the ’373 patent are obvious over the following prior art references. Ex. 1002, ¶ 43.

### **A. Harris**

Harris was filed on June 10, 1996, over a decade before the ’373 patent, and was not considered during prosecution. Harris teaches providing a first supply voltage to an integrated circuit, while also dynamically selecting between first and second supply voltages to provide to the memory in the integrated circuit. Ex. 1002, ¶ 44.

Figure 1, annotated below, shows an embodiment of Harris's integrated circuit. The **data processor 100** includes a core 101, which further includes a **memory portion 106** and a **central processing unit (CPU) 110**. Ex. 1003, 2:27-42, Fig. 1. The memory portion 106 contains banks of SRAM or DRAM. *Id.*, 2:34-38, 1:12-21. Ex. 1002, ¶ 45.



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**FIG. 1**

The core also includes a “switch” circuit 104 containing switches 144. The “switch in the switching circuit is used to determine which of the two power supply voltages ... will be supplied” to the memory banks within the integrated circuit. Ex. 1003, 2:6-9. “The **Vstby terminal 130** is coupled to the switch circuit

104, and the VDD terminal 132 is also coupled to the switch circuit 104.” *Id.*, 2:42-44. The switch circuit 104 uses a “switch control/channel signal 154” to determine which of these voltages to provide to the memory banks. *Id.*, 2:44-47. Ex. 1002, ¶ 46.

Harris teaches several uses for the memory switching circuit. One use is “for testing on-chip memory on a microcontroller.” Ex. 1003, Abstract. Another use for the voltage switching circuit is to ensure that the memory is provided with sufficient voltage to avoid data loss. To achieve this, “voltage level on the terminal VDD” is “monitored to ensure that a functional voltage is provided” to the memory. Ex. 1003, 3:54-56. If “this VDD voltage level drops below a set level or threshold, the voltage on the VSTBY terminal 132 is ***switched to power the memory*** 106 to sustain memory contents when either main or VDD power is failing.” *Id.*, 3:57-60. In other words, if one voltage being provided to the memory (VDD) “falls below” the memory’s minimum operating threshold, then the memory voltage switching circuit switches the memory to a different voltage (Vstby) “to avoid memory data loss.” *Id.*, 3:64-67, Claim 8. Ex. 1002, ¶¶ 47-48.

Another use for Harris’s voltage switching circuit is to enable a “low power feature” in which the voltage supplied to the CPU is lowered to reduce power, but the memory’s voltage is not. Harris explains that VDD may be lowered “so that lower power is consumed in the data processor.” Ex. 1003, 4:63-5:4. In this

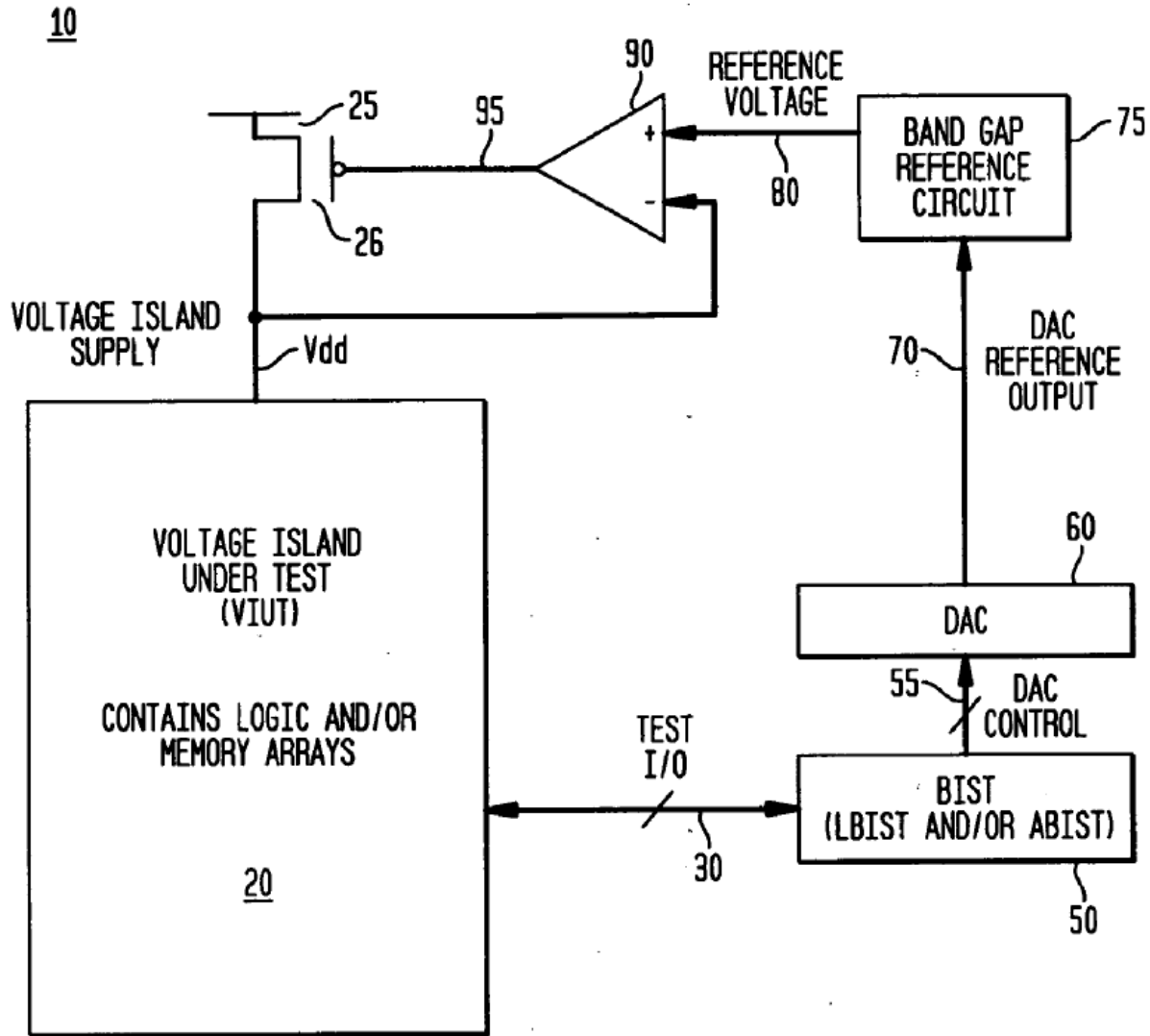
embodiment, *one* power supply voltage “which is being supplied to the CPU *is lowered* so that lower power is consumed in the data processor.” *Id.* The memory voltage switching circuit then provides *a different* power supply voltage to the memory so that “data within the at least one memory array is maintained.” *Id.* Ex. 1002, ¶¶ 49-50.

**B. Abadeer**

Abadeer was filed on May 12, 2005, and was not considered during prosecution. Abadeer provides a “solution for determining minimum operating voltages” for various components in an integrated circuit and storing those minimum operating voltages in non-volatile memory, such as fuses, in the integrated circuit. Ex. 1004, Abstract. Ex. 1002, ¶ 51.

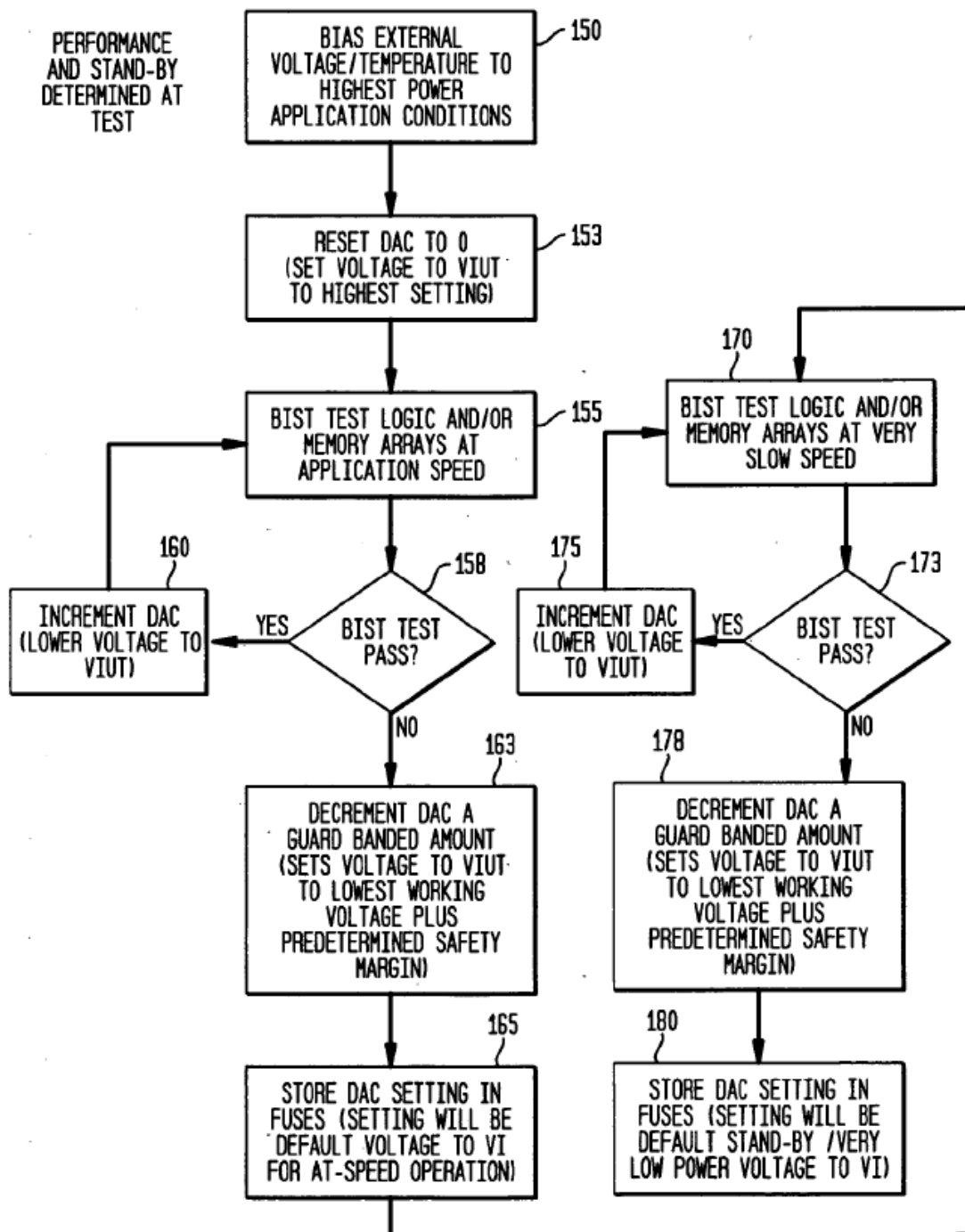
Specifically, Abadeer “relates generally to integrated circuits, and, more particularly, to a system and method for determining a minimum operating voltage of the IC.” Ex. 1004, ¶ 0002. Abadeer discloses a Built-In-Self-Test (BIST) for determining the minimum operating voltage for a “voltage island,” which may be logic and/or memory arrays, as illustrated in Figure 1 below. *Id.*, ¶ 0012. The memory arrays may be SRAM or DRAM. *Id.*, ¶ 0042. Once determined, the minimum operating voltage can be stored in non-volatile memory. *Id.*, ¶ 0045. Ex. 1002, ¶ 52.

**FIG. 1**



Abadeer further describes “a test flow method for determining both minimum power consumption while maintaining application performance and minimum power consumption for stand-by/very low power (while maintaining data/state information) via BIST during manufacturing test.” Ex. 1004, ¶ 0045. Figure 4 depicts this test flow methodology. Ex. 1002, ¶ 53.

**FIG. 4**



The method begins in step 153 by providing the logic and/or memory arrays with the highest voltage. Ex. 1004, ¶ 0045, Fig. 4. The method then checks to see

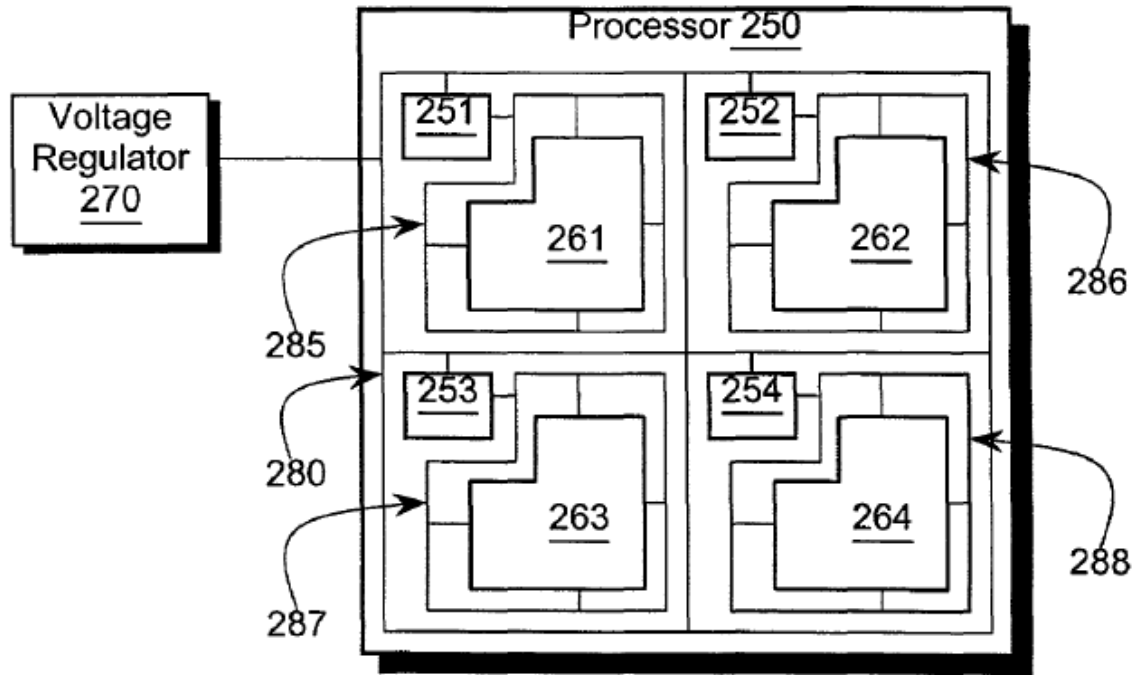
if the BIST test passes at application speed (steps 155 and 158). *Id.* If the test passes, the method reduces the voltage until the BIST fails. *Id.* When the BIST fails, “a predetermined safety margin” is added to the failure voltage and that value is stored in fuses. *Id.* Using this stored minimum operating voltage, the voltage supply to each voltage island, *i.e.*, memory, can be “tuned” to “obtain the best yield / power / performance tradeoff.” *Id.*, ¶ 0052. Ex. 1002, ¶ 54.

Abadeer further explains that during operation, after the minimum operating voltage of the memory is determined, power consumption can be reduced to the “lowest possible stand-by/very low power level” by operating the memory at the minimum operating voltage. Ex. 1004, ¶ 0044 (“This voltage level, if used for a standby mode, would be the lowest voltage supply that still allows the memory ... to maintain data.”), Abstract. Ex. 1002, ¶ 55.

### **C. Zhang**

Zhang was published on July 3, 2003, over three years before the '373 patent was filed, and was not considered during prosecution. Zhang discloses a processor with “one or more integrated voltage regulators” that generate “one or more local supply voltages.” Ex. 1005, Abstract. In Zhang, “[t]he local supply voltage(s) may be adjusted by the processor in accordance with a power management policy.” *Id.* Figure 2C of Zhang shows local voltage regulators 251-254 powering one or more circuits 261-264. *Id.*, ¶¶ 0026-0027. The one or more circuits can include

“all or a portion of one or more processor cores or memory regions such as a cache.” *Id.*, ¶ 0031. Ex. 1002, ¶ 56.



**Figure 2C**

Zhang discloses that “[e]ach local supply voltage provided by each local regulator 251-254 ... may be independently adjusted by processor 250” and “[e]ach local supply voltage can be individually tuned to the circuitry that it powers.” Ex. 1005, ¶¶ 0028, 0030. Zhang explains that “the local supply voltage that powers a critical, high performance circuit may be set to a higher voltage than the local supply voltage that powers a less critical, lower performance circuit.” *Id.*, ¶ 0030. By individually adjusting each local voltage, each circuit can operate “at the lowest (or nearly the lowest) local supply voltage appropriate for the each



circuit individually,” which “may result in a reduction of the overall power consumed by the processor.” *Id.* Ex. 1002, ¶ 57.

**D. Cornwell**

Cornwell, filed on January 25, 2006, teaches adjusting the operating voltage of a flash memory to at or near its minimum to “substantially minimize power consumption.” Ex. 1006, Abstract. Cornwell explains that the “minimum operating voltage for individual flash memory devices may vary from IC to IC, by manufacturing lot, and by manufacturer.” *Id.* Cornwell provides the minimum operating voltage information for an individual flash memory to a voltage regulator. *Id.*, Abstract, 2:5-13. Ex. 1002, ¶ 58.

Figure 1 of Cornwell discloses an integrated circuit with a register 120 that stores operating voltage information about the memory 110. Ex. 1006, 2:41-45, 3:1-23. Ex. 1002, ¶ 59.

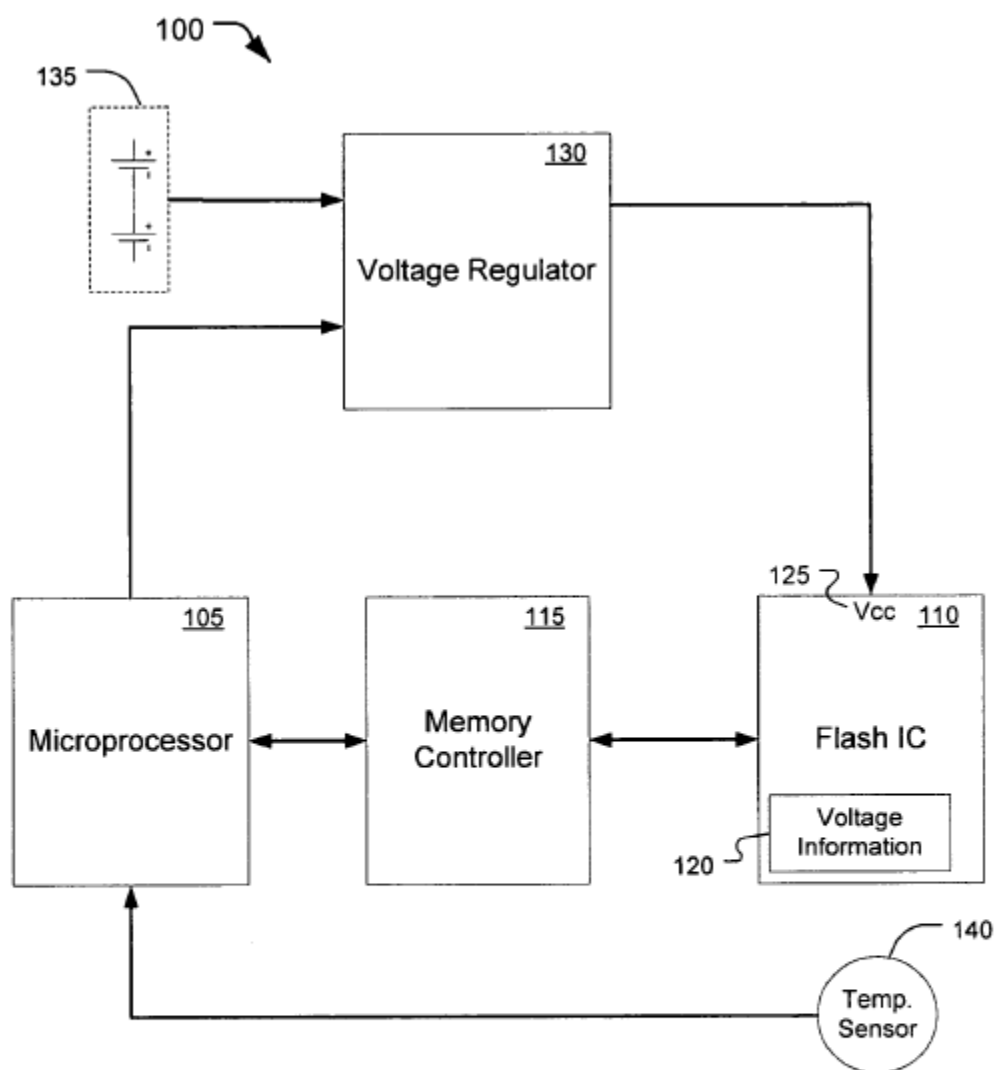


FIG. 1

Cornwell teaches that a memory may have different minimum voltages according to function. Ex. 1006, 3:44-47. Voltage information stored in register

120 may include “operating voltages in various operating conditions, such as the minimum read and/or write operating voltage in battery life preservation mode.”

*Id.*, 6:47-53. Cornwell explains that the minimum read and write operating voltages “may be determined and recorded, for example, through testing performed in the manufacturing process.” *Id.*, 3:14-17. Ex. 1002, ¶ 60.

#### **E. Bilak**

Bilak, published on August 25, 2005, was not considered during prosecution. Bilak discloses “[a] method and apparatus for adaptively adjusting the operating voltage of an integrated circuit.” Ex. 1007, Abstract. Bilak “enables tailoring of the operating voltage of integrated circuits on a part-by-part basis which results in power consumption optimization.” *Id.* Ex. 1002, ¶ 61.

To achieve the highest power consumption optimization, Bilak explains that the operating voltage can be adjusted to be the minimum operating voltage of the integrated circuit (“Vmin”). Ex. 1007, Abstract. Vmin “is determined during testing of the IC (typically by an external tester during manufacturing test).” *Id.*, ¶ 0047. Bilak recognizes that “[v]arious techniques are well known in the art for determining the Vmin of an IC using an external tester.” *Id.* Ex. 1002, ¶ 62.

#### **IX. CLAIM CONSTRUCTION**

“In an *inter partes* review proceeding, a claim of a patent ... shall be construed using the same claim construction standard that would be used to

construe the claim in a civil action ..., including construing the claim in accordance with the ordinary and customary meaning of such claim as is understood by” a person of ordinary skill in the art (“POSA”). 37 C.F.R.

§ 42.100(b). Petitioner submits that each claim term in the claims challenged by this Petition should be construed in accordance with its ordinary and customary meaning, and that no terms otherwise need construction for purposes of resolving the issues raised in this Petition. Ex. 1002, ¶ 63.

#### **X. LEVEL OF ORDINARY SKILL IN THE ART**

A POSA at the time of the alleged invention would have had at least the following (or equivalents): a B.S. degree in electrical engineering with at least five years of experience in power management design of integrated circuits or an M.S. degree in electrical engineering with at least two years of experience in power management design of integrated circuits. Ex. 1002, ¶¶ 64-65.

#### **XI. SPECIFIC GROUNDS FOR PETITION**

Pursuant to 37 C.F.R. §§ 42.104(b)(4)-(5), the below sections, as confirmed in the Singh Declaration (Ex. 1002), demonstrate in detail how the prior art discloses each and every limitation of claims 1-13 and 15-16 of the ’373 patent, and how those claims are rendered obvious by the prior art.

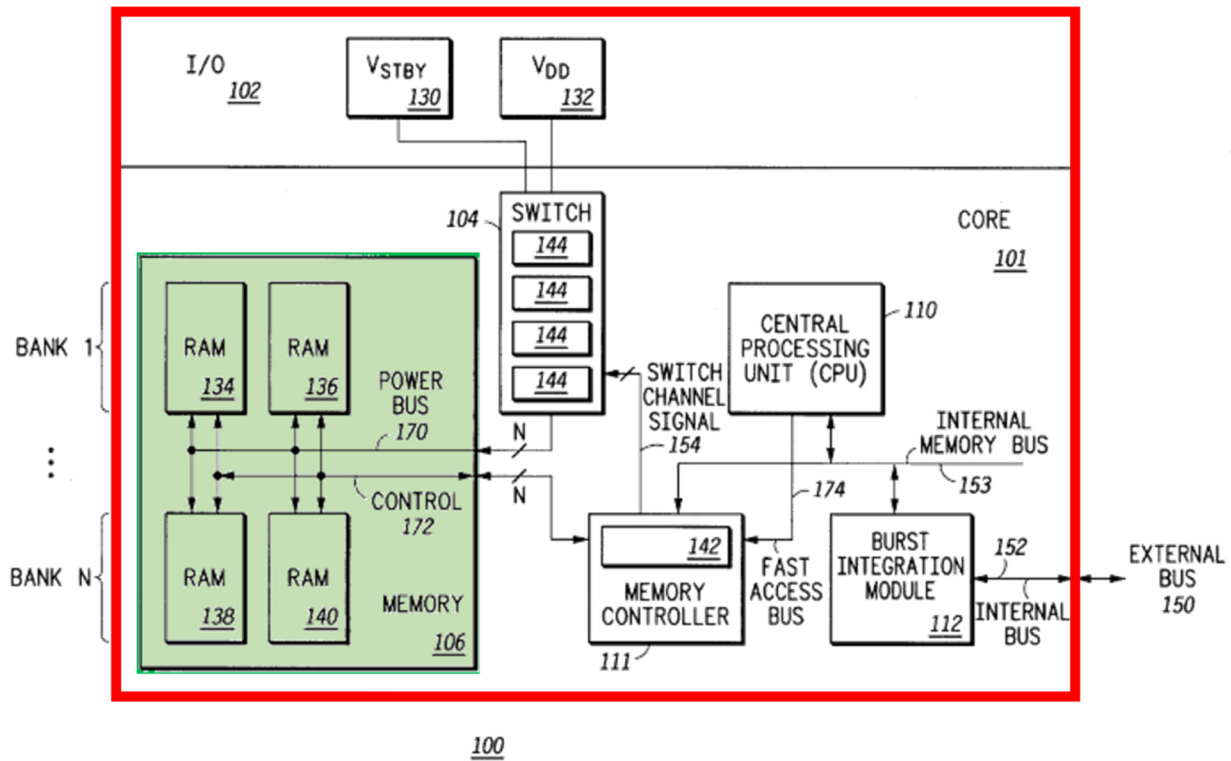
**A. Ground I: Claims 1-7, 9-11, 13, and 15-16 are obvious in view of Harris, Abadeer, and Zhang**

1. Claim 1

*a. 1[a]: “A method, comprising: providing an integrated circuit with a memory;”*

Harris discloses providing an integrated circuit with a memory. Ex. 1003, 1:66-2:10, 2:27-38. Ex. 1002, ¶ 67.

Specifically, Harris explains that “the present invention is a microprocessor or microcontroller design [and the] microprocessor is a packaged integrated circuit.” *Id.*, 1:66-2:2. Harris discloses that “the packaged integrated circuit ... contains ... a core 101, [and the] core 101 comprises a memory portion 106,” which “contains N banks of memory,” and “each bank of RAM [random access memory] can contain more than one block or array of RAM sections 134, 136, 138, and 140.” *Id.*, 2:27-38; *see also* Claim 10. Annotated Figure 1 of Harris, below, shows the integrated circuit with memory 106. Ex. 1002, ¶ 68.

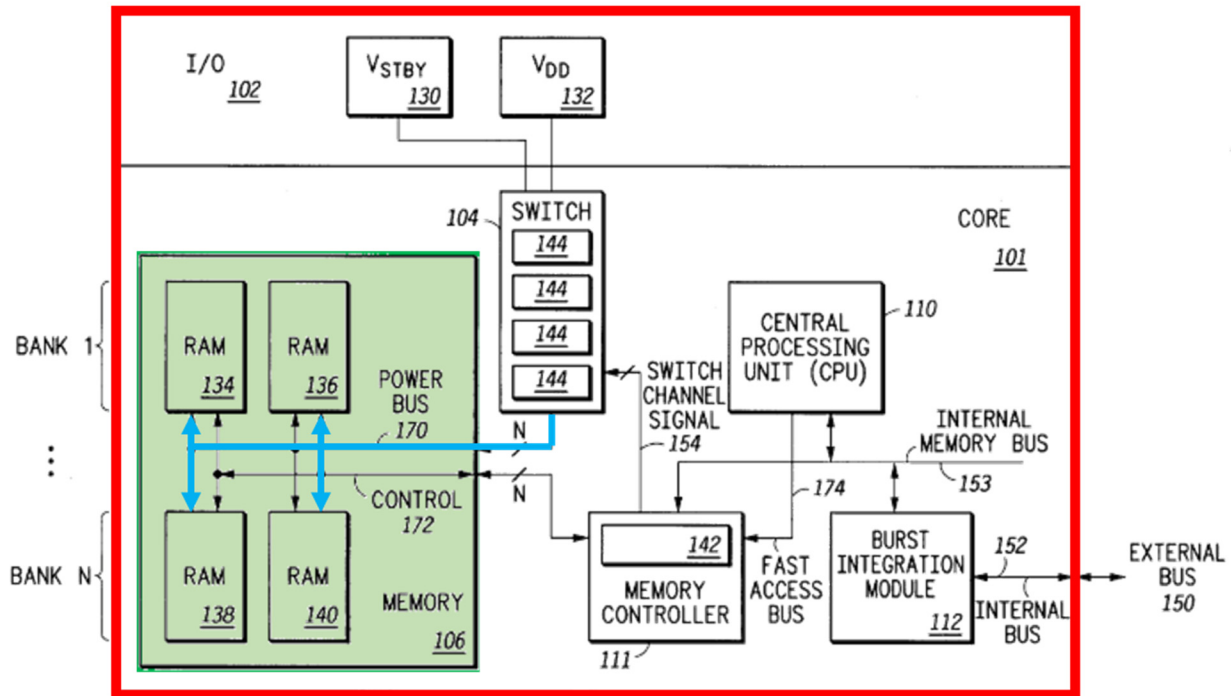


**FIG. 1**

**b. 1[b]: “operating the memory with an operating voltage;”**

Harris discloses operating the memory with an operating voltage. In Harris, power bus 170 is used to provide a voltage to the memory 106. Ex. 1003, 2:63-66 (“Each of the RAM blocks is connected to at least one line of the power bus 170 as provided by switch 104.”). In particular, switching circuit 104 “has outputs VDarr 0, VDarr 1, VDarr 2, and VDarr 3 (which stand for Voltage applied to array #).” *Id.*, 4:7-9, Fig. 2. Harris further discloses operating the memory with the voltage provided by power bus 170. *See id.*, 2:60-67, 3:1-2, Claim 1. Annotated Figure 1 of Harris, below, shows operating the memory with an operating voltage over the

“power bus 170.” Ex. 1002, ¶ 69.



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FIG. 1

c. 1[c]: “determining a value of a minimum operating voltage of the memory;”

Abadeer discloses determining a value of a minimum operating voltage of a memory. Abadeer provides “[a] solution for determining minimum operating voltages due to performance/power requirements....” Ex. 1004, Abstract.

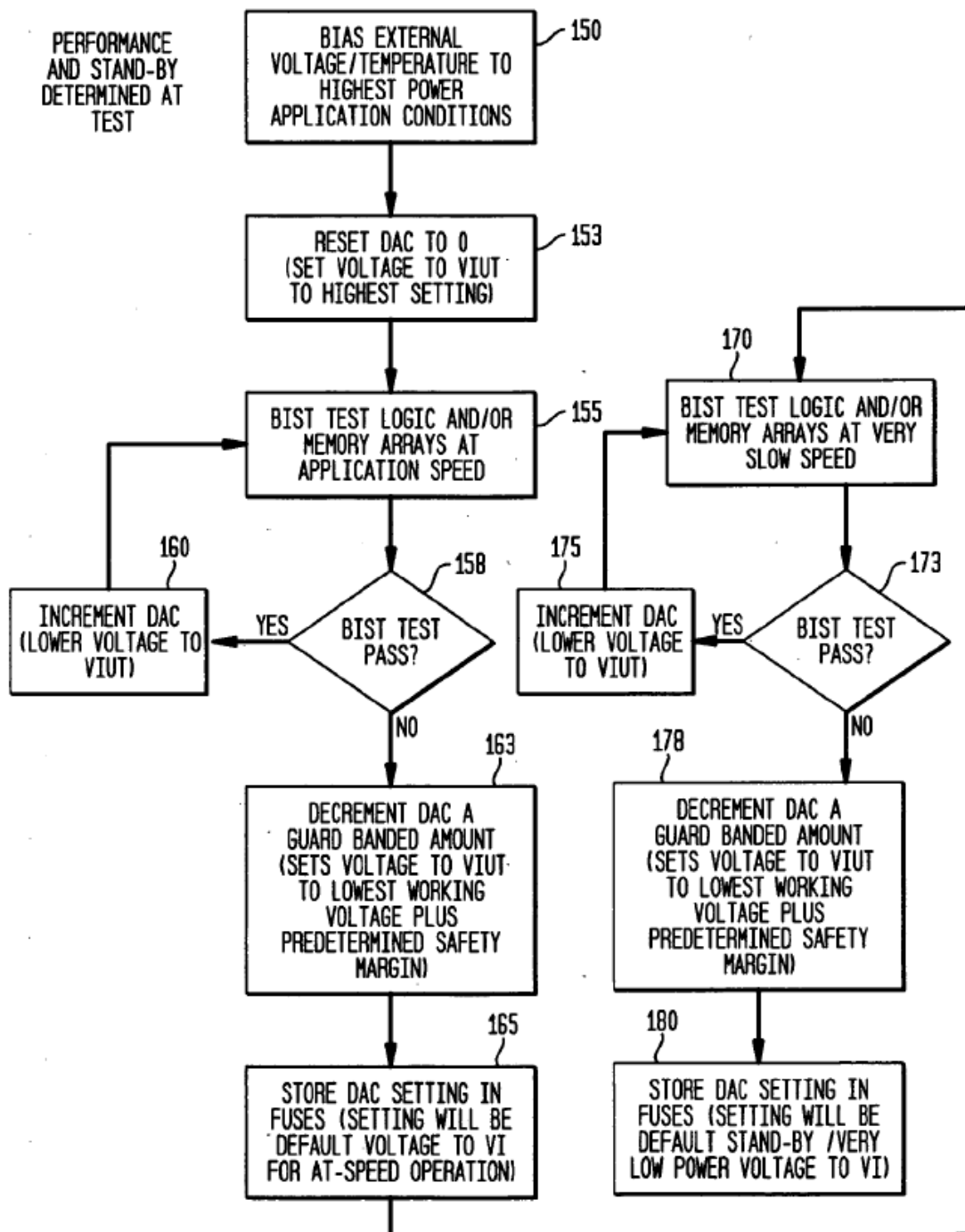
Abadeer describes “a self-test system and methodology for determining the minimum operating voltage of an IC having a voltage island under test that includes both logic and *memory* arrays.” *Id.*, ¶ 0012. Abadeer’s solution includes

“a test flow methodology for dynamically reducing power consumption to the lowest possible *stand-by*/very low power level.” *Id.*, Abstract. The minimum operating voltage, “*if used for a standby mode*, would be the lowest voltage supply that still allows the *memory* ... to maintain data.” *Id.*, ¶ 0044. Abadeer therefore discloses testing a memory to determine its minimum operating (“standby”) voltage. Ex. 1002, ¶ 70.

In Abadeer’s “test flow method for determining ... minimum power consumption for *stand-by*/very low power (while maintaining data/state information),” a Built-In-Self-Test (BIST) determines the minimum standby operating voltage. Ex. 1004, ¶ 0045. Figure 4, below, shows this test flow. *Id.* Ex. 1002, ¶ 71.



**FIG. 4**



In step 153, the method for determining the minimum operating voltage of the memory provides the memory arrays with the highest voltage. Ex. 1004,

¶ 0045, Fig. 4. The method checks to see if the test passes for a “stand-by/very low power operational setting” (steps 170 and 173). *Id.* If the test passes, the method reduces the voltage provided to the memory arrays (step 175) and performs the test again. *Id.* These steps are repeated until the test fails. *Id.* When the test fails, “a predetermined safety margin” is added to the lowest working voltage (step 178) and that value is stored in fuses (step 180). *Id.*, Figs. 3-4, ¶¶ 0044-0045. The ’373 patent explains that the stored minimum operating voltage need not be the absolute minimum operating voltage of the memory, but may take into consideration other factors such as temperature, and the memory may be able to actually operate at a lower voltage. *See, e.g.*, Ex. 1001, 2:9-15, 6:51-55. Abadeer’s stored minimum operating voltage, with its included safety margin, is therefore an example of a minimum operating voltage. Ex. 1002, ¶ 72.

It would have been obvious to a POSA to apply Abadeer’s teachings to determine the minimum operating voltage of the memory in Harris. Ex. 1002, ¶ 73.

**First**, Harris teaches a “set level or threshold” below which there may be “memory data loss.” Ex. 1003, 3:54-4:3. Harris explains that the set level or threshold is used to determine whether to switch the voltage supplied to the memory from VDD to VSTBY in order to “sustain memory contents” when VDD falls. *Id.* Harris does not explicitly disclose how to determine this threshold;

however, this minimum operating threshold is a common concept, and Abadeer teaches one technique for determining it. Specifically, Abadeer teaches testing for and storing the minimum operating voltage of a memory, which is “the lowest voltage supply necessary to maintain data” plus a “predetermined safety margin.” Ex. 1004, ¶¶ 0045, 0049. A POSA would have therefore looked to Abadeer for how to determine the set level or threshold disclosed in Harris, and would have had a reasonable expectation of success in applying those teachings to Harris. The predetermined safety margin would ensure that the voltage provided to the memory in Harris would not drop low enough for the memory to fail when the voltage to the memory is switched from VDD to VSTBY. Ex. 1002, ¶ 74.

**Second**, Harris teaches that its voltage switching circuit can be used as a “low power feature” in which “lower power is consumed in the data processor while data within the at least one memory array is maintained.” Ex. 1003, 4:63-5:4. Harris explains that, for this feature, the voltage supplied to the memory is switched from VDD to VSTBY when the voltage VDD, which is also supplied to other components in the integrated circuit, will be lowered below the point needed to maintain data in the memory. *Id.* This allows “lower power [to be] consumed in the data processor while data within the [memory] is maintained.” *Id.* It was well-known that to reduce power consumption, voltage to the components of an integrated circuit could be lowered; however, if data needed to be preserved in

volatile memory, the voltage to that memory could not be lowered below a minimum threshold. Harris itself teaches “a set level or threshold” below which there may be “memory data loss. *Id.*, 3:54-4:3. And as Abadeer explains, a system and method for determining the minimum operating voltage serves to “reduc[e] supply voltage in order to reduce power consumption.” Ex. 1004, ¶¶ 0013-0014. Abadeer therefore discloses techniques for determining the minimum operating voltage that a POSA would have understood could be used in the “low power feature” contemplated by Harris. *Id.*, ¶ 0051 (explaining that for memories, the testing technique “can be used to tune the voltage to maximum yield, minimize power, and still maintain performance”). A POSA would, therefore, have been motivated to determine the minimum operating voltage as described in Abadeer for use with the system and method taught by Harris, and would have had a reasonable expectation of success in doing so for these reasons. Ex. 1002, ¶ 75.

***Third***, a POSA would have known that determining the minimum operating voltage, as described in Abadeer, and using that to implement the methods taught by Harris (e.g. operating a “low power feature” and ensuring at least the minimum operating voltage is provided to the memory at all times) would have involved nothing more than combining known prior art techniques (Harris’s low power mode and threshold-based voltage switching with Abadeer’s technique for determining a minimum operating voltage) according to known methods

(determining and using Abadeer’s minimum operating voltage as the threshold at which to switch the voltage supplied to the memory in Harris) to yield predictable results (obtaining and storing the minimum operating voltage to use as the threshold for switching voltages in Harris’s low power and failure modes to avoid memory data loss), and a POSA would have had a reasonable expectation of success in combining these teachings for the reasons explained above. Ex. 1002, ¶ 76.

***d. 1[d]: “providing a non-volatile memory (NVM) location; storing the value of the minimum operating voltage of the memory in the NVM location;”***

Abadeer discloses providing a non-volatile memory location and storing a minimum operating voltage of the memory in that location. Abadeer teaches that “[t]he values determined at test [are] stored in a non-volatile memory (such as fuses).” Ex. 1004, ¶ 0045, Fig. 4. Abadeer further explains that “fuses or any other non-volatile memory (Flash memory for example) can be used for saving DAC [voltage] settings when the chip is powered off...” *Id.*, ¶ 0048. Ex. 1002, ¶ 77.

For the reasons explained in Section XI.A.1.c, it would have been obvious to a POSA to modify Harris’s integrated circuit to include Abadeer’s non-volatile memory (fuses) to store the minimum operating voltage of the memory as taught by Abadeer. Specifically, a POSA would have been motivated to include the non-

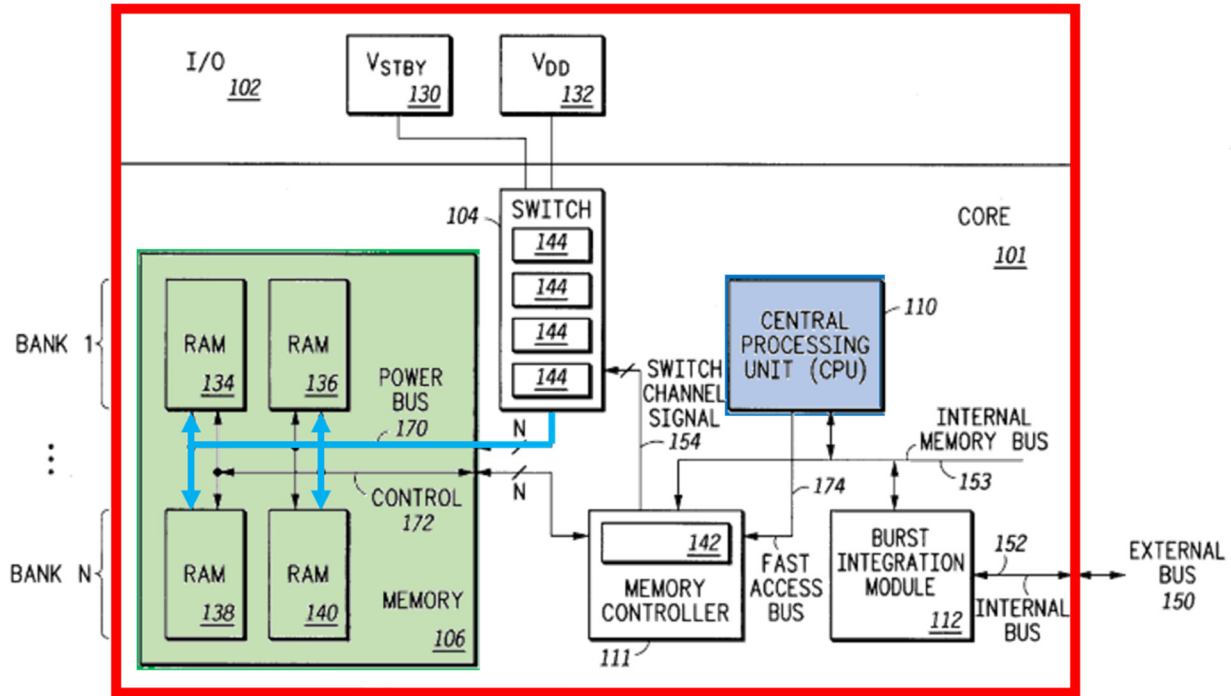
volatile fuses in Abadeer to store the minimum operating voltage of Harris's memory for use in Harris's low power feature or as the "set level or threshold" for use in Harris's failure monitoring. A POSA would have appreciated that it would be preferable to store the minimum operating voltages in non-volatile memory rather than to re-determine them every time the circuit was power cycled, and Abadeer teaches using fuses for that purpose. Ex. 1004, ¶ 0045. A POSA would therefore have been motivated to use Abadeer's non-volatile fuses to store the minimum operating voltage of Harris's memory. Ex. 1002, ¶ 78.

*e. 1[e]: "providing a functional circuit on the integrated circuit exclusive of the memory;"*

Harris discloses a functional circuit (central processing unit (CPU) 110) on the integrated circuit exclusive of the memory 106. Ex. 1003, 1:66-2:2, 2:27-42, Fig. 1. For example, Harris explains that the data processor 100 contains a core 101, which in turn comprises a CPU 110. *Id.*, 1:66-2:2, 2:39-42. According to the '373 patent, a processor is an example of a functional circuit. Ex. 1001, 6:13-21 ("Processor 16 may be any type of *processor* such as, for example, a microcontroller, microprocessor, digital signal processor, etc., and operates as known in the art. ... Alternatively, processor 16 may be any type of functional circuit in system 10."). Ex. 1002, ¶ 79.

Figure 1 of Harris, below, shows the integrated circuit with a CPU 110 that

is exclusive of memory 106. Ex. 1002, ¶ 80.



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**FIG. 1**

*f. 1[f]: “providing a first regulated voltage to the functional circuit;”*

Harris discloses providing a first voltage (VDD) to the functional circuit (CPU 110). Ex. 1003, 2:19-21; 3:25-29; 4:63-5:4; Fig. 1. In particular, Harris explains “all other non-array-current-tested portions of the microcontroller are powered by VDD.” Ex. 1003, 2:19-21, 3:25-29 (“[S]ome portion of memory 106 will be powered with VSTBY 130 while *all other circuitry* in processor 100 is powered by VDD 132.”). Moreover, the voltage switching circuit in Harris can be used in a low power mode such that “the first power supply (VDD or VSTBY) [is]

supplied to the CPU ....” *Id.*, 4:53-5:4. Ex. 1002, ¶ 81.

Zhang discloses providing “a regulated voltage” to a functional circuit. Specifically, Zhang discloses a processor with “one or more integrated **voltage regulators**” that generate “one or more local supply voltages.” Ex. 1005, Abstract. Figure 2C of Zhang shows local **voltage regulators 251-254** powering one or more circuits 261-264. *Id.*, ¶¶ 0026-0027. “Each local voltage regulator ... may be powered by Vcc(global), ... and each provides a local supply voltage, Vcc(local), for the processor.” *Id.*, ¶ 0027. The circuits 261-264 in Zhang can be “any other functional unit or other circuit of processor 250.” *Id.*, ¶ 0031. Zhang therefore discloses providing a regulated voltage to a functional circuit (e.g., a processor). Ex. 1002, ¶ 82.

It would have been obvious to a POSA to modify Harris’s integrated circuit in view of Abadeer to include the separate integrated voltage regulators taught by Zhang for supplying VDD and VSTBY, and a POSA would have been motivated to do so for several reasons. Ex. 1002, ¶ 83.

**First**, a POSA would have been motivated to control the supply voltages, VDD and VSTBY. For some operations, a POSA would have been motivated to provide both CPU 110 and the memory 106 with a stable voltage (VDD). A POSA would have recognized that a voltage regulator provides a stable, precise voltage for these operations. *See, e.g.*, Ex. 1024, 2269 (“voltage regulator: a device that



maintains the terminal voltage ... within required limits despite variations in input voltage or load. Also known as ... voltage stabilizer.”). Using voltage regulators to provide a stable voltage supply to a processor has been known for decades. For example, a POSA would have understood that CPU 110 in Harris would perform more consistently with a stable voltage (VDD), and a voltage regulator could provide that stable voltage (VDD). Furthermore, Harris explains that, in the test mode, a voltage (VSTBY) is applied to the memory and the current is tested. Ex. 1003, Abstract, 2:12-24. A POSA would have also understood that to accurately measure current, a stable voltage would be needed, such as the voltage provided by a voltage regulator. Accordingly, a POSA would have been motivated to use a voltage regulator as taught by Zhang to provide a stable voltage (for each of VDD and VSTBY) during operation. A POSA would have had a reasonable expectation of success in doing so for the reasons explained above. Ex. 1002, ¶ 84.

***Second***, a POSA would have been motivated to raise or lower VDD and/or VSTBY to decrease power consumption or improve performance. Both Harris and Zhang discuss scenarios in which it is desirable to both (a) independently supply voltages within an integrated circuit and (b) vary the supply voltages to manage power consumption. Harris explains that in the test mode, the voltage supplied to the memory can be “decoupled” from the voltage supplied to other components. Ex. 1003, 2:12-24. Harris further explains that either of the power supply voltages

(VDD and VSTBY) can be “lowered so that lower power is consumed in the data processor.” *Id.*, 4:63-5:4. Harris, however, does not expressly disclose *how* the power supply voltage is lowered. A POSA, in implementing this “low power feature” taught by Harris, would have looked to references, including Zhang, explaining how to adjust the voltage provided to different components in the integrated circuit. Zhang teaches that “*local supply voltage(s) may be adjusted* by the processor in accordance with a power management policy.” Ex. 1005, Abstract, ¶¶ 0013, 0028. Zhang teaches that a voltage regulator can be used to adjust the voltage provided to different circuits to save power as contemplated by Harris: “[L]ocal voltage regulators may provide local supply voltages at different voltage levels to different circuits in the processor. Each local supply voltage can be individually tuned to the circuitry that it powers. ... This may result in a *reduction of the overall power* consumed by the processor.” *Id.*, ¶ 0030. These benefits, among others, of using an adjustable voltage regulator to provide a regulated voltage were well-known. A POSA would have been motivated to incorporate the voltage regulators taught by Zhang to supply Harris’s VDD and VSTBY to permit independent voltage control and to manage power in low power operation. A POSA would have had a reasonable expectation of success in doing so for the reasons explained above. Ex. 1002, ¶ 85.

*Third*, it would have been obvious to a POSA to include the voltage

regulators for VDD and VSTBY on the same integrated circuit as the memory and logic as taught by Zhang. Both Harris and Zhang disclose an integrated circuit with memory and logic. Ex. 1003, 2:27-42; Ex. 1005, ¶ 0031. It would have been obvious to try to place the voltage regulators on the same integrated circuit as the memory and logic. There are only a finite number of identified and predictable solutions for placing the voltage regulators for generating VDD and VSTBY: on the same integrated circuit as the other components or external to the integrated circuit. There is nothing non-obvious about either predictable solution. A POSA would have found it obvious to try using the integrated (on-chip) voltage regulators of Zhang in the system of Harris. As Zhang explains, “[b]y including voltage regulator 211 *as part of the same integrated circuit as processor 210*, two or more different supply voltages can be routed to the various circuits of the processor. By providing processor 210 with different supply voltages at different voltage levels, *each supply voltage can be individually tuned to the circuitry that it powers*, resulting in a reduction of the overall power consumed by the processor.” Ex. 1005, ¶ 0024. Zhang’s integrated voltage regulators also would reduce the response time for adjusting each local voltage because the integrated circuit would not need to wait for an external voltage regulator, and would provide greater flexibility in the power management policy because each local voltage could be independently adjusted. A POSA would have had a reasonable expectation of

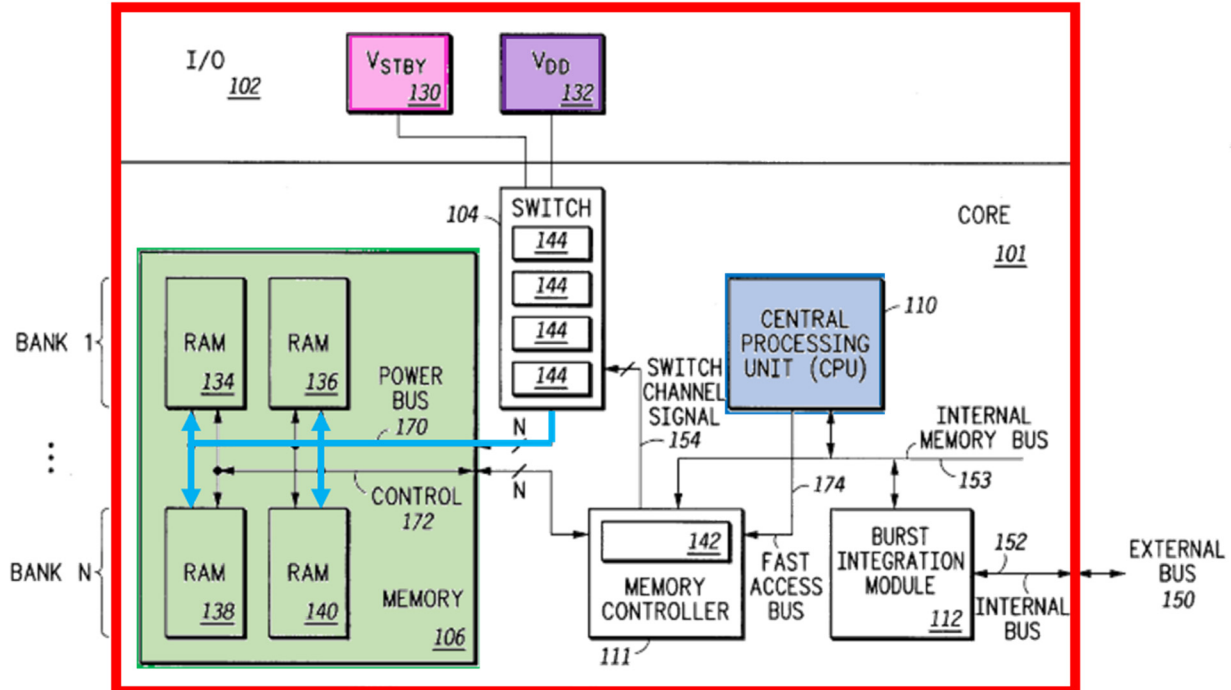
success in doing so for the reasons explained above. Ex. 1002, ¶ 86.

**Fourth**, using the integrated voltage regulators in Zhang to provide the VDD and VSTBY voltages in Harris would have involved nothing more than combining prior art elements (adding the integrated voltage regulators of Zhang to the integrated circuit of Harris) according to known methods (integrating voltage regulators as taught by Zhang) to yield predictable results (Harris's integrated circuit with integrated voltage regulators for independent control and power management). A POSA would have had a reasonable expectation of success in doing so for the reasons explained above. Ex. 1002, ¶ 87.

Harris, Abadeer, and Zhang describe similar systems in the same field of endeavor and their teachings are complementary as described in Sections VII.A, VII.B, and VII.C. All three references teach circuit design and operation for processors and/or memory to manage power by adjusting voltage levels to components of an integrated circuit. Ex. 1003, 4:63-5:4; Ex. 1004, ¶¶ 0044-0045; Ex. 1005, ¶¶ 0028, 0030. Combining the teachings of Harris, Abadeer, and Zhang as set forth herein involves nothing more than combining prior art elements according to known methods to yield predictable results, and use of known techniques to improve similar devices (or methods) in the same way. Ex. 1002, ¶ 88.

***g. 1[g]: “providing a second regulated voltage, the second regulated voltage is greater than the first regulated voltage;”***

Harris discloses providing a second voltage (**VSTBY**), greater than the first voltage (**VDD**). Ex. 1003, 3:54-4:3, 4:63-5:4. Figure 1, illustrated below, shows first voltage **VDD** and second voltage **VSTBY**. *Id.*, Fig. 1. **VSTBY** is provided to the integrated circuit on a pin separate from **VDD**. *Id.*, 2:2-6 (“The switching circuit receives a first supply voltage from a **VDD** external terminal and a second supply voltage from a second voltage source which is typically a **VSTBY** pin (a power supply voltage standby terminal).”). Accordingly, **VSTBY** is a different (second) voltage from **VDD** (the first voltage). Ex. 1002, ¶ 89.



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**FIG.1**

Harris discloses that **VSTBY** is greater than **VDD**. For example, Harris's "switch 104" can be used to switch the voltage supplied to the memory from **VDD** to **VSTBY** when **VDD** power is failing or "falls below a voltage threshold" in order "to avoid memory data loss." Ex. 1003, 3:54-4:3, Claim 8. Because **VSTBY** is at a voltage to maintain data in the memory, whereas **VDD** "falls below a voltage threshold" at which data would not be maintained in the memory, a POSA would have understood that **VSTBY** is greater than **VDD**. Accordingly, the second voltage, **VSTBY**, is greater than the first voltage, **VDD**. Ex. 1002, ¶ 90.

Harris also discloses that its voltage switch may be used in the test mode "as a low power feature" where a "first power supply voltage" (**VDD**) is provided to the CPU, but that the first power voltage supply "is lowered" so that less power is consumed. Ex. 1003, 4:63-5:4. At the same time, a "second power supply voltage" (**VSTBY**) is provided to the memory "so that lower power is consumed in the data processor while data within the ... memory ... is maintained." *Id.* Because the voltage provided to the memory is switched from **VDD** to **VSTBY** to maintain the data within the memory when the voltage supplied to the CPU (**VDD**) is lowered to save power, a POSA would have understood that **VSTBY** is greater than **VDD**. *Id.*, 3:1-2, 4:63-5:4, Claims 1 and 6. Ex. 1002, ¶ 91.

Zhang discloses providing a second regulated voltage to a memory. Specifically, Zhang discloses a processor with "one *or more* integrated *voltage*

**regulators**” that generate “one **or more** local supply voltages.” Ex. 1005, Abstract. Figure 2C of Zhang shows local **voltage regulators 251-254** powering one or more circuits 261-264. *Id.*, ¶¶ 0026-0027. Each local voltage regulator is powered by Vcc(global), and each provides a local supply voltage, Vcc(local), for the processor. *Id.*, ¶ 0027. The circuits 261-264 in Zhang can be “memory regions such as a cache.” *Id.* ¶ 0031. Zhang therefore discloses providing a regulated voltage to a memory. Ex. 1002, ¶¶ 92-93.

***h. 1[h]: “providing the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the value of the minimum operating voltage; and”***

Harris teaches providing the first voltage (**VDD**) as the operating voltage of the memory when the first voltage (**VDD**) is at least the value of the minimum operating voltage. Harris teaches that **VDD** is provided to the non-memory components of the IC, including the processor. Ex. 1003, 2:19-21, 3:26-29. Harris also teaches that **VDD** can be provided to the memory. *Id.*, 3:15-16 (“The power supply (**VDD** or **VSTBY**) to the selected [memory] block or blocks 134-140 is controlled by switch 104 ....”). Harris explains that “[i]n a normal mode of operation, the core 101 [which includes memory blocks 134-140] would be powered by a supply voltage applied to VDD terminal 132.” *Id.*, 3:1-2, Claim 1. Ex. 1002, ¶ 94.

While **VDD** is provided to the **entire** circuit (including the memory) during a

normal mode of operation, during failure mode, the switch causes **VSTBY** to be provided to the memory instead of **VDD**. Ex. 1003, 3:54-4:3. “When this **VDD** *voltage level drops below a set level or threshold, the voltage on the **VSTBY** terminal 132 is switched to power the memory 106 to sustain memory contents* when either main or **VDD** power is failing.” *Id.*, 3:57-60, Claim 8. Harris therefore teaches that the same voltage (**VDD**) can be supplied to both the memory and the CPU when **VDD** (the first voltage) is at least the value of “a set level or threshold” (the minimum operating voltage). *Id.*, 3:53-4:3. Ex. 1002, ¶¶ 95-96.

- i. 1[i]: “providing the second regulated voltage as the operating voltage of the memory when the first regulated voltage is less than the value of the minimum operating voltage,”*

Harris discloses providing the second voltage (**VSTBY**) as the operating voltage of the memory when the first voltage (**VDD**) is less than the value of the minimum operating voltage. Ex. 1003, 3:53-4:3, 4:63-5:4. Harris teaches a “low power feature,” where the voltage supplied to the memory would be switched from **VDD** to **VSTBY**, when **VDD** is lowered to save power. *Id.*, 4:63-5:4. Specifically, “the second power supply voltage (**VSTBY** or **VDD**) is provided to the [memory] while the first power supply voltage (**VDD** or **VSTBY**) which is being supplied to the CPU is lowered so that lower power is consumed in the data processor while data within the [memory] is maintained.” *Id.*, 4:63-5:4. Harris also teaches a failure mode that “[w]hen this **VDD** voltage level drops below a set level or



threshold, the voltage on the **VSTBY** terminal 132 is switched to power the memory 106 to sustain memory contents when either main or **VDD** power is failing.” *Id.*, 3:57-60. As Harris explains, “**VSTBY** must be substituted for **VDD** to avoid memory data loss.” *Id.*, 3:64-67. Ex. 1002, ¶ 97.

Harris further teaches that there is “a set level or threshold” at which the memory will no longer maintain its data. *Id.*, 3:57-60. Harris explains that when **VDD** is lowered below the set level or threshold, **VSTBY** should be provided to the memory so that “the at least one memory array is maintained.” *Id.*, 4:62-5:4, 3:57-60 (“When this **VDD** voltage level drops below a set level or threshold, the voltage on the **VSTBY** terminal 132 is switched to power the memory 106 to sustain memory contents when either main or **VDD** power is failing.”). Accordingly, Harris in view of Abadeer and Zhang discloses this limitation. Ex. 1002, ¶¶ 98-99.

**j. 1[j]: “wherein while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the functional circuit.”**

Harris discloses that while the second voltage (**VSTBY**) is provided as the operating voltage of the memory, the first voltage (**VDD**) is provided to the functional circuit. Harris discloses that all the circuitry, other than the memory, is provided with **VDD**. Ex. 1003, 1:18-20, 3:26-30. Harris explains that “all other non-array-current-tested portions of the microcontroller are powered by **VDD**.” *Id.*, 2:12-24. For the test mode, Harris explains that “some portion of memory 106 will

be powered by **VSTBY 130** *while* all other circuitry in **processor 100** is powered by **VDD 132.**” *Id.*, 3:26-29. And when the test mode is used as a low power feature, **VSTBY** is provided to the memory while **VDD** is provided to the CPU. *Id.*, 4:63-5:4. Ex. 1002, ¶ 100.

Accordingly, Harris in view of Abadeer and Zhang renders claim 1 obvious. Ex. 1002, ¶¶ 101-102.

2. Claim 2

*a. “The method of claim 1,”*

As described in Section XI.A.1, Harris in view of Abadeer and Zhang renders obvious the method of claim 1. Ex. 1002, ¶103.

*b. “wherein the step of testing the memory is further characterized by the minimum operating voltage comprising one of a group consisting of minimum write voltage, minimum read voltage, and a minimum standby voltage.”*

Abadeer discloses the step of testing the memory,<sup>5</sup> where that step is characterized by the minimum operating voltage comprising one of a group

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<sup>5</sup> Claim 1 does not recite “a step of testing the memory.” While for purposes of this petition only, Petitioner assumes that “step of testing the memory” refers to one or more of the steps of “determining” and/or “storing,” Petitioner also demonstrates how a step of testing the memory is made obvious by the prior art .

consisting of minimum write voltage, minimum read voltage, and a minimum standby voltage. **First**, Abadeer discloses the step of testing the memory. Specifically, Abadeer describes a “**test flow** method for determining ... minimum power consumption for stand-by/very low power.” Ex. 1004, ¶ 0045. **Second**, Abadeer tests for the minimum standby voltage of the memory. Abadeer’s test flow method is used to determine the voltage to use for the memory for “minimum power consumption for **stand-by/very low power**.” *Id.* In Abadeer, the memory is repeatedly tested at increasingly lower voltages (Fig. 4 steps 170, 173, and 175) until the test fails so that a minimum “default **stand-by/very low power voltage setting**” can be determined, and the standby voltage setting, including a safety margin, is stored (Fig. 4 steps 178 and 180). *Id.* Accordingly, Harris in view of Abadeer and Zhang renders claim 2 obvious. Ex. 1002, ¶ 104.

3. Claim 3

**a. “The method of claim 1,”**

As described in Section XI.A.1, Harris in view of Abadeer and Zhang renders obvious the method of claim 1. Ex. 1002, ¶ 105.

- b. “wherein the step of providing the integrated circuit with the memory is further characterized by the memory comprising one of a group consisting of dynamic random access memory and static random access memory.”***

Harris discloses that the memory (“memory portion 106”) may be one of a group consisting of dynamic random access memory (“DRAM”) and static random access memory (“SRAM”). Harris identifies two types of memories: SRAM and DRAM. Ex. 1003, 1:12-19. Harris explains that use of SRAM has become more common as processor speeds have increased over time because it does not require refresh cycles to retain data like DRAM. *Id.* Harris, however, recognizes that SRAM does not have “perfect data retention” and proposes a system to test for defects in SRAM. *Id.*, 1:19-52, 1:66-2:24. While Harris provides the specific example of using SRAM, Harris teaches memory comprising SRAM and/or DRAM. Accordingly, Harris in view of Abadeer and Zhang renders claim 3 obvious. Ex. 1002, ¶ 106.

4. Claim 4

- a. “The method of claim 1,”***

As described in Section XI.A.1, Harris in view of Abadeer and Zhang renders obvious the method of claim 1. Ex. 1002, ¶ 107.

- b. “wherein the step of providing the NVM location is further characterized by the NVM location comprising a non-volatile register.”***

Abadeer discloses this limitation. The '373 patent explains that “non-volatile registers may be implemented as programmable fuses.” Ex. 1001, 7:47-49. Abadeer discloses fuses. Abadeer teaches that “[t]he values determined at test [are] stored in a non-volatile memory (*such as fuses*).” Ex. 1004, ¶ 0045 (“Subsequently, at step 180, the DAC setting is stored *as a control word in fuse devices* to subsequently function as providing a default stand-by/very low power voltage setting to the VI.”). A POSA would have understood that using a plurality of fuses to store a word of data is a way to implement a non-volatile register. *See, e.g.*, Ex. 1025, 4:20-25 (disclosing fuses that “include a plurality of non-volatile register bits”). Accordingly, Harris in view of Abadeer and Zhang renders claim 4 obvious. Ex. 1002, ¶ 108.

5. Claim 5

- a. “The method of claim 1, further comprising:”***

As described in Section XI.A.1, Harris in view of Abadeer and Zhang renders obvious the method of claim 1. Ex. 1002, ¶ 109.

- b. “providing a signal in response to a desired value for the first regulated voltage being below the minimum operating voltage.”***

Harris in view of Abadeer and Zhang renders obvious this limitation.

Harris's writing to a register for test mode and/or providing switch control/channel signal 154 teaches the "signal" recited by claim 5. Ex. 1003, 2:47-51. Harris uses switch control signal 154 to "set the configuration of switches 144 to control power supply distribution in the data processor 100." *Id.* Harris explains that the switch control signal 154 "is software controlled or software programmable." *Id.* The CPU 110 writes a register 142 in memory controller 111 to change switch control signal 154. *Id.*, 2:9-12 ("The selection of VDD or VSTBY to the memory array is software programmable through a register accessed by a CPU core of the microprocessor design."), 3:15-18, 3:65-4:3, Claim 9. In the test mode for the low power feature in Harris, CPU 110 can write to the register to switch the voltage provided to the memory from VDD to VSTBY. *See id.*, 2:9-12, 3:15-18, 4:63-5:4. Thus, in order to enter the test mode for the low power feature and lower VDD, CPU 110 writes a value to the memory controller to provide a switch control signal to switch the voltage provided to the memory. Ex. 1002, ¶ 110.

While Harris teaches lowering VDD to save power, Harris does not explicitly detail the components that control, or lower, VDD. Ex. 1003, 4:63-5:4. However, as explained below, it would have been obvious to use Harris' CPU 110 to control the level of VDD. That is, Harris' CPU 110 would have identified a "desired value" of VDD, *e.g.*, so that CPU 110 could lower VDD when appropriate to save power. In response to the desired value of VDD being below the minimum

operating voltage, requiring a switch of the voltage supplied to the memory from VDD to VSTBY, CPU 110 would then write to the register in the memory controller (“providing a signal”) to enter test mode for the low power feature in order to generate the switch control signal 154 (also “providing a signal”). *Id.*, 2:9-12, 3:15-18, 4:63-5:4. Ex. 1002, ¶ 111.

Processors that controlled their own voltage supplies were well known long before the '373 patent. Ex. 1005, ¶¶ 0028-0030. For example, Zhang discloses a processor that regulates its own supply voltage. Zhang teaches that “[e]ach local supply voltage provided by each local voltage regulator ... may be independently ***adjusted by processor 250***. ... These values may be adjusted by the processor in accordance with a power management policy.” *Id.* “For example, when a circuit powered by a local voltage regulator is inactive, the local supply voltage provided by the local voltage regulator may be reduced by the processor.” *Id.* “The local supply voltage may additionally be adjusted in response to a change in the operating frequency of the processor.” *Id.* In Zhang, the processor, “may set the values in a control register” to control the output voltage. *Id.*, ¶¶ 0033-0036. These values represent “a desired value for the first regulated voltage.” Ex. 1002, ¶ 112.

A POSA would have used Zhang’s technique of regulating the CPU’s supply voltage in the system of Harris in view of Abadeer. A POSA would have been

motivated to do so to permit the CPU 110 to determine when to raise VDD (e.g., to provide increased performance) and when to lower VDD (e.g., to conserve power when high performance was not needed) as taught by Zhang. Ex. 1005, ¶¶ 0028-0030. In the combination of Harris, Abadeer and Zhang, CPU 110 of Harris sets the level of VDD, e.g., by writing control values to a control register for a VDD voltage regulator that has been integrated in Harris according to Zhang's teachings. That is, CPU 110 sets the "desired level" of VDD (the first regulated voltage). When entering the low power mode described in Harris, switch channel signal 154 causes switch 104 to deliver VSTBY (instead of VDD) to memory 106. Ex. 1002, ¶¶ 113-114.

6. Claim 6

*a. "The method of claim 1, further comprising:"*

As described in Section XI.A.1, Harris in view of Abadeer and Zhang renders obvious the method of claim 1. Ex. 1002, ¶ 115.

*b. 6[a] "providing a controller on the integrated circuit that selects an operating value for the operating voltage of the memory; and"*

Harris discloses this limitation. Harris teaches providing "a switch control/channel signal 154 from the memory controller 111." Ex. 1003, 2:46-47. Memory controller 111 is part of core 101, which is contained within the packaged integrated circuit. *Id.*, 2:27-42. Harris also teaches that "[t]he switch control



signal 154 is software controlled or software programmable and is used to set a configuration of switches 144 to control power supply distribution in the data processor 100.” *Id.*, 2:47-51. Memory controller 111 selects an operating value for the operating voltage of the memory array (from among VDD and VSTBY) and generates switch control signal 154 accordingly. *Id.*, 2:51-53. Switch control signal 154 determines whether the voltage from the VDD terminal 132 or the VSTBY terminal 130 is supplied to the memory array. *Id.*, 4:9-14. Ex. 1002, ¶ 116.

- c. 6[b] “providing the operating voltage to the memory at a value at least as great as the minimum operating voltage in response to the operating value selected by the processor being below the minimum operating voltage.”*

Harris in view of Abadeer and Zhang renders obvious this limitation. As explained in Section XI.A.5.b for claim 5, in the combination of Harris, Abadeer and Zhang, Harris’s CPU 110 selects the value of VDD. Further, in that combination, when Harris enters a test mode for the low power feature, switch 104 provides VSTBY (instead of VDD) to memory 106, where VSTBY is greater than VDD and is at least as great as the minimum operating voltage. Accordingly, Harris in view of Abadeer and Zhang provides the operating voltage to the memory (Harris’ memory 106) at a value (VSTBY ) at least as great as the minimum operating voltage in response to the operating value selected by the processor (Harris’ CPU 110) being below the minimum operating voltage. Ex. 1002, ¶ 117.

To the extent that Patent Owner argues that “the processor” of limitation 6[b] refers to “a controller” of limitation 6[a], Harris in view of Abadeer and Zhang also teaches this limitation. As explained in Section XI.A.5.b, it would have been obvious for CPU 110 in Harris to request a value of VDD using the power management technique disclosed in Zhang. Further, as explained in Section XI.A.5.b, it would have been obvious for CPU 110 in Harris to also select the operating voltage of the memory. As Harris explains, “[t]he switch control signal 154 is *software controlled or software programmable* and is used to set a configuration of the switches 144 *to control power supply distribution in the data processor 100.*” Ex. 1003, 2:47-51. Under this interpretation of limitations 6[a] and 6[b], CPU 110 in the combination of Harris, Abadeer and Zhang sets the level of VDD, *e.g.*, by writing to a control register in a VDD voltage regulator that has been integrated in Harris according to Zhang’s teachings. Moreover, core 101 includes both CPU 110 and memory controller 111, and core 101 therefore performs both of the functions recited in limitations [6a] and [6b]. *Id.*, 2:27-59. Accordingly, Harris in view of Abadeer and Zhang renders obvious claim 6. Ex. 1002, ¶¶ 118-119.

7. Claim 7

a. *“The method of claim 1, further comprising”*

As described in Section XI.A.1, Harris in view of Abadeer and Zhang

renders obvious the method of claim 1. Ex. 1002, ¶ 120.

***b. “providing the value of the minimum operating voltage external to the integrated circuit.”***

Abadeer discloses this limitation. Abadeer teaches that “fuses or any other non-volatile memory (Flash memory for example) can be used for saving DAC settings [voltage control values] when the chip is powered off.” Ex. 1004, ¶ 0048. Abadeer also explains that “[t]he volatile/non-volatile methods for storing the DAC settings [voltage control values] necessary for correct operation under certain circumstances can be located inside the BIST engine, external to the BIST engine, *or external to the chip.*” *Id.* Accordingly, Harris in view of Abadeer and Zhang renders claim 7 obvious. Ex. 1002, ¶ 121.

8. Claim 9

***a. 9[a] “An integrated circuit, comprising:”***

As described in Section XI.A.1.a, Harris discloses an integrated circuit. Ex. 1002, ¶ 122.

***b. 9[b] “a memory that operates using an operating voltage, wherein the memory is characterized as having a minimum operating voltage”***

As described in Sections XI.A.1.b–XI.A.1.c, Harris in view of Abadeer renders obvious a memory that operates using an operating voltage, wherein the memory is characterized as having a minimum operating voltage. Ex. 1002, ¶ 123.

It would have been obvious to a POSA to combine the teachings of Harris

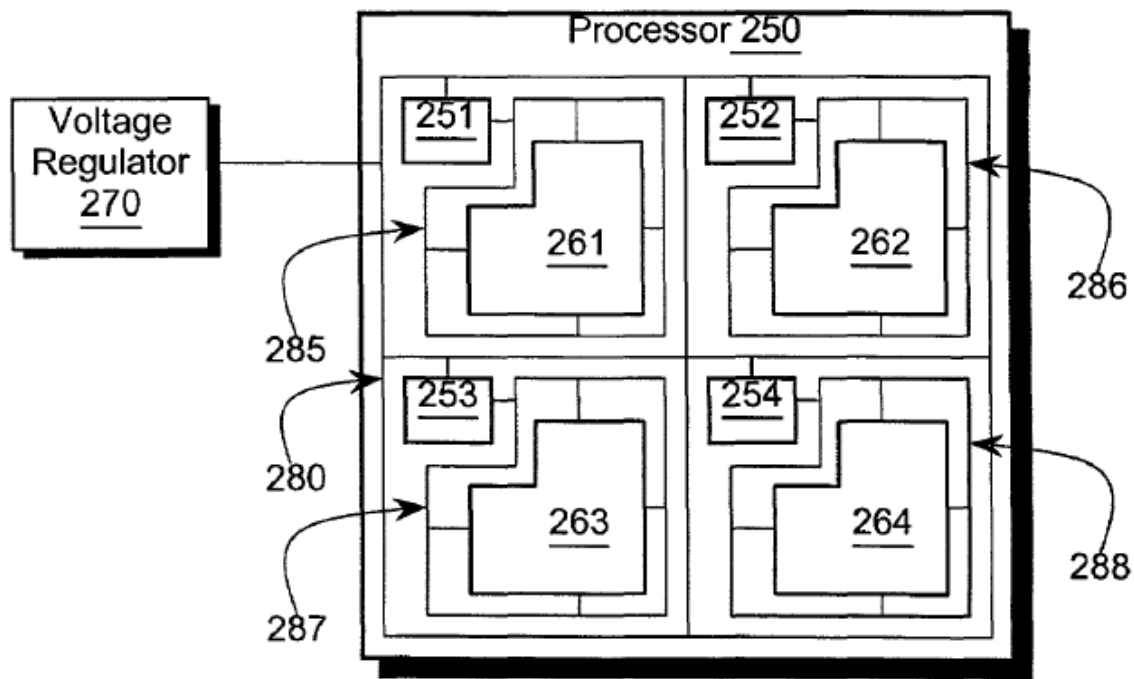
and Abadeer for the reasons described in Sections XI.A.1.c-j. Ex. 1002, ¶ 124.

*c. 9[c] “a memory location that stores a value representative of the minimum operating voltage”*

As described in Section XI.A.1.d, Harris in view of Abadeer discloses a memory location that stores a value representative of the minimum operating voltage. Ex. 1002, ¶ 125.

*d. 9[d] “a first voltage regulator for supplying a first regulated voltage”*

As described in Section XI.A.1.f, Harris discloses a first voltage supply. Zhang discloses a first voltage regulator in the integrated circuit. Specifically, Zhang discloses a processor with “one or more *integrated voltage regulators*” that generate “one or more local supply voltages.” Ex. 1005, Abstract. Figure 2C of Zhang, reproduced below, shows local voltage regulators 251-254 powering one or more circuits 261-264 on the same integrated circuit. *Id.*, ¶¶ 0026-0027. Ex. 1002, ¶ 126.



**Figure 2C**

As explained in Sections XI.A.1.f-j, it would have been obvious to integrate the voltage regulators of Zhang on Harris's integrated circuit to generate VDD and VSTBY as regulated voltages. Ex. 1002, ¶ 127.

***e. 9[e] "a circuit that provides a function and uses the first regulated voltage"***

As described in Sections XI.A.1.e and XI.A.1.f, Harris in view of Zhang renders obvious a circuit that provides a function (e.g., central processing unit (CPU) 110) and uses the first regulated voltage. Ex. 1002, ¶ 128.

It would have been obvious to a POSA to combine the teachings of Harris and Zhang for the reasons described in Sections XI.A.1.e-j. Ex. 1002, ¶ 129.

- f. 9[f] “a second voltage regulator for supplying a second regulated voltage, wherein the second regulated voltage is greater than the first regulated voltage;”***

As described in Section XI.A.1.g, Harris discloses a second voltage, wherein the second voltage is greater than the first voltage, and Zhang discloses a second voltage regulator for supplying a second regulated voltage. Ex. 1002, ¶ 130.

As described in Sections XI.A.1.f and XI.A.1.g, Zhang discloses multiple voltage regulators on the same integrated circuit. As explained in Sections XI.A.1.f-j, it would have been obvious to integrate the voltage regulators of Zhang on Harris’s integrated circuit to generate VDD and VSTBY as regulated voltages. Ex. 1002, ¶ 131.

- g. 9[g] “a power supply selector that supplies the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the minimum operating voltage and supplies the second regulated voltage as the operating voltage when the first regulated voltage is below the minimum operating voltage, wherein while the second regulated voltage is supplied as the operating voltage, the circuit uses the first regulated voltage.”***

As described in Sections XI.A.1.h-j, Harris in view of Abadeer and Zhang renders obvious this limitation. Further, Harris discloses “a power supply selector.” Specifically, Harris discloses memory controller 111 that uses switch control signal 154 to “set the configuration of the switches 144 to control power supply distribution in the data processor 100.” Ex. 1003, 2:47-51. The CPU 110

writes a register 142 in memory controller 111 to change switch control signal 154.

*Id.*, 2:9-12, 3:15-18, 3:65-4:3, Claim 9. Accordingly, Harris in view of Abadeer and Zhang renders claim 9 obvious. Ex. 1002, ¶ 132.

9. Claim 10

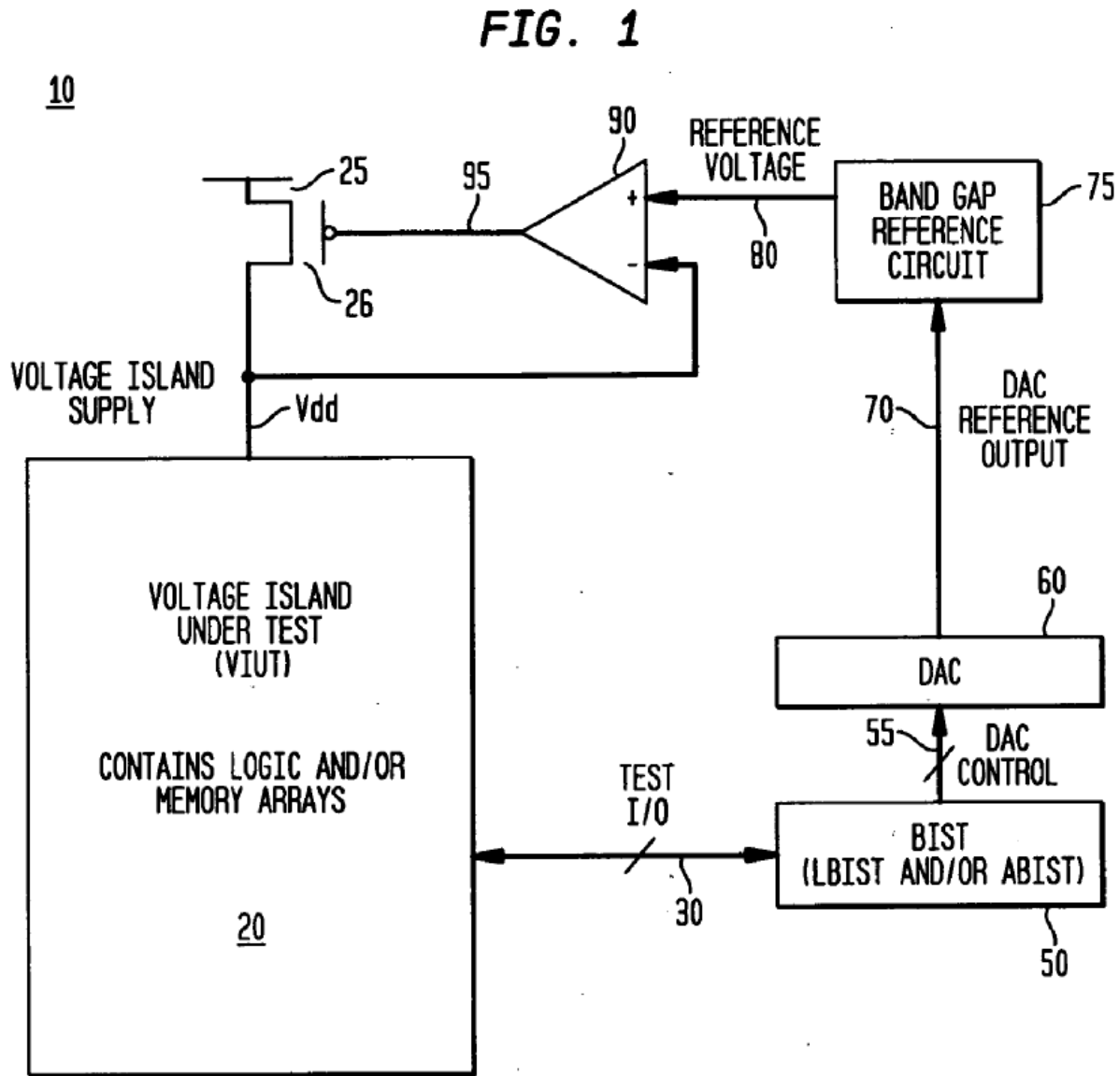
*a. “The integrated circuit of claim 9,”*

As described in Section XI.A.8, Harris in view of Abadeer and Zhang renders obvious the integrated circuit of claim 9. Ex. 1002, ¶ 133.

*b. “wherein the circuit that provides a function comprises a processor, further comprising: a built-in self-test (BIST) circuit, coupled to the processor, which determines the minimum operating voltage.”*

Abadeer discloses that the integrated circuit may include a built-in self-test (BIST) circuit, coupled to the processor, which determines the minimum operating voltage. Abadeer discloses “*a Built-In-Self-Test (BIST) circuit* is used to determine the correct supply voltage for all elements in a design (which takes into account variability between devices on a chip).” Ex. 1004, ¶ 0014. In particular, Abadeer discloses a “test flow method for determining ... minimum power consumption for stand-by/very low power (while maintaining data/state information),” in which *a BIST* determines the minimum operating voltage that still allows the memory to maintain data. *Id.*, ¶ 0045. A voltage is provided to the memory, and the *BIST* tests the memory to determine if it can retain data at that voltage. *Id.* Ex. 1002, ¶ 134.

As shown in Figure 1 of Abadeer below, **BIST 50** is coupled to voltage island 20 (which “contains logic and/or memory arrays”) via test input/output signal lines 30. Ex. 1004, ¶ 0033. Ex. 1002, ¶ 135.



As explained in Section XI.A.1.c, it would have been obvious to a POSA to modify the integrated circuit of Harris to include the teachings of Abadeer



regarding testing the memory to determine its minimum operating voltage. For the same reasons, it also would have been obvious to a POSA to modify the integrated circuit of Harris to include the BIST taught by Abadeer, and a POSA would have been motivated to do so for several additional reasons. Ex. 1002, ¶ 136.

**First**, Harris and Abadeer both recognize that, due to variations in manufacture and other factors, characteristics of memory can differ from chip-to-chip. Ex. 1003, 1:21-24, 1:36-52; Ex. 1004, ¶¶ 0014-0015. Harris describes testing for such variations in operating current range. Ex. 1003, 3:1-49. Abadeer describes testing for such variations in minimum operating voltage of memories. Ex. 1004, ¶¶ 0014-0015. Both Harris and Abadeer describe performing this testing in order to save power. Ex. 1003, 4:63-5:4; Ex. 1004, ¶ 0044. Incorporating the BIST of Abadeer onto the integrated circuit of Harris would have thus involved nothing more than use of known technique (a BIST for determining minimum operating voltages) to improve similar devices (the memory tester of Harris and the memory tester of Abadeer) in the same way (incorporating a BIST in the system of Harris to permit self-testing of minimum operating voltage as taught by Abadeer). Ex. 1002, ¶ 137.

**Second**, incorporating the BIST of Abadeer into the integrated circuit of Harris to determine minimum operating voltage of the memory would have involved nothing more than combining prior art elements (the BIST of Abadeer

with the integrated circuit of Harris) according to known methods (using the BIST to determine a minimum operating voltage threshold for switching between two supply voltages) to yield predictable results (customized power savings from a chip testing its own memory). Accordingly, Harris in view of Abadeer and Zhang renders claim 10 obvious. Ex. 1002, ¶ 138.

10. Claim 11

*a. “The memory of claim 9,”*

As described in Section XI.A.8, Harris in view of Abadeer and Zhang renders obvious the memory of claim 9. Ex. 1002, ¶ 139.

*b. “wherein the minimum operating voltage comprises one of a group consisting of minimum retention voltage, minimum read voltage, minimum write voltage, and minimum standby voltage.”*

As described in Section XI.A.2.b, Abadeer discloses this limitation. Accordingly, Harris in view of Abadeer and Zhang renders claim 11 obvious. Ex. 1002, ¶ 140.

11. Claim 13

*a. “The memory of claim 9,”*

As described in Section XI.A.8, Harris in view of Abadeer and Zhang renders obvious the memory of claim 9. Ex. 1002, ¶ 141.

- b. “wherein the memory comprises one of a group consisting of a static random access memory and a dynamic random access memory.”***

As described in Section XI.A.3.b, Harris discloses wherein the memory comprises one of a group consisting of a SRAM and a DRAM. Accordingly, Harris in view of Abadeer and Zhang renders claim 13 obvious. Ex. 1002, ¶ 142.

12. Claim 15

- a. “The memory of claim 9,”***

As described in Section XI.A.8, Harris in view of Abadeer and Zhang renders obvious the memory of claim 9. Ex. 1002, ¶ 143.

- b. “wherein the memory location is characterized as being a non-volatile register.”***

As described in Section XI.A.4.b, Abadeer discloses wherein the memory location is characterized as being a non-volatile register. Accordingly, Harris in view of Abadeer and Zhang renders claim 15 obvious. Ex. 1002, ¶ 144.

13. Claim 16

- a. 16[a] “A method, comprising: providing an integrated circuit with a memory that uses an operating voltage”***

As described in Sections XI.A.1.a–XI.A.1.b, Harris discloses this limitation. For the same reasons described with respect to claim 1 in Sections XI.A.1.c, XI.A.1.e, and XI.A.1.f, it would have been obvious to combine the teachings of Harris, Abadeer, and Zhang in a manner that meets the limitations of claim 16 as described in more detail below. Ex. 1002, ¶ 145.

- b. 16[b] “testing the memory to determine the operating voltage of the memory that is a minimum operating voltage;”***

As described in Sections XI.A.1.c and XI.A.2.b, Abadeer discloses this limitation. Ex. 1002, ¶ 146.

- c. 16[c] “storing, in a non-volatile manner, the value of the minimum operating voltage;”***

As described in Section XI.A.1.d, Abadeer discloses this limitation. Ex. 1002, ¶ 147.

- d. 16[d] “providing a functional circuit on the integrated circuit exclusive of the memory;”***

As described in Section XI.A.1.e, Harris discloses this limitation. Ex. 1002, ¶ 148.

- e. 16[e] “providing a first regulated voltage to the functional circuit;”***

As described in Section XI.A.1.f, Harris in view of Zhang renders obvious this limitation. Ex. 1002, ¶ 149.

- f. 16[f] “providing a second regulated voltage, wherein the second regulated voltage is greater than the first regulated voltage;”***

As described in Section XI.A.1.g, Harris in view of Zhang renders obvious this limitation. Ex. 1002, ¶ 150.

- g. 16[g] “providing the first regulated voltage as the operating voltage of the memory when the first regulated voltage is at least the value of the minimum operating voltage; and”**

As described in Section XI.A.1.h, Harris in view of Abadeer and Zhang renders obvious this limitation. Ex. 1002, ¶ 151.

- h. 16[h] “providing the second regulated voltage as the operating voltage of the memory when the first regulated voltage is less than the value of the minimum operating voltage,”**

As described in Section XI.A.1.i, Harris in view of Abadeer and Zhang renders obvious this limitation. Ex. 1002, ¶ 152.

- i. 16[i] “wherein while the second regulated voltage is provided as the operating voltage of the memory, the first regulated voltage is provided to the functional circuit.”**

As described in Section XI.A.1.j, Harris in view of Zhang renders obvious this limitation. Accordingly, Harris in view of Abadeer and Zhang renders claim 16 obvious. Ex. 1002, ¶ 153.

**B. Ground II: Claims 2 and 11-12 are obvious in view of Harris, Abadeer, Zhang, and Cornwell**

**1. Claim 2**

- a. “The method of claim 1,”**

As described in Section XI.A.1, Harris in view of Abadeer and Zhang renders obvious the method of claim 1. Ex. 1002, ¶ 154.

- b. “wherein the step of testing the memory is further characterized by the minimum operating voltage comprising one of a group consisting of minimum write voltage, minimum read voltage, and a minimum standby voltage.”***

To the extent that Patent Owner argues that claim 2 requires a capability to test for each of a minimum write voltage, minimum read voltage, and a minimum standby voltage, Abadeer and Cornwell disclose this limitation. Ex. 1002, ¶ 155.

As described in Section XI.A.1.c, Abadeer discloses testing the memory to determine its minimum standby voltage. Specifically, Abadeer discloses “a Built-In-Self-Test (BIST) circuit” to determine a “more accurate supply voltage setting” to “maintain data integrity *during standby*.” Ex. 1004, ¶ 0014. Abadeer explains that its test flow can be used to determine voltage settings for a “*stand-by*/very low power” operation. *Id.*, ¶¶ 0044-0045. Abadeer therefore discloses testing a memory for “a minimum standby voltage.” Ex. 1002, ¶ 156.

Cornwell discloses that “[t]he register 120 may store a variety of information about the operation voltage of the flash memory IC 110.” Ex. 1006, 3:1-2. For example, register 120 may store “a suggested minimum voltage for read operation, a suggested maximum voltage for read operation, a suggested minimum voltage for write operation, and/or a suggested maximum voltage for write operation.” *Id.*, 3:2-6. According to Cornwell, these minimum read and write voltages “may be determined and recorded, for example, through testing performed in the

manufacturing process.” *Id.*, 3:14-17. Accordingly, Cornwell discloses testing of a memory for a minimum read voltage and for a minimum write voltage. Ex. 1002, ¶ 157.

It would have been obvious to a POSA to modify the voltage switching circuit of Harris to use the determined minimum operating voltages, as taught by Abadeer and Cornwell, and a POSA would have been motivated to do so for several reasons. Ex. 1002, ¶ 158.

**First**, Harris teaches that its voltage switching circuit can be used as a low power feature to lower the power consumption. Ex. 1003, 4:63-5:4. It was well-known that to lower the power consumption of an integrated circuit, the voltage of the circuit should be lowered to as close as possible to the minimum operating voltage of the circuit. As Abadeer explains, a system and method for determining the minimum operating voltage serves to “reduc[e] supply voltage in order to reduce power consumption in semiconductor circuits, while still maintaining at-application speed performance.” Ex. 1004, ¶¶ 0013-0014. Cornwell also teaches that operating a memory “near a minimal operating voltage may substantially minimize power consumption.” Ex. 1006, Abstract, 1:58-60, 2:4-13, 2:34-45; 3:44-56. A POSA would have been motivated to test the memory to determine the minimum operating voltage for multiple possible functions of the memory (*i.e.*, read, write, standby voltages), as taught by Cornwell and Abadeer, at which it

could operate to achieve the greatest power savings. A POSA would have had a reasonable expectation of success in doing so for the reasons explained. Ex. 1002, ¶ 159.

**Second**, a POSA would have known that using the minimum operating voltages of Abadeer and Cornwell to control when the voltage supplied to the memory in Harris is switched would have involved nothing more than combining prior art elements (the voltage monitoring and threshold-based switching of Harris with the determined minimum operating voltages of Abadeer and Cornwell) according to known methods (using the threshold to switch the voltage supplied to the memory) to yield predictable results (ensuring that the voltage supplied to the memory does not drop below the minimum operating voltage depending on the function performed by the memory). A POSA would have had a reasonable expectation of success in doing so for the reasons explained above. Ex. 1002, ¶ 160.

Moreover, a POSA would have known that the techniques for determining a minimum read and write voltage for a flash memory as taught by Cornwell could be used for determining the minimum read and write voltages for a SRAM memory as taught by Harris and Abadeer. A POSA would have recognized that, because SRAM memory has distinct read and write voltages like the flash memory of Cornwell, testing could likewise be used to determine those thresholds. *See*,



e.g., Ex. 1026, 2:37-52 (disclosing an SRAM memory with “a write voltage” and a separate “read voltage”). Accordingly, Harris in view of Abadeer, Zhang, and Cornwell renders claim 2 obvious. Ex. 1002, ¶¶ 161-162.

2. Claim 11

*a. “The memory of claim 9,”*

As described in Section XI.A.8, Harris in view of Abadeer and Zhang renders obvious the memory of claim 9. Ex. 1002, ¶ 163.

*b. “wherein the minimum operating voltage comprises one of a group consisting of minimum retention voltage, minimum read voltage, minimum write voltage, and minimum standby voltage.”*

To the extent that Patent Owner argues that claim 11 requires the capability to test for each of a minimum retention voltage, minimum write voltage, minimum read voltage, and a minimum standby voltage, the combination of Harris, Zhang, Abadeer and Cornwell renders obvious this limitation. Ex. 1002, ¶ 164.

As explained in Section XI.B.1.b, Abadeer and Cornwell teach testing the memory to determine its minimum write voltage, minimum read voltage, and a minimum standby voltage. Abadeer also discloses testing the memory to determine its minimum retention voltage. The '373 patent explains that “there is a minimum data retention voltage such that if the memory operating voltage falls below this minimum data retention voltage, the data in memory array 22 may be lost.” Ex. 1001, 4:38-41. Abadeer tests for “the lowest voltage supply that still

allows the memory ... to maintain data.” Ex. 1004, ¶ 0044. Abadeer therefore discloses testing for a minimum retention voltage. Ex. 1002, ¶ 165.

As explained in Section XI.B.1.b, it would have been obvious to a POSA to modify the voltage switching circuit of Harris to use the determined minimum operating voltages, as taught by Abadeer and Cornwell. Accordingly, Harris in view of Abadeer, Zhang, and Cornwell renders claim 11 obvious. Ex. 1002, ¶ 166.

3. Claim 12

*a. “The memory of claim 11,”*

As described in Section XI.B.2, Harris in view of Abadeer, Zhang, and Cornwell renders obvious the memory of claim 11. Ex. 1002, ¶ 167.

*b. “wherein the minimum operating voltage comprises another one of the group consisting of minimum retention voltage, minimum read voltage, minimum write voltage, and minimum standby voltage.”*

As described in Section XI.B.2, Harris in view of Abadeer, Zhang, and Cornwell renders obvious this limitation. Ex. 1002, ¶ 168.

**C. Ground III: Claim 8 is obvious in view of Harris, Abadeer, Zhang, and Bilak**

1. Claim 8

*a. “The method of claim 1,”*

As described in Section XI.A.1, Harris in view of Abadeer and Zhang renders obvious the method of claim 1. Ex. 1002, ¶ 169.

***b. “wherein the step of determining is further characterized as performing a test applied externally from the integrated circuit.”***

The '373 patent explains that “an external tester may be used to apply a testing protocol external from system 10 during or after manufacture of system 10 to determine the minimum operating voltages.” Ex. 1001, 7:57-60. Bilak discloses this limitation. Ex. 1002, ¶ 170.

Bilak discloses a system and method for determining the minimum operating voltage of an integrated circuit “either during external testing of the integrated circuit or during built-in-self-testing.” Ex. 1007, Abstract. Bilak discloses that the minimum operating voltage of the integrated circuit (“Vmin”) can be determined “during testing of the IC (typically by an external tester during manufacturing test).” *Id.*, ¶ 0047. Bilak explains that “[v]arious techniques are well known in the art for determining the Vmin of an IC using an external tester.” *Id.* One example taught by Bilak is to “exercis[e] the microprocessor with functional patterns (in the form of instructions) at some fixed frequency and at various operating voltages.... [and] [t]he last voltage where the IC functioned properly would be its Vmin.” *Id.* Finally, Bilak explains that “[o]ther techniques for determining Vmin using external testers are well[-known] in the art and this invention is not limited by the ones previously described.” *Id.* Accordingly, Bilak discloses “wherein the step of determining is further characterized as performing a test applied externally from

the integrated circuit.” Ex. 1002, ¶ 171.

It would have been obvious to a POSA to modify the voltage switching circuit of Harris in view of Zhang to use the minimum operating voltage, as determined and stored in the manner taught by both Abadeer and Bilak, and a POSA would have been motivated to do so. Ex. 1002, ¶ 172.

Placing the testing circuitry external to the integrated circuit would have been obvious to try. There are only a finite number of identified and predictable solutions for placing the testing circuitry: *i.e.*, the testing circuitry can be placed either internal or external to the integrated circuit. There is nothing non-obvious about either predictable solution. Further, Bilak explicitly teaches both options, *i.e.*, one set of Bilak’s circuitry for determining the minimum operating voltage is external to the integrated circuit and another set is internal to the integrated circuit. Ex. 1007, ¶¶ 0047-0048. Bilak explains that “[v]arious techniques are well known in the art for determining the  $V_{min}$  of an IC using an external tester.” *Id.*, ¶ 0047. It would have been obvious for a POSA to use “well known” external test circuitry, as taught in Bilak, for determining a minimum operating voltage, and a POSA would have had a reasonable expectation of success in doing so for the reasons explained above. Accordingly, Harris in view of Abadeer, Zhang, and Bilak renders claim 8 obvious. Ex. 1002, ¶ 173.

## **XII. CONCLUSION**

Based on the foregoing, claims 1-13 and 15-16 of the '373 patent recite subject matter that is unpatentable. The Petitioner requests institution of an *inter partes* review to cancel these claims.

Respectfully Submitted,

/Benjamin S. Fernandez/

Benjamin S. Fernandez

Reg. No. 55,172

Petition for *Inter Partes* Review of U.S. Patent 7,523,373  
Claims 1-13 and 15-16

**Table of Exhibits for U.S. Patent 7,523,373 Petition for *Inter Partes* Review**

<b>Exhibit</b>	<b>Description</b>
1001	U.S. Patent No. 7,523,373
1002	Declaration of Dr. Adit Singh
1003	U.S. Patent No. 5,867,719
1004	U.S. Patent Application Publication No. 2006/0259840
1005	U.S. Patent Application Publication No. 2003/0122429
1006	U.S. Patent No. 7,702,935
1007	U.S. Patent Application Publication No. 2005/0188230
1008	System-on-Chip for Real-Time Applications (2003)
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1025	U.S. Patent No. 7,484,140
1026	U.S. Patent No. 5,760,624
1027	Declaration of Dr. Sylvia Hall-Ellis

**CERTIFICATE OF COMPLIANCE REGARDING WORD COUNT**

I hereby certify that the foregoing, **Petition for *Inter Partes* Review of U.S. Patent No. 7,523,373**, contains 13,888 words as measured by the word processing software used to prepare the document, in compliance with 37 C.F.R. § 42.24 (d).

Respectfully submitted,

/Benjamin S. Fernandez/

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**CERTIFICATE OF SERVICE**

I hereby certify that on November 20, 2019, I caused a true and correct copy of the foregoing materials:

- Petition for Inter Partes Review
- Certificate of Compliance Regarding Word Count
- Intel Corporation Power of Attorney
- Fee Authorization
- Exhibits 1001-1027

to be served via Fed Ex on the following attorney of record as listed on PAIR:

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