UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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FLEX LOGIX TECHNOLOGIES, INC.
Petitioner

v.

VENKAT KONDA
Patent Owner

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Patent No. 8,269,523

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# PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 8,269,523

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# I. INTRODUCTION

Flex Logix Technologies, Inc. ("Petitioner") requests *inter partes* review ("IPR") of claims 1, 15-18, 20-22, 32, and 47 ("the challenged claims") of U.S. Patent No. 8,269,523 ("the '523 patent") (Ex. 1001), which, according to PTO records, is assigned to Venkat Konda ("Patent Owner" or "PO"). For the reasons set forth in this Petition, the challenged claims should be found unpatentable and canceled.

As explained below (*infra* Section VII.B), during prosecution the Examiner rejected various claims as being anticipated by U.S. Patent No. 6,940,308 to Wong ("*Wong*") (Ex. 1008), PO (then the applicant) amended the claims in response, and after an interview, the Examiner mailed a Notice of Allowance. While it is not clear what PO and the Examiner discussed during the interview (because the interview summary mailed by the Examiner merely reproduces the entirety of amended claim 1), it appears that the Examiner incorrectly relied on a misrepresentation by PO regarding the limitations added in the amendment. (*Infra* Section IX.A.1(k) (discussing PO's statement that in *Wong*, "[i]t is clear as [*Wong*'s routing] network is scaled up, **only columns are increasing**" (Ex. 1004, 63 (applicant's foregoing statement regarding *Wong*) (emphasis added).) As explained below regarding limitation 1(k), *Wong* is not limited to only adding more columns and explicitly

discloses scaling up the network by adding **both columns and rows** (i.e. both vertical and horizontal scaling). (*Infra* Section IX.A.1(k); Ex. 1008, 13:33-49.)

In any event, the Examiner's statement of reasons for allowance indicates that certain limitations of claim 1 (the ones indicated as limitations 1(j) and 1(k) in this Petition) are the only possible distinction over *Wong*. (*Infra* Section VII.B; Ex. 1004, 28 (Notice of Allowance).) As explained in detail below—and supported by previously-absent expert testimony that would have helped the Examiner recognize the inaccuracy of the PO's misrepresentation—the Examiner simply erred in allowing the claims over *Wong*.

## II. MANDATORY NOTICES UNDER 37 C.F.R. § 42.8

### A. Real Parties-in-Interest

Petitioner identifies Flex Logix Technologies, Inc. as the real party-in-interest.

### B. Related Matters

#### 1. Litigations and PTAB Proceedings

PO has asserted the '523 patent against Petitioner in *Konda Technologies Inc. v. Flex Logix Technologies, Inc.*, No. 5:18-cv-07581 (N.D. Cal.). PO has also asserted U.S. Patent Nos. 8,898,611 ("the '611 patent"), 9,529,958 ("the '958 patent"), 10,050,904 ("the '904 patent"), 10,003,553 ("the '553 patent") in the

foregoing district court litigation. The '553 patent is the subject of pending instituted post-grant review (PGR) proceedings PGR2019-00037 and PGR2019-00042. Another PGR petition (in PGR2019-00040) regarding the '553 patent was previously denied.

### 2. Related Applications

The '523 patent issued from U.S. Application No. 12/601,275 ("the '275 application"), which is a national stage entry of International Application PCT/US2008/064605 ("the '605 PCT"), and claims priority to U.S. Provisional Application No. 60/940,394 ("the '394 provisional") filed May 25, 2007.[1,2] Pending U.S. Application No. 16/202,067 claims priority to the '275 application, according to the PTO PAIR database.

### 3. Concurrently-filed petition

Petitioner is concurrently filing two additional petitions for IPR of certain

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[1] Petitioner does not concede that the national stage was properly entered or that the '523 patent properly issued based on such national stage entry. Petitioner reserves the right to assert such issues in other forums. (*See, e.g.*, Ex. 1004, 1-2, 148-159.)

[2] The'605 PCT and the '394 provisional are submitted as Exhibits 1007 and 1026, respectively.

claims of the '523 patent.

### C. Counsel and Service Information

Lead counsel is Naveen Modi (Reg. No. 46,224), and Backup counsel are (1) Joseph E. Palys (Reg. No. 46,508), (2) Paul M. Anderson (Reg. No. 39,896), and (3) Arvind Jairam (Reg. No. 62,759). Service information is Paul Hastings LLP, 875 15th St. N.W., Washington, D.C., 20005, Tel.: 202.551.1700, Fax: 202.551.1705, email: PH-FlexLogix-Konda-IPR@paulhastings.com. Petitioner consents to electronic service.

## III. PAYMENT OF FEES UNDER 37 C.F.R. § 42.15(a)

The PTO is authorized to charge all fees due at any time during this proceeding, including filing fees, to Deposit Account No. 50-2613.

## IV. GROUNDS FOR STANDING UNDER 37 C.F.R. § 42.204(a)

Petitioner certifies that the '523 patent is available for review and Petitioner is not barred or estopped from requesting review on the grounds identified herein.

## V. PRECISE RELIEF REQUESTED AND GROUNDS RAISED

### A. Claims for Which Review is Requested

Petitioner respectfully requests review of claims 1, 15-18, 20-22, 32, and 47 ("challenged claims") of the '523 patent, and cancellation of these claims as unpatentable.

### B. Statutory Grounds of Challenge

The challenged claims should be canceled as unpatentable on the following grounds:

**Ground 1**: Claims 1 and 20-22 are unpatentable under pre-AIA 35 U.S.C. § 102(b) as being anticipated by *Wong*.

**Ground 2**: Claims 15-18, 32, and 47 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over *Wong*.

The '523 patent issued from the '275 application, which claims priority to the '394 provisional filed May 25, 2007 and is a national stage entry of the '605 PCT, which was filed May 22, 2008 and published as International Publication No. WO2008/147928 (Ex. 1005). *Wong* issued on September 6, 2005. Therefore, even if the '523 patent is entitled to the May 25, 2007 priority date of the '394 provisional, *Wong* qualifies as prior art under § 102(b).[3] (*See* Ex. 1002, ¶¶40-45 (overview of *Wong*).)[4]

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[3] Petitioner demonstrates that the '523 patent is not entitled to the priority date of the '394 provisional in the concurrently-filed IPR petitions.

[4] Petitioner submits the declaration of Dr. R. Jacob Baker (Ex. 1002), an expert in the field of the '523 patent. (Ex. 1002, ¶¶1-19; Ex. 1003.)

## VI. LEVEL OF ORDINARY SKILL IN THE ART

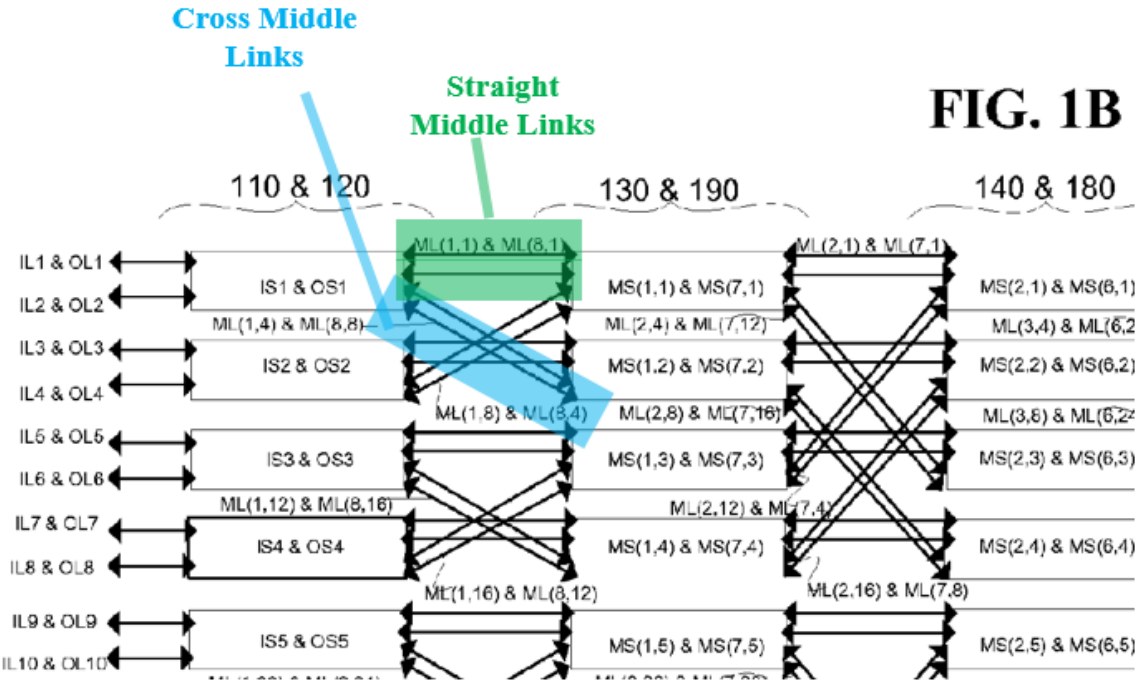
A person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the '523 patent would have had a master's degree in electrical engineering or a similar field, and at least two to three years of experience with integrated circuits and networks. (Ex. 1002, ¶¶18-19.) More education can supplement practical experience and vice versa. (*Id.*)

## VII. OVERVIEW OF THE '523 PATENT

The '523 patent is entitled "VLSI Layouts of Fully Connected Generalized Networks." (Ex. 1001, Title.) The '523 patent acknowledges that multi-stage hierarchical networks were known and used in many applications, including field-programmable gate arrays (FPGAs). (*Id.*, 2:25-27, 2:62-67; Ex. 1002, ¶¶31-38.) The '523 patent contends that prior art network layouts were "inefficient and complicated" (Ex. 1001. 2:28-30, 3:1-6) and alleges to disclose layouts of networks that use horizontal and vertical cross links between switches in succeeding stages. (*Id.*, 3:21-29.)

In addition to inlet and outlet links on the periphery of the network, the '523 patent discloses middle links that provide connections between the switches in the different stages of the network. "The middle links which connect switches in the same row in two successive middle stages are called hereinafter **straight middle**

**links**; and the middle links which connect switches in different rows in two successive middle stages are called hereinafter **cross middle links**." (Ex. 1001, 9:45-49 (emphasis added).) Examples of straight and cross middle links are highlighted in figure 1B below.




(*Id.*, FIG. 1B (excerpt, annotated); Ex. 1002, ¶38.)

As explained below (*infra* Section IX), the above features were all known in the prior art. (*See* Ex. 1002, ¶¶46-170; *see also id.*, ¶¶20-30 (describing the state of the art).)

### A. Prosecution History

During prosecution of the '275 application, the Examiner issued an Office Action rejecting claim 1 (the only independent claim) and other claims as being anticipated by *Wong*. (Ex. 1004, 90-117 (Office Action dated February 7, 2012).) PO amended claim 1 (and other claims) to add certain limitations. (*Id.*, 60-80 (Amendment dated April 30, 2012).)

PO and the Examiner conducted an interview, but it is unclear what was discussed as the interview summary merely reproduces the entirety of claim 1 of the '523 patent. (*Id.*, 57.) After the interview PO filed a supplemental amendment "[t]o correct mistakes [with the format of the claims and not identifying the cancelled claim], and the Examiner mailed a Notice of Allowance stating that:

> the cited prior arts fail to teach said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right, each said plurality of sub-integrated circuit blocks comprising same number of said [stages] and said switches in each said stage, regardless of the size of said two-dimensional grid so that

> each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid, as required by amended claim 1.

(*Id.*, 28.) The foregoing limitations are referred to as limitations 1(j) and 1(k) in this Petition, and are discussed below in Sections IX.A.1(j)-(k).

## VIII. CLAIM CONSTRUCTION

In an IPR, claims are construed in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. 37 C.F.R. § 42.200(b). In particular, claim terms are generally given their "ordinary and customary meaning," that is, "the meaning that the term would have to a POSITA in question at the time of the invention, i.e., as the effective filing date of the patent application." *Phillips v. AWH Corp.*, 415 F.3d 1303, 1313 (Fed. Cir. 2005) (*en banc*). The Board only construes the claims when necessary to resolve the underlying controversy. *Toyota Motor Corp. v. Cellport Systems*, Inc., IPR2015-00633, Paper 11 at 16 (August 14, 2015). Petitioner submits that for purposes of this proceeding, no term of the challenged

claims requires construction.[5] (Ex. 1002, ¶39.)

## IX. DETAILED EXPLANATION OF GROUNDS

### A. Ground 1: *Wong* Anticipates Claims 1 and 20-22

#### 1. Claim 1

##### a) "An integrated circuit device comprising"

To the extent the preamble is limiting, *Wong* discloses the limitations therein. (Ex. 1002, ¶¶50-52.) For instance, *Wong* discloses an FPGA (field-programmable gate array) integrated circuit ("an integrated circuit device"). (*Id.*, ¶50.) *Wong* discloses that "[t]he present invention relates to integrated circuit interconnections and, in particular, to the interconnection architecture of FPGA (Field Programmable

[5] Petitioner reserves all rights to raise claim construction and other arguments in district court as relevant and necessary to those proceedings. For example, Petitioner has not raised all challenges to the '523 patent in this petition, including invalidity under 35 U.S.C. § 112, and a comparison of the claims to any accused products in litigation may raise controversies that need to be resolved through claim construction that are not presented here given the similarities between the references and the patent.

Gate Array) integrated circuits." (Ex. 1008, 1:14-17; *see also id.*, 1:18-21, 1:59-61; Ex. 1002, ¶¶50-51.)

Figures 13A and 13B of *Wong* illustrate exemplary floorplan layouts of FPGAs ("integrated circuit devices"). (Ex. 1008, 3:7-10; 13:19-22, 13:36-38, FIGs. 13A, 13B.)

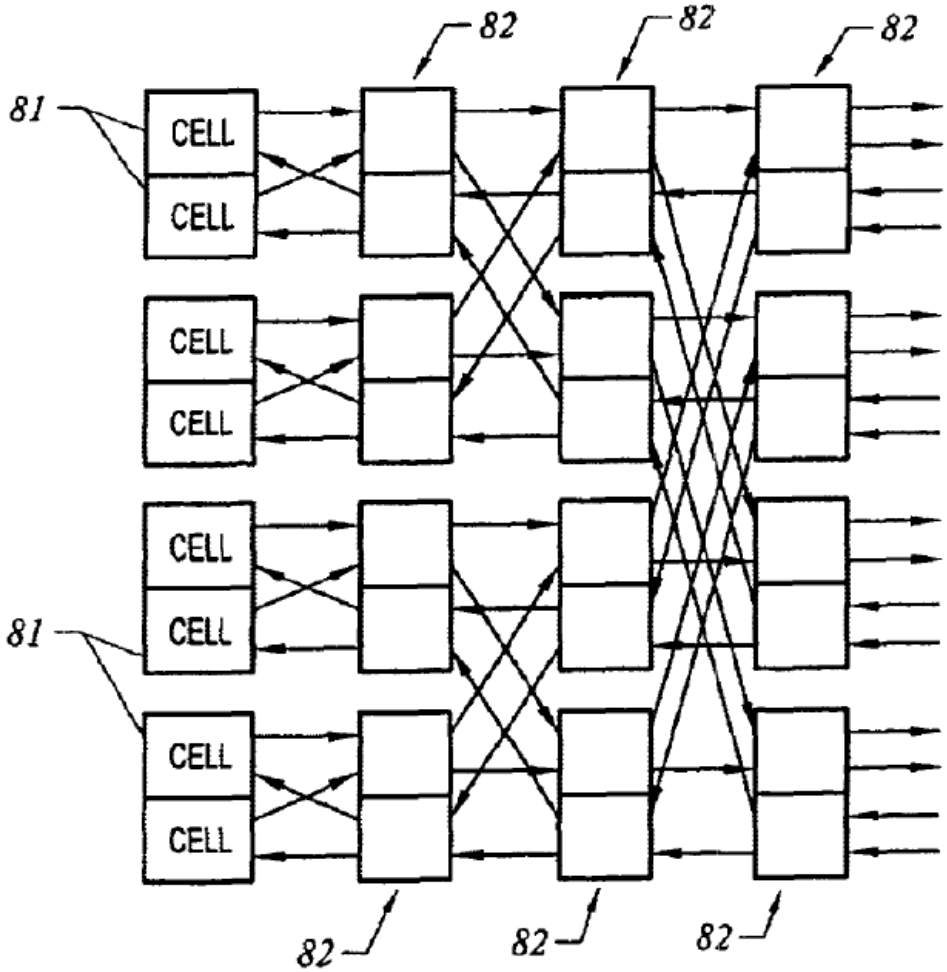



*FIG. 13A*

(Ex. 1008, FIG. 13A; Ex. 1002, ¶52.)

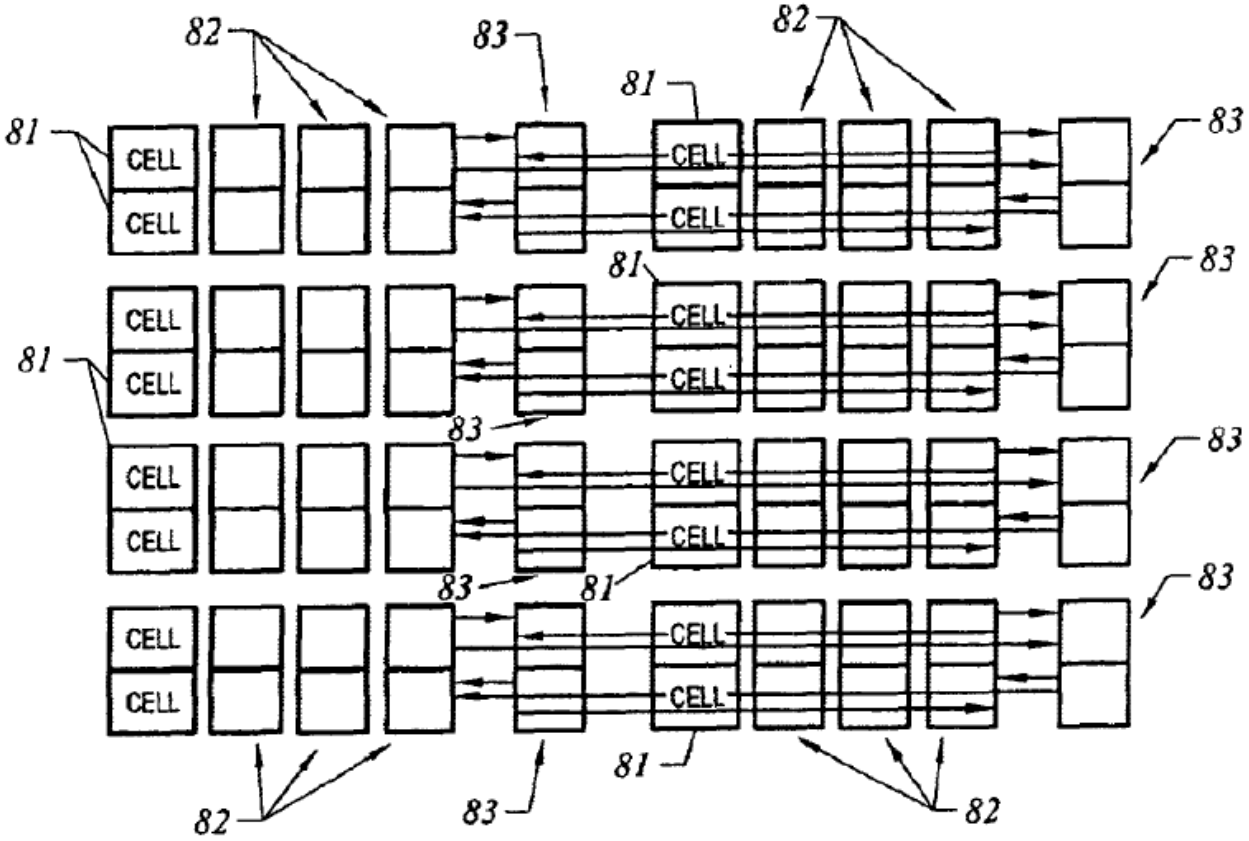



*FIG. 13B*

(Ex. 1008, FIG. 13B; Ex. 1002, ¶52; *see also infra* Sections IX.A.1(b)-(k) regarding the remaining elements of this claim.)

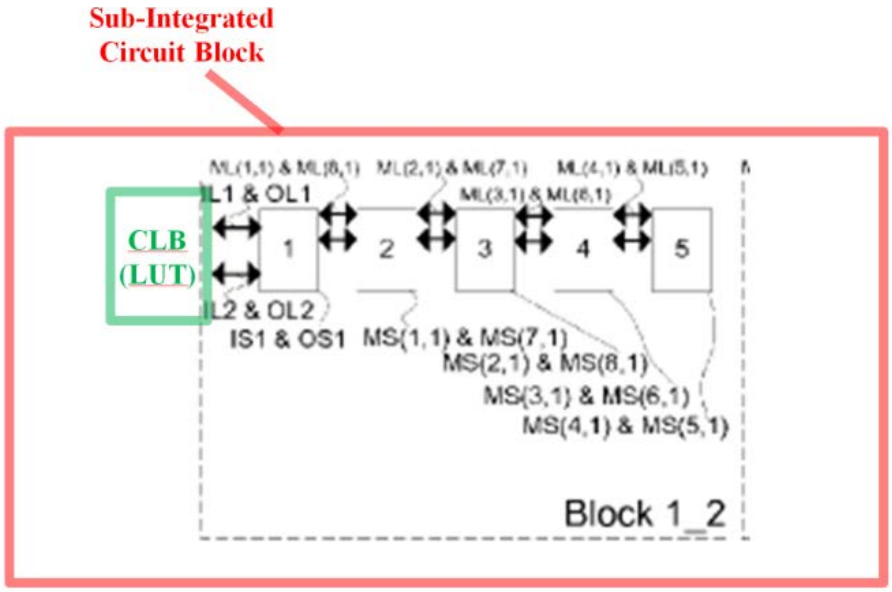
**b) "a plurality of sub-integrated circuit blocks and a routing network"**

*Wong* discloses this limitation. (Ex. 1002, ¶¶53-63.) For instance, *Wong* discloses an integrated circuit (e.g., an FPGA) that includes a plurality of logic cells that are coupled to a programmable network. (Ex. 1008, 1:59-61.)

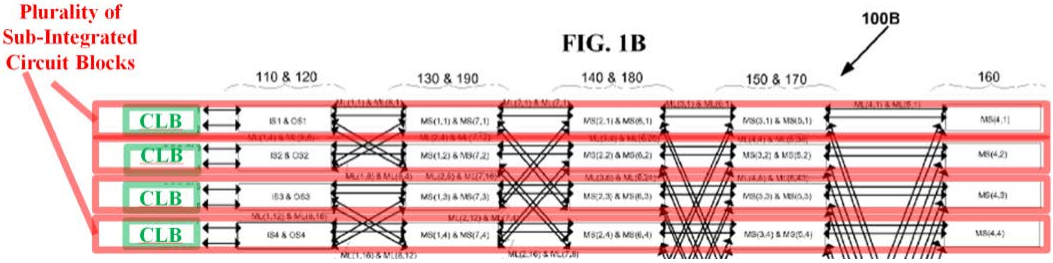
A POSITA would have understood that a "sub-integrated circuit block" in the context of the '523 patent corresponds to a row of switches in a network such as that illustrated in figure 1B in addition to the configurable logic that is coupled to that row. (Ex. 1001, 15:22-24 ("Some of the key aspects of the current invention are discussed. 1) All the switches in one row of the multi-stage network 100B are implemented in a single block."), 13:38-42; Ex. 1002, ¶54.) For example, with respect to figure 1C of the '523 patent, which shows the "blocks" (i.e. sub-integrated circuit blocks) of figure 1B, the '523 patent states that "in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit (hereinafter 'sub-integrated circuit block') depending on the applications in different embodiments." (Ex. 1001, 13:38-42.)

Therefore, in the context of the '523 patent a "sub-integrated circuit block" includes the switches corresponding to a single row (which figure 1C of the '523 patent shows as a single "block") with the addition of "Configurable Logic Blocks (CLB) or any arbitrary digital circuit." (Ex. 1002, ¶55.) The following demonstratives supplied in Dr. Baker's declaration illustrate a "sub-integrated circuit block" in figures 1B and 1C of the '523 patent in the context of how a POSITA would have understood claim 1. (*Id.*) As is apparent from the discussion below,

such an understanding of a "sub-integrated circuit block" is consistent with the other claim limitations. (*Infra* Sections IX.A.1(c)-(k); Ex. 1002, ¶55.)




(Ex. 1001, FIG. 1C (excerpt, annotated); Ex. 1002, ¶55.)




(Ex. 1001, FIG. 1B (excerpt, annotated), Ex. 1002, ¶55.)

In the annotated excerpts of figures 1B and 1C above, each "sub-integrated circuit block" (red box) includes all of the switches in a row and a "Configurable Logic Block[] (CLB) or any arbitrary digital circuit" (green "CLB" box). (Ex. 1002, ¶56.)

*Wong* discloses a plurality of "sub-integrated circuit blocks." (Ex. 1002, ¶57.) The folded network shown below in figure 4C of *Wong* is similar to the folded network shown in figure 1B of the '523 patent. (*Id.*)

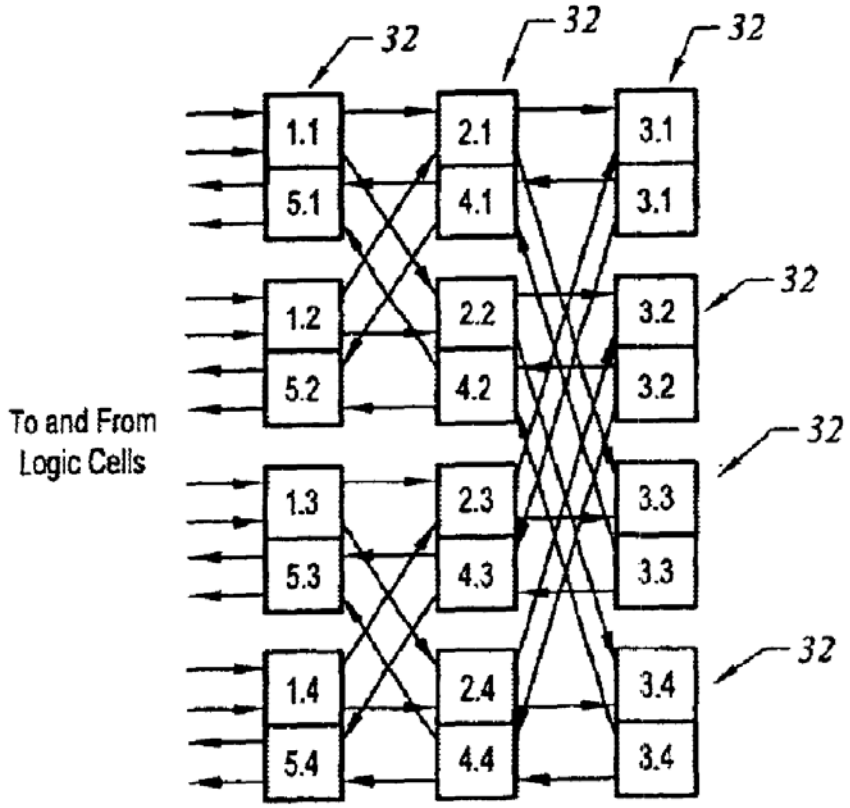
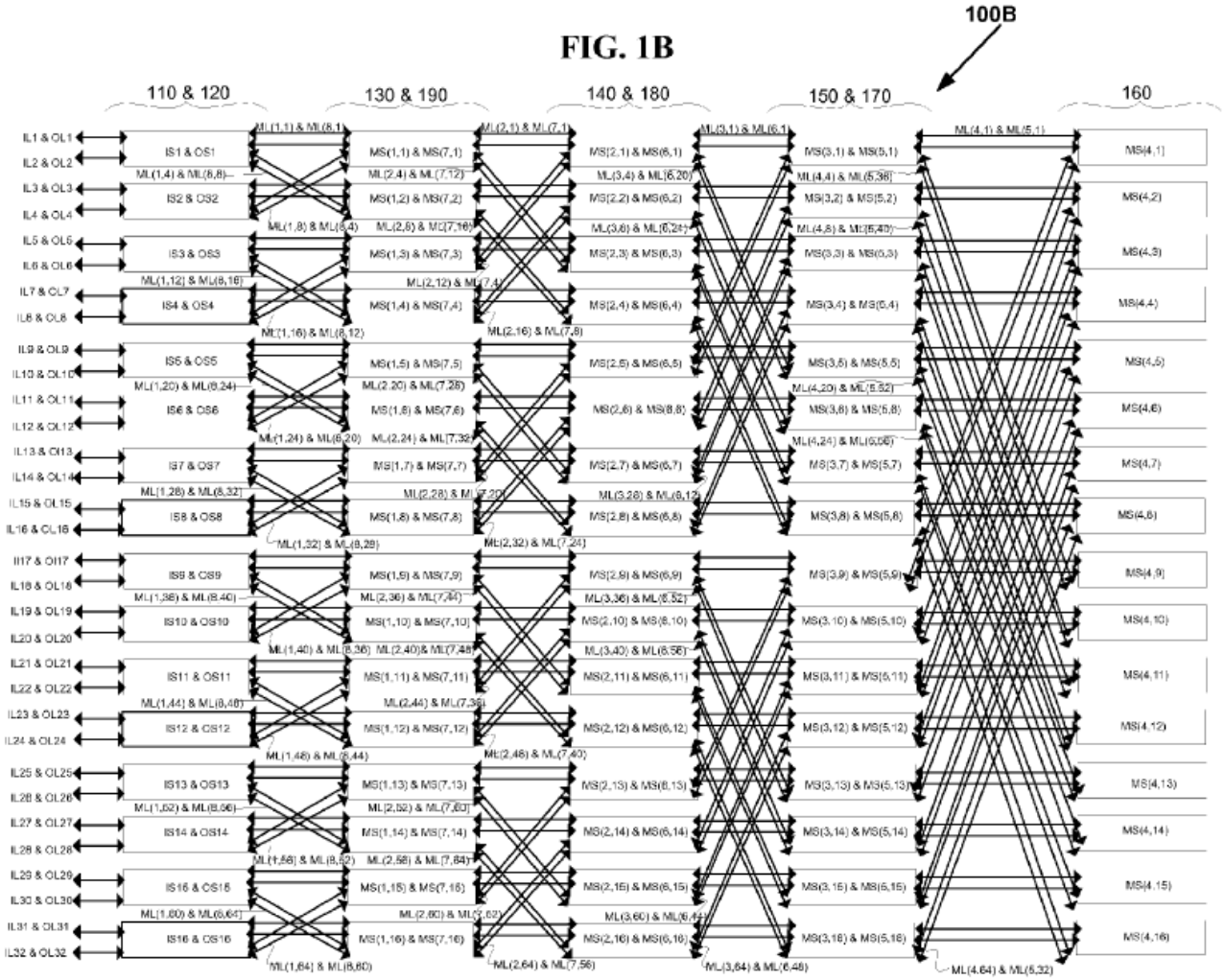



*FIG. 4C*

(Ex. 1008, FIG. 4C; Ex. 1002, ¶57.)




(Ex. 1001, FIG. 1B; Ex. 1002, ¶57.)

Figures 13A and 13B of *Wong* illustrate exemplary floorplan layouts of FPGAs that use a Benes network topology such as that shown in figure 4C. (Ex. 1008, 3:7-10, 13:19-22, FIG. 13A (reproduced below); Ex. 1002, ¶58.) Thus, figure 13A of *Wong* illustrates the network of figure 4C of *Wong* with the addition of logic cells 81. (Ex. 1002, ¶58.)

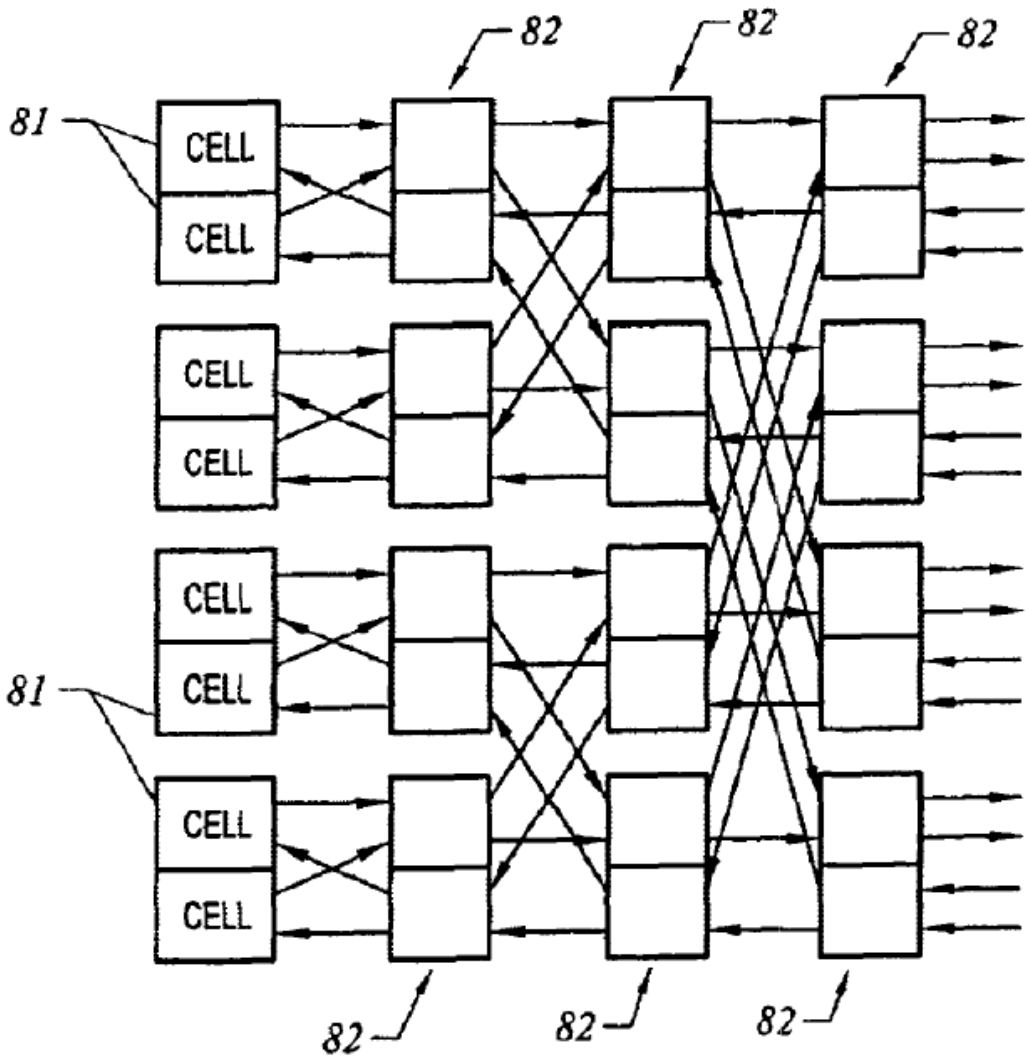



*FIG. 13A*

(Ex. 1008, FIG. 13A; Ex. 1002, ¶58.)

As shown in figure 13A of *Wong*, each row includes a plurality of switches 82 and a pair of logic cells 81. (Ex. 1002, ¶59.) Similarly, figure 13B shows a multi-column embodiment that includes two instantiations of the layout shown in figure 13A. (Ex. 1008, 3:7-10, 13:36-38; Ex. 1002, ¶59.) In each of the two columns

shown in figure 13B, each row includes a plurality of switches 82, 83 and a pair of logic cells 81. (Ex. 1002, ¶59.)

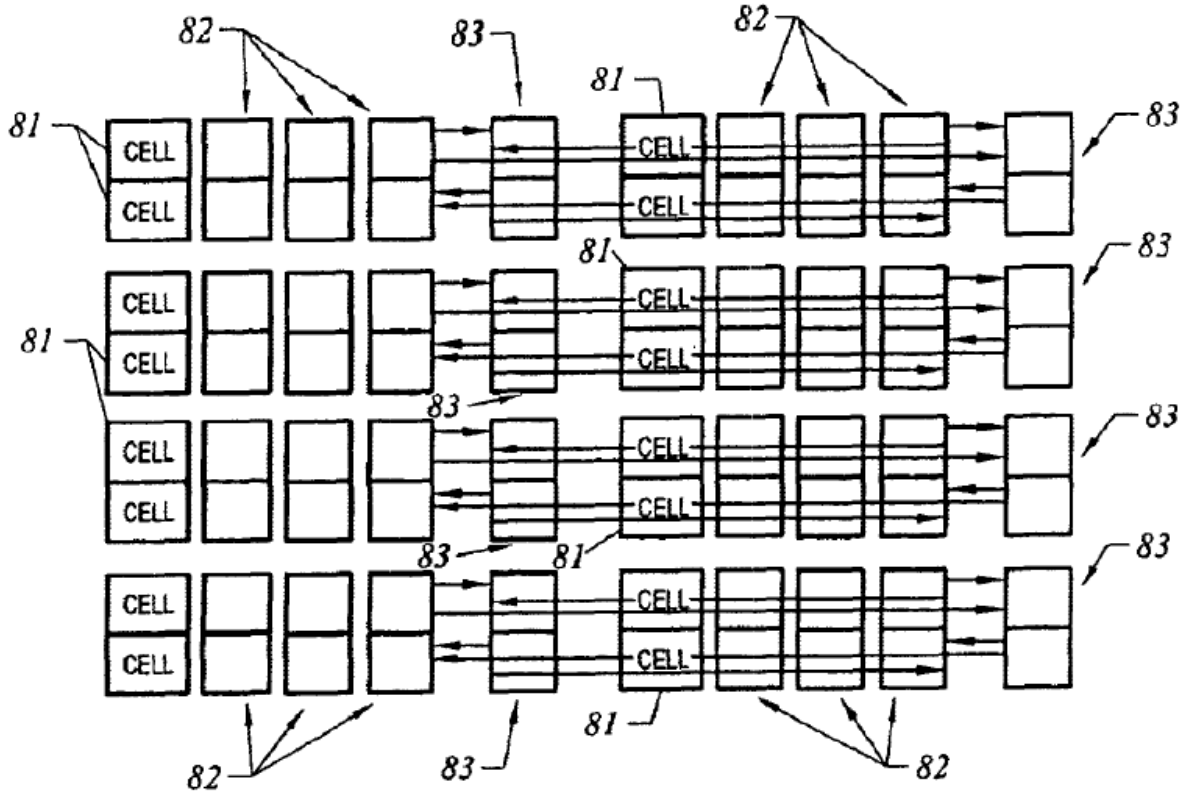



*FIG. 13B*

(Ex. 1008, FIG. 13B; Ex. 1002, ¶59.)

As depicted in figures 13A and 13B, logic cells 81 are included in the FPGA along with switch cells 82 and 83, where the switch cells make up the "routing network" that provides the interconnect in the FPGA. (Ex. 1008, 13:22-23, 13:36-38; Ex. 1002, ¶60.) *Wong* discloses that the logic cells are configurable and can be

programmed to perform desired functions. (Ex. 1008, 3:22-24, 7:34-38; Ex. 1002, ¶¶60-62.)

Therefore, *Wong* discloses "a plurality of sub-integrated circuit blocks and a routing network" as recited in claim element 1(b). (Ex. 1002, ¶63.) *Wong* discloses a plurality of rows of switches and their corresponding logic cells ("plurality of sub-integrated circuit blocks"), where the switches provide the desired interconnects for the network ("routing network") in the FPGA ("integrated circuit device"). (*Id.*)

Annotated figures 13A and 13B below show *Wong's* plurality of sub-integrated circuit blocks and corresponding routing network. (*Id.*, ¶63.)

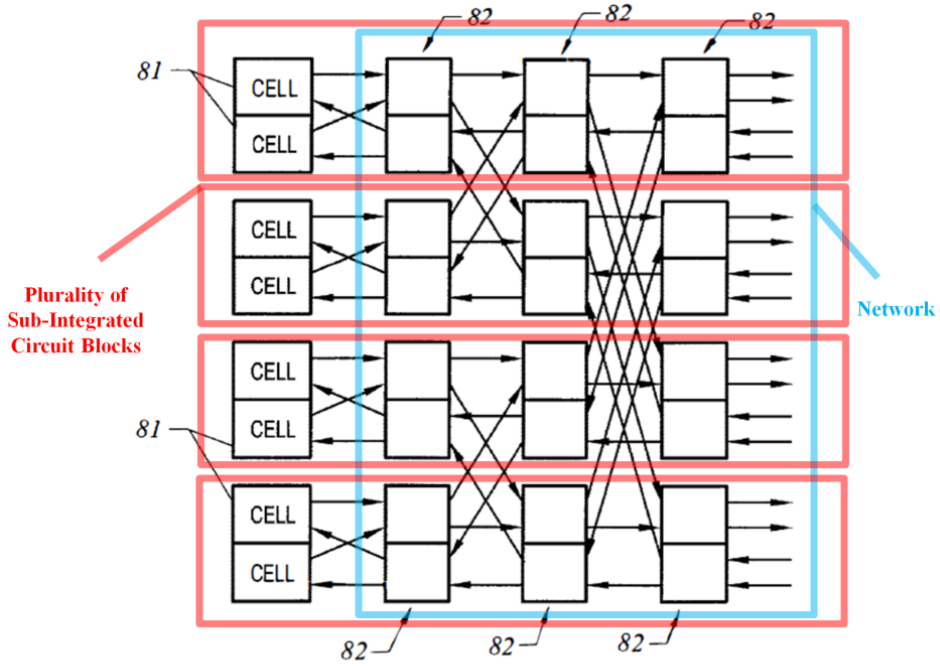



FIG. 13A

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶63.)

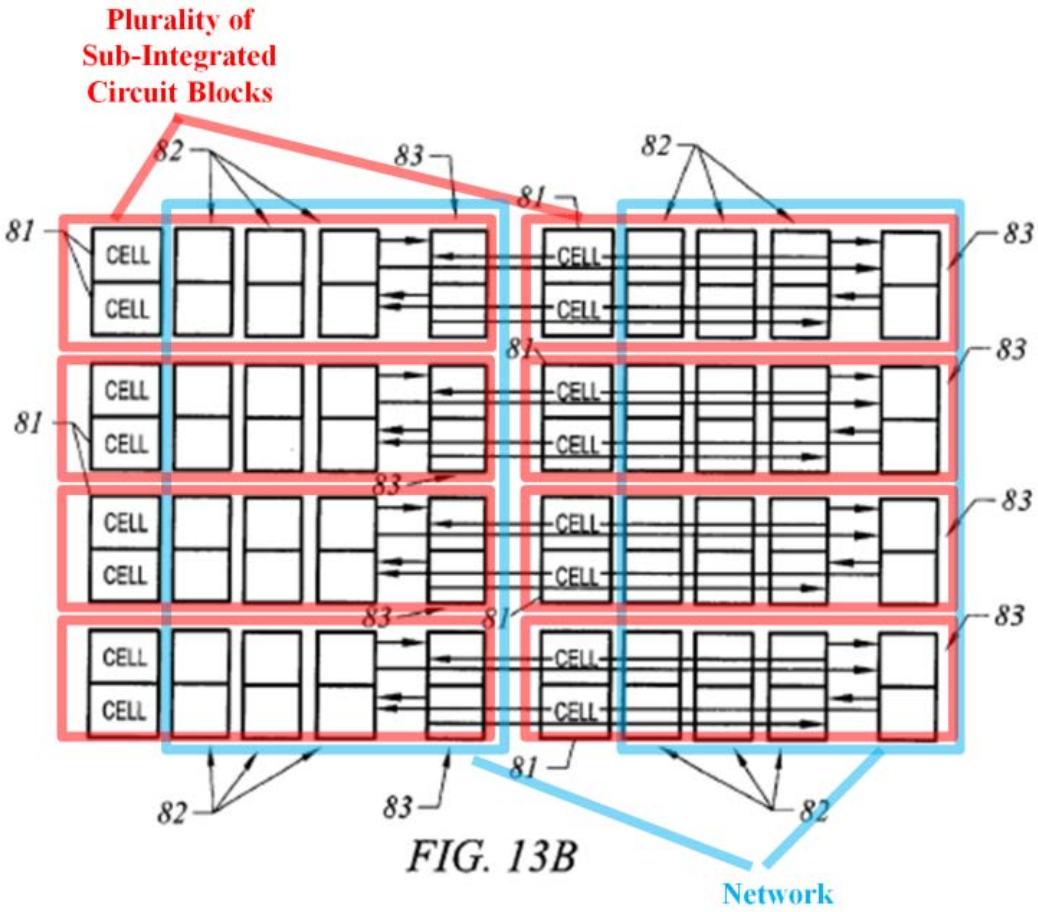



FIG. 13B

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶63.)

**c) "Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links"**

*Wong* discloses this limitation. (Ex. 1002, ¶¶64-68.) For instance, *Wong* discloses that the logic cells 81 included in the "sub-integrated circuit blocks" include output pins ("plurality of outlet links"), which are coupled to inputs of the switches 82 in the first stage of the network. (*Id.*, ¶64.) The logic cells 81 also

include input pins ("plurality of inlet links") that are coupled to outputs of the switches 82 in the first stage of the network inputs. (*Id.*)

For example, as shown in figure 13A of *Wong* (annotated below), each of the two logic cells in each of the "sub-integrated circuit blocks" includes an output pin ("plurality of outlet links") that is coupled to an input of one of the switches 82 in the first stage of the network. (Ex. 1008, FIG. 13A, 13:24-26; Ex. 1002, ¶65.)

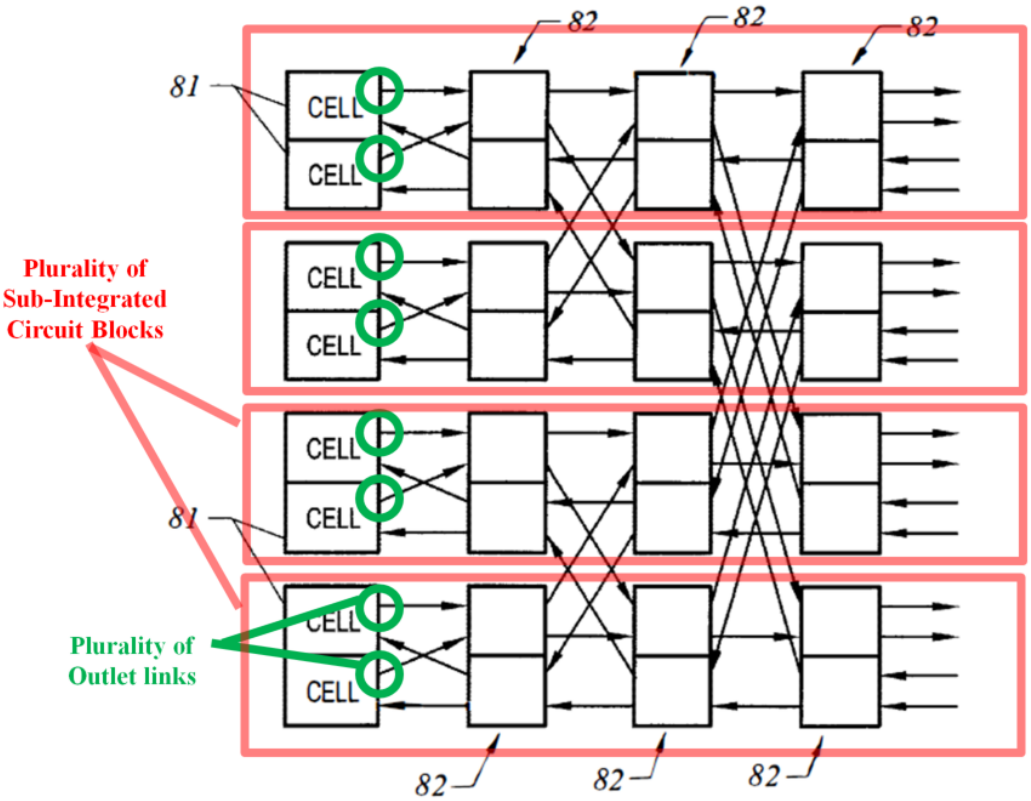



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶65.)

Each of the two logic cells in each sub-integrated circuit block also includes an input pin ("plurality of inlet links") that is coupled to an output of one of the switches 82 in the first stage of the network. (Ex. 1008, FIG. 13A, 13:24-26.)

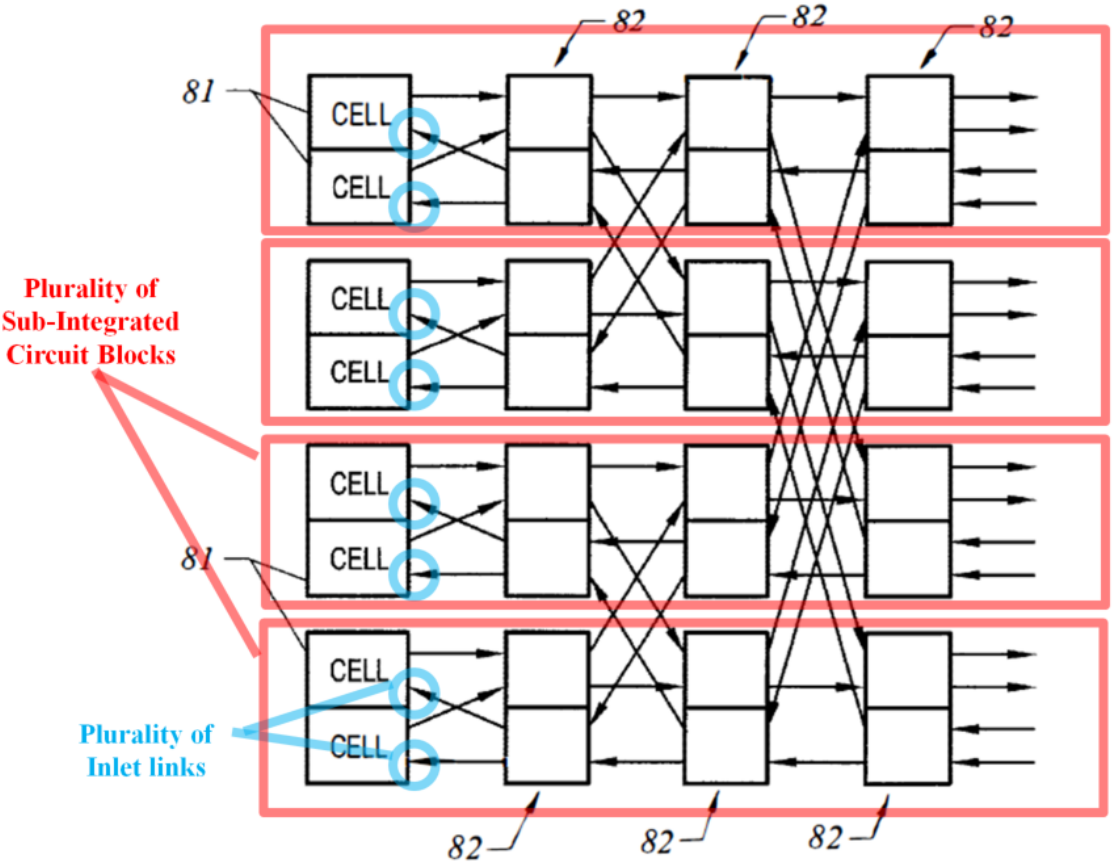


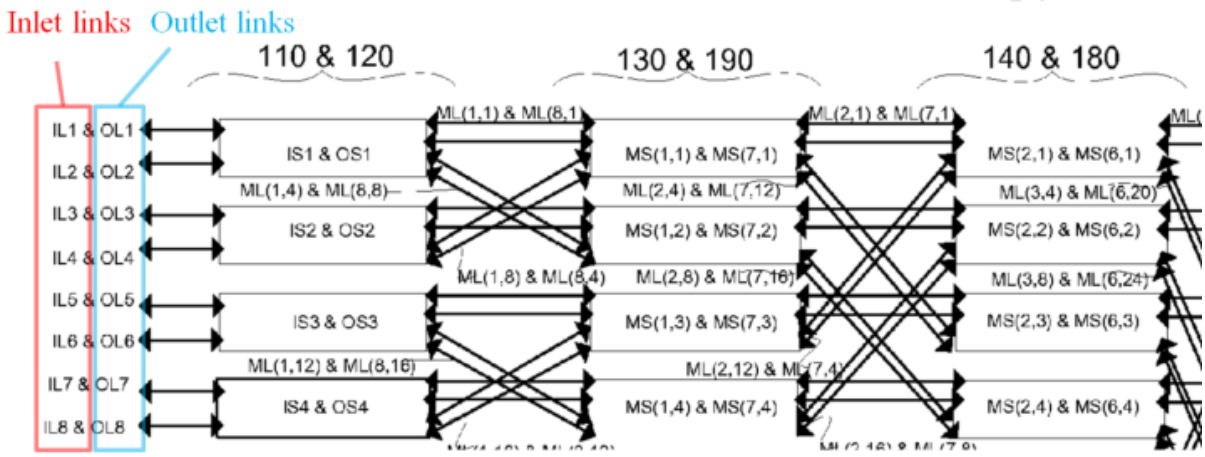

*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶66.)

Because figure 13B of *Wong* includes two instantiations of the layout shown in figure 13A of *Wong*, figure 13B also discloses the claimed "inlet links" and "outlet links" in the same manner described with respect to figure 13A. (Ex. 1008, 13:36-

38; Ex. 1002, ¶67.) The inlet links and outlet links shown in figure 13A of *Wong* above correspond to inlet links and outlet links included in embodiments in the '523 patent. (Ex. 1002, ¶67.) Examples of such inlet links and outlet links are illustrated in an excerpt from figure 1B of the '523 patent annotated below. (Ex. 1001, 12:6-19, FIG. 1B; Ex. 1002, ¶67.)

**FIG. 1B**




(Ex. 1001, FIG. 1B (excerpt, annotated); Ex. 1002, ¶67.)

The inlet links (IL1, IL2, … IL8) and outlet links (OL1, OL2, … OL8) provide connections between the configurable logic blocks and the first stage of switches in the '523 patent in the same manner that the inlet links and outlet links shown above in *Wong* connect the logic cells with the first stage of switches in *Wong's* network. (Ex. 1002, ¶68; Ex. 1001, 8:44-52, 12:6-8.)

**d) "Said routing network comprising of a plurality of stages y, in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y, where y ≥ 1; and"**

*Wong* discloses this limitation. (Ex. 1002, ¶¶69-71.) For example, within the routing network of figure 13A of *Wong*, each sub-integrated circuit block includes three stages (each switch 82 corresponds to a "stage"), and therefore *Wong* discloses the "routing network comprising of a plurality of stages y, in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y, where y ≥ 1." (*Id.*, ¶69.)

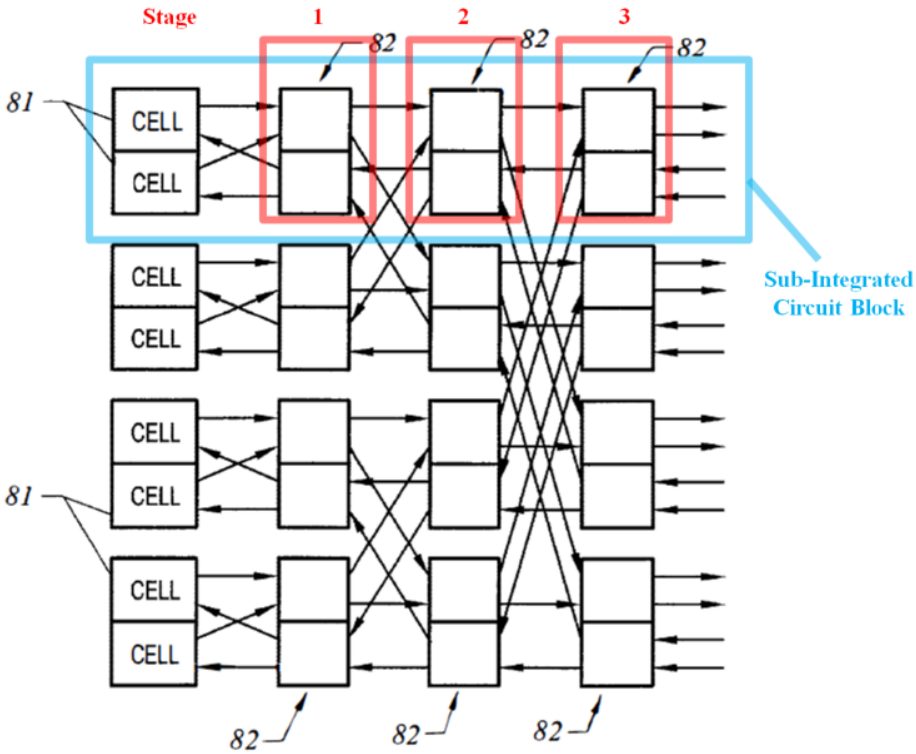



FIG. 13A

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶69.)

Similarly, as shown in figure 13B of *Wong* (annotated below), each sub-integrated circuit block includes four stages (each switch 82, 83 corresponds to a "stage"). (Ex. 1002, ¶70.)

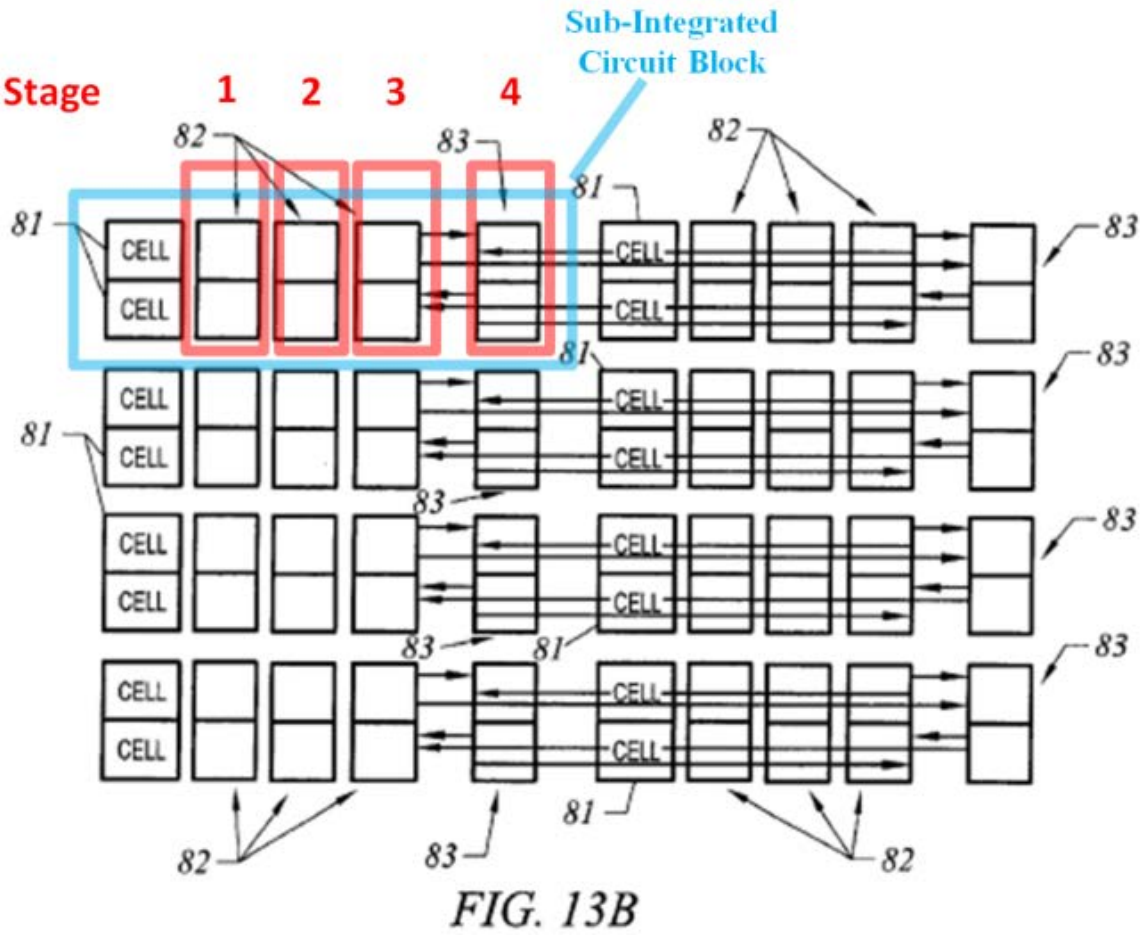



FIG. 13B

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶70.)

*Wong's* disclosure of the sub-integrated circuit blocks including a plurality of stages aligns with the teachings of the '523 patent. (Ex. 1002, ¶71.) For example, the '523 patent states that figure 1A has nine stages (Ex. 1001, 3:51-57), whereas figure 1B has five stages (*id.*, 3:58-64).

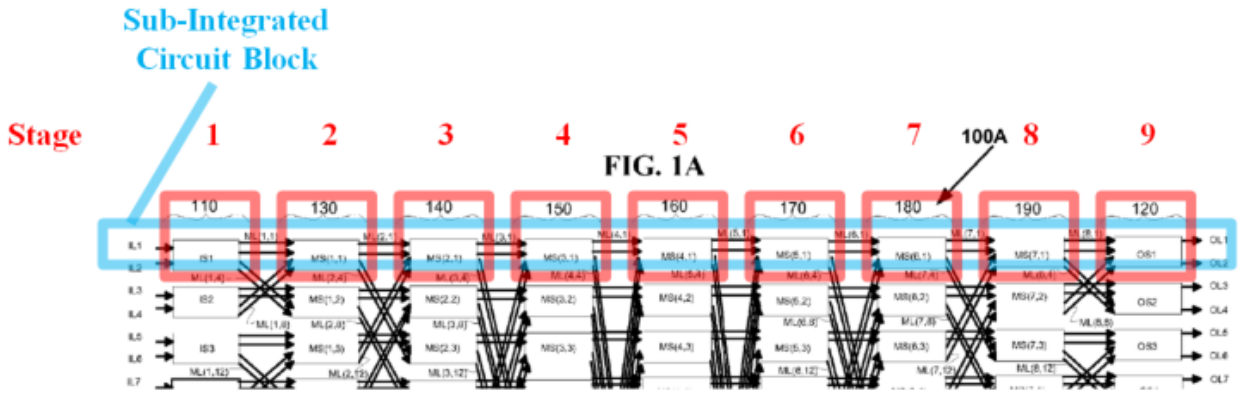



FIG. 1A

(Ex. 1001, FIG. 1A (excerpt, annotated); Ex. 1002, ¶71.)

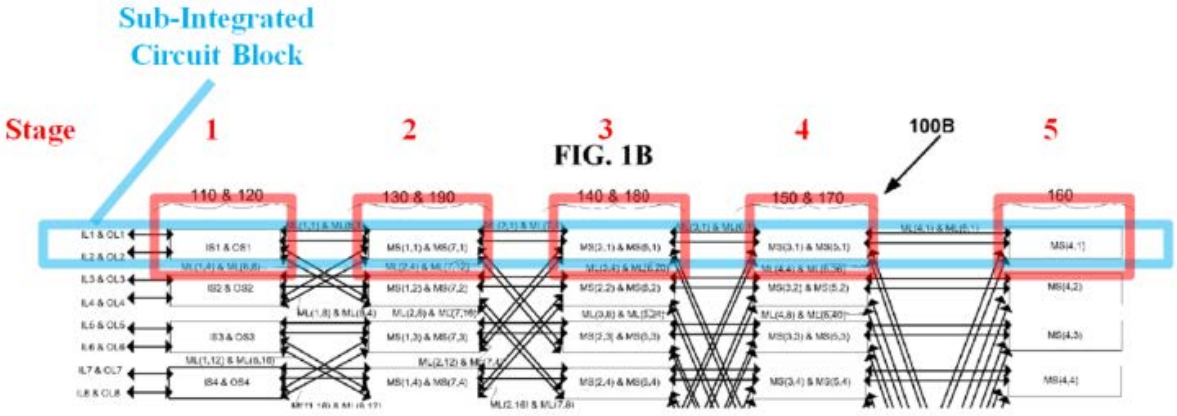



FIG. 1B

(Ex. 1001, FIG. 1B (excerpt, annotated); Ex. 1002, ¶71.)

**e) "Said routing network comprising a plurality of switches of size dxd, where d≥2, in each said stage and each said switch of size dxd having d inlet links and d outlet links; and"**

*Wong* discloses this feature. (Ex. 1002, ¶¶72-83.) According to limitation 1(e), each stage of the network includes a plurality of switches, each of which has at least two inlet links (d inputs) and the same number of outlet links (d outputs).

Notably, in the relevant art of integrated circuits, "a switch of size d x d" in the context of "each said switch of size dxd having d inlet links and d outlet links" would have informed a POSITA about the input/output configuration of the switch, and not the actual area (i.e., physical size) of the switch. (Ex. 1002, ¶72.) In other words, a POSITA would have understood that "size" in the context of this claim term does not refer to the physical measurements of the switch, but instead refers to the number of inputs and outputs. (*Id.*) A POSITA would have understood that a dxd switch is a symmetrical switch in that it has the same number of inputs and outputs. (*Id.*, ¶73 (citing Ex. 1006, 49:1-3).)

As explained below, *Wong* discloses that in the embodiments shown in figures 13A and 13B each stage includes a 4x4 switch that in turn can be made up of multiple 2x2 switches. (Ex. 1002, ¶74.) Therefore, *Wong* discloses "a plurality of switches of size d x d, where $d \geq 2$, in each said stage and each said switch of size d x d having d inlet links and d outlet links." (*Id.*)

Each stage in the sub-integrated circuit blocks shown in figures 13A and 13B includes a switch. (*Id.*, ¶75.) For example, as shown below in figure 13A, each of stages 1-3 includes a switch 82. (Ex. 1008, 13:22-24; Ex. 1002, ¶75.)

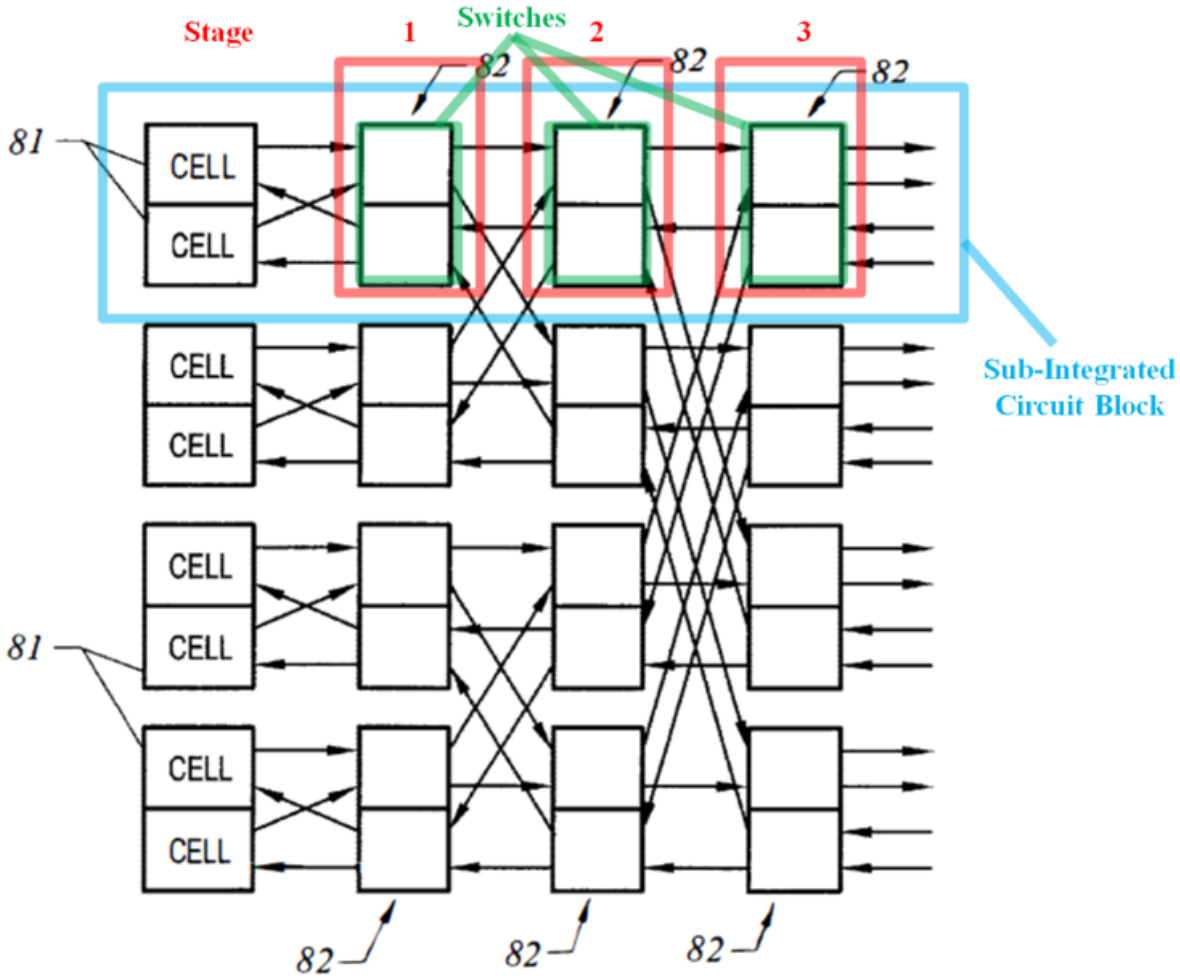



FIG. 13A

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶75.)

Similarly, each stage in each sub-integrated circuit block in figure 13B includes switches 82 and 83. (Ex. 1008, 13:22-24, 13:33-38; Ex. 1002, ¶76.)

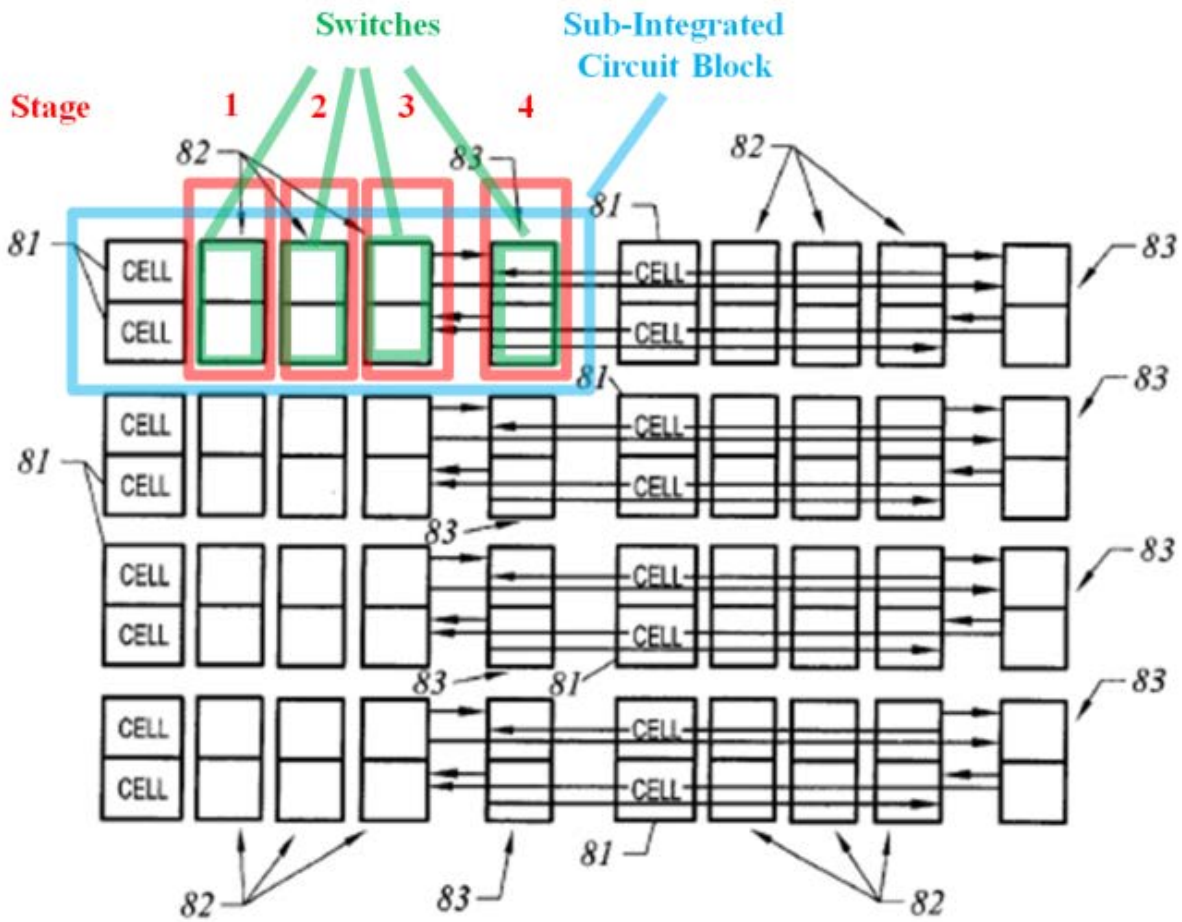



FIG. 13B

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶76.)

As shown in figure 13A, each switch 82 has four inputs and four outputs. (Ex. 1008, FIG. 13A; Ex. 1002, ¶77.) While the switches 83 added in figure 13B only show two inputs and outputs, a POSITA would have understood that there are also

two additional inputs and outputs corresponding to the primary input/output (I/O) of the FPGA, which are not shown in figure 13B, but are shown in figure 13A. (Ex. 1008, FIGs. 13A-13B, 13:42-43 ("As before, each column's top-level inputs and outputs are connected to the primary I/O of the FPGA."); Ex. 1002, ¶77.)

*Wong* discloses that the 4x4 switches shown in figures 13A and 13B can be made up of sets of 2x2 switches such as those shown in figures 2A and 2B. (Ex. 1008, 5:4-6 ("[t]he building block of the described Benes network is the 2x2 (2 input, 2 output) switch 20, having operations illustrated in FIGS. 2A and 2B.").) As further disclosed by *Wong*, "[t]hese 2x2 switches are connected in a specific topology to build a Benes network. (*Id.,* 5:26-27.) Such a Benes network is shown in figure 4B, where figures 13A and 13B are also Benes networks that build on the disclosure corresponding to figure 4B in *Wong*. (*Id.,* 7:6-8, 8:65-9-1, 13:19-22, 13:33-38; Ex. 1002, ¶78.)

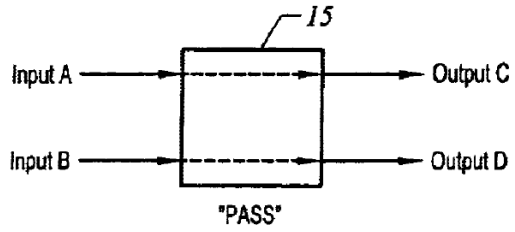



*FIG. 2A*

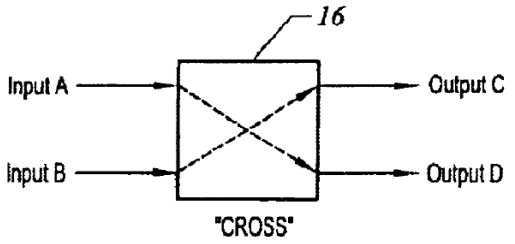



*FIG. 2B*

(Ex. 1008, FIGs. 2A, 2B; Ex. 1002, ¶78.)

Therefore, a POSITA would have understood that all of the switches 82, 83 shown in figures 13A and 13B can be 4x4 switches or a set of two 2x2 switches (such as is shown in figure 4B). (Ex. 1008, FIGs. 13A, 13B, 4B.) As shown in the annotated versions of figure 13A of *Wong* below, each switch cell 82 in each of stages 1-3 can include two 2x2 switches, where each 2x2 switch has two inputs ("d inlet links") and two outputs ("d outlet links"). (Ex. 1002, ¶78.)

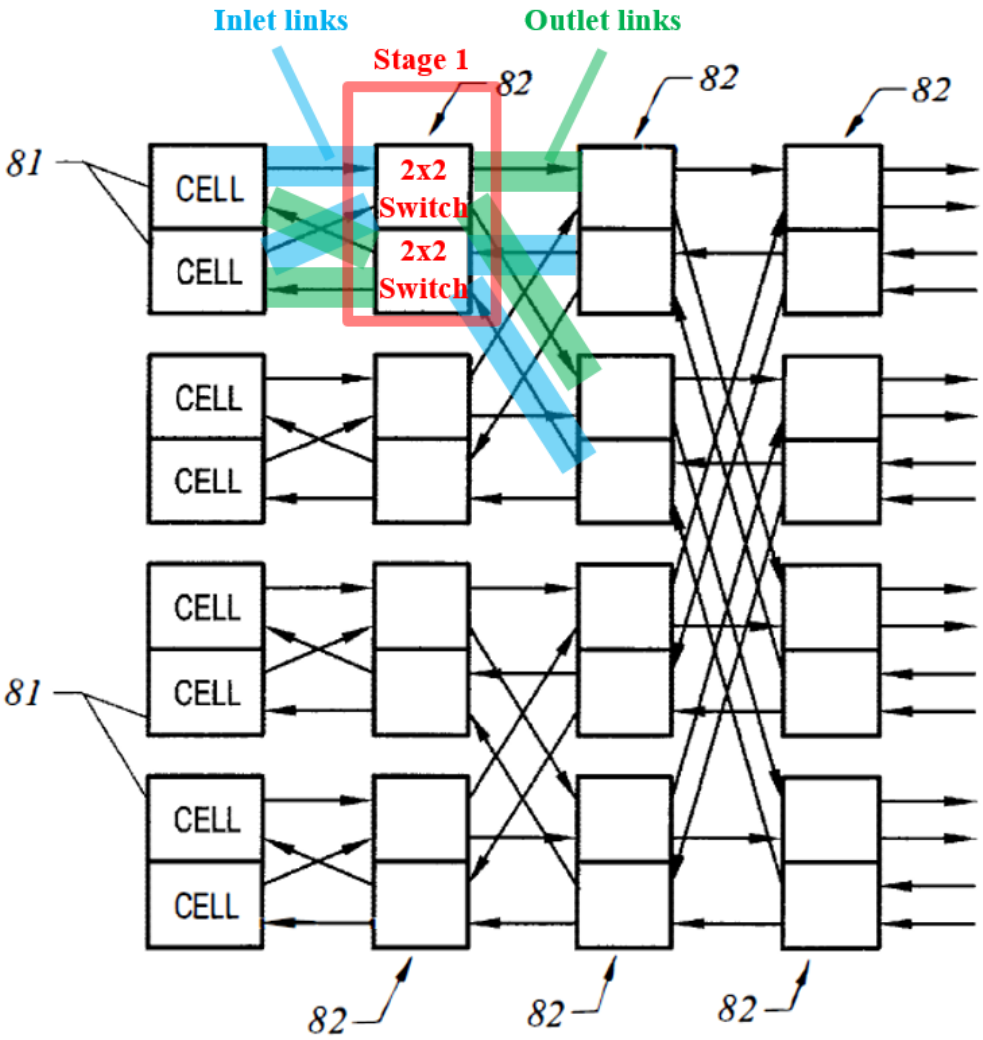



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶79.)

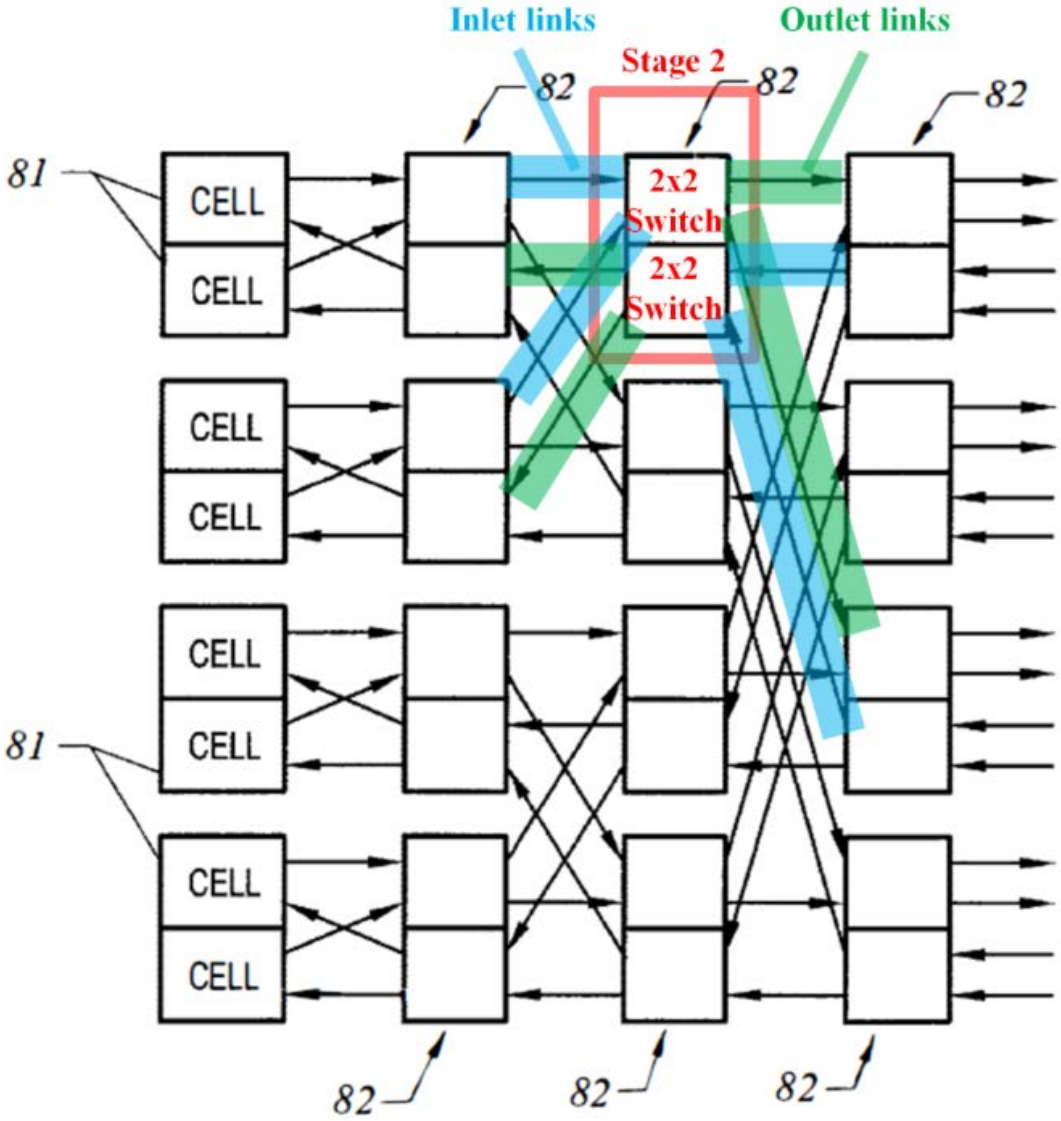



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶79.)

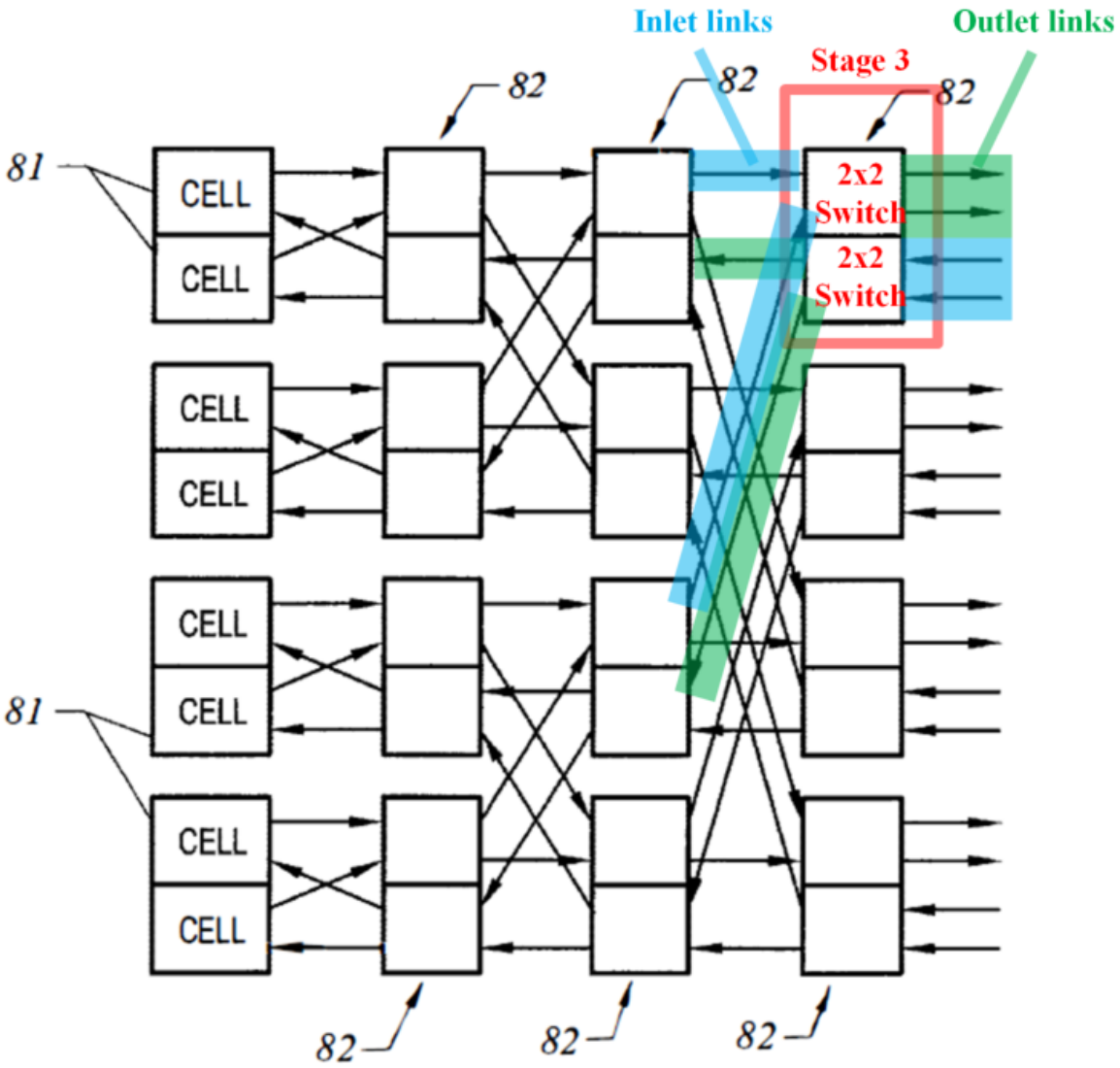



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶79.)

As disclosed by *Wong*, figure 13B includes two instantiations of figure 13A with the addition of another stage of switches 83. (Ex. 1008, 3:7-10, 13:36-38; Ex. 1002, ¶80.) Therefore, like the network of figure 13A, each switch in each of the

stages in figure 13B can be implemented using two 2x2 switches, where each switch has two incoming links and two outgoing links. (Ex. 1002, ¶80.)

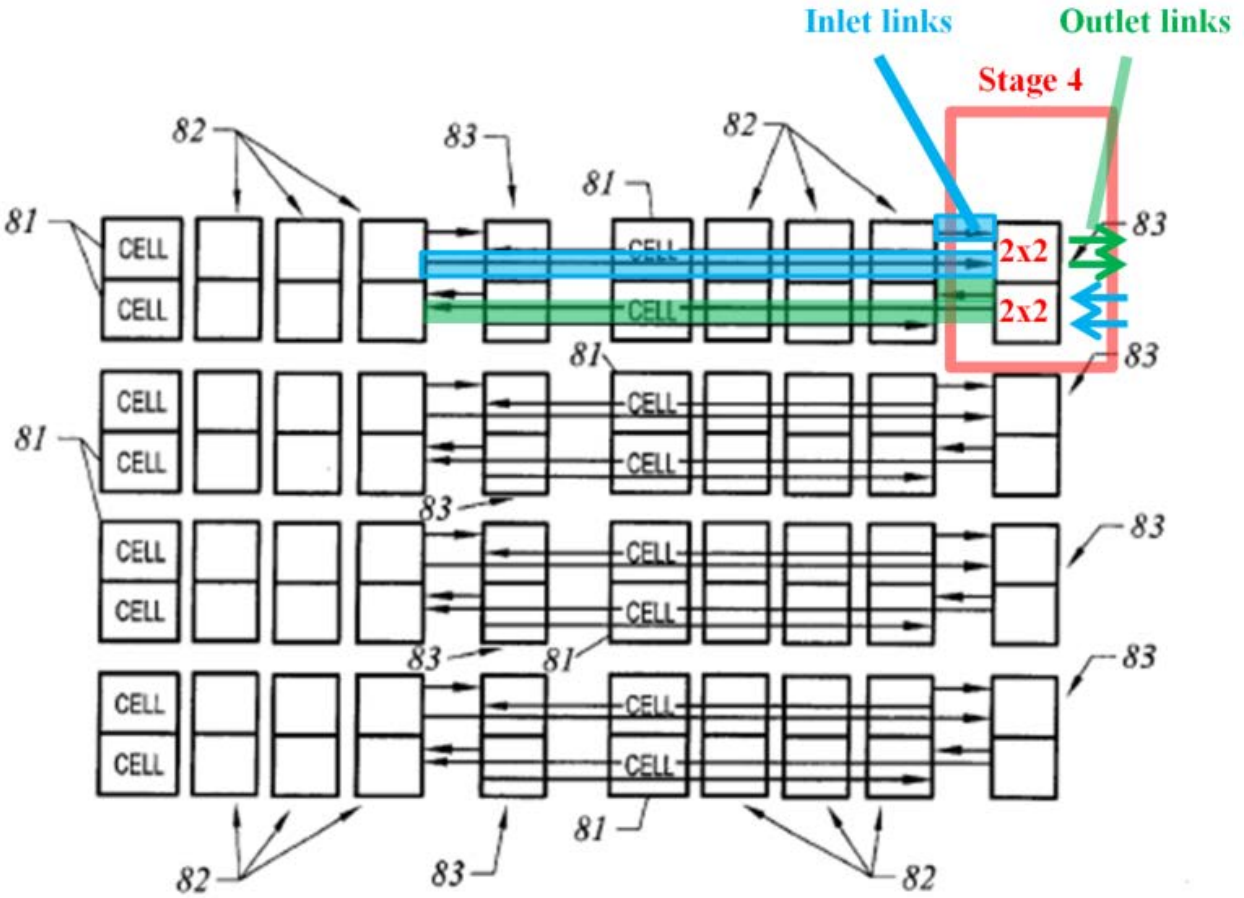



FIG. 13B

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶80.)

Annotated figure 13B above shows the inlet links and outlet links corresponding to the primary I/O of the FPGA. (Ex. 1008, 13:41-42 ("As before each columns top-level inputs and outputs are connected to the primary I/O of the

FPGA."); Ex. 1002, ¶81.) As such, each switch 83 includes two 2x2 switches, each of which has two incoming links and two outgoing links. (Ex. 1002, ¶81.)

Because the network includes a plurality of sub-integrated circuit blocks, each stage includes a plurality of 4x4 switches, where those 4x4 switches can be implemented as a plurality of 2x2 switches. (*Id.*, ¶82.) For example, because there are four sub-integrated circuit blocks in the network of figure 13A, each of stages 1-3 in the routing network has four 4x4 switches (one 4x4 switch per sub-integrated circuit block in each of stages 1-3). (*Id.*) If the 4x4 switches are implemented using 2x2 switches, then each stage includes eight 2x2 switches (two 2x2 switches per stage). (Ex. 1008, FIG. 13A; Ex. 1002, ¶82.) For the embodiment in figure 13B, there are eight sub-integrated circuit blocks and therefore each stage includes eight 4x4 switches or 16 2x2 switches. (Ex. 1008, FIG. 13B.) Therefore, *Wong* discloses "said routing network comprising a plurality of switches of size dxd, where d≥2, in each said stage and each said switch of size dxd having d inlet links and d outlet links." (Ex. 1002, ¶82.)

Notably, a POSITA would have understood that limitation 1(e) does not require a plurality of dxd switches **in each stage in each sub-integrated circuit block**, but instead simply requires a plurality of dxd switches **in each stage of the routing network**. (Ex. 1002, ¶83.) Original claim 1 of the '275 application

included, in addition to the feature that issued as limitation 1(e), an additional limitation that required "[s]aid each sub-integrated circuit block comprising a plurality of said switches corresponding to each stage." (Ex. 1004, 217 (lines 15-16), 325 (lines 15-16).) But that additional feature, which required a plurality of dxd switches in each stage in **each sub-integrated circuit block**, was deleted by PO during prosecution. (*Id.*, 67.)

> **f)** "**Said plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1; and**"

*Wong* discloses this limitation. (Ex. 1002, ¶¶84-86.) For example, as shown in figure 13A of *Wong* (annotated below), each of the output pins ("outlet links") of the logic cells in each sub-integrated circuit block is directly connected to a corresponding inlet link of the first stage ("said lowest stage of 1") of the same sub-integrated circuit block. (*Id.*, ¶84.)

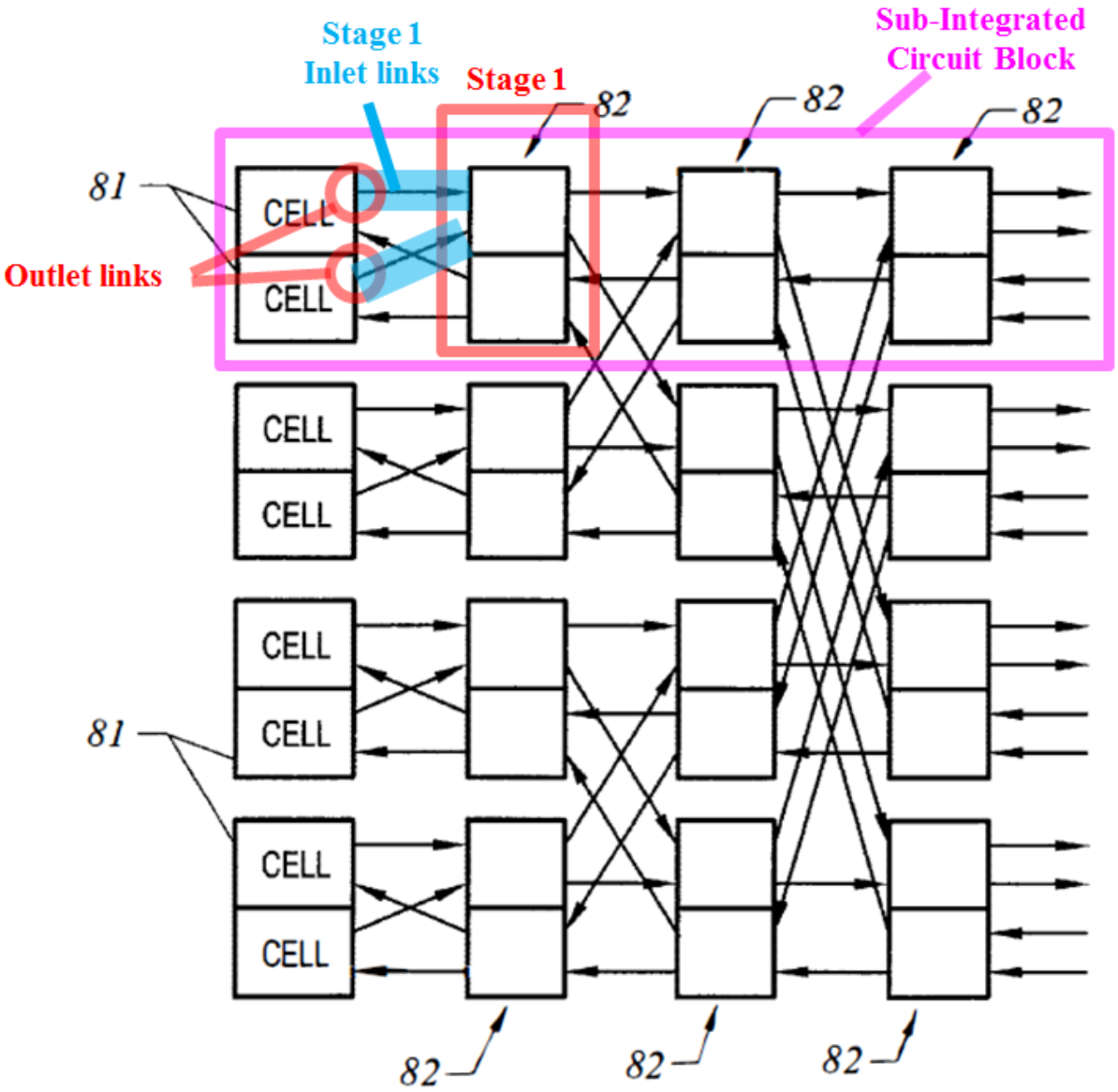



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶84.)

Similarly, as shown in figure 13A of *Wong*, each of the input pins ("inlet links") of the logic cells in each sub-integrated circuit block is directly connected to a corresponding outlet link of the first stage ("said lowest stage of 1") of the same sub-integrated circuit block. (Ex. 1002, ¶85.)

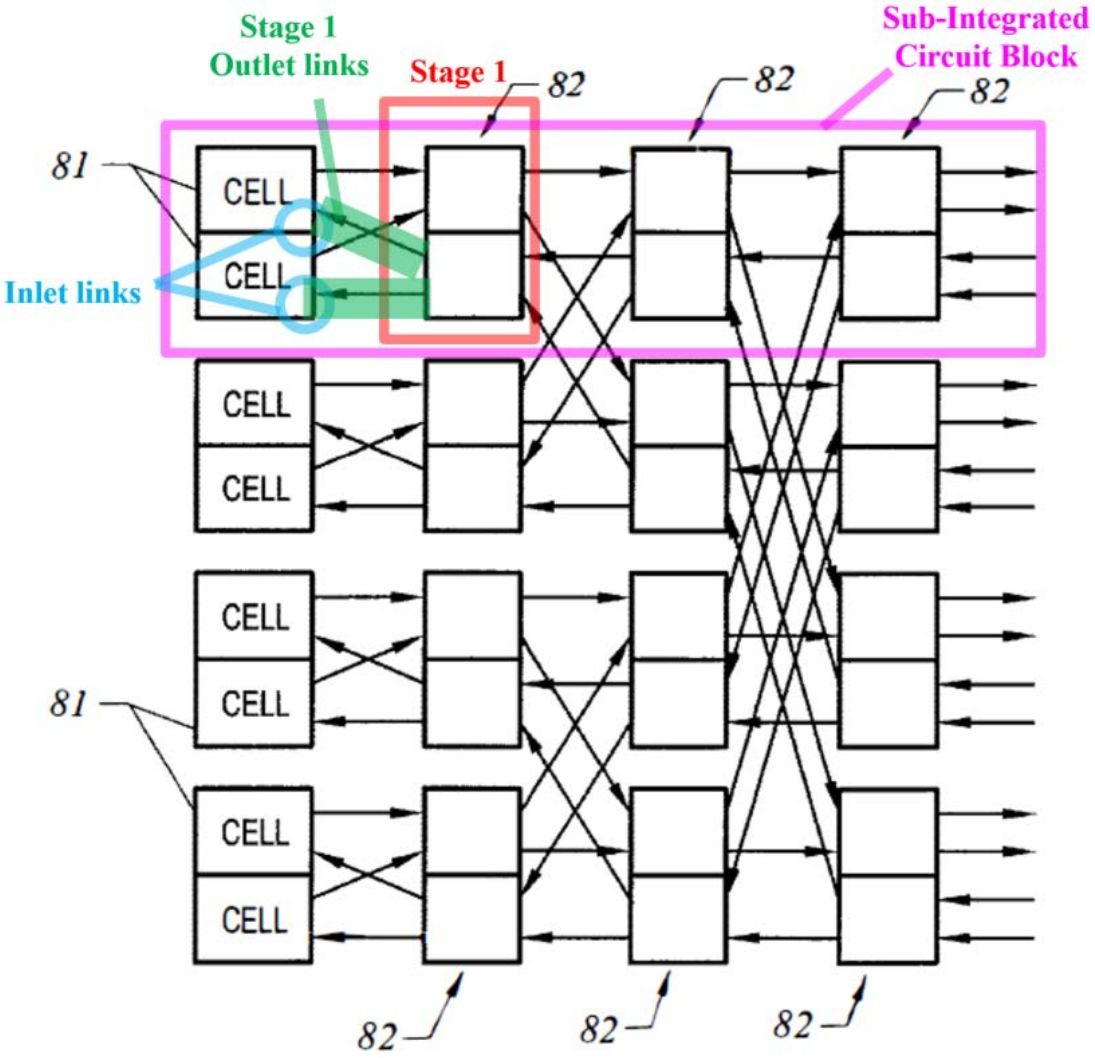



FIG. 13A

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶85.)

While not explicitly shown in figure 13B of *Wong*, the connections between the logic cells and stage 1 switches of the sub-integrated circuit block are also present in figure 13B because figure 13B includes two instantiations of the circuitry and connections shown in figure 13A. (Ex. 1008, 13:36-38; Ex. 1002, ¶86.) Therefore, each of the embodiments shown in figures 13A and 13B of *Wong* discloses the claimed feature. (Ex. 1002, ¶86.)

**g)** "**Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in a lower stage to switches in its immediate succeeding higher stage, and also comprising a plurality of backward connecting links connecting from switches in a higher stage to switches in its immediate preceding lower stage; and**"

*Wong* discloses this limitation. (Ex. 1002, ¶¶87-95.) Consistent with '523 patent specification and other claimed features, "forward connecting links" include links from switches in a lower stage to an immediately succeeding higher stage in the same or a different sub-integrated circuit block. Such an assumption is consistent with the forward connecting links including cross links and straight links in claim limitation 1(h), as the '523 patent specification defines "cross links" to be between successive stages in *different* blocks, whereas "straight links" are links between successive stages in the *same* block. (Ex. 1001, 9:45-49; Ex. 1002, ¶87.)

As illustrated in annotated figure 13A of *Wong* below, each sub-integrated circuit block includes "a plurality of forward connecting links." (Ex. 1002, ¶88.) For example, the top-most sub-integrated circuit block (highlighted in purple) includes a plurality of forward connecting links (highlighted in green). (*Id.*) Each of the forward connecting links shown is connected from a switch in a lower stage to a switch in an immediately succeeding higher stage. (*Id.*)

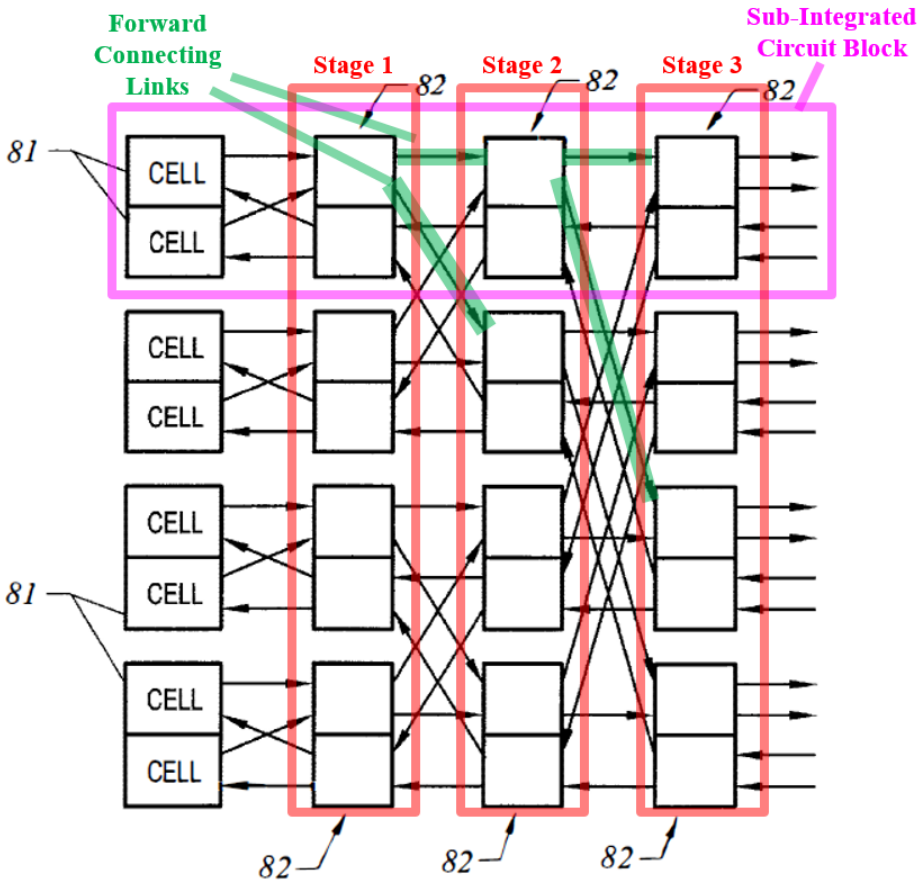



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶88.)

The forward connecting links shown in annotated figure 13A above are connected from switches in stage 1 ("a lower stage") to switches in stage 2 ("an immediate succeeding higher stage") or from switches in stage 2 ("a lower stage") to switches in stage 3 ("an immediate succeeding higher stage"). (Ex. 1002, ¶89.) While the annotations above are only used to highlight the forward connecting links in the top sub-integrated circuit block, figure 13A shows that each of the sub-integrated circuit blocks includes a plurality of forward connecting links. (*Id.*)

Figure 13B also includes a plurality of forward connecting links in each of the sub-integrated circuit blocks. (*Id.*, ¶90.) In addition to the forward connecting links described above with respect to figure 13A, which are also present in the embodiment of figure 13B, figure 13B shows additional forward connecting links between stage 3 and the added stage 4 for each sub-integrated circuit block. (*Id.*) The additional forward connecting links shown in annotated figure 13B below are connected from switches in stage 3 ("a lower stage") to switches in stage 4 ("an immediate succeeding higher stage"). (*Id.*)

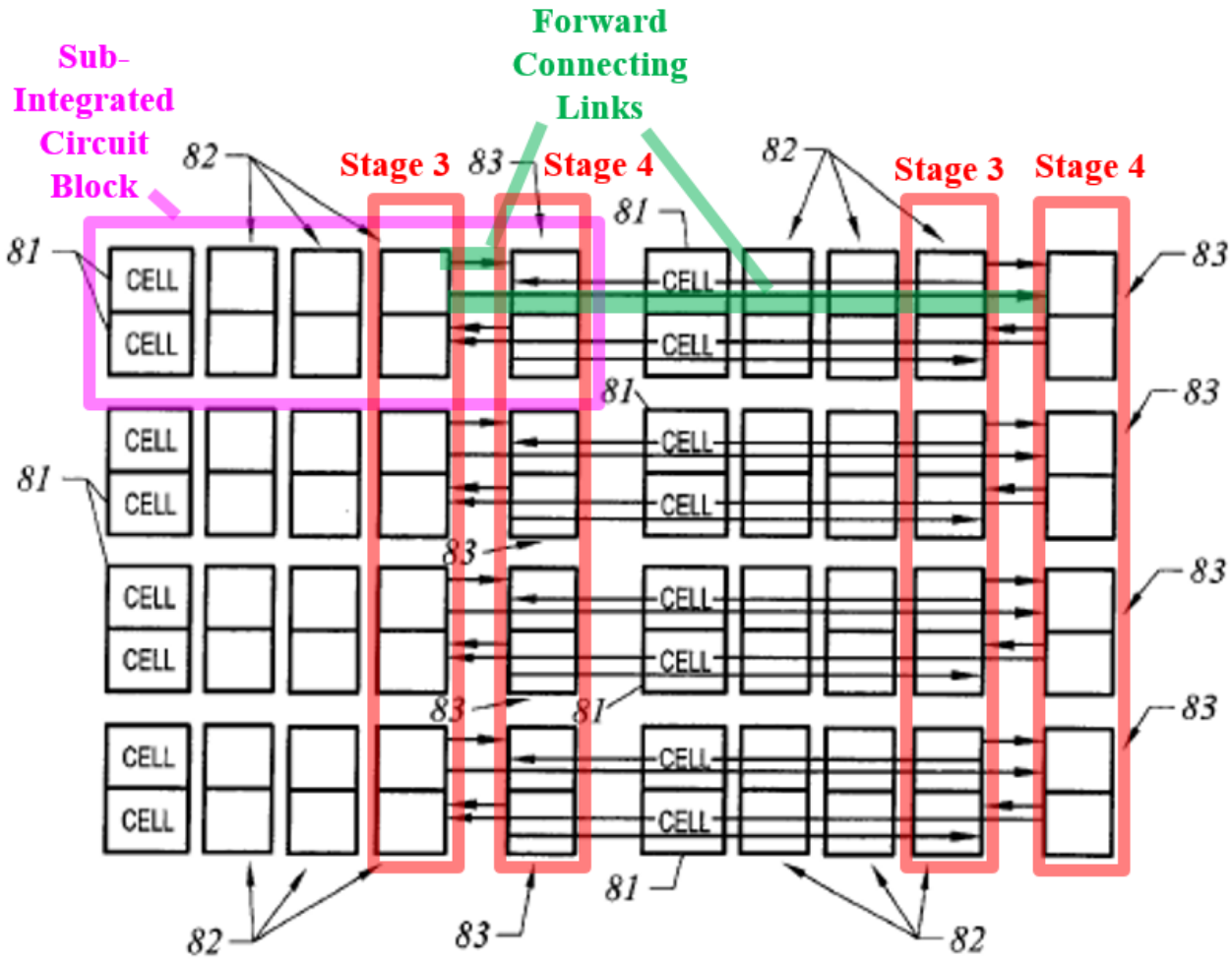



*FIG. 13B*

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶90.)

While the annotations above are only used to highlight the forward connecting links in the top-left sub-integrated circuit block, each of the sub-integrated circuit blocks in figure 13B includes a plurality of forward connecting links. (Ex. 1002, ¶91.)

*Wong* also discloses backward connecting links as recited in limitation 1(g). (*Id.*, ¶92.) As illustrated in figure 13A of *Wong*, each sub-integrated circuit block includes a plurality of backward connecting links. (*Id.*) For example, as shown in annotated figure 13A below, the top-most sub-integrated circuit block (highlighted in purple) includes a plurality of backward connecting links (highlighted in blue). (*Id.*) Each of the backward connecting links shown is connected from a switch in a higher stage to a switch in an immediately preceding lower stage. (*Id.*)

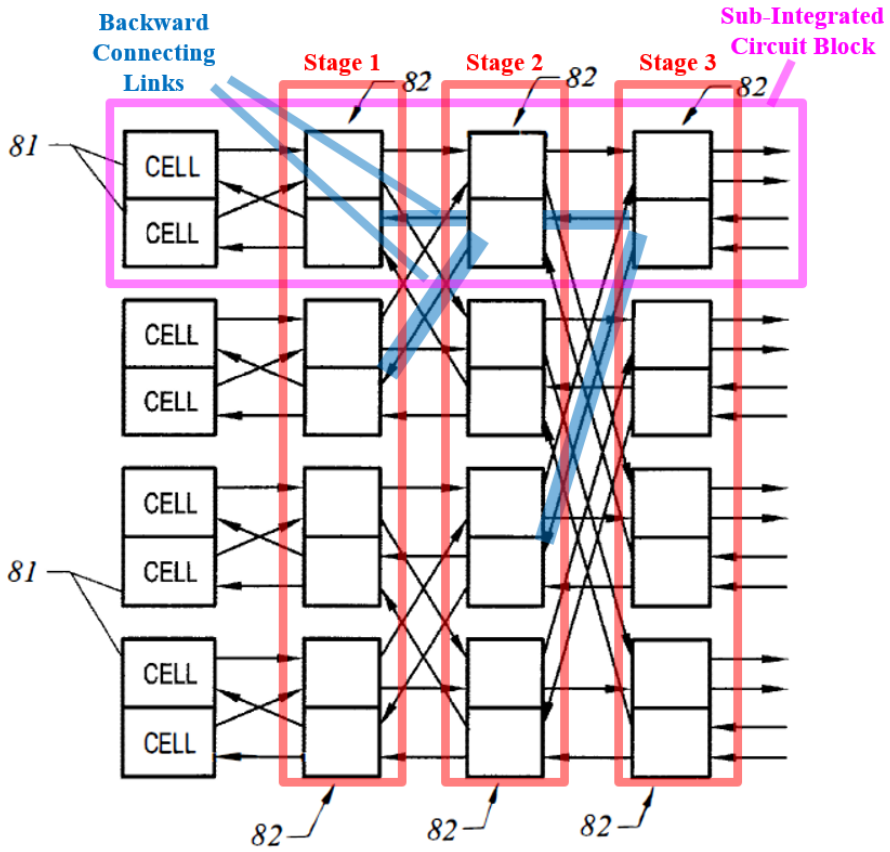



FIG. 13A

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶92.)

The backward connecting links shown in annotated figure 13A above are connected from switches in stage 2 ("a higher stage") to switches in stage 1 ("an immediate preceding lower stage") or from switches in stage 3 ("a higher stage") to switches in stage 2 ("an immediate preceding lower stage"). (Ex. 1002, ¶93.) While the annotations above are only used to highlight the backward connecting links in the top sub-integrated circuit block, figure 13A shows that each of the sub-integrated circuit blocks includes a plurality of backward connecting links. (*Id.*)

Figure 13B also includes a "plurality of backward connecting links" in each of the sub-integrated circuit blocks. (*Id.*, ¶94.) In addition to the backward connecting links described above with respect to figure 13A, which are also present in the embodiment shown in figure 13B, figure 13B includes additional backward connecting links between the added stage 4 and stage 3 for each sub-integrated circuit block. (*Id.*) The additional backward connecting links highlighted in annotated figure 13B below are connected from switches in stage 4 ("a higher stage") to switches in stage 3 ("an immediate preceding lower stage"). (*Id.*)

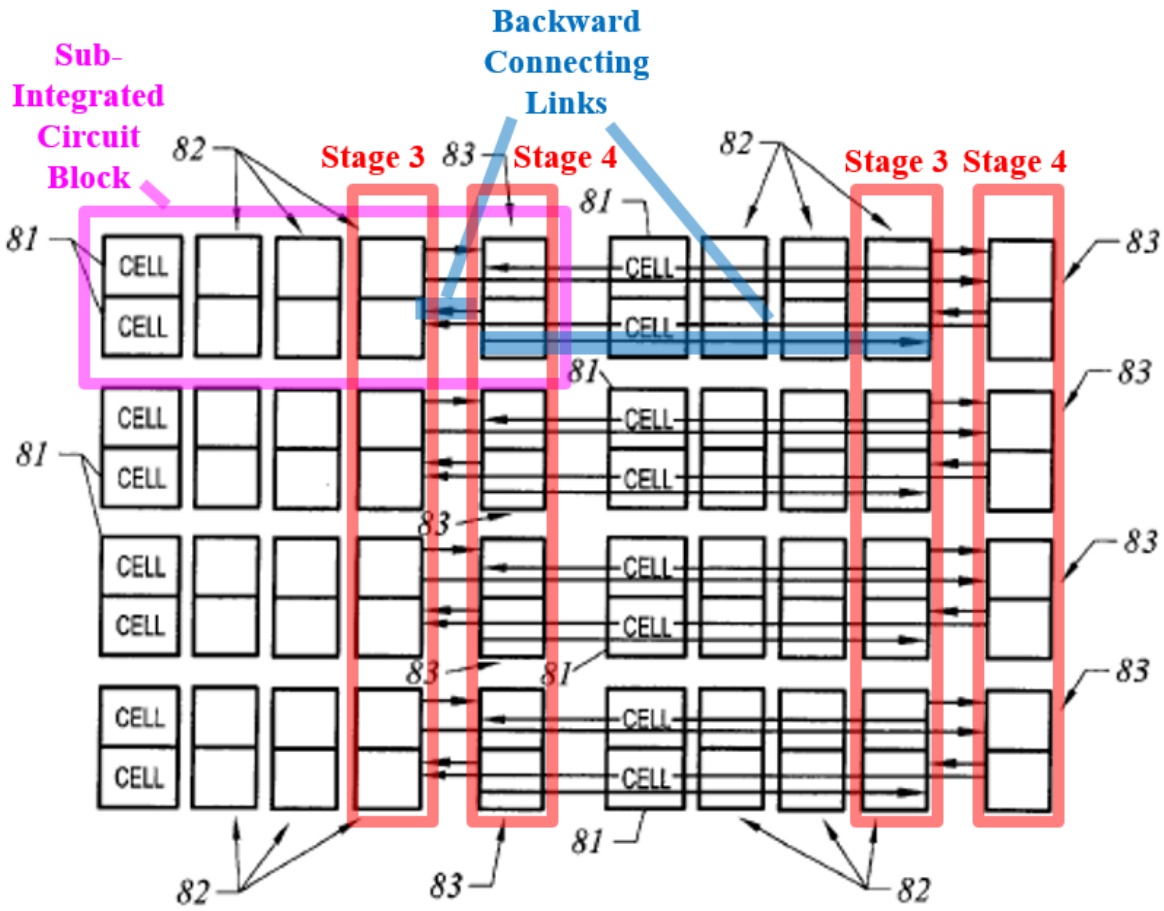



*FIG. 13B*

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶95.)

While the annotations above are only used to highlight the backward connecting links in the top-left sub-integrated circuit block, figure 13B shows that each of the sub-integrated circuit blocks includes a plurality of backward connecting links. (Ex. 1002, ¶95.)

**h)** "**Said each sub-integrated circuit block comprising a plurality [of] straight links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage and a plurality [of] cross links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage,**"

*Wong* discloses this feature. (Ex. 1002, ¶96.) According to the '523 patent, "[t]he middle links which connect switches in the same row in two successive middle stages are called hereinafter straight middle links; and the middle links which connect switches in different rows in two successive middle stages are called hereinafter cross middle links." (Ex. 1001, 9:45-49.) *Wong* discloses straight and cross links consistent with this definition and the language of claim 1, as explained below. (Ex. 1002, ¶96.)

**(1) "a plurality [of] straight links in said forward connecting links"**

As shown in annotated figure 13A below, *Wong* discloses that each sub-integrated circuit block includes "a plurality straight links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding

higher stage." (Ex. 1002, ¶97.) Annotated figure 13A below shows a plurality of straight links in the forward connecting links for the top sub-integrated circuit block, where the plurality of straight links includes a straight link from stage 1 to stage 2 and another straight link from stage 2 to stage 3. (*Id.*)

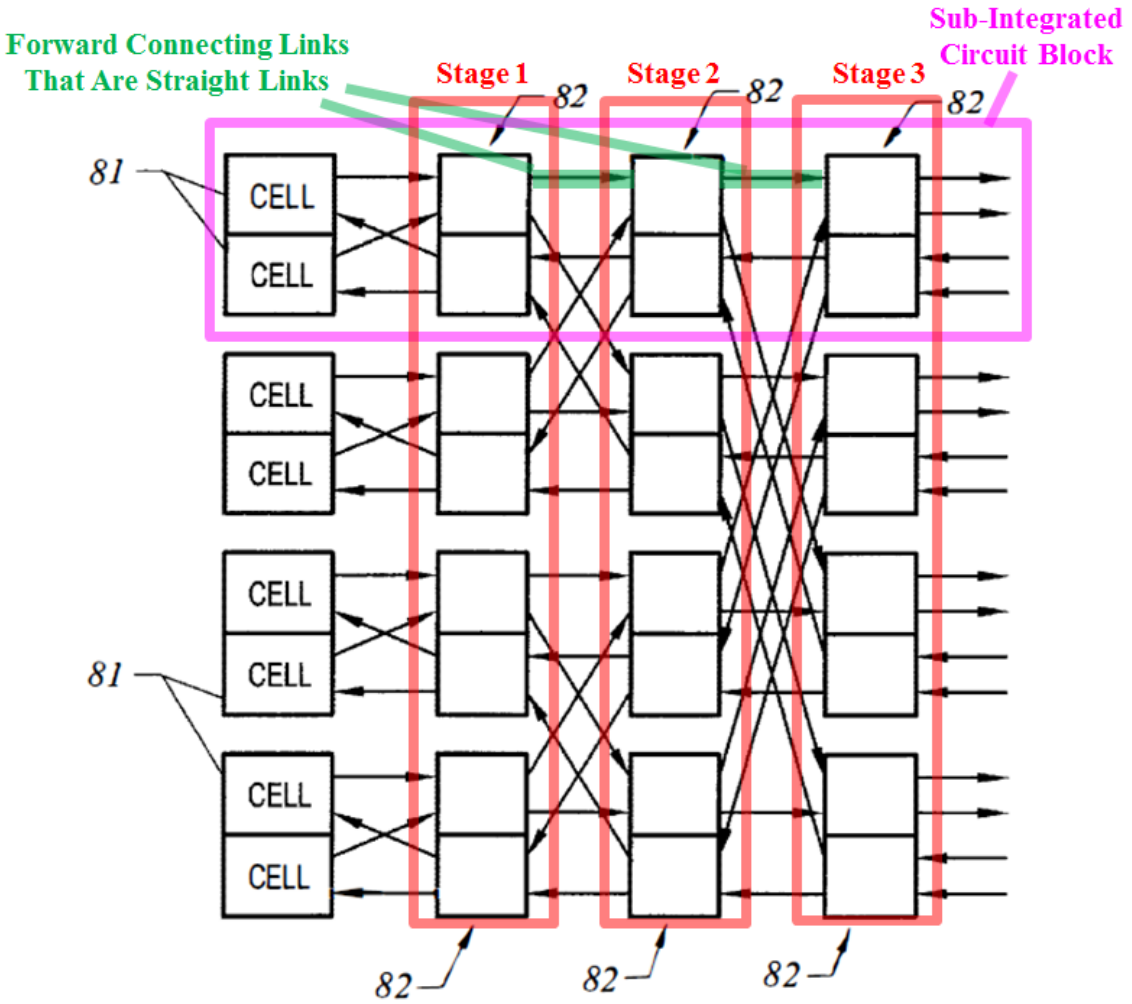



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶97.)

While the annotations above are only used to highlight the straight links in the top sub-integrated circuit block, figure 13A shows that each of the sub-integrated circuit blocks includes a plurality of forward connecting links that are straight links. (Ex. 1002, ¶98.)

Figure 13B also discloses this feature. (*Id.*, ¶99.) In addition to the straight links included in figure 13A discussed immediately above, which are also present in the figure 13B embodiment, figure 13B adds an additional forward connecting link that is a straight link for each sub-integrated circuit block. (*Id.*) In the annotated figure 13B below, the additional straight link highlighted in green is from stage 3 to stage 4 for the top-left sub-integrated circuit block. (*Id.*)

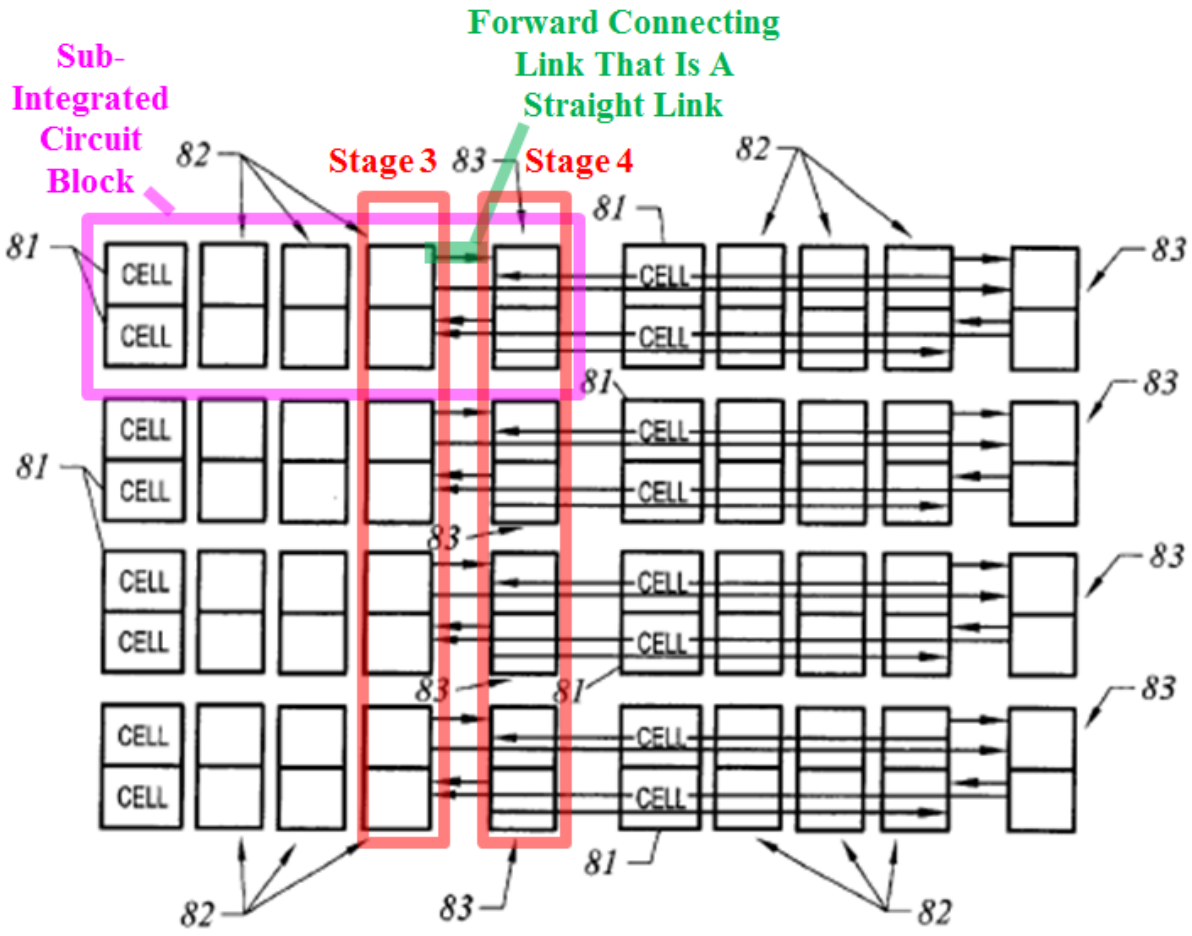



FIG. 13B

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶99.)

While the annotations above are only used to highlight the forward connecting links that are straight links in the top-left sub-integrated circuit block, figure 13B shows that each of the sub-integrated circuit blocks includes a plurality of forward connecting links that are straight links. (Ex. 1002, ¶100.)

**(2) "[Said each sub-integrated circuit block comprising . . .] a plurality [of] cross links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage, and"**

In addition to forward connecting links that are straight links, *Wong* also discloses forward connecting links that are cross links. (Ex. 1002, ¶¶101-103.) As shown in annotated figure 13A below, *Wong* discloses that each sub-integrated circuit block includes "a plurality [of] cross links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage," as claimed. (*Id.*, ¶101.) The plurality of cross links for the top sub-integrated circuit block in figure 13A are highlighted below, where the plurality of cross links includes cross links from stage 1 to stage 2 and from stage 2 to stage 3. (*Id.*) As shown in the annotated figure 13A below, the cross links are links which connect switches in different rows (corresponding to different sub-integrated circuit blocks). (*Id.*)

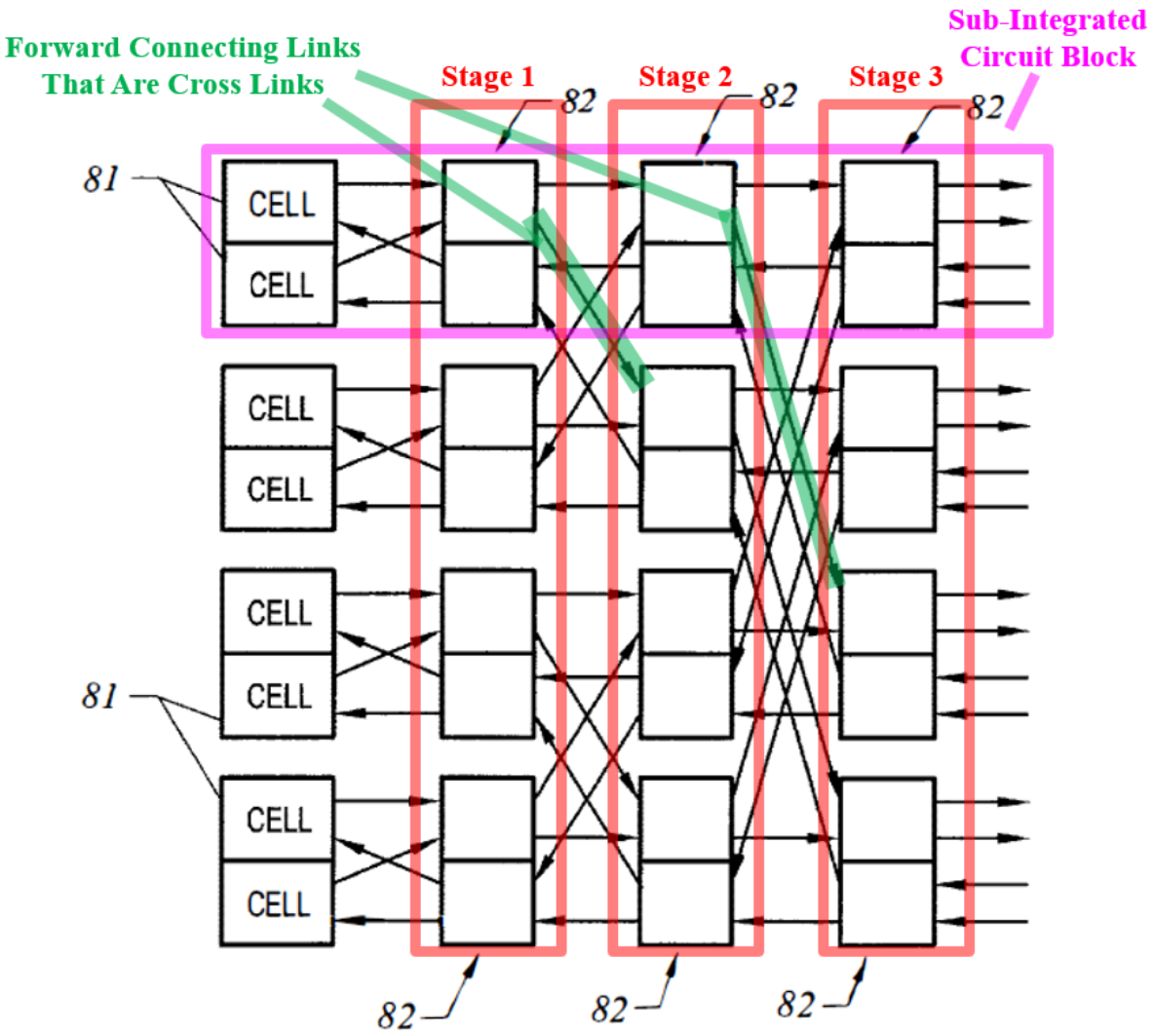



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶101.)

While the annotations above are only used to highlight the forward connecting links that are cross links for the top sub-integrated circuit block, figure 13A shows that each of the sub-integrated circuit blocks includes a plurality of forward connecting links that are cross links. (Ex. 1002, ¶102.)

The embodiment in figure 13B of *Wong* also discloses this feature. (*Id.*, ¶103.) For example, the cross links included in figure 13A annotated above are also present in the figure 13B embodiment between the top-left sub-integrated circuit block and other sub-integrated circuit blocks in the same column. (*Id.*) Furthermore, figure 13B adds an additional forward-connecting cross link for each sub-integrated circuit block. (*Id.*) As shown in the annotated figure 13B below, there is an additional forward connecting link that is a cross links for the top-left sub-integrated circuit block that is from stage 3 to stage 4 between the top-left sub-integrated circuit block and the sub-integrated circuit block directly to the right in the second column. (*Id.*)

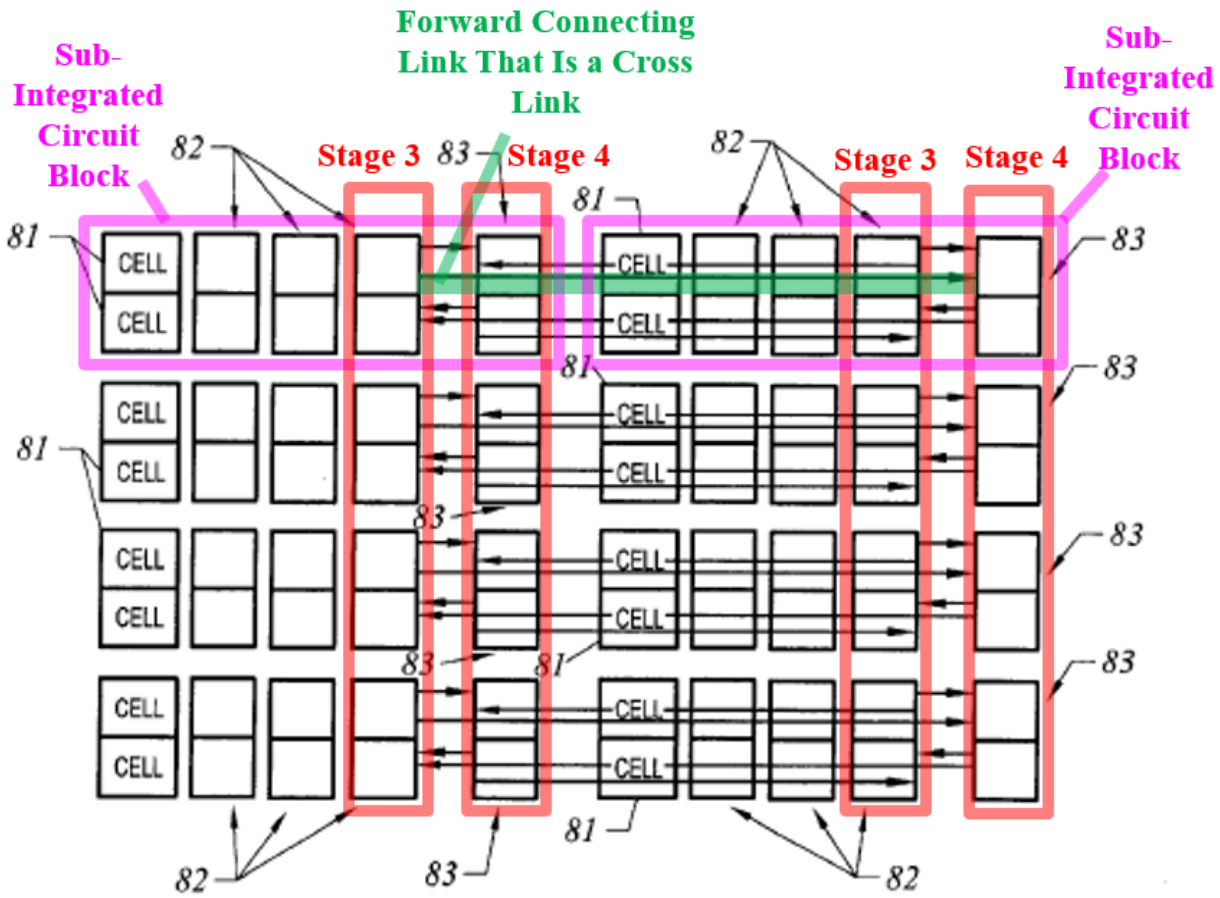



*FIG. 13B*

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶103.)

**(3) "[Said each sub-integrated circuit block . . .] further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage and"**

In addition to the forward connecting links including straight and cross links, the backward connecting links in *Wong* also include straight and cross links as recited in claim 1. (Ex. 1002, ¶¶104-106.) For example, as shown in annotated

figure 13A below, *Wong* discloses "a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage." (*Id.*, ¶104.) Annotated figure 13A below shows a plurality of straight links in the backward connecting links for the top sub-integrated circuit block, where the plurality of straight links includes a straight link from stage 2 to stage 1 and another straight link from stage 3 to stage 2. (*Id.*)

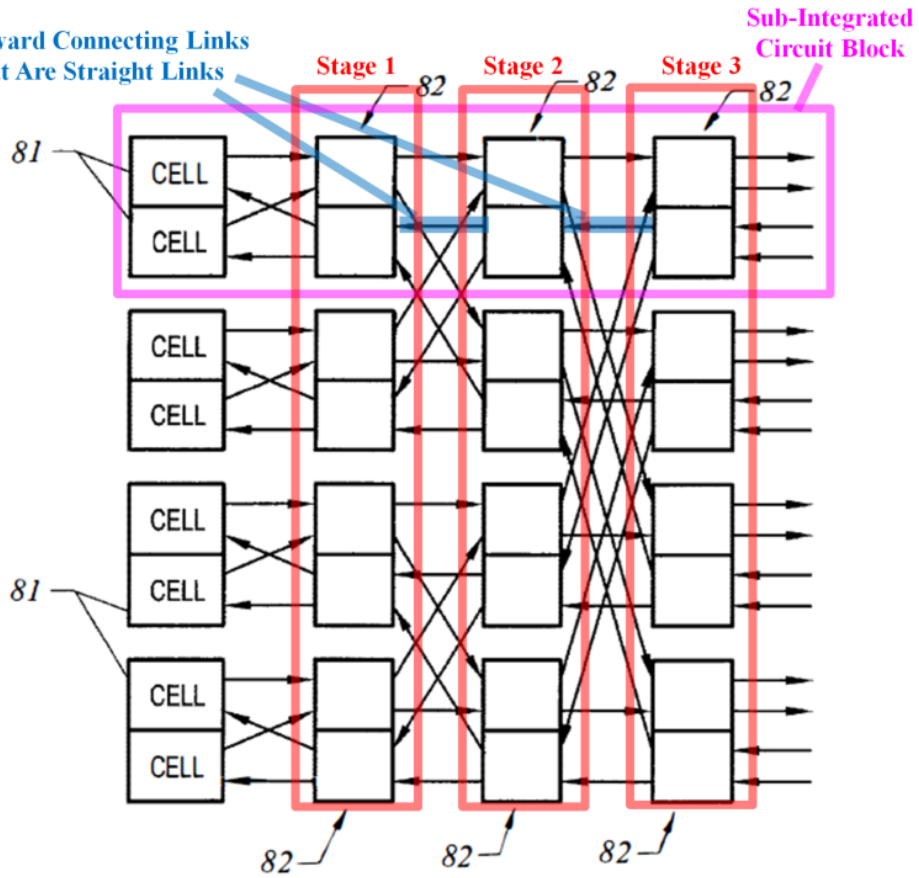



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶104.)

While the annotations above are only used to highlight the straight links in the top sub-integrated circuit block, figure 13A shows that each of the sub-integrated circuit blocks includes a plurality of backward connecting links that are straight links. (Ex. 1002, ¶105.)

Figure 13B also discloses the claimed feature. (*Id.*, ¶106.) In addition to the backward connecting links that are straight links included in figure 13A discussed immediately above, which are also present in the figure 13B embodiment, figure 13B adds an additional backward connecting link that is a straight link for each sub-integrated circuit block. (*Id.*) As shown in annotated figure 13B below, the depicted embodiment includes an additional backward connecting link that is a straight link for each sub-integrated circuit block. In the annotated figure 13B below, the additional straight link highlighted in blue is from stage 4 to stage 3 for the top-left sub-integrated circuit block. (*Id.*)

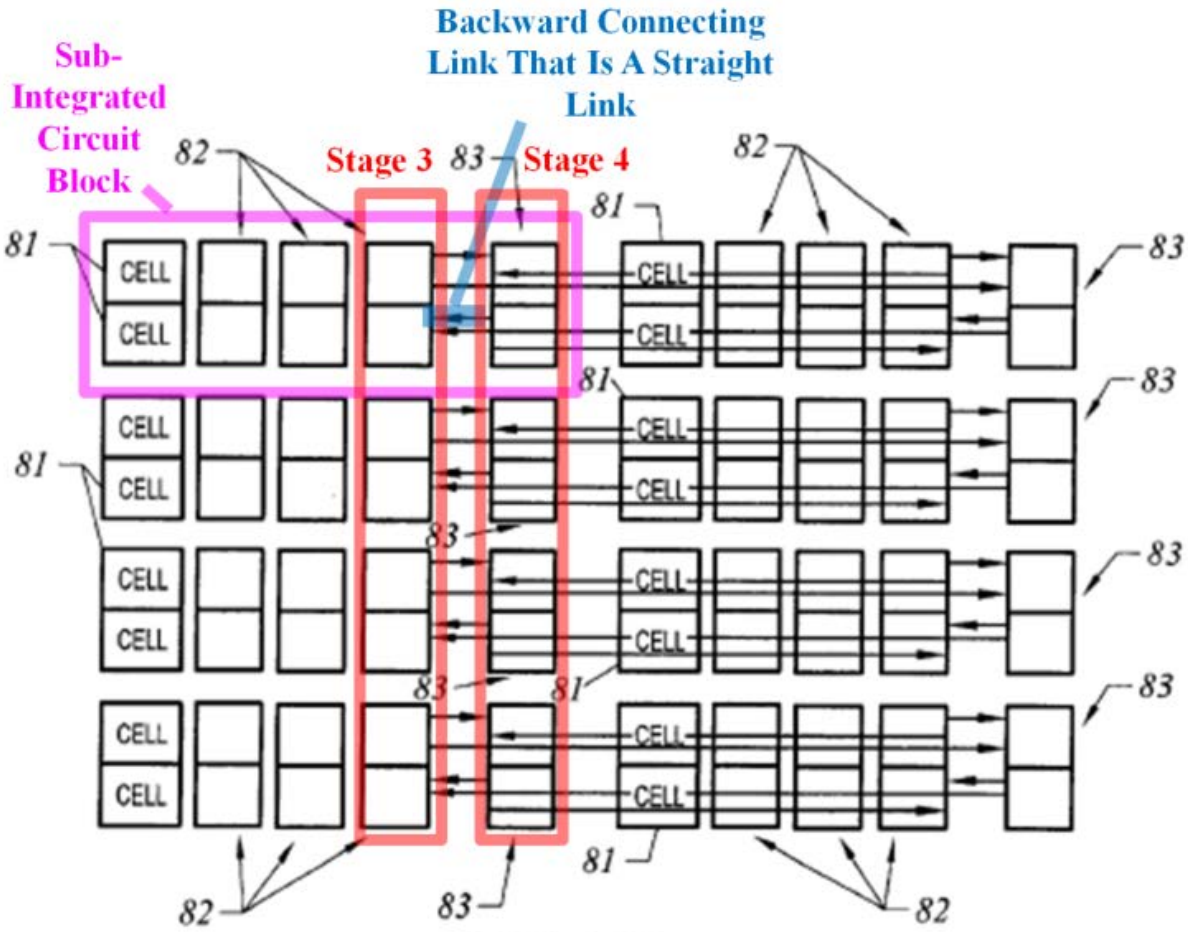



FIG. 13B

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶106.)

**(4) "[Said each sub-integrated circuit block comprising . . .] a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage"**

In addition to backward connecting links that are straight links, *Wong* also discloses backward connecting links that are cross links. (Ex. 1002, ¶¶107-109.) As shown in annotated figure 13A below, *Wong* discloses that each sub-integrated

circuit block includes "a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage." (*Id.*, ¶107.) The plurality of backward-connecting cross links for the top sub-integrated circuit block in figure 13A are highlighted below, where the plurality of cross links includes cross links from stage 2 to stage 1 and cross links from stage 3 to stage 2. (*Id.*) As shown below, the cross links are links that connect switches in different rows (corresponding to different sub-integrated circuit blocks). (*Id.*)

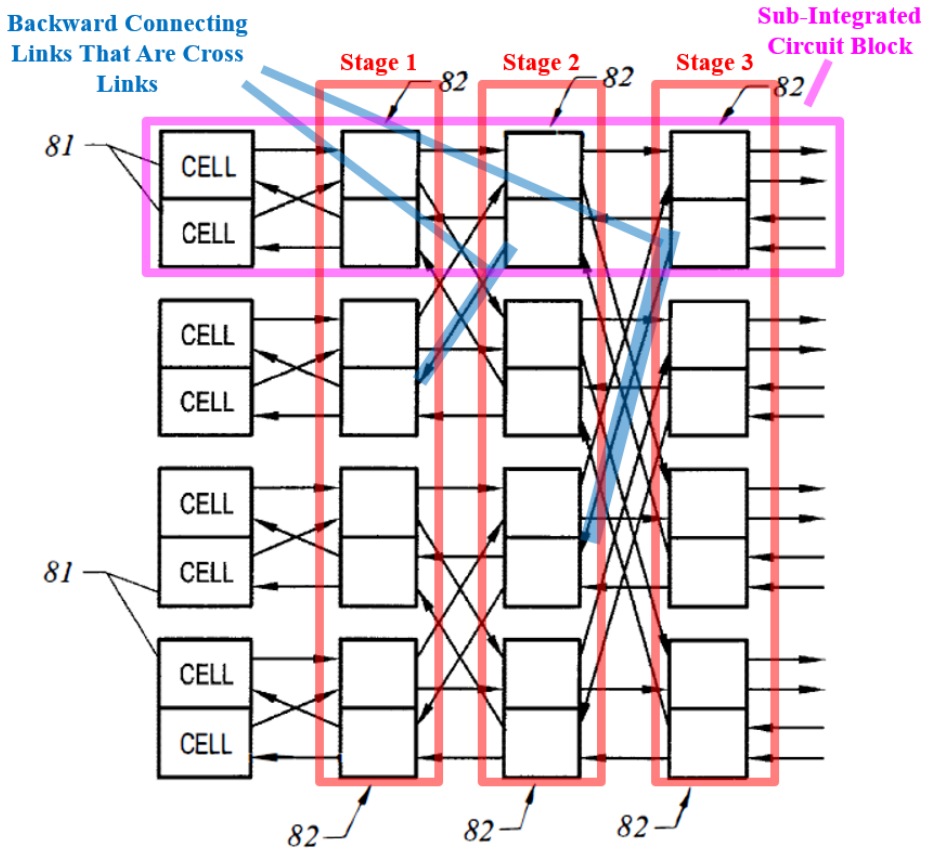



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶107.)

While the annotations above are only used to highlight the backward connecting links that are cross links for the top sub-integrated circuit block, figure 13A shows that each of the sub-integrated circuit blocks includes a plurality of backward connecting links that are cross links. (Ex. 1002, ¶108.)

The embodiment depicted in figure 13B of *Wong* also discloses this claim feature. (*Id.*, ¶109.) For example, the backward connecting links that are cross links shown above in figure 13A annotated above are also present in the figure 13B embodiment between the top-left sub-integrated circuit block and sub-integrated circuit blocks in the same column. (*Id.*) Furthermore, the embodiment shown in figure 13B adds an additional backward-connecting cross link for each sub-integrated circuit block. (*Id.*) Annotated figure 13B below shows an additional backward connecting link that is a cross links for the top-left sub-integrated circuit block. (*Id.*) The additional cross link is from stage 4 to stage 3 between the top-left sub-integrated circuit block and the sub-integrated circuit block directly to the right in the second column. (*Id.*)

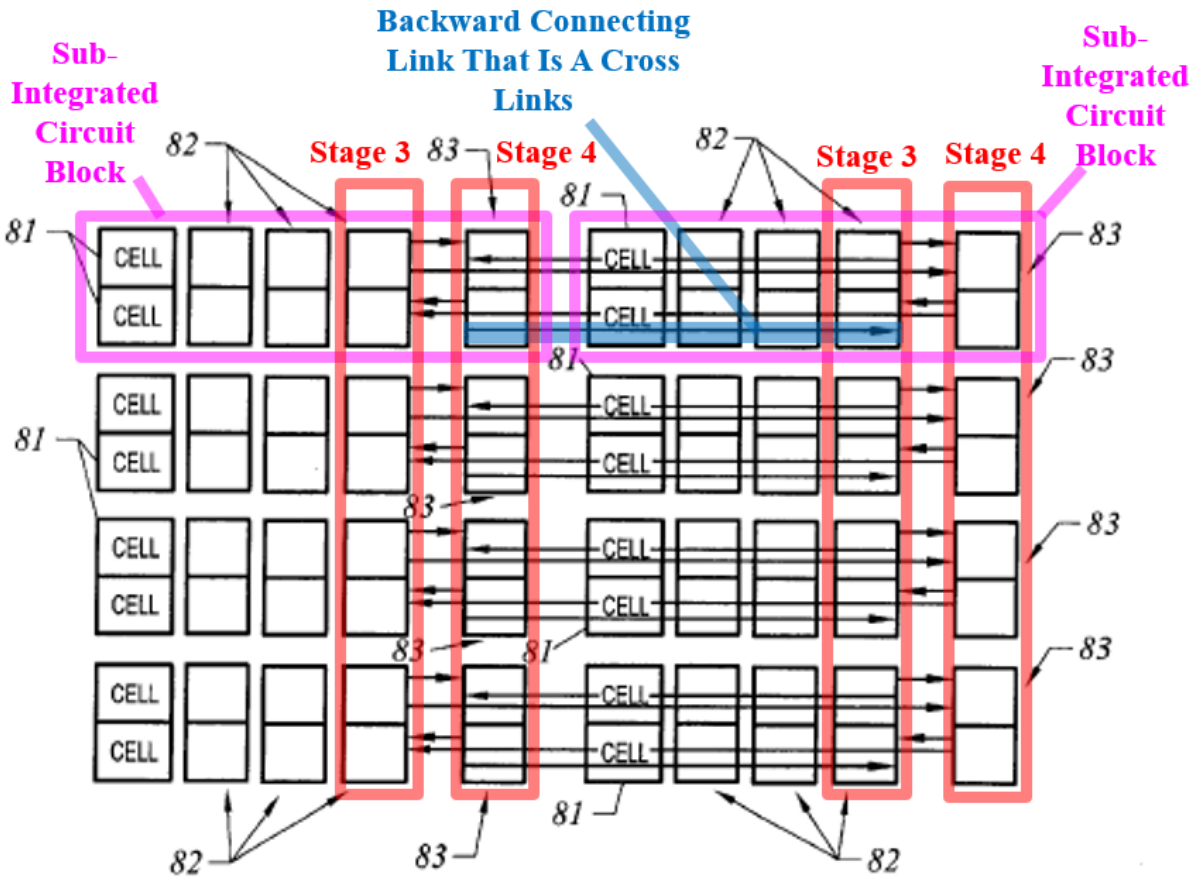



*FIG. 13B*

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶109.)

**i) "said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns; and"**

*Wong* discloses this limitation. (Ex. 1002, ¶¶110-117.) For example, figures 13A and 13B of *Wong* disclose the "plurality of sub-integrated circuit blocks" identified above with respect to claim element 1(b) arranged in rows and columns. (*Id.*, ¶110.) Figure 13A of *Wong* shows the sub-integrated circuit blocks arranged

in four rows in a single column ("plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns"). (*Id.*)

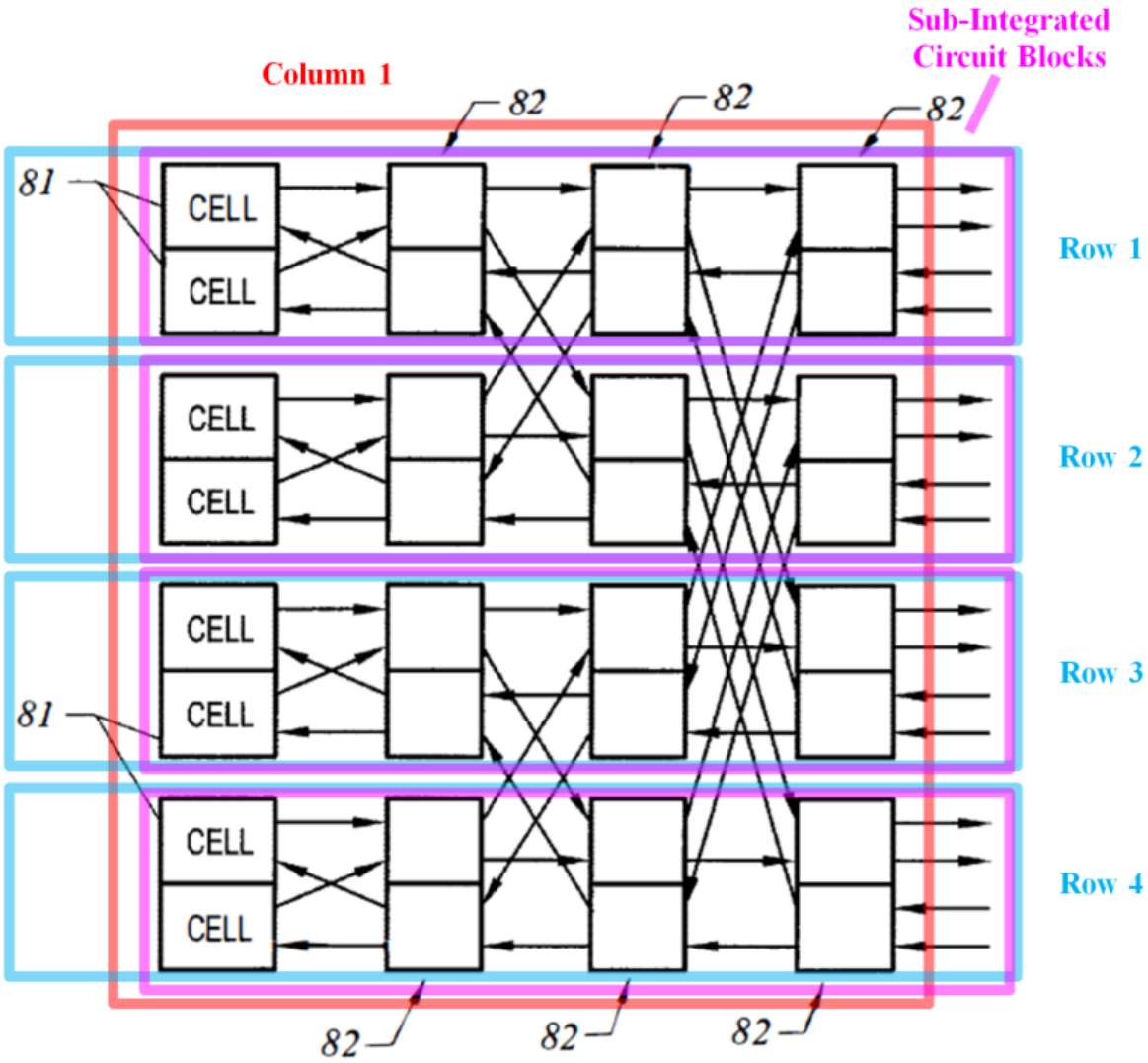



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶110.)

To the extent PO may contend that claim 1 requires a two-dimensional grid of rows and columns that includes both multiple rows and multiple columns of sub-

integrated circuit blocks, such an interpretation would be improper, as it conflicts with other claims in a related patent. Specifically, U.S. Patent No. 10,050,904 ("the '904 patent") (Ex. 1046), which incorporates the '523 patent by reference (Ex. 1046, 2:20-24) and lists the same inventor as the '523 patent, recites a plurality of subnetworks "arranged in a two-dimensional grid of rows and columns" in independent claim 1. (*Id.*, 69:25-27). Claim 10 of the '904 patent, which depends from claim 1, states that "said plurality of subnetworks are implemented in a single dimension." (*Id.*, 71:11-12.) In the '904 patent, the term "subnetwork" maps to a row of switches in the same manner as the "sub-integrated circuit block" does in the '523 patent. (Ex. 1002, ¶111.) Claim 10 of the '904 patent demonstrates that claim 1 of the '904 patent is broad enough to encompass a two-dimensional grid where the subnetworks are only laid out in a single dimension (e.g., one row or one column). (*Id.*) Therefore, claims 1 and 10 of the '904 patent support the understanding that figure 13A of *Wong*, which has multiple rows in a single column, discloses "said

plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns" as recited in claim 1 of the '523 patent.[6] (*Id.*)

Moreover, the embodiment shown in figure 13B of *Wong* also discloses the claim feature, and the embodiment of figure 13B includes multiple rows and multiple columns. (*Id.*, ¶112.) As shown in annotated figure 13B below, the sub-integrated circuit blocks are arranged in four rows and two columns. (Ex. 1008, 3:7-10, 13:33-38; Ex. 1002, ¶112.)

[6] In the "Background of the Invention" section, the '523 patent concedes that "[t]he most commonly used VLSI layout in an integrated circuit is based on a two-dimensional grid model comprising only horizontal and vertical tracks." (Ex. 1001, 2:40-42.)

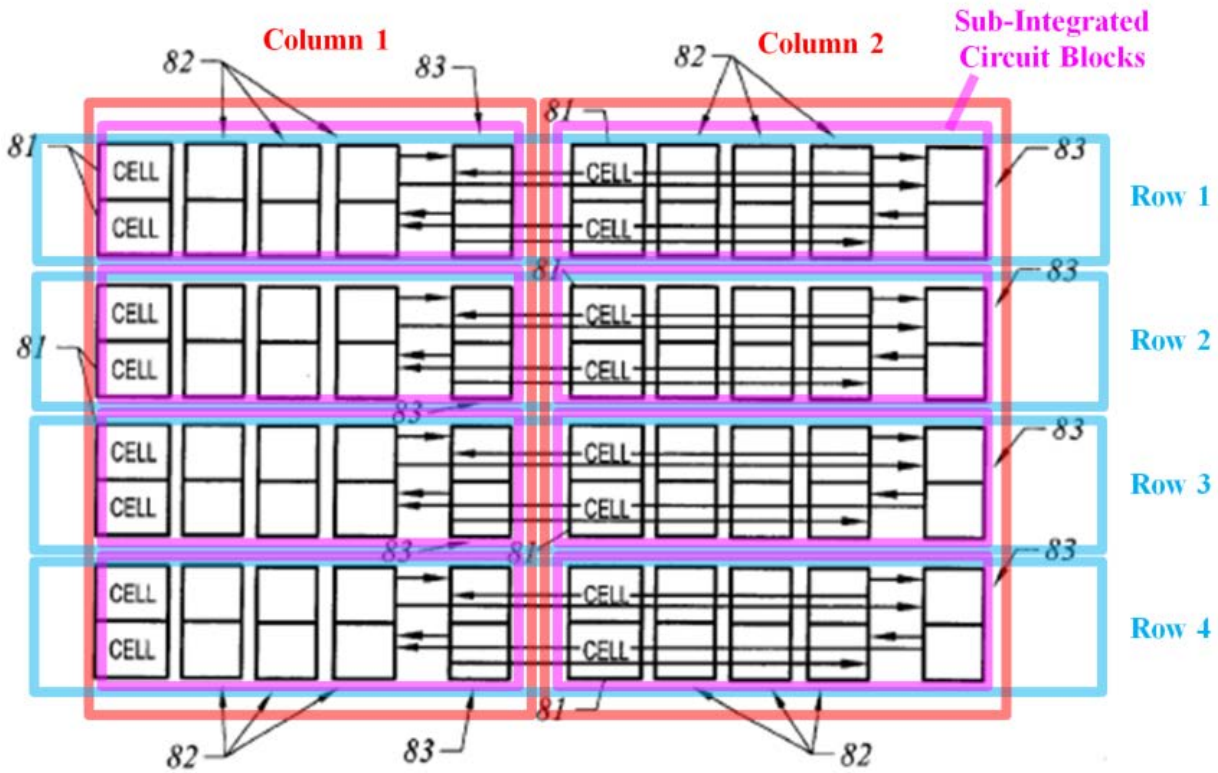



*FIG. 13B*

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶112.)

Notably, *Wong* also discloses that further expansion of the network is contemplated to provide additional columns in the network. (Ex. 1008, 13:38-40 ("For each additional doubling of the number of cell columns, an additional column of switch cells must be added to each of the cell columns …."); Ex. 1002, ¶¶113-114.) *Wong* further states that "[t]he strength of this column floorplan is that **the number of cells in a column can be any power of 2, and the number of rows can also independently be any power of 2**." (Ex. 1008, 13:44-46 (emphasis added); Ex. 1002, ¶114.)

To the extent PO may argue that the two-dimensional grid of rows and columns recited in claim 1 corresponds to a physical layout of the sub-integrated circuit blocks on an integrated circuit, *Wong* discloses that figures 13A and 13B correspond to such a physical layout, and therefore *Wong* discloses limitation 1(i) even under such a narrow interpretation. (Ex. 1008, 13:13-16, 13:19-22; Ex. 1002, ¶115.)

A POSITA would also have recognized that figure 14A of *Wong* also supports the understanding that figures 13A and 13B of *Wong* correspond to physical layouts. (Ex. 1002, ¶116.) Figure 14A "shows a 16 logic cell column floorplan (the same as shown in figure 13B) with the cells labeled for identification" (Ex. 1008, 13:60-62) that arranges the sub-networks in a two-dimensional grid of rows and columns. (Ex. 1002, ¶116.)

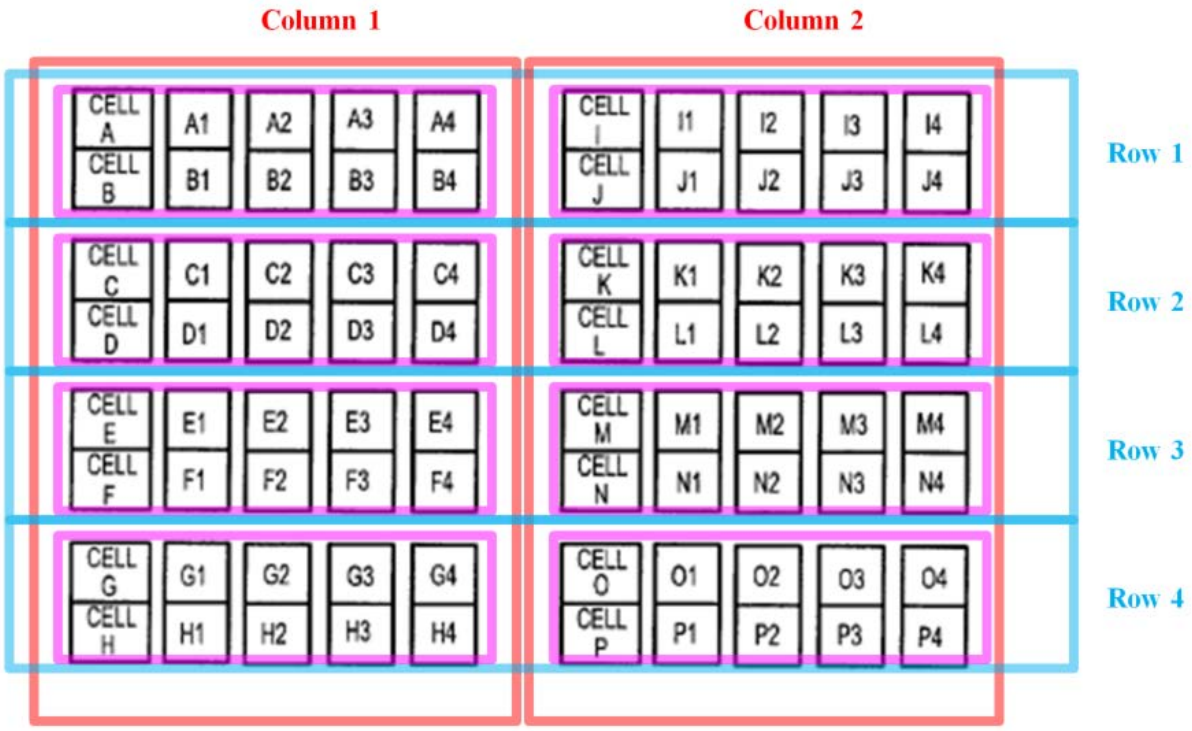



*FIG. 14A*

(Ex. 1008, FIG. 14A (annotated); Ex. 1002, ¶116.)

Notably, during prosecution of the application that led to the '523 patent, PO argued that *Wong* uses a "[c]olumn-based layout," which was alleged to be different from the "2D-grid in row-column layout" of the '523 patent. (Ex. 1004, 62.) As shown above in figure 14A of *Wong*, the column-based layout is a 2D grid of rows and columns. (Ex. 1002, ¶117.) Related to the "2D-grid in row-column layout," PO further asserted during prosecution that a "[k]ey insight in the disclosure is to arrange the sub-integrated circuits in a hypercube topology)." (Ex. 1004, 62.) However, no such "hypercube topology" is recited in claim 1. (Ex. 1002, ¶117.)

**j)** "**said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right,**"

*Wong* discloses this feature. (Ex. 1002, ¶¶118-129.) As discussed above with respect to claim limitations 1(h)(1) and 1(h)(3), all of the straight links in the network connect switches within the same sub-integrated circuit block ("said all straight links are connecting from switches in each said sub-integrated circuit block to switches in the same integrated circuit block"). (*Supra* Sections IX.A.1(h)(1), IX.A.1(h)(3).) Annotated figure 13A below shows the straight links for the top sub-integrated circuit block, where all of the straight links connect switches in the same sub-integrated circuit block (the same row). (Ex. 1002, ¶118.)

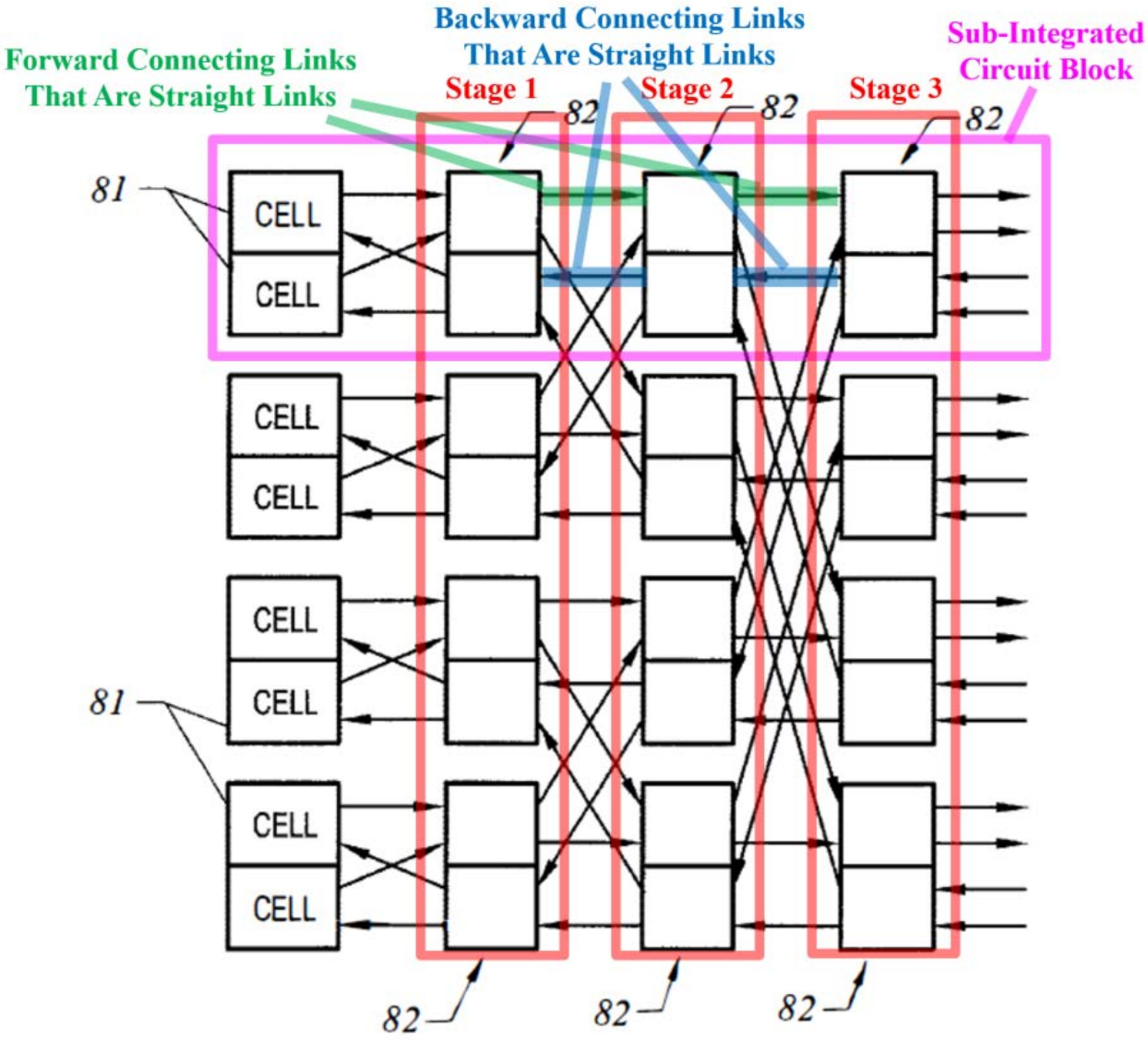



FIG. 13A

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶118.)

Similarly, the embodiment shown in figure 13B of *Wong* also discloses this feature. (*Supra* Sections IX.A.1(h)(1), IX.A.1(h)(3); Ex. 1002, ¶119.) Annotated figure 13B below (which also includes the straight links highlighted above with

respect to the embodiment of figure 13A) shows the additional straight links for the top-left sub-integrated circuit block. (Ex. 1002, ¶119.)

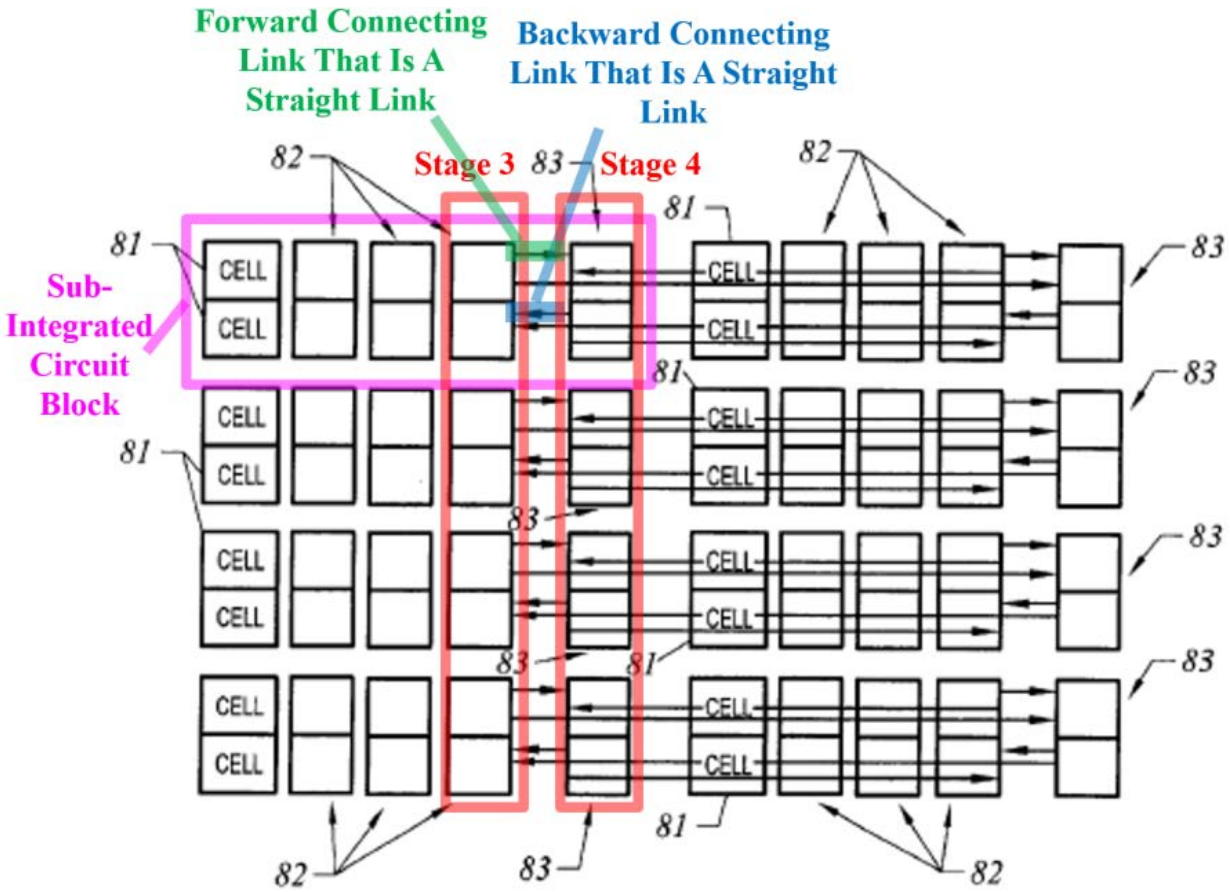



FIG. 13B

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶119.)

*Wong* further discloses "said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right." (Ex. 1002, ¶120.) As discussed above with respect to claim

feature 1(i), in both the figure 13A and 13B embodiments, the plurality of sub-integrated circuit blocks are arranged in a two-dimensional array of rows and columns. (*Supra* Section IX.A.1(i).) With respect to the embodiment shown in figure 13A, all of the cross links are implemented as vertical links between switches in different sub-integrated circuit blocks that are placed vertically above or below each other. (Ex. 1002, ¶120.)

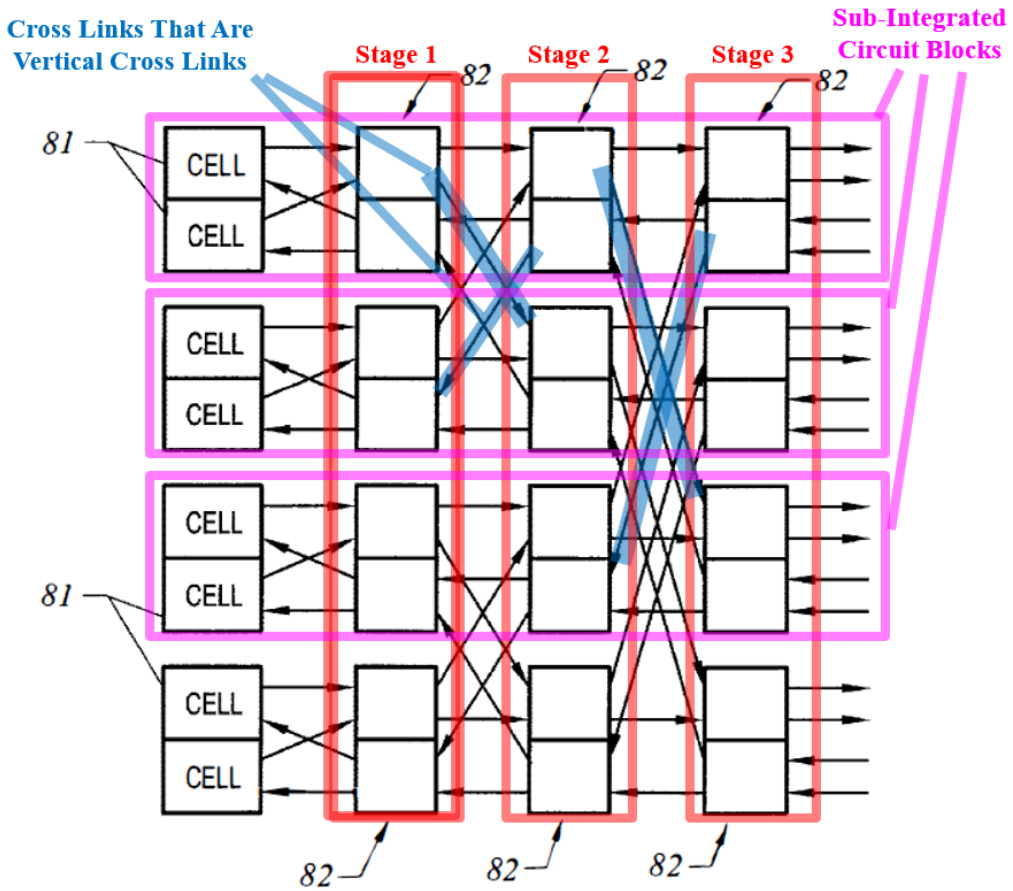



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶120.)

*Wong's* disclosure of cross links between different sub-integrated circuit blocks in figure 13A being implemented as "vertical links . . . between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below" is consistent with the disclosure of the '523 patent.[7] For example, as shown in the annotated excerpts of figures 13A and 14A of *Wong* below, the cross links between stages 1 and 2 constitute vertical links between switches in two different sub-integrated circuit blocks placed vertically above or below each other in the same manner as the cross links shown in annotated excerpts of figures 1B and 1D of the '523 patent. (Ex. 1002, ¶121.)

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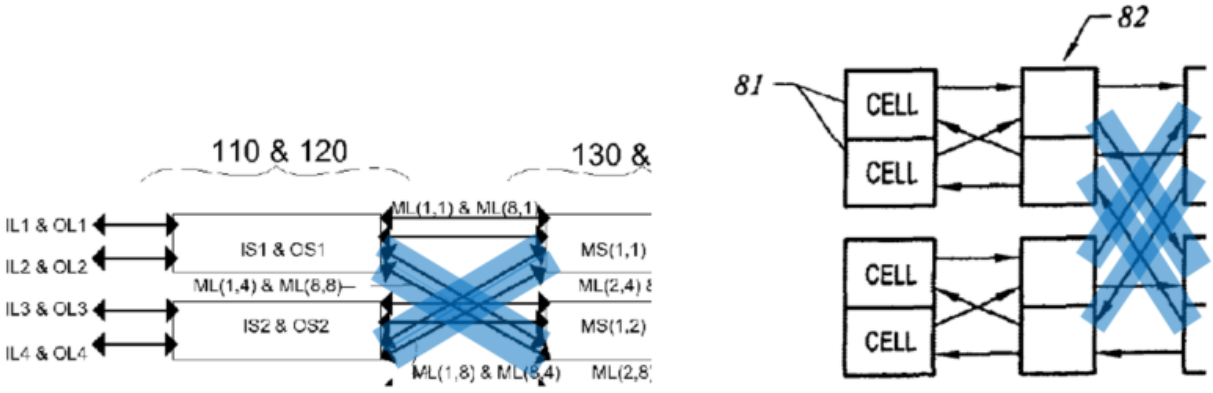
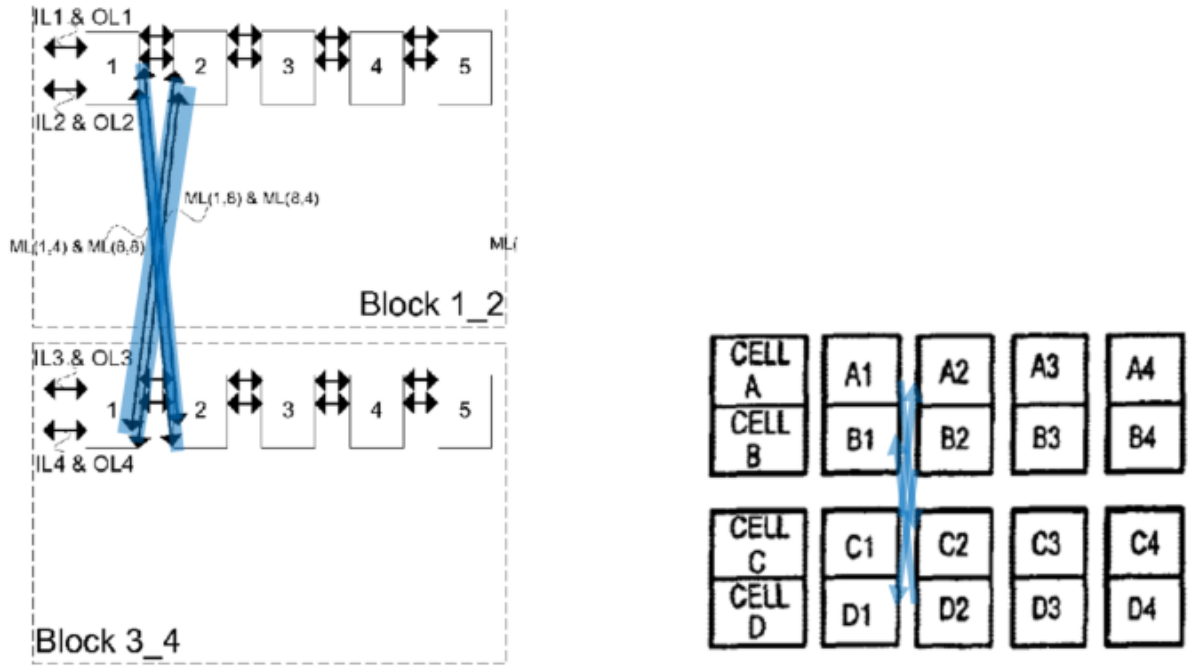
[7] The '523 patent acknowledges that "[t]he most commonly used VLSI layout in an integrated circuit is based on a two-dimensional grid model comprising only horizontal and vertical tracks." (Ex. 1001, 2:40-42.) The '523 patent also states that "[w]hen large scale sub-integrated circuit blocks with inlet and outlet links are layed out in an integrated circuit device in a two-dimensional grid arrangement, (for example in an FPGA where the sub-integrated circuit blocks are Lookup Tables) the most intuitive routing network is a network that uses horizontal and vertical links only . . . ." (*Id.*, 3:12-17.)




(Ex. 1001, FIG. 1B (excerpt, annotated); Ex. 1008, FIG. 13A excerpt, annotated); Ex. 1002, ¶121.)




(Ex. 1001, FIG. 1D (excerpt, annotated); Ex. 1008, FIG. 14A excerpt, annotated); Ex. 1002, ¶121.)

As shown in the annotated excerpts above, *Wong's* figure 13A network and two-dimensional row-column layout shown in figure 14A includes vertical cross links between stages 1 and 2 of two sub-integrated circuit blocks that are placed above and below one another in the same manner as that shown in the annotated excerpts of figures 1B and 1D of the '523 patent. (Ex. 1002, ¶122.) According to the '523 patent, figure 1D shows the inter-block links ("cross links") as vertical links between switches that are placed vertically above or below each other. (Ex. 1001, 15:9-12; Ex. 1002, ¶122.)

In the embodiment shown in figure 13B of *Wong*, the cross links between stages 1 and 2 and between stages 2 and 3 are implemented as vertical links between switches in two different sub-integrated circuit blocks placed vertically above or below each other in the same manner as shown in figure 13A. (Ex. 1002, ¶123.) That is because figure 13B includes two instantiations of the network of switches shown in figure 13A. (Ex. 1008, 13:36-38; Ex. 1002, ¶123.) In addition to those vertical cross links, the cross links between stages 3 and 4 in the network of figure 13B are implemented as "horizontal links between switches in two different said sub-integrated circuit blocks which are . . . placed horizontally to the left or to the right" of each other. Indeed, PO conceded that figure 13B of *Wong* shows horizontal links during prosecution of the application leading to the '523 patent. (Ex. 1008,

FIGs. 13A, 13B; Ex. 1004, 63 ("As disclosed in Fig. 13B, columns are doubled by adding one more stage of switches in both the columns (for example Fig. 13A is replicated to get Fig. 13B and a new stage of switches 83 are added and **the cross links between the new stage of switches in the two columns become horizontal links**).") (emphasis added); Ex. 1002, ¶123.)

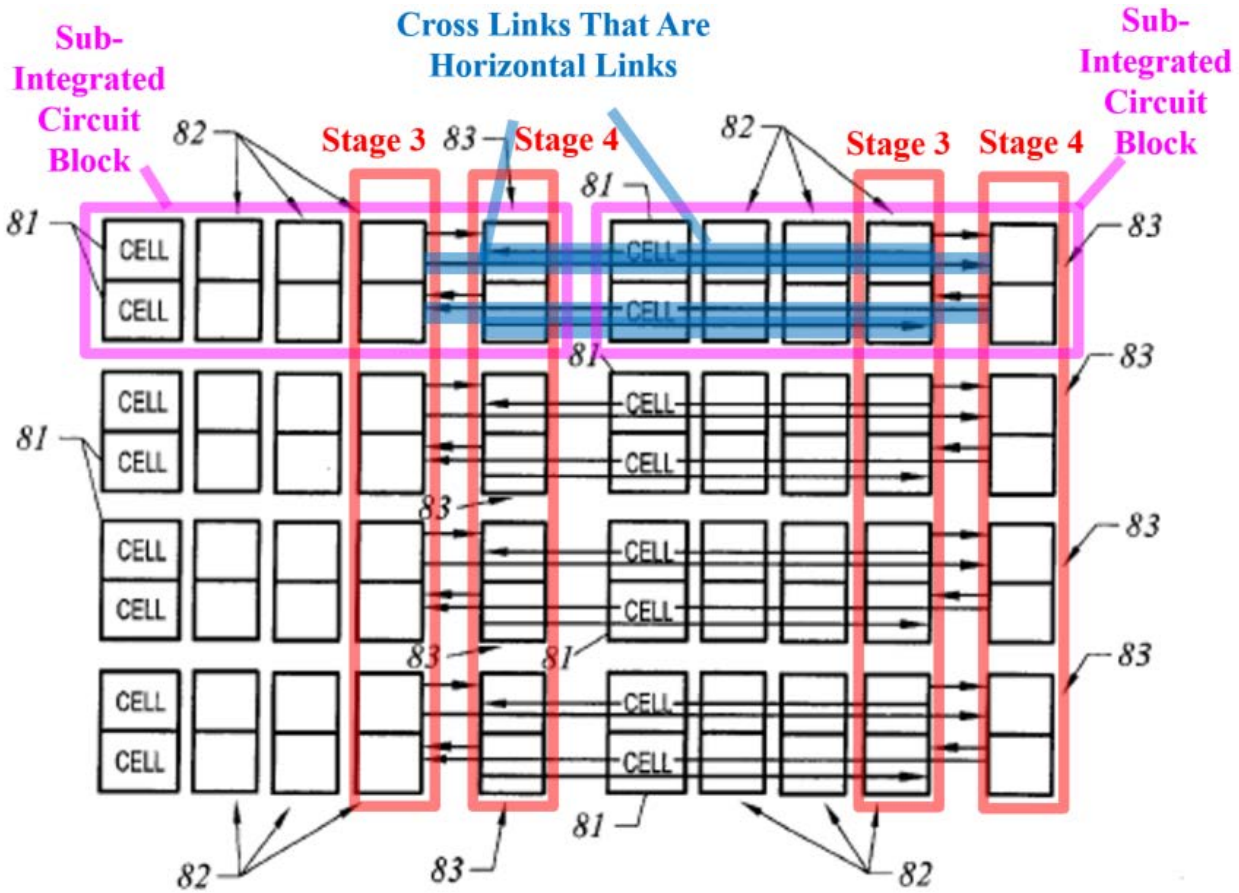
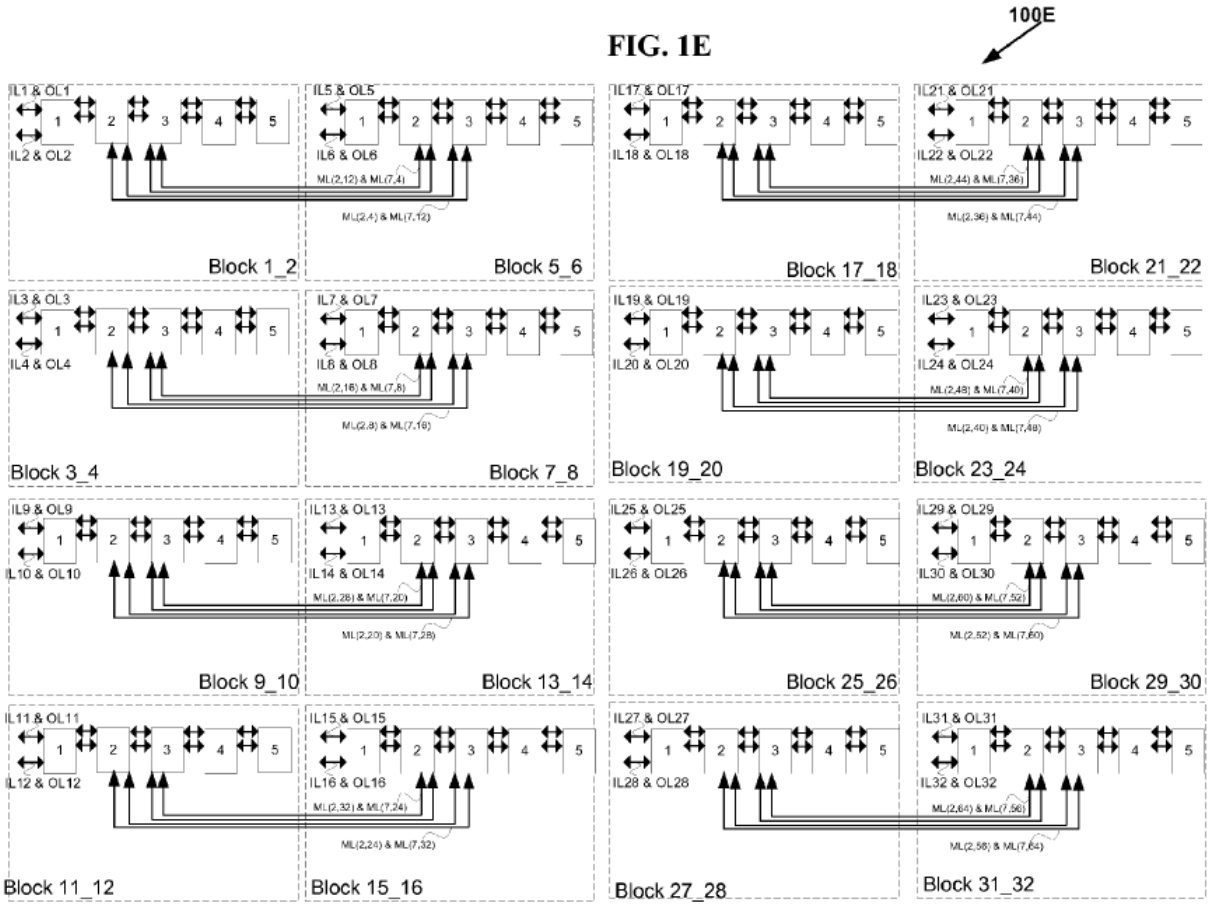



FIG. 13B

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶123.)

Such an understanding is also consistent with the '523 patent's description of the cross links in figures 1E and 1G being "horizontal tracks." (Ex. 1001, 15:9-19, FIGs. 1E and 1G; Ex. 1002, ¶124.)




(Ex. 1001, FIG. 1E; Ex. 1002, ¶124.)

Therefore, the embodiment shown in figure 13B of *Wong* also discloses this claim feature. (Ex. 1002, ¶125.) Specifically, in figure 13B the cross links between stages 1 and 2 and between stages 2 and 3 are vertical links between switches in two

different sub-integrated circuit blocks that are placed vertically above or below each other, whereas the cross links between stages 3 and 4 are horizontal links between switches in two different sub-integrated circuit blocks that are placed horizontally to the left or to the right of each other. (*Id.*)

During prosecution of the '275 application, which eventually issued as the '523 patent, PO argued that *Wong* did not disclose this feature. Specifically, the applicant argued that the entirety of figure 13A of *Wong* constitutes a "sub-integrated circuit block" and is the "basic building block of the column-based layout." (Ex. 1004, 62-63.) Based on that contention, PO further argued that the sub-integrated circuit block that includes all of the switches in figure 13A "has cross links connected between switches of two succeeding stages with in the same sub-integrated circuit." (*Id.*) PO's characterization of *Wong* during prosecution is incorrect. (Ex. 1002, ¶126.) As demonstrated above with respect to claim limitation 1(b), each row of switches in the network shown in figure 13A of *Wong* constitutes a "sub-integrated circuit block" in a manner consistent with how that term is used in the context of the '523 patent. (*Supra* Section IX.A.1(b); Ex. 1002, ¶126.) Because **each row of switches is a sub-integrated circuit block, and not the entire network structure shown in figure 13A** as PO argued during prosecution, each of

the cross links between switches in figure 13A of *Wong* is between two different sub-integrated circuit blocks. (Ex. 1002, ¶126.)

PO's position that the entirety of figure 13A is a "sub-integrated circuit block" appears to be based on excerpted language from *Wong* taken out of context. (*Id.*, ¶127.) Specifically, during prosecution PO cited to *Wong's* disclosure of "[t]here are two logic cells 81 per switch cell 82, connected in the so called 'butterfly' pattern, consistent with the Benes network topology: . . . ." (Ex. 1004, 62 (citing Ex. 1008, 13:22-24).) Based on this excerpt, PO then alleged that the sub-integrated circuit block in *Wong* has **cross links connected between switches in the same sub-integrated circuit block**, "[o]therwise there will not be a butterfly pattern." (Ex. 1004, 62-63.) But a POSITA would have understood that PO's conclusion that there must be cross links in the same sub-integrated circuit block in *Wong* does not follow from the excerpted text from *Wong*. (Ex. 1002, ¶127.) *Wong's* statement about the "butterfly pattern" is not concerned with links between switches and instead corresponds to the connections between the logic cells 81 and the switches 82 in the first stage of the network. (Ex. 1008, 13:22-26; Ex. 1002, ¶127.)

PO's arguments during prosecution are also internally inconsistent. (Ex. 1002, ¶128.) As discussed above, PO acknowledged during prosecution that figure 13A of *Wong* has cross links. (Ex. 1004, 62-63 ("cross links connected between

switches of two succeeding stages with in the same sub-integrated circuit").) But based on the definition provided in the '523 patent, cross links are between switches in different sub-integrated circuit blocks. (Ex. 1001, 9:47-49.) If the entirety of figure 13A is one sub-integrated circuit block as PO asserted in attempting to argue over *Wong*, then there would not be any cross links in figure 13A of *Wong*, which is inconsistent with PO's recognition that figure 13A of *Wong* has cross links. (Ex. 1002, ¶128.)

Based on the prosecution history, to the extent that PO's only basis for contending that claim limitation 1(j) is not disclosed by *Wong* was the assertion that the entirety of figure 13A constituted a "sub-integrated circuit block," that basis is incorrect and inapposite here. (*Id.*, ¶129.) As noted above, Petitioner disagrees with the applicant's grouping of the plurality of rows of switches in figure 13A together to form a single "sub-integrated circuit block," as such a grouping is inconsistent with how a POSITA would have understood "sub-integrated circuit block" in view of the disclosure of the '523 patent. (*Id.*)

**k)** "**each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid.**"

*Wong* discloses this limitation. (Ex. 1002, ¶¶130-140.) For example, figure 13A of *Wong*, annotated below, discloses that each of the rows in the network ("sub-integrated circuit blocks") has three stages ("same number of stages"). (Ex. 1008, FIG. 13A; Ex. 1002, ¶130).) Moreover, each of the sub-integrated circuit blocks has the same construction as the other sub-integrated circuit blocks, and therefore has the "same number of . . . said switches in each said stage." (Ex. 1008, FIGs. 4B, 4C, 13A-B, 14A; Ex. 1002, ¶130.)

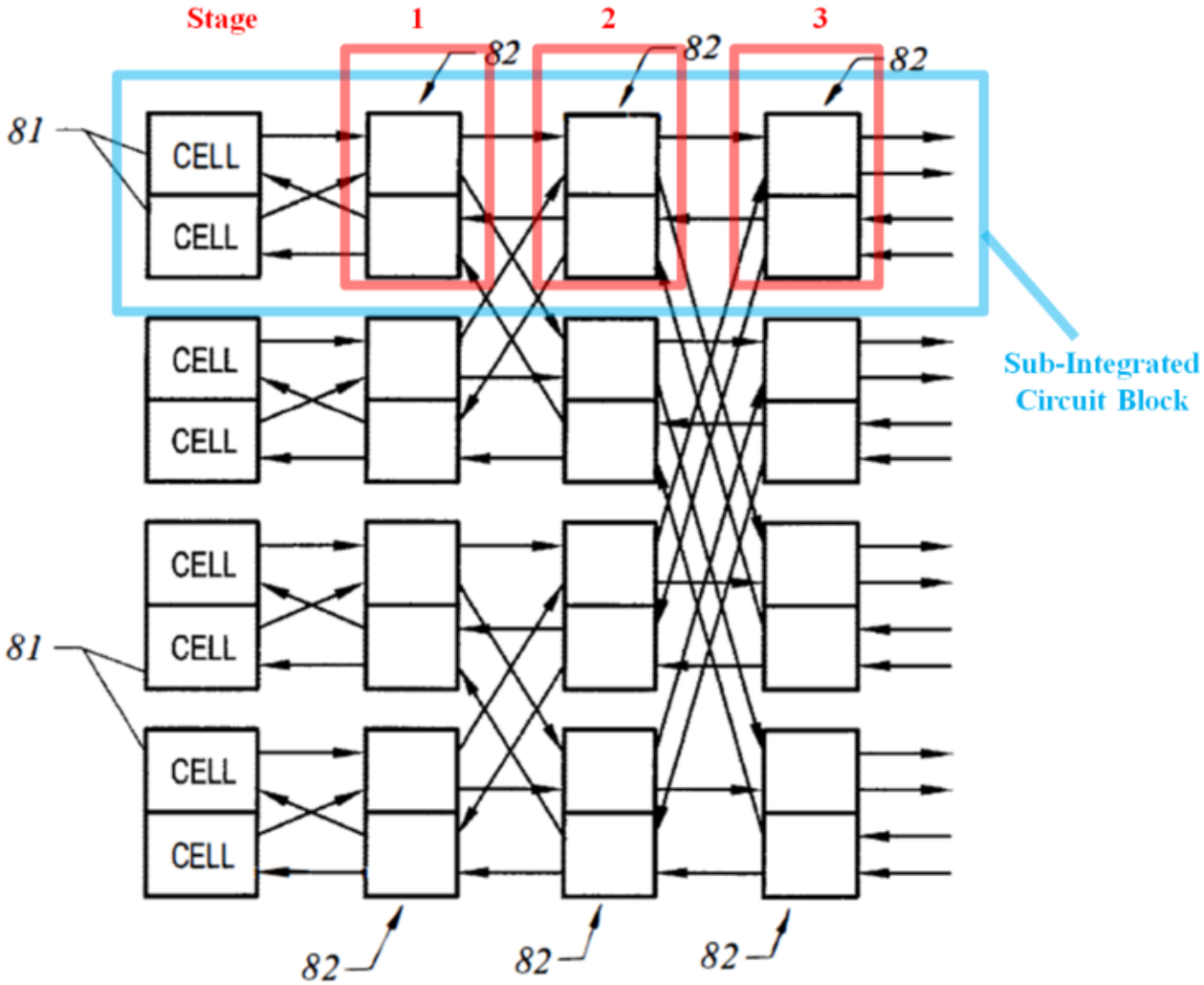



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶130.)

Similarly, as shown below in figure 13B of *Wong*, each sub-integrated circuit block includes four stages ("same number of stages") and each of the sub-integrated circuit blocks has the same construction ("same number of . . . said switches in each said stage"). (*Supra* Section IX.A.1(e); Ex. 1008, FIG. 13B; Ex. 1002, ¶131.)

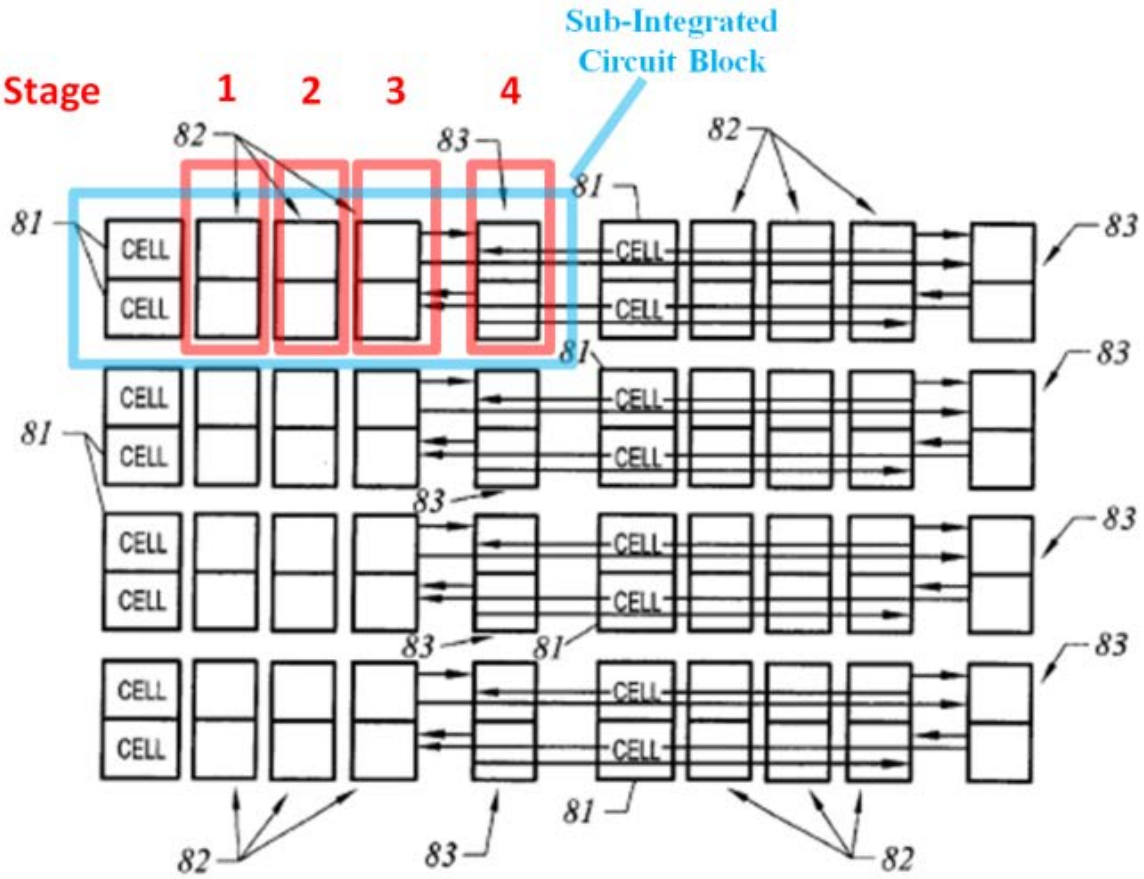



*FIG. 13B*

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶131.)

As further disclosed by *Wong*, each sub-integrated circuit block has the same configuration (same number of stages and same number of switches in each stage) regardless of the size of the network. (Ex. 1002, ¶132.) For example, the network

of figure 13A has a single column and each sub-integrated circuit block includes three stages:

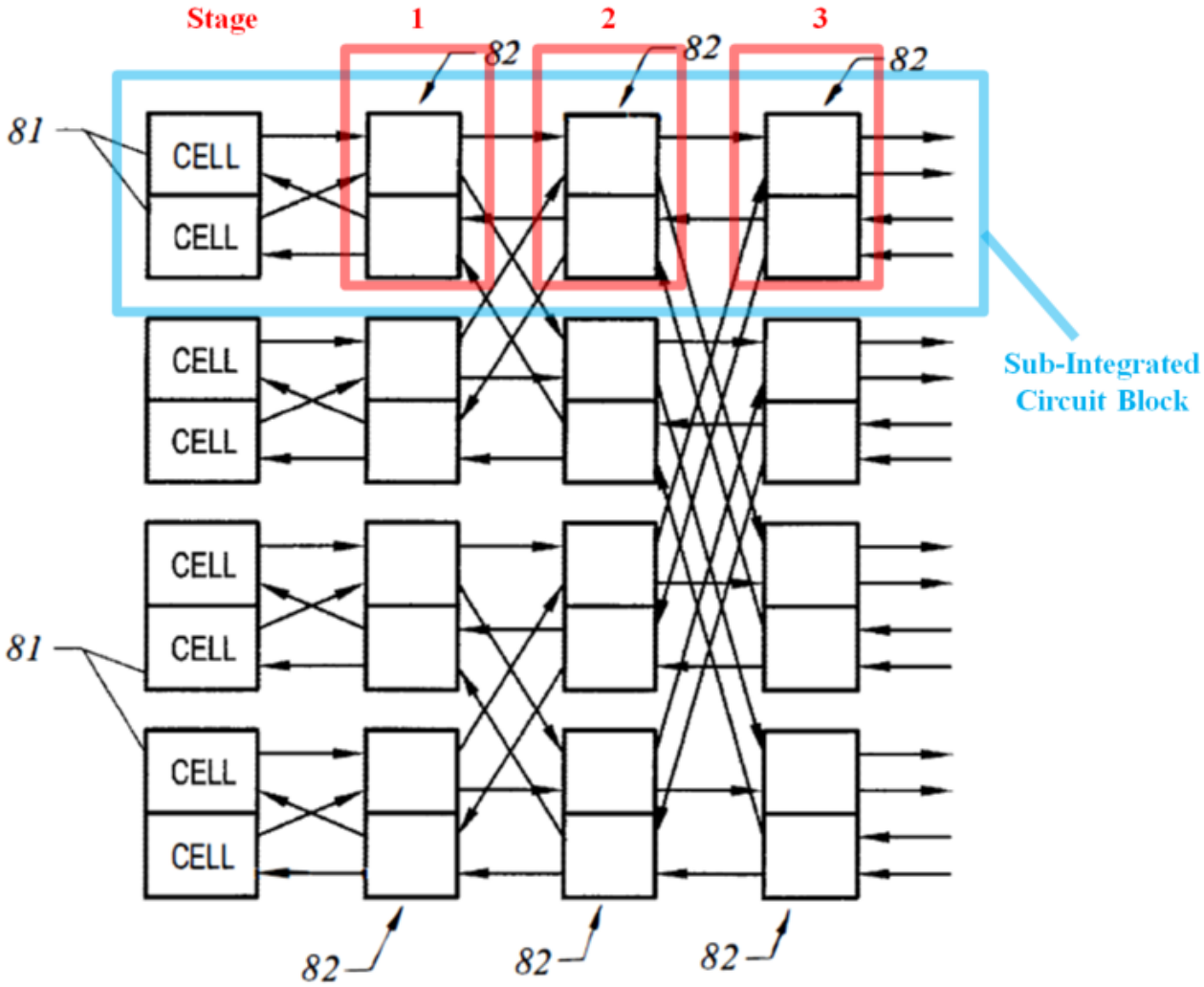



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶132.)

Expanding the network of figure 13A by a power of two in the horizontal direction creates a second column and adds a fourth stage to each sub-integrated circuit block as is shown in figure 13B:

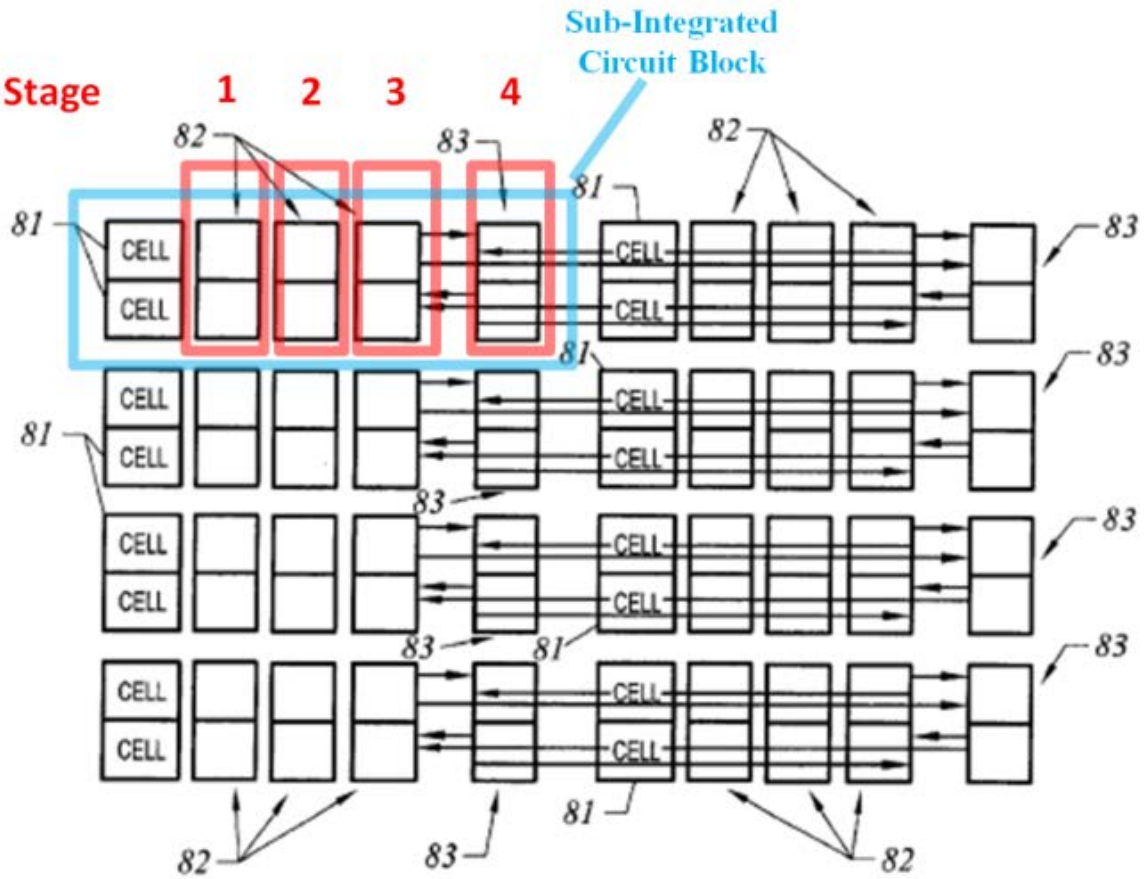



*FIG. 13B*

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶133.)

*Wong* further discloses that "[f]or each additional doubling of the number of cell columns, an additional column of switch cells must be added to each of the cell columns . . . ." (Ex. 1008, 13:38-40.) Therefore, *Wong* discloses that "regardless of the size of said two-dimensional grid" "each said plurality of sub-integrated circuit

block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid." (Ex. 1002, ¶134.) In other words, *Wong* discloses that as the network is scaled up, each of the sub-integrated circuit blocks has the same construction as the other sub-integrated circuit blocks in the network. (*Id.*) As demonstrated by the increase in size of the network in figure 13B in comparison to figure 13A, instantiations of the sub-integrated circuit blocks can be replicated both in the vertical (column) and horizontal (row) dimensions. (Ex. 1008, FIGs. 13A, 13B; Ex. 1002, ¶134.)

Petitioner anticipates that PO may argue that the sub-integrated circuit blocks of *Wong* are not replicable in the vertical (row) dimension of the two dimensional grid, similar to PO's argument during prosecution that in *Wong* "[i]t is clear as the network is scaled up, only columns are increasing." (Ex. 1004, 63.) But PO misrepresented the disclosure of *Wong* during prosecution, as *Wong* explicitly discloses that scaling up of the network can result in increased numbers of both columns and rows (i.e., both vertical and horizontal scaling.) (Ex. 1008, 13:33-49; Ex. 1002, ¶135.) With respect to horizontal scaling, figures 13A and 13B of *Wong* show expansion in the horizontal dimension as a second column of sub-integrated circuit blocks is added:

> For **multiple column arrays**, levels of switch cells are added to each column's sub-network. The new levels are connected together between columns in a topology consistent with a Benes Network. See FIG. 13B in which a level of switch cells 83 are added to make the connection between two FIG. 13A column arrays. For **each additional doubling of the number of cell columns**, an additional column of switch cells must be added to each of the cell columns, and the span for connecting these new columns to each other doubles as well.

(Ex. 1008, 13:33-42 (emphasis added); Ex. 1002, ¶135.)

In addition, contrary to PO's misrepresentation during prosecution that "[i]t is clear as the network is scaled up, only columns are increasing" (Ex. 1004, 63), *Wong* discloses adding additional rows and increasing the vertical dimension of the network:

> The strength of this column floorplan is that the number of cells in a column can be any power of 2, and **the number of rows can also independently be any power of 2**. This enables the generation of arrays containing numbers of cells that are any power of 2, and **with a selection of various aspect ratios**.

(Ex. 1008, 13:44-49 (emphasis added); Ex. 1002, ¶136.)

Therefore, *Wong* explicitly discloses increasing the number of rows of sub-integrated circuit blocks in order to increase the size of the network. (Ex. 1002, ¶137.) As *Wong* teaches, when the network is expanded, another level (stage) is added to each of the sub-integrated circuit blocks for "each additional doubling" of the size of the network. (Ex. 1008, 13:36-40; Ex. 1002, ¶137.)

Indeed, PO acknowledged during prosecution that:

> As disclosed in Fig. 13B [of *Wong*], columns are doubled by adding one more stage of switches in both the columns (for example Fig. 13A is replicated to get Fig. 13B and a new stage of switches 83 are added and the cross links between the new stage of switches become horizontal links).

(Ex. 1004, 63; Ex. 1002, ¶138.)

Therefore, contrary to PO's contention during prosecution that *Wong* only adds columns when the network is expanded, *Wong* discloses that the network can be scaled up by adding columns or rows, where each doubling in size adds another level (stage) that is the same in each of the sub-integrated circuit blocks. (Ex. 1002, ¶¶139-140.)

### 2. Claim 20

#### a) "The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks comprising any arbitrary hardware logic or memory circuits."

*Wong* discloses this limitation. (Ex. 1002, ¶¶141-142.) As discussed above with respect to claim limitations 1(b) and 1(c), *Wong* discloses an integrated circuit device that includes a "plurality of sub-integrated circuit blocks" where such blocks include logic cells 81. (*Supra* Sections IX.A.1(b)-(c); Ex. 1008, FIG. 13A; Ex. 1002, ¶141.)

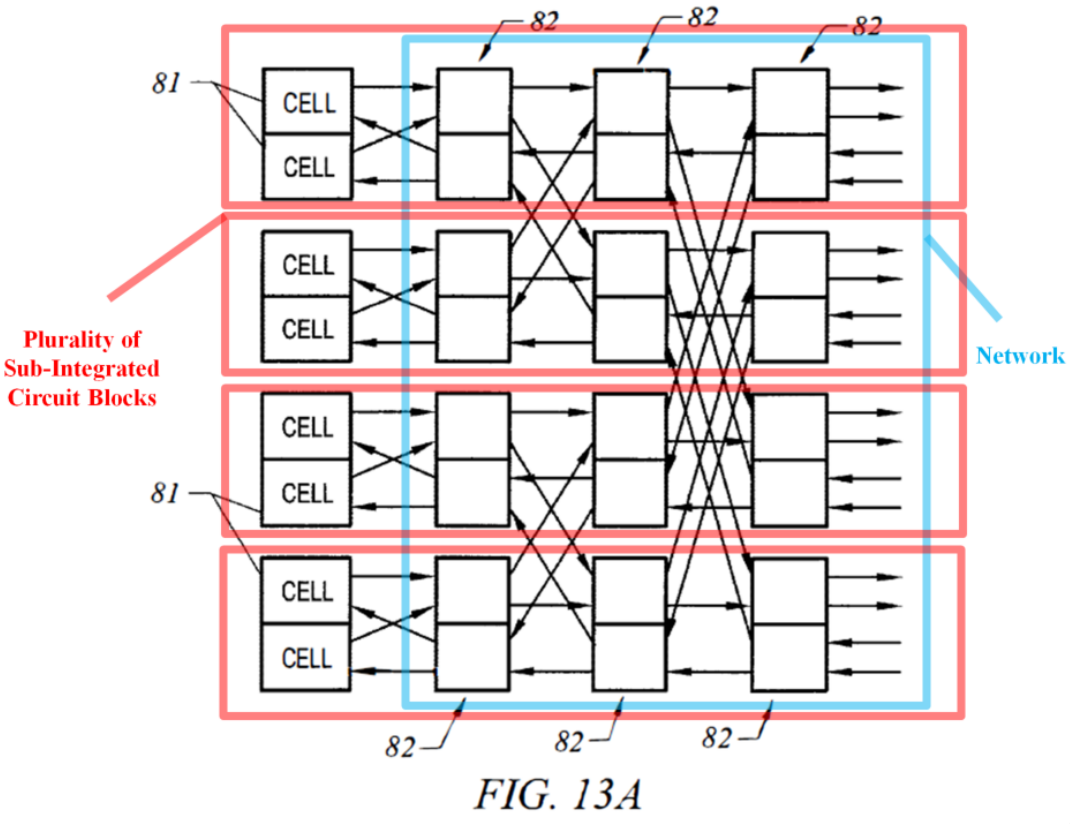



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶141.)

As further disclosed by *Wong*, "[i]n an FPGA, the logic is composed from building blocks called 'logic cells'" where "[a]n example of a typical logic cell is a 2-input NAND gate." (Ex. 1008, 6:55-58.) *Wong* further discloses that the logic cells that connect to the routing network in FPGA embodiments can be lookup tables. (Ex. 1008, 8:51, 9:9-11.) A POSITA would have understood that disclosure of NAND gates and lookup tables discloses "any arbitrary hardware logic" as recited in claim 20. (Ex. 1002, ¶142.)

**3. Claim 21**

**a) "The integrated circuit device of claim 1, wherein said switches comprising active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device or structured ASIC device."**

*Wong* discloses this limitation. (Ex. 1002, ¶¶143-145.) The '523 patent discloses that the switches in the network can be "one-time programmable cross points" that are implemented using vias that couple inlet links with outlet links at each of the crosspoints. (Ex. 1001, 32:62-33:1, 33:58-67; Ex. 1002, ¶143.)

*Wong* discloses Mask Programmable Gate Arrays (MPGAs) that include "one-time programmable cross points" implemented using vias in the same manner as the disclosure in the '523 patent. Specifically, *Wong* discloses "the disclosed Benes interconnect network can also be applied to MPGAs (Mask Programmable

Gate Arrays)" "where each switch cell used in the routing is replaced with . . . a metal via . . . ." (Ex. 1008, 14:28-32; Ex. 1002, ¶144.)

Therefore, *Wong* discloses "said switches comprising **active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device** or structured ASIC device" as recited in claim 21. (Ex. 1002, ¶145.)

**4. Claim 22**

**a) "The integrated circuit device of claim 1, wherein said switches comprising passive cross points or just connection of two links or not and said integrated circuit device is a[n] Application Specific Integrated Circuit (ASIC) device."**

*Wong* discloses this limitation. (Ex. 1002, ¶¶146-148.) For example, *Wong* discloses "each switch cell used in the routing is replaced with either a metal via or an end-to-end concatenation of two same layer metal wires . . . ." (Ex. 1008, 14:27-37; Ex. 1002, ¶148.) Therefore, *Wong* discloses "said switches comprising . . . just connection of two links or not," by disclosing metal vias connecting links or the concatenation of two wires. (Ex. 1002, ¶147.) *Wong* also discloses that the FPGA and MPGA embodiments are used in ASICs. (Ex. 1008, 12:67-13:5; Ex. 1002, ¶147-148.)

### B. Ground 2: *Wong* Renders Obvious Claims 15-18, 32, and 47

#### 1. Claim 15

##### a) "The integrated circuit device of claim 1, wherein said horizontal and vertical links are implemented on two or more metal layers."

*Wong* discloses or suggests this limitation. (Ex. 1002, ¶¶149-152.) As discussed above with respect to claim element 1(j), *Wong* discloses that the cross links in the networks of figures 13A and 13B are implemented using horizontal and vertical links. (*Supra* Section IX.A.1(j).) *Wong* further discloses that the networks shown in figures 13A and 13B are included in FPGAs, which are integrated circuits that can be implemented using complementary metal-oxide-semiconductor (CMOS) technology. (Ex. 1008, 4:66-5:2, 5:22-25; Ex. 1002, ¶150.) *Wong* further discloses that the interconnections between switches, which include the cross links that are vertical and horizontal links as discussed above with respect to claim feature 1(j), are implemented using metal conductors. (Ex. 1008, 13:50-53; Ex. 1002, ¶150.) *Wong* discloses integrated circuits with multiple layers of metal, which a POSITA would have understood to be typical of most integrated circuits in the early 2000s timeframe. (Ex. 1008, 14:28-34; Ex. 1002, ¶150.)

While *Wong* does not explicitly disclose that the "horizontal and vertical links are implemented on two or more metal layers," it would have been obvious to

implement this feature in *Wong*'s integrated circuit device. (Ex. 1002, ¶151.) Such an implementation would have been a mere combination of known components and technologies (e.g., horizontal and vertical links as in *Wong*, and multiple metal layers as also disclosed in *Wong*), according to known methods, to produce predictable results, and a POSITA would have had a reasonable expectation of success regarding this implementation. (*Id.*) *See KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). A POSITA would have understood that because the links are implemented using metal wires in *Wong*, using two or more layers for the links is either necessarily present in *Wong* or a POSITA would have been motivated to implement the links in two or more metal layers. (Ex. 1002, ¶151.) For example, as shown in figure 13A of *Wong* (annotated below), certain cross links overlap between the switches. (*Id.*) If the cross links were implemented using only a single metal layer, a short circuit would occur where they intersect, whereas if they are routed on different metal layers, no such shorting occurs as they are overlapping instead of intersecting. (*Id.*)

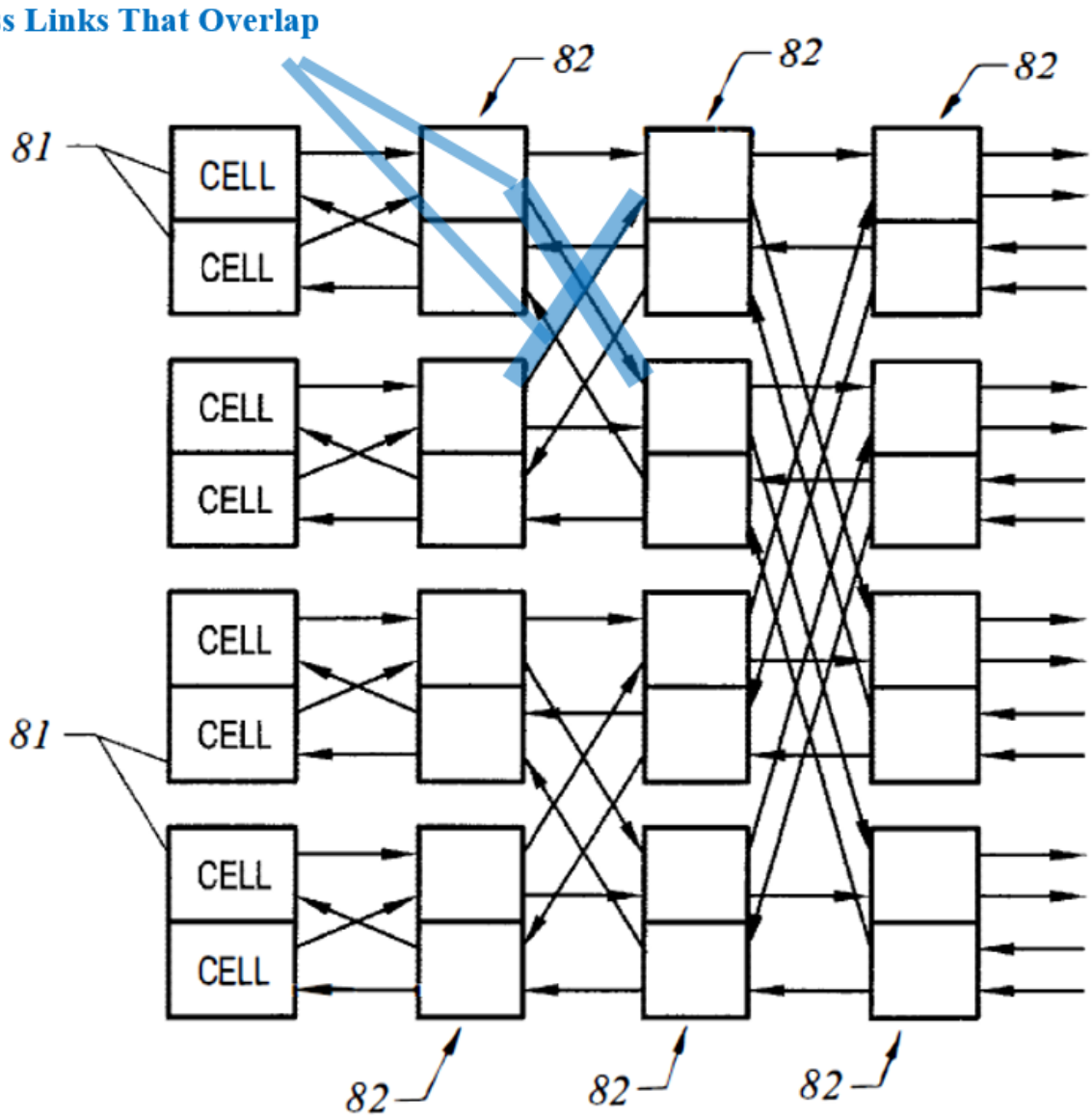



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶151.)

Therefore, a POSITA would have understood that *Wong* discloses or suggests that the "horizontal and vertical links are implemented on two or more metal layers," as claimed. (Ex. 1002, ¶152.)

**2. Claim 16**

**a) "The integrated circuit device of claim 1, wherein said switches comprising active and reprogrammable cross points and said each cross point is programmable by an SRAM cell or a Flash Cell."**

*Wong* discloses or suggests this limitation. (Ex. 1002, ¶¶153-156.) *Wong* discloses that the FPGA integrated circuits can be "SRAM-based FPGA[s]." (Ex. 1008, 2:25-26, 3:20-22 ("Current SRAM (Static Random Access Memory)-based FPGA products conform to the interconnect architecture as illustrated in FIG. 1.").) *Wong* further discloses that a configuration bit is used to determine the connectivity of the different links within the network. (*Id.*, 3:48-50, 5:4-13.) A POSITA would have known that in an SRAM-based FPGA, SRAM memory cells are used to store the configuration bits used in determining the different connection in the network. (Ex. 1002, ¶¶153-154 (citing Ex. 1043, 1:22-2:25; Ex. 1044, 1:30-60.)

In addition, *Wong* discloses that while switches implemented with multiplexers can be used in the FPGA designs, replacing sub-networks in the network with crossbar switches reduces the latency of the network. (Ex. 1008, 11:30-42 ("the maximum latency can be reduced if just the lowest levels of Benes networks are substituted with crossbars"); Ex. 1002, ¶155.)

While *Wong* does not explicitly disclose that "said switches comprising active and reprogrammable cross points and said each cross point is programmable by an

SRAM cell or a Flash Cell," it would have been obvious to implement such features. (Ex. 1002, ¶156.) Such an implementation would have been a mere combination of known components and technologies, according to known methods, to produce predictable results, and a POSITA would have had a reasonable expectation of success regarding this implementation. (*Id.*) *KSR*, 550 U.S. at 416. A POSITA would have understood that in an "SRAM-based FPGA" as disclosed by *Wong*, the control bits that control the switches would predictably be implemented using SRAM cells that store the "1s" and "0s" that are the control bits. (Ex. 1002, ¶156.) Such a POSITA would also have understood that a "rearrangeable crossbar" as disclosed by *Wong* includes "reprogrammable crosspoints" where the programming would be based on the control bits stored in the SRAM cells. (*Id.*) It would have been obvious for a POSITA reading *Wong* to use SRAM cells in an "SRAM-based FPGA" to control the "rearrangeable crossbar" because SRAM cells provide a well-understood data storage medium on integrated circuits and the control bits that determine the connectivity in the crossbar are easily stored in the SRAM, which is a reprogrammable memory. (*Id.*)

### 3. Claim 17

#### a) "The integrated circuit device of claim 1, said sub-integrated circuit blocks are of equal die size."

*Wong* discloses or suggests this feature. (Ex. 1002, ¶¶157-159.) As discussed above with respect to claim element 1(k) and shown in figures 13A, 13B, and 14A, each of the sub-integrated circuit blocks includes the same number of stages and the same number of switches. (Ex. 1008, FIGs. 13A, 13B, 14C; *supra* Section IX.A.1(k).)

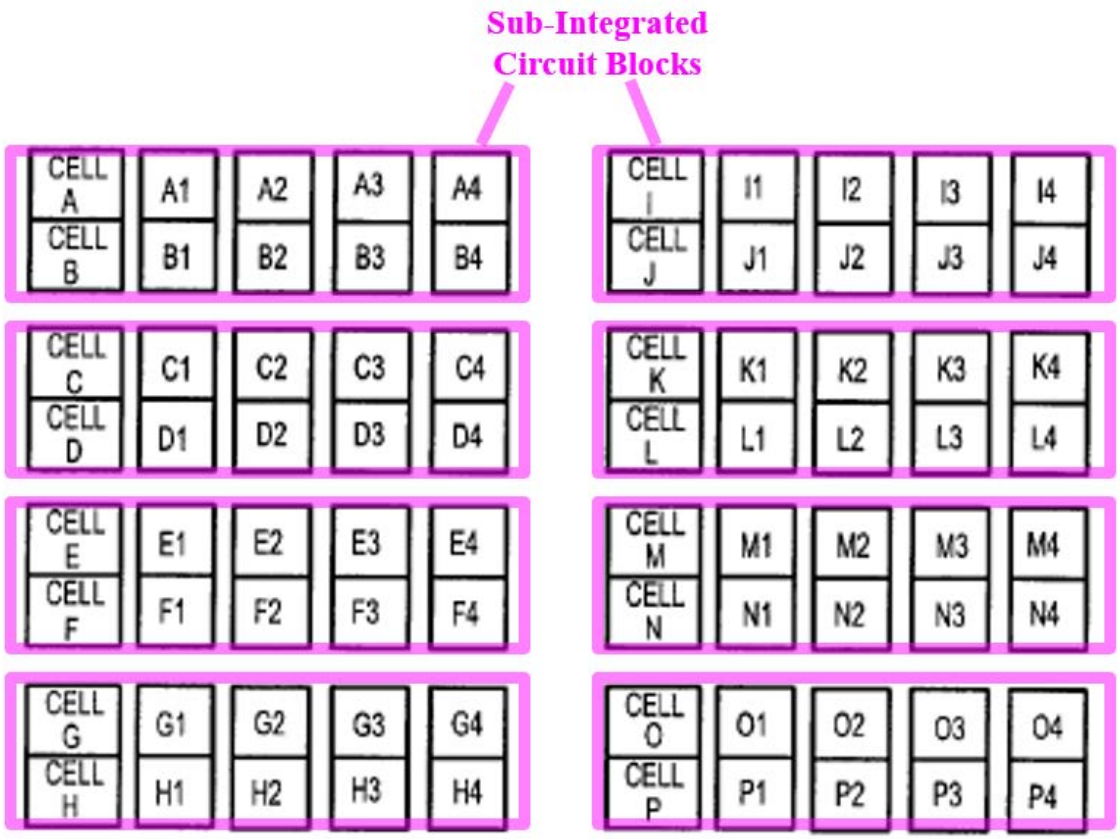



*FIG. 14A*

(Ex. 1008, FIG. 14A (annotated); Ex. 1002, ¶157.)

Therefore, *Wong* discloses that each sub-integrated circuit block has the same configuration (same number of stages and same number of switches in each stage) in the network. (*Supra* Section IX.A.1(k); Ex. 1002, ¶158.) *Wong* further discloses that an FPGA generator can be used to provide an end user with flexibility in terms of how the FPGA is configured. (Ex. 1008, 11:62-12:7 ("provide an FPGA array generator program"); Ex. 1002, ¶158.)

*Wong* further discloses that in some embodiments "the same switch cell is used everywhere in the generator." (Ex. 1008, 14:9.) A POSITA would have understood that if the same switch cell is used everywhere in the FPGA and the sub-integrated circuit blocks are configured the same as is shown in figures 13A, 13B, and 14A, then the "sub-integrated circuit blocks are of equal die size." (Ex. 1002, ¶159.) Even if it is not explicitly disclosed in *Wong*, it would have been obvious for a POSITA to use the same layout for each of the sub-integrated circuit blocks on *Wong*'s integrated circuit device. (*Id.*) A POSITA implementing *Wong*'s integrated circuit device would have had two choices regarding the die size for the sub-integrated circuit blocks: they could be implemented with equal die size, or unequal die size. (*Id.*) Thus, an implementation as in claim 17, where the sub-integrated circuit blocks are of equal die size, would have been recognized as being a mere choice among a finite number of known alternatives, each having predictable outcomes. (*Id.*) *KSR*, 550 U.S. at 421. Of these known alternatives, choice of equal die size would have been recognized as predictable and beneficial. (Ex. 1002, ¶159.) For example, A POSITA would have understood that reusing the layout for each of the blocks would have been more efficient from a design standpoint and would have ensured uniformity in placing the blocks in the two-dimensional grid and uniformity in block operation (delays, drive strength, etc.) Because a POSITA would have been

motivated to use the same layout for the sub-integrated circuit blocks, the area on the integrated circuit occupied by each of the sub-integrated circuit blocks ("die size") is the same. (*Id.*)

Therefore, the claimed feature of "equal die size" would have constituted an obvious implementation choice. (*Id.*) A POSITA would have been capable of implementing this feature, e.g., because implementing a desired layout and/or die size for a given circuit component was well within the skill of an ordinary artisan long before the alleged invention date. (*Id.*) A POSITA would have had a reasonable expectation of success regarding implementing "equal die size" as in claim 17, because this would have been a straightforward implementation involving a simple choice, as discussed above. (*Id.*)

**4. Claim 18**

**a) "The integrated circuit device of claim 15, where said sub-integrated circuit blocks are Lookup Tables (hereinafter "LUTs") and said integrated circuit device is a field programmable gate array (FPGA) device or field programmable gate array (FPGA) block embedded in another integrated circuit device."**

*Wong* discloses or suggests this limitation to the extent it can be understood. (Ex. 1002, ¶¶160-162.) As discussed above, *Wong* discloses or suggests an integrated circuit as recited in claim 15. (*Supra* Section IX.B.1.) Moreover, as discussed above with respect to claim element 1(a), *Wong* discloses that the

integrated circuit is an FPGA. (Ex. 1008, 1:14-21, 1:59-61, 3:7-10; 13:19-22, 13:36-38, FIGs. 13A, 13B.); *supra* Section IX.A.1(a); Ex. 1002, ¶160.) *Wong* discloses the inclusion of lookup tables with the routing network.[8] (Ex. 1002, ¶161.) For example, figure 13A of *Wong* shows a routing network made up of switches in stages, where the network is used to provide connections between logic cells. (Ex. 1008, FIG. 13A; Ex. 1002, ¶161.)

[8] Claim 18 conflicts with claim 1 by stating that the "sub-integrated circuit blocks **are** Lookup Tables." For the present analysis, Petitioner assumes that claim 18 requires that a lookup table is included in each of the sub-integrated circuit blocks recited in claim 1 like the configurable logic blocks or arbitrary digital circuits interconnected by the routing network. (Ex. 1001, 13:38-42; Ex. 1002, ¶161 fn.7.)

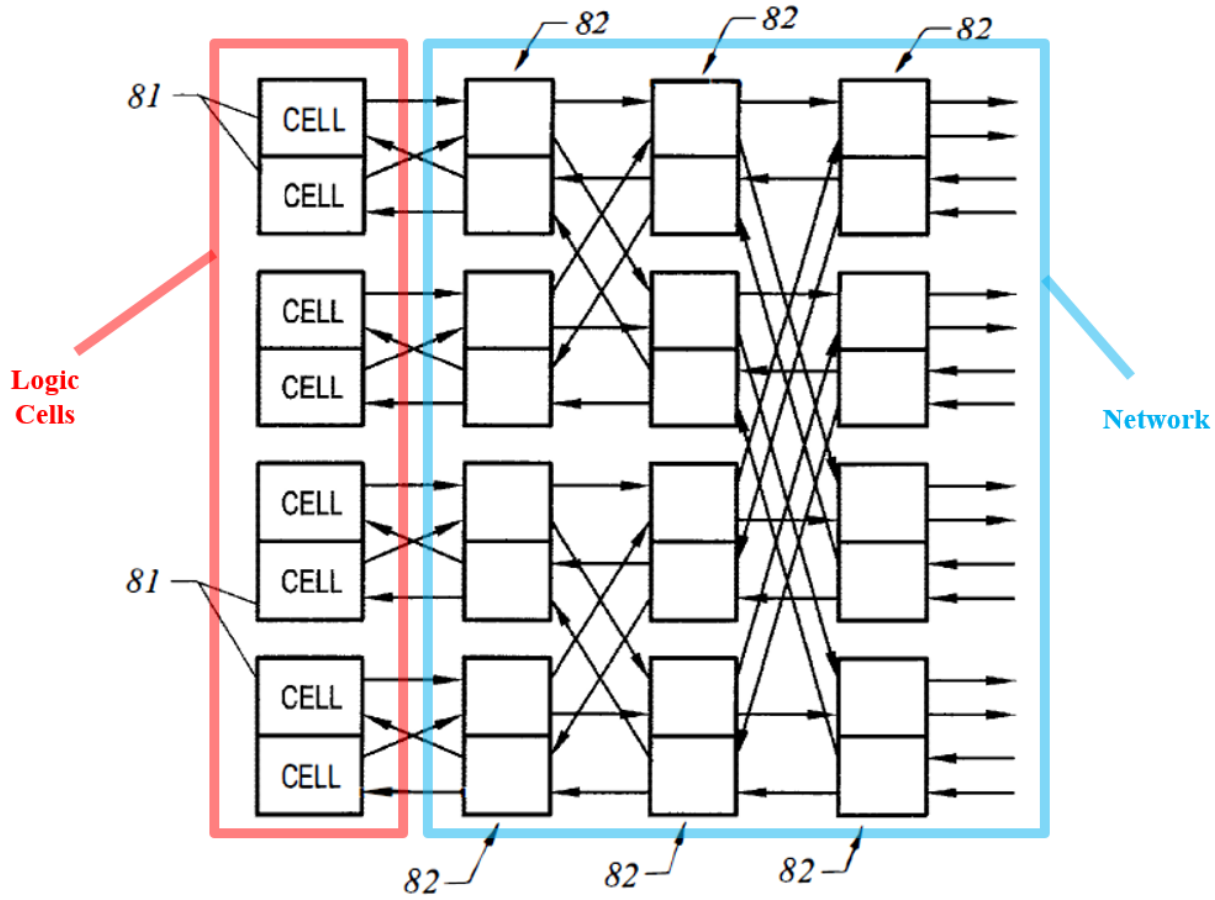



*FIG. 13A*

(Ex. 1008, FIG. 13A (annotated); Ex. 1002, ¶161.)

*Wong* further discloses that the logic cells that connect to the routing network in FPGA embodiments are lookup tables. (Ex. 1008, 8:51 ("Each logic cell is a 4-LUT (4 input Look Up Table)."), 9:9-11 ("For the purpose of analysis, assuming the logic cell is a 4-LUT (4-input Look-Up Table) with a latched output . . . ."); Ex. 1002, ¶162.).)

**5. Claim 32**

**a) "The integrated circuit device of claim 1, wherein said straight links connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and**

**Said cross links are connecting as vertical or horizontal or diagonal links between two different said sub-integrated circuit blocks."**

*Wong* discloses or suggests this feature for at least the same reasons discussed above for claim limitation 1(j). (Ex. 1002, ¶163; *supra* Section IX.A.1(j).)

**6. Claim 47**

**a) "The integrated circuit device of claim 1, wherein said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-inverting buffers."**

*Wong* discloses or suggests this limitation. (Ex. 1002, ¶¶164-169.) As discussed above with respect to claim element 1(g), *Wong* discloses a plurality of forward connecting links and a plurality of backward connecting links. (*Supra* Section IX.A.1(g).) *Wong* further discloses that buffers can be inserted "on signals with long routing lines in order to improve their overall delay" and that such buffers "can be inserted without affecting the logic of the design." (Ex. 1008, 10:60-64; Ex. 1002, ¶164.)

*Wong* also discloses that buffers can be inserted to lengthen the shorter delay paths until the delay paths match. (Ex. 1008, 11:1-6; Ex. 1002, ¶165.) While *Wong* does not explicitly disclose that the "said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them," it would have been obvious for a POSITA to include such buffers in the forward and backward connecting links. (Ex. 1002, ¶165.)

A POSITA reading *Wong* would have been motivated to use buffers in the forward and backward connecting links because such buffers provide a well-understood means for reducing propagation delay on long routing lines such as those between higher-level switches in different sub-integrated circuit blocks of *Wong*. (*Id.*, ¶166.) For example, as shown in annotated figure 13B of *Wong* below, the horizontal links between stages 3 and 4 of different sub-integrated circuit blocks are much longer than the links between lower level stages. (*Id.*; Ex. 1008, FIG. 13B.)

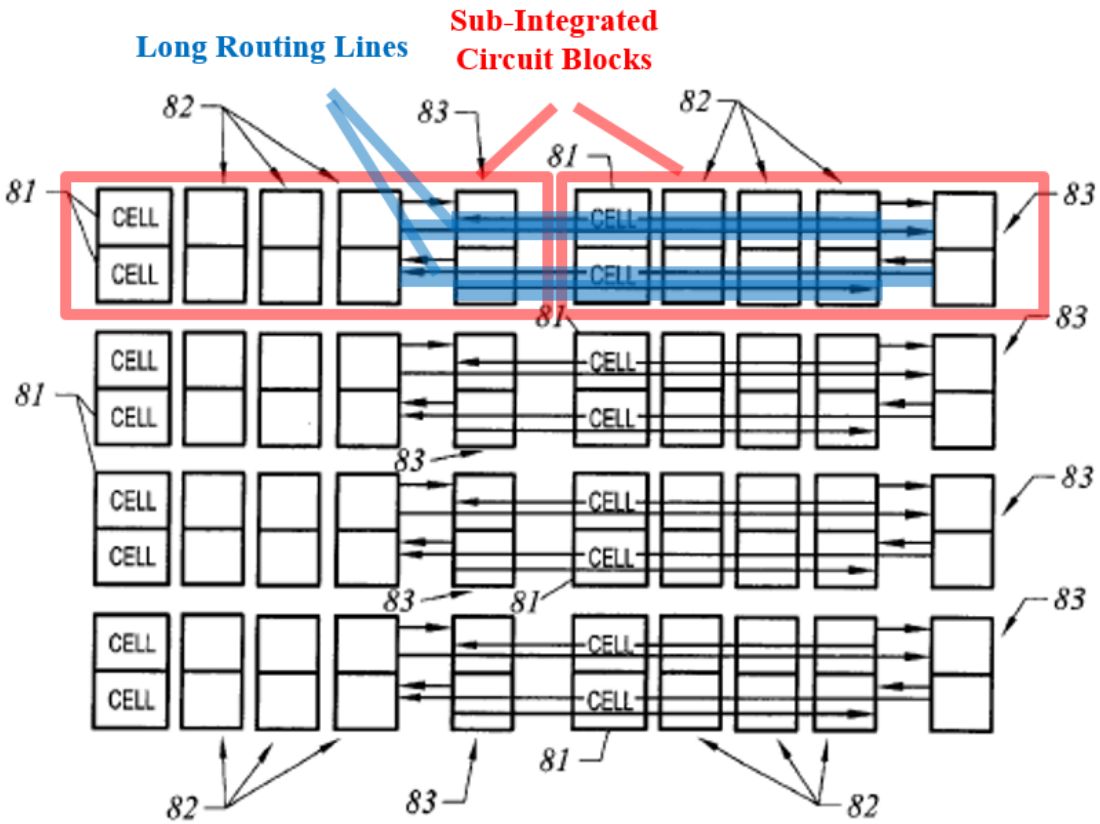



*FIG. 13B*

(Ex. 1008, FIG. 13B (annotated); Ex. 1002, ¶166.)

A POSITA would have understood that as the network disclosed in *Wong* is further scaled up in size, the length of the routing lines or "links" connecting the higher-level switches will continue to grow in length. (Ex. 1008, 13:38-42 ("For each additional doubling of the number of cell columns, an additional column of switch cells must be added to each of the cell columns, and **the span for connecting these new columns to each other doubles as well**.") (emphasis added); Ex. 1002, ¶167.) Therefore, a POSITA would have been motivated to include buffers in such

forward and backward connecting links, e.g., in order to improve the overall delay on such lines as is disclosed by *Wong*. (Ex. 1008, 10:59-67; Ex. 1002, ¶167.) A POSITA would also have been motivated to include buffers in the forward and backward connecting links to address any mismatch in delays, as *Wong* further discloses that buffers can be used to lengthen the shorter delay paths until the delay paths match. (Ex. 1008, 11:1-6; Ex. 1002, ¶167.)

A POSITA reading *Wong* would have understood that the buffers disclosed by *Wong* include "non-inverting" buffers. (Ex. 1002, ¶168.) *Wong* discloses that "[b]uffers can be inserted without affecting the logic of the design," thereby indicating that no further circuitry is required to maintain the logic of a circuit to which the buffers are added. (*Id*.; Ex. 1008, 10:60-61; *see also id*., FIGs. 11A, 11B.) If inverting buffers were used, further inversion would be required in order to restore the non-inverted state of the signal being inverted. (Ex. 1002, ¶168.) In any event, the use of a non-inverting buffer was well known long before the alleged invention date of the '523 patent, e.g., for adjusting or compensating timing in a circuit. (*Id.* (citing Ex. 1045, 2:9-11).) Therefore, a POSITA would have found the use of "non-inverting" buffers to be entirely predictable. (Ex. 1002, ¶168.)

For at least these reasons, it would have been obvious to configure *Wong*'s forward connecting links to "use a plurality of buffers to amplify signals driven

through them" and to configure *Wong*'s backward connecting links to "use a plurality of buffers to amplify signals driven through them" where "said buffers can be inverting or non-inverting buffers" as recited in claim 47. (*Id.*, ¶169.) This configuration would have been a mere combination of known components and technologies (e.g., forward connecting links and backward connecting links as disclosed in *Wong*, and buffers as also disclosed in *Wong*), according to known methods, to produce predictable results, and a POSITA would have had a reasonable expectation of success regarding this configuration. (*Id.*) *KSR*, 550 U.S. at 416.

## X. THE BOARD SHOULD NOT EXERCISE DISCRETION UNDER §325(D) TO DENY THE PETITION

As discussed above, the Examiner cited *Wong* for claim rejections during prosecution of the '275 application that ultimately issued as the '523 patent. (*Supra* Section VII.B; *see also supra* Section I.) But the manner in which Petitioner relies on *Wong* has minimal or no overlap with the arguments made during examination of the '275 application. That is because, as noted above in Section I, the Examiner simply erred in allowing the application after the applicant added limitations via amendment. This is not a situation where the Examiner made certain arguments regarding a claim limitation, showing how prior art was being mapped to (or not mapped to) the limitation. Rather, the Examiner apparently did not recognize the

relevance of portions of the *Wong* reference with respect to the limitations that the applicant added (e.g., the portions of *Wong* discussed above in Sections IX.A.1(j)-(k)), where Petitioner has clearly mapped *Wong* to limitations 1(j) and 1(k)). Moreover, the present Petition is supported by expert testimony that was not before the Examiner. (*See generally* Ex. 1002.)

Thus, the present case is distinguishable from *Becton, Dickinson and Co. v. B. Braun Melsungen AG*, IPR2017-01586, Paper No. 8 at 16-28 (PTAB December 15, 2017) where the Patent Office had already considered certain references during prosecution of the patent to which the patent-at-issue claimed priority. Accordingly, the Board should not exercise its discretion under § 325(d) to deny this Petition.

## XI. CONCLUSION

For the reasons given above, Petitioner requests institution of IPR for claims 1, 15-18, 20-22, 32, and 47 of the '523 patent, and a finding that the claims are unpatentable based on the above grounds.

Respectfully submitted,

Dated: December 16, 2019 By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

## CERTIFICATE OF COMPLIANCE

Pursuant to 37 C.F.R. § 42.24(d), the undersigned certifies that the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,269,523 contains, as measured by the word processing system used to prepare this paper, 13,795 words. This word count does not include the items excluded by 37 C.F.R. § 42.24 as not counting towards the word limit.

Respectfully submitted,

Dated: December 16, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner

## CERTIFICATE OF SERVICE

I hereby certify that on December 16, 2019, I caused a true and correct copy of the foregoing Petition for *Inter Partes* Review of U.S. Patent No. 8,269,523 and supporting exhibits to be served via express mail on the Patent Owner at the following correspondence address of record as listed on PAIR:

Konda Technologies, Inc
6278 Grand Oak Way
San Jose, CA 95135

A courtesy copy was also sent via electronic mail to the Patent Owner at the following address:

venkat@kondatech.com

Respectfully submitted,

Dated: December 16, 2019

By: /Naveen Modi/
Naveen Modi (Reg. No. 46,224)
Counsel for Petitioner