

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

FLEX LOGIX TECHNOLOGIES, INC.
Petitioner

v.

KONDA TECHNOLOGIES INC.
Patent Owner

Patent No. 8,369,523 B2

**DECLARATION OF R. JACOB BAKER, PH.D., P.E.
IN SUPPORT OF PETITION FOR *INTER PARTES* REVIEW
OF U.S. PATENT NO. 8,369,523**

TABLE OF CONTENTS

I.	INTRODUCTION	1
II.	BACKGROUND AND QUALIFICATIONS	1
III.	MATERIALS REVIEWED	5
IV.	PERSON OF ORDINARY SKILL IN THE ART.....	6
V.	TECHNICAL BACKGROUND	7
A.	Field-Programmable Gate Arrays (FPGAs).....	8
VI.	OVERVIEW OF THE '523 PATENT	17
VII.	CLAIM CONSTRUCTION	25
VIII.	OVERVIEW OF THE PRIOR ART.....	25
A.	<i>Wong</i>	25
IX.	THE PRIOR ART DISCLOSES Or Suggests ALL OF THE FEATURES OF CLAIMS 1, 15-18, 20-22, 32, and 47 OF THE '523 PATENT	30
A.	<i>Wong</i> Discloses the Features of Claims 1 and 20-22.....	30
1.	Claim 1	32
2.	Claim 20	120
3.	Claim 21	122
4.	Claim 22	125
B.	<i>Wong</i> Discloses or Suggests the Features of Claims 15-18, 32, and 47	127
1.	Claim 15	127
2.	Claim 16	130
3.	Claim 17	135
4.	Claim 18	139

5.	Claim 32	142
6.	Claim 47	142
X.	CONCLUSION	148

I, R. Jacob Baker, Ph.D., P.E., declare as follows:

I. INTRODUCTION

1. I have been retained by Flex Logix, Inc. (“Petitioner”) as an independent expert consultant in this proceeding before the United States Patent and Trademark Office (“PTO”) regarding U.S. Patent No. 8,269,523 (“the ’523 patent”) (Ex. 1001).¹ I have been asked to consider whether certain references disclose or suggest the features recited in claims 1, 15-18, 20-22, 32, and 47 of the ’523 patent. My opinions are set forth below.

2. I am being compensated at a rate of \$615/hour for my work in this proceeding. My compensation is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other interest in this proceeding.

II. BACKGROUND AND QUALIFICATIONS

3. I presently serve as a Professor of Electrical and Computer Engineering at the University of Nevada, Las Vegas (UNLV). All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In

¹ Where appropriate, I refer to exhibits that I understand are to be attached to the petition for *Inter Partes* Review of the ’523 patent.

forming my opinions, I have relied on my knowledge and experience in designing, developing, researching, and teaching regarding circuit design and memory devices referenced in this declaration.

4. I am over 18 years of age and, if I am called upon to do so, I would be competent to testify as to the matters set forth herein. I understand that a copy of my current curriculum vitae, which details my education and professional and academic experience, is being submitted by Petitioner. The following provides an overview of some of my experience that is relevant to the matters set forth in this declaration.

5. I have been teaching electrical engineering at UNLV since 2012. Prior to this position, I was a Professor of Electrical and Computer Engineering at Boise State University from 2000. Prior to my position at Boise State University, I was an Associate Professor Electrical Engineering between 1998 and 2000 and Assistant Professor of Electrical Engineering between 1993 and 1998 at the University of Idaho. I have been teaching electrical engineering since 1991.

6. I received my Ph.D. in Electrical Engineering from the University of Nevada, Reno in 1993. I also received a MS and BS in Electrical Engineering from UNLV in 1988 and 1986, respectively.

7. As described in my curriculum vitae, which I understand is being provided as Exhibit 1003, I am a licensed Professional Engineer in the state of Idaho and have more than 30 years of experience, including extensive experience in circuit designs for networks and communications including the design of modems, driver circuits, phase- and delay-locked loops for PCI, USB, and DDR standard specifications.

8. I have taught courses in integrated circuit design (analog, digital, mixed-signal, memory circuit design, etc.), linear circuits, microelectronics, communication systems, and fiber optics. As a professor, I have been the main advisor to nine Doctoral students and 79 Master's students.

9. I am the author of several books covering the area of integrated circuit design including: DRAM Circuit Design: Fundamental and High-Speed Topics (two editions), CMOS Circuit Design, Layout, and Simulation (four editions), and CMOS Mixed-Signal Circuit Design (two editions). I have authored, and coauthored, more than 100 papers and presentations in the areas of solid-state circuit design, the design of field-programmable gate array (FPGA) data converters, and circuits used in standard specification implementations including double data rate (DDR) for communications. I am the named inventor on 151 granted U.S. patents in CMOS integrated circuit designs including array topologies including flash memory and

DRAM. My textbook CMOS Circuit Design, Layout, and Simulation includes, among other things, sections covering digital logic gates as well as phase- and delay-locked loops for networking and communications.

10. I have received numerous awards for my work, including the Frederick Emmons Terman (the “Father of Silicon Valley”) Award. The Terman Award is bestowed annually upon an outstanding young electrical/computer engineering educator in recognition of the educator’s contributions to the profession.

11. I am a Fellow of the IEEE for contributions to memory circuit design. I have also received the IEEE Circuits and Systems Education Award (2011).

12. I have received the President’s Research and Scholarship Award (2005), Honored Faculty Member recognition (2003), and Outstanding Department of Electrical Engineering Faculty recognition (2001), all from Boise State University. I have also received the Tau Beta Pi Outstanding Electrical and Computer Engineering Professor award during my time at UNLV.

13. I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art.

III. MATERIALS REVIEWED

14. The opinions contained in this Declaration are based on the documents I reviewed, my professional judgment, as well as my education, experience, and knowledge regarding integrated circuits, including networks and switches used to implement field-programmable gate arrays (FPGAs).

15. In forming my opinions expressed in this Declaration, I reviewed the '523 patent (Ex. 1001); File History of the '523 patent (Ex. 1004); PCT Publication No. WO2008/147928 (Ex. 1005); U.S. Patent No. 10,003,553 (Ex. 1006); Body of PCT Application No. PCT/US08/64605 As Filed ("the '605 PCT") (Ex. 1007); U.S. Patent No. 6,940,308 ("*Wong*") (Ex. 1008); File History of U.S. Provisional Application No. 60/940,394 (Ex. 1026); U.S. Patent No. 3,358,269 ("*Benes*") (Ex. 1040); U.S. Patent No. 5,847,577 ("*Trimberger*") (Ex. 1043); U.S. Patent No. 7,558,967 ("*Wong-967*") (Ex. 1044); U.S. Patent No. 4,874,971 ("*Fletcher*") (Ex. 1045); U.S. Patent No. 10,050,904 (Ex. 1046); and any other materials I refer to in this Declaration in support of my opinions.

16. All of the opinions contained in this declaration are based on the documents I reviewed and my knowledge and professional judgment. My opinions have also been guided by my appreciation of how a person of ordinary skill in the art would have understood the claims and the specification of the '523 patent at the

time of the alleged invention, which I have been asked to initially consider was the mid-to-late-2000s timeframe (including May 25, 2007, the filing date of U.S. Provisional Patent Application No. 60/940,394, which I understand is the earliest possible priority date for the '523 patent.). My opinions reflect how one of ordinary skill in the art would have understood the '523 patent, the prior art to the patent, and the state of the art at the time of the alleged invention.

17. Based on my experience and expertise, it is my opinion that certain references disclose or suggest the features recited in claims 1, 15-18, 20-22, 32, and 47 of the '523 patent.

IV. PERSON OF ORDINARY SKILL IN THE ART

18. I am familiar with the level of ordinary skill in the art with respect to the alleged inventions of the '523 patent as of what I understand is the earliest possible priority date of May 25, 2007, which is the filing date of U.S. Provisional Patent Application No. 60/940,394 to which the '523 patent claims priority. Specifically, based on my review of the '523 patent, the technology, the educational level and experience of active workers in the field, the types of problems faced by workers in the field, the solutions found to those problems, the sophistication of the technology in the field, and drawing on my own experience, I believe a person of ordinary skill in the art would have had a master's degree in

electrical engineering or a similar field, and at least two to three years of experience with integrated circuits and networks. More education can supplement practical experience and vice versa. Depending on the engineering background and level of education of a person, it would have taken a few years for the person to become familiar with the problems encountered in the art and to become familiar with the prior and current solutions to those problems.

19. All of my opinions in this declaration are from the perspective of one of ordinary skill in the art, as I have defined it here, during the relevant timeframe, i.e., mid-to-late 2000s.

V. TECHNICAL BACKGROUND

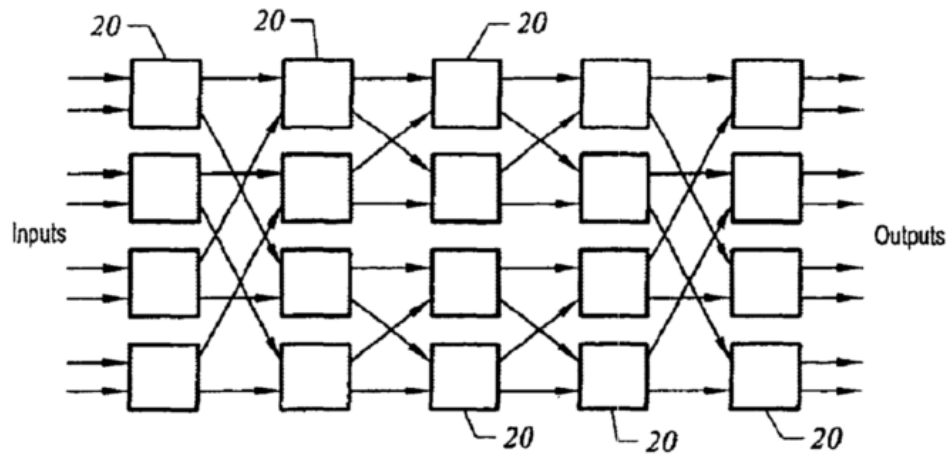
20. In this section, I present a brief overview of certain aspects of switching networks and FPGAs at the time of the alleged invention that will assist in better understanding the '523 patent and the prior art that I discuss in this declaration. For example, the prior art I discuss in this declaration and the '523 patent generally relates to switching networks that can be used to route signals between logic blocks included on an integrated circuit device. Below, I begin with a description of some fundamental aspects of FPGAs such as those described in the '523 patent and/or prior art references cited in this declaration.

A. Field-Programmable Gate Arrays (FPGAs)

21. *Wong* (Ex. 1008), which was filed on January 23, 2004 and claims priority to a provisional application filed on August 4, 2000 (i.e., long before the alleged invention in the '523 patent), and which issued on September 6, 2005, provides a good overview of FPGAs and example networks used in FPGAs. FPGAs are integrated circuits that are designed to allow a user to configure the circuitry of the FPGA to perform a desired function after the FPGA integrated circuit has already been manufactured. (Ex. 1008 at 1:18-21.) As the name implies, FPGAs include an array or arrays of programmable logic blocks (e.g., gates), where the connections between the logic blocks can be set up after manufacturing and therefore are considered to be “field-programmable.” In other words, once manufacturing is complete, the FPGA integrated circuit device includes logic and a network interconnecting the logic, where the user can configure the logic and interconnection network such that the FPGA performs a desired processing function. The interconnection network on the FPGA is used to provide the configurable connections between the programmable logic blocks. (*Id.* at 1:22-25.)

22. In FPGAs such as those discussed in *Wong*, the interconnection network that connects the logic blocks includes links between programmable switches, where the links provide connections between the switches and also provide

connections from the switches to the logic blocks in the FPGA. As such, the links are the inputs to, and outputs from, the switches. Within each switch, the inputs to the switch are programmably routed to particular outputs of the switch. (*Id.* at 1:61-2:6.) For example, figure 3D of *Wong* (below) illustrates an interconnection network that includes a plurality of switches 20 (shown as square boxes) that can be used to route any of the inputs to the network on the left to any of the outputs of the network on the right. (*Id.* at 4:18-26, FIG. 3D.) The arrows between the switches correspond to the “links” in the network. According to *Wong*, the particular network illustrated in figure 3D is an 8x8 Benes network that has eight inputs and eight outputs. (*Id.* at 2:36-37.)



(*Id.* at FIG. 3D.)

23. Each of the switches 20 shown in the network of figure 3D above is a 2x2 switch that has two inputs and two outputs. (*Id.* at 2:31-37, 5:4-6, FIG. 3D.) As shown in figures 2A and 2B of *Wong* below, each switch can be set up in either a “pass” configuration where the inputs are passed straight through to the outputs (with the upper input passed to the upper output, and the lower input passed to the lower output) or set up in a “cross” configuration where the upper input is routed to the lower output and vice-versa. (*Id.* at 2:27-29, 5:6-13.) As further disclosed by *Wong*, “[t]he building block of the described Benes network is the 2x2 (2 input, 2 output) switch 20, having operations illustrated in FIGS. 2A and 2B” (*id.* at 5:4-6) where “[t]hese 2x2 switches are connected in a specific topology to build a Benes network” (*id.* at 5:26-27).

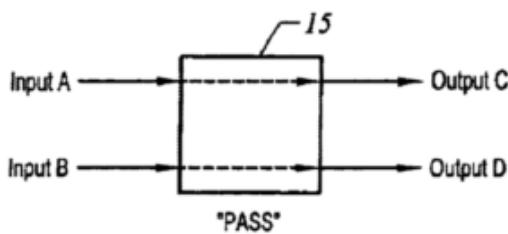


FIG. 2A

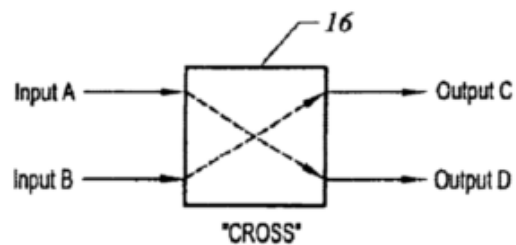


FIG. 2B

(*Id.* at FIGs. 2A, 2B.)

24. A controlling configuration bit is used to determine how the inputs to the switch are routed to the outputs of the switch (e.g., whether the switch is in a “pass” or “cross” configuration). (*Id.* at 3:48-50.) For example, figure 2C of *Wong*,

replicated below, shows how multiplexers are used to implement a 2x2 switch with the functionality of the switches shown in figures 2A and 2B. The multiplexers are controlled by a configuration bit or control bit that is used to determine which outputs are connected to which inputs of the switch.

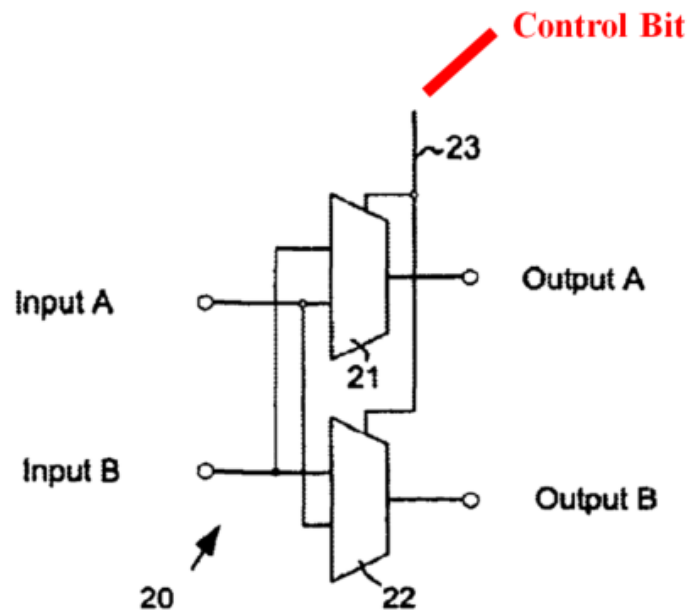
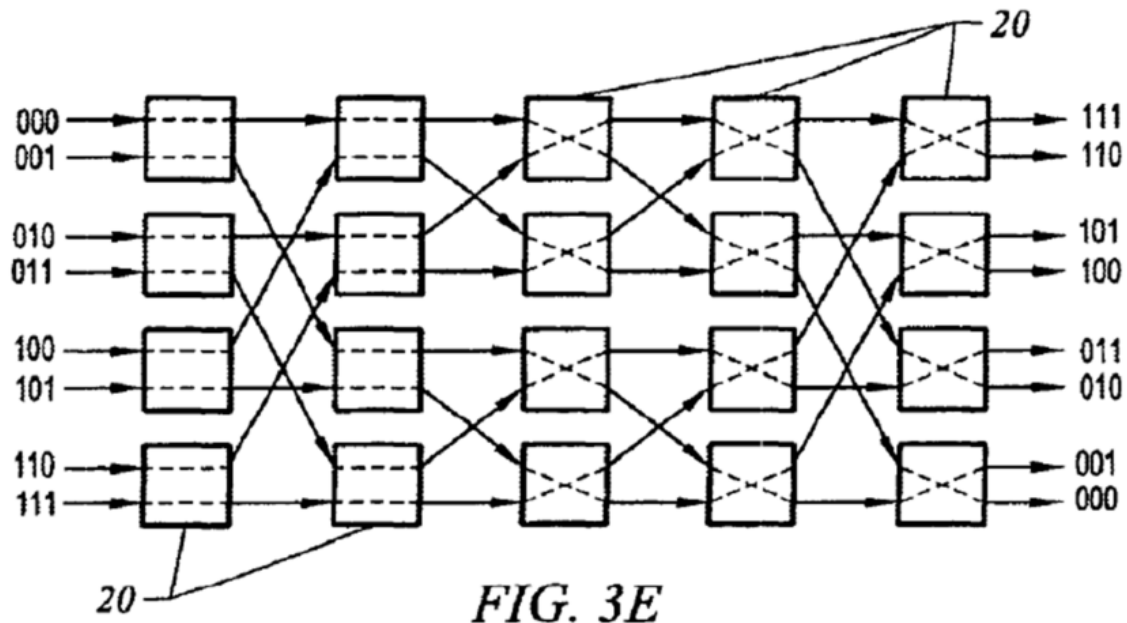


FIG. 2C

(Ex. 1008 at FIG. 2C (annotated).)

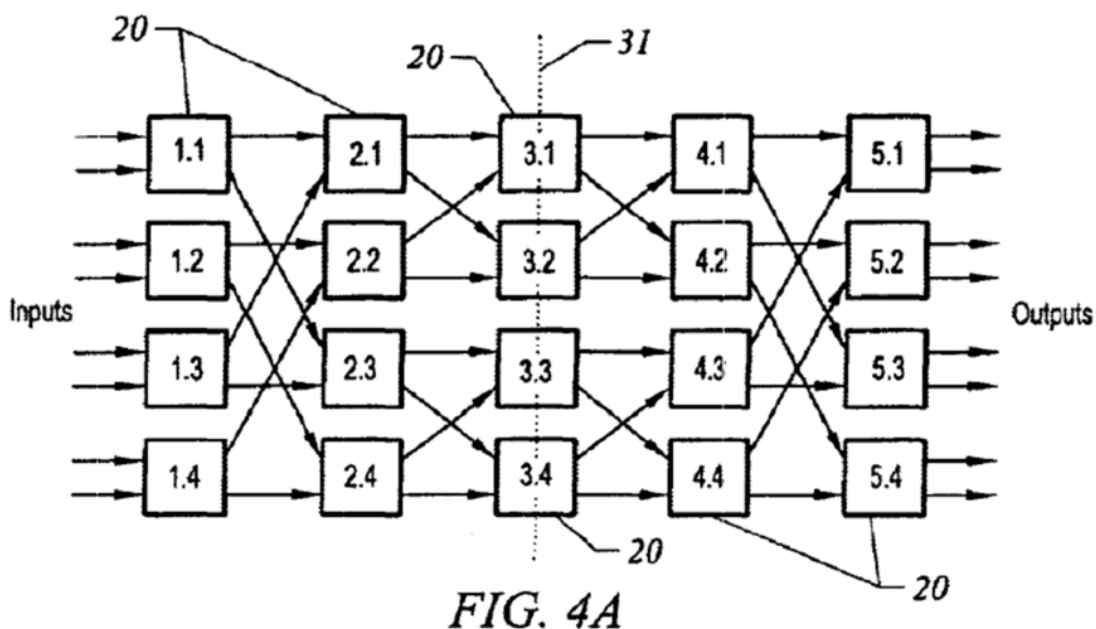
25. By controlling the individual switches in the network, the routing of the inputs to the network to selected outputs can be controlled. In the example configuration shown below in figure 3E of *Wong*, by placing some of the switches in the “pass” configuration and others in the “cross” configuration, the network of

switches can be used to route any of the eight inputs to any of the eight outputs. (*Id.* at 5:65-67.) For example, as shown in figure 3E of *Wong* below, a particular configuration of the switches reverses the ordering of input signals at the output terminals of the network. (*Id.* at 2:38-40, 5:67-6:5.) For example, by setting each of the switches to be either “pass” or “cross” as shown below in figure 3E, the top-most input on the left (“000”) is routed such that it comes out at the bottom-most output on the right, whereas the bottom-most input on the left (“111”) is routed to the top-most output on the right. In traversing the network, each of the inputs to the network passes through five switches in the network.



(*Id.* at FIG. 3E.)

26. As demonstrated by *Wong*, it was well known long before the time of the alleged invention in the '523 patent to use networks, such as, for example, the one depicted above in figure 3E of *Wong*, in FPGA devices. Moreover, it was also well known to modify such networks in order to make them more efficient as the interconnection network for an FPGA. For example, because the logic cells used in the FPGA include both inputs and outputs, the network can be folded in half in order to put both the inputs to the network and the outputs from the network adjacent to each other for easy connection to the inputs and outputs of the logic cells. (*Id.* at 6:52-61.) Such folding is illustrated by figure 4A of *Wong*, where the folding is done along the dotted line 31. (*Id.* at 6:65-67.)



(*Id.* at FIG. 4A.)

27. The resulting folded network is shown in figures 4B and 4C of *Wong* below, where figure 4C has rearranged the connections between the switches in the network so that the shorter connections are closer to the logic cells, which are placed on the left hand side of the network. (*Id.* at 7:6-21.) As can be seen in figures 4B and 4C, folding the network puts switches 1.1 and 5.1 together (both of these switches are two stages away from switch 3.1 of figure 4A) and switches 2.1 and 4.1 together (both of these switches are one stage away from switch 3.1).

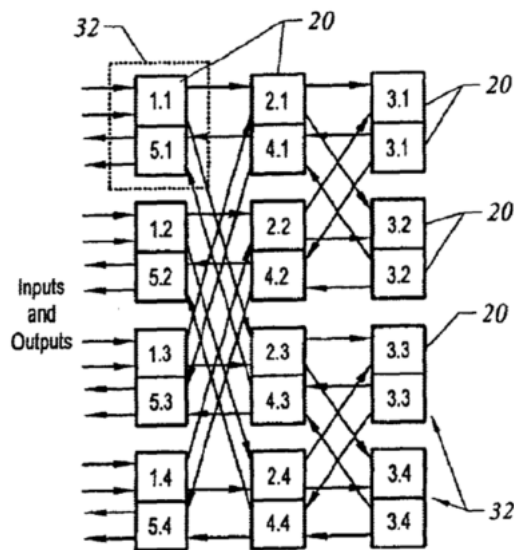


FIG. 4B

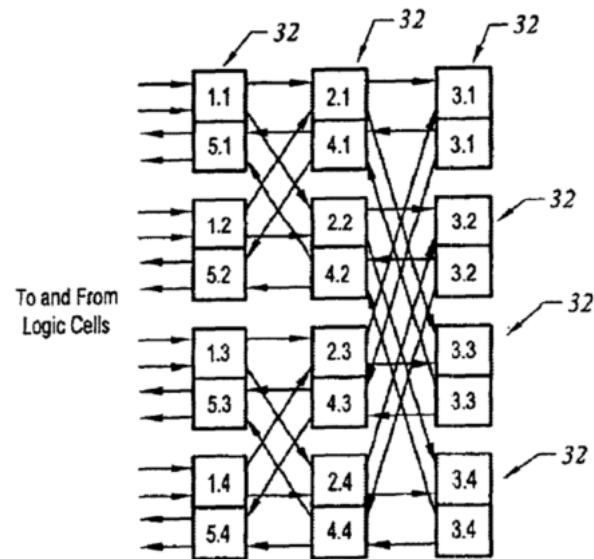


FIG. 4C

(*Id.* at FIGs. 4B, 4C.)

28. A physical layout of the network shown in figure 4C with the accompanying logic cells for an FPGA is shown below in figure 13A of *Wong*. The

physical layout shown in Figure 13A includes the network of switches 82 and associated logic cells 81. (*Id.* at 13:12-26.)

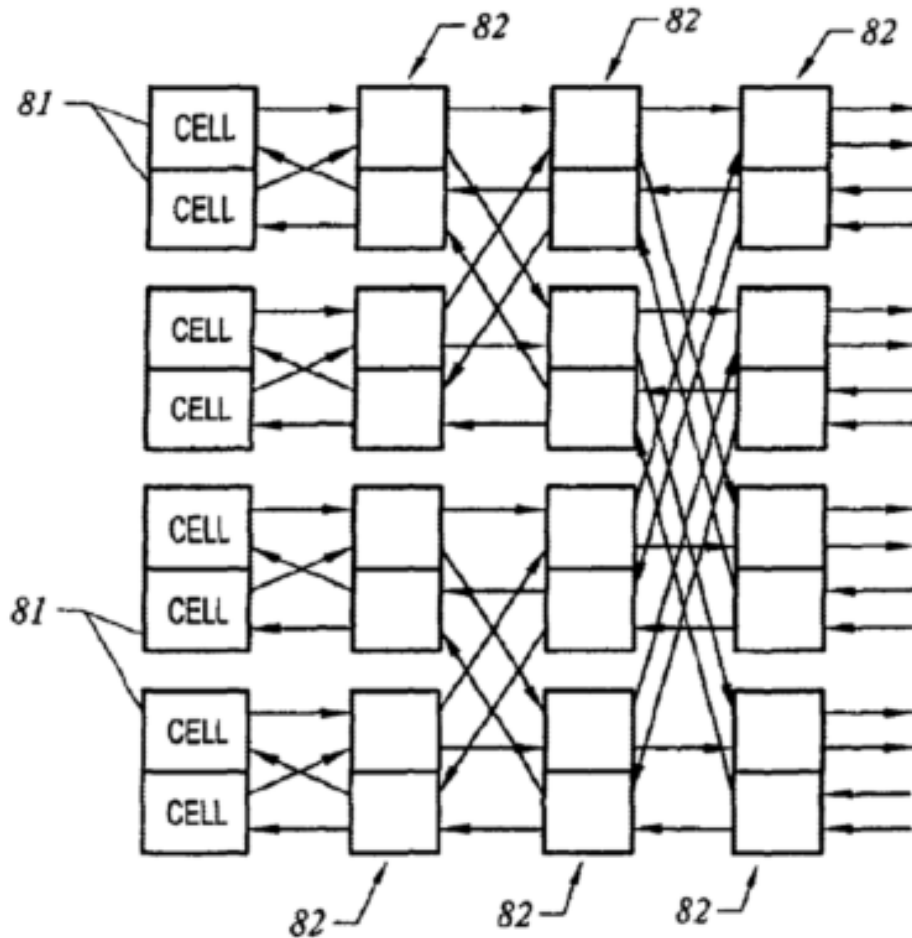


FIG. 13A

(*Id.* at FIG. 13A.)

29. A person of ordinary skill in the art would have understood that the physical layout corresponds to how the circuitry is physically arranged on the integrated circuit device. In other words, in the integrated circuit FPGA that includes

the network shown in figure 13A above, the logic cells 81 would be arranged vertically in a column, and the switches 82 would be arrayed in rows and columns with appropriate connections corresponding to the illustrated links provided on the integrated circuit. The arrows on the right-hand side of figure 13A correspond to the top level connections between the network and primary input/output (I/O) of the FPGA. (*Id.* at 13:42-43.) A person of ordinary skill in the art would have understood that the signals provided to the FPGA, which the logic cells 81 are used to process, are provided on the primary inputs of the FPGA, whereas the results generated by that processing are provided on the primary outputs of the FPGA.

30. As depicted in figure 13A of *Wong*, logic cells 81 are included in the FPGA along with switch cells 82. (*Id.* at 13:22-23 (“There are two logic cells 81 per switch cell 82....”).) The logic cells in an FPGA are used to process the inputs provided to the FPGA. The processing functions performed by the logic cells are often configurable by the user. (*Id.* at 7:32-38, 8:51, 9:10, 14:44-48.) As such, not only the connections between the logic cells are configurable, but the actual processing functions performed by the logic cells are also configurable by the user after manufacturing is complete.

VI. OVERVIEW OF THE '523 PATENT

31. The '523 patent is entitled “VLSI Layouts of Fully Connected Generalized Networks.” (Ex. 1001 at Title.) The '523 patent acknowledges that multi-stage hierarchical networks were known and used in many applications at the time of the alleged invention. (Ex. 1001 at 2:25-27 (“Multi-stage interconnection networks such as Benes networks and butterfly fat tree networks are widely useful in telecommunications, parallel and distributed computing.”).) Practical applications where the multi-stage hierarchical networks can be used include FPGAs. (*Id.* at 2:62-67.)

32. The '523 patent recognizes that VLSI (very large scale integration) layouts for integrated circuits with such networks were known, but states that such layouts are “inefficient and complicated.” (*Id.* at 2:28-30.) For example, the '523 patent acknowledges that *Wong* (Ex. 1008) discloses a layout of a Benes network.² (Ex. 1001 at 2:56-61.) However, the '523 patent contends that prior art network layouts “require large area to implement the switches on the chip, large number of

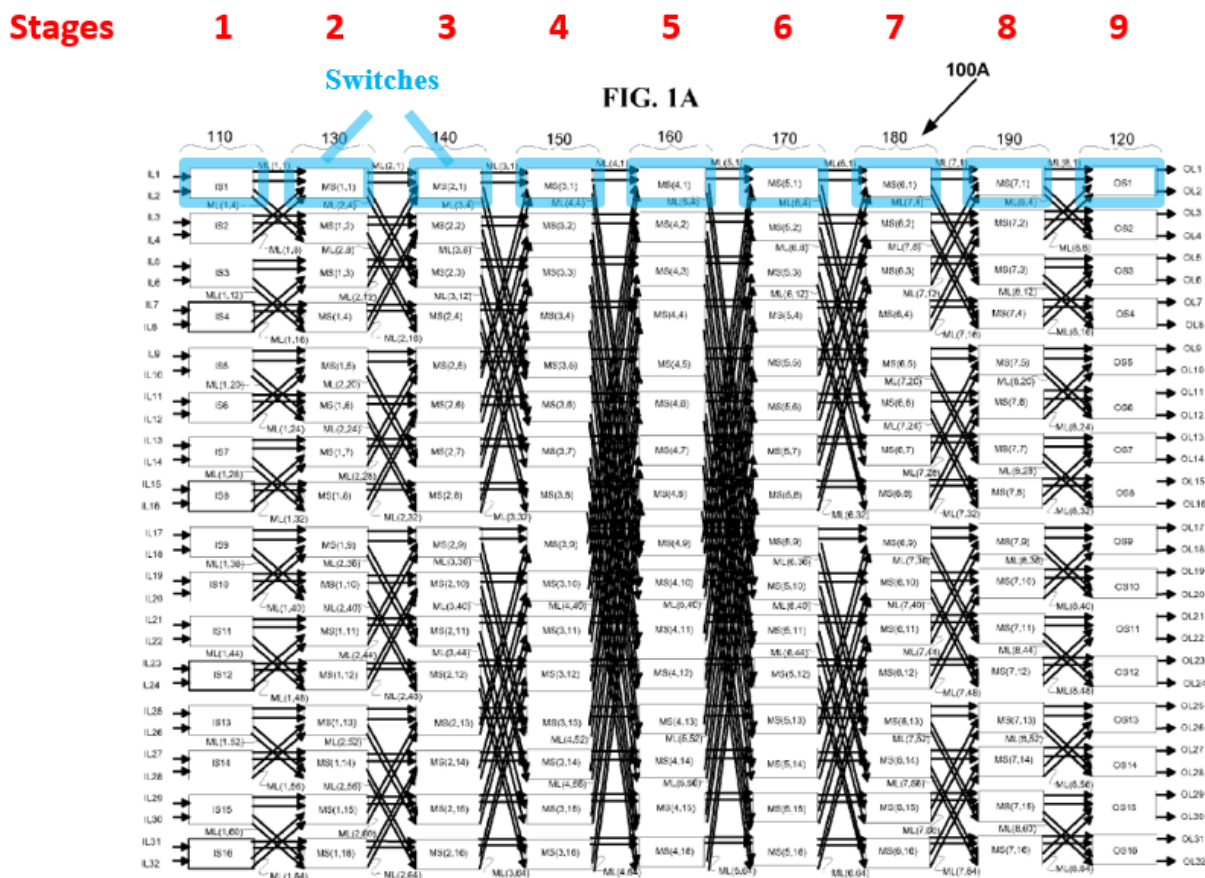
² Benes networks were originally developed by Vaclav E. Benes at Bell Labs in the mid-1960s. (*See, e.g.*, Ex. 1040 at Cover.)

wires, longer wires, with increased power consumption, increased latency of the signal which effect the maximum clock speed of operation.” (*Id.* at 3:1-6.)

33. Evidently in an attempt to address these issues, the '523 patent alleges to disclose “VLSI layouts of generalized multi-stage networks for broadcast, unicast and multicast connections [] using only horizontal and vertical links” where “[t]he VLSI layouts employ shuffle exchange links where outlet links of cross links from switches in a stage in one sub-integrated circuit block are connected to inlet links of switches in the succeeding stage in another sub-integrated circuit block so that said cross links are either vertical links or horizontal and vice versa.” (*Id.* at 3:21-29.) The '523 patent describes using such networks, which are made up of switches, “for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks.” (*Id.* at 8:44-50.)

34. For example, figure 1A of the '523 patent shows an exemplary 32x32 (32 inputs and 32 outputs) multi-stage network. (*Id.* at 8:44-50.) The multi-stage network includes a plurality of stages, where a stage corresponds to a column in the array of switches. The example network in figure 1A of the '523 patent includes nine stages, including an input stage 110 (left-most column) and output stage 120 (right-most column) with middle stages 130, 140, 150, 160, 170, 180, and 190

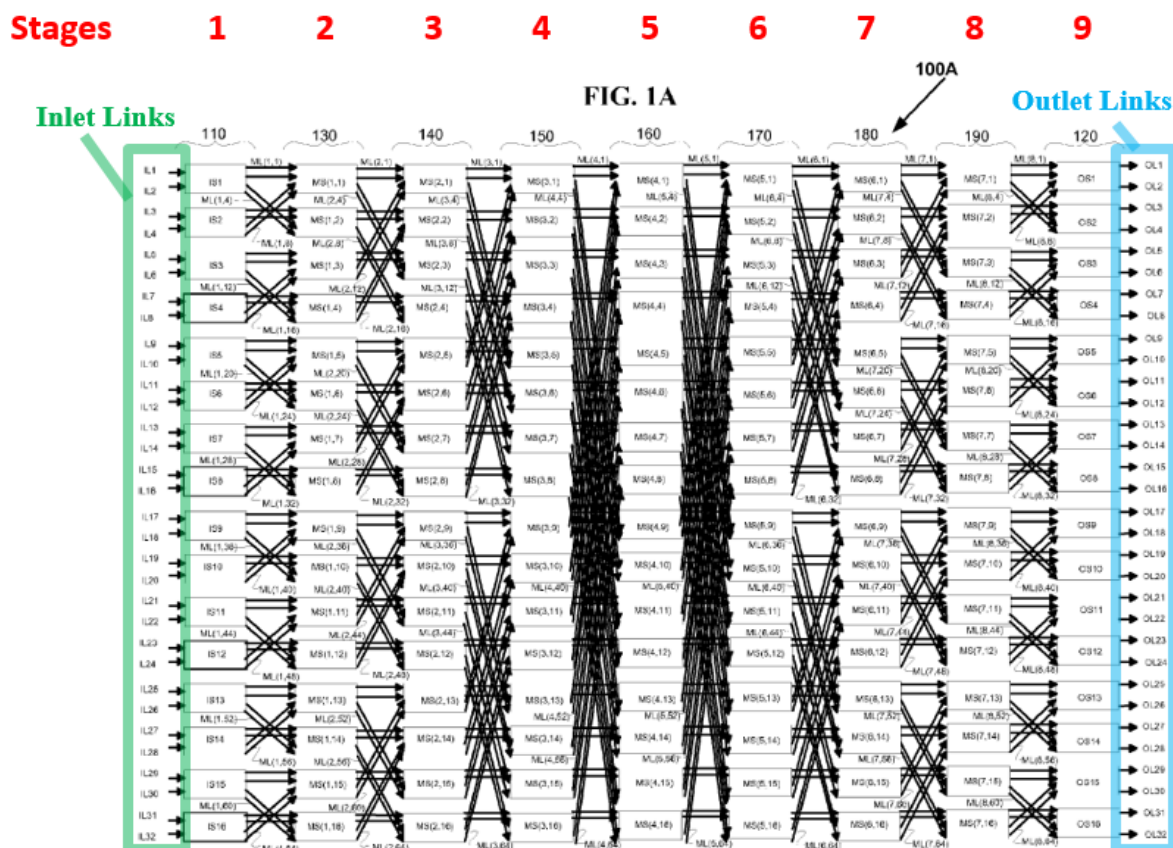
between the input stage 110 and the output stage 120. (*Id.* at 3:51-57, 8:44-52, FIG. 1A.)



(Ex. 1001 at FIG. 1A (annotated.))

35. The '523 patent describes the connection topology of the network 100A in figure 1A as “having inverse Benes connection topology of nine stages.” (*Id.* at 3:51-57.) Within the network 100A a number of “links” are provided that interconnect the switches. As highlighted in annotated figure 1A below, inlet links

IL1-IL32 provide inputs to the network and outlet links OL1-OL32 provide outputs from the network. (*Id.* at 9:3-12, FIG. 1A.)



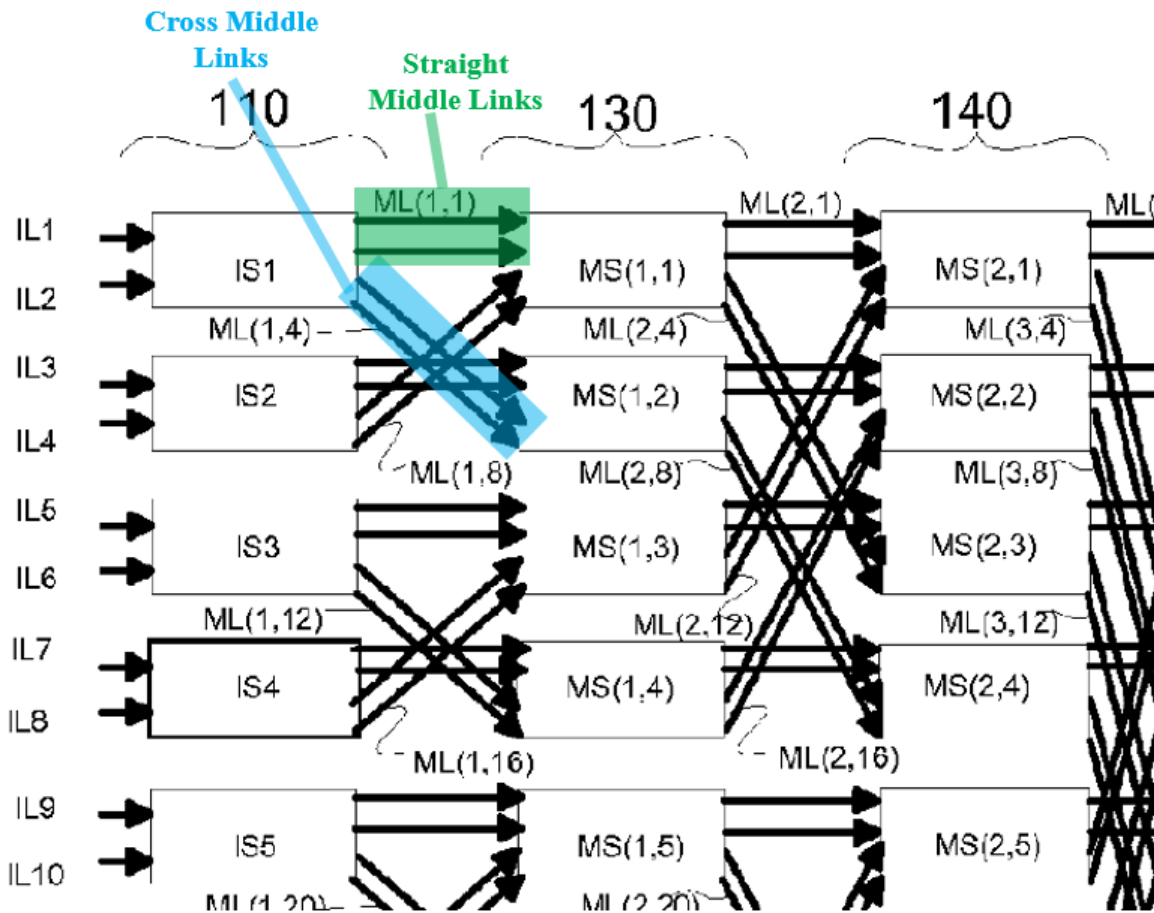
(*Id.* at FIG. 1A (annotated.))

36. In addition to the inlet and outlet links on the periphery of the network, the '523 patent also includes middle links that provide connections between the switches in the different stages of the network. According to the '523 patent, “[t]he middle links which connect switches in the same row in two successive middle stages are called hereinafter **straight middle links**; and the middle links which connect switches in different rows in two successive middle stages are called

hereinafter **cross middle links**.” (*Id.* at 9:45-49 (emphasis added).) Examples of such **straight middle links** and **cross middle links** are shown in the annotated excerpt of figure 1A below.

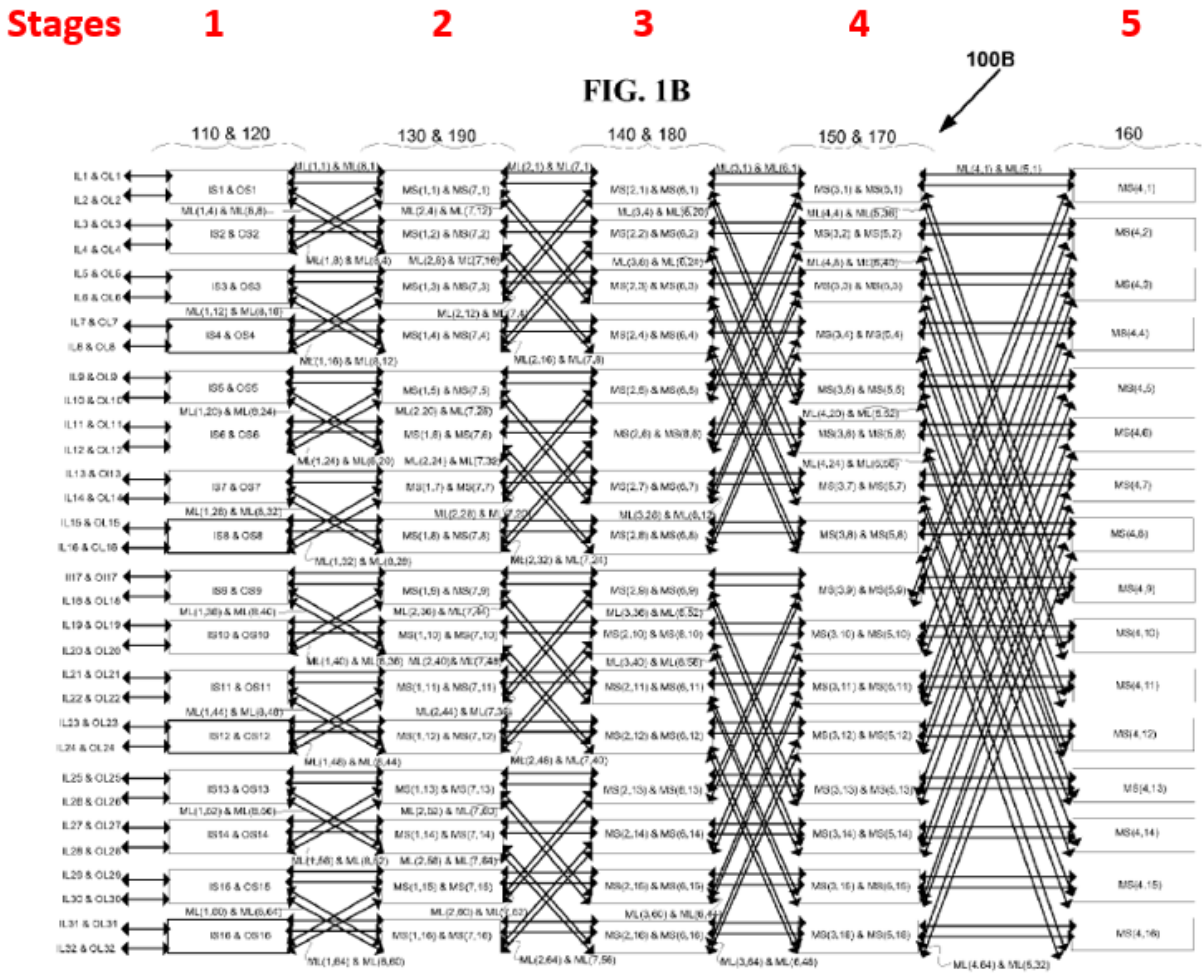
For example, the middle links ML(1,1) and ML(1,2) connect input switch IS1 and middle switch MS(1,1), so middle links ML(1,1) and ML(1,2) are straight middle links; where as the middle links ML(1,3) and ML(1,4) connect input switch IS1 and middle switch (MS1,2), since input switch IS1 and middle switch MS(1,2) belong to two different rows in diagram 100A of FIG. 1A, middle links ML(1,3) and ML(1,4) are cross middle links.

(*Id.* at 9:49-57; *see also id.* at 35:65-36:3.)



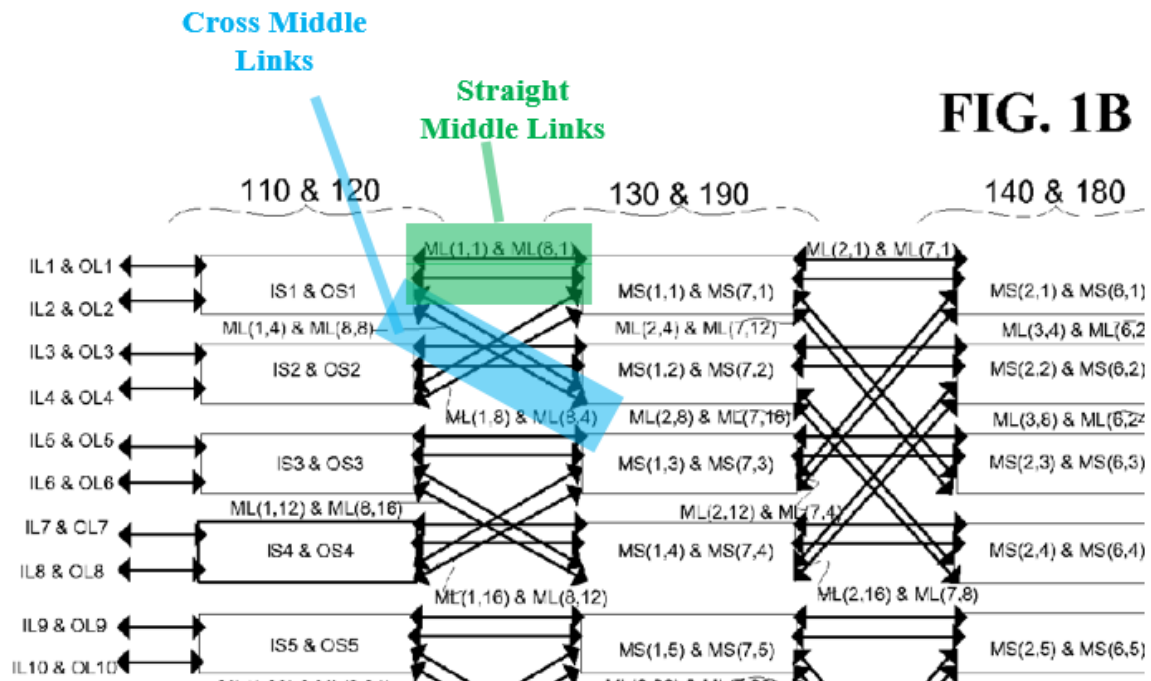
(*Id.* at FIG. 1A (excerpt, annotated).)

37. The '523 patent further describes folding the network 100A shown in figure 1A to form network 100B shown below in figure 1B. (*Id.* at 3:58-64, 12:6-8.) This is similar to the folding described above with respect to figures 4A-4C of *Wong*. (See my discussion in Section V.A above; Ex. 1008 at FIGs. 4A-4C, 6:51-7:22.) The network 100B in figure 1B has five stages, with the inputs and outputs of the network on the left-hand side of the figure. (*Id.* at 3:58-64, 12:6-53, FIG. 1B.)



(*Id.* at FIG. 1B (annotated).)

38. As can be seen in the annotated excerpt of figure 1B below, the folded network includes straight middle links and cross middle links.



(*Id.* at FIG. 1B (excerpt, annotated).)

VII. CLAIM CONSTRUCTION

39. I understand that claim terms are typically given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art, at the time of the alleged invention, which I understand is mid-to-late 2000s (including May 25, 2007, the filing date of the '394 provisional application to which the '523 patent claims priority). In considering the meaning of the claims, however, I understand that one must consider the language of the claims, the specification, and the prosecution history of record.

VIII. OVERVIEW OF THE PRIOR ART

A. *Wong*

40. *Wong* relates to an “interconnection network architecture which provides an interconnection network which is especially useful for FPGAs.” (Ex. 1008 at Abstract.) An example layout of an FPGA that includes *Wong*’s interconnection network architecture is shown in figure 13A below. (*Id.* at FIG. 13A, 13:12-16.) The FPGA layout includes switches 82 (annotated in green) and associated logic cells 81 (annotated in red). (*Id.* at FIG. 13A, 13:12-16.)

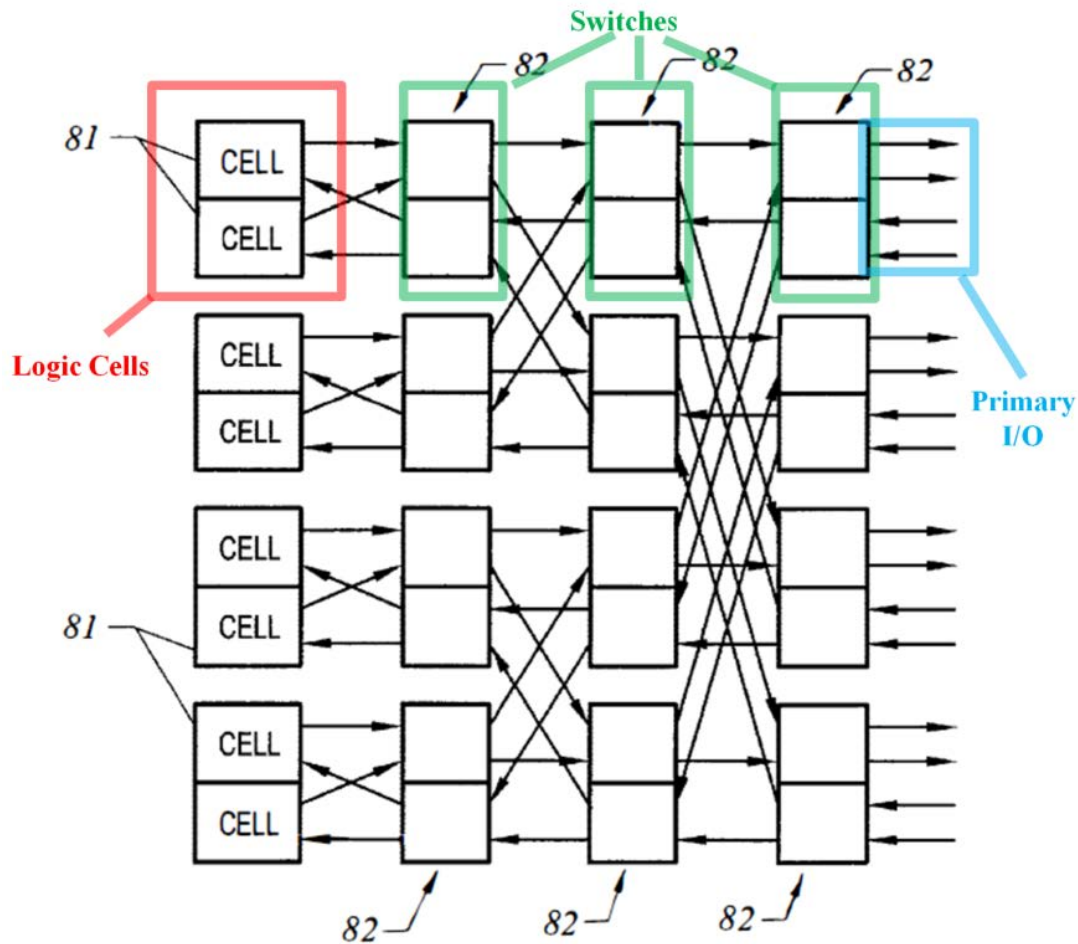


FIG. 13A

(*Id.* at FIG. 13A (annotated).)

41. The layout shown in figure 13A of *Wong* includes a single column with four rows of switches. The arrows on the right hand side of figure 13A (annotated in blue above) correspond to the top level connections between the network and primary input/output (I/O) of the FPGA. (*Id.* at 13:42-43.) A person of ordinary skill in the art would have understood that the signals provided to the FPGA that are processed by the logic blocks 81 are provided on the primary inputs of the FPGA.

Similarly, a person of ordinary skill in the art would have understood that the results generated by that processing are provided on the primary outputs of the FPGA.

42. The networks used in the FPGAs disclosed in *Wong* utilize links between switches in successive stages in the same row of switches (annotated in blue below) as well as links between switches in successive stages in different rows (annotated in green below).

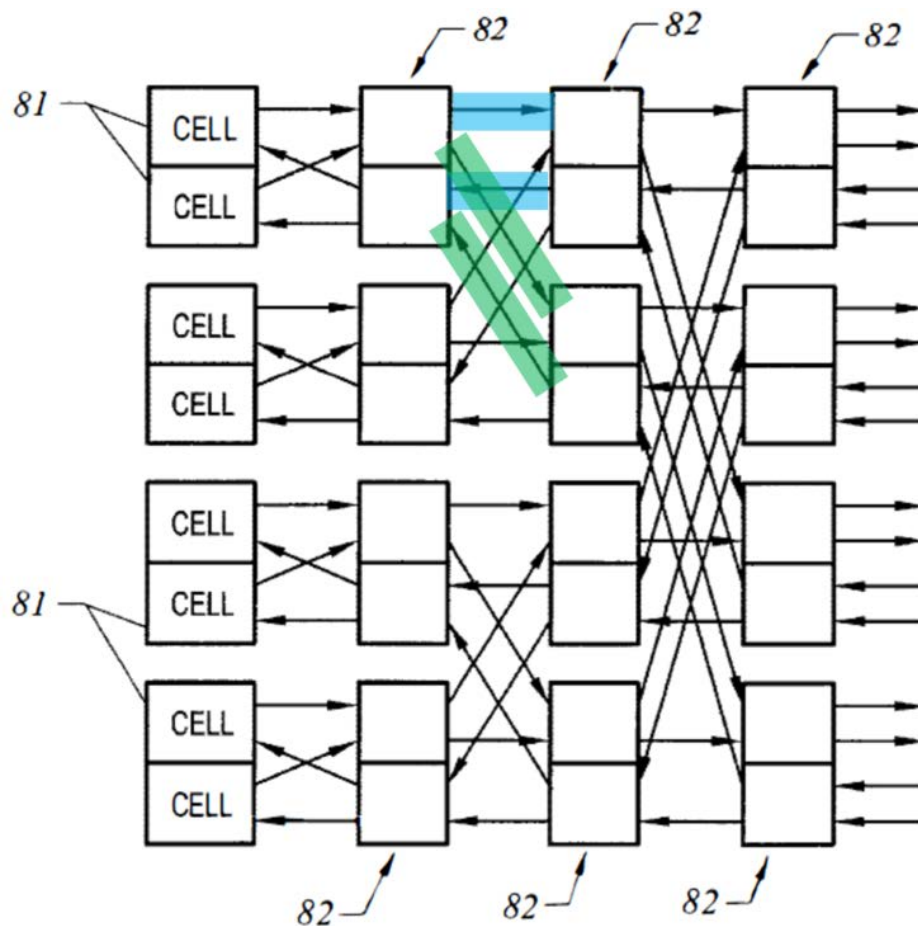
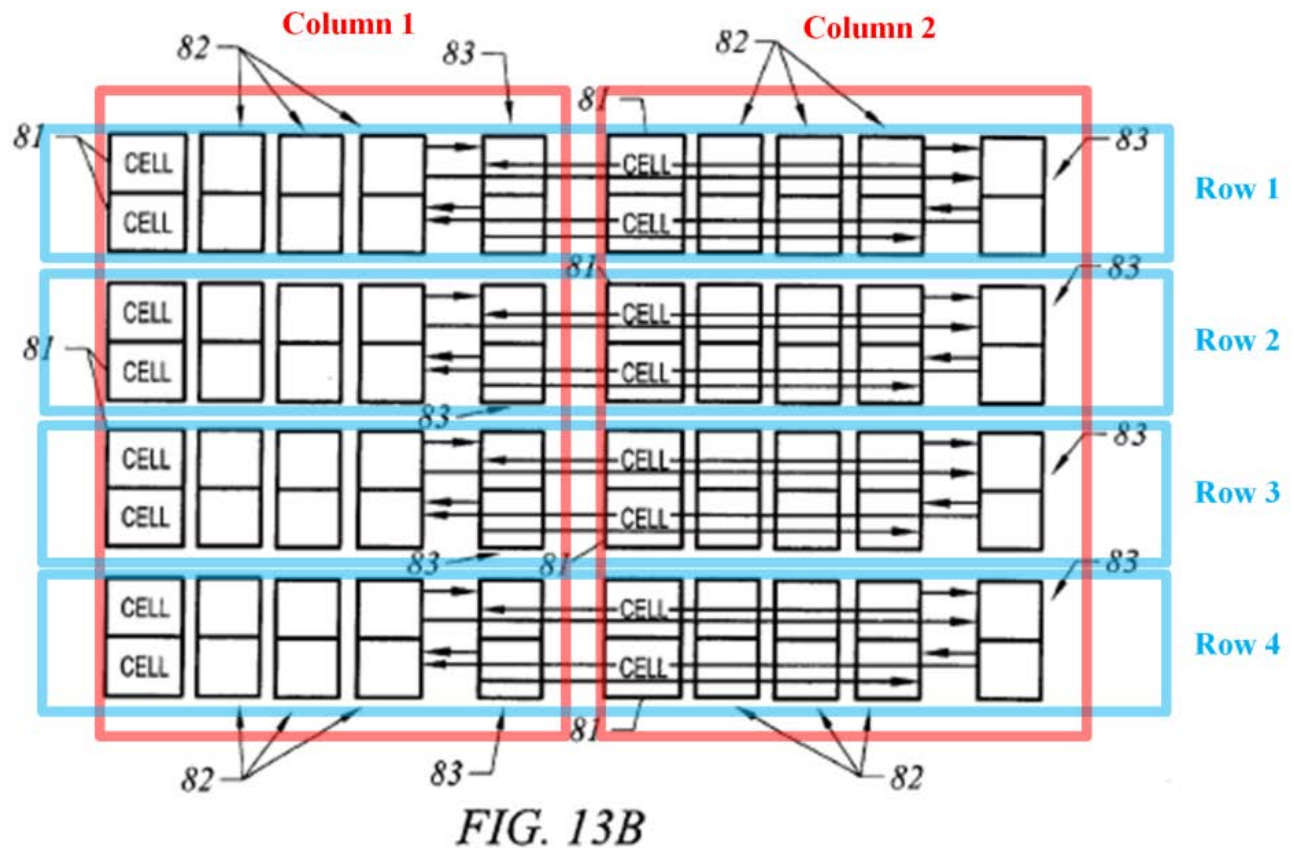


FIG. 13A

(*Id.* at FIG. 13A (annotated).)

43. *Wong* discloses that the single column network shown in figure 13A can be expanded to include multiple columns. (*Id.* at 13:33-42.) For example, figure 13B of *Wong* shows a network that includes two columns where each column includes four rows.

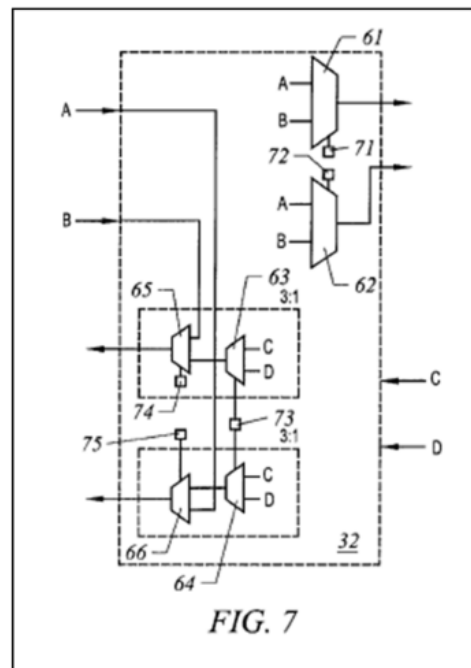
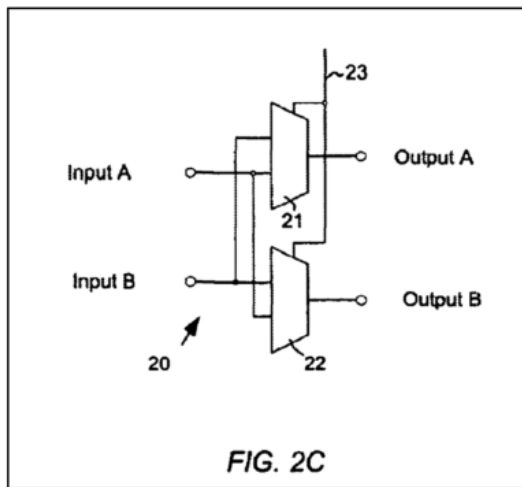


(*Id.* at FIG. 13B (annotated).)

44. According to *Wong*, “[t]he strength of this column floorplan is that the number of cells in a column can be any power of 2, and the number of rows can also independently be any power of 2,” which “enables the generation of arrays

containing numbers of cells that are any power of 2, and with a selection of various aspect ratios.” (*Id.* at 13:44-49.) In other words, the networks disclosed in *Wong* are expandable in both the row dimension and the column dimension, and various aspect ratios having different row:column ratios (number of rows vs. number of columns) are contemplated.

45. *Wong* also discloses example implementations of switches that can be used in the networks disclosed. For example, figure 2C shows an example 2x2 switch, and figure 7 shows an example 4x4 switch. (*Id.* at 2:29-30, 2:56-57, 5:14-29, 8:12-34, FIGs. 2C, 7.)



(*Id.* at FIGs. 2C, 7.)

IX. THE PRIOR ART DISCLOSES OR SUGGESTS ALL OF THE FEATURES OF CLAIMS 1, 15-18, 20-22, 32, AND 47 OF THE '523 PATENT

46. As I describe below at Sections IX.A-B, in my opinion, *Wong* discloses or suggests all of the features of claims 1, 15-18, 20-22, 32, and 47. As I describe below at Section IX.A, in my opinion *Wong* discloses all of the features of claims 1 and 20-22, and as I describe below at Section IX.B, *Wong* discloses or suggests all of the features of claims 15-18, 32, and 47.

A. *Wong* Discloses the Features of Claims 1 and 20-22

47. In my opinion, *Wong* discloses all of the features of claims 1 and 20-22 of the '523 patent. As discussed above in Section V.A, *Wong* discloses implementing a Benes network in an FPGA device. (*See* section V.A above.) Indeed, during prosecution, the Examiner rejected several pending claims, including pending claim 1, as anticipated by *Wong*. (Ex. 1004 at 92-99.) In response to the rejection, the applicant³ argued that “the current patent application discloses the VLSI layouts or floor plans of the Benes Network, Butterfly Fat Tree Networks including more generalizations of these networks” where “[t]he layout is critical to

³ I note that the applicant during prosecution of the '523 patent is the same as the Patent Owner in this IPR, namely, Venkat Konda.

implement these networks in a semiconductor chip which is typically a 2D-plane.” (*Id.* at 61.) Patent Owner did not contend during prosecution that the routing network described in the ’523 patent was new. Instead, Patent Owner argued during prosecution that the layout of the network was new:

As such **topologies of the Benes Network** and Butterfly Fat Tree networks **are known in the prior art and the topologies of the Benes Network** and Butterfly Fat Tree networks **disclosed in the current invention are the same as in the prior art.** However the layouts of these networks are novel.

(*Id.* at 61 (emphasis added).)

48. A person of ordinary skill in the art reading such statements by Patent Owner during prosecution of the ’523 patent would have understood Patent Owner to have conceded that there is nothing new with respect to the network topology presented, and instead, the only novel features disclosed are those related to how the network is laid out on the semiconductor chip.

49. The ’523 patent itself acknowledges that *Wong*, like the ’523 patent, discloses a Benes network. (Ex. 1001 at 2:56-61, 3:51-64.) In arguing against the rejection based on *Wong* during prosecution, Patent Owner listed a number of alleged differences between *Wong*’s disclosure and that of the ’523 patent. (Ex.

1004 at 62-65.) Some of those alleged differences are not represented in the claims, and therefore I do not address them. With respect to possibly relevant alleged differences identified by Patent Owner during prosecution, which are related to the layout of the network, the arguments that were presented focus heavily on a tree-based layout disclosed in figure 14C of *Wong*. However, those arguments ignore figure 14A of *Wong*, which shows a row-column layout similar to that of the '523 patent. (*Id.* at 65.) Moreover, Patent Owner's arguments during prosecution mischaracterized the column-based layout disclosed in *Wong*. As discussed in more detail below, contrary to the applicant's allegations during prosecution, the column-based layout of *Wong* includes sub-integrated circuit blocks arrayed in rows and columns in the same manner as the network disclosed and claimed in the '523 patent.

1. Claim 1

a) "An integrated circuit device comprising"

50. I understand that "[a]n integrated circuit device comprising" is the preamble of claim 1, and I have been asked to assume that the preamble is a limitation of the claim. Under that assumption, it is my opinion that *Wong* discloses an integrated circuit device. For instance, *Wong* discloses an FPGA (field-programmable gate array) integrated circuit ("an integrated circuit device"). (*See* above at Section V.A. for an overview of FPGAs.) For example, *Wong* discloses

that “[t]he present invention relates to integrated circuit interconnections and, in particular, to the interconnection architecture of FPGA (Field Programmable Gate Array) integrated circuits.” (Ex. 1008 at 1:14-17.) Claim 18 of the ’523 patent recites that “said integrated circuit device is a field programmable gate array (FPGA) device or field programmable gate array (FPGA) block embedded in another integrated circuit device” (Ex. 1001 at 37:67-38:3), thereby confirming that the FPGA disclosed by *Wong* is an integrated circuit device as recited in claim 1 of the ’523 patent.

51. *Wong* also discloses that “FPGAs are integrated circuits whose functionalities are designated by the users of the FPGA” where the “user programs the FPGA (hence the term, ‘field programmable’) to perform the functions desired by the user.” (Ex. 1008 at 1:18-21.) *Wong* discloses FPGAs that include “an integrated circuit having a plurality of logic cells; and a programmable network interconnecting the logic cells.” (*Id.* at 1:59-61).

52. Figures 13A and 13B of *Wong* illustrate exemplary floorplan layouts of FPGAs (“integrated circuit devices”). (*Id.* at 3:7-10; 13:19-22, 13:36-38, FIGs. 13A, 13B.)

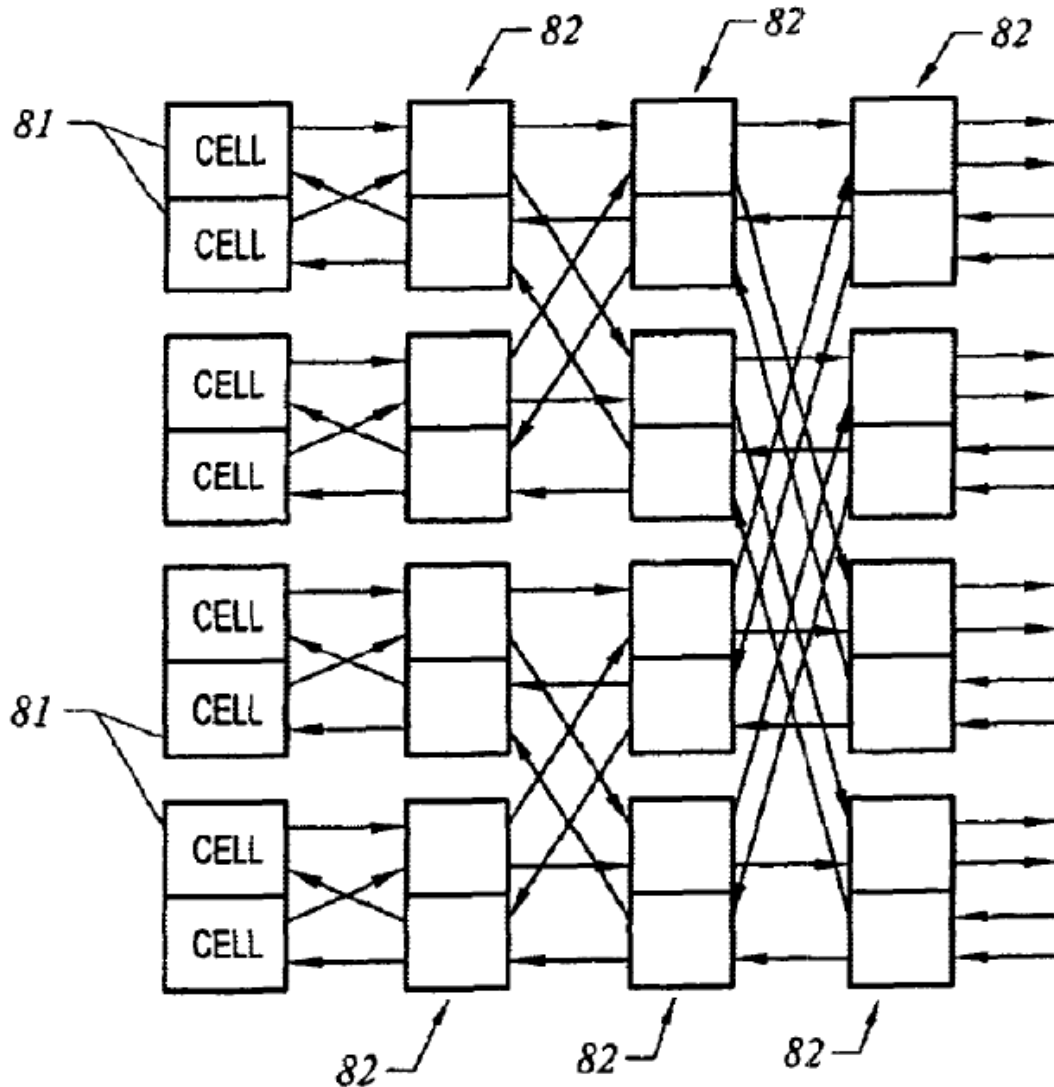
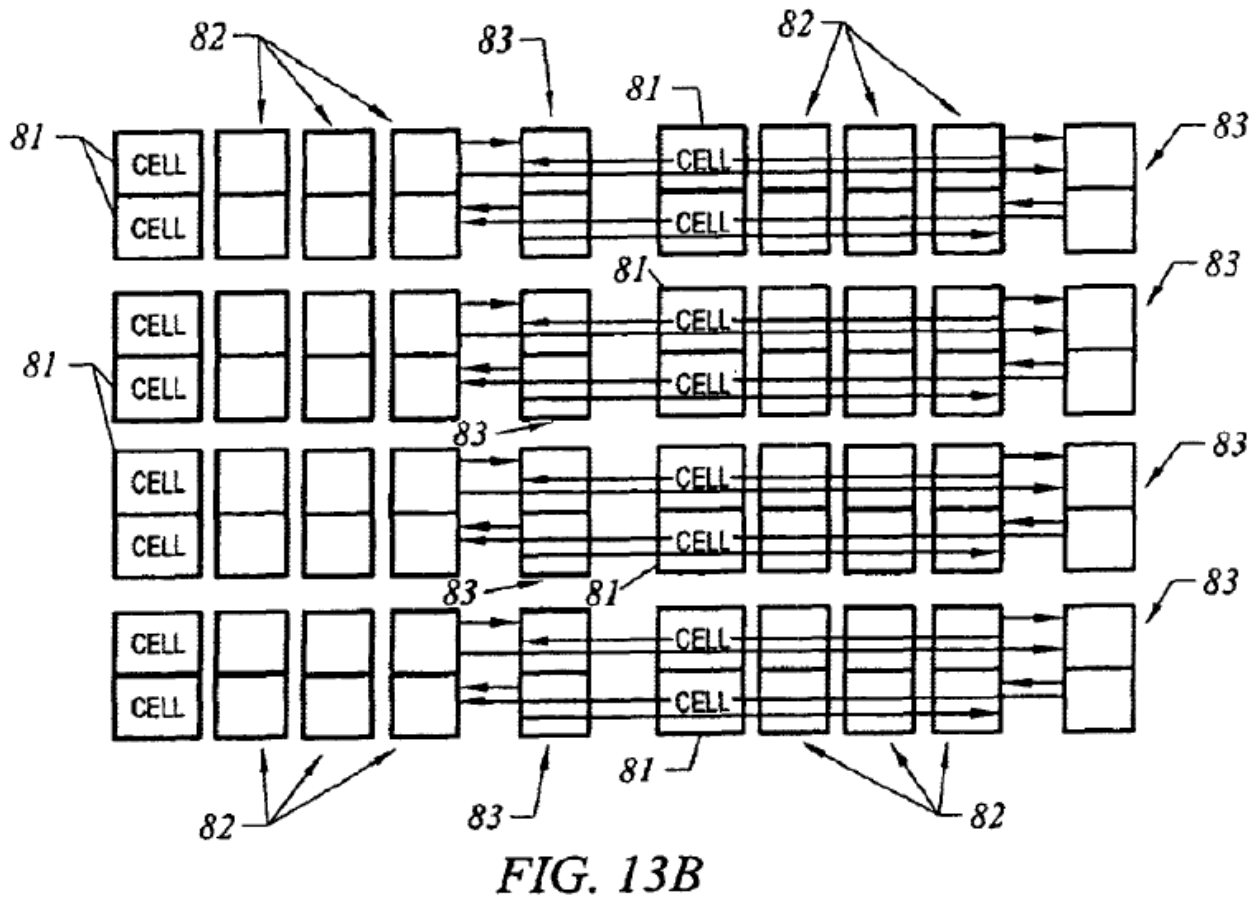


FIG. 13A

(Ex. 1008 at FIG. 13A.)



(Ex. 1008 at FIG. 13B.)

b) “a plurality of sub-integrated circuit blocks and a routing network, and”

53. In my opinion, *Wong* discloses this feature. For instance, *Wong* discloses an integrated circuit (e.g. an FPGA) that includes a plurality of logic cells that are coupled to a programmable network. (Ex. 1008 at 1:59-61 (“The present invention provides for an integrated circuit having a plurality of logic cells; and a programmable network interconnecting the logic cells.”).)

54. A person of ordinary skill in the art would have understood that a “sub-integrated circuit block” in the context of the ’523 patent corresponds to a row of switches in a network such as that illustrated in figure 1B in addition to the configurable logic that is coupled to that row. (Ex. 1001 at 15:22-24 (“Some of the key aspects of the current invention are discussed. 1) All the switches in one row of the multi-stage network 100B are implemented in a single block.”), 13:38-42.) For example, with respect to figure 1C of the ’523 patent, which shows the “blocks” (i.e. sub-integrated circuit blocks) of figure 1B, the ’523 patent states that:

Even though it is not illustrated in layout 100C of FIG. 1C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit (hereinafter ‘sub-integrated circuit block.’) depending on the applications in different embodiments.

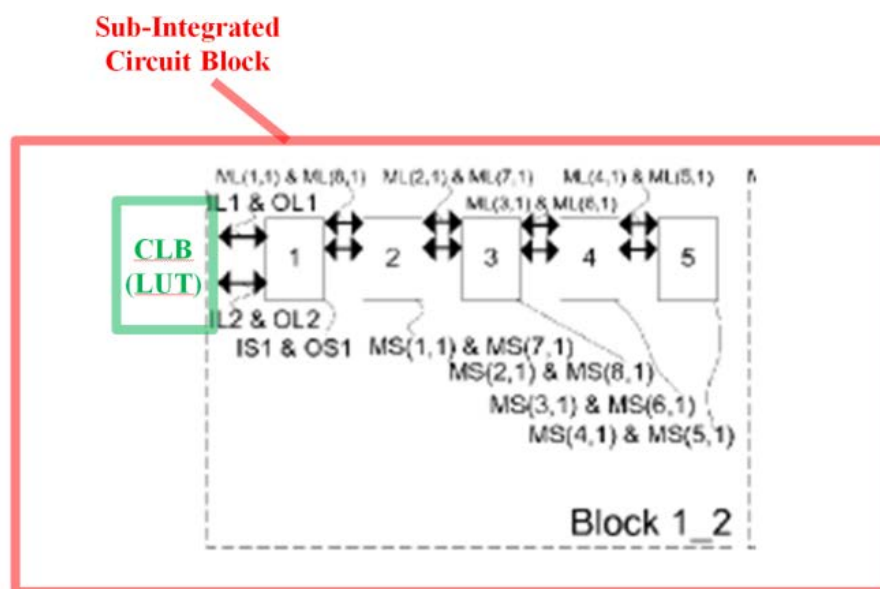
(Ex. 1001 at 13:38-42.)

55. Therefore, in the context of the ’523 patent a “sub-integrated circuit block” includes the switches corresponding to a single row (which figure 1C of the ’523 patent shows as a single “block”) with the addition of “Configurable Logic

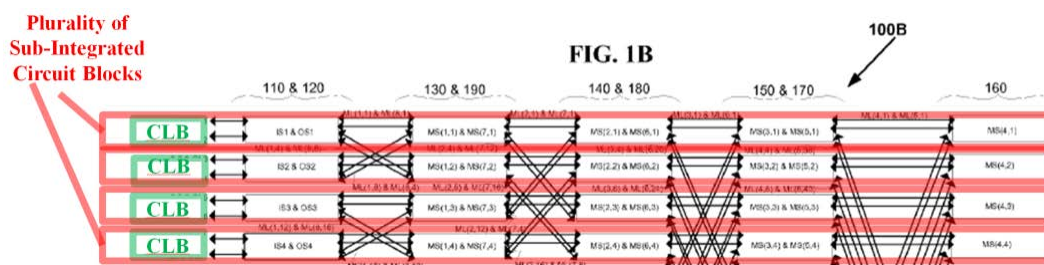
Blocks (CLB) or any arbitrary digital circuit.”⁴ I have created the demonstratives below to illustrate a “sub-integrated circuit block” in figures 1B and 1C of the ’523 patent in the context of how a person of ordinary skill in the art would have

⁴ Claim 18 of the ’523 patent states “wherein said sub-integrated circuit blocks are Lookup Tables (hereinafter ‘LUTs’).” Based on the disclosure of the ’523 patent, a person of ordinary skill in the art would have understood that a lookup table constitutes a “Configurable Logic Block[] (CLB) or any arbitrary digital circuit” that would be included in a “sub-integrated circuit block” in the context of claim 1 of the ’523 patent. Claim 18’s statement that the “sub-integrated circuit blocks are Lookup Tables” does not comport with the other features recited in claim 1, which require the sub-integrated circuit blocks to include forward and backward connecting links. Therefore, the sub-integrated circuit blocks must include more than simply the lookup tables, as a person of ordinary skill in the art would not have understood the recited links to be part of the lookup tables themselves. Instead, the links would have been understood to be between the switches in the network, and therefore part of each block. While claim 18 does not make sense in this regard, it does provide support for the understanding that lookup tables constitute “Configurable Logic Blocks (CLB) or any arbitrary digital circuit[s].”

understood claim 1. As is apparent from the discussion below, such an understanding of a “sub-integrated circuit block” is consistent with the other claim limitations. (See my discussion below in Sections IX.A.1(c)-(k).)



(Ex. 1001 at FIG. 1C (excerpt, annotated).)



(Ex. 1001 at FIG. 1B (excerpt, annotated).)

56. In the annotated excerpts of figures 1B and 1C above, each “sub-integrated circuit block” (outlined in a red box) includes all of the switches in a row, which the ’523 patent refers to as a “block.” In addition to the switches in the block,

the sub-integrated circuit block also includes a “Configurable Logic Block[] (CLB) or any arbitrary digital circuit,” which is represented by a green “CLB” box.

57. In my opinion, *Wong* discloses a plurality of “sub-integrated circuit blocks” as recited in claim 1. The folded network shown in figure 4C of *Wong* below is similar to the folded network shown in figure 1B of the '523 patent.

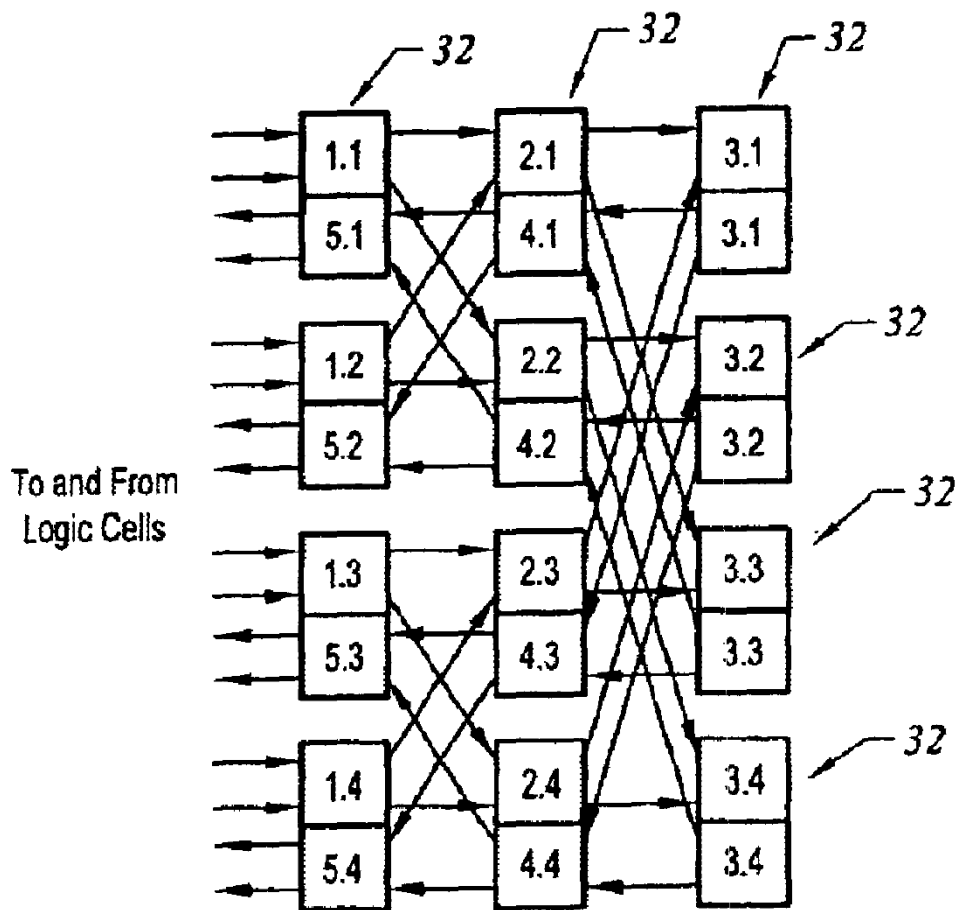
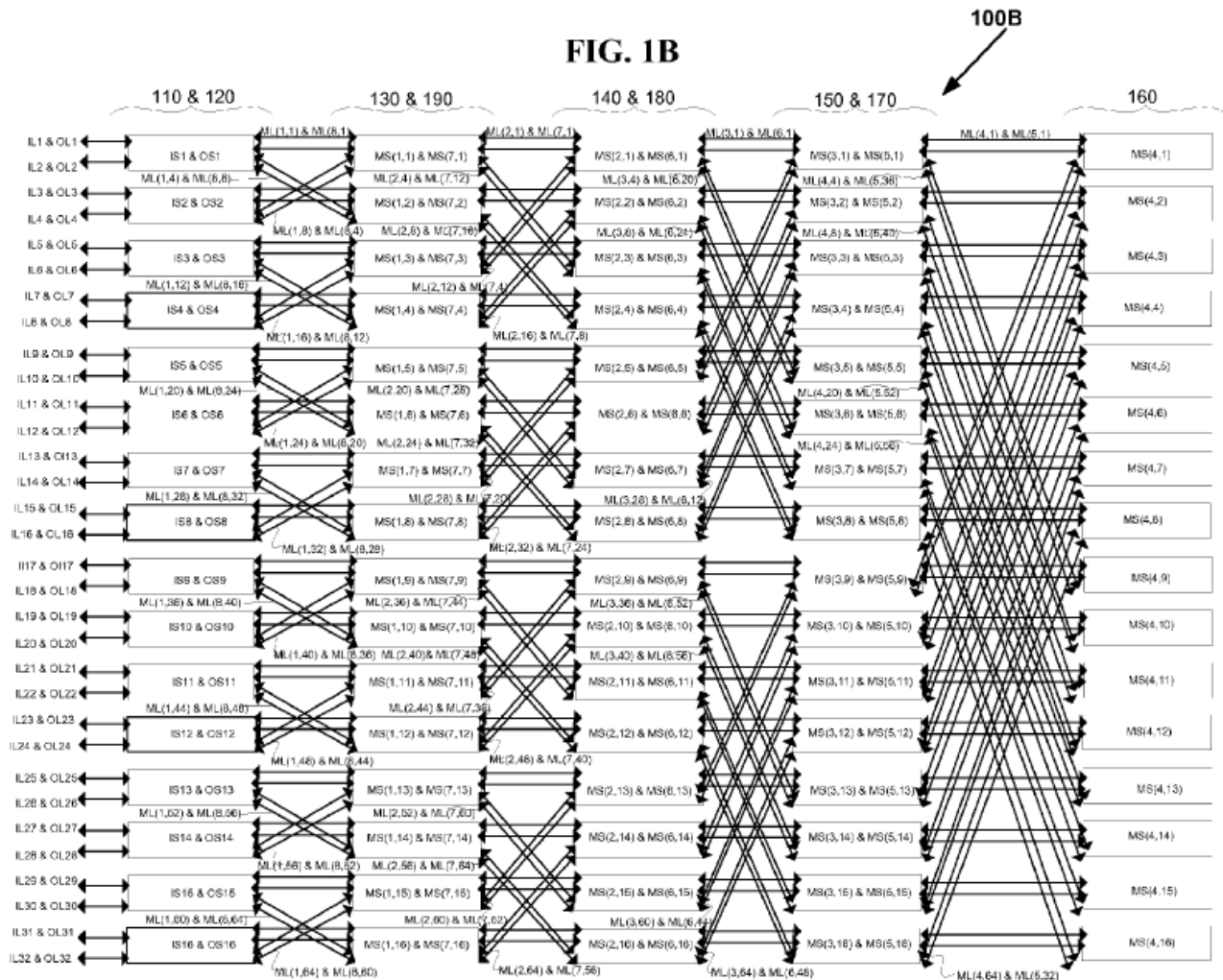


FIG. 4C

(Ex. 1008 at FIG. 4C.)



(Ex. 1001 at FIG. 1B.)

58. Figures 13A and 13B of *Wong* illustrate exemplary floorplan layouts of FPGAs that use a Benes network topology such as that shown in figure 4C. (Ex. 1008 at 3:7-10, 13:19-22 (“With the previous illustrations of the Benes interconnect network and columns of logic cells added, the layout is nearly completed. See FIG. 13A.”), FIG. 13A (reproduced below).) Thus, figure 13A of *Wong* illustrates the network of figure 4C of *Wong* with the addition of logic cells 81.

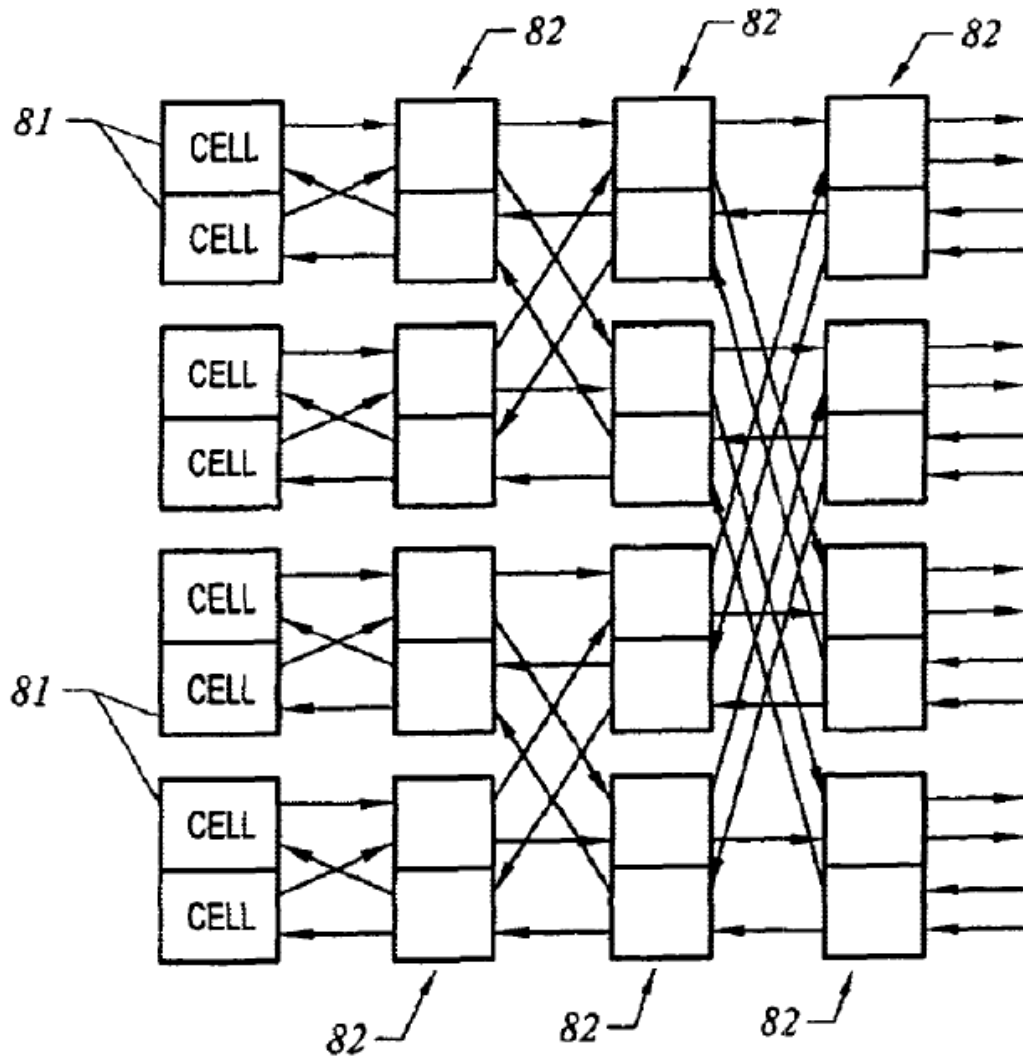


FIG. 13A

(Ex. 1008 at FIG. 13A.)

59. As shown in figure 13A of *Wong*, each row includes a plurality of switches 82 and a pair of logic cells 81. Similarly, figure 13B shows a multi-column embodiment that includes two instantiations of the layout shown in figure 13A. (Ex.

1008 at 3:7-10; 13:36-38.) In each of the two columns shown in figure 13B, each row includes a plurality of switches 82, 83 and a pair of logic cells 81.

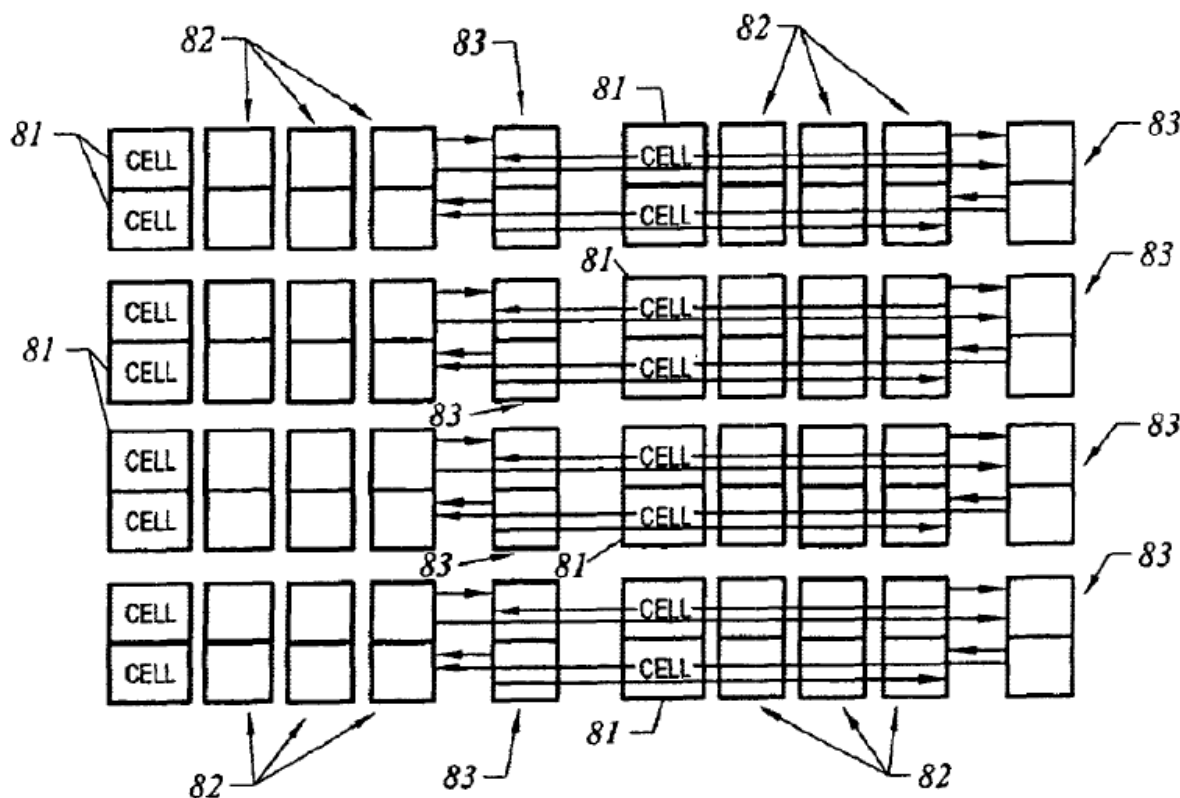


FIG. 13B

(Ex. 1008 at FIG. 13B.)

60. As depicted in figures 13A and 13B, logic cells 81 are included in the FPGA along with switch cells 82 and 83, where the switch cells make up the “routing network” that provides the interconnect in the FPGA. (Ex. 1008 at 13:22-23 (“There are two logic cells 81 per switch cell 82....”), 13:36-38 (“See FIG. 13B in which a level of switch cells 83 are added to make the connection between two FIG. 13A column arrays.”).) *Wong* discloses that the logic cells are configurable and can be

programmed to perform desired functions. (Ex. 1008 at 3:22-24 (“... logic cells 10, which implement the desired circuit logic by the user”), 7:34-38, (“Note that ‘placement’ for an FPGA logic cell is not the physical placement of selected logic gates to form a desired function, but rather the programming of a selected logic cell to perform the desired function.”).)

61. *Wong* discloses that each of the logic cells shown in figure 13A can be implemented as a “4-input, 1-output Look Up Table” (“LUT”). (Ex. 1008 at 13:28-32 (For example, if the logic cell is a 4-input, 1-output Look Up Table (see FIG. 9), the single output pin is fanned out 4 times to form 4 pin-pairs for each cell, and there are 2 switch cells in the first level of the Benes network connecting to each logic cell”), 8:51 (“Each logic cell is a 4-LUT (4 input Look Up Table).”), 9:9-12 (“For the purpose of analysis, assuming the logic cell is a 4-LUT (4-input Look-Up Table) with a latched output and the array is built with 16K logic cells (a 64K gate equivalent)”).) A person of ordinary skill in the art would have recognized that the output of a lookup table for different sets of inputs can be programmed, thereby allowing a wide variety of logic functions to be implemented by programming the entries in the lookup table. A person of ordinary skill in the art would have understood that a lookup table constitutes a “Configurable Logic Block[] (CLB) or

any arbitrary digital circuit” included in a “sub-integrated circuit block” in the context of the ’523 patent. (Ex. 1001 at 37:65-67 (claim 18).)

62. *Wong* also discloses that “while logic cells are interconnected in an FPGA, the interconnection network of the present invention may be used to interconnect arbitrary components, such as multiple processors or peripheral blocks, of an integrated circuit.” (Ex. 1008 at 14:44-48.) A person of ordinary skill in the art would have understood that “arbitrary components, such as multiple processors or peripheral blocks” would correspond to a “Configurable Logic Block[] (CLB) or any arbitrary digital circuit” included in a “sub-integrated circuit block” in the context of claim 1 of the ’523 patent.

63. Therefore, in my opinion, that *Wong* discloses “a plurality of sub-integrated circuit blocks and a routing network” as recited in claim element 1(b). *Wong* discloses a plurality of rows of switches and their corresponding logic cells (“plurality of sub-integrated circuit blocks”), where the switches provide the desired interconnect for the network (“routing network”) in the FPGA (“integrated circuit device”). I have annotated figures 13A and 13B below to show the plurality of sub-integrated circuit blocks and corresponding routing networks.

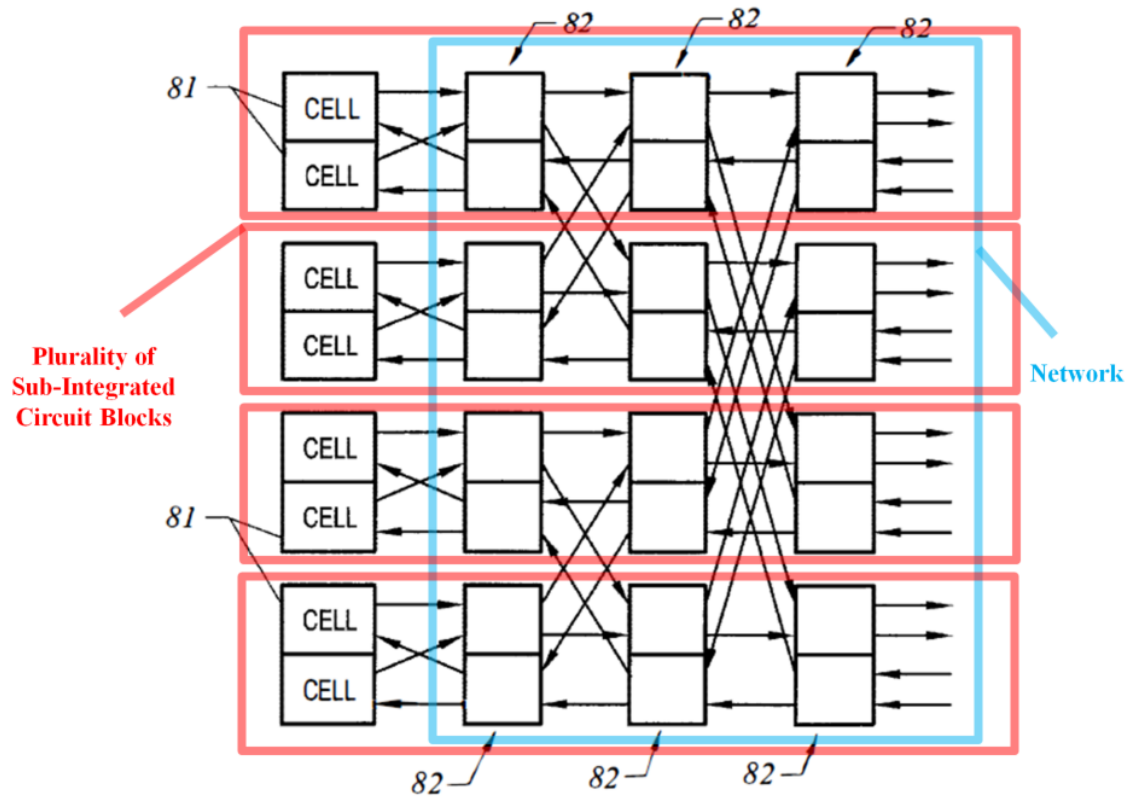
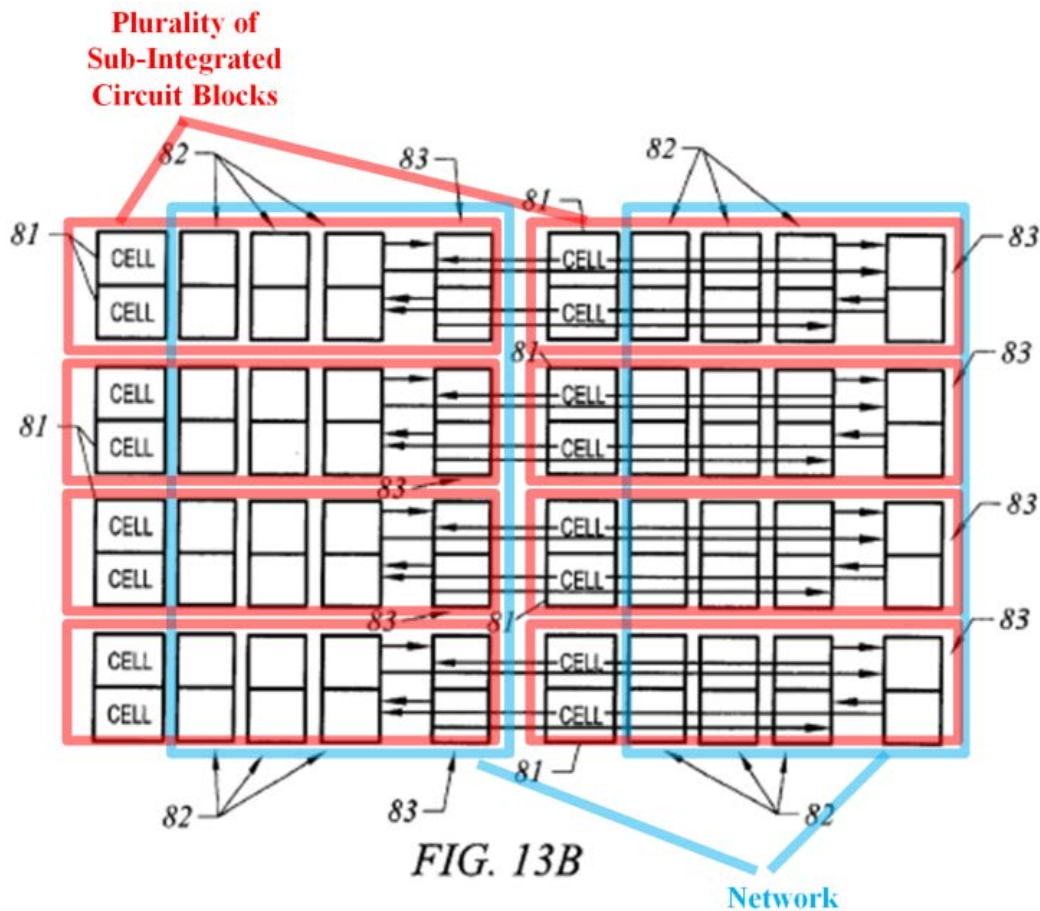


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated).)



(Ex. 1008 at FIG. 13B (annotated).)

- c) “Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links; and”

64. In my opinion, *Wong* discloses this feature. Specifically, *Wong* discloses that the logic cells 81 included in the “sub-integrated circuit blocks” include output pins (“plurality of outlet links”), which are coupled to inputs of the switches 82 in the first stage of the network. The logic cells 81 also include input pins (“plurality of inlet links”) that are coupled to outputs of the switches 82 in the

first stage of the network inputs. As I discussed above, those logic cells can be lookup tables that would have inputs that are decoded to determine the outputs. (See my discussion above in Section IX.A.1(b).)

65. For example, as shown in figure 13A of *Wong* (annotated below), each of the two logic cells in each of the “sub-integrated circuit blocks” includes an output pin (“plurality of outlet links”) that is coupled to an input of one of the switches 82 in the first stage of the network. (Ex. 1008 at FIG. 13A, 13:24-26.)

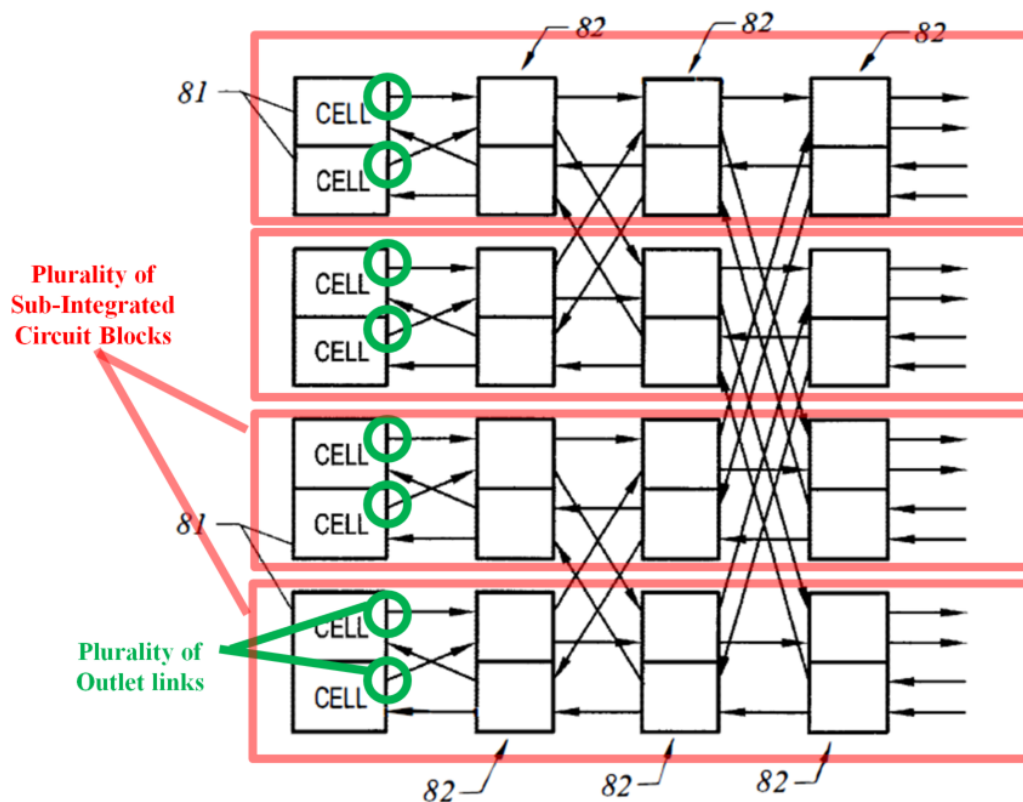


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated to show plurality of outlet links for each sub-integrated circuit block).)

66. Each of the two logic cells in each sub-integrated circuit block also includes an input pin (“plurality of inlet links”) that is coupled to an output of one of the switches 82 in the first stage of the network. (Ex. 1008 at FIG. 13A, 13:24-26.)

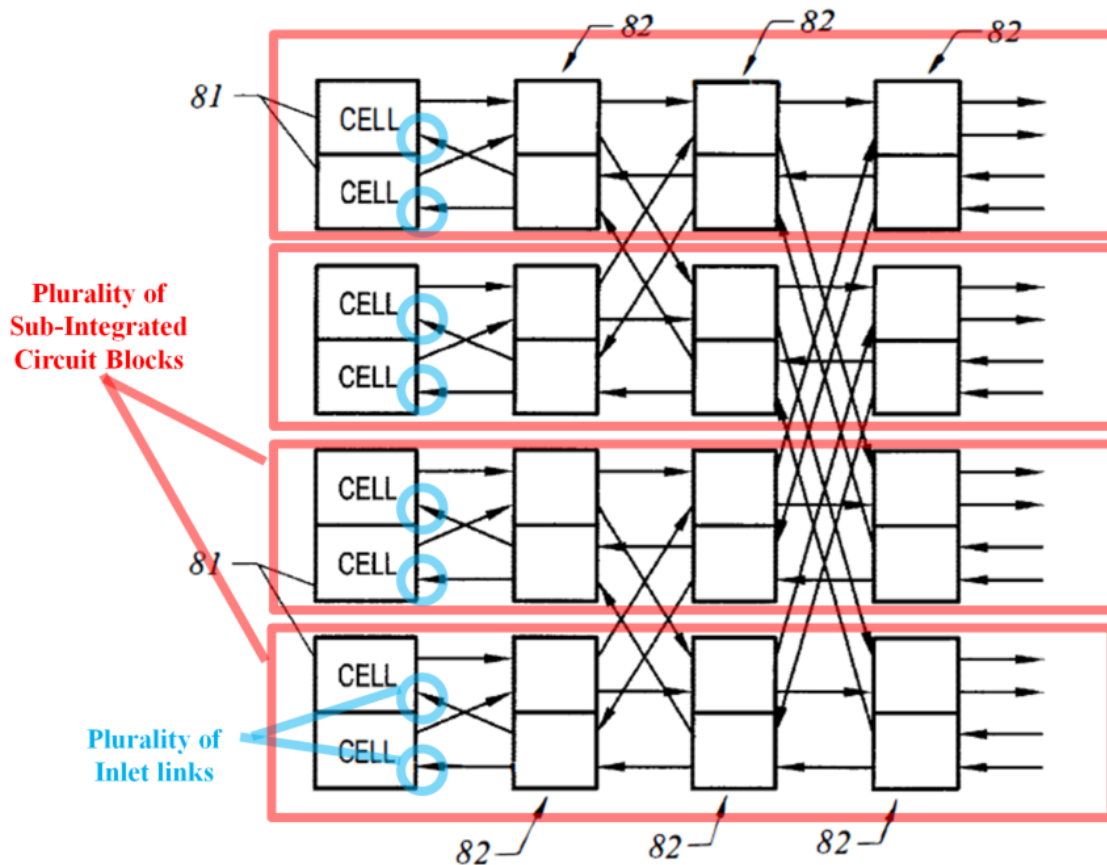
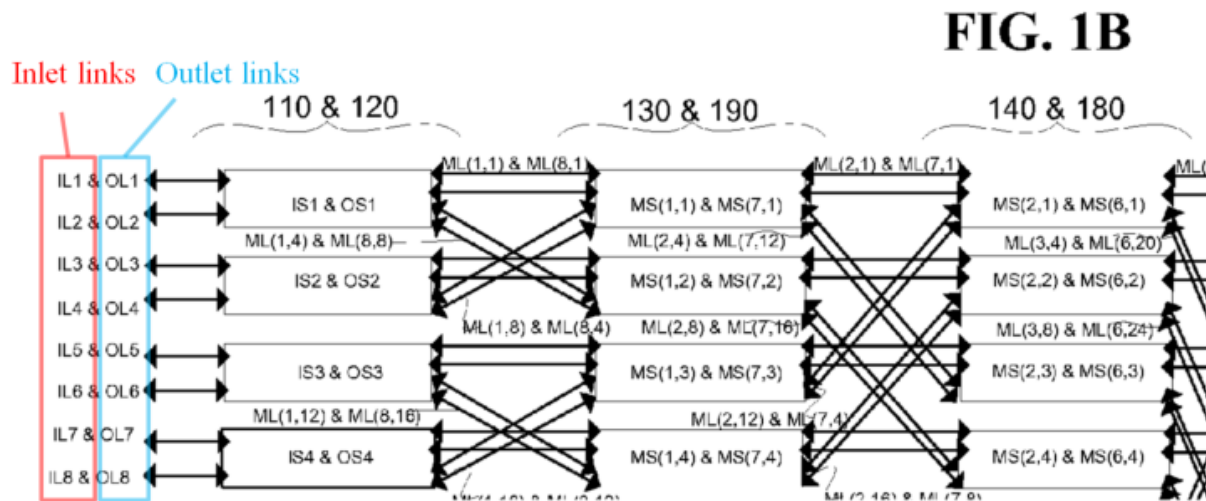


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated to show plurality of inlet links for each sub-integrated circuit block).)

67. Because figure 13B of *Wong* includes two instantiations of the layout shown in figure 13A of *Wong*, figure 13B also discloses the claimed “inlet links”

and “outlet links” in the same manner described with respect to figure 13A. (Ex. 1008 at 13:36-38.) The inlet links and outlet links shown in figure 13A of *Wong* above correspond to inlet links and outlet links included in embodiments in the ’523 patent. Examples of such inlet links and outlet links are illustrated in an excerpt from figure 1B of the ’523 patent annotated below.



(Ex. 1001 at FIG. 1B (excerpt, annotated to show inlet links and outlet links).)

68. Specifically, the figure 1B excerpt above shows inlet links (IL1, IL2, ... IL8) and outlet links (OL1, OL2, ... OL8), where, for example, the inlet links IL1 and IL2 correspond to the inputs of switch IS1 & OS1, and outlet links OL1 and OL2 correspond to the outputs of switch IS1 & OS1. (Ex. 1001 at 12:6-19.) As described by the ’523 patent, the network shown in figure 1B is a folded version of the network shown in figure 1A, which can set up a connection between

“configurable logic blocks, between an input stage 110 and an output stage 120 via middle stages 130, 140, 150, 160, 170, 180 and 190” (*Id.* at 8:44-52, 12:6-8.) A person of ordinary skill in the art would have understood that the inlet links (IL1, IL2, ... IL8) and outlet links (OL1, OL2, ... OL8) provide connections between the configurable logic blocks and the first stage of switches in the '523 patent in the same manner that the inlet links and outlet links shown above in *Wong* connect the logic cells with the first stage of switches in *Wong*'s network.

d) “Said routing network comprising of a plurality of stages y , in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y , where $y \geq 1$; and,”

69. In my opinion, *Wong* discloses this feature. For example, within the routing network of figure 13A of *Wong*, each sub-integrated circuit block includes three stages (each switch 82 corresponds to a “stage”), and therefore *Wong* discloses the “routing network comprising of a plurality of stages y , in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y , where $y \geq 1$.”

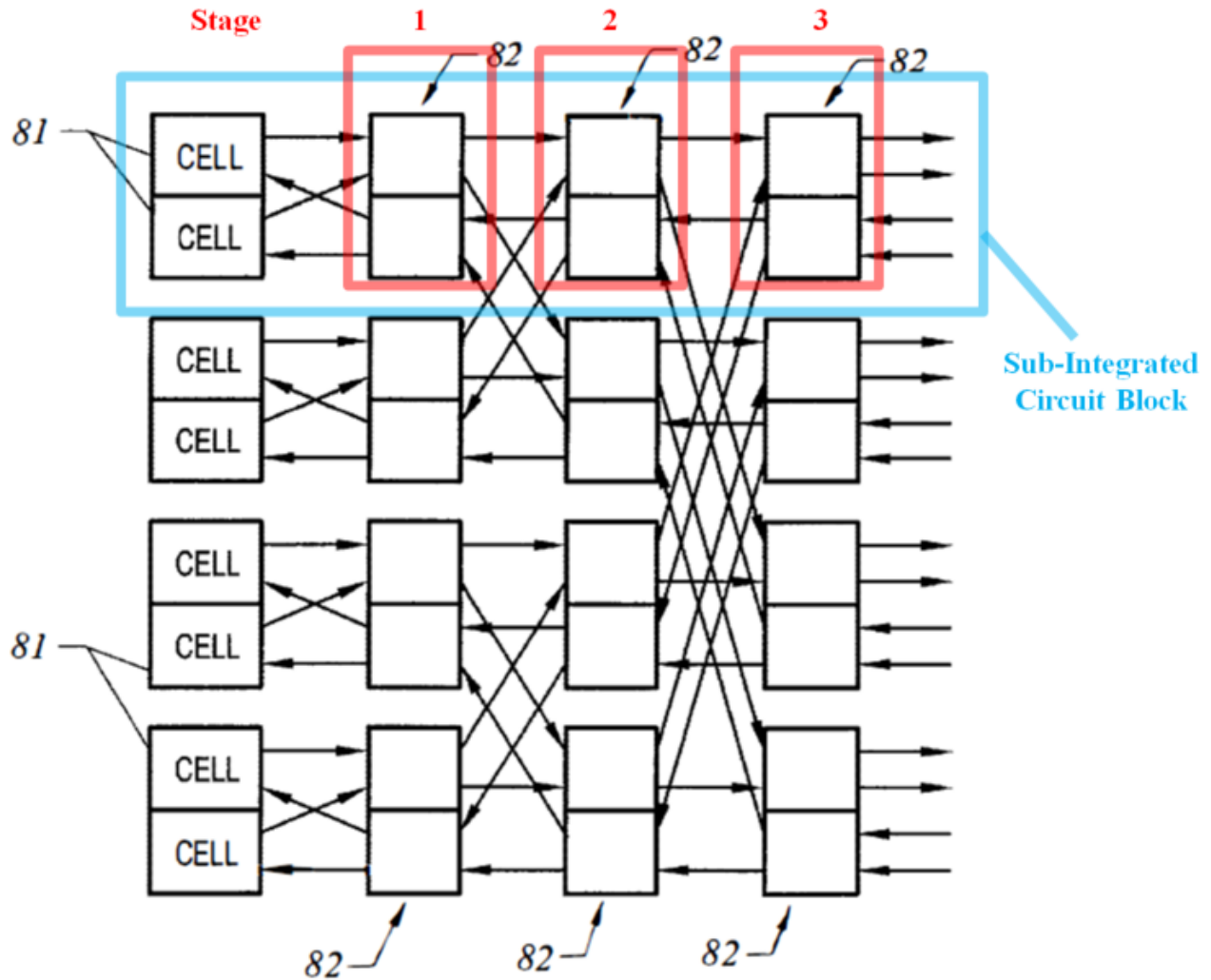


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated).)

70. Similarly, as shown in figure 13B of *Wong* (annotated below), each sub-integrated circuit block includes four stages (each switch 82, 83 corresponds to a “stage”).

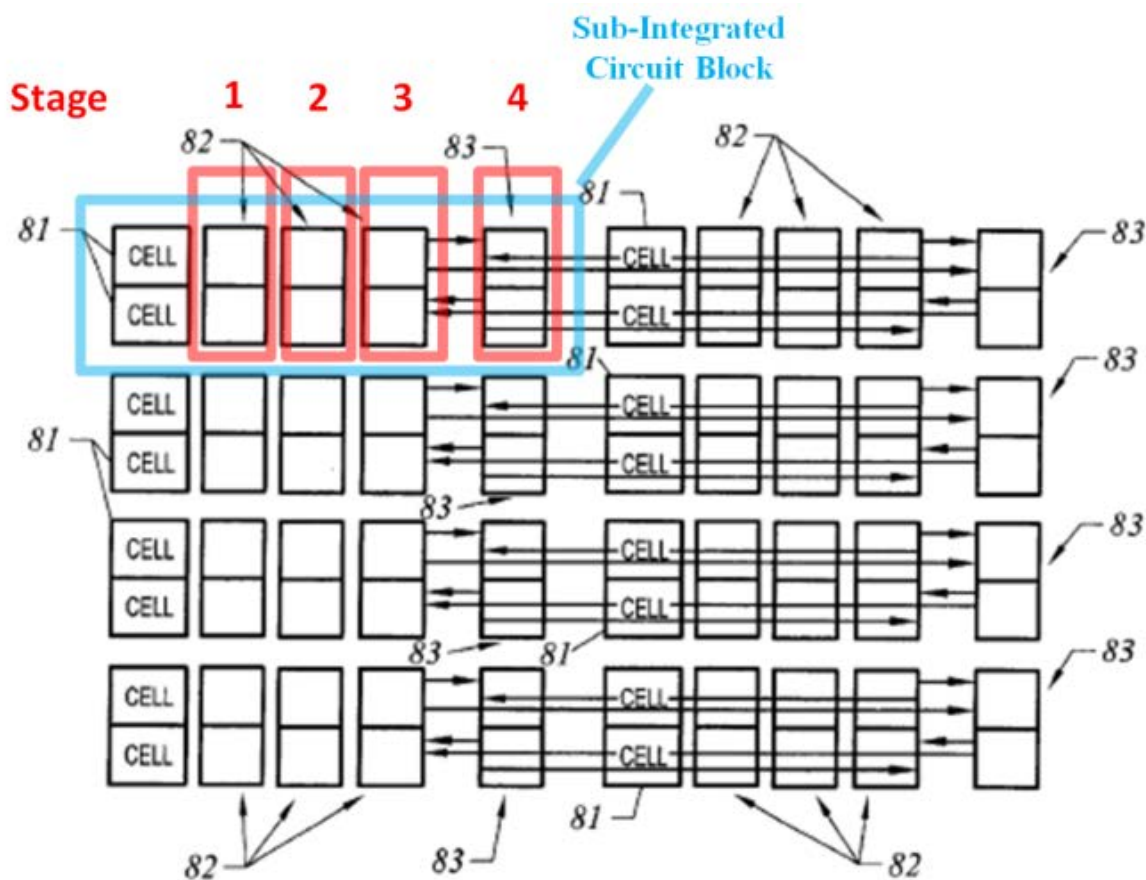
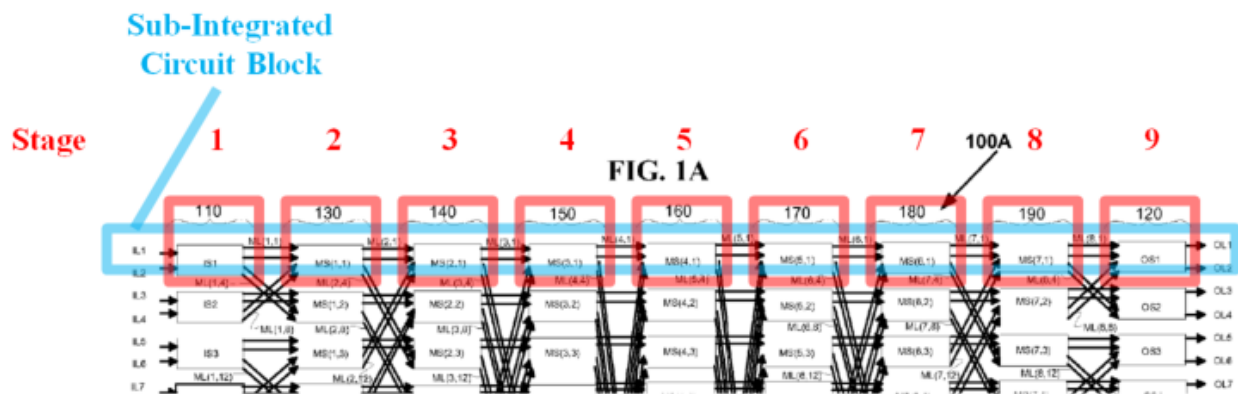


FIG. 13B

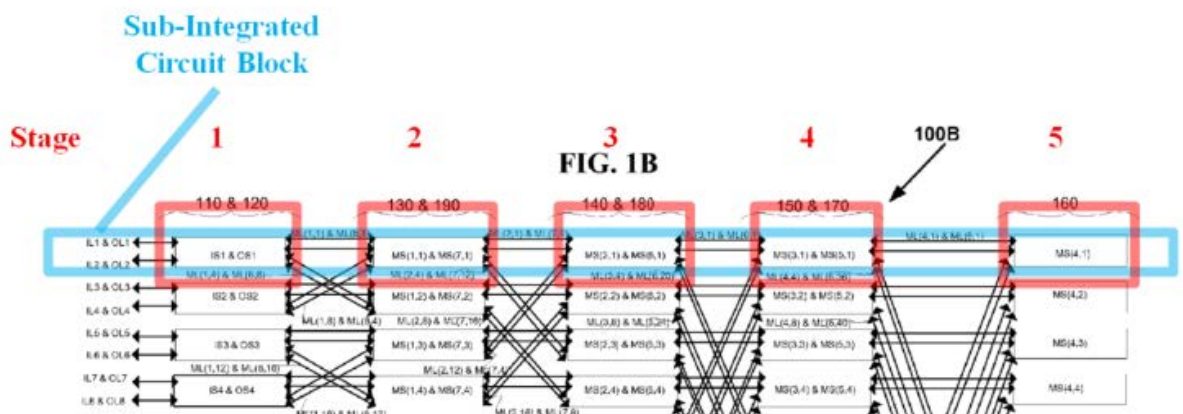
(Ex. 1008 at FIG. 13B (annotated).)

71. *Wong*'s disclosure of the sub-integrated circuit blocks including a plurality of stages aligns with the teachings of the '523 patent. For example, the '523 patent states that figure 1A is a diagram of a network “having inverse Benes connection topology of nine stages” (Ex. 1001 at 3:51-57), whereas figure 1B is a

diagram of the “equivalent symmetrical folded” network shown in figure 1A with five stages (*id.* at 3:58-64). Therefore, once the network of figure 1A has been folded, the switches that were in the upper-level stages are considered to be part of the lower level stages. For example, switch 120, which corresponds to stage 9 in figure 1A, is part of stage 1 in the folded network shown in figure 8B.



(Ex. 1001 at FIG. 1A (excerpt, annotated).)



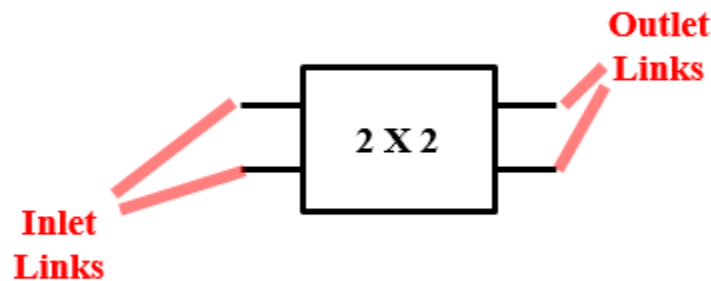
(Ex. 1001 at FIG. 1B (excerpt, annotated).)

- e) **“Said routing network comprising a plurality of switches of size $d \times d$, where $d \geq 2$, in each said stage and each said switch of size $d \times d$ having d inlet links and d outlet links; and”**

72. In my opinion, *Wong* discloses this feature. According to claim element 1(e), each stage of the network includes a plurality of switches, each of which has at least two inlet links (d inputs) and the same number of outlet links (d outputs). Notably, in the relevant art of integrated circuits, “a switch of size $d \times d$ ” in the context of “each said switch of size $d \times d$ having d inlet links and d outlet links” would have informed a person of ordinary skill in the art about the input/output configuration of the switch, and not the actual area (i.e., physical size) of the switch. In other words, a person of ordinary skill would have understood that “size” in the context of this claim term does not refer to the physical measurements of the switch, but instead refers to the number of inputs and outputs.

73. A person of ordinary skill in the art would have understood that a $d \times d$ switch is a symmetrical switch in that it has the same number of inputs and outputs. Examples of $d \times d$ switches with $d \geq 2$ include a 2×2 switch (two inputs and two outputs), a 3×3 switch (three inputs and three outputs), and a 4×4 switch (four inputs and four outputs). Such an understanding is supported by other patents naming the same inventor as the '523 patent. For example, claim 1 of U.S. Patent No. 10,003,553 (“the '553 patent”) recites “each stage comprising a switch of size $d_i \times$

d_o , where $d_i \geq 2$ and $d_o \geq 2$ and each switch of size $d_i \times d_o$ having d_i incoming links and d_o outgoing links.” (Ex. 1006 at 49:1-3.) Because claim 1 of the ’553 patent does not require that d_i must equal d_o , a person of ordinary skill in the art would have understood that in the ’553 patent the named inventor claimed switches that can have different numbers of inputs and outputs. In contrast, in the ’523 patent the recited $d \times d$ switches have the same number of inputs as outputs. I have created the demonstrative below showing a 2×2 switch with two inputs (“ d inlet links”) and two outputs (“ d outlet links”).



74. As explained below, *Wong* discloses that in the embodiments shown in figures 13A and 13B each stage includes a 4×4 switch that in turn can be made up of multiple 2×2 switches. Therefore, *Wong* discloses “a plurality of switches of size $d \times d$, where $d \geq 2$, in each said stage and each said switch of size $d \times d$ having d inlet links and d outlet links.”

75. Each stage in the sub-integrated circuit blocks shown in figures 13A and 13B includes a switch. For example, as shown below in figure 13A, each of stages 1-3 includes a switch 82. (Ex. 1008 at 13:22-24.)

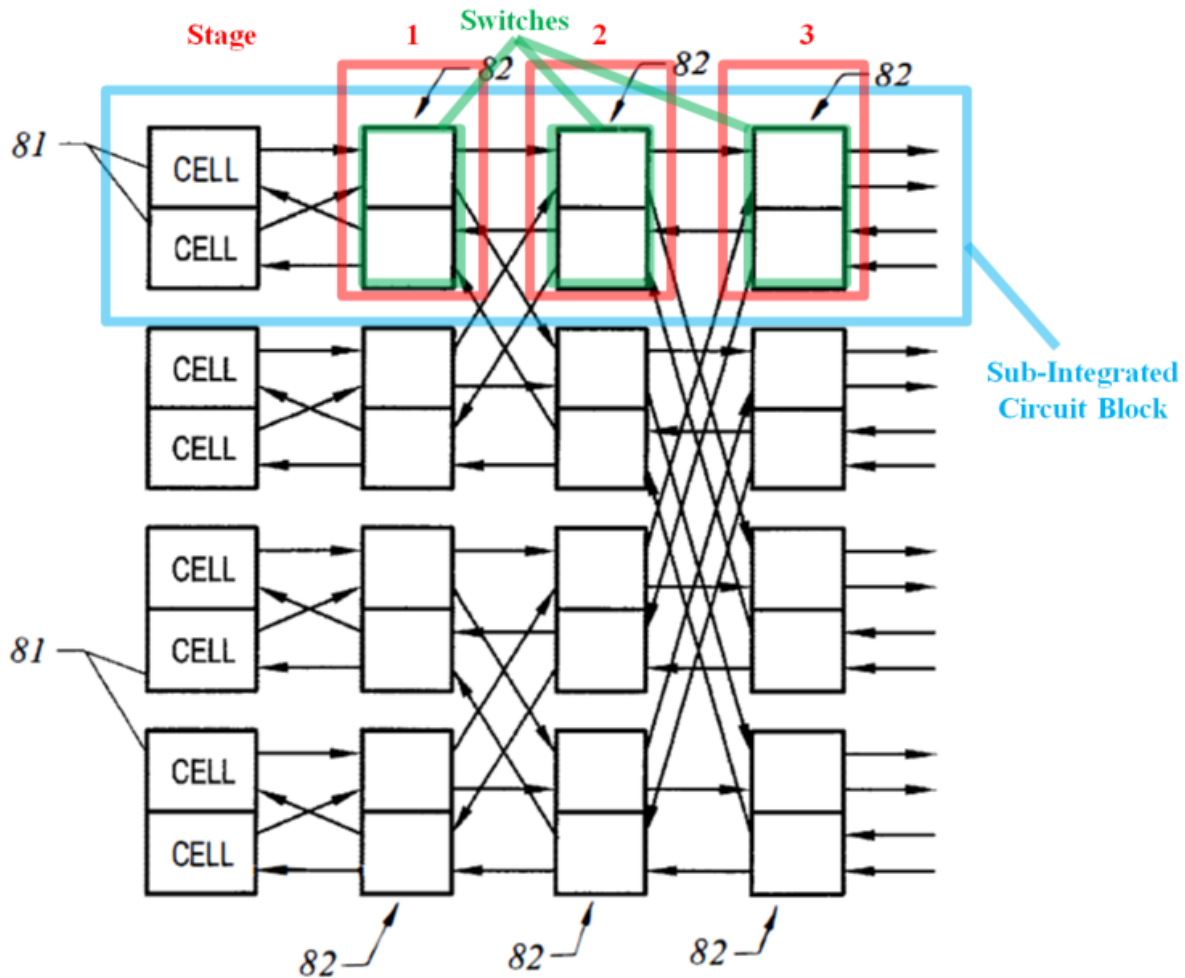
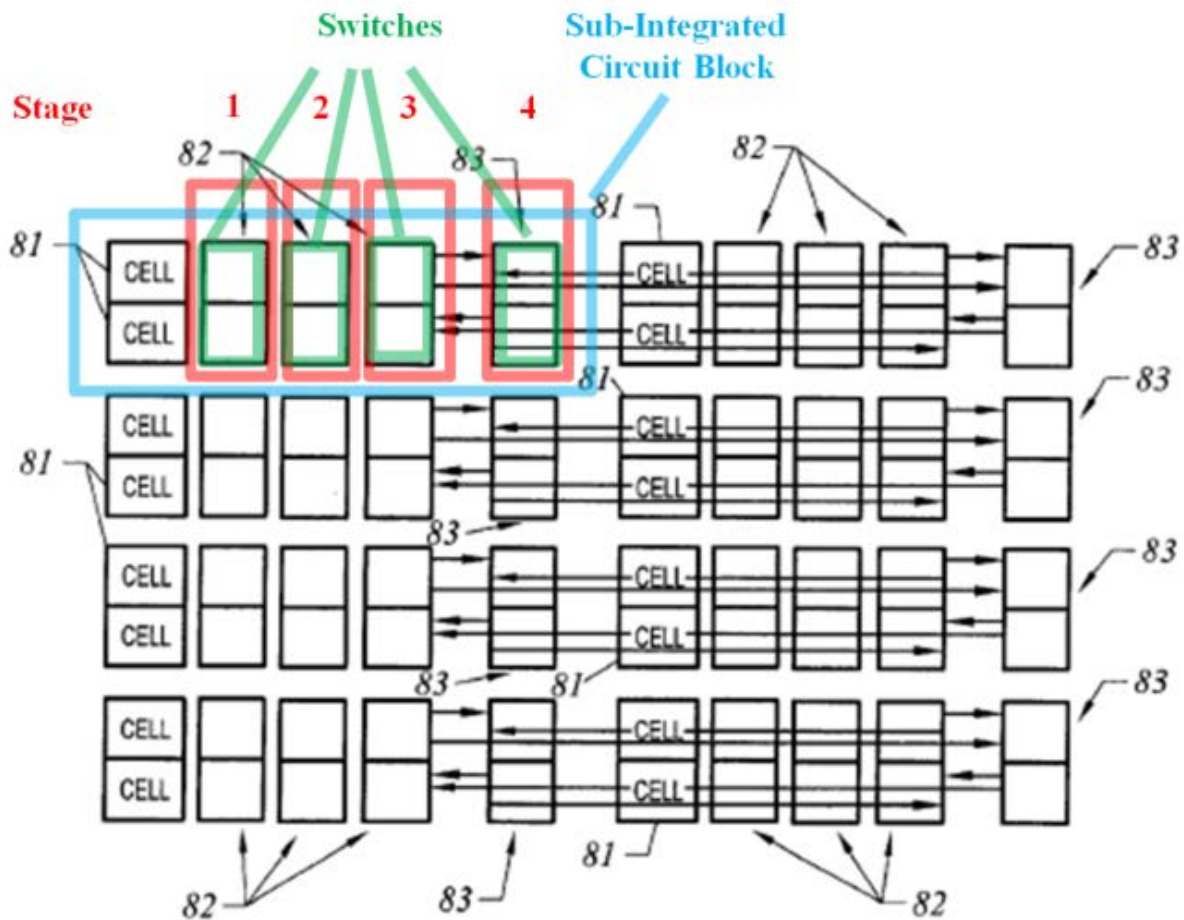


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated).)

76. Similarly, each stage in each sub-integrated circuit block in figure 13B includes switches 82 and 83. (Ex. 1008 at 13:22-24, 13:33-38.)



(Ex. 1008 at FIG. 13B (annotated).)

77. As shown in figure 13A, each switch 82 has four inputs and four outputs. (Ex. 1008 at FIG. 13A.) While the switches 83 added in figure 13B only show two inputs and outputs, a person of ordinary skill would have understood that there are also two additional inputs and outputs corresponding to the primary input/output (I/O) of the FPGA, which are not shown in figure 13B, but are shown

in figure 13A. (Ex. 1008 at FIGs. 13A-13B, 13:42-43 (“As before, each column’s top-level inputs and outputs are connected to the primary I/O of the FPGA.”).)

78. *Wong* discloses that the 4x4 switches shown in figures 13A and 13B can be made up of sets of 2x2 switches such as those shown in figures 2A and 2B. (Ex. 1008 at 5:4-6 (“[t]he building block of the described Benes network is the 2x2 (2 input, 2 output) switch 20, having operations illustrated in FIGS. 2A and 2B.”).) As further disclosed by *Wong*, “[t]hese 2x2 switches are connected in a specific topology to build a Benes network. (*Id.* at 5:26-27.) Such a Benes network is shown in figure 4B, where figures 13A and 13B are also Benes networks that build on the disclosure corresponding to figure 4B in *Wong*. (*Id.* at 7:6-8, 8:65-9-1, 13:19-22, 13:33-38.)

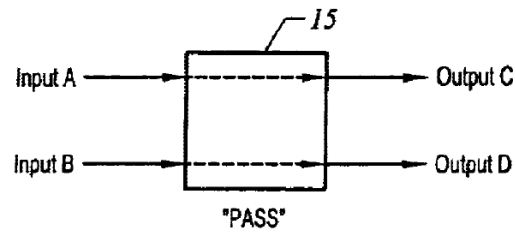


FIG. 2A

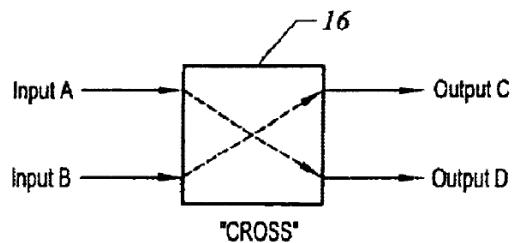


FIG. 2B

(Ex. 1008 at FIGs. 2A, 2B.)

79. Therefore, a person of ordinary skill in the art would have understood that all of the switches 82, 83 shown in figures 13A and 13B can be 4x4 switches or a set of two 2x2 switches (such as is shown in figure 4B). (*Id.* at FIGs. 13A, 13B, 4B.) As shown in the annotated versions of figure 13A of *Wong* below, each switch cell 82 in each of stages 1-3 can include two 2x2 switches, where each 2x2 switch has two inputs ("d inlet links") and two outputs ("d outlet links").

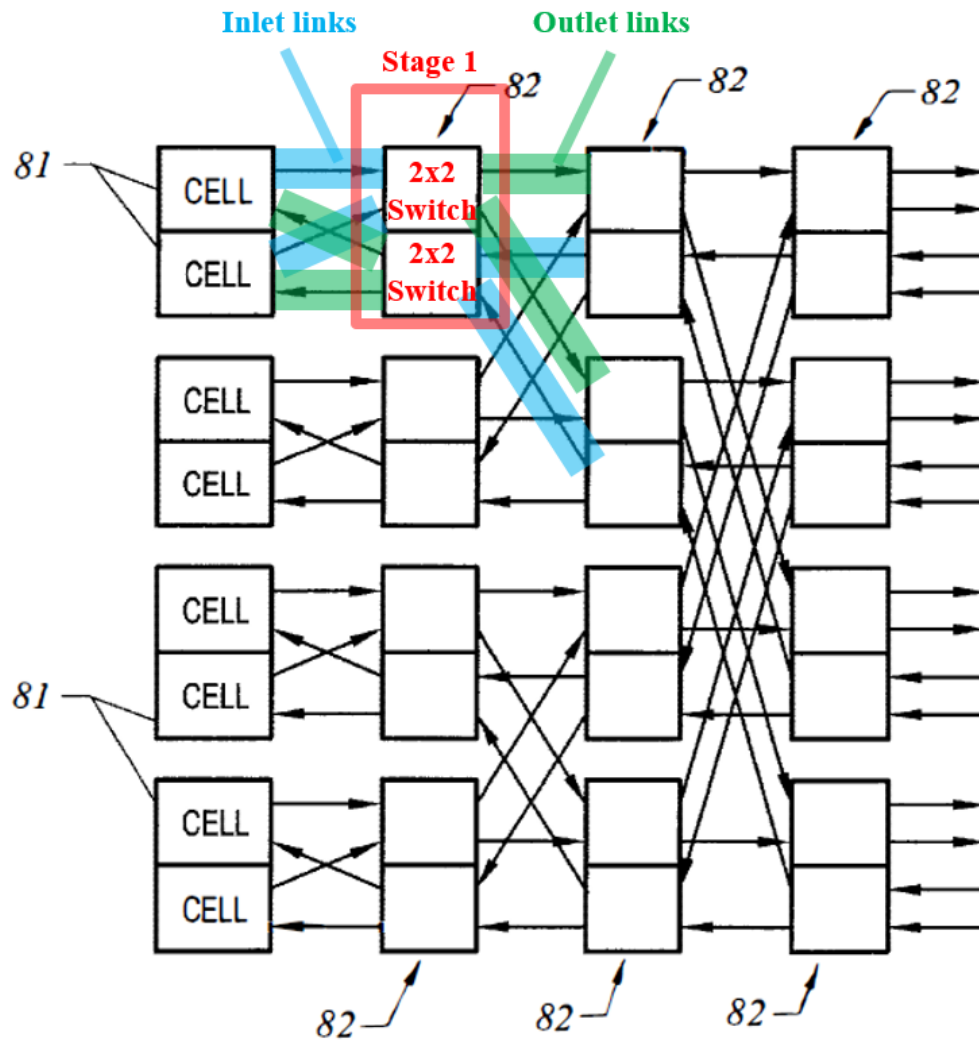


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated to show inlet links (blue) and outlet links (green) for Stage 1).)

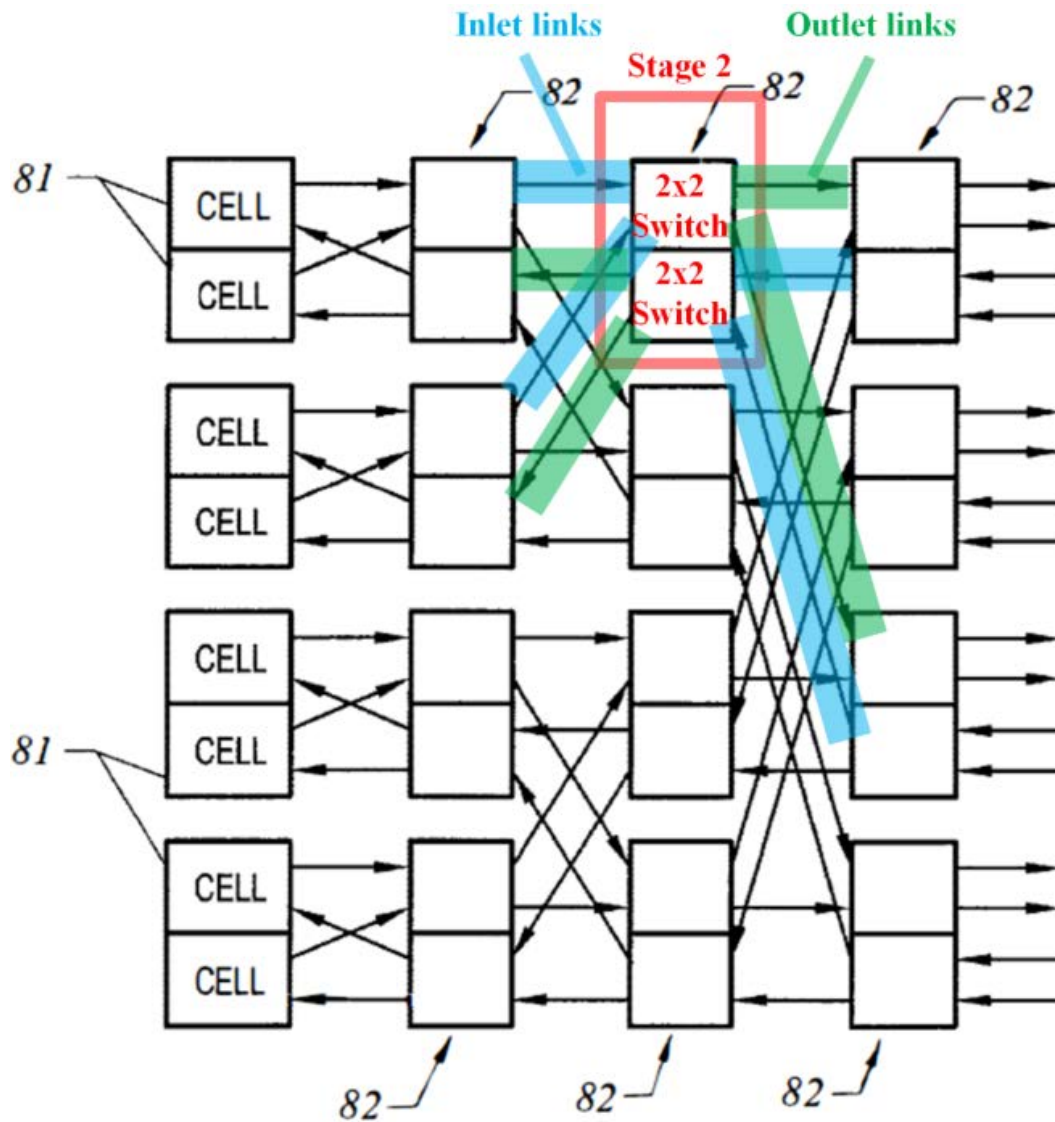


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated to show inlet links (blue) and outlet links (green) for Stage 2).)

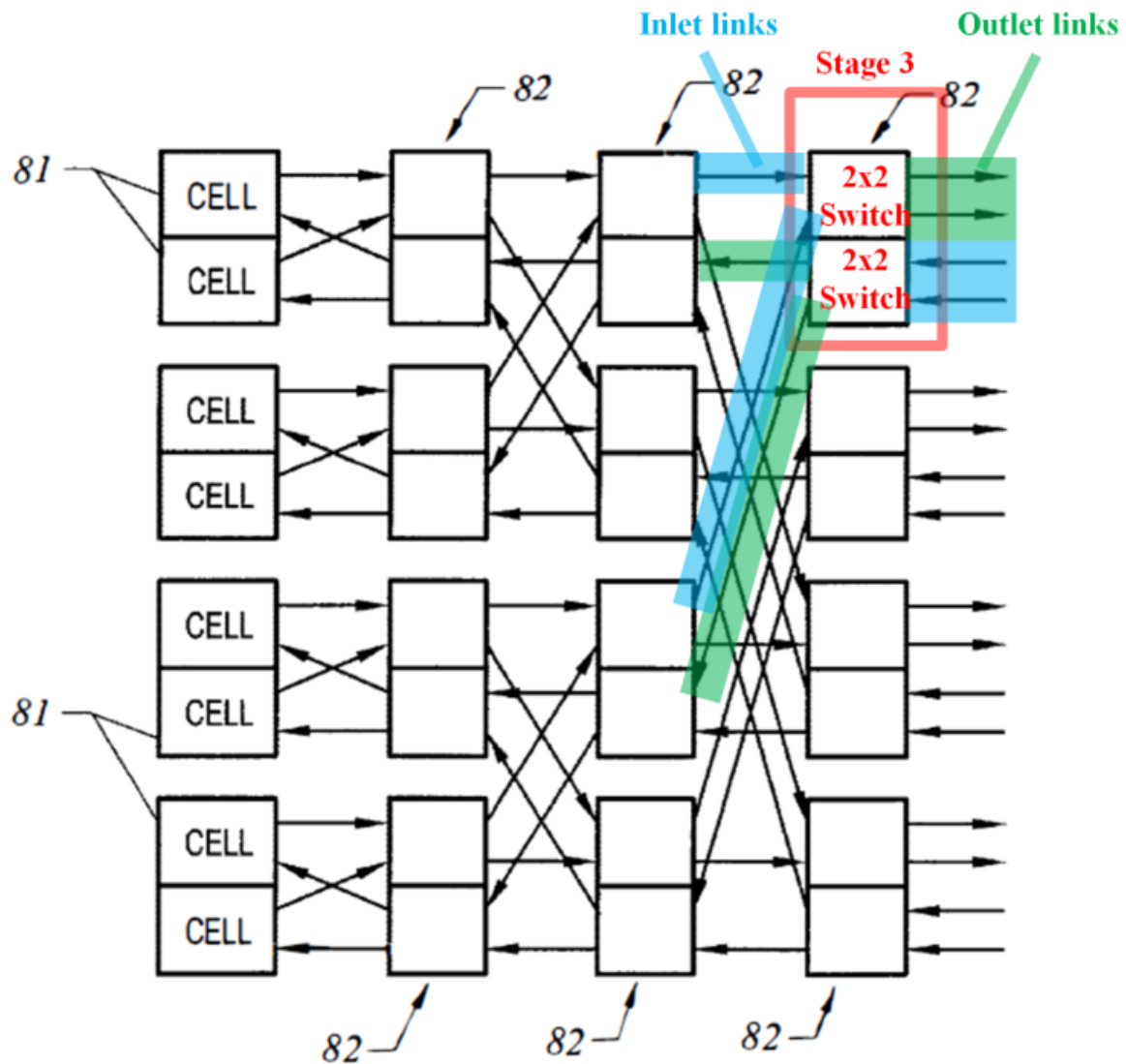
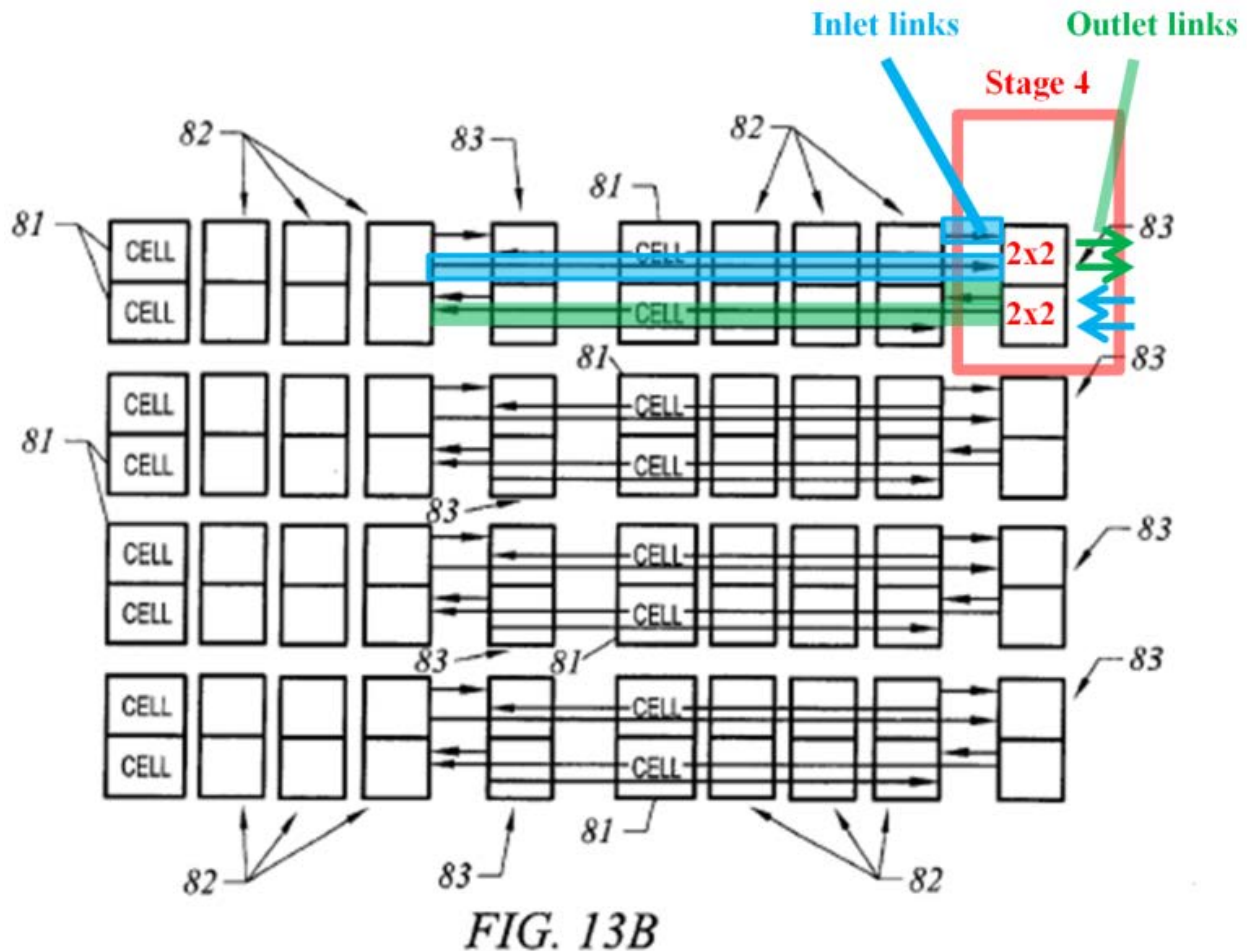


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated to show inlet links (blue) and outlet links (green) for Stage 3).)

80. As disclosed by *Wong*, figure 13B includes two instantiations of figure 13A with the addition of another stage of switches 83. (Ex. 1008 at 3:7-10, 13:36-38.) Therefore, like the network of figure 13A, each switch in each of the stages in

figure 13B can be implemented using two 2x2 switches, where each switch has two incoming links and two outgoing links.



(Ex. 1008 at FIG. 13B (annotated to show inlet links (blue) and outlet links (green) for stage 4).)

81. Note that I have added annotations to figure 13B above to show the inlet links and outlet links corresponding to the primary I/O of the FPGA. (Ex. 1008 at 13:41-42 (“As before each columns top-level inputs and outputs are connected to

the primary I/O of the FPGA.”.) As such, each switch 83 includes two 2x2 switches, each of which has two incoming links and two outgoing links.

82. Because the network includes a plurality of sub-integrated circuit blocks, each stage includes a plurality of 4x4 switches, where those 4x4 switches can be implemented as a plurality of 2x2 switches. For example, because there are four sub-integrated circuit blocks in the network of figure 13A, each of stages 1-3 in the routing network has four 4x4 switches (one 4x4 switch per sub-integrated circuit block in each of stages 1-3). If the 4x4 switches are implemented using 2x2 switches, then each stage includes eight 2x2 switches (two 2x2 switches per stage). (Ex. 1008 at FIG. 13A.) For the embodiment in figure 13B, there are eight sub-integrated circuit blocks and therefore each stage includes eight 4x4 switches or 16 2x2 switches. (*Id.* at FIG. 13B.) Therefore, *Wong* discloses “said routing network comprising a plurality of switches of size $d \times d$, where $d \geq 2$, in each said stage and each said switch of size $d \times d$ having d inlet links and d outlet links.”

83. Notably, a person of ordinary skill in the art would have understood that this claim feature does not require a plurality of $d \times d$ switches **in each stage in each sub-integrated circuit block**, but instead simply requires a plurality of $d \times d$ switches **in each stage of the routing network**. Such an understanding is supported by the prosecution history of the '523 patent. Original claim 1 of U.S. Application

No. 12/601,275 (the application that ultimately issued as the '523 patent) included, in addition to the feature that issued as limitation 1(e), an additional limitation that required “[s]aid each sub-integrated circuit block comprising a plurality of said switches corresponding to each stage.” (Ex. 1004 at 217 (lines 15-16), 325 (lines 15-16).) But that additional feature, which required a plurality of dxd switches in each stage in **each sub-integrated circuit block**, was deleted by the applicant during prosecution. (*Id.* at 67.) Therefore, a person of ordinary skill in the art would have understood that claim element 1(e) does not require a plurality of dxd switches in each stage of each sub-integrated circuit block.

- f) **“Said plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1; and”**

84. In my opinion, *Wong* discloses this feature. For example, as shown in figure 13A of *Wong*, each of the output pins (“outlet links”) of the logic cells in each sub-integrated circuit block is directly connected to a corresponding inlet link of the first stage (“said lowest stage of 1”) of the same sub-integrated circuit block.

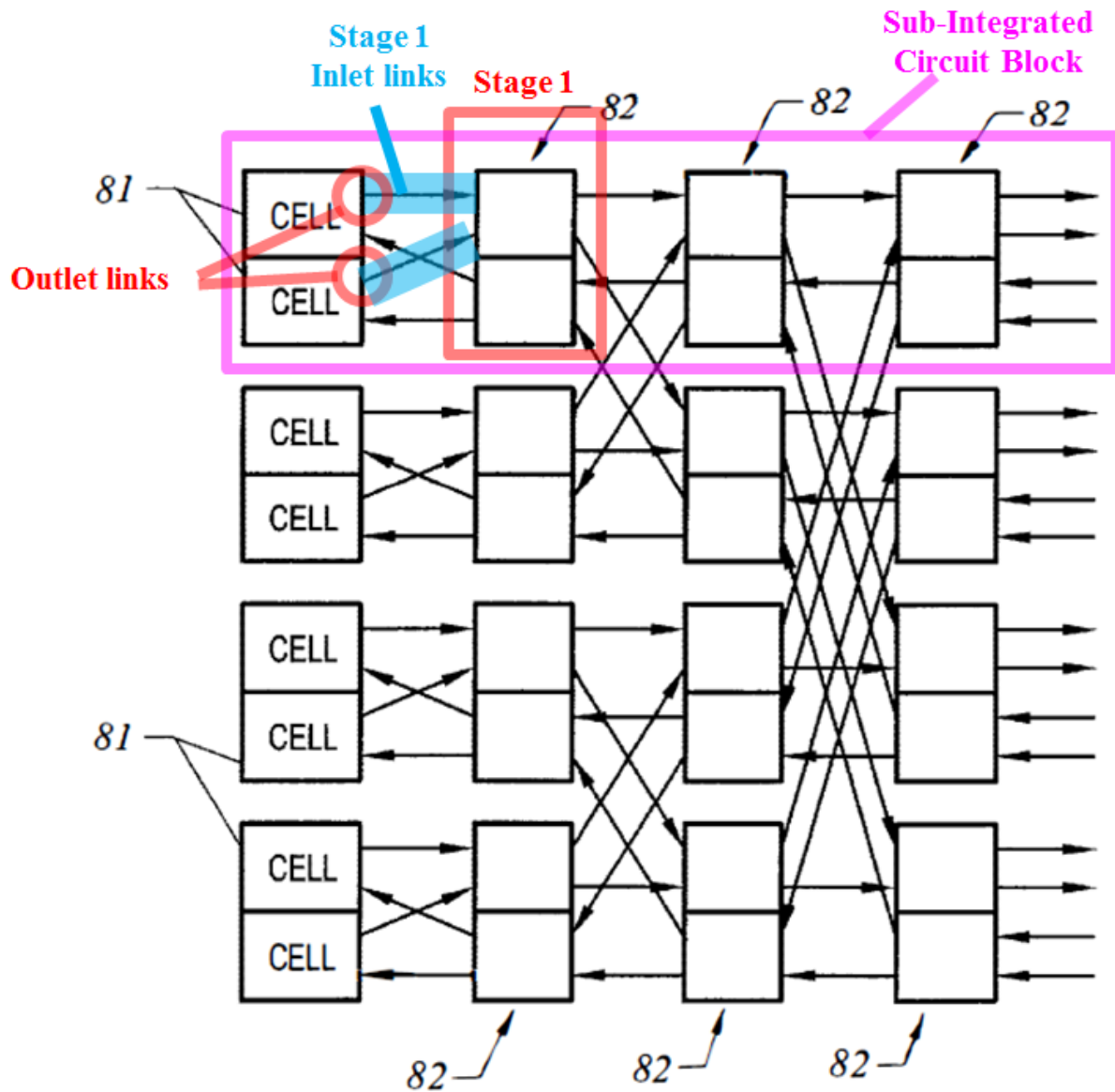


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated).)

85. Similarly, as shown in figure 13A of *Wong*, each of the input pins (“inlet links”) of the logic cells in each sub-integrated circuit block is directly

connected to a corresponding outlet link of the first stage (“said lowest stage of 1”) of the same sub-integrated circuit block.

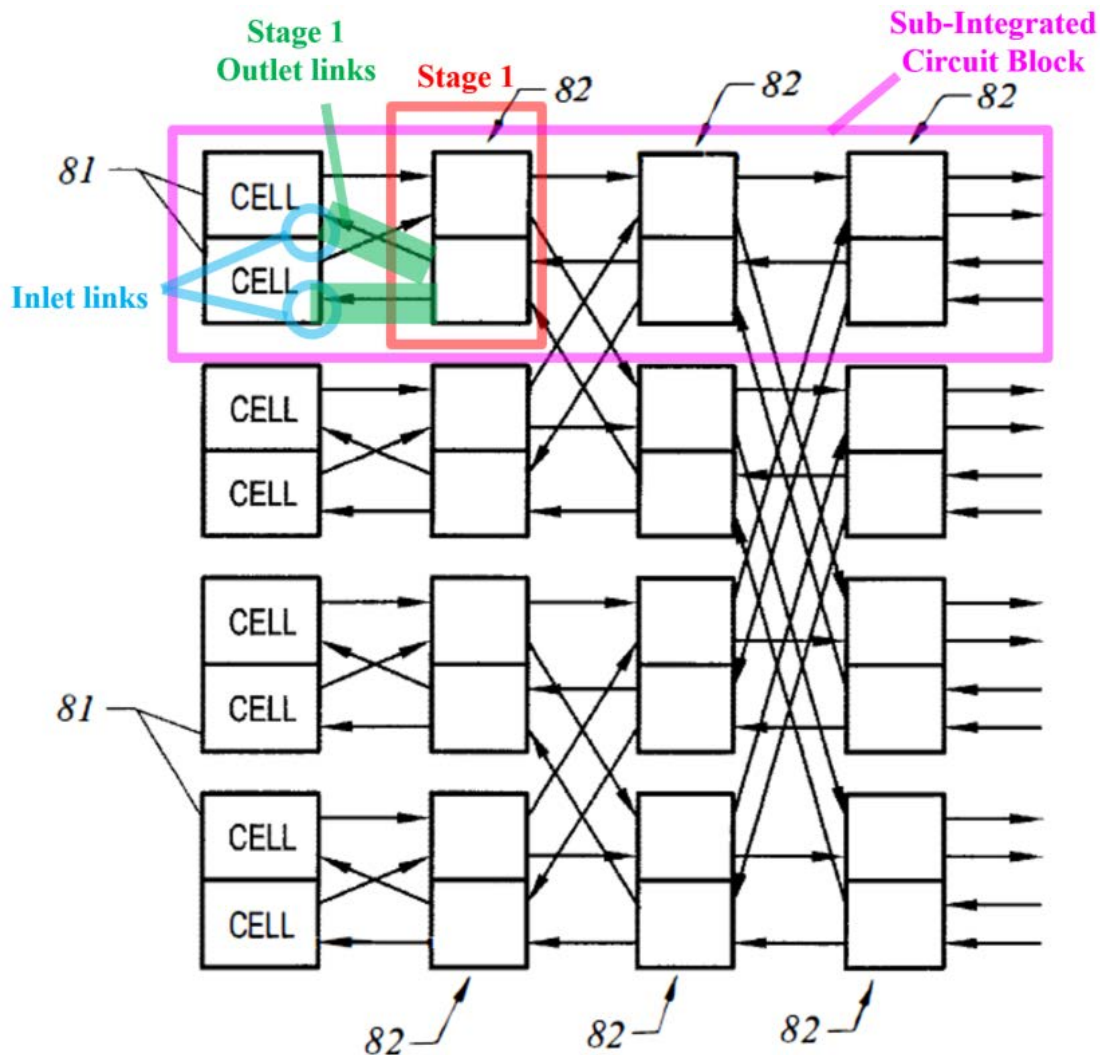


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated).)

86. While not explicitly shown in figure 13B, the connections between the logic cells and stage 1 switches of the sub-integrated circuit block are also present

in figure 13B because figure 13B includes two instantiations of the circuitry and connections shown in figure 13A. (Ex. 1008 at 13:36-38.) Therefore, each of the embodiments shown in figures 13A and 13B of *Wong* discloses the claimed feature “[s]aid plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1.”

- g) **“Said each sub-integrated circuit block comprising a plurality of forward connecting links connecting from switches in a lower stage to switches in its immediate succeeding higher stage, and also comprising a plurality of backward connecting links connecting from switches in a higher stage to switches in its immediate preceding lower stage; and”**

87. In my opinion, *Wong* discloses this feature. I have been instructed to assume that the recited “forward connecting links” include links from switches in a lower stage to an immediately succeeding higher stage in the same or a different sub-integrated circuit block. Such an assumption is consistent with the forward connecting links including cross links and straight links in claim limitation 1(h) (*see* below at Section IX.A.1(h)), as the ’523 patent specification defines “cross links” to

be between successive stages in *different* blocks, whereas “straight links” are links between successive stages in the *same* block. (Ex. 1001 at 9:45-49.)

88. As illustrated in annotated figure 13A of *Wong* below, each sub-integrated circuit block includes “a plurality of forward connecting links” as claimed in limitation 1(g). For example, the top-most sub-integrated circuit block (highlighted in purple) includes a plurality of forward connecting links (highlighted in green). Each of the forward connecting links shown is connected from a switch in a lower stage to a switch in an immediately succeeding higher stage.

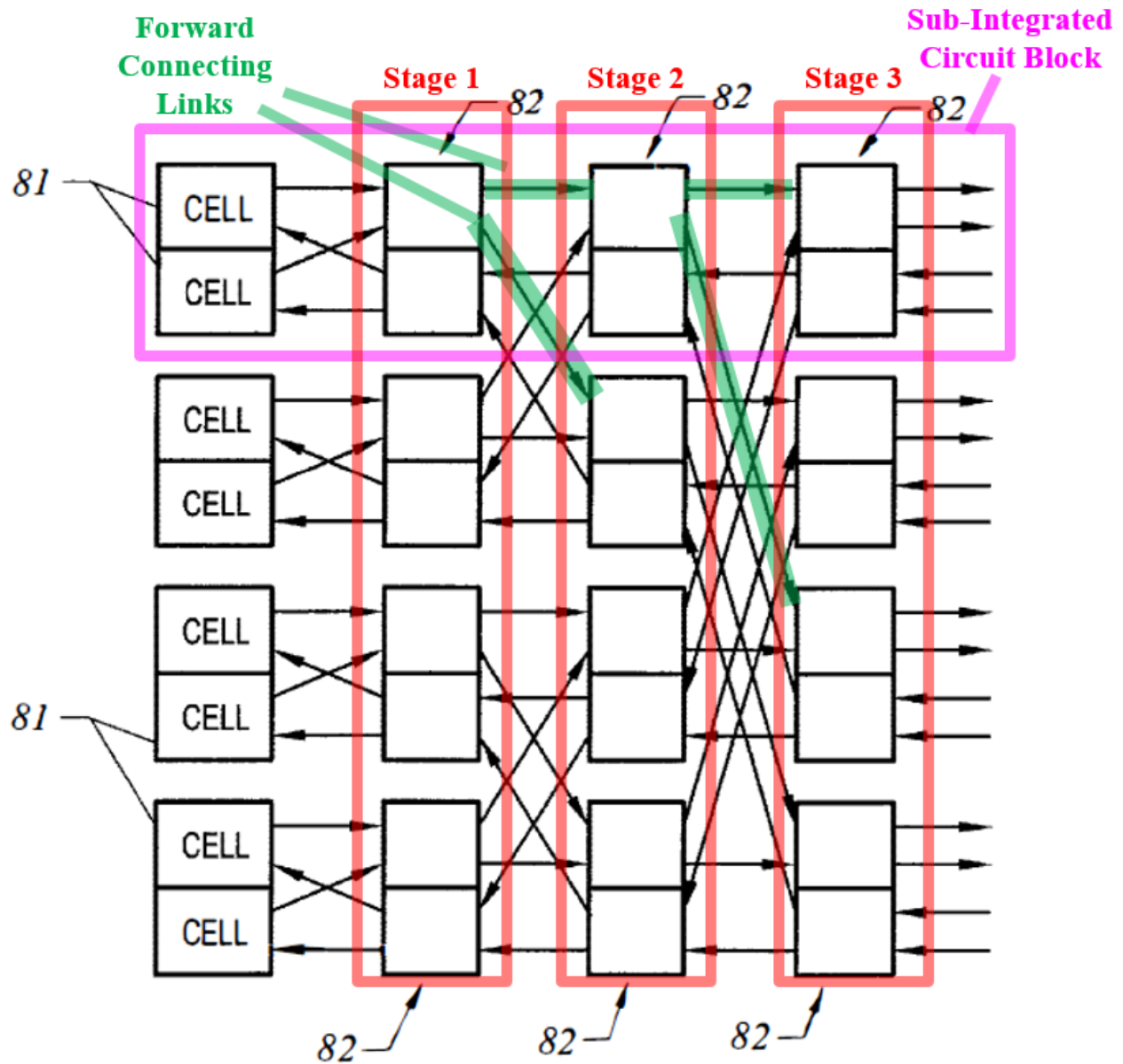
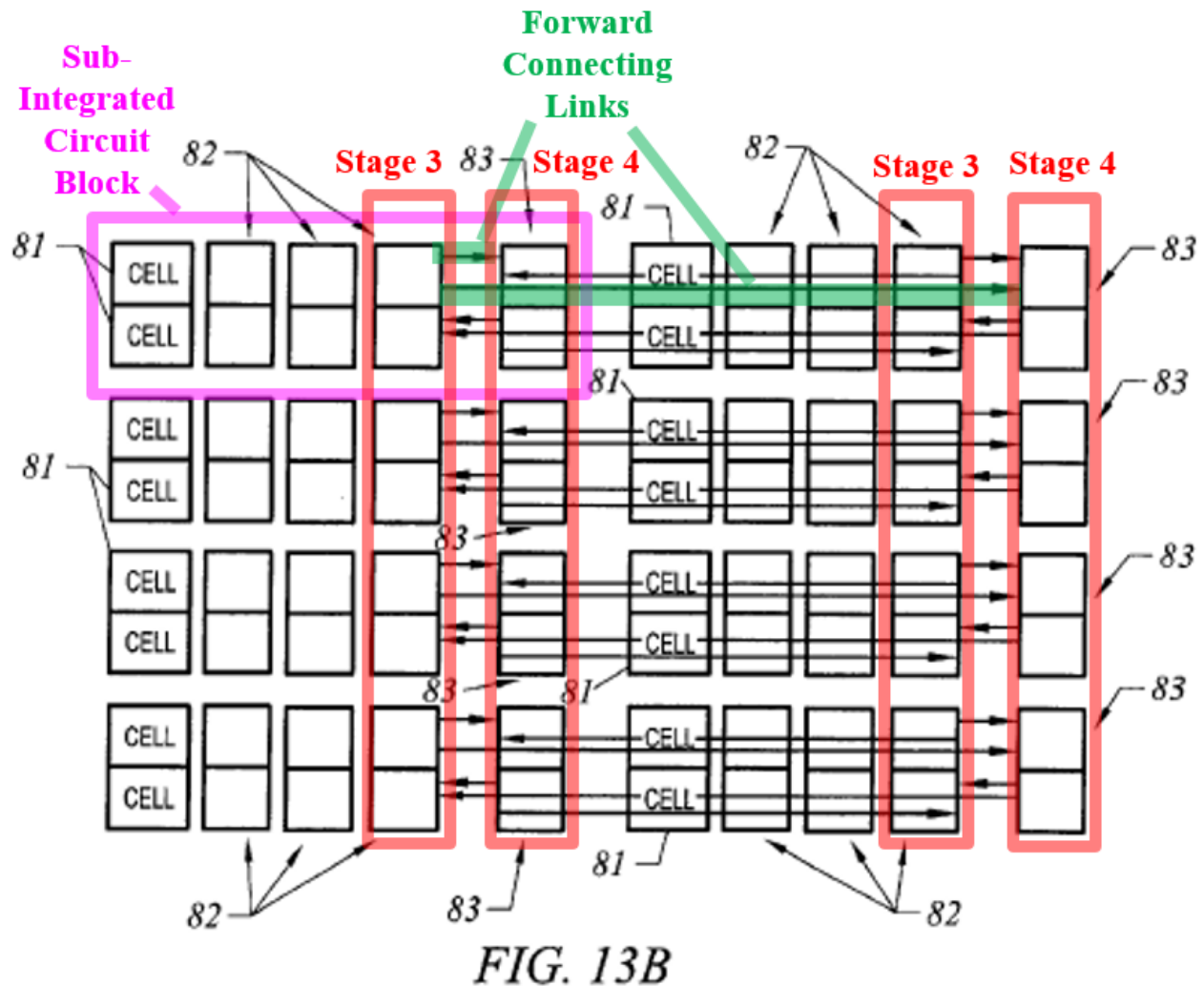


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated to show forward connecting links (green) for the top sub-integrated circuit block (purple)).)

89. The forward connecting links shown in annotated figure 13A above are connected from switches in stage 1 (“a lower stage”) to switches in stage 2 (“an immediate succeeding higher stage”) or from switches in stage 2 (“a lower stage”) to switches in stage 3 (“an immediate succeeding higher stage”). While the annotations above are only used to highlight the forward connecting links in the top sub-integrated circuit block, a person of ordinary skill in the art would have understood that figure 13A shows that each of the sub-integrated circuit blocks includes a plurality of forward connecting links.

90. Figure 13B also includes a plurality of forward connecting links in each of the sub-integrated circuit blocks. In addition to the forward connecting links described above with respect to figure 13A, which are also present in the embodiment of figure 13B, figure 13B shows additional forward connecting links between stage 3 and the added stage 4 for each sub-integrated circuit block. The additional forward connecting links shown in annotated figure 13B below are connected from switches in stage 3 (“a lower stage”) to switches in stage 4 (“an immediate succeeding higher stage”).



(Ex. 1008 at FIG. 13B (annotated to show forward connecting links (green) for the top left sub-integrated circuit block (purple)).)

91. While the annotations above are only used to highlight the forward connecting links in the top-left sub-integrated circuit block, a person of ordinary skill in the art would have understood that each of the sub-integrated circuit blocks in figure 13B includes a plurality of forward connecting links.

92. In my opinion, *Wong* also discloses backward connecting links as recited in claim element 1(g). As illustrated in figure 13A of *Wong*, each sub-integrated circuit block includes a plurality of backward connecting links. For example, as shown in the annotated figure 13A below, the top-most sub-integrated circuit block (highlighted in purple) includes a plurality of backward connecting links (highlighted in blue). Each of the backward connecting links shown is connected from a switch in a higher stage to a switch in an immediately preceding lower stage.

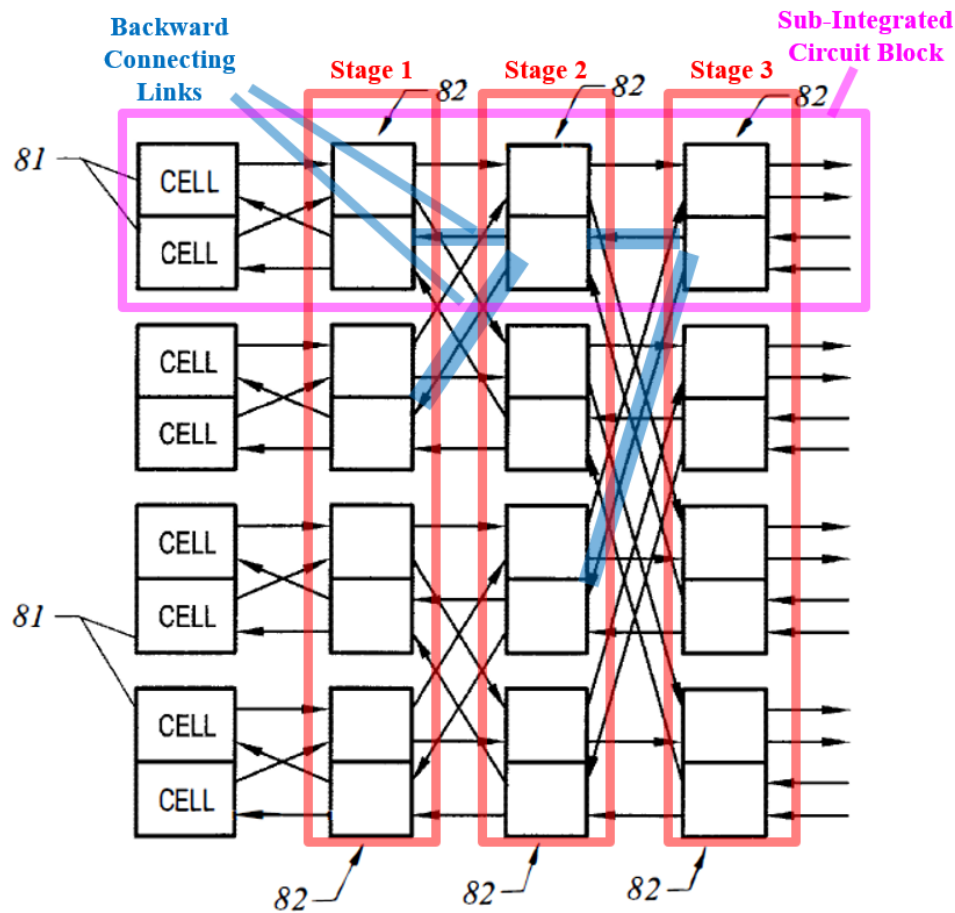


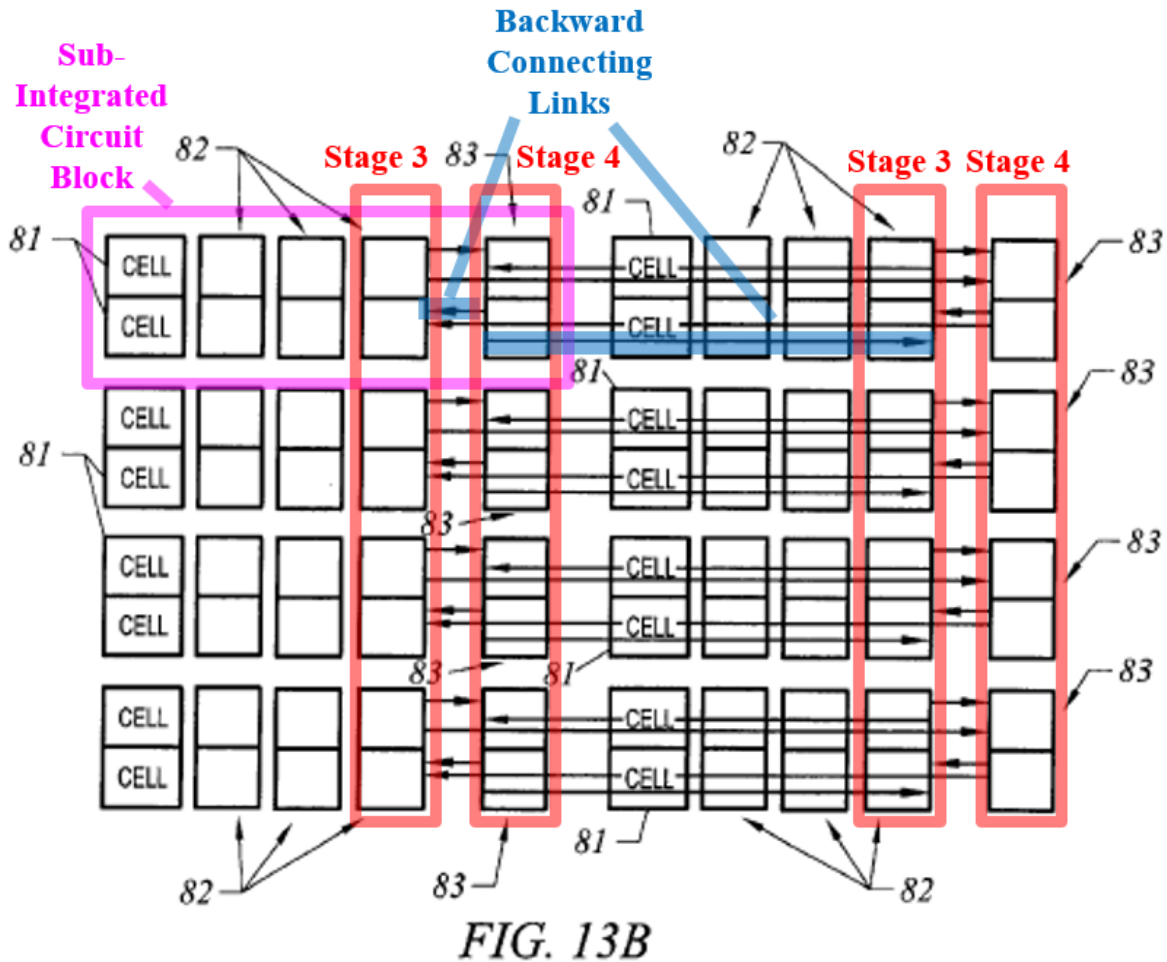
FIG. 13A

(Ex. 1008 at FIG. 13A (annotated to show backward connecting links (blue) for the top sub-integrated circuit block (purple)).)

93. The backward connecting links shown in annotated figure 13A above are connected from switches in stage 2 (“a higher stage”) to switches in stage 1 (“an immediate preceding lower stage”) or from switches in stage 3 (“a higher stage”) to switches in stage 2 (“an immediate preceding lower stage”). While the annotations above are only used to highlight the backward connecting links in the top sub-

integrated circuit block, a person of ordinary skill in the art would have understood that figure 13A shows that each of the sub-integrated circuit blocks includes a plurality of backward connecting links.

94. Figure 13B also includes a “plurality of backward connecting links” in each of the sub-integrated circuit blocks, as recited in limitation 1(g). In addition to the backward connecting links described above with respect to figure 13A, which are also present in the embodiment shown in figure 13B, figure 13B includes additional backward connecting links between the added stage 4 and stage 3 for each sub-integrated circuit block. The additional backward connecting links highlighted in annotated figure 13B below are connected from switches in stage 4 (“a higher stage”) to switches in stage 3 (“an immediate preceding lower stage”).



(Ex. 1008 at FIG. 13B (annotated to show backward connecting links (blue) for the top-left sub-integrated circuit block (purple)).)

95. While the annotations above are only used to highlight the backward connecting links in the top-left sub-integrated circuit block, a person of ordinary skill in the art would have understood that figure 13B shows that each of the sub-integrated circuit blocks includes a plurality of backward connecting links.

- h) **“Said each sub-integrated circuit block comprising a plurality [of] straight links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage and a plurality [of] cross links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage, and further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage and a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage,”**

96. In my opinion, *Wong* discloses this feature. According to the '523 patent, “[t]he middle links which connect switches in the same row in two successive middle stages are called hereinafter straight middle links; and the middle links which connect switches in different rows in two successive middle stages are called hereinafter cross middle links.” (Ex. 1001 at 9:45-49.) *Wong* discloses straight and cross links consistent with this definition and the language of claim 1.

- (1) **“Said each sub-integrated circuit block comprising a plurality [sic] straight links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage”**

97. As shown in annotated figure 13A below, *Wong* discloses that each sub-integrated circuit block includes “a plurality straight links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding

higher stage.” Annotated figure 13A below shows a plurality of straight links in the forward connecting links for the top sub-integrated circuit block, where the plurality of straight links includes a straight link from stage 1 to stage 2 and another straight link from stage 2 to stage 3.

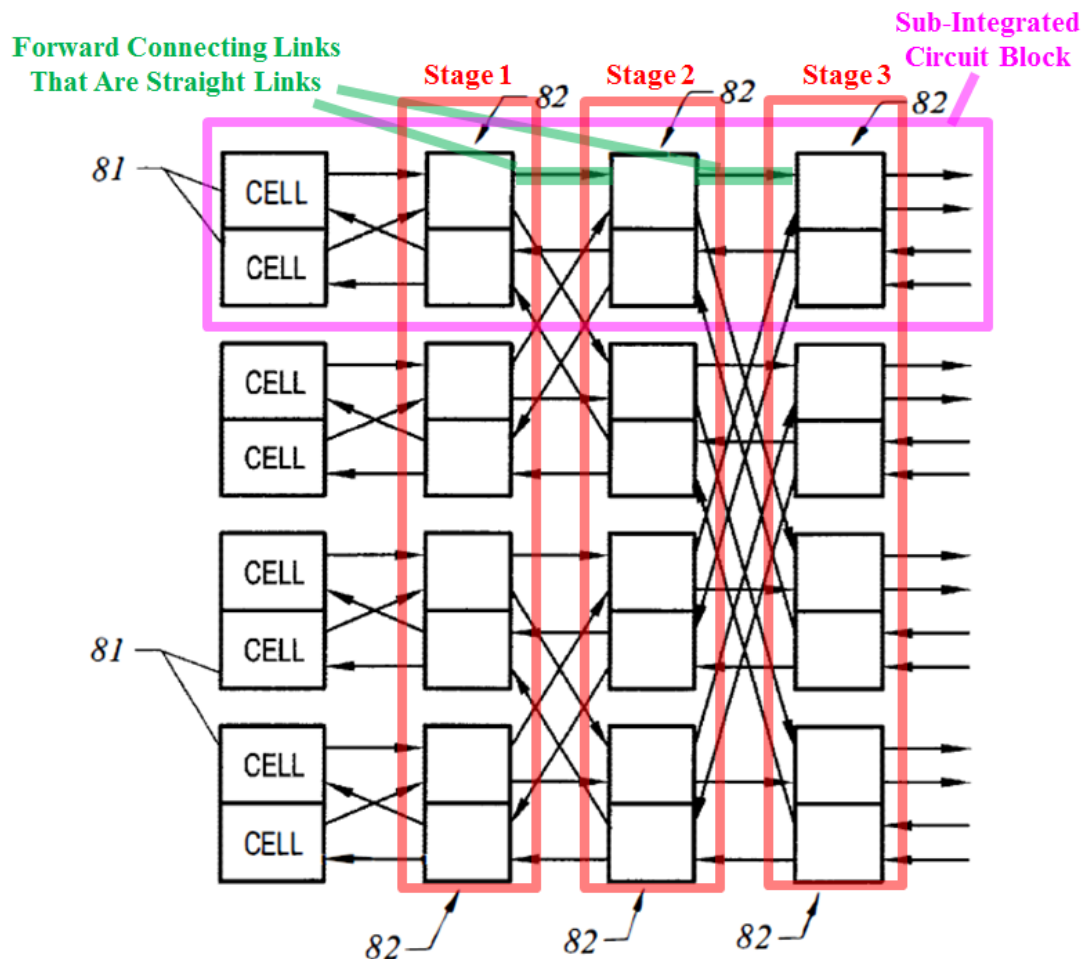


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated to show forward connecting links that are straight links (green) in the top sub-integrated circuit block (purple)).)

98. While the annotations above are only used to highlight the straight links in the top sub-integrated circuit block, a person of ordinary skill in the art would have understood that figure 13A shows that each of the sub-integrated circuit blocks includes a plurality of forward connecting links that are straight links.

99. Figure 13B also discloses that each sub-integrated circuit block includes “a plurality straight links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage.” In addition to the straight links included in figure 13A discussed immediately above, which are also present in the figure 13B embodiment, figure 13B adds an additional forward connecting link that is a straight link for each sub-integrated circuit block. In the annotated figure 13B below, the additional straight link highlighted in green is from stage 3 to stage 4 for the top-left sub-integrated circuit block.

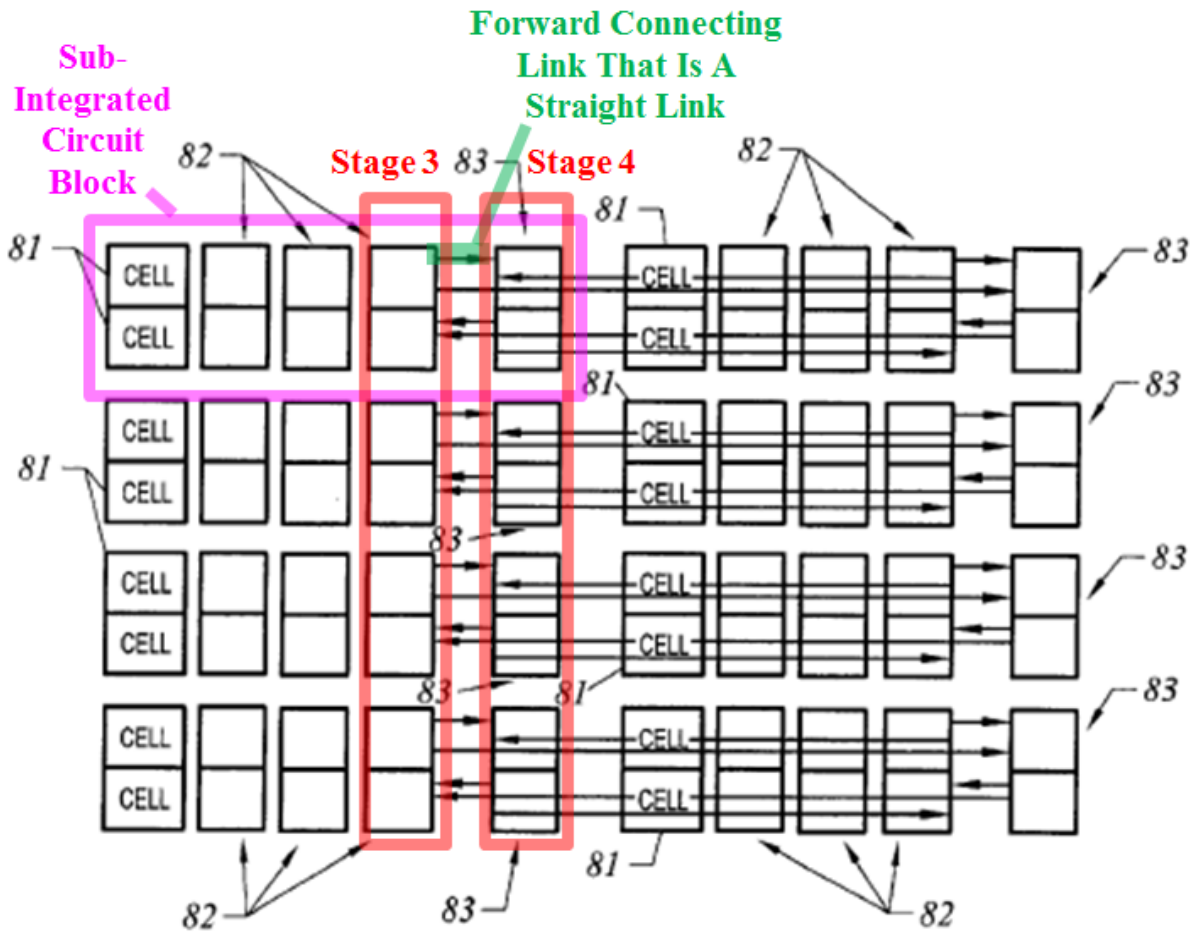


FIG. 13B

(Ex. 1008 at FIG. 13B (annotated to show a forward connecting link that is a straight link (green) from stage 3 to stage 4 in the top-left sub-integrated circuit block (purple)).)

100. While the annotations above are only used to highlight the forward connecting links that are straight links in the top-left sub-integrated circuit block, a person of ordinary skill in the art would have understood that figure 13B shows that

each of the sub-integrated circuit blocks includes a plurality of forward connecting links that are straight links.

- (2) “[Said each sub-integrated circuit block comprising . . .] a plurality [of] cross links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage, and”

101. In addition to forward connecting links that are straight links, *Wong* also discloses forward connecting links that are cross links. As shown in annotated figure 13A below, *Wong* discloses that each sub-integrated circuit block includes “a plurality [of] cross links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage,” as claimed. The plurality of cross links for the top sub-integrated circuit block in figure 13A are highlighted below, where the plurality of cross links includes cross links from stage 1 to stage 2 and from stage 2 to stage 3. As shown in the annotated figure 13A below, the cross links are links which connect switches in different rows (corresponding to different sub-integrated circuit blocks).

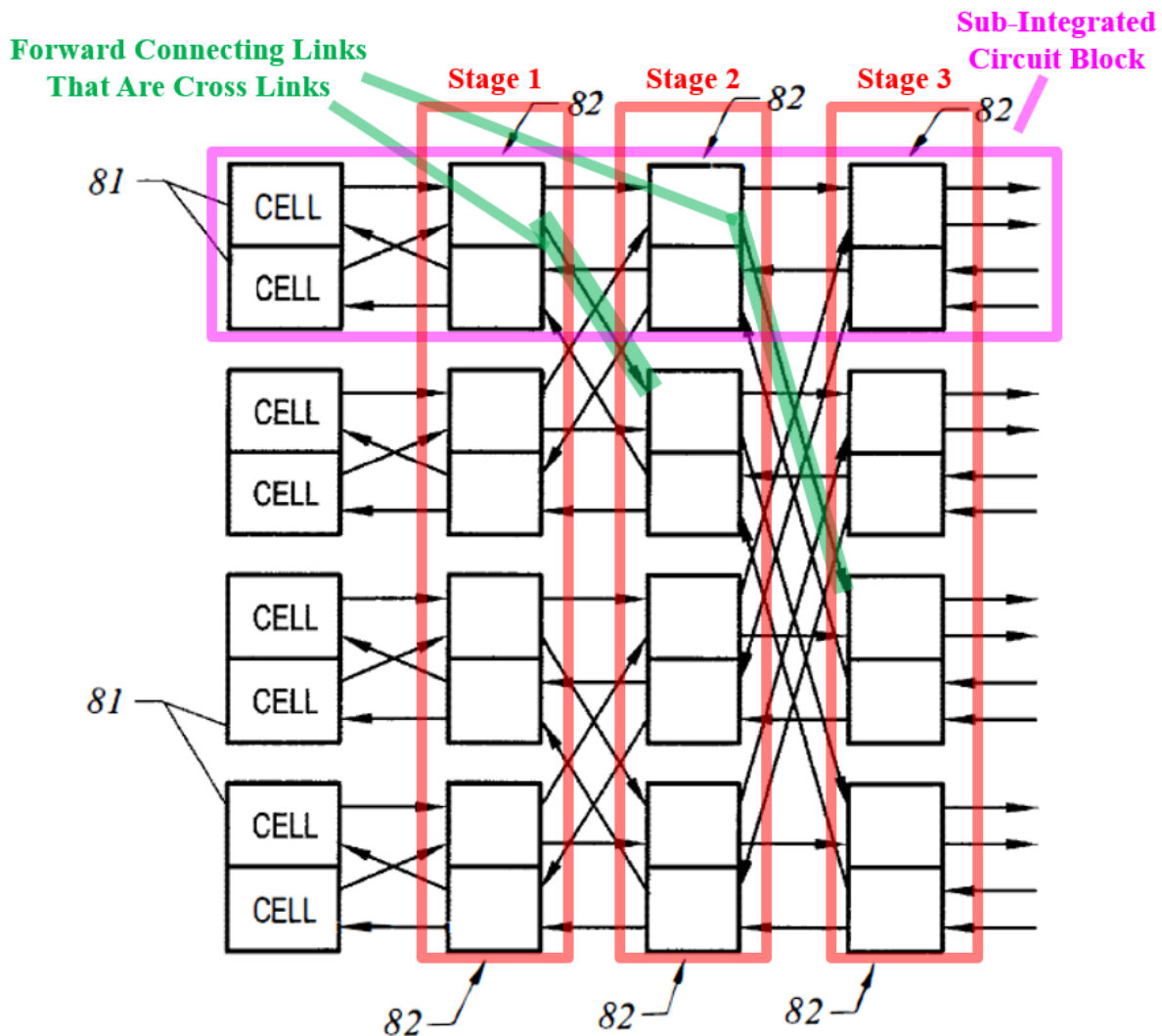


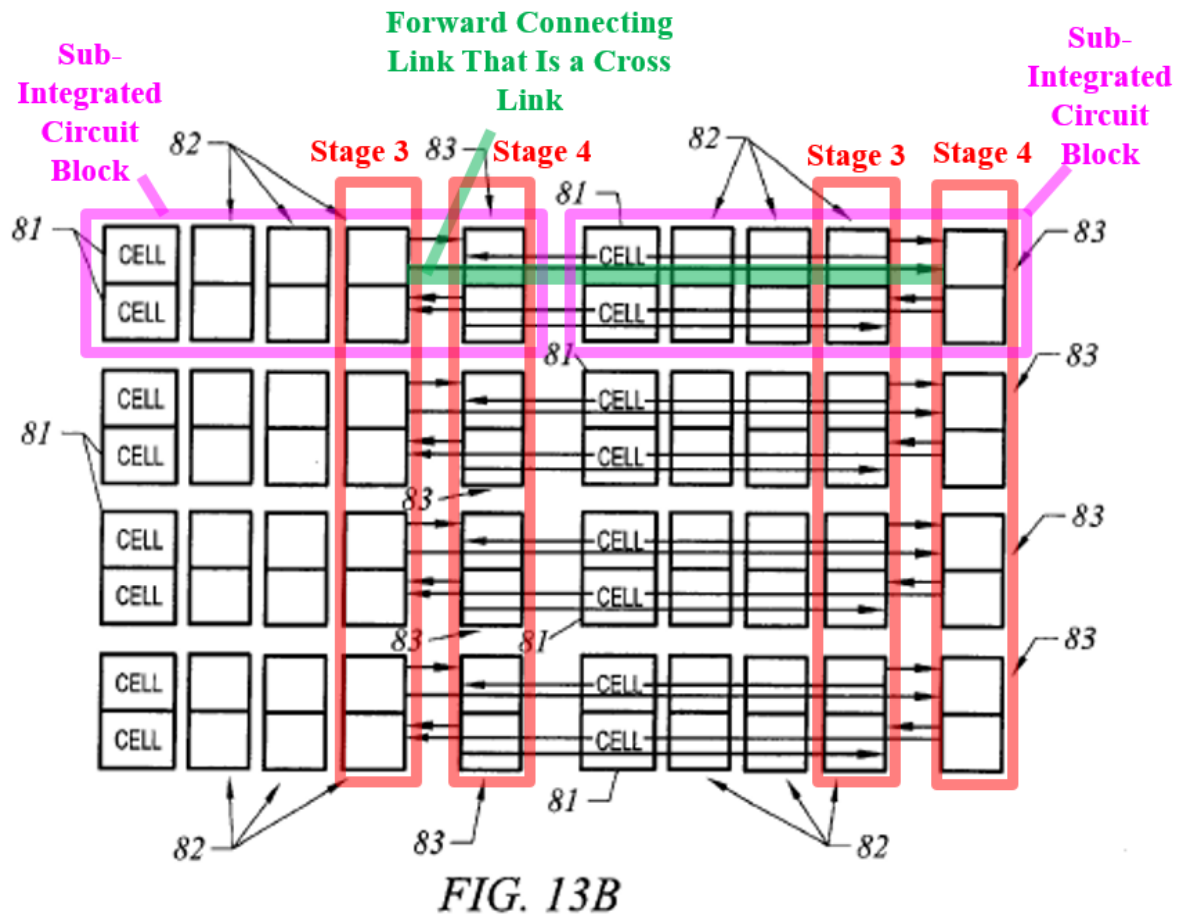
FIG. 13A

(Ex. 1008 at FIG. 13A (annotated to show forward connecting links that are cross links (green) between different sub-integrated circuit blocks (purple)).)

102. While the annotations above are only used to highlight the forward connecting links that are cross links for the top sub-integrated circuit block, a person of ordinary skill in the art would have recognized that figure 13A demonstrates that

each of the sub-integrated circuit blocks includes a plurality of forward connecting links that are cross links.

103. The embodiment in figure 13B of *Wong* also discloses that each sub-integrated circuit block includes “a plurality cross links in said forward connecting links from switches in said each lower stage to switches in its immediate succeeding higher stage.” For example, the cross links included in figure 13A annotated above are also present in the figure 13B embodiment between the top-left sub-integrated circuit block and other sub-integrated circuit blocks in the same column. Furthermore, figure 13B adds an additional forward-connecting cross link for each sub-integrated circuit block. As shown in the annotated figure 13B below, there is an additional forward connecting link that is a cross links for the top-left sub-integrated circuit block that is from stage 3 to stage 4 between the top-left sub-integrated circuit block and the sub-integrated circuit block directly to the right in the second column.



(Ex. 1008 at FIG. 13B (annotated to show forward connecting links that are cross links (green) from stage 3 to stage 4 between different sub-integrated circuit blocks (purple)).)

- (3) “[Said each sub-integrated circuit block . . .] further comprising a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage and”

104. In addition to the forward connecting links including straight and cross links, the backward connecting links in *Wong* also include straight and cross links

as recited in claim 1. For example, as shown in annotated figure 13A below, *Wong* discloses “a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage.” Annotated figure 13A below shows a plurality of straight links in the backward connecting links for the top sub-integrated circuit block, where the plurality of straight links includes a straight link from stage 2 to stage 1 and another straight link from stage 3 to stage 2.

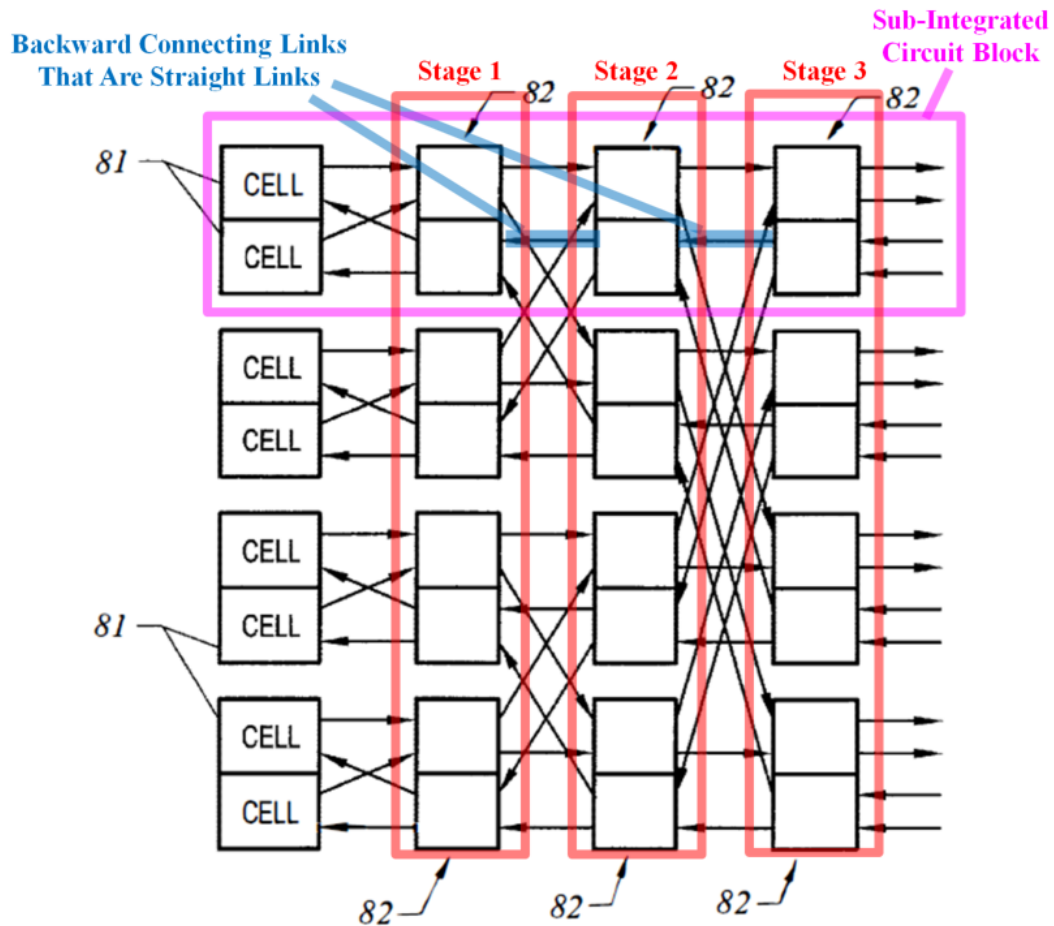
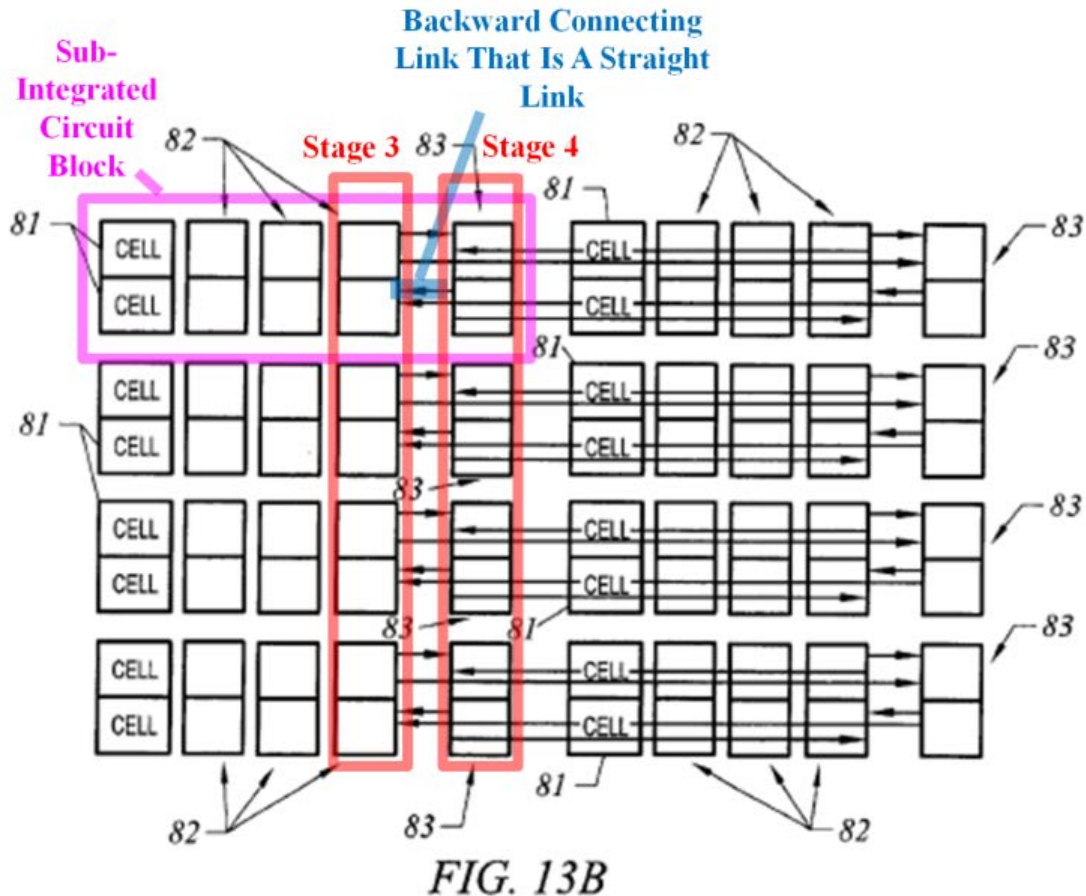


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated to show backward connecting links that are straight links (blue) in the top sub-integrated circuit block (purple)).)

105. While the annotations above are only used to highlight the straight links in the top sub-integrated circuit block, a person of ordinary skill in the art would have understood that figure 13A shows that each of the sub-integrated circuit blocks includes a plurality of backward connecting links that are straight links.

106. In addition to the embodiment of figure 13A of *Wong* disclosing the claimed feature, figure 13B also discloses that each sub-integrated circuit block includes “a plurality of straight links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage.” In addition to the backward connecting links that are straight links included in figure 13A discussed immediately above, which are also present in the figure 13B embodiment, figure 13B adds an additional backward connecting link that is a straight link for each sub-integrated circuit block. As shown in annotated figure 13B below, the depicted embodiment includes an additional backward connecting link that is a straight link for each sub-integrated circuit block. In the annotated figure 13B below, the additional straight link highlighted in blue is from stage 4 to stage 3 for the top-left sub-integrated circuit block.



(Ex. 1008 at FIG. 13B (annotated to show a backward connecting link that is a straight link (blue) from stage 4 to stage 3 in the top-left sub-integrated circuit block (purple)).)

- (4) “[Said each sub-integrated circuit block comprising . . .] a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage”

107. In addition to backward connecting links that are straight links, *Wong* also discloses backward connecting links that are cross links. As shown in annotated

figure 13A below, *Wong* discloses that each sub-integrated circuit block includes “a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage.” The plurality of backward-connecting cross links for the top sub-integrated circuit block in figure 13A are highlighted below, where the plurality of cross links includes cross links from stage 2 to stage 1 and cross links from stage 3 to stage 2. As shown in annotated figure 13A below, the cross links are links which connect switches in different rows (corresponding to different sub-integrated circuit blocks).

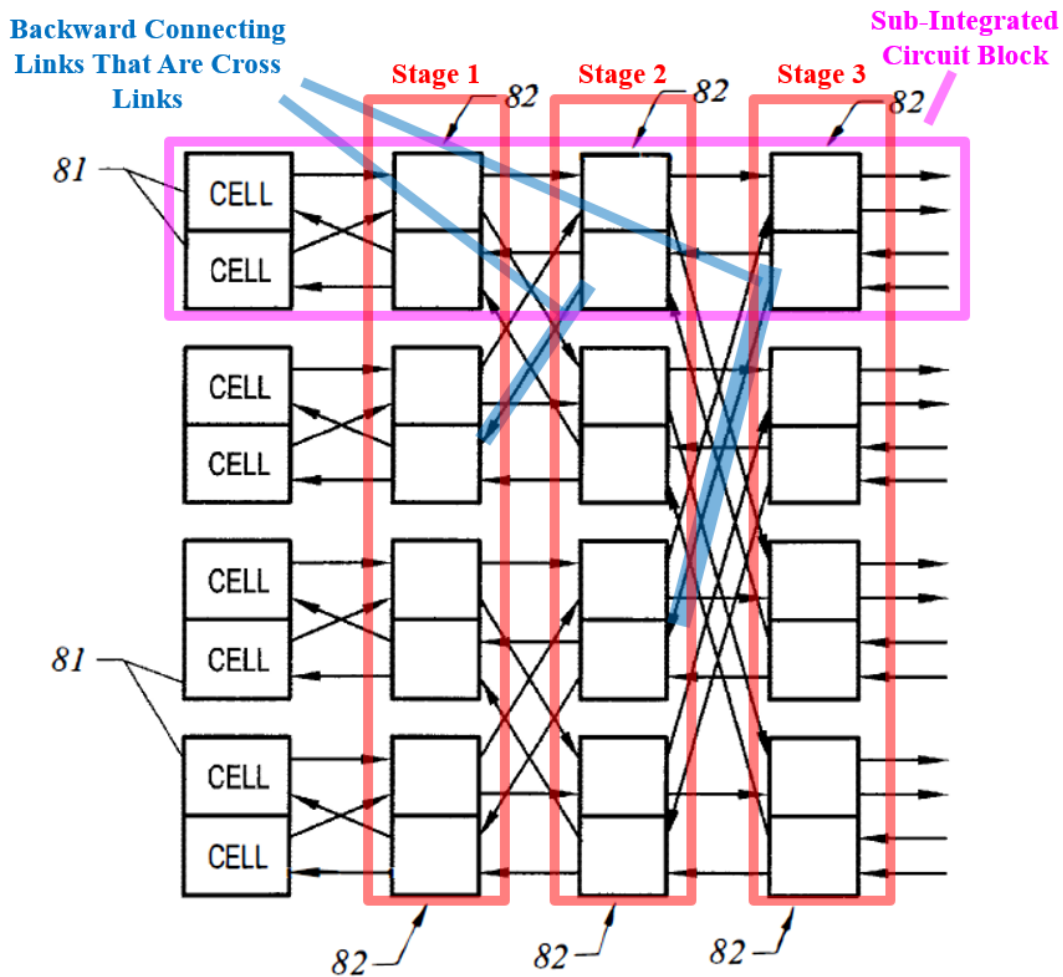


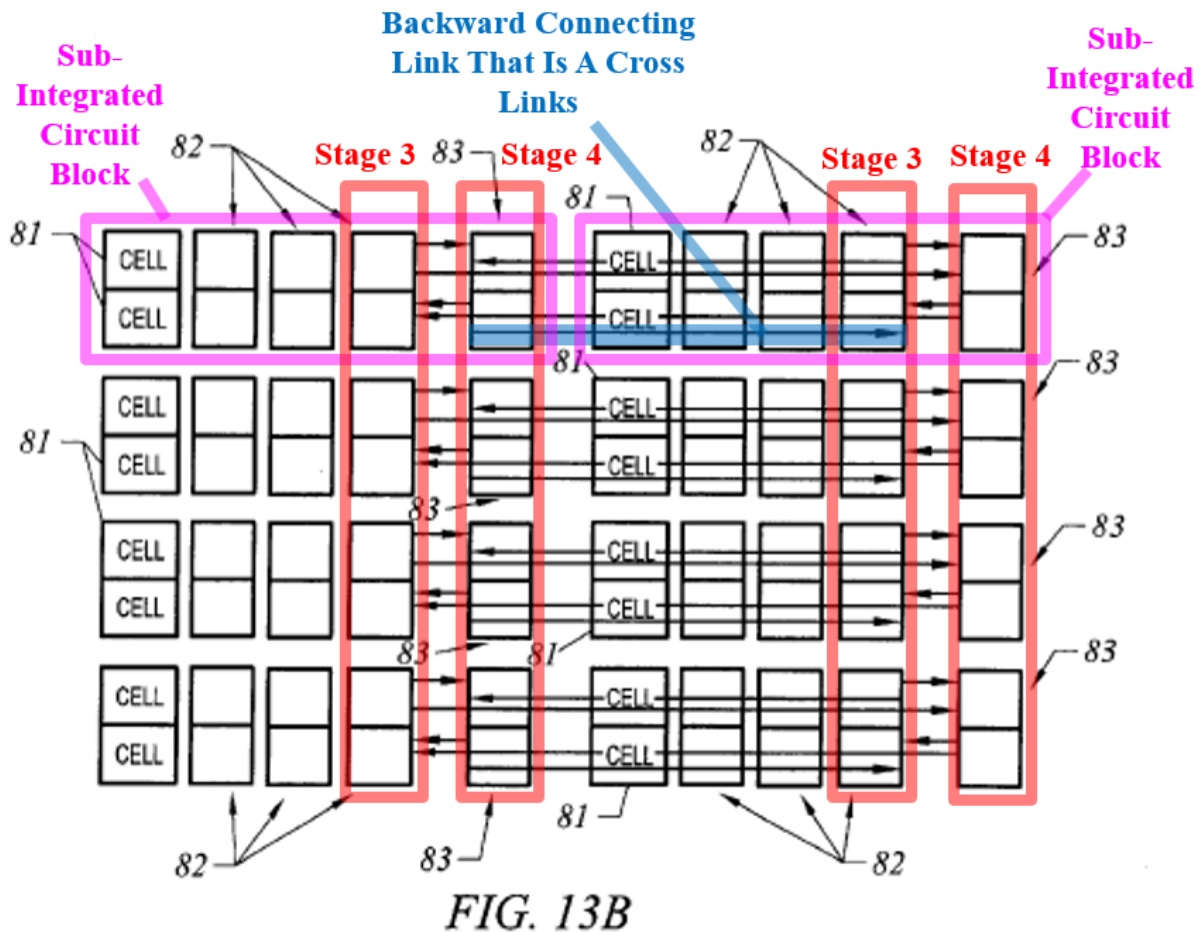
FIG. 13A

(Ex. 1008 at FIG. 13A (annotated to show backward connecting links that are cross links (blue) between different sub-integrated circuit blocks (purple)).)

108. While the annotations above are only used to highlight the backward connecting links that are cross links for the top sub-integrated circuit block, a person of ordinary skill in the art would have understood that figure 13A discloses that each

of the sub-integrated circuit blocks includes a plurality of backward connecting links that are cross links.

109. The embodiment depicted in figure 13B of *Wong* also discloses that each sub-integrated circuit block includes “a plurality of cross links in said backward connecting links from switches in said each higher stage to switches in its immediate preceding lower stage.” For example, the backward connecting links that are cross links shown above in figure 13A annotated above are also present in the figure 13B embodiment between the top-left sub-integrated circuit block and sub-integrated circuit blocks in the same column. Furthermore, the embodiment shown in figure 13B adds an additional backward-connecting cross link for each sub-integrated circuit block. As shown in annotated figure 13B below, there is an additional backward connecting link that is a cross links for the top-left sub-integrated circuit block. The additional cross link is from stage 4 to stage 3 between the top-left sub-integrated circuit block and the sub-integrated circuit block directly to the right in the second column.



(Ex. 1008 at FIG. 13B (annotated to show backward connecting links that are cross links (blue) from stage 4 to stage 3 between the two top-row sub-integrated circuit blocks (purple)).)

- i) “said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns, and”

110. In my opinion, *Wong* discloses this feature. For example, figures 13A and 13B of *Wong* disclose the “plurality of sub-integrated circuit blocks” identified above with respect to claim element 1(b) arranged in rows and columns. Figure 13A

of *Wong* shows the sub-integrated circuit blocks arranged in four rows in a single column (“plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns”).

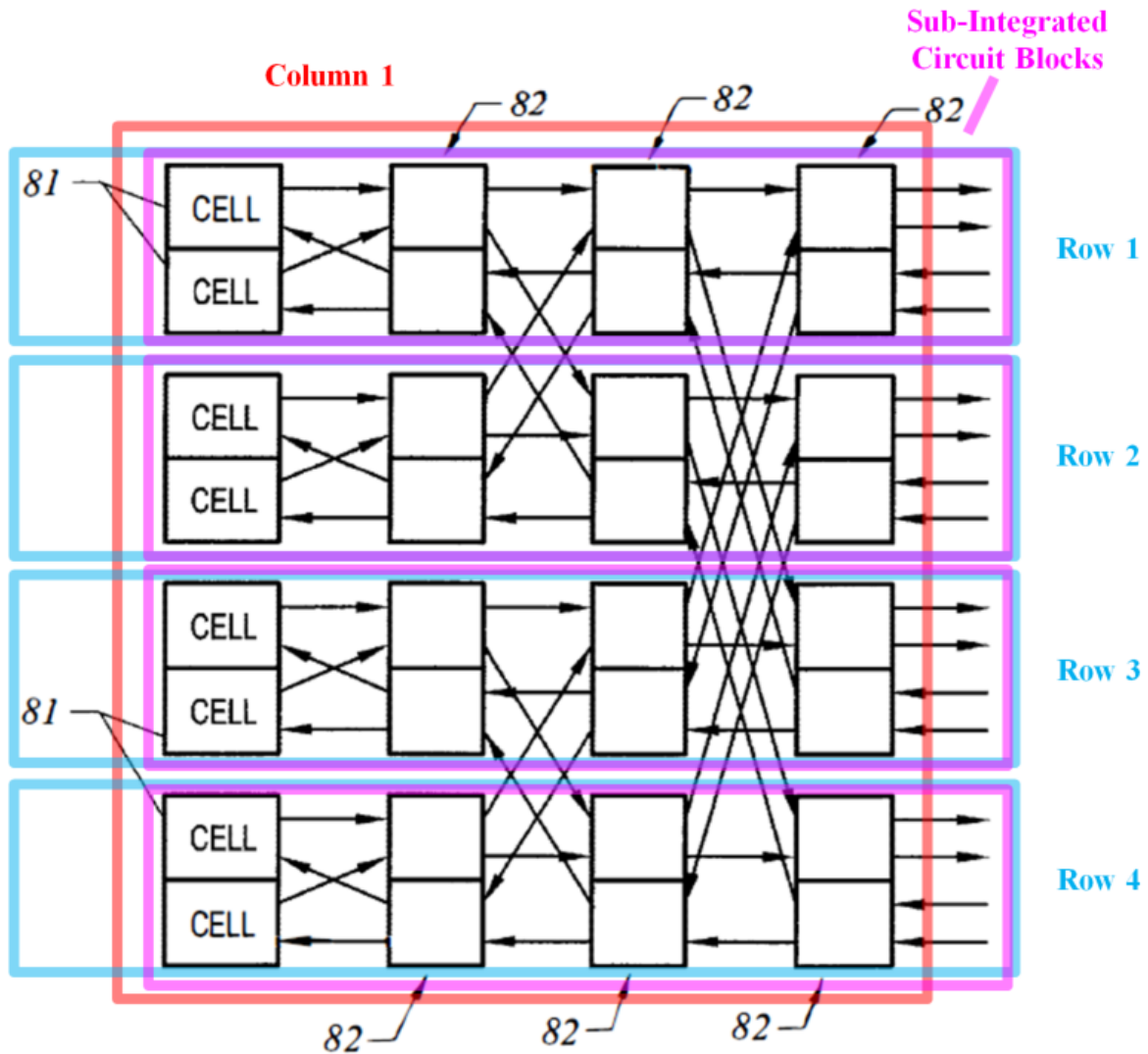


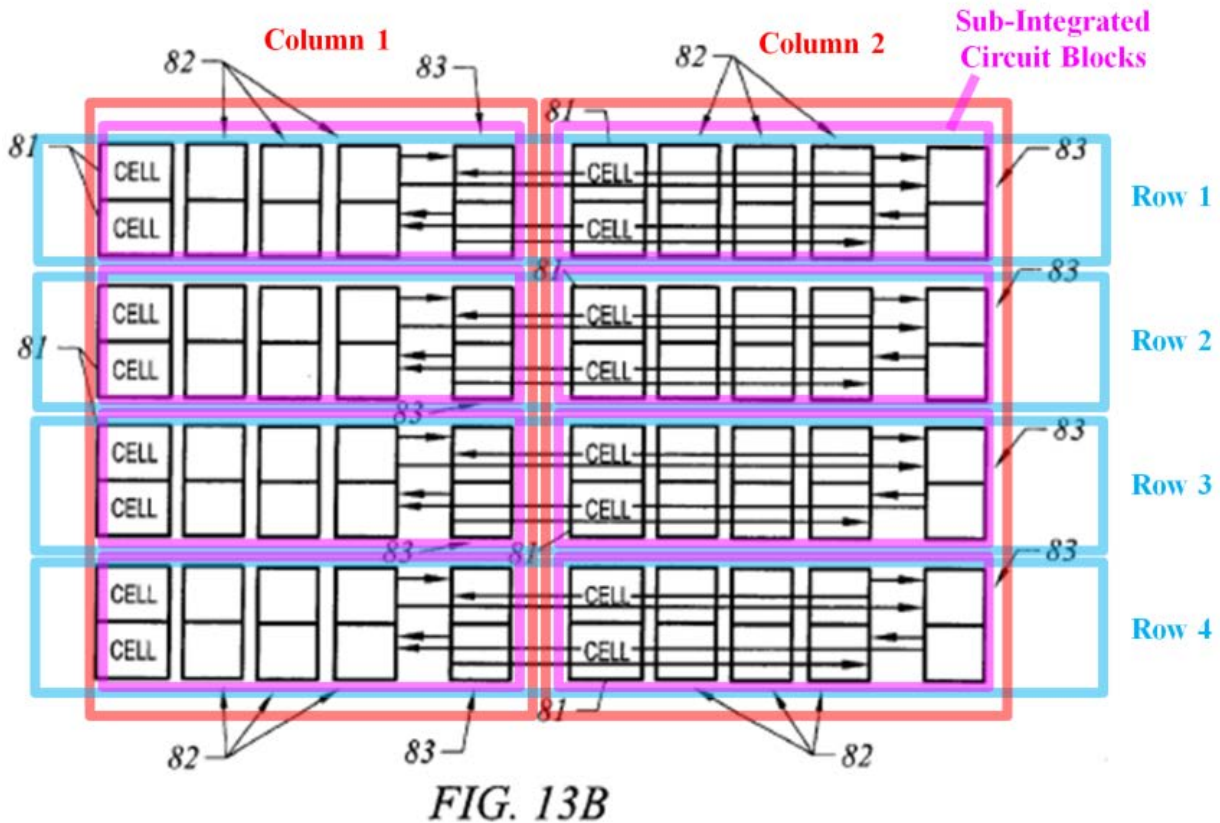
FIG. 13A

(Ex. 1008 at FIG. 13A (annotated).)

111. I have been asked to assume that Patent Owner may contend that claim 1 requires a two-dimensional grid of rows and columns that includes both multiple rows and multiple columns of sub-integrated circuit blocks. I disagree with such an interpretation as it conflicts with other claims in a related patent. Specifically, claim 1 of U.S. Patent No. 10,050,904 (“the ’904 patent”) (Ex. 1046), which incorporates the ’523 patent by reference (Ex. 1046 at 2:20-24) and lists the same inventor as the ’523 patent, recites a plurality of subnetworks “arranged in a two-dimensional grid of rows and columns” (*id.* at 69:25-27). Claim 10 of the ’904 patent, which depends from claim 1, further recites that “said plurality of subnetworks are implemented in a single dimension.” (*Id.* at 71:11-12.) Based on my review of the ’904 patent, in the ’904 patent, the term “subnetwork” maps to a row of switches in the same manner as the “sub-integrated circuit block” does in the ’523 patent. A person of ordinary skill in the art would have recognized that claim 10 of the ’904 patent demonstrates that claim 1 of the ’904 patent is broad enough to encompass a two-dimensional grid where the subnetworks are only laid out in a single dimension (e.g., one row or one column). Therefore, in my opinion, claims 1 and 10 (and claims 11 and 18, which include similar features) of the ’904 patent support the understanding that figure 13A of *Wong*, which has multiple rows in a single column, discloses “said plurality of

sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns” as recited in claim 1 of the ’523 patent.

112. Moreover, the embodiment shown in figure 13B of *Wong* shows the “plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns,” where the embodiment of figure 13B includes multiple rows and multiple columns.



(Ex. 1008 at FIG. 13B (annotated).)

113. Figure 13B of *Wong* includes two instantiations of the layout shown in figure 13A (Ex. 1008 at 3:7-10, 13:36-38), and figure 13B discloses an embodiment

that has a plurality of columns (*id.* at 13:33-36 (“For multiple column arrays, levels of switch cells are added to each column’s sub-network.”)). The embodiment shown in figure 13B of *Wong* shows the sub-integrated circuit blocks arranged in four rows and two columns (“plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns”).

114. Notably, *Wong* also discloses that further expansion of the network is contemplated to provide additional columns in the network. (Ex. 1008 at 13:38-40 (“For each additional doubling of the number of cell columns, an additional column of switch cells must be added to each of the cell columns”).) *Wong* further states that “[t]he strength of this column floorplan is that **the number of cells in a column can be any power of 2, and the number of rows can also independently be any power of 2.**” (Ex. 1008 at 13:44-46 (emphasis added).)

115. I have been told to assume that Patent Owner may argue that the two-dimensional grid of rows and columns recited in claim 1 corresponds to a physical layout of the sub-integrated circuit blocks on an integrated circuit. While I disagree with such a narrow view of the claim language, *Wong* indicates that figures 13A and 13B correspond to such a physical layout, and therefore *Wong* discloses the claim feature even under such a narrow interpretation. Specifically, *Wong* discloses two floorplans “to map the topology of the present invention’s interconnect network onto

a physical layout, i.e., on the surface of the substrate of an integrated circuit.” (Ex. 1008 at 13:13-16.) “The most straightforward mapping is column-based. With the previous illustrations of the Benes interconnect network and columns of logic cells added, the layout is nearly completed. See FIG. 13A.”⁵ (Ex. 1008 at 13:19-22.) Therefore, figures 13A and 13B correspond to the physical arrangement of the sub-integrated circuit blocks on the integrated circuit.

116. A person of ordinary skill in the art would also have recognized that figure 14A of *Wong* also supports the understanding that figures 13A and 13B of *Wong* correspond to physical layouts. Figure 14A “shows a 16 logic cell column floorplan (the same as shown in figure 13B) with the cells labeled for identification” (*id.* at 13:60-62) that arranges the sub-networks in a two-dimensional grid of rows and columns.

⁵ In the “Background of the Invention” section, the ’523 patent concedes that “[t]he most commonly used VLSI layout in an integrated circuit is based on a two-dimensional grid model comprising only horizontal and vertical tracks.” (Ex. 1001 at 2:40-42.)

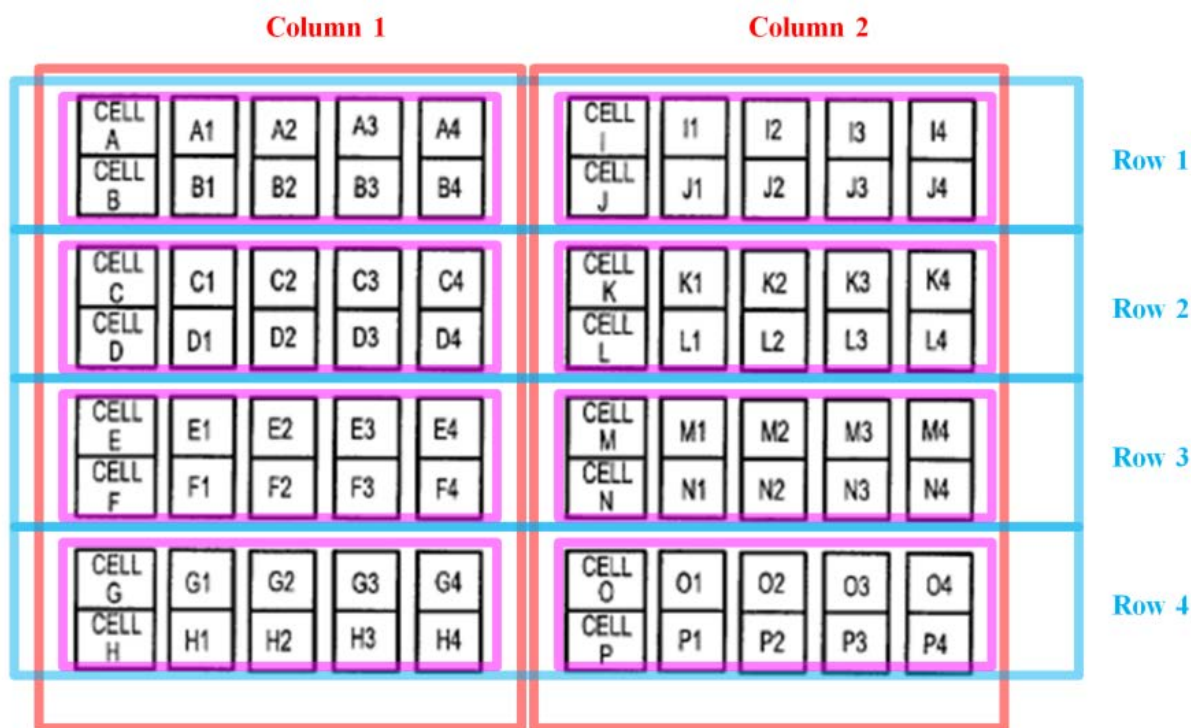


FIG. 14A

(Ex. 1008 at FIG. 14A (annotated).)

117. Notably, during prosecution of the application that led to the '523 patent, Patent Owner argued that *Wong* uses a “[c]olumn-based layout,” which was alleged to be different from the “2D-grid in row-column layout” of the '523 patent. (Ex. 1004 at 62.) As shown above in figure 14A of *Wong*, the column-based layout is a 2D grid of rows and columns. Patent Owner further asserted during prosecution that, related to the “2D-grid in row-column layout,” a “[k]ey insight in the disclosure is to arrange the sub-integrated circuits in a hypercube topology.” (*Id.* at 62.)

However, a person of ordinary skill in the art would have recognized that no such “hypercube topology” is recited in claim 1.

- j) **“said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right,”**

118. In my opinion, *Wong* discloses this feature. As I discussed above with respect to claim limitations 1(h)(1) and 1(h)(3), all of the straight links in the network connect switches within the same sub-integrated circuit block (“said all straight links are connecting from switches in each said sub-integrated circuit block to switches in the same integrated circuit block”). (See my analysis above in Sections IX.A.1(h)(1), IX.A.1(h)(3).) Annotated figure 13A below shows the straight links for the top sub-integrated circuit block, where all of the straight links connect switches in the same sub-integrated circuit block.

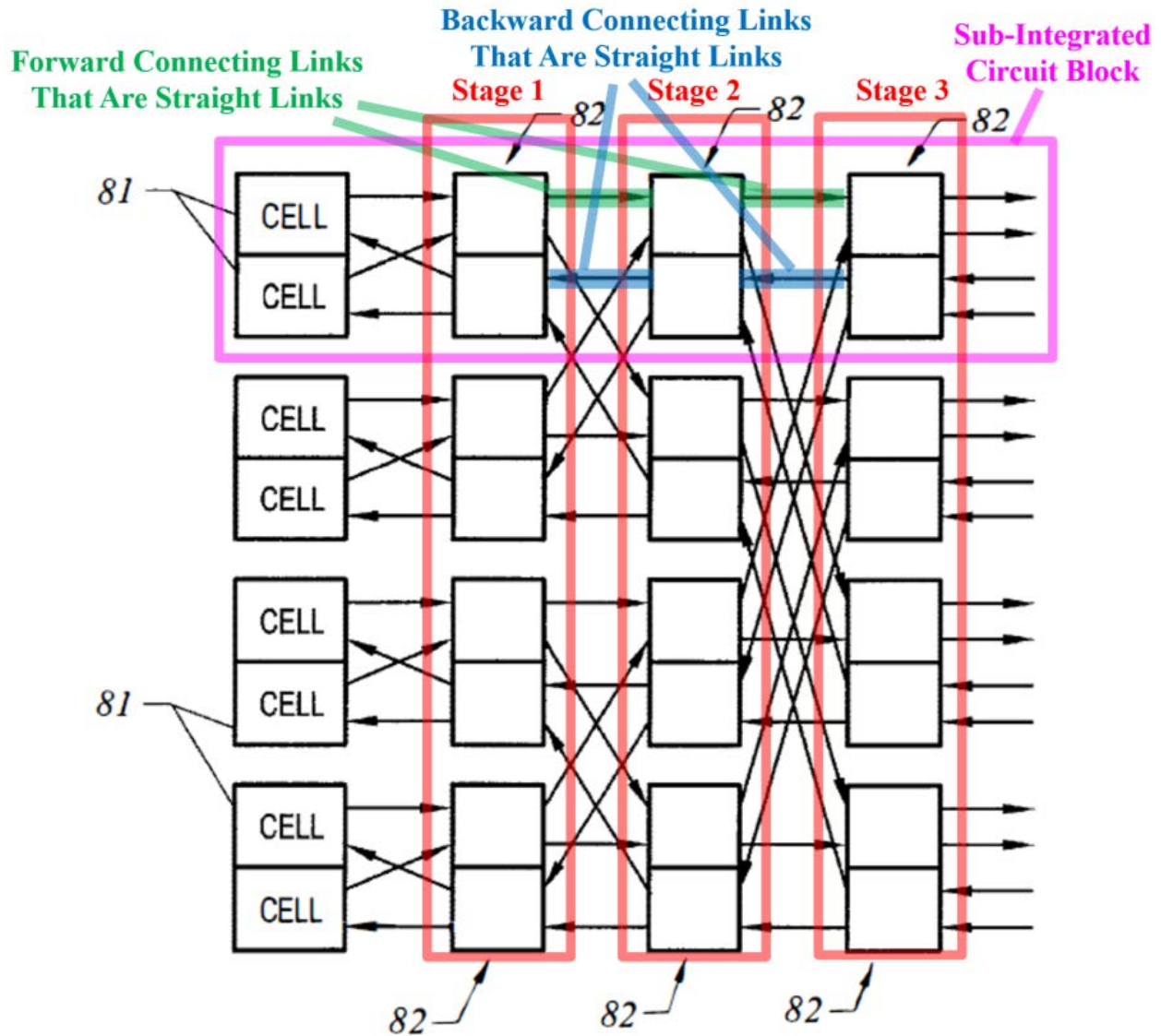
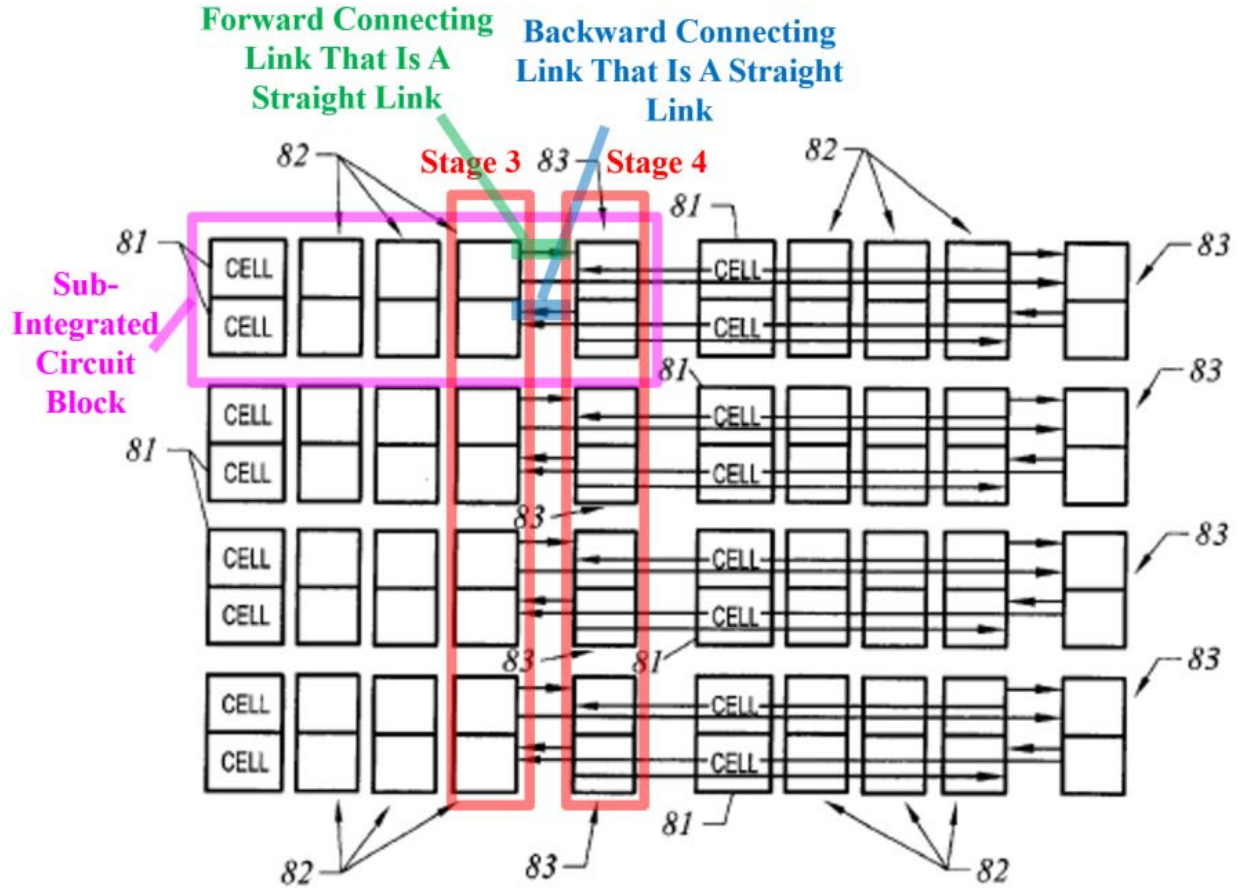


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated to straight links (green and blue) in the top sub-integrated circuit block (purple)).)

119. Similarly, the embodiment shown in figure 13B of *Wong* also discloses that all straight links in the network connect switches within the same sub-integrated

circuit block (“said all straight links are connecting from switches in each said sub-integrated circuit block to switches in the same integrated circuit block”). (*See my analysis above in Sections IX.A.1(h)(1), IX.A.1(h)(3).*) Annotated figure 13B below shows the additional straight links for the top-left sub-integrated circuit block. Notably, figure 13B also includes the straight links highlighted above with respect to the embodiment of figure 13A, which is replicated to form the network of figure 13B. (Ex. 1008 at 13:36-38.)



(Ex. 1008 at FIG. 13B (annotated to straight links (green and blue) in the top-left sub-integrated circuit block (purple)).)

120. *Wong* further discloses the claimed feature “said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right.” As discussed above with respect to claim feature 1(i), in both the figure 13A and 13B embodiments, the plurality of sub-integrated circuit blocks are arranged in a two-dimensional array of rows and

columns. (See my discussion above in Section IX.A.1(i).) With respect to the embodiment shown in figure 13A, all of the cross links are implemented as vertical links between switches in different sub-integrated circuit blocks that are placed vertically above or below each other.

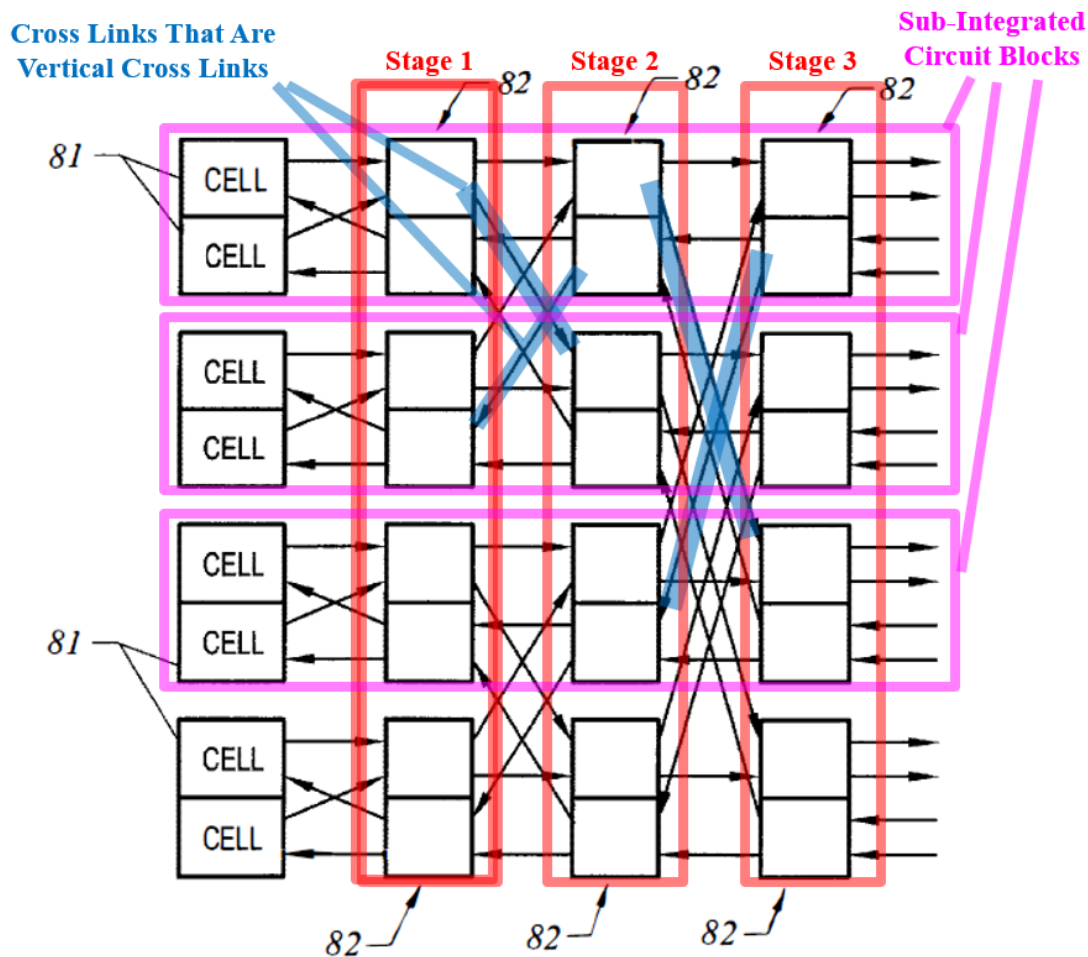
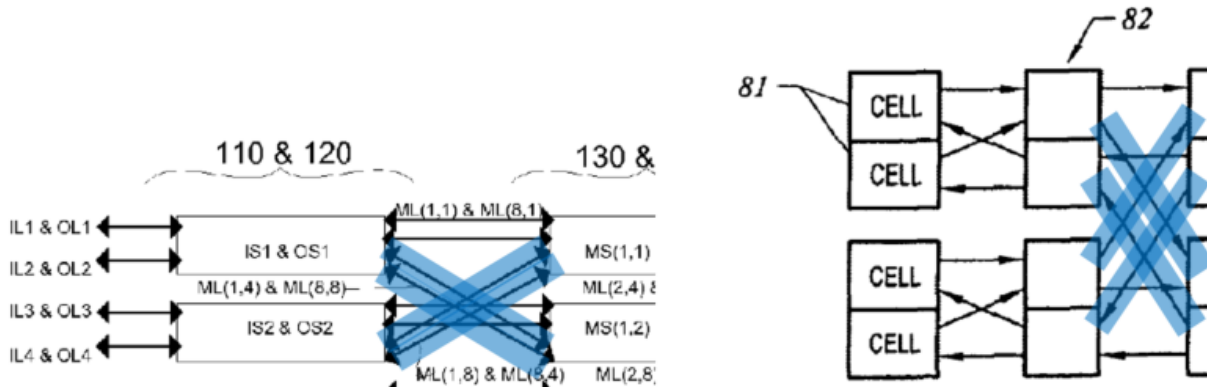


FIG. 13A

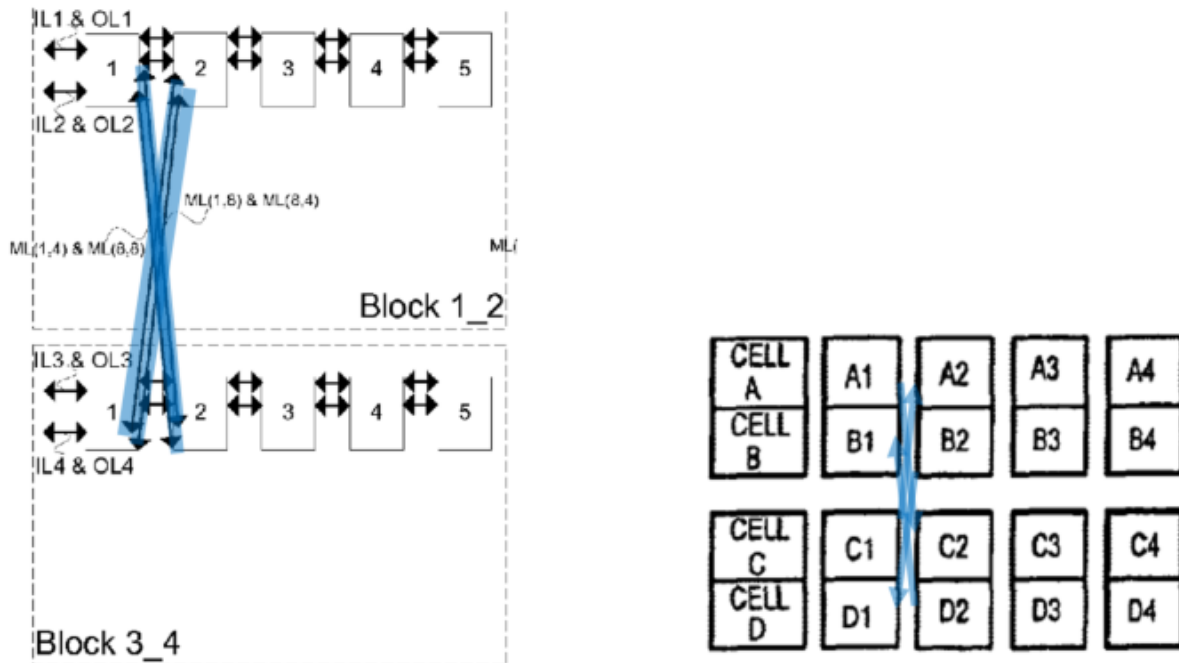
(Ex. 1008 at FIG. 13A (annotated to show vertical cross links (blue) for the top sub-integrated circuit block.)

121. *Wong's* disclosure of cross links between different sub-integrated circuit blocks in figure 13A being implemented as “vertical links . . . between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below” is consistent with the disclosure of the '523 patent.⁶ For example, as shown in the annotated excerpts of figures 13A and 14A of *Wong* below, the cross links between stages 1 and 2 constitute vertical links between switches in two different sub-integrated circuit blocks placed vertically above or below each other in the same manner as the cross links shown in annotated excerpts of figures 1B and 1D of the '523 patent.

⁶ The '523 patent acknowledges that “[t]he most commonly used VLSI layout in an integrated circuit is based on a two-dimensional grid model comprising only horizontal and vertical tracks.” (Ex. 1001 at 2:40-42.) The '523 patent also states that “[w]hen large scale sub-integrated circuit blocks with inlet and outlet links are layed out in an integrated circuit device in a two-dimensional grid arrangement, (for example in an FPGA where the sub-integrated circuit blocks are Lookup Tables) the most intuitive routing network is a network that uses horizontal and vertical links only” (*Id.* at 3:12-17.)



(Ex. 1001 at FIG. 1B (excerpt, annotated); Ex. 1008 at FIG. 13A excerpt, annotated).)



(Ex. 1001 at FIG. 1D (excerpt, annotated); Ex. 1008 at FIG. 14A excerpt, annotated).)

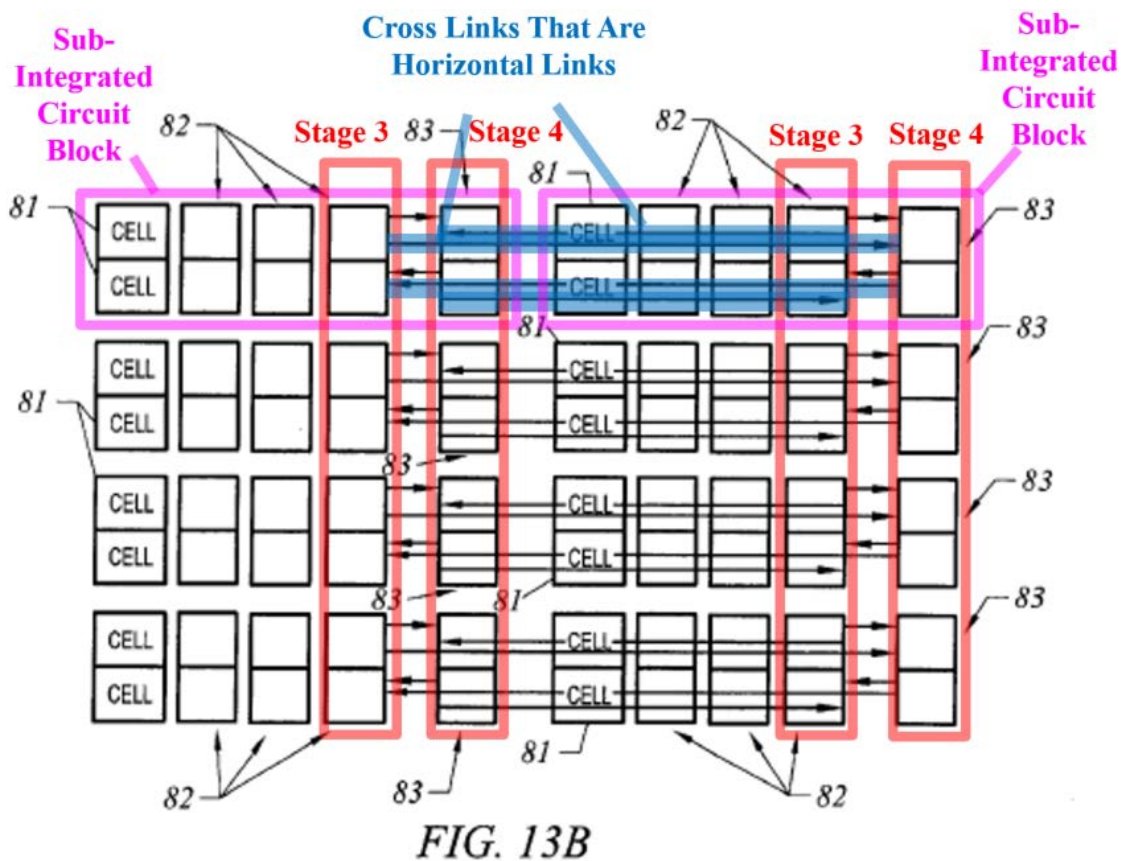
122. As shown in the annotated excerpts above, *Wong*'s figure 13A network and two-dimensional row-column layout shown in figure 14A includes vertical cross links between stages 1 and 2 of two sub-integrated circuit blocks that are placed above and below one another in the same manner as that shown in the annotated excerpts of figures 1B and 1D of the '523 patent. According to the '523 patent, figure 1D shows the inter-block links ("cross links") as vertical links between switches that are placed vertically above or below each other:

Applicant notes that in the layout 100C of FIG. 1C, the inter-block links between switch 1 and switch 2 of corresponding blocks are **vertical tracks** as shown in layout 100D of FIG. 1D.

(Ex. 1001 at 15:9-12 (emphasis added).)

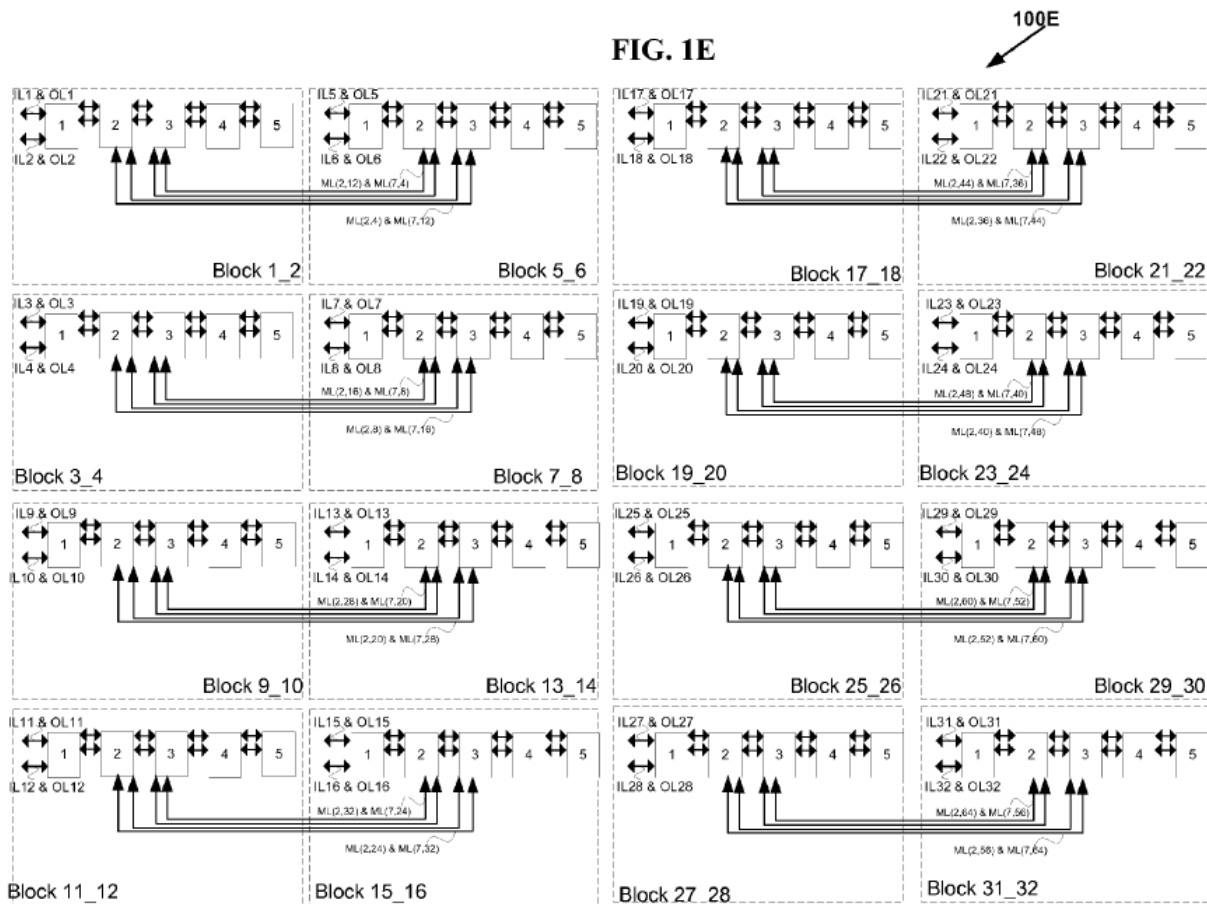
123. In the embodiment shown in figure 13B of *Wong*, the cross links between stages 1 and 2 and between stages 2 and 3 are implemented as vertical links between switches in two different sub-integrated circuit blocks placed vertically above or below each other in the same manner as shown in figure 13A. That is because figure 13B includes two instantiations of the network of switches shown in figure 13A. (Ex. 1008 at 13:36-38.) In addition to those vertical cross links, the cross links between stages 3 and 4 in the network of figure 13B are implemented as

“horizontal links between switches in two different said sub-integrated circuit blocks which are . . . placed horizontally to the left or to the right” of each other. Indeed, Patent Owner conceded that figure 13B of *Wong* shows horizontal links during prosecution. (Ex. 1008 at FIGs. 13A, 13B; Ex. 1004 at 63 (“As disclosed in Fig. 13B, columns are doubled by adding one more stage of switches in both the columns (for example Fig. 13A is replicated to get Fig. 13B and a new stage of switches 83 are added and **the cross links between the new stage of switches in the two columns become horizontal links**).”) (emphasis added).)



(Ex. 1008 at FIG. 13B (annotated).)

124. Such an understanding is also consistent with the '523 patent's description of the cross links in figures 1E and 1G being "horizontal tracks." (Ex. 1001 at 15:9-19, FIGs. 1E and 1G.)



(*Id.* at FIG. 1E.)

125. Therefore, the embodiment shown in figure 13B of *Wong* also discloses that all of the cross links are implemented as horizontal links between switches in two different sub-integrated circuit blocks that are placed horizontally to the left or to the right of each other or vertical links between switches in two different

sub-integrated circuit blocks that are placed vertically above or below each other. Specifically, the cross links between stages 1 and 2 and between stages 2 and 3 are vertical links between switches in two different sub-integrated circuit blocks that are placed vertically above or below each other, whereas the cross links between stages 3 and 4 are horizontal links between switches in two different sub-integrated circuit blocks that are placed horizontally to the left or to the right of each other.

126. During prosecution of the '523 patent, Patent Owner argued that *Wong* did not disclose this feature. Specifically, Patent Owner argued that the entirety of figure 13A of *Wong* constitutes a “sub-integrated circuit block” and is the “basic building block of the column-based layout.” (Ex. 1004 at 62-63.) Based on that contention, Patent Owner further argued that the sub-integrated circuit block that includes all of the switches in figure 13A “has cross links connected between switches of two succeeding stages within the same sub-integrated circuit.” (*Id.*) I disagree with Patent Owner’s characterization of *Wong* during prosecution. As I demonstrated above with respect to claim limitation 1(b), each row of switches in the network shown in figure 13A of *Wong* constitutes a “sub-integrated circuit block” in a manner consistent with how that term is used in the context of the '523 patent. (*See* my analysis above in Section IX.A.1(b).) Because each row of switches is a sub-integrated circuit block, and not the entire network structure shown in figure

13A as Patent Owner argued during prosecution, each of the cross links between switches in figure 13A of *Wong* is between two different sub-integrated circuit blocks.

127. Moreover, Patent Owner's position that the entirety of figure 13A is a "sub-integrated circuit block" appears to be based on excerpted language from *Wong* taken out of context. Specifically, during prosecution Patent Owner cited to *Wong*'s disclosure of "[t]here are two logic cells 81 per switch cell 82, connected in the so called 'butterfly' pattern, consistent with the Benes network topology:" (Ex. 1004 at 62 (citing Ex. 1008 at 13:22-24).) Based on this excerpt, Patent Owner then alleged that the sub-integrated circuit block in *Wong* has cross links connected between switches in the same sub-integrated circuit block, "[o]therwise there will not be a butterfly pattern." (Ex. 1004 at 62-63.) But a person of ordinary skill in the art would have understood that Patent Owner's conclusion that there must be cross links in the same sub-integrated circuit block in *Wong* does not follow from the excerpted text from *Wong*. *Wong*'s statement about the "butterfly pattern" is not concerned with links between switches and instead corresponds to the connections between the logic cells 81 and the switches 82 in the first stage of the network:

There are two logic cells 81 per switch cell 82 connected in the so called “butterfly” pattern, consistent with the Benes network topology: More generally, an input-output pin-pair of a logic cells forms the leaves of the Benes interconnect network.

(Ex. 1008 at 13:22-26.)

128. A person of ordinary skill in the art would also have understood Patent Owner’s arguments during prosecution to be internally inconsistent. As discussed above, Patent Owner acknowledged during prosecution that figure 13A of *Wong* has cross links. (Ex. 1004 at 62-63 (“cross links connected between switches of two succeeding stages with in the same sub-integrated circuit”).) But based on the definition provided in the ’523 patent, cross links are between switches in different sub-integrated circuit blocks. (Ex. 1001 at 9:47-49.) If the entirety of figure 13A is one sub-integrated circuit block as Patent Owner asserted in attempting to argue over *Wong*, then there would not be any cross links in figure 13A of *Wong*, which is inconsistent with Patent Owner’s recognition that figure 13A of *Wong* has cross links.

129. Based on my review of the prosecution history, it appears that Patent Owner’s only basis for contending that claim limitation 1(j) is not disclosed by *Wong* was the assertion that the entirety of figure 13A constituted a “sub-integrated circuit

block.” As I noted above, I disagree with Patent Owner’s grouping of the plurality of rows of switches in figure 13A together to form a single “sub-integrated circuit block,” as such a grouping is inconsistent with how a person of ordinary skill in the art would have understood “sub-integrated circuit block” in view of the disclosure of the ’523 patent.

- k) **“each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid.”**

130. *Wong* discloses this feature. For example, figure 13A of *Wong*, discloses that each of the rows in the network (“sub-integrated circuit blocks”) has three stages (“same number of stages”). (*See* my discussion above in Section X.A.1(d).) Moreover, each of the sub-integrated circuit blocks has the same construction as the other sub-integrated circuit blocks, and therefore has the “same number of . . . said switches in each said stage.” (Ex. 1008 at FIGs. 4B, 4C, 13A-B, 14A.)

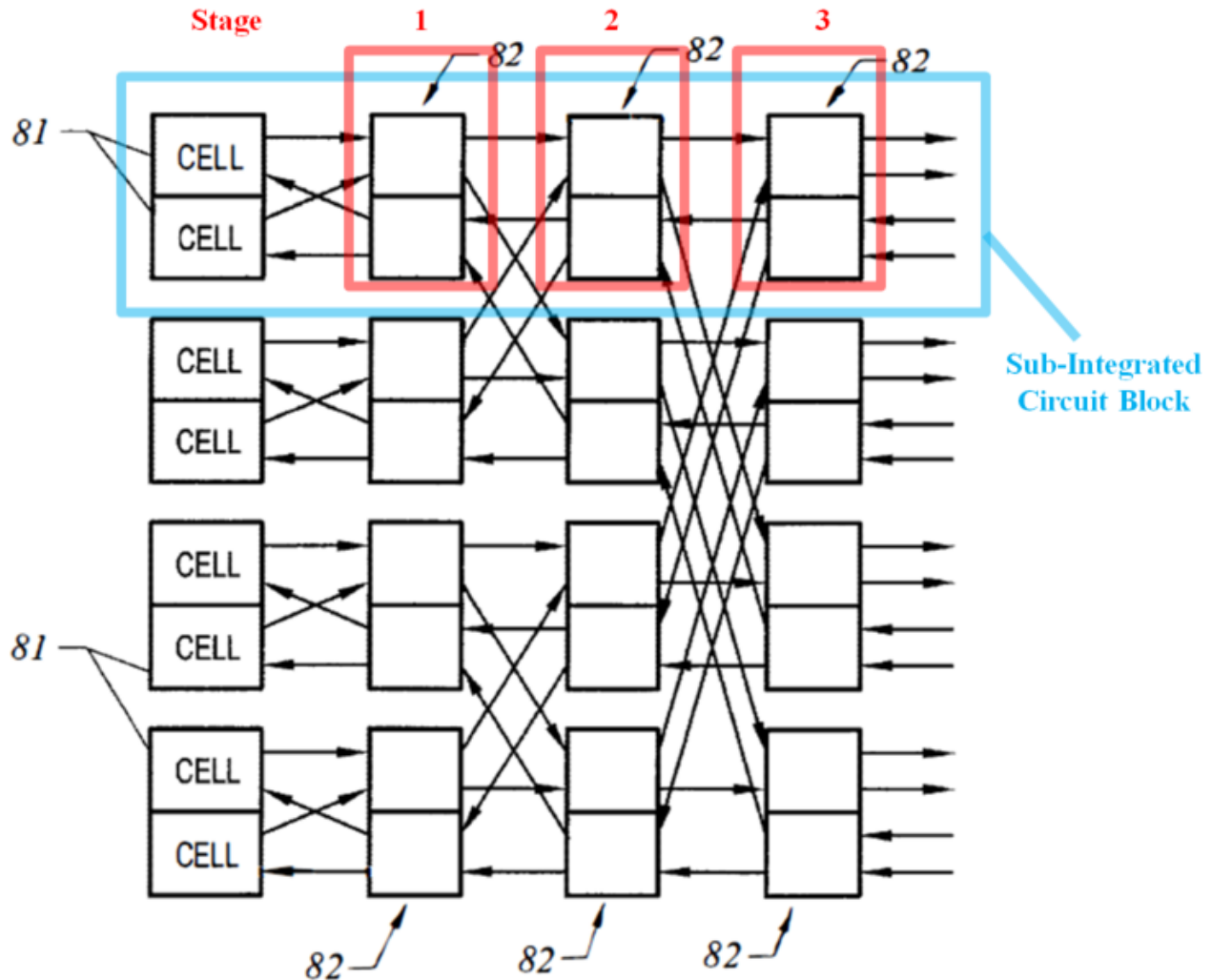
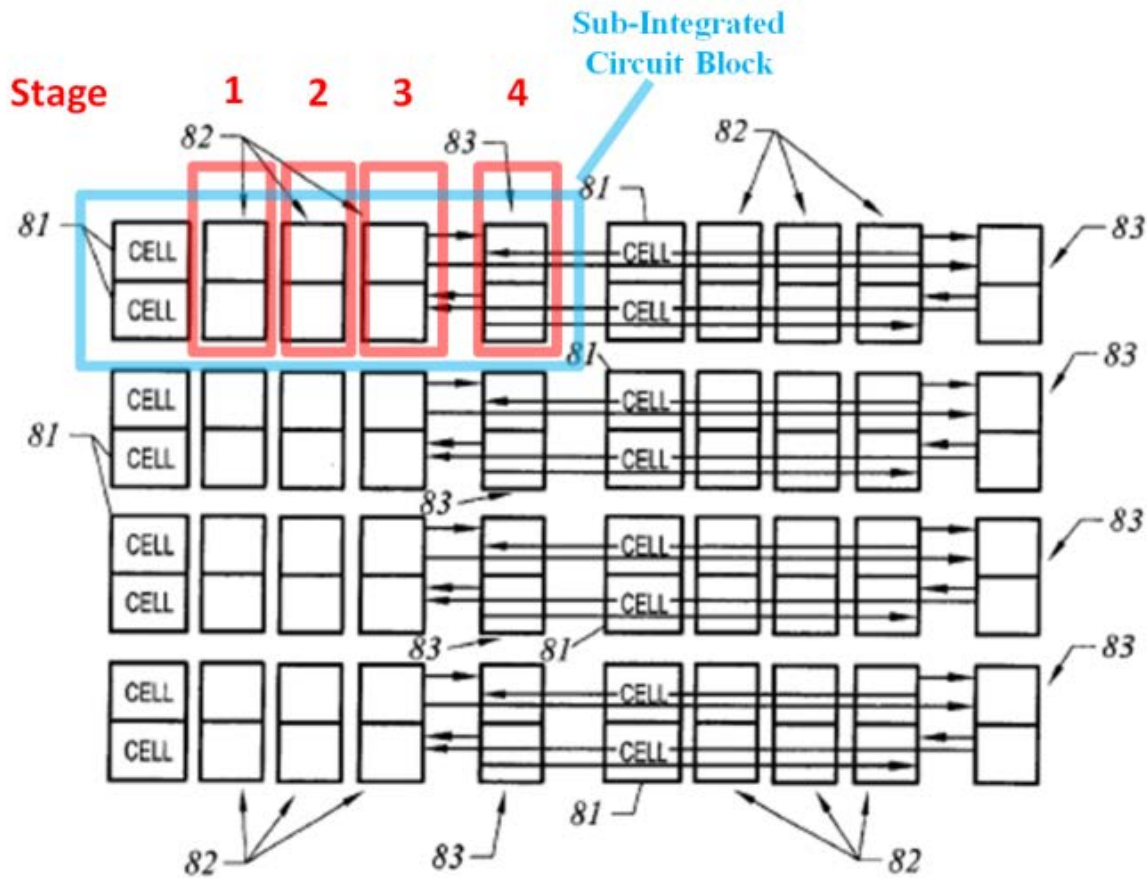


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated).)

131. Similarly, as shown in figure 13B of *Wong*, each sub-integrated circuit block includes four stages (“same number of stages”) and each of the sub-integrated circuit blocks has the same construction (“same number of . . . said switches in each said stage”). (See my discussion above in Section IX.A.1(e); Ex. 1008 at FIG. 13B.)



(Ex. 1008 at FIG. 13B (annotated).)

132. As further disclosed by *Wong*, each sub-integrated circuit block has the same configuration (same number of stages and same number of switches in each stage) regardless of the size of the network. For example, the network of figure 13A has a single column and each sub-integrated circuit block includes three stages:

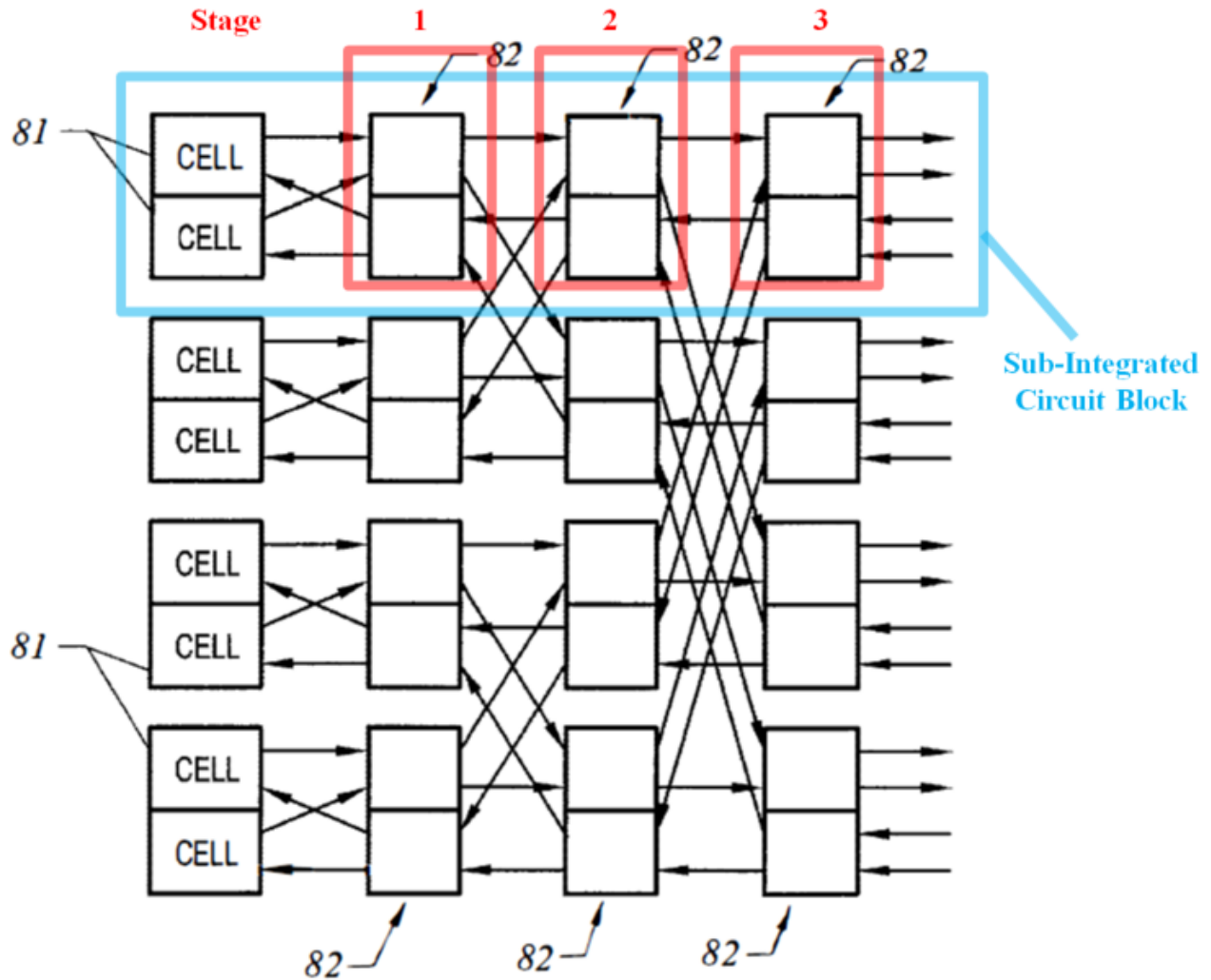


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated).)

133. Expanding the network of figure 13A by a power of two in the horizontal direction creates a second column and adds a fourth stage to each sub-integrated circuit block as is shown in figure 13B:

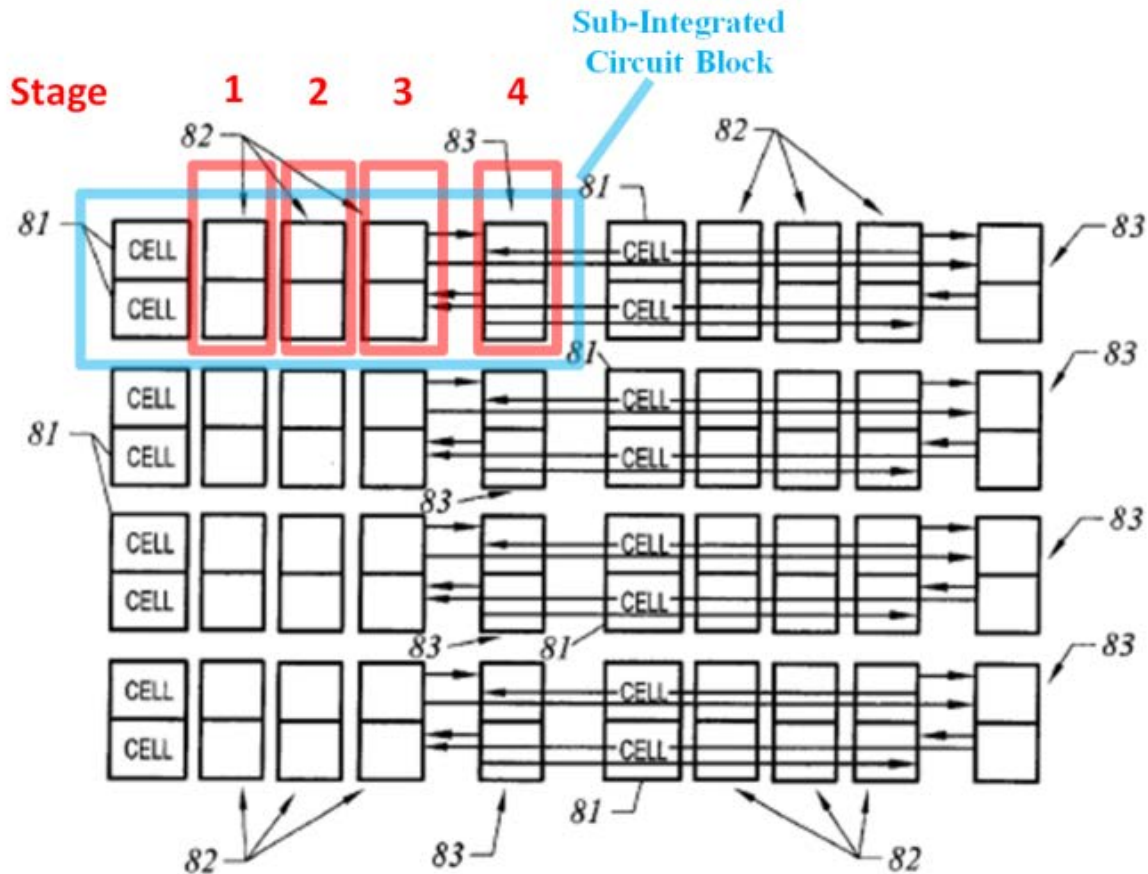


FIG. 13B

(Ex. 1008 at FIG. 13B (annotated).)

134. *Wong* further discloses that “[f]or each additional doubling of the number of cell columns, an additional column of switch cells must be added to each of the cell columns” (Ex. 1008 at 13:38-40.) Therefore, *Wong* discloses that “regardless of the size of said two-dimensional grid” “each said plurality of sub-

integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid.” In other words, *Wong* discloses that as the network is scaled up, each of the sub-integrated circuit blocks has the same construction as the other sub-integrated circuit blocks in the network. As demonstrated by the increase in size of the network in figure 13B in comparison to figure 13A, instantiations of the sub-integrated circuit blocks can be replicated both in the vertical (column) and horizontal (row) dimensions. (Ex. 1008 at FIGs. 13A, 13B.)

135. Based on my review of the prosecution history, I understand that Patent Owner may argue that the sub-integrated circuit blocks are not replicable in the vertical (row) dimension of the two dimensional grid. My understanding regarding Patent Owner’s possible argument is based on Patent Owner’s argument during prosecution that in *Wong* “[i]t is clear as the network is scaled up, only columns are increasing.” (Ex. 1004 at 63.) I disagree with Patent Owner’s characterization of *Wong*, as *Wong* explicitly discloses that scaling up of the network can result in increased numbers of both columns and rows (i.e. both vertical and horizontal scaling.) (Ex. 1008 at 13:33-49.) With respect to horizontal scaling, figures 13A and 13B of *Wong* show expansion in the horizontal dimension as a second column of sub-integrated circuit blocks is added:

For **multiple column arrays**, levels of switch cells are added to each column's sub-network. The new levels are connected together between columns in a topology consistent with a Benes Network. See FIG. 13B in which a level of switch cells 83 are added to make the connection between two FIG. 13A column arrays. For **each additional doubling of the number of cell columns**, an additional column of switch cells must be added to each of the cell columns, and the span for connecting these new columns to each other doubles as well.

(Ex. 1008 at 13:33-42 (emphasis added).)

136. In addition, contrary to Patent Owner's allegation during prosecution that "[i]t is clear as the network is scaled up, only columns are increasing" (Ex. 1004 at 63), *Wong* discloses adding additional rows and increasing the vertical dimension of the network:

The strength of this column floorplan is that the number of cells in a column can be any power of 2, and **the number of rows can also independently be any power of 2**. This enables the generation of arrays containing numbers of cells that are any power of 2, and **with a selection of various aspect ratios**.

(Ex. 1008 at 13:44-49 (emphasis added).)

137. Therefore, *Wong* explicitly discloses increasing the number of rows of sub-integrated circuit blocks in order to increase the size of the network. As *Wong* teaches, when the network is expanded, another level (stage) is added to each of the sub-integrated circuit blocks for “each additional doubling” of the size of the network. (Ex. 1008 at 13:36-40.)

138. Indeed, Patent Owner acknowledged during prosecution that:

As disclosed in Fig. 13B [of *Wong*], columns are doubled by adding one more stage of switches in both the columns (for example Fig. 13A is replicated to get Fig. 13B and a new stage of switches 83 are added and the cross links between the new stage of switches become horizontal links).

(Ex. 1004 at 63.)

139. Therefore, contrary to Patent Owner’s contention during prosecution, *Wong* discloses that the network can be scaled up by adding columns or rows, where each doubling in size adds another level (stage) that is the same in each of the sub-integrated circuit blocks.

140. *Wong*’s inclusion of an additional switch in each sub-integrated circuit block when the size of the network is doubled is consistent with the disclosure of the ’523 patent. Specifically, figure 1H of the ’523 patent shows “the extension of

layout 100C” where the size of the network has been quadrupled (128 inputs and outputs in figure 1H vs. 32 inputs and outputs in figure 1C). (Ex. 1001 at 15:41-43.) As disclosed by the ’523 patent with respect to figure 1H, “[e]ach block in all the super-quadrants has **two more switches** namely switch 6 and switch 7 in addition to the switches [1-5] illustrated in layout 100C of FIG. 1C.” (*Id.* at 15:49-51 (emphasis added).) Therefore, a person of ordinary skill in the art would have recognized that, just as is disclosed in *Wong*, each time the size of the network is doubled in the ’523 patent, another switch (stage) is added to each of the sub-integrated circuit blocks.

2. Claim 20

“The integrated circuit device of claim 1, wherein said sub-integrated circuit blocks comprising any arbitrary hardware logic or memory circuits.”

141. In my opinion, *Wong* discloses this claim element. As I discussed above with respect to claim limitations 1(b) and 1(c), *Wong* discloses an integrated circuit device that includes a “plurality of sub-integrated circuit blocks” where such blocks include logic cells 81 shown in figure 13A below. (See my discussion above in Sections IX.A.1(b)-(c); Ex. 1008 at FIG. 13A.)

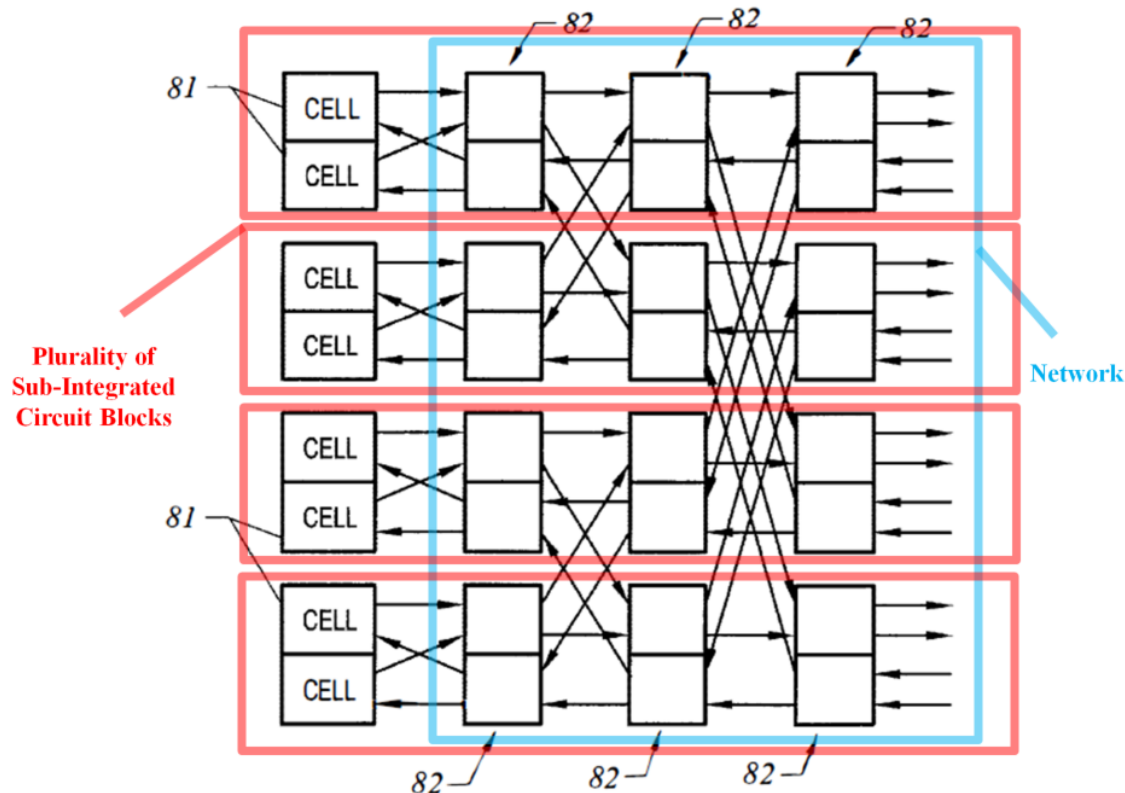


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated).)

142. As further disclosed by *Wong*, “[i]n an FPGA, the logic is composed from building blocks called ‘logic cells’” where “[a]n example of a typical logic cell is a 2-input NAND gate.” (Ex. 1008 at 6:55-58.) *Wong* further discloses that the logic cells that connect to the routing network in FPGA embodiments can be lookup tables. (Ex. 1008 at 8:51-51 (“Each logic cell is a 4-LUT (4 input Look Up Table).”), 9:9-11 (“For the purpose of analysis, assuming the logic cell is a 4-LUT (4-input Look-Up Table) with a latched output . . .”).) A person of ordinary skill in the art

would have understood that *Wong's* disclosure of NAND gates and lookup tables constitutes disclosure of “any arbitrary hardware logic” as recited in claim 20.

3. Claim 21

“The integrated circuit device of claim 1, wherein said switches comprising active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device or structured ASIC device.”

143. *Wong* discloses this feature. The '523 patent discloses that the switches in the network can be “one-time programmable cross points” that are implemented using vias that couple inlet links with outlet links:

All the embodiments disclosed in the current invention are useful in many varieties of applications. FIG. 5A1 illustrates the diagram of 500A1 which is a typical two by two switch with two inlet links namely IL1 and IL2, and two outlet links namely OL1 and OL2. The two by two switch also implements four crosspoints namely CP(1,1), CP(1,2), CP(2,1) and CP(2,2) as illustrated in FIG. 5A1.

(Ex. 1001 at 32:62-33:1.)

All the embodiments disclosed in the current invention are useful in one-time programmable integrated circuit applications. FIG. 5A3 illustrates the detailed diagram 500A3 for the implementation of the diagram 500A1 in one-time programmable integrated circuit embodiments. Each crosspoint is implemented by a via coupled between the corresponding inlet link and outlet link in one-time programmable integrated circuit embodiments. Specifically crosspoint CP(1,1) is implemented by via V(1,1) coupled between inlet link IL1 and outlet link OL1”

(Ex. 1001 at 33:58-67.)

144. *Wong* discloses Mask Programmable Gate Arrays (MPGAs) that include “one-time programmable cross points” implemented using vias in the same manner as the disclosure in the ’523 patent. Specifically, *Wong* discloses:

Applicability to MPGA

Finally, the disclosed Benes interconnect network can also be applied to MPGAs (Mask Programmable Gate Arrays). This is accomplished as a post-processing step where each switch cell used in the routing is replaced with either a metal via or an end-to-end concatenation of two same layer metal wires, depending on the orientation of the wires. The advantage over existing MPGA interconnect

architectures is the guaranteed routability, support for pipelining, as well as the fast execution speed of the place-and-route algorithms.

(Ex. 1008 at 14:27-37.)

145. Therefore, in my opinion, *Wong* discloses “said switches comprising **active one-time programmable cross points and said integrated circuit device is a mask programmable gate array (MPGA) device** or structured ASIC device” as recited in claim 21.

4. Claim 22

“The integrated circuit device of claim 1, wherein said switches comprising passive cross points or just connection of two links or not and said integrated circuit device is a[n] Application Specific Integrated Circuit (ASIC) device.”

146. *Wong* discloses this feature. For example, *Wong* discloses:

Finally, the disclosed Benes interconnect network can also be applied to MPGAs (Mask Programmable Gate Arrays). This is accomplished as a post-processing step where each **switch cell used in the routing is replaced with either a metal via or an end-to-end concatenation of two same layer metal wires**, depending on the orientation of the wires. The advantage over existing MPGA interconnect architectures is the guaranteed routability, support for pipelining, as well as the fast execution speed of the place-and-route algorithms.

(Ex. 1008 at 14:27-37 (emphasis added).)

147. Therefore, *Wong* discloses “said switches comprising . . . just connection of two links or not” as it discloses metal vias connecting links or concatenation of two wires. *Wong* also discloses that the FPGA and MPGA embodiments are used in ASICs:

It is even possible to accommodate a user who has only a general idea of the logic design, but can specify the maximum gate count anticipated, and does so in order to begin the manufacturing of his or her **ASIC (Application Specific Integrated Circuit)** before the final logic design is finished.

(*Id.* at 12:67-13:5.)

148. Therefore, in my opinion, *Wong* discloses “wherein said switches comprising passive cross points or just connection of two links or not and said integrated circuit device is a[n] Application Specific Integrated Circuit (ASIC) device” as recited in claim 22.

B. Wong Discloses or Suggests the Features of Claims 15-18, 32, and 47

149. In my opinion, *Wong* discloses or suggests all of the features of claims 15-18, 32, and 47 of the '523 patent.

1. Claim 15

“The integrated circuit device of claim 1, wherein said horizontal and vertical links are implemented on two or more metal layers.”

150. In my opinion, *Wong* discloses or suggests this feature. As discussed above with respect to claim element 1(j), *Wong* discloses that the cross links in the networks of figures 13A and 13B are implemented using horizontal and vertical links. (*See* my discussion above in Section IX.A.1(j).) *Wong* further discloses that the networks shown in figures 13A and 13B are included in FPGAs, which are integrated circuits that can be implemented using complementary metal-oxide-semiconductor (CMOS) technology. (Ex. 1008 at 4:66-5:2, 5:22-25.) *Wong* further discloses that the interconnections between switches, which includes the cross links that are vertical and horizontal links as discussed above with respect to claim feature 1(j), are implemented using metal conductors. (*Id.* at 13:50-53 (“[T]he long inter-column connections for several levels can all pass in parallel over the same area. The floorplan may be limited by the **metal pitch** constraints of the semiconductor process used to manufacture the FPGA” (emphasis added).) *Wong* discloses integrated circuits with multiple layers of metal, which a person of ordinary skill in

the art would have understood to be typical of most integrated circuits in the early 2000s timeframe. (*Id.* at 14:28-34 (discussing the use of “vias” that connect different conductive layers and “same layer metal wires” thereby indicating metal wires on different layers are also present).)

151. While *Wong* does not explicitly disclose that the “horizontal and vertical links are implemented on two or more metal layers,” it would have been predictable to implement this feature in *Wong*’s integrated circuit device. Such an implementation would have been a mere combination of known components and technologies (e.g., horizontal and vertical links as in *Wong*, and multiple metal layers as also disclosed in *Wong*), according to known methods, to produce predictable results, and a person of ordinary skill would have had a reasonable expectation of success regarding this implementation. A person of ordinary skill in the art would have understood that because the links are implemented using metal wires in *Wong*, using two or more layers for the links is either necessarily present in *Wong* or such a person of skill would have been motivated to implement the links in two or more metal layers. For example, as shown in figure 13A of *Wong*, certain cross links overlap between the switches. If the cross links were implemented using only a single metal layer, a short circuit would occur where they intersect, whereas if they

are routed on different metal layers, no such shorting occurs as they are overlapping instead of intersecting.

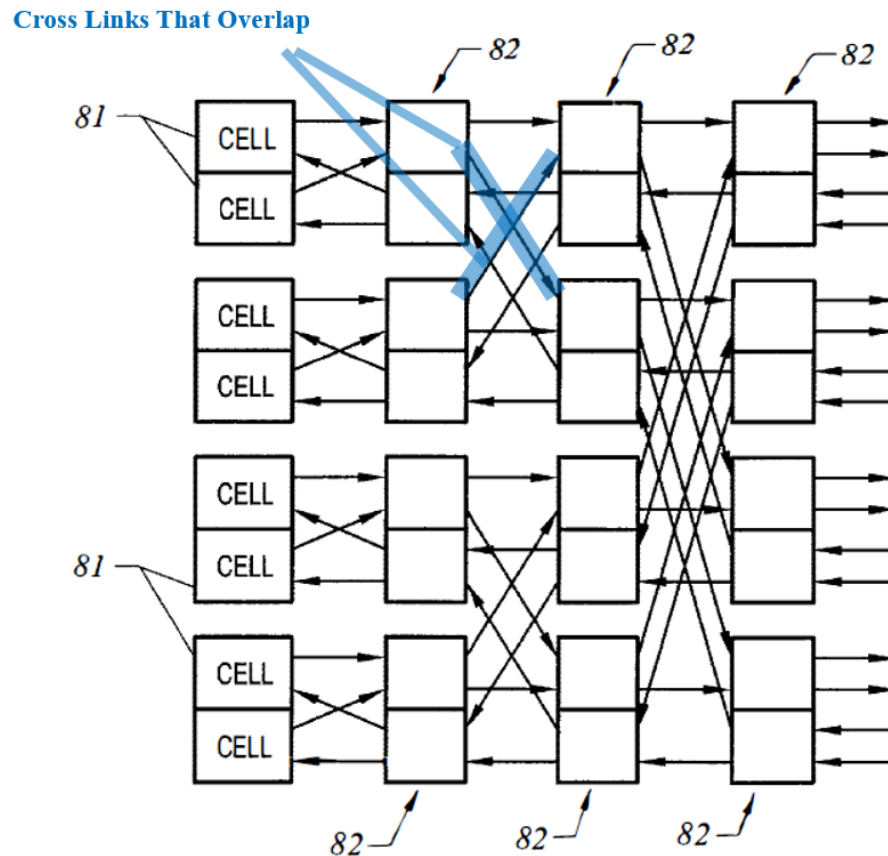


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated).)

152. Therefore, a person of ordinary skill in the art would have understood that *Wong* discloses or suggests that the “horizontal and vertical links are implemented on two or more metal layers.”

2. Claim 16

“The integrated circuit device of claim 1, wherein said switches comprising active and reprogrammable cross points and said each cross point is programmable by an SRAM cell or a Flash Cell.”

153. In my opinion, *Wong* discloses or suggests this feature. *Wong* discloses that the FPGA integrated circuits can be “SRAM-based FPGA[s].” (Ex. 1008 at 2:25-26, 3:20-22 (“Current SRAM (Static Random Access Memory)-based FPGA products conform to the interconnect architecture as illustrated in FIG. 1.”).) *Wong* further discloses that a configuration bit is used to determine the connectivity of the different links within the network. (*Id.* at 3:48-50, 5:4-13.) A person of ordinary skill in the art would have understood that in an SRAM-based FPGA, SRAM memory cells are used to store the configuration bits used in determining the different connection in the network. For example, U.S. Patent No. 7,558,967 (“*Wong-967*”) (Ex. 1044) discloses:

FPGAs may typically include a physical template that includes an array of circuits, sets of uncommitted routing interconnects, and sets of user programmable switches associated with both the circuits and the routing interconnects. When these **switches are properly programmed (set to on or off states)**, the template or the underlying circuit and **interconnect of the FPGA is customized or configured** to perform specific customized

functions. By reprogramming the on-off states of these switches, an FPGA can perform many different functions.

...

The user programmable switches in an FPGA can be implemented in various technologies, such as Oxide Nitrogen Oxide (ONO) antifuse, Metal- Metal (M-M) antifuse, **Static Random Access Memory (SRAM) memory cell**, Flash Erasable Programmable Read Only Memory (EPROM) memory cell, and electronically Erasable Programmable Read Only Memory (EEPROM) memory cell. . . . A memory cell controlled switch implementation of an FPGA can be reprogrammed repeatedly. In this scenario, a NMOS transistor may be used as the switch to either connect or leave unconnected two selected points (A,B) in the circuit. The source and drain nodes of the transistor may be connected to points A, B respectively, and its gate node may be directly or indirectly connected to the memory cell. **By setting the state of the memory cell to either logical “1” or “0”, the switch can be turned on or off and thus point A and B are either connected or remain unconnected.** Thus, the ability to program these switches provides for a very flexible device.

(Ex. 1044, 1:30-60 (emphasis added).)

154. Similarly, U.S. Patent No. 5,847,577 (“*Trimberger*”) (Ex. 1043) discloses that:

FPGAs are well known in the art . . . [A] configurable logic array [] includes a plurality of [configurable logic blocks, or CLBs] interconnected in response to control signals to perform a selected logic function, and [] a memory is used to store the particular data used to configure the CLBs. . . .

Each CLB typically has a plurality of input and output pins, and a set of programmable interconnect points (PIPs) for each input and output pin. . . .

Because the PIPs in the FPGA are programmable, any given output pin of a CLB is connectable to any given input pin of any other desired CLB. . . .

Each PIP typically includes a single pass transistor (i.e. effectively a switch). The state of conduction, i.e. whether the switch is opened or closed, is controlled by application of the control signals discussed above to a transistor control terminal, e.g. a gate. **The programmed state of each pass transistor is typically latched by a storage device, such as a static random access memory (SRAM) cell 100,** illustrated in FIG. 1. As shown in FIG. 1, a high signal ADDR on address line 102 identifies the **SRAM cell to be programmed** by turning on an n-type pass transistor 104, thereby allowing the desired memory

cell state DATA to be transferred from the data line 101 to a latch 106. **The state of the control signal stored in the latch 106 determines whether a pass transistor (PIP) 109 is turned on or off, thereby opening or closing a path in the FPGA interconnect.**

(Ex. 1043, 1:22-2:25 (emphasis added).)

155. *Wong* discloses that while switches implemented with multiplexers can be used in the FPGA designs, replacing sub-networks in the network with crossbar switches reduces the latency of the network:

Because of the hierarchical structure of a Benes network, the Benes network can be recursively constructed. The Upper Network and Lower Network are themselves expanded into Benes networks, each with half the number of inputs and outputs of the original network. See FIG. 3B. In essence, each of these sub-networks simply guarantees a means of routing any of its inputs to any of its outputs. Functionally, this is a crossbar switch. A Benes network is a much more area efficient method of implementing a rearrangeable crossbar. The size of a Benes network grows by $N \cdot \log_2 N$, whereas the size of a crossbar grows by N^2 . However, the **maximum latency can be reduced if just the lowest levels of Benes networks are substituted with crossbars.**

(Ex. 1008 at 11:30-42 (emphasis added).)

156. While *Wong* does not explicitly disclose that the “said switches comprising active and reprogrammable cross points and said each cross point is programmable by an SRAM cell or a Flash Cell,” it would have been predictable to implement such features. Such an implementation would have been a mere combination of known components and technologies, according to known methods, to produce predictable results, and a person of ordinary skill would have had a reasonable expectation of success regarding this implementation. A person of

ordinary skill in the art would have understood that in an “SRAM-based FPGA” as disclosed by *Wong*, the control bits that control the switches would be implemented using SRAM cells that store the “1s” and “0s” that are the control bits. Such a person of ordinary skill in the art would also have understood that a “rearrangeable crossbar” as disclosed by *Wong* includes “reprogrammable crosspoints” where the programming would be based on the control bits stored in the SRAM cells. A person of ordinary skill in the art reading *Wong* would have been motivated to use SRAM cells in an “SRAM-based FPGA” to control the “rearrangeable crossbar” because SRAM cells provide a well-understood data storage medium on integrated circuits and the control bits that determine the connectivity in the crossbar are easily stored in the SRAM, which is a reprogrammable memory. Therefore, in my opinion, *Wong* discloses or suggests this feature.

3. Claim 17

“The integrated circuit device of claim 1, said sub-integrated circuit blocks are of equal die size.”

157. In my opinion, *Wong* discloses or suggests this feature. As discussed above with respect to claim element 1(k) and shown in figures 13A, 13B, and 14A, each of the sub-integrated circuit blocks includes the same number of stages and the same number of switches. (Ex. 1008 at FIGs. 13A, 13B, 14C; *see* my discussion above in Section IX.A.1(k).)

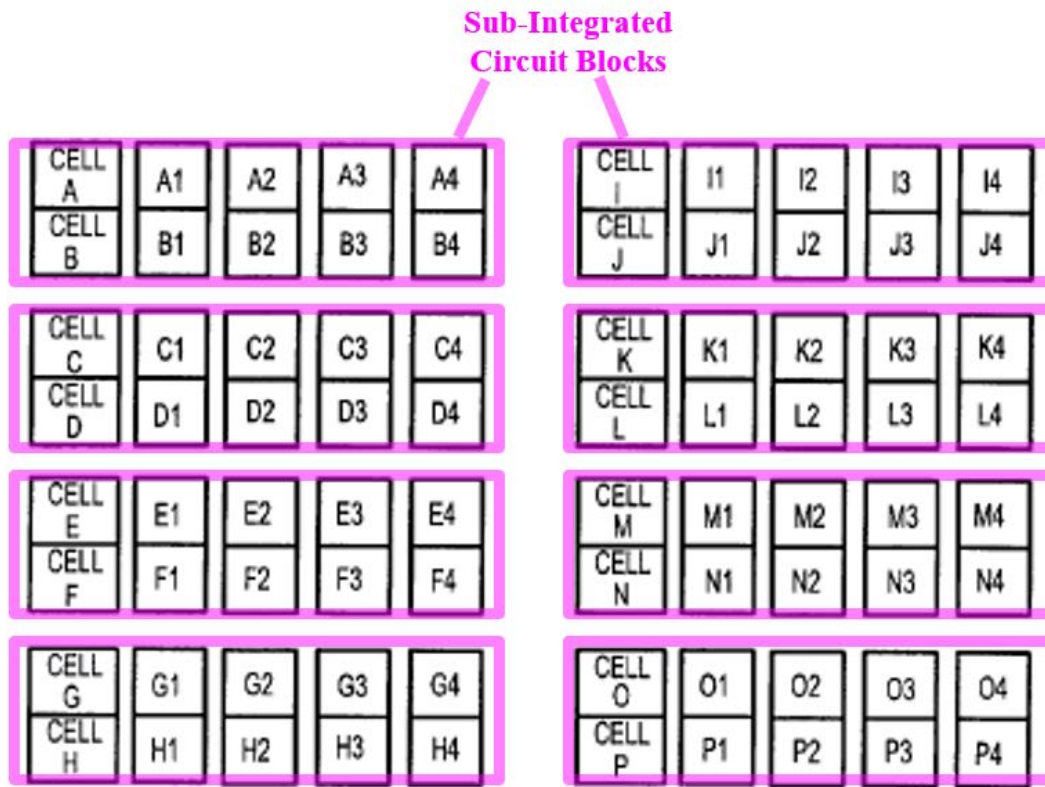


FIG. 14A

(Ex. 1008 at FIG. 14A (annotated).)

158. Therefore, *Wong* discloses that each sub-integrated circuit block has the same configuration (same number of stages and same number of switches in each stage) in the network. (*See* my discussion above in Section IX.A.1(k).) *Wong* further discloses that an FPGA generator can be used to provide an end user with flexibility in terms of how the FPGA is configured:

In accordance with the present invention, the described interconnect network has several options which trade off area, latency, and throughput. To take advantage of this flexibility, different families of FPGA products, each family optimized for different design objectives, may be created. Perhaps a better way is to provide an FPGA array generator program to the end user. Such a generator-based methodology allow the user to explore various tradeoffs for his or her specific application. In addition, the generator allows the end user to specify the size and shape of the array desired. This enables the use to fit an FPGA component onto a larger VLSI chip floorplan with other components, a further advantage of the present invention.

(Ex. 1008 at 11:62-12:7.)

159. *Wong* further discloses that in some embodiments “the same switch cell is used everywhere in the generator.” (*Id.* at 14:9.) A person of ordinary skill in the art would have understood that if the same switch cell is used everywhere in the FPGA and the sub-integrated circuit blocks are configured the same as is shown in figures 13A, 13B, and 14A, then the “sub-integrated circuit blocks are of equal die size.” Even if it is not explicitly disclosed, in my opinion a person of ordinary skill in the art would have been motivated to use the same layout for each of the sub-integrated circuit blocks on the integrated circuit device. A person of ordinary skill

implementing *Wong's* integrated circuit device would have had two choices regarding the die size for the sub-integrated circuit blocks: they could be implemented with equal die size, or unequal die size. Thus, an implementation as in claim 17, where the sub-integrated circuit blocks are of equal die size, would have been recognized as being a mere choice among a finite number of known alternatives, each having predictable outcomes. Of these known alternatives, choice of equal die size would have been recognized as predictable and beneficial. For example, a person of ordinary skill in the art would have understood that reusing the layout for each of the blocks would have been more efficient from a design standpoint and would have ensured uniformity in placing the blocks in the two-dimensional grid and uniformity in block operation (delays, drive strength, etc.) Because a person of ordinary skill in the art would have been motivated to use the same layout for the sub-integrated circuit blocks, the area on the integrated circuit occupied by each of the sub-integrated circuit blocks ("die size") is the same. A person of ordinary skill would have been capable of implementing the "equal die size" feature, e.g., because implementing a desired layout and/or die size for a given circuit component was well within the skill of an ordinary artisan long before the alleged invention date. A person of ordinary skill would have had a reasonable expectation of success regarding implementing "equal die size" as in claim 17,

because this would have been a straightforward implementation involving a simple choice, as discussed above. Therefore, a person of ordinary skill in the art would have understood that *Wong* discloses or suggests that all of the sub-integrated circuit blocks have “equal die size.”

4. Claim 18

“The integrated circuit device of claim 15, where said sub-integrated circuit blocks are Lookup Tables (hereinafter “LUTs”) and said integrated circuit device is a field programmable gate array (FPGA) device or field programmable gate array (FPGA) block embedded in another integrated circuit device.”

160. In my opinion, *Wong* discloses or suggests these features to the extent they can be understood. As I discussed above, *Wong* discloses or suggests an integrated circuit as recited in claim 15. (See my discussion above in Section IX.B.1.) Moreover, as discussed above with respect to claim element 1(a), *Wong* discloses that the integrated circuit is an FPGA. (Ex. 1008 at 1:14-21, 1:59-61, 3:7-10; 13:19-22, 13:36-38, FIGs. 13A, 13B); see my discussion above in Section IX.A.1(a) and my overview of FPGAs in Section V.A.)

161. *Wong* discloses the inclusion of lookup tables with the routing network.⁷ For example, figure 13A of *Wong* shows a routing network made up of switches in stages, where the network is used to provide connections between logic cells. (Ex. 1008 at FIG. 13A.)

⁷ Claim 18 conflicts with claim 1 in that it states that the “sub-integrated circuit blocks **are** Lookup Tables.” I have been asked to assume that claim 18 requires that a lookup table is included in each of the sub-integrated circuit blocks recited in claim 1 in a manner similar to the configurable logic blocks or arbitrary digital circuits that are interconnected by the routing network.

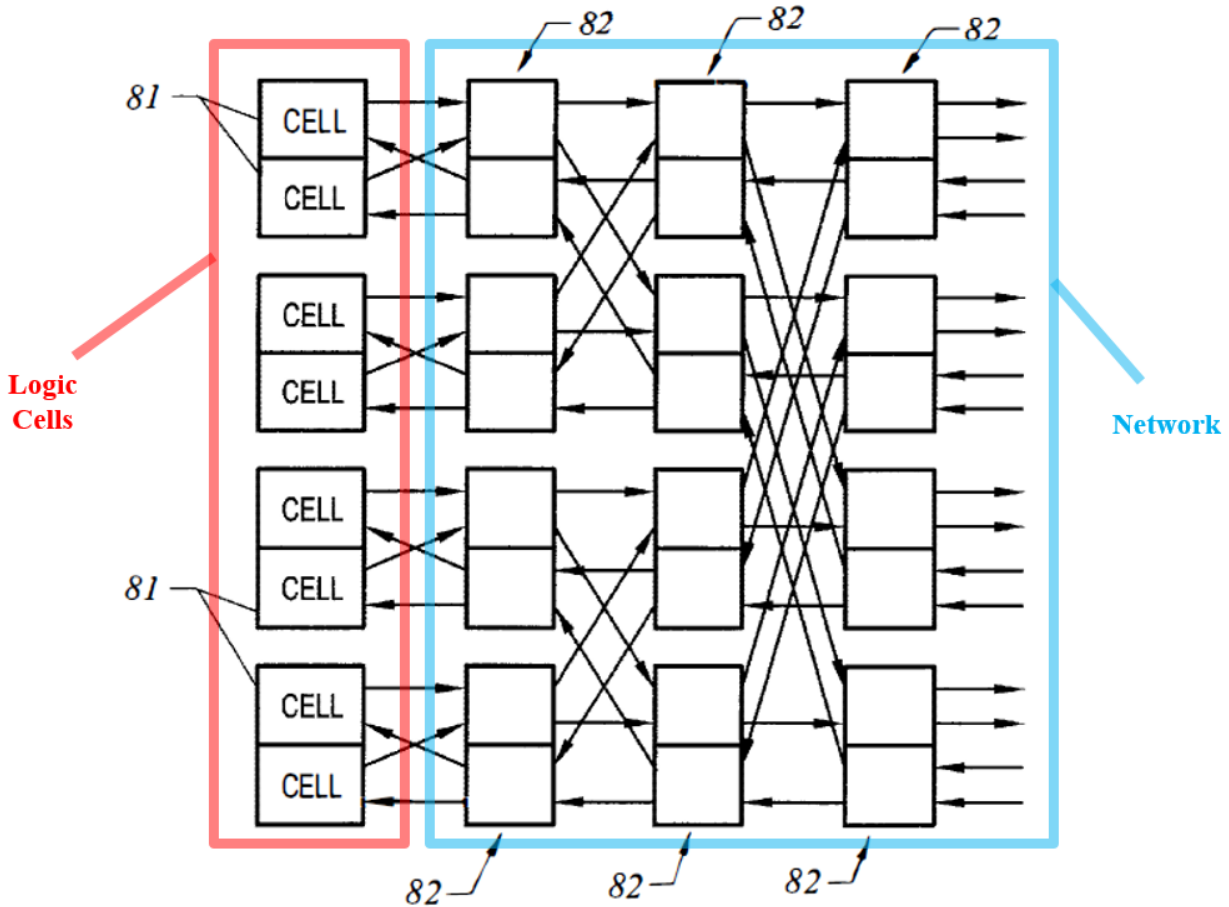


FIG. 13A

(Ex. 1008 at FIG. 13A (annotated).)

162. *Wong* further discloses that the logic cells that connect to the routing network in FPGA embodiments are lookup tables. (Ex. 1008 at 8:51 (“Each logic cell is a 4-LUT (4 input Look Up Table).”), 9:9-11 (“For the purpose of analysis, assuming the logic cell is a 4-LUT (4-input Look-Up Table) with a latched output . . .”).) Therefore, in my opinion, the *Wong* discloses or suggests the features of

claim 18, including “where said sub-integrated circuit blocks are Lookup Tables (hereinafter ‘LUTs’).”

5. Claim 32

“The integrated circuit device of claim 1, wherein said straight links connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and

Said cross links are connecting as vertical or horizontal or diagonal links between two different said sub-integrated circuit blocks.”

163. *Wong* discloses or suggests this feature for at least the same reasons discussed above for claim limitation 1(j). (*See* my discussion above at Section IX.A.1(j).)

6. Claim 47

“The integrated circuit device of claim 1, wherein said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-inverting buffers.”

164. In my opinion, *Wong* discloses or suggests this feature. As discussed above with respect to claim element 1(g), *Wong* discloses a plurality of forward connecting links and a plurality of backward connecting links. (*See* my discussion above in Section IX.A.1(g).) *Wong* further discloses:

FIG. 11B shows the insertion of a buffer 55 along the upper path between the logic cells 51 and 54. Buffers can be inserted without affecting the logic of the design. In fact, most commercial place-and-route tools will insert buffers on signals with long routing lines in order to improve their overall delay; this is done transparently for the user. The present invention allows buffer insertion to be made simply because the signal delays through the interconnect network are known.

(Ex. 1008 at 10:59-67; *see also id.* at FIG. 11B (showing buffer 55).)

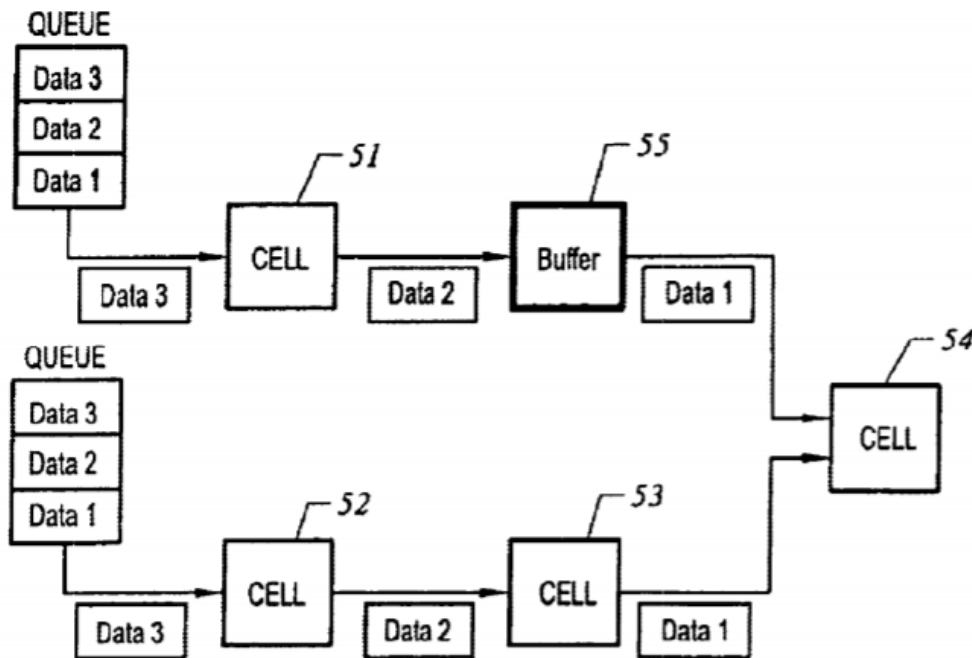
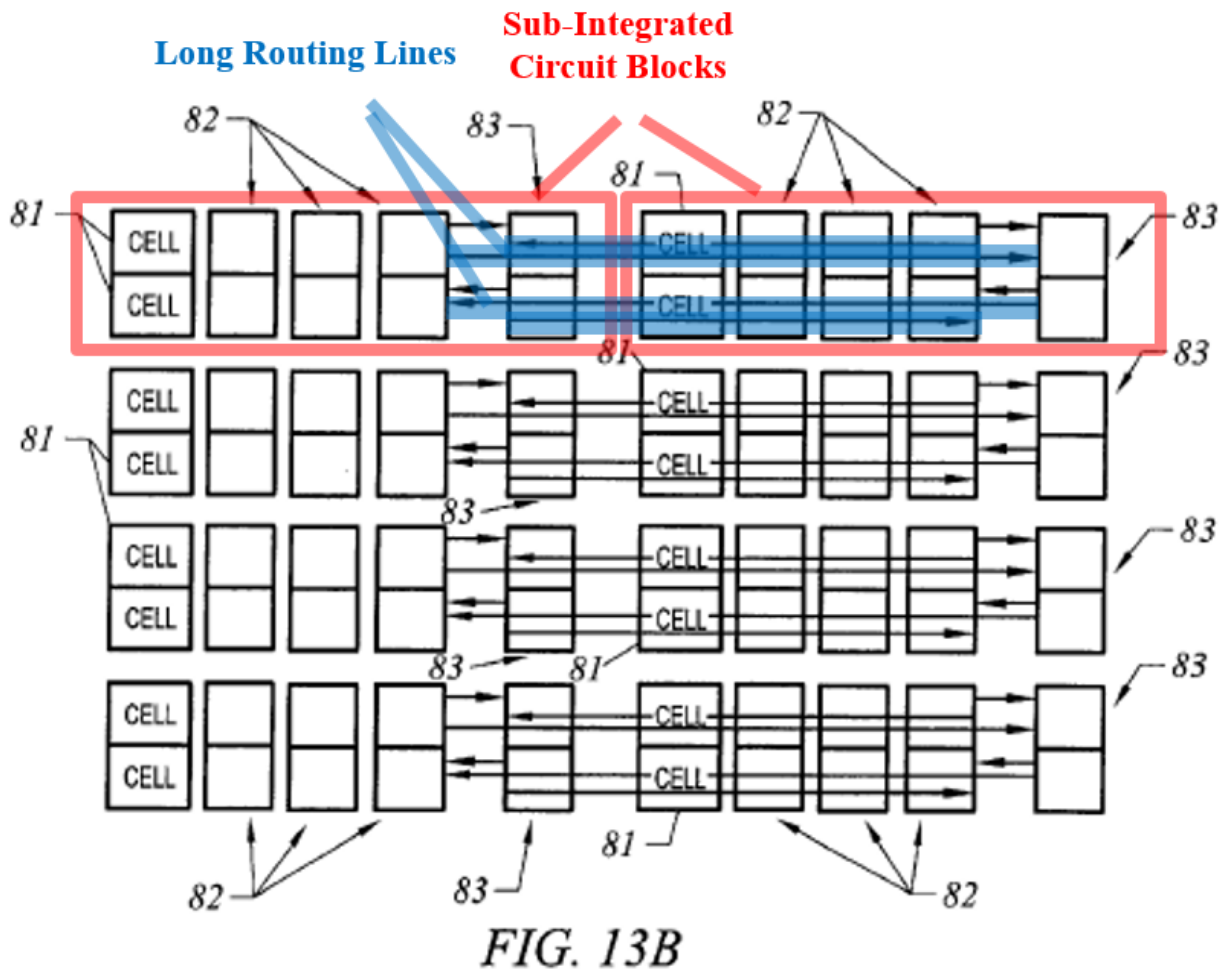


FIG. 11B

(*Id.* at FIG. 11B (showing buffer 55).)

165. *Wong* also discloses that buffers can be inserted to lengthen the shorter delay paths until the delay paths match. (*Id.* at 11:1-6.) While *Wong* does not explicitly disclose that the “said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them,” a person of ordinary skill in the art would have been motivated to include such buffers in the forward and backward connecting links.

166. A person of ordinary skill in the art reading *Wong* would have been motivated to use buffers in the forward and backward connecting links because such buffers provide a well-understood means for reducing propagation delay on long routing lines such as those between higher-level switches in different sub-integrated circuit blocks of *Wong*. For example, as shown in annotated figure 13B of *Wong* below, the horizontal links between stages 3 and 4 of different sub-integrated circuit blocks are much longer than the links between lower level stages.



(Ex. 1008 at FIG. 13B (annotated).)

167. A person of ordinary skill in the art would have understood that as the network disclosed in *Wong* is further scaled up in size, the length of the routing lines or “links” connecting the higher-level switches will continue to grow in length. (*Id.* at 13:38-42 (“For each additional doubling of the number of cell columns, an additional column of switch cells must be added to each of the cell columns, and **the span for connecting these new columns to each other doubles as well.**”))

(emphasis added).) Therefore, such a person of ordinary skill in the art would have been motivated to include buffers in such forward and backward connecting links, e.g., in order to improve the overall delay on such lines as is disclosed by *Wong*. (*Id.* at 10:59-67.) A person of ordinary skill in the art would also have been motivated to include buffers in the forward and backward connecting links to address any mismatch in delays, as *Wong* further discloses that buffers can be used to lengthen the shorter delay paths until the delay paths match. (*Id.* at 11:1-6.) A person of ordinary skill in the art would have reasonably expected success in including such buffers and would have known how to make any necessary changes to the teachings of *Wong* in order to make a functioning circuit.

168. A person of ordinary skill in the art reading *Wong* would have understood that the buffers disclosed by *Wong* include “non-inverting” buffers. *Wong* discloses that “[b]uffers can be inserted without affecting the logic of the design,” thereby indicating that no further circuitry is required to maintain the logic of a circuit to which the buffers are added. (*Id.* at 10:60-61; *see also id.* at FIGs. 11A, 11B.) If inverting buffers were used, further inversion would be required in order to restore the non-inverted state of the signal being inverted. In any event, the use of a non-inverting buffer was well known long before the alleged invention date of the ’523 patent, e.g., for adjusting or compensating timing in a circuit. (*See, e.g.,*

Ex. 1045, 2:9-11 (“The delay element may, however, be a non-inverting buffer circuit.”).) Therefore, a person of ordinary skill would have found the use of “non-inverting” buffers to be entirely predictable and would have found them desirable to use, particularly because an inverting buffer would have been understood to constitute and entail more complexity than a non-inverting one.

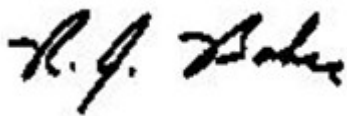
169. For at least these reasons, *Wong* discloses or suggests “wherein said plurality of forward connecting links use a plurality of buffers to amplify signals driven through them and said plurality of backward connecting links use a plurality of buffers to amplify signals driven through them; and said buffers can be inverting or non-inverting buffers” as recited in claim 47. This configuration (i.e., implementing the features of claim 47) would have been a mere combination of known components and technologies (e.g., forward connecting links and backward connecting links as disclosed in *Wong*, and buffers as also disclosed in *Wong*), according to known methods, to produce predictable results, and a person of ordinary skill would have had a reasonable expectation of success regarding this configuration.

X. CONCLUSION

170. In summary, it is my opinion that all of the features of claims 1, 15-18, 20-22, 32, and 47 of the '523 patent are disclosed or suggested by the prior art.

171. I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Dated: December 16, 2019

By: 

R. Jacob Baker, Ph.D., P.E.