

VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

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5 CROSS REFERENCE TO RELATED APPLICATIONS

This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Docket No. M-0037US entitled "FULLY CONNECTED GENERALIZED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed concurrently.

- 10 This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Docket No. M-0038US entitled "FULLY CONNECTED GENERALIZED BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed concurrently.

- 15 This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Docket No. M-0039US entitled "FULLY CONNECTED GENERALIZED REARRANGEABLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed concurrently.

- 20 This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Docket No. M-0040US entitled "FULLY CONNECTED GENERALIZED MULTI-LINK BUTTERFLY FAT TREE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed concurrently.

- 25 This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Docket No. M-0041US entitled "FULLY CONNECTED GENERALIZED FOLDED MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application, filed concurrently.

This application is related to and incorporates by reference in its entirety the U.S. Provisional Patent Application Docket No. M-0042US entitled "FULLY CONNECTED GENERALIZED STRICTLY NONBLOCKING MULTI-LINK MULTI-STAGE NETWORKS" by Venkat Konda assigned to the same assignee as the current application,
 5 filed concurrently.

BRIEF DESCRIPTION OF DRAWINGS

FIG. 1A is a diagram 100A of an exemplary symmetrical multi-link multi-stage network $V_{fold-link}(N, d, s)$ having inverse Benes connection topology of nine stages with $N = 32$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and
 10 rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1B is a diagram 100B of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-link}(N, d, s)$ of the network 100A shown in FIG. 1A, having inverse Benes connection topology of five stages with $N = 32$, $d = 2$ and $s=2$, strictly nonblocking
 15 network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 1C is a diagram 100C layout of the network $V_{fold-link}(N, d, s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

20 FIG. 1D is a diagram 100D layout of the network $V_{fold-link}(N, d, s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links $ML(1,i)$ for $i = [1, 64]$ and $ML(8,i)$ for $i = [1, 64]$.

FIG. 1E is a diagram 100E layout of the network $V_{fold-link}(N, d, s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links $ML(2,i)$ for $i = [1, 64]$ and
 25 $ML(7,i)$ for $i = [1, 64]$.

FIG. 1F is a diagram 100F layout of the network $V_{fold-link}(N, d, s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links $ML(3,i)$ for $i = [1, 64]$ and $ML(6,i)$ for $i = [1, 64]$.

FIG. 1G is a diagram 100G layout of the network $V_{fold-link}(N, d, s)$ shown in
 5 FIG. 1B, in one embodiment, illustrating the connection links $ML(4,i)$ for $i = [1, 64]$ and $ML(5,i)$ for $i = [1, 64]$.

FIG. 1H is a diagram 100H layout of a network $V_{fold-link}(N, d, s)$ where $N = 128$, $d = 2$, and $s = 2$, in one embodiment, illustrating the connection links belonging with in each block only.

10 FIG. 1I is a diagram 100I detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N, d, s)$ or $V_{fold}(N, d, s)$.

FIG. 1J is a diagram 100J detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out
 15 when the layout 100C is implementing $V(N, d, s)$ or $V_{fold}(N, d, s)$.

FIG. 1K is a diagram 100K detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N, d, s)$ or $V_{fold}(N, d, s)$.

FIG. 1K1 is a diagram 100M1 detailed connections of BLOCK 1_2 in the network
 20 layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N, d, s)$ or $V_{fold}(N, d, s)$ for $s = 1$.

FIG. 1L is a diagram 100L detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N, d, s)$ or $V_{fold}(N, d, s)$.

FIG. 1L1 is a diagram 100L1 detailed connections of BLOCK 1_2 in the network layout 100C in one embodiment, illustrating the connection links going in and coming out when the layout 100C is implementing $V(N, d, s)$ or $V_{fold}(N, d, s)$ for $s = 1$.

FIG. 2A1 is a diagram 200A1 of an exemplary symmetrical multi-link multi-stage network $V_{fold-link}(N, d, s)$ having inverse Benes connection topology of one stage with $N = 2$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2A2 is a diagram 200A2 of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-link}(N, d, s)$ of the network 200A1 shown in FIG. 2A1, having inverse Benes connection topology of one stage with $N = 2$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2A3 is a diagram 200A3 layout of the network $V_{fold-link}(N, d, s)$ shown in FIG. 2A2, in one embodiment, illustrating all the connection links.

FIG. 2B1 is a diagram 200B1 of an exemplary symmetrical multi-link multi-stage network $V_{fold-link}(N, d, s)$ having inverse Benes connection topology of one stage with $N = 4$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2B2 is a diagram 200B2 of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-link}(N, d, s)$ of the network 200B1 shown in FIG. 2B1, having inverse Benes connection topology of one stage with $N = 4$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2B3 is a diagram 200B3 layout of the network $V_{fold-link}(N, d, s)$ shown in FIG. 2B2, in one embodiment, illustrating the connection links belonging with in each block only. FIG. 2B4 is a diagram 200B4 layout of the network $V_{fold-link}(N, d, s)$ shown in FIG. 2B2, in one embodiment, illustrating the connection links $ML(1,i)$ for $i = [1, 8]$ and $ML(2,i)$ for $i = [1, 8]$.

FIG. 2C11 is a diagram 200C11 of an exemplary symmetrical multi-link multi-stage network $V_{fold-link}(N,d,s)$ having inverse Benes connection topology of one stage with $N = 8$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention. FIG. 2C12 is a diagram 200C12 of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-link}(N,d,s)$ of the network 200C11 shown in FIG. 2C11, having inverse Benes connection topology of one stage with $N = 8$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2C21 is a diagram 200C21 layout of the network $V_{fold-link}(N,d,s)$ shown in FIG. 2C12, in one embodiment, illustrating the connection links belonging with in each block only. FIG. 2C22 is a diagram 200C22 layout of the network $V_{fold-link}(N,d,s)$ shown in FIG. 2C12, in one embodiment, illustrating the connection links $ML(1,i)$ for $i = [1, 16]$ and $ML(4,i)$ for $i = [1,16]$. FIG. 2C23 is a diagram 200C23 layout of the network $V_{fold-link}(N,d,s)$ shown in FIG. 2C12, in one embodiment, illustrating the connection links $ML(2,i)$ for $i = [1, 16]$ and $ML(3,i)$ for $i = [1,16]$.

FIG. 2D1 is a diagram 200D1 of an exemplary symmetrical multi-link multi-stage network $V_{fold-link}(N,d,s)$ having inverse Benes connection topology of one stage with $N = 16$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2D2 is a diagram 200D2 of the equivalent symmetrical folded multi-link multi-stage network $V_{fold-link}(N,d,s)$ of the network 200D1 shown in FIG. 2D1, having inverse Benes connection topology of one stage with $N = 16$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 2D3 is a diagram 200D3 layout of the network $V_{fold-link}(N,d,s)$ shown in FIG. 2D2, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 2D4 is a diagram 200D4 layout of the network $V_{fold-link}(N,d,s)$ shown in
 5 FIG. 2D2, in one embodiment, illustrating the connection links $ML(1,i)$ for $i = [1, 32]$ and $ML(6,i)$ for $i = [1,32]$.

FIG. 2D5 is a diagram 200D5 layout of the network $V_{fold-link}(N,d,s)$ shown in FIG. 2D2, in one embodiment, illustrating the connection links $ML(2,i)$ for $i = [1, 32]$ and $ML(5,i)$ for $i = [1,32]$.

10 FIG. 2D6 is a diagram 200D6 layout of the network $V_{fold-link}(N,d,s)$ shown in FIG. 2D2, in one embodiment, illustrating the connection links $ML(3,i)$ for $i = [1, 32]$ and $ML(4,i)$ for $i = [1,32]$.

FIG. 3A is a diagram 300A of an exemplary symmetrical multi-link multi-stage network $V_{hcube}(N,d,s)$ having inverse Benes connection topology of nine stages with $N =$
 15 32, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3B is a diagram 300B of the equivalent symmetrical folded multi-link multi-stage network $V_{hcube}(N,d,s)$ of the network 300A shown in FIG. 3A, having inverse
 20 Benes connection topology of five stages with $N = 32$, $d = 2$ and $s=2$, strictly nonblocking network for unicast connections and rearrangeably nonblocking network for arbitrary fan-out multicast connections, in accordance with the invention.

FIG. 3C is a diagram 300C layout of the network $V_{hcube}(N,d,s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links belonging with in each block
 25 only.

FIG. 3D is a diagram 100D layout of the network $V_{hcube}(N, d, s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links $ML(1, i)$ for $i = [1, 64]$ and $ML(8, i)$ for $i = [1, 64]$.

FIG. 3E is a diagram 300E layout of the network $V_{hcube}(N, d, s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links $ML(2, i)$ for $i = [1, 64]$ and $ML(7, i)$ for $i = [1, 64]$.

FIG. 3F is a diagram 300F layout of the network $V_{hcube}(N, d, s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links $ML(3, i)$ for $i = [1, 64]$ and $ML(6, i)$ for $i = [1, 64]$.

FIG. 3G is a diagram 300G layout of the network $V_{hcube}(N, d, s)$ shown in FIG. 3B, in one embodiment, illustrating the connection links $ML(4, i)$ for $i = [1, 64]$ and $ML(5, i)$ for $i = [1, 64]$.

FIG. 3H is a diagram 300H layout of a network $V_{hcube}(N, d, s)$ where $N = 128$, $d = 2$, and $s = 2$, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 4A is a diagram 400A layout of the network $V_{fold-link}(N, d, s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

FIG. 4B is a diagram 400B layout of the network $V_{fold-link}(N, d, s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links $ML(1, i)$ for $i = [1, 64]$ and $ML(8, i)$ for $i = [1, 64]$.

FIG. 4C is a diagram 400C layout of the network $V_{fold-link}(N, d, s)$ shown in FIG. 4C, in one embodiment, illustrating the connection links $ML(2, i)$ for $i = [1, 64]$ and $ML(7, i)$ for $i = [1, 64]$.

FIG. 4D is a diagram 400D layout of the network $V_{fold-link}(N, d, s)$ shown in FIG. 4D, in one embodiment, illustrating the connection links $ML(3, i)$ for $i = [1, 64]$ and $ML(6, i)$ for $i = [1, 64]$.

FIG. 4E is a diagram 400E layout of the network $V_{fold-link}(N, d, s)$ shown in FIG. 4E, in one embodiment, illustrating the connection links $ML(4, i)$ for $i = [1, 64]$ and $ML(5, i)$ for $i = [1, 64]$.

FIG. 4C1 is a diagram 400C1 layout of the network $V_{fold-link}(N, d, s)$ shown in FIG. 1B, in one embodiment, illustrating the connection links belonging with in each block only.

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DETAILED DESCRIPTION OF THE INVENTION

The present invention is concerned with the VLSI layouts of arbitrarily large switching networks for broadcast, unicast and multicast connections. Particularly switching networks considered in the current invention include: generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$, generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-link}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ for $s =$ 1, 2, 3 or any number in general.

Efficient VLSI layout of networks on a semiconductor chip are very important and greatly influence many important design parameters such as the area taken up by the network on the chip, total number of wires, length of the wires, latency of the signals, capacitance and hence the maximum clock speed of operation. Some networks may not even be implemented practically on a chip due to the lack of efficient layouts. The different varieties of multi-stage networks described above have not been implemented previously on the semiconductor chips efficiently. For example in Field Programmable

Gate Array (FPGA) designs, multi-stage networks described in the current invention have not been successfully implemented primarily due to the lack of efficient VLSI layouts. Current commercial FPGA products such as Xilinx Vertex, Altera's Stratix implement island-style architecture using mesh and segmented mesh routing interconnects using
 5 either full crossbars or sparse crossbars. These routing interconnects consume large silicon area for crosspoints, long wires, large signal propagation delay and hence consume lot of power.

The current invention discloses the VLSI layouts of numerous types of multi-stage networks which are very efficient. Moreover they can be embedded on to mesh and
 10 segmented mesh routing interconnects of current commercial FPGA products. The VLSI layouts disclosed in the current invention are applicable to including the numerous generalized multi-stage networks disclosed in the following provisional patent applications, filed concurrently:

1) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and
 15 unicast for generalized multi-stage networks $V(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application, Attorney Docket No. M-0037 US that is incorporated by reference above.

2) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$ with numerous
 20 connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application, Attorney Docket No. M-0038 US that is incorporated by reference above.

3) Rearrangeably nonblocking for arbitrary fan-out multicast and unicast, and strictly nonblocking for unicast for generalized multi-link multi-stage networks
 25 $V_{mlink}(N_1, N_2, d, s)$ and generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application, Attorney Docket No. M-0039 US that is incorporated by reference above.

4) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application, Attorney Docket No. M-0040 US that is
 5 incorporated by reference above.

5) Strictly and rearrangeably nonblocking for arbitrary fan-out multicast and unicast for generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application, Attorney Docket No. M-0041 US that is incorporated by
 10 reference above.

6) Strictly nonblocking for arbitrary fan-out multicast and unicast for generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$ and generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$ with numerous connection topologies and the scheduling methods are described in detail in U.S. Provisional Patent Application,
 15 Attorney Docket No. M-0042 US that is incorporated by reference above.

In addition the layouts of the current invention are also applicable to generalized multi-stage pyramid networks $V_p(N_1, N_2, d, s)$, generalized folded multi-stage pyramid networks $V_{fold-p}(N_1, N_2, d, s)$, generalized butterfly fat pyramid networks $V_{bjp}(N_1, N_2, d, s)$, generalized multi-link multi-stage pyramid networks
 20 $V_{mlink-p}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage pyramid networks $V_{fold-mlink-p}(N_1, N_2, d, s)$, generalized multi-link butterfly fat pyramid networks $V_{mlink-bjp}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{cube}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general.

Symmetric RNB generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$:

25 Referring to diagram 100A in FIG. 1A, in one embodiment, an exemplary generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages of one hundred and forty four switches for satisfying

communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, 150, 160, 170, 180 and 190 is shown where input stage 110 consists of sixteen, two by four switches IS1-IS16 and output stage 120 consists of
 5 sixteen, four by two switches OS1-OS16. And all the middle stages namely the middle stage 130 consists of sixteen, four by four switches MS(1,1) - MS(1,16), middle stage 140 consists of sixteen, four by four switches MS(2,1) - MS(2,16), middle stage 150 consists of sixteen, four by four switches MS(3,1) - MS(3,16), middle stage 160 consists of sixteen, four by four switches MS(4,1) - MS(4,16), middle stage 170 consists of sixteen,
 10 four by four switches MS(5,1) - MS(5,16), middle stage 180 consists of sixteen, four by four switches MS(6,1) - MS(6,16), and middle stage 190 consists of sixteen, four by four switches MS(7,1) - MS(7,16).

As disclosed in U.S. Provisional Patent Application, Attorney Docket No. M-0039 US that is incorporated by reference above, such a network can be operated in
 15 rearrangeably non-blocking manner for arbitrary fan-out multicast connections and also can be operated in strictly non-blocking manner for unicast connections.

In one embodiment of this network each of the input switches IS1-IS4 and output switches OS1-OS4 are crossbar switches. The number of switches of input stage 110 and of output stage 120 can be denoted in general with the variable $\frac{N}{d}$, where N is the total
 20 number of inlet links or outlet links. The number of middle switches in each middle stage is denoted by $\frac{N}{d}$. The size of each input switch IS1-IS4 can be denoted in general with the notation $d * 2d$ and each output switch OS1-OS4 can be denoted in general with the notation $2d * d$. Likewise, the size of each switch in any of the middle stages can be denoted as $2d * 2d$. A switch as used herein can be either a crossbar switch, or a
 25 network of switches each of which in turn may be a crossbar switch or a network of switches. A symmetric multi-stage network can be represented with the notation $V_{mlink}(N, d, s)$, where N represents the total number of inlet links of all input switches (for example the links IL1-IL32), d represents the inlet links of each input switch or

outlet links of each output switch, and s is the ratio of number of outgoing links from each input switch to the inlet links of each input switch.

Each of the $\frac{N}{d}$ input switches IS1 – IS16 are connected to exactly d switches in middle stage 130 through two links each for a total of $2 \times d$ links (for example input switch IS1 is connected to middle switch MS(1,1) through the links ML(1,1), ML(1,2), and also connected to middle switch MS(1,2) through the links ML(1,3) and ML(1,4)). The middle links which connect switches in the same row in two successive middle stages are called hereinafter straight middle links; and the middle links which connect switches in different rows in two successive middle stages are called hereinafter cross middle links. For example, the middle links ML(1,1) and ML(1,2) connect input switch IS1 and middle switch MS(1,1), so middle links ML(1,1) and ML(1,2) are straight middle links; where as the middle links ML(1,3) and ML(1,4) connect input switch IS1 and middle switch MS(1,2), since input switch IS1 and middle switch MS(1,2) belong to two different rows in diagram 100A of FIG. 1A, middle links ML(1,3) and ML(1,4) are cross middle links.

Each of the $\frac{N}{d}$ middle switches MS(1,1) – MS(1,16) in the middle stage 130 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(1,1) and ML(1,2) are connected to the middle switch MS(1,1) from input switch IS1, and the links ML(1,7) and ML(1,8) are connected to the middle switch MS(1,1) from input switch IS2) and also are connected to exactly d switches in middle stage 140 through two links each for a total of $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected from middle switch MS(1,1) to middle switch MS(2,1), and the links ML(2,3) and ML(2,4) are connected from middle switch MS(1,1) to middle switch MS(2,3)).

Each of the $\frac{N}{d}$ middle switches MS(2,1) – MS(2,16) in the middle stage 140 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(2,1) and ML(2,2) are connected to the middle switch MS(2,1) from input switch MS(1,1), and the links ML(1,11) and ML(1,12) are connected to the

middle switch MS(2,1) from input switch MS(1,3)) and also are connected to exactly d switches in middle stage 150 through two links each for a total of $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected from middle switch MS(2,1) to middle switch MS(3,1), and the links ML(3,3) and ML(3,4) are connected from middle switch MS(2,1) to middle switch MS(3,5)).

Each of the $\frac{N}{d}$ middle switches MS(3,1) – MS(3,16) in the middle stage 150 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(3,1) and ML(3,2) are connected to the middle switch MS(3,1) from input switch MS(2,1), and the links ML(2,19) and ML(2,20) are connected to the middle switch MS(3,1) from input switch MS(2,5)) and also are connected to exactly d switches in middle stage 160 through two links each for a total of $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected from middle switch MS(3,1) to middle switch MS(4,1), and the links ML(4,3) and ML(4,4) are connected from middle switch MS(3,1) to middle switch MS(4,9)).

Each of the $\frac{N}{d}$ middle switches MS(4,1) – MS(4,16) in the middle stage 160 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected to the middle switch MS(4,1) from input switch MS(3,1), and the links ML(4,35) and ML(4,36) are connected to the middle switch MS(4,1) from input switch MS(3,9)) and also are connected to exactly d switches in middle stage 170 through two links each for a total of $2 \times d$ links (for example the links ML(5,1) and ML(5,2) are connected from middle switch MS(4,1) to middle switch MS(5,1), and the links ML(5,3) and ML(5,4) are connected from middle switch MS(4,1) to middle switch MS(5,9)).

Each of the $\frac{N}{d}$ middle switches MS(5,1) – MS(5,16) in the middle stage 170 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(5,1) and ML(5,2) are connected to the middle switch MS(5,1) from input switch MS(4,1), and the links ML(5,35) and ML(5,36) are connected to the middle switch MS(5,1) from input switch MS(4,9)) and also are connected to exactly d

switches in middle stage 180 through two links each for a total of $2 \times d$ links (for example the links ML(6,1) and ML(6,2) are connected from middle switch MS(5,1) to middle switch MS(6,1), and the links ML(6,3) and ML(6,4) are connected from middle switch MS(5,1) to middle switch MS(6,5)).

- 5 Each of the $\frac{N}{d}$ middle switches MS(6,1) – MS(6,16) in the middle stage 180 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(6,1) and ML(6,2) are connected to the middle switch MS(6,1) from input switch MS(5,1), and the links ML(6,19) and ML(6,20) are connected to the middle switch MS(6,1) from input switch MS(5,5)) and also are connected to exactly d
- 10 switches in middle stage 190 through two links each for a total of $2 \times d$ links (for example the links ML(7,1) and ML(7,2) are connected from middle switch MS(6,1) to middle switch MS(7,1), and the links ML(7,3) and ML(7,4) are connected from middle switch MS(6,1) to middle switch MS(7,3)).

- Each of the $\frac{N}{d}$ middle switches MS(7,1) – MS(7,16) in the middle stage 190 are
- 15 connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(7,1) and ML(7,2) are connected to the middle switch MS(7,1) from input switch MS(6,1), and the links ML(7,11) and ML(7,12) are connected to the middle switch MS(7,1) from input switch MS(6,3)) and also are connected to exactly d
- 20 switches in middle stage 120 through two links each for a total of $2 \times d$ links (for example the links ML(8,1) and ML(8,2) are connected from middle switch MS(7,1) to middle switch MS(8,1), and the links ML(8,3) and ML(8,4) are connected from middle switch MS(7,1) to middle switch OS2).

- Each of the $\frac{N}{d}$ middle switches OS1 – OS16 in the middle stage 120 are
- 25 connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(8,1) and ML(8,2) are connected to the output switch OS1 from input switch MS(7,1), and the links ML(8,7) and ML(7,8) are connected to the output switch OS1 from input switch MS(7,2)).

Finally the connection topology of the network 100A shown in FIG. 1A is known to be back to back inverse Benes connection topology.

Referring to diagram 100B in FIG. 1B, is a folded version of the multi-link multi-stage network 100A shown in FIG. 1A. The network 100B in FIG. 1B shows input stage 110 and output stage 120 are placed together. That is input switch IS1 and output switch OS1 are placed together, input switch IS2 and output switch OS2 are placed together, and similarly input switch IS16 and output switch OS16 are placed together. All the right going middle links {i.e., inlet links IL1 – IL32 and middle links ML(1,1) - ML(1,64)} correspond to input switches IS1 - IS16, and all the left going middle links {i.e., middle links ML(8,1) - ML(8,64) and outlet links OL1-OL32} correspond to output switches OS1 - OS16.

Middle stage 130 and middle stage 190 are placed together. That is middle switches MS(1,1) and MS(7,1) are placed together, middle switches MS(1,2) and MS(7,2) are placed together, and similarly middle switches MS(1,16) and MS(7,16) are placed together. All the right going middle links {i.e., middle links ML(1,1) - ML(1,64) and middle links ML(2,1) – ML(2,64)} correspond to middle switches MS(1,1) – MS(1,16), and all the left going middle links {i.e., middle links ML(7,1) - ML(7,64) and middle links ML(8,1) and ML(8,64)} correspond to middle switches MS(7,1) – MS(7,16).

Middle stage 140 and middle stage 180 are placed together. That is middle switches MS(2,1) and MS(6,1) are placed together, middle switches MS(2,2) and MS(6,2) are placed together, and similarly middle switches MS(2,16) and MS(6,16) are placed together. All the right going middle links {i.e., middle links ML(2,1) - ML(2,64) and middle links ML(3,1) – ML(3,64)} correspond to middle switches MS(2,1) – MS(2,16), and all the left going middle links {i.e., middle links ML(6,1) - ML(6,64) and middle links ML(7,1) and ML(7,64)} correspond to middle switches MS(6,1) – MS(6,16).

Middle stage 150 and middle stage 170 are placed together. That is middle switches MS(3,1) and MS(5,1) are placed together, middle switches MS(3,2) and MS(5,2) are placed together, and similarly middle switches MS(3,16) and MS(5,16) are

placed together. All the right going middle links {i.e., middle links ML(3,1) - ML(3,64) and middle links ML(4,1) – ML(4,64)} correspond to middle switches MS(3,1) – MS(3,16), and all the left going middle links {i.e., middle links ML(5,1) - ML(5,64) and middle links ML(6,1) and ML(6,64)} correspond to middle switches MS(5,1) – MS(5,16).

Middle stage 160 is placed alone. All the right going middle links are the middle links ML(4,1) - ML(4,64) and all the left going middle links are middle links ML(5,1) - ML(5,64).

In one embodiment, in the network 100B of FIG. 1B, the switches that are placed together are implemented as separate switches then the network 100B is the generalized folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages as disclosed in U.S. Provisional Patent Application, Attorney Docket No. M-0039 US that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four by two switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links ML(1,1) – ML(1,4) being the outputs of the input switch IS1; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the output switch OS1 and outlet links OL1 – OL2 being the outputs of the output switch OS1. Similarly in this embodiment of network 100B all the switches that are placed together in each middle stage are implemented as separate switches.

Hypercube Topology layout schemes:

Referring to layout 100C of FIG. 1C, in one embodiment, there are sixteen blocks namely Block 1_2, Block 3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14, Block 15_16, Block 17_18, Block 19_20, Block 21_22, Block 23_24, Block 25_26, Block 27_28, Block 29_30, and Block 31_32. Each block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention. For example Block 1_2 implements the input switch IS1, output Switch OS1,

middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are
 5 denoted by switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4; Middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 100C of FIG. 1C. For example in Block 1_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link
 10 ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 100C of FIG. 1C.

15 Even though it is not illustrated in layout 100C of FIG. 1C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary digital circuit depending on the applications in different embodiments. There are four quadrants in the layout 100C of FIG. 1C namely top-left, bottom-left, top-right and bottom-right quadrants. Top-left quadrant implements Block 1_2, Block 3_4, Block 5_6,
 20 and Block 7_8. Bottom-left quadrant implements Block 9_10, Block 11_12, Block 13_14, and Block 15_16. Top-right quadrant implements Block 17_18, Block 19_20, Block 21_22, and Block 23_24. Bottom-right quadrant implements Block 25_26, Block 27_28, Block 29_30, and Block 31_32. There are two halves in layout 100C of FIG. 1C namely left-half and right-half. Left-half consists of top-left and bottom-left quadrants.
 25 Right-half consists of top-right and bottom-right quadrants.

Recursively in each quadrant there are four sub-quadrants. For example in top-left quadrant there are four sub-quadrants namely top-left sub-quadrant, bottom-left sub-quadrant, top-right sub-quadrant and bottom-right sub-quadrant. Top-left sub-quadrant of top-left quadrant implements Block 1_2. Bottom-left sub-quadrant of top-left quadrant
 30 implements Block 3_4. Top-right sub-quadrant of top-left quadrant implements Block 5_6. Finally bottom-right sub-quadrant of top-left quadrant implements Block 7_8.

Similarly there are two sub-halves in each quadrant. For example in top-left quadrant there are two sub-halves namely left-sub-half and right-sub-half. Left-sub-half of top-left quadrant implements Block 1_2 and Block 3_4. Right-sub-half of top-left quadrant implements Block 5_6 and Block 7_8. Finally applicant notes that in each quadrant or

5 half the blocks are arranged as a general binary hypercube. Recursively in larger multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ where $N_1 = N_2 > 32$, the layout in this embodiment in accordance with the current invention, will be such that the super-quadrants will also be arranged in d-ary hypercube manner. (In the embodiment of the layout 100C of FIG. 1C, it is binary hypercube manner since $d = 2$, in the network $V_{fold-link}(N_1, N_2, d, s)$

10 100B of FIG. 1B).

Layout 100D of FIG. 1D illustrates the inter-block links between switches 1 and 2 of each block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected between switch 1 of Block 1_2 and switch 2 of Block 3_4. Similarly middle links ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block

15 1_2 and switch 1 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100D of FIG. 1D can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(1,4) and ML(8,8) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed

20 single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time division multiplexed single track).

Layout 100E of FIG. 1E illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are connected between switch 2 of Block 1_2 and switch 3 of Block 3_4. Similarly middle

25 links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1_2 and switch 2 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100E of FIG. 1E can be implemented as horizontal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or

30 in an alternative embodiment inter-block links are implemented as a time division

multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

Layout 100F of FIG. 1F illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are connected between switch 3 of Block 1_2 and switch 4 of Block 3_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1_2 and switch 3 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100F of FIG. 1F can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time division multiplexed single track).

Layout 100G of FIG. 1G illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are connected between switch 4 of Block 1_2 and switch 5 of Block 3_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of Block 1_2 and switch 4 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100G of FIG. 1G can be implemented as horizontal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

The complete layout for the network 100B of FIG. 1B is given by combining the links in layout diagrams of 100C, 100D, 100E, 100F, and 100G. Applicant notes that in the layout 100C of FIG. 1C, the inter-block links between switch 1 and switch 2 of corresponding blocks are vertical tracks as shown in layout 100D of FIG. 1D; the inter-block links between switch 2 and switch 3 of corresponding blocks are horizontal tracks as shown in layout 100E of FIG. 1E; the inter-block links between switch 3 and switch 4 of corresponding blocks are vertical tracks as shown in layout 100F of FIG. 1F; and

finally the inter-block links between switch 4 and switch 5 of corresponding blocks are horizontal tracks as shown in layout 100G of FIG. 1G. The pattern is alternate vertical tracks and horizontal tracks. It continues recursively for larger networks of $N > 32$ as will be illustrated later.

- 5 Some of the key aspects of the current invention are discussed. 1) All the switches in one row of the multi-stage network 100B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-block links are either horizontal tracks or vertical tracks; 3) Since all the inter-block links are either horizontal or vertical tracks, all the inter-block links can be mapped on to island-style architectures in current commercial
10 FPGA's; 4) The length of the longest wire is about half of the width (or length) of the complete layout (For example middle link ML(4,4) is about half the width of the complete layout).

- In accordance with the current invention, the layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-link multi-stage
15 network $V_{fold-link}(N_1, N_2, d, s)$ the sub-quadrants, quadrants, and super-quadrants are arranged in d-ary hypercube manner and also the inter-blocks are accordingly connected in d-ary hypercube topology. Even though all the embodiments in the current invention are illustrated for $N_1 = N_2$, the embodiments can be extended for $N_1 \neq N_2$.

- Referring to layout 100H of FIG. 1H, illustrates the extension of layout 100C for the
20 network $V_{fold-link}(N_1, N_2, d, s)$ where $N_1 = N_2 = 128$; $d = 2$; and $s = 2$. There are four super-quadrants in layout 100H namely top-left super-quadrant, bottom-left super-quadrant, top-right super-quadrant, bottom-right super-quadrant. Total number of blocks in the layout 100H is sixty four. Top-left super-quadrant implements the blocks from block 1_2 to block 31_32. Each block in all the super-quadrants has two more switches
25 namely switch 6 and switch 7 in addition to the switches [1-5] illustrated in layout 100C of FIG. 1C. The inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as it is shown in the layouts of FIG. 1D, FIG. 1E, FIG. 1F, and FIG. 1G respectively.

Bottom-left super-quadrant implements the blocks from block 33_34 to block 63_64. Top-right super-quadrant implements the blocks from block 65_66 to block 95_96. And bottom-right super-quadrant implements the blocks from block 97_98 to block 127_128. In all these three super-quadrants also, the inter-block link connection
 5 topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as that of the top-left super-quadrant.

Recursively in accordance with the current invention, the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-left super-quadrant and bottom-left super-quadrant. And similarly the
 10 inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-right super-quadrant and bottom-right super-quadrant. The inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of top-left super-quadrant and top-right super-quadrant. And similarly the inter-block links connecting the switch 6 and switch 7 will be horizontal
 15 tracks between the corresponding switches of bottom-left super-quadrant and bottom-right super-quadrant.

Referring to diagram 100I of FIG. 1I illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized folded multi-link multi-stage network
 20 $V_{fold-link}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$. Block 1_2 in 100I illustrates both the intra-block and inter-block links connected to Block 1_2. The layout diagram 100I corresponds to the embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized folded multi-link multi-stage network
 25 $V_{fold-link}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages as disclosed in U.S. Provisional Patent Application, Attorney Docket No. M-0039 US that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1I are namely input switch IS1 and output switch OS1 belonging to switch 1, illustrated by
 30 dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the

switches implemented are input switch IS1 and output switch OS1); middle switch MS(1,1) and middle switch MS(7,1) belonging to switch 2; middle switch MS(2,1) and middle switch MS(6,1) belonging to switch 3; middle switch MS(3,1) and middle switch MS(5,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

5 Input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links ML(1,1) – ML(1,4) being the outputs of the input switch IS1; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1) – ML(8,4) being the inputs of the output switch OS1 and outlet links OL1 – OL2 being the outputs of the output switch OS1.

10 Middle switch MS(1,1) is implemented as four by four switch with the middle links ML(1,1), ML(1,2), ML(1,7) and ML(1,8) being the inputs and middle links ML(2,1) – ML(2,4) being the outputs; and middle switch MS(7,1) is implemented as four by four switch with the middle links ML(7,1), ML(7,2), ML(7,11) and ML(7,12) being the inputs and middle links ML(8,1) – ML(8,4) being the outputs. Similarly all the other middle
15 switches are also implemented as four by four switches as illustrated in 100I of FIG. 1I.

Now the VLSI layouts of generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 < 32$; $d = 2$; $s = 2$ and its corresponding version of folded generalized multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 < 32$; $d = 2$; $s = 2$ are discussed. Referring to diagram 200A1 of FIG. 2A1 is generalized
20 multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 2$; $d = 2$. Diagram 200A2 of FIG. 2A2 illustrates the corresponding folded generalized multi-link multi-stage network $V_{fold-mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 2$; $d = 2$, version of the diagram 200A1 of FIG. 2A1. Layout 200A3 of FIG. 2A3 illustrates the VLSI layout of the network 200A2 of FIG. 2A2. There is only one block i.e., Block 1_2 comprising switch
25 1. Just like in the layout 100C of FIG. 1C, switch 1 consists of input switch IS1 and output switch OS1.

Referring to diagram 200B1 of FIG. 2B1 is generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 4$; $d = 2$; $s = 2$. Diagram 200B2 of FIG. 2B2 illustrates the corresponding folded generalized multi-link multi-stage network

$V_{fold-link}(N_1, N_2, d, s)$ where $N_1 = N_2 = 4$; $d = 2$; $s = 2$, version of the diagram 200B1 of FIG. 2B1. Layout 200B3 of FIG. 2B3 illustrates the VLSI layout of the network 200B2 of FIG. 2B2. There are two blocks i.e., Block 1_2 and Block 3_4 each comprising switch 1 and switch 2. Switch 1 in each block consists of the corresponding input switch and
 5 output switch. For example switch 1 in Block 1_2 consists of input switch IS1 and output switch OS1. Similarly switch 2 in Block 1_2 consists of middle switch (1,1). Layout 200B4 of FIG. 2B4 illustrates the inter-block links of the VLSI layout diagram 200B3 of FIG. 2B3. For example middle links ML(1,4) and ML(2,8). It must be noted that all the inter-block links are vertical tracks in this layout. (Alternatively all the inter-blocks can
 10 also be implemented as horizontal tracks).

Referring to diagram 200C11 of FIG. 2C11 is generalized multi-link multi-stage network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 8$; $d = 2$; $s = 2$. Diagram 200C12 of FIG. 2C12 illustrates the corresponding folded generalized multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ where $N_1 = N_2 = 8$; $d = 2$; $s = 2$, version of the diagram 200C11 of
 15 FIG. 2C11. Layout 200C21 of FIG. 2C21 illustrates the VLSI layout of the network 200C12 of FIG. 2C12. There are four blocks i.e., Block 1_2, Block 3_4, Block 5_6, and Block 7_8 each comprising switch 1, switch 2 and switch 3. For example switch 1 in Block 1_2 consists of input switch IS1 and output switch OS1; Switch 2 in Block 1_2 consists of MS(1,1) and MS(3,1). Switch 3 in Block 1_2 consists of MS(2,1).

20 Layout 200C22 of FIG. 2C22 illustrates the inter-block links between the switch 1 and switch 2 of the VLSI layout diagram 200C21 of FIG. 2C21. For example middle links ML(1,4) and ML(4,8) are connected between Block 1_2 and Block 3_4. It must be noted that all the inter-block links between switch 1 and switch 2 of all blocks are vertical tracks in this layout. Layout 200C23 of FIG. 2C23 illustrates the inter-block links
 25 between the switch 2 and switch 3 of the VLSI layout diagram 200C21 of FIG. 2C21. For example middle links ML(2,12) and ML(3,4) are connected between Block 1_2 and Block 5_6. It must be noted that all the inter-block links between switch 2 and switch 3 of all blocks are horizontal tracks in this layout

Referring to diagram 200D1 of FIG. 2D1 is generalized multi-link multi-stage
 30 network $V_{mlink}(N_1, N_2, d, s)$ where $N_1 = N_2 = 16$; $d = 2$; $s = 2$. Diagram 200D2 of FIG.

- 2D2 illustrates the corresponding folded generalized multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ where $N_1 = N_2 = 16$; $d = 2$; $s = 2$, version of the diagram 200D1 of FIG. 2D1. Layout 200D3 of FIG. 2D3 illustrates the VLSI layout of the network 200D2 of FIG. 2D2. There are eight blocks i.e., Block 1_2, Block 3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14 and Block 15_16 each comprising switch 1, switch 2, switch 3 and switch 4. For example switch 1 in Block 1_2 consists of input switch IS1 and output switch OS1; Switch 2 in Block 1_2 consists of MS(1,1) and MS(5,1). Switch 3 in Block 1_2 consists of MS(2,1) and MS(4,1), and switch 4 in Block 1_2 consists of MS(3,1).
- Layout 200D4 of FIG. 2D4 illustrates the inter-block links between the switch 1 and switch 2 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(1,4) and ML(6,8) are connected between Block 1_2 and Block 3_4. It must be noted that all the inter-block links between switch 1 and switch 2 of all blocks are vertical tracks in this layout. Layout 200D5 of FIG. 2D5 illustrates the inter-block links between the switch 2 and switch 3 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(2,12) and ML(5,4) are connected between Block 1_2 and Block 5_6. It must be noted that all the inter-block links between switch 2 and switch 3 of all blocks are horizontal tracks in this layout. Layout 200D6 of FIG. 2D6 illustrates the inter-block links between the switch 3 and switch 4 of the VLSI layout diagram 200D3 of FIG. 2D3. For example middle links ML(3,4) and ML(4,20) are connected between Block 1_2 and Block 9_10. It must be noted that all the inter-block links between switch 3 and switch 4 of all blocks are vertical tracks in this layout.

Generalized Multi-link Butterfly Fat Tree Network Embodiment:

- In another embodiment in the network 100B of FIG. 1B, the switches that are placed together are implemented as combined switch then the network 100B is the generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with five stages as disclosed in U.S. Provisional Patent Application, Attorney Docket No. M-0040 US that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a six by six switch. For example the input switch IS1 and output switch OS1 are placed

together; so input switch IS1 and output OS1 are implemented as a six by six switch with the inlet links IL1, IL2, ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the combined switch (denoted as IS1&OS1) and middle links ML(1,1), ML(1,2), ML(1,3), ML(1,4), OL1 and OL2 being the outputs of the combined switch IS1&OS1. Similarly in
 5 this embodiment of network 100B all the switches that are placed together are implemented as a combined switch.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with five stages. The layout
 10 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$.

Referring to diagram 100J of FIG. 1J illustrates a high-level implementation of
 15 Block 1_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$. Block 1_2 in 100J illustrates both the intra-block and inter-block links. The layout diagram 100J corresponds to the embodiment where the switches that are placed together are implemented as combined
 20 switch in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized multi-link butterfly fat tree network $V_{mlink-bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with five stages as disclosed in U.S. Provisional Patent Application, Attorney Docket No. M-0040 US that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1J are
 25 namely the combined input and output switch IS1&OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switch implemented is combined input and output switch IS1&OS1); middle switch MS(1,1) belonging to switch 2; middle switch MS(2,1) belonging to switch 3; middle switch MS(3,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Combined input and output switch IS1&OS1 is implemented as six by six switch with the inlet links IL1, IL2 and ML(8,1) – ML(8,4) being the inputs and middle links ML(1,1) – ML(1,4), and outlet links OL1 – OL2 being the outputs.

5 Middle switch MS(1,1) is implemented as eight by eight switch with the middle links ML(1,1), ML(1,2), ML(1,7), ML(1,8), ML(7,1), ML(7,2), ML(7,11) and ML(7,12) being the inputs and middle links ML(2,1) – ML(2,4) and middle links ML(8,1) – ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as eight by eight switches as illustrated in 100J of FIG. 1J.

10 In another embodiment, middle switch MS(1,1) (or the middle switches in any of the middle stage excepting the root middle stage) of Block 1_2 of $V_{mlink-bft}(N_1, N_2, d, s)$ can be implemented as a four by eight switch and a four by four switch to save cross points. This is because the left going middle links of these middle switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1_2 as shown FIG. 1J, the left going middle links namely ML(7,1), ML(7,2), ML(7,11), and ML(7,12) are never switched to the right going middle links ML(2,1), ML(2,2), ML(2,3), and ML(2,4). And hence to implement MS(1,1) two switches namely: 1) a four by eight switch with the middle links ML(1,1), ML(1,2), ML(1,7), and ML(1,8) as inputs and the middle links ML(2,1), ML(2,2), ML(2,3), ML(2,4), ML(8,1), ML(8,2), ML(8,3), and ML(8,4) as outputs and 2) a four by four switch with the middle links ML(7,1), ML(7,2), ML(7,11), and ML(7,12) as inputs and the middle links ML(8,1), ML(8,2), ML(8,3), and ML(8,4) as outputs are sufficient without losing any connectivity of the embodiment of MS(1,1) being implemented as an eight by eight switch as described before.)

Generalized multi-stage network Embodiment:

25 In one embodiment, in the network 100B of FIG. 1B, the switches that are placed together are implemented as two separate switches in input stage 110 and output stage 120; and as four separate switches in all the middle stages, then the network 100B is the generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages as disclosed in U.S. Provisional Patent Application, Attorney Docket No. M-0041 US that is incorporated by reference above. That is the switches that

are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four by two switch respectively. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs and middle links
 5 ML(1,1) – ML(1,4) being the outputs; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,4), ML(8,7) and ML(8,8) being the inputs and outlet links OL1 – OL2 being the outputs.

The switches, corresponding to the middle stages that are placed together are implemented as four two by two switches. For example middle switches MS(1,1),
 10 MS(1,17), MS(7,1), and MS(7,17) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,7) being the inputs and middle links ML(2,1) and ML(2,3) being the outputs; middle switch MS(1,17) is implemented as two by two switch with the middle links ML(1,2) and ML(1,8) being the inputs and middle links ML(2,2) and ML(2,4) being the outputs; middle switch
 15 MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,11) being the inputs and middle links ML(8,1) and ML(8,3) being the outputs; And middle switch MS(7,17) is implemented as two by two switch with the middle links ML(7,2) and ML(7,12) being the inputs and middle links ML(8,2) and ML(8,4) being the outputs; Similarly in this embodiment of network 100B all the switches that are placed together
 20 are implemented as separate switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized folded multi-stage network
 $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-
 25 stage network $V_{fold}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$.

Referring to diagram 100K of FIG. 1K illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) of the layout 100C of FIG. 1C which represents a generalized folded multi-stage network
 30 $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$. Block 1_2 in 100K illustrates

both the intra-block and inter-block links. The layout diagram 100K corresponds to the embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$;
 5 and $s = 2$ with nine stages as disclosed in U.S. Provisional Patent Application, Attorney Docket No. M-0041 US that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1K are namely the input switch IS1 and output switch OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the
 10 switches implemented are input switch IS1 and output switch OS1); middle switches MS(1,1), MS(1,17), MS(7,1) and MS(7,17) belonging to switch 2; middle switches MS(2,1), MS(2,17), MS(6,1) and MS(6,17) belonging to switch 3; middle switches MS(3,1), MS(3,17), MS(5,1) and MS(5,17) belonging to switch 4; And middle switches MS(4,1), and MS(4,17) belonging to switch 5.

15 Input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,4) being the outputs; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,4), ML(8,7) and ML(8,8) being the inputs and outlet links OL1 – OL2 being the outputs.

20 Middle switches MS(1,1), MS(1,17), MS(7,1), and MS(7,17) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,7) being the inputs and middle links ML(2,1) and ML(2,3) being the outputs; middle switch MS(1,17) is implemented as two by two switch with the middle links ML(1,2) and ML(1,8) being the inputs and middle links ML(2,2) and ML(2,4) being
 25 the outputs; middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,11) being the inputs and middle links ML(8,1) and ML(8,3) being the outputs; And middle switch MS(7,17) is implemented as two by two switch with the middle links ML(7,2) and ML(7,12) being the inputs and middle links ML(8,2) and ML(8,4) being the outputs. Similarly all the other middle switches are also
 30 implemented as two by two switches as illustrated in 100K of FIG. 1K.

Generalized multi-stage network Embodiment with $S = 1$:

In one embodiment, in the network 100B of FIG. 1B (where it is implemented with $s = 1$), the switches that are placed together are implemented as two separate switches in input stage 110 and output stage 120; and as two separate switches in all the middle stages, then the network 100B is the generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 1$ with nine stages as disclosed in U.S. Provisional Patent Application, Attorney Docket No. M-0041 US that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a two by two switch and a two by two switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by two switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,2) being the outputs; and output switch OS1 is implemented as two by two switch with the middle links ML(8,1) and ML(8,3) being the inputs and outlet links OL1 – OL2 being the outputs.

The switches, corresponding to the middle stages that are placed together are implemented as two, two by two switches. For example middle switches MS(1,1) and MS(7,1) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,3) being the inputs and middle links ML(2,1) and ML(2,2) being the outputs; middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,5) being the inputs and middle links ML(8,1) and ML(8,2) being the outputs; Similarly in this embodiment of network 100B all the switches that are placed together are implemented as two separate switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 1$ with nine stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$.

Referring to diagram 100K1 of FIG. 1K1 illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) for the layout 100C of FIG. 1C when $s = 1$ which represents a generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 1$ (All the double links are replaced by single links when $s = 1$). Block 1_2 in 100K1 illustrates both the intra-block and inter-block links. The layout diagram 100K1 corresponds to the embodiment where the switches that are placed together are implemented as separate switches in the network 100B of FIG. 1B when $s = 1$. As noted before then the network 100B is the generalized folded multi-stage network $V_{fold}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 1$ with nine stages as disclosed in U.S. Provisional Patent Application, Attorney Docket No. M-0041 US that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1K1 are namely the input switch IS1 and output switch OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switches MS(1,1) and MS(7,1) belonging to switch 2; middle switches MS(2,1) and MS(6,1) belonging to switch 3; middle switches MS(3,1) and MS(5,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by two switch with the inlet links IL1 and IL2 being the inputs and middle links ML(1,1) – ML(1,2) being the outputs; and output switch OS1 is implemented as two by two switch with the middle links ML(8,1) and ML(8,3) being the inputs and outlet links OL1 – OL2 being the outputs.

Middle switches MS(1,1) and MS(7,1) are placed together; so middle switch MS(1,1) is implemented as two by two switch with middle links ML(1,1) and ML(1,3) being the inputs and middle links ML(2,1) and ML(2,2) being the outputs; And middle switch MS(7,1) is implemented as two by two switch with middle links ML(7,1) and ML(7,5) being the inputs and middle links ML(8,1) and ML(8,2) being the outputs. Similarly all the other middle switches are also implemented as two by two switches as illustrated in 100K1 of FIG. 1K1.

Generalized Butterfly Fat Tree Network Embodiment:

In another embodiment in the network 100B of FIG. 1B, the switches that are placed together are implemented as two combined switches then the network 100B is the generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with five stages as disclosed in U.S. Provisional Patent Application, Attorney Docket No. M-0038 US that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a six by six switch. For example the input switch IS1 and output switch OS1 are placed together; so input output switch IS1&OS1 are implemented as a six by six switch with the inlet links IL1, IL2, ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the combined switch (denoted as IS1&OS1) and middle links ML(1,1), ML(1,2), ML(1,3), ML(1,4), OL1 and OL2 being the outputs of the combined switch IS1&OS1.

The switches, corresponding to the middle stages that are placed together are implemented as two four by four switches. For example middle switches MS(1,1) and MS(1,17) are placed together; so middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,7), ML(7,1) and ML(7,11) being the inputs and middle links ML(2,1), ML(2,3), ML(8,1) and ML(8,3) being the outputs; middle switch MS(1,17) is implemented as four by four switch with the middle links ML(1,2), ML(1,8), ML(7,2) and ML(7,12) being the inputs and middle links ML(2,2), ML(2,4), ML(8,2) and ML(8,4) being the outputs. Similarly in this embodiment of network 100B all the switches that are placed together are implemented as a two combined switches.

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with five stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$.

Referring to diagram 100L of FIG. 1L illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) of the layout 100C of

FIG. 1C which represents a generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$. Block 1_2 in 100L illustrates both the intra-block and inter-block links. The layout diagram 100L corresponds to the embodiment where the switches that are placed together are implemented as two combined switches in the network 100B of FIG. 1B. As noted before then the network 100B is the generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with five stages as disclosed in U.S. Provisional Patent Application, Attorney Docket No. M-0038 US that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1L are namely the combined input and output switch IS1&OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switch implemented is combined input and output switch IS1&OS1); middle switch MS(1,1) and MS(1,17) belonging to switch 2; middle switch MS(2,1) and MS(2,17) belonging to switch 3; middle switch MS(3,1) and MS(3,17) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Combined input and output switch IS1&OS1 is implemented as six by six switch with the inlet links IL1, IL2, ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs and middle links ML(1,1) – ML(1,4) and outlet links OL1 – OL2 being the outputs.

Middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,7), ML(7,1) and ML(7,11) being the inputs and middle links ML(2,1), ML(2,3), ML(8,1) and ML(8,3) being the outputs; And middle switch MS(1,17) is implemented as four by four switch with the middle links ML(1,2), ML(1,8), ML(7,2) and ML(7,12) being the inputs and middle links ML(2,2), ML(2,4), ML(8,2) and ML(8,4) being the outputs. Similarly all the other middle switches are also implemented as two four by four switches as illustrated in 100L of FIG. 1L.

In another embodiment, middle switch MS(1,1) (or the middle switches in any of the middle stage excepting the root middle stage) of Block 1_2 of $V_{mlink-bft}(N_1, N_2, d, s)$ can be implemented as a two by four switch and a two by two switch to save cross points. This is because the left going middle links of these middle

switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1_2 as shown FIG. 1L, the left going middle links namely ML(7,1) and ML(7,11) are never switched to the right going middle links ML(2,1) and ML(2,3). And hence to implement MS(1,1) two switches namely: 1) a two by four switch with the middle links ML(1,1) and ML(1,7) as inputs and the middle links ML(2,1), ML(2,3), ML(8,1), and ML(8,3) as outputs and 2) a two by two switch with the middle links ML(7,1) and ML(7,11) as inputs and the middle links ML(8,1) and ML(8,3) as outputs are sufficient without losing any connectivity of the embodiment of MS(1,1) being implemented as an eight by eight switch as described before.)

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Generalized Butterfly Fat Tree Network Embodiment with S = 1:

In one embodiment, in the network 100B of FIG. 1B (where it is implemented with $s = 1$), the switches that are placed together are implemented as a combined switch in input stage 110 and output stage 120; and as a combined switch in all the middle stages, then the network 100B is the generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 1$ with five stages as disclosed in U.S. Provisional Patent Application, Attorney Docket No. M-0038 US that is incorporated by reference above. That is the switches that are placed together in input stage 110 and output stage 120 are implemented as a four by four switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input and output switch IS1&OS1 is implemented as four by four switch with the inlet links IL1, IL2, ML(8,1) and ML(8,3) being the inputs and middle links ML(1,1) – ML(1,2) and outlet links OL1 – OL2 being the outputs

The switches, corresponding to the middle stages that are placed together are implemented as a four by four switch. For example middle switches MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,3), ML(7,1) and ML(7,5) being the inputs and middle links ML(2,1), ML(2,2), ML(8,1) and ML(8,2) being the outputs..

Layout diagrams 100C in FIG. 1C, 100D in FIG. 1D, 100E in FIG. 1E, 100F in FIG. 1G are also applicable to generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 1$ with five stages. The layout 100C in FIG. 1C can be recursively extended for any arbitrarily large generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$. Accordingly layout 100H of FIG. 1H is also applicable to generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$.

Referring to diagram 100L1 of FIG. 1L1 illustrates a high-level implementation of Block 1_2 (Each of the other blocks have similar implementation) for the layout 100C of FIG. 1C when $s = 1$ which represents a generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 1$ (All the double links are replaced by single links when $s = 1$). Block 1_2 in 100K1 illustrates both the intra-block and inter-block links. The layout diagram 100L1 corresponds to the embodiment where the switches that are placed together are implemented as a combined switch in the network 100B of FIG. 1B when $s = 1$. As noted before then the network 100B is the generalized butterfly fat tree network $V_{bft}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 1$ with nine stages as disclosed in U.S. Provisional Patent Application, Attorney Docket No. M-0038 US that is incorporated by reference above.

That is the switches that are placed together in Block 1_2 as shown in FIG. 1L1 are namely the input and output switch IS1&OS1 belonging to switch 1, illustrated by dotted lines, (as noted before switch 1 is for illustration purposes only, in practice the switches implemented are input switch IS1 and output switch OS1); middle switch MS(1,1) belonging to switch 2; middle switch MS(2,1) belonging to switch 3; middle switch MS(3,1) belonging to switch 4; And middle switch MS(4,1) belonging to switch 5.

Input and output switch IS1&OS1 are placed together; so input and output switch IS1&OS1 is implemented as four by four switch with the inlet links IL1, IL2, ML(8,1) and ML(8,3) being the inputs and middle links ML(1,1) – ML(1,2) and outlet links OL1 – OL2 being the outputs.

Middle switch MS(1,1) is implemented as four by four switch with middle links ML(1,1), ML(1,3), ML(7,1) and ML(7,5) being the inputs and middle links ML(2,1),

ML(2,2), ML(8,1) and ML(8,2) being the outputs. Similarly all the other middle switches are also implemented as four by four switches as illustrated in 100L1 of FIG. 1L1.

In another embodiment, middle switch MS(1,1) (or the middle switches in any of the middle stage excepting the root middle stage) of Block 1_2 of

- 5 $V_{m\text{link-bft}}(N_1, N_2, d, s)$ can be implemented as a two by four switch and a two by two switch to save cross points. This is because the left going middle links of these middle switches are never setup to the right going middle links. For example, in middle switch MS(1,1) of Block 1_2 as shown FIG. 1L1, the left going middle links namely ML(7,1) and ML(7,5) are never switched to the right going middle links ML(2,1) and ML(2,2).
- 10 And hence to implement MS(1,1) two switches namely: 1) a two by four switch with the middle links ML(1,1) and ML(1,3) as inputs and the middle links ML(2,1), ML(2,2), ML(8,1), and ML(8,2) as outputs and 2) a two by two switch with the middle links ML(7,1) and ML(7,5) as inputs and the middle links ML(8,1) and ML(8,2) as outputs are sufficient without loosing any connectivity of the embodiment of MS(1,1) being
- 15 implemented as an eight by eight switch as described before.)

Hypercube-like Topology layout schemes:

- Referring to diagram 300A in FIG. 3A, in one embodiment, an exemplary generalized multi-link multi-stage network $V_{m\text{link}}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d =$
- 20 2; and $s = 2$ with nine stages of one hundred and forty four switches for satisfying communication requests, such as setting up a telephone call or a data call, or a connection between configurable logic blocks, between an input stage 110 and output stage 120 via middle stages 130, 140, 150, 170, 170, 180 and 190 is shown where input stage 110 consists of sixteen, two by four switches IS1-IS16 and output stage 120 consists of
 - 25 sixteen, four by two switches OS1-OS16.

As disclosed in U.S. Provisional Patent Application, Attorney Docket No. M-0039 US that is incorporated by reference above, such a network can be operated in rearrangeably non-blocking manner for arbitrary fan-out multicast connections and also can be operated in strictly non-blocking manner for unicast connections.

The diagram 300A in FIG. 3A is exactly the same as the diagram 100A in FIG. 1A excepting the connection links between middle stage 150 and middle stage 160 as well as between middle stage 160 and middle stage 170.

Each of the $\frac{N}{d}$ middle switches are connected to exactly d switches in middle stage 160 through two links each for a total of $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected from middle switch MS(3,1) to middle switch MS(4,1), and the links ML(4,3) and ML(4,4) are connected from middle switch MS(3,1) to middle switch MS(4,15)).

Each of the $\frac{N}{d}$ middle switches MS(4,1) – MS(4,16) in the middle stage 160 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(4,1) and ML(4,2) are connected to the middle switch MS(4,1) from input switch MS(3,1), and the links ML(4,59) and ML(4,60) are connected to the middle switch MS(4,1) from input switch MS(3,15)) and also are connected to exactly d switches in middle stage 170 through two links each for a total of $2 \times d$ links (for example the links ML(5,1) and ML(5,2) are connected from middle switch MS(4,1) to middle switch MS(5,1), and the links ML(5,3) and ML(5,4) are connected from middle switch MS(4,1) to middle switch MS(5,15)).

Each of the $\frac{N}{d}$ middle switches MS(5,1) – MS(5,16) in the middle stage 170 are connected from exactly d input switches through two links each for a total of $2 \times d$ links (for example the links ML(5,1) and ML(5,2) are connected to the middle switch MS(5,1) from input switch MS(4,1), and the links ML(5,59) and ML(5,60) are connected to the middle switch MS(5,1) from input switch MS(4,15)).

Finally the connection topology of the network 100A shown in FIG. 1A is also basically back to back inverse Benes connection topology but with a slight variation. All the cross middle links from middle switches MS(3,1) - MS(3,8) connect to middle switches MS(4,9) – MS(4,16) and all the cross middle links from middle switches MS(3,9) - MS(3,16) connect to middle switches MS(4,1) – MS(4,8). Applicant makes a

key observation that there are many combinations of connections possible using this property. The difference in the connection topology between diagram 100A of FIG. 1A and diagram 300A of FIG. 3A is that the connections formed by cross middle links between middle stage 150 and middle stage 160 are made of two different combinations
 5 otherwise both the diagrams 100A and 300A implement back to back inverse Benes connection topology. Since these networks implement back to back inverse Benes topologies since there is difference in the connections of cross middle links between middle stage 150 and middle stage 160, the same difference in the connections of cross middle links between 160 and middle stage 170 occurs.

10 Referring to diagram 300B in FIG. 3B, is a folded version of the multi-link multi-stage network 300A shown in FIG. 3A. The network 300B in FIG. 3B shows input stage 110 and output stage 120 are placed together. That is input switch IS1 and output switch OS1 are placed together, input switch IS2 and output switch OS2 are placed together, and similarly input switch IS16 and output switch OS16 are placed together. All the right
 15 going middle links {i.e., inlet links IL1 – IL32 and middle links ML(1,1) - ML(1,64)} correspond to input switches IS1 - IS16, and all the left going middle links {i.e., middle links ML(7,1) - ML(7,64) and outlet links OL1-OL32} correspond to output switches OS1 - OS16.

Just the same way there is difference in the connection topology between diagram
 20 100A of FIG. 1A and diagram 300A of FIG. 3A in the way the connections are formed by cross middle links between middle stage 150 and middle stage 160 and also between middle stage 160 and middle stage 170, the exact similar difference is there between the diagram 100B of FIG. 1B and the diagram 300B of FIG. 3B, i.e., in the way the connections are formed by cross middle links between middle stage 150 and middle stage
 25 160 and also between middle stage 160 and middle stage 170.

In one embodiment, in the network 300B of FIG. 3B, the switches that are placed together are implemented as separate switches then the network 300B is the generalized folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ where $N_1 = N_2 = 32$; $d = 2$; and $s = 2$ with nine stages as disclosed in U.S. Provisional Patent Application, Attorney
 30 Docket No. M-0039 US that is incorporated by reference above. That is the switches that

are placed together in input stage 110 and output stage 120 are implemented as a two by four switch and a four by two switch. For example the switch input switch IS1 and output switch OS1 are placed together; so input switch IS1 is implemented as two by four switch with the inlet links IL1 and IL2 being the inputs of the input switch IS1 and middle links ML(1,1) – ML(1,4) being the outputs of the input switch IS1; and output switch OS1 is implemented as four by two switch with the middle links ML(8,1), ML(8,2), ML(8,7) and ML(8,8) being the inputs of the output switch OS1 and outlet links OL1 – OL2 being the outputs of the output switch OS1. Similarly in this embodiment of network 300B all the switches that are placed together are implemented as separate switches.

Referring to layout 300C of FIG. 3C, in one embodiment, there are sixteen blocks namely Block 1_2, Block 3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14, Block 15_16, Block 17_18, Block 19_20, Block 21_22, Block 23_24, Block 25_26, Block 27_28, Block 29_30, and Block 31_32. Each block implements all the switches in one row of the network 300B of FIG. 3B, one of the key aspects of the current invention. For example Block 1_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1; Middle switch MS(1,1) and middle switch MS(7,1) together are denoted as switch 2; Middle switch MS(2,1) and middle switch MS(6,1) together are denoted as switch 3; Middle switch MS(3,1) and middle switch MS(5,1) together are denoted as switch 4; And middle switch MS(4,1) is denoted as switch 5.

All the straight middle links are illustrated in layout 300C of FIG. 3C. For example in Block 1_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are illustrated in layout 300C of FIG. 3C.

Even though it is not illustrated in layout 300C of FIG. 3C, in each block, in addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary

digital circuit depending on the applications in different embodiments. There are four quadrants in the layout 300C of FIG. 3C namely top-left, bottom-left, top-right and bottom-right quadrants. Top-left quadrant implements Block 1_2, Block 3_4, Block 5_6, and Block 7_8. Bottom-left quadrant implements Block 9_10, Block 11_12, Block 13_14, and Block 15_16. Top-right quadrant implements Block 25_26, Block 27_28, Block 29_30, and Block 31_32. Bottom-right quadrant implements Block 17_18, Block 19_20, Block 21_22, and Block 23_24. There are two halves in layout 300C of FIG. 3C namely left-half and right-half. Left-half consists of top-left and bottom-left quadrants. Right-half consists of top-right and bottom-right quadrants.

10 Recursively in each quadrant there are four sub-quadrants. For example in top-left quadrant there are four sub-quadrants namely top-left sub-quadrant, bottom-left sub-quadrant, top-right sub-quadrant and bottom-right sub-quadrant. Top-left sub-quadrant of top-left quadrant implements Block 1_2. Bottom-left sub-quadrant of top-left quadrant implements Block 3_4. Top-right sub-quadrant of top-left quadrant implements Block 7_8. Finally bottom-right sub-quadrant of top-left quadrant implements Block 5_6. Similarly there are two sub-halves in each quadrant. For example in top-left quadrant there are two sub-halves namely left-sub-half and right-sub-half. Left-sub-half of top-left quadrant implements Block 1_2 and Block 3_4. Right-sub-half of top-left quadrant implements Block 7_8 and Block 5_6. Recursively in larger multi-stage network

15 $V_{fold-link}(N_1, N_2, d, s)$ where $N_1 = N_2 > 32$, the layout in this embodiment in accordance with the current invention, will be such that the super-quadrants will also be arranged in a similar manner.

Layout 300D of FIG. 3D illustrates the inter-block links (in the layout 300C of FIG. 3C all the cross middle links are inter-block links) between switches 1 and 2 of each block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected between switch 1 of Block 1_2 and switch 2 of Block 3_4. Similarly middle links ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block 1_2 and switch 1 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 100D of FIG. 1D can be implemented as vertical tracks in one embodiment. Also in one

25 embodiment inter-block links are implemented as two different tracks (for example middle links ML(1,4) and ML(8,8) are implemented as two different tracks); or in an

30

alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time division multiplexed single track).

Layout 300E of FIG. 3E illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are connected between switch 2 of Block 1_2 and switch 3 of Block 3_4. Similarly middle links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1_2 and switch 2 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 300E of FIG. 3E can be implemented as diagonal tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

Layout 300F of FIG. 3F illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are connected between switch 3 of Block 1_2 and switch 4 of Block 3_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1_2 and switch 3 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 300F of FIG. 3F can be implemented as vertical tracks in one embodiment. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time division multiplexed single track).

Layout 300G of FIG. 3G illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are connected between switch 4 of Block 1_2 and switch 5 of Block 3_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of Block 1_2 and switch 4 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 300G of FIG. 3G can be implemented as horizontal tracks in one embodiment.

Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

The complete layout for the network 300B of FIG. 3B is given by combining the links in layout diagrams of 300C, 300D, 300E, 300F, and 300G. Applicant notes that in the layout 300C of FIG. 3C, the inter-block links between switch 1 and switch 2 are vertical tracks as shown in layout 300D of FIG. 3D; the inter-block links between switch 2 and switch 3 are horizontal tracks as shown in layout 300E of FIG. 3E; the inter-block links between switch 3 and switch 4 are vertical tracks as shown in layout 300F of FIG. 3F; and finally the inter-block links between switch 4 and switch 5 are horizontal tracks as shown in layout 300G of FIG. 3G. The pattern is either vertical tracks, horizontal tracks or diagonal tracks. It continues recursively for larger networks of $N > 32$ as will be illustrated later.

Some of the key aspects of the current invention related to layout diagram 300C of FIG. 3C are noted. 1) All the switches in one row of the multi-stage network 300B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-block links are either horizontal tracks, vertical tracks or diagonal tracks; 3) The length of the longest wire is about half of the width (or length) of the complete layout (For example middle link ML(4,4) is about half the width of the complete layout.);

The layout 300C in FIG. 3C can be recursively extended for any arbitrarily large generalized folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$. Referring to layout 300H of FIG. 3H, illustrates the extension of layout 300C for the network $V_{fold-link}(N_1, N_2, d, s)$ where $N_1 = N_2 = 128$; $d = 2$; and $s = 2$. There are four super-quadrants in layout 300H namely top-left super-quadrant, bottom-left super-quadrant, top-right super-quadrant, bottom-right super-quadrant. Total number of blocks in the layout 300H is sixty four. Top-left super-quadrant implements the blocks from block 1_2 to block 31_32. Each block in all the super-quadrants has two more switches namely switch 6 and switch 7 in addition to the switches [1-5] illustrated in layout 300C of FIG.

3C. The inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as it is shown in the layouts of FIG. 3D, FIG. 3E, FIG. 3F, and FIG. 3G respectively.

Bottom-left super-quadrant implements the blocks from block 33_34 to block 63_64. Top-right super-quadrant implements the blocks from block 65_66 to block 95_96. And bottom-right super-quadrant implements the blocks from block 97_98 to block 127_128. In all these three super-quadrants also, the inter-block link connection topology is the exactly the same between the switches 1 and 2; switches 2 and 3; switches 3 and 4; switches 4 and 5 as that of the top-left super-quadrant.

10 Recursively in accordance with the current invention, the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-left super-quadrant and bottom-left super-quadrant. And similarly the inter-block links connecting the switch 5 and switch 6 will be vertical tracks between the corresponding switches of top-right super-quadrant and bottom-right super-quadrant. The
15 inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of top-left super-quadrant and top-right super-quadrant. And similarly the inter-block links connecting the switch 6 and switch 7 will be horizontal tracks between the corresponding switches of bottom-left super-quadrant and bottom-right super-quadrant.

20 **Ring Topology layout schemes:**

Layout diagram 400C of FIG. 4C is another embodiment for the generalized folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ diagram 100B in FIG. 1B.

Referring to layout 400C of FIG. 4C, there are sixteen blocks namely Block 1_2, Block 3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14, Block 15_16,
25 Block 17_18, Block 19_20, Block 21_22, Block 23_24, Block 25_26, Block 27_28, Block 29_30, and Block 31_32. Each block implements all the switches in one row of the network 100B of FIG. 1B, one of the key aspects of the current invention. For example Block 1_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch
30 MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of

illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1;
 Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2;
 Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3;
 Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4;
 5 And middle switch MS(4,1) is denoted by switch 5.

All the straight middle links are illustrated in layout 400C of FIG. 4C. For
 example in Block 1_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link
 ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link
 ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link
 10 ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link
 ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are
 illustrated in layout 400C of FIG. 4C.

Even though it is not illustrated in layout 400C of FIG. 4C, in each block, in
 addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary
 15 digital circuit depending on the applications in different embodiments. The topology of
 the layout 400C in FIG. 4C is a ring. For each of the neighboring rows in diagram 100B
 of FIG. 1B the corresponding blocks are also physically neighbors in layout diagram
 400C of FIG. 4C. In addition the topmost row is also logically considered as neighbor to
 the bottommost row. For example Block 1_2 (implementing the switches belonging to a
 20 row in diagram 100B of FIG. 1B) has Block 3_4 as neighbor since Block 3_4 implements
 the switches in its neighboring row. Similarly Block 1_2 also has Block 31_32 as
 neighbor since Block 1_2 implements topmost row of switches and Block 31_32
 implements bottommost row of switches in diagram 100B of FIG. 1B. The ring layout
 scheme illustrated in 400C of FIG. 4C can be generalized for a large multi-stage network
 25 $V_{fold-link}(N_1, N_2, d, s)$ where $N_1 = N_2 > 32$, in accordance with the current invention.

Layout 400B of FIG. 4B illustrates the inter-block links (in the layout 400A of
 FIG. 4A all the cross middle links are inter-block links) between switches 1 and 2 of each
 block. For example middle links ML(1,3), ML(1,4), ML(8,7), and ML(8,8) are connected
 between switch 1 of Block 1_2 and switch 2 of Block 3_4. Similarly middle links
 30 ML(1,7), ML(1,8), ML(8,3), and ML(8,4) are connected between switch 2 of Block 1_2

and switch 1 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 400B of FIG. 4B are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(1,4) and ML(8,8) are implemented as two different
5 tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(1,4) and ML(8,8) are implemented as a time division multiplexed single track).

Layout 400C of FIG. 4C illustrates the inter-block links between switches 2 and 3 of each block. For example middle links ML(2,3), ML(2,4), ML(7,11), and ML(7,12) are
10 connected between switch 2 of Block 1_2 and switch 3 of Block 3_4. Similarly middle links ML(2,11), ML(2,12), ML(7,3), and ML(7,4) are connected between switch 3 of Block 1_2 and switch 2 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 400C of FIG. 4C are implemented as vertical tracks or horizontal tracks or diagonal tracks. Also in one embodiment inter-block links are implemented as two
15 different tracks (for example middle links ML(2,12) and ML(7,4) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(2,12) and ML(7,4) are implemented as a time division multiplexed single track).

Layout 400D of FIG. 4D illustrates the inter-block links between switches 3 and 4 of each block. For example middle links ML(3,3), ML(3,4), ML(6,19), and ML(6,20) are
20 connected between switch 3 of Block 1_2 and switch 4 of Block 3_4. Similarly middle links ML(3,19), ML(3,20), ML(6,3), and ML(6,4) are connected between switch 4 of Block 1_2 and switch 3 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 400D of FIG. 4D are implemented as vertical tracks or horizontal tracks or
25 diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(3,4) and ML(6,20) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(3,4) and ML(6,20) are implemented as a time division multiplexed single track).

Layout 400E of FIG. 4E illustrates the inter-block links between switches 4 and 5 of each block. For example middle links ML(4,3), ML(4,4), ML(5,35), and ML(5,36) are

connected between switch 4 of Block 1_2 and switch 5 of Block 3_4. Similarly middle links ML(4,35), ML(4,36), ML(5,3), and ML(5,4) are connected between switch 5 of Block 1_2 and switch 4 of Block 3_4. Applicant notes that the inter-block links illustrated in layout 400E of FIG. 4E are implemented as vertical tracks or horizontal tracks or
 5 diagonal tracks. Also in one embodiment inter-block links are implemented as two different tracks (for example middle links ML(4,4) and ML(5,36) are implemented as two different tracks); or in an alternative embodiment inter-block links are implemented as a time division multiplexed single track (for example middle links ML(4,4) and ML(5,36) are implemented as a time division multiplexed single track).

10 The complete layout for the network 100B of FIG. 1B is given by combining the links in layout diagrams of 400A, 400B, 400C, 400D, and 400E.

Some of the key aspects of the current invention related to layout diagram 400A of FIG. 4A are noted. 1) All the switches in one row of the multi-stage network 100B are implemented in a single block. 2) The blocks are placed in such a way that all the inter-
 15 block links are either horizontal tracks, vertical tracks or diagonal tracks; 3) Length of the different wires between the same two middle stages is not the same. However it gives an opportunity to implement the most connected circuits to place and route through the blocks which have shorter wires.

Layout diagram 400C1 of FIG. 4C1 is another embodiment for the generalized
 20 folded multi-link multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ diagram 100B in FIG. 1B. Referring to layout 400C1 of FIG. 4C1, there are sixteen blocks namely Block 1_2, Block 3_4, Block 5_6, Block 7_8, Block 9_10, Block 11_12, Block 13_14, Block 15_16, Block 17_18, Block 19_20, Block 21_22, Block 23_24, Block 25_26, Block 27_28, Block 29_30, and Block 31_32. Each block implements all the switches in one row of the
 25 network 100B of FIG. 1B, one of the key aspects of the current invention. For example Block 1_2 implements the input switch IS1, output Switch OS1, middle switch MS(1,1), middle switch MS(7,1), middle switch MS(2,1), middle switch MS(6,1), middle switch MS(3,1), middle switch MS(5,1), and middle switch MS(4,1). For the simplification of illustration, Input switch IS1 and output switch OS1 together are denoted as switch 1;
 30 Middle switch MS(1,1) and middle switch MS(7,1) together are denoted by switch 2;

Middle switch MS(2,1) and middle switch MS(6,1) together are denoted by switch 3;
 Middle switch MS(3,1) and middle switch MS(5,1) together are denoted by switch 4;
 And middle switch MS(4,1) is denoted by switch 5.

5 All the straight middle links are illustrated in layout 400C1 of FIG. 4C1. For
 example in Block 1_2, inlet links IL1 – IL2, outlet links OL1 – OL2, middle link
 ML(1,1), middle link ML(1,2), middle link ML(8,1), middle link ML(8,2), middle link
 ML(2,1), middle link ML(2,2), middle link ML(7,1), middle link ML(7,2), middle link
 ML(3,1), middle link ML(3,2), middle link ML(6,1), middle link ML(6,2), middle link
 ML(4,1), middle link ML(4,2), middle link ML(5,1) and middle link ML(5,2) are
 10 illustrated in layout 400C1 of FIG. 4C1.

Even though it is not illustrated in layout 400C1 of FIG. 4C1, in each block, in
 addition to the switches there may be Configurable Logic Blocks (CLB) or any arbitrary
 digital circuit depending on the applications in different embodiments. The topology of
 the layout 400C1 in FIG. 4C1 is another embodiment of ring layout topology. For each of
 15 the neighboring rows in diagram 100B of FIG. 1B the corresponding blocks are also
 physically neighbors in layout diagram 400C of FIG. 4C. In addition the topmost row is
 also logically considered as neighbor to the bottommost row. For example Block 1_2
 (implementing the switches belonging to a row in diagram 100B of FIG. 1B) has Block
 3_4 as neighbor since Block 3_4 implements the switches in its neighboring row.
 20 Similarly Block 1_2 also has Block 31_32 as neighbor since Block 1_2 implements
 topmost row of switches and Block 31_32 implements bottommost row of switches in
 diagram 100B of FIG. 1B. The ring layout scheme illustrated in 400C of FIG. 4C can be
 generalized for a large multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ where $N_1 = N_2 > 32$,
 in accordance with the current invention.

25 All the layout embodiments disclosed in the current invention are applicable to
 generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage
 networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$,
 generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-
 link multi-stage networks $V_{fold-link}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree

networks $V_{mlink-bft}(N_1, N_2, d, s)$, and generalized hypercube networks $V_{hcube}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general, and for both $N_1 = N_2 = N$ and $N_1 \neq N_2$, and d is any integer.

- Conversely applicant makes another important observation that generalized
- 5 hypercube networks $V_{hcube}(N_1, N_2, d, s)$ are implemented with the layout topology being the hypercube topology shown in layout 100C of FIG. 1C with large scale cross point reduction as any one of the networks described in the current invention namely:
- generalized multi-stage networks $V(N_1, N_2, d, s)$, generalized folded multi-stage networks $V_{fold}(N_1, N_2, d, s)$, generalized butterfly fat tree networks $V_{bft}(N_1, N_2, d, s)$,
- 10 generalized multi-link multi-stage networks $V_{mlink}(N_1, N_2, d, s)$, generalized folded multi-link multi-stage networks $V_{fold-mlink}(N_1, N_2, d, s)$, generalized multi-link butterfly fat tree networks $V_{mlink-bft}(N_1, N_2, d, s)$ for $s = 1, 2, 3$ or any number in general, and for both $N_1 = N_2 = N$ and $N_1 \neq N_2$, and d is any integer.

- Numerous modifications and adaptations of the embodiments, implementations,
- 15 and examples described herein will be apparent to the skilled artisan in view of the disclosure.

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS		
First Named Inventor/Applicant Name:		Venkat Konda		
Filer:		Venkar Konda		
Attorney Docket Number:		M-0045US		
Filed as Small Entity				
Provisional Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Provisional Application filing fee	2005	1	100	100
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				100

Electronic Acknowledgement Receipt

EFS ID:	1814731
Application Number:	60940394
International Application Number:	
Confirmation Number:	7100
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkar Konda
Filer Authorized By:	
Attorney Docket Number:	M-0045US
Receipt Date:	25-MAY-2007
Filing Date:	
Time Stamp:	23:34:37
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment was successfully received in RAM	\$ 100
RAM confirmation Number	2887
Deposit Account	

File Listing:

Document Number	Document Description	File Name	File Size(Bytes)	Multi Part /.zip	Pages (if appl.)
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1	Specification	M-0045US-PPA.pdf	218198	no	47
Warnings:					
Information:					
2	Drawings	M-0045US-FIGs.pdf	567002	no	38
Warnings:					
Information:					
3	Fee Worksheet (PTO-06)	fee-info.pdf	8123	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			793323		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					

FIG. 1A

100A

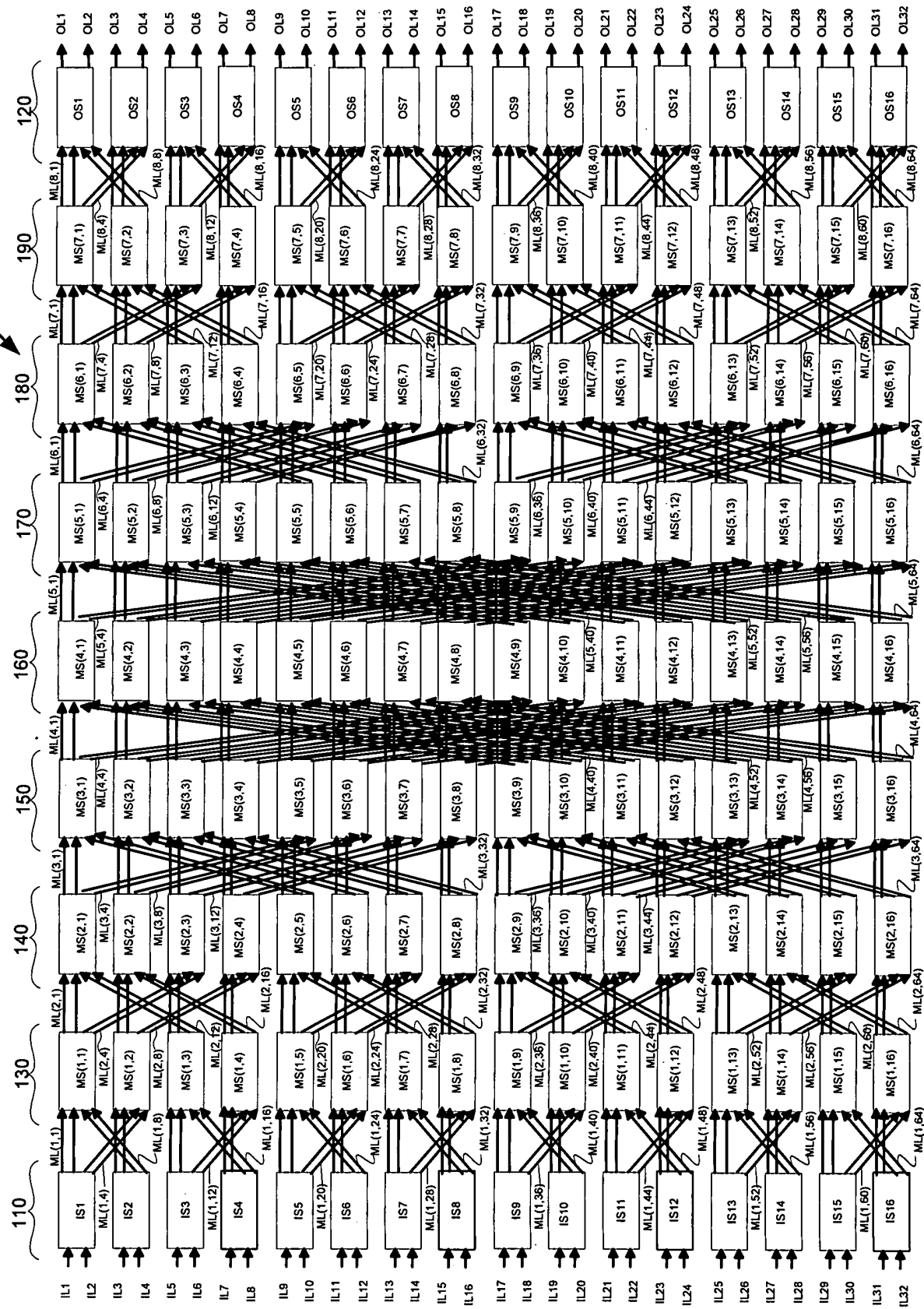


FIG. 1B

100B

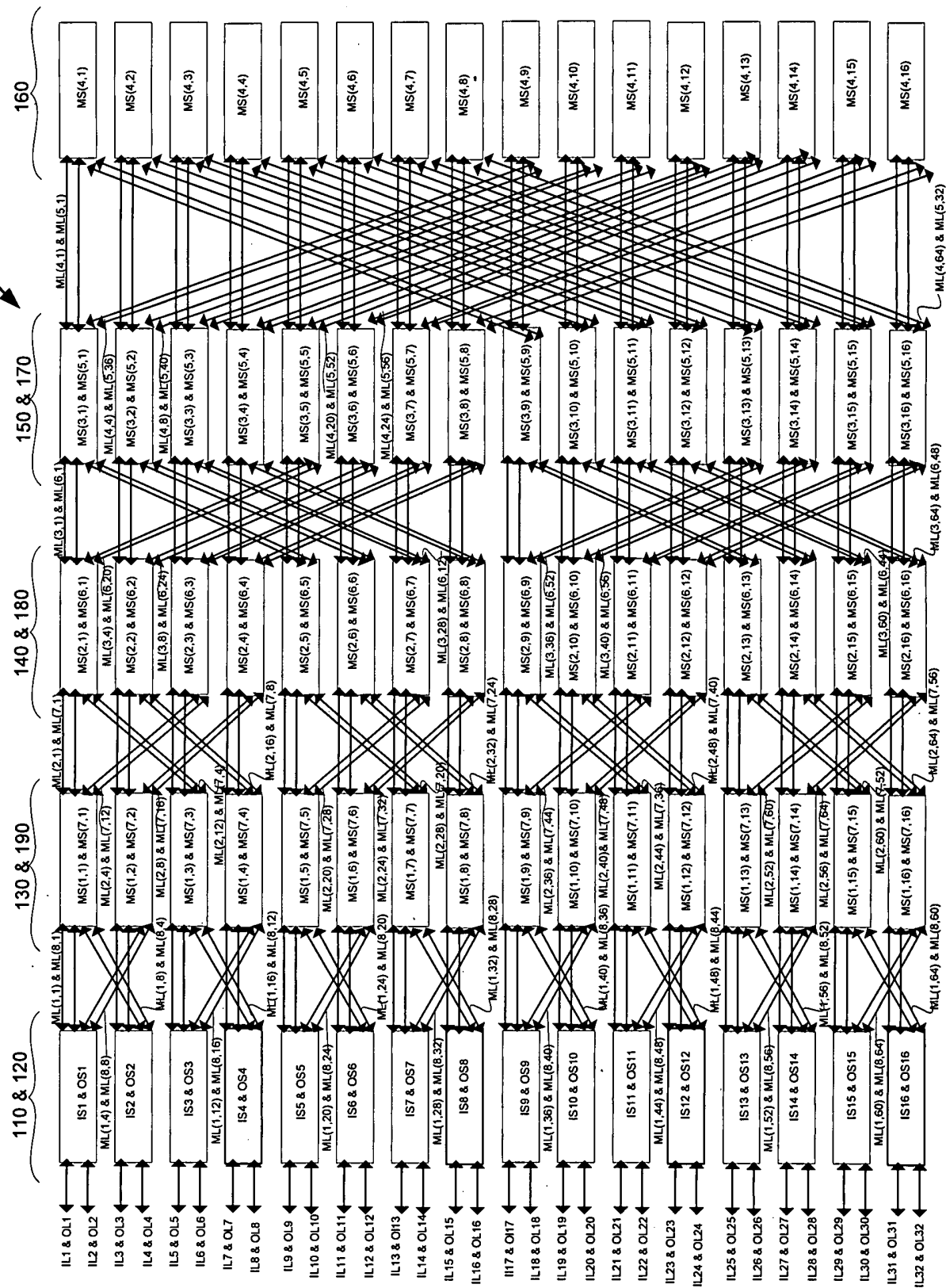


FIG. 1C

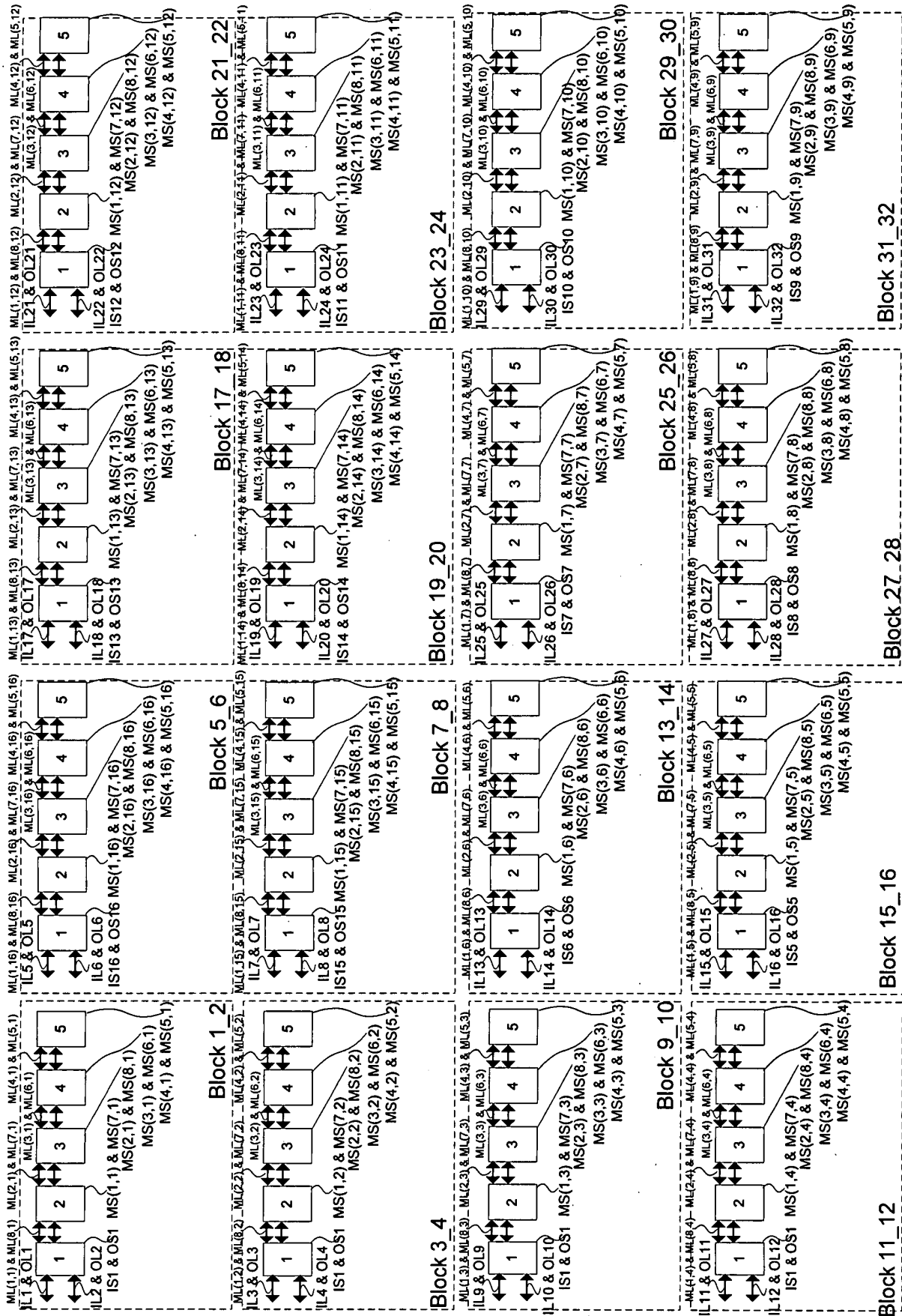


FIG. 1D

100D

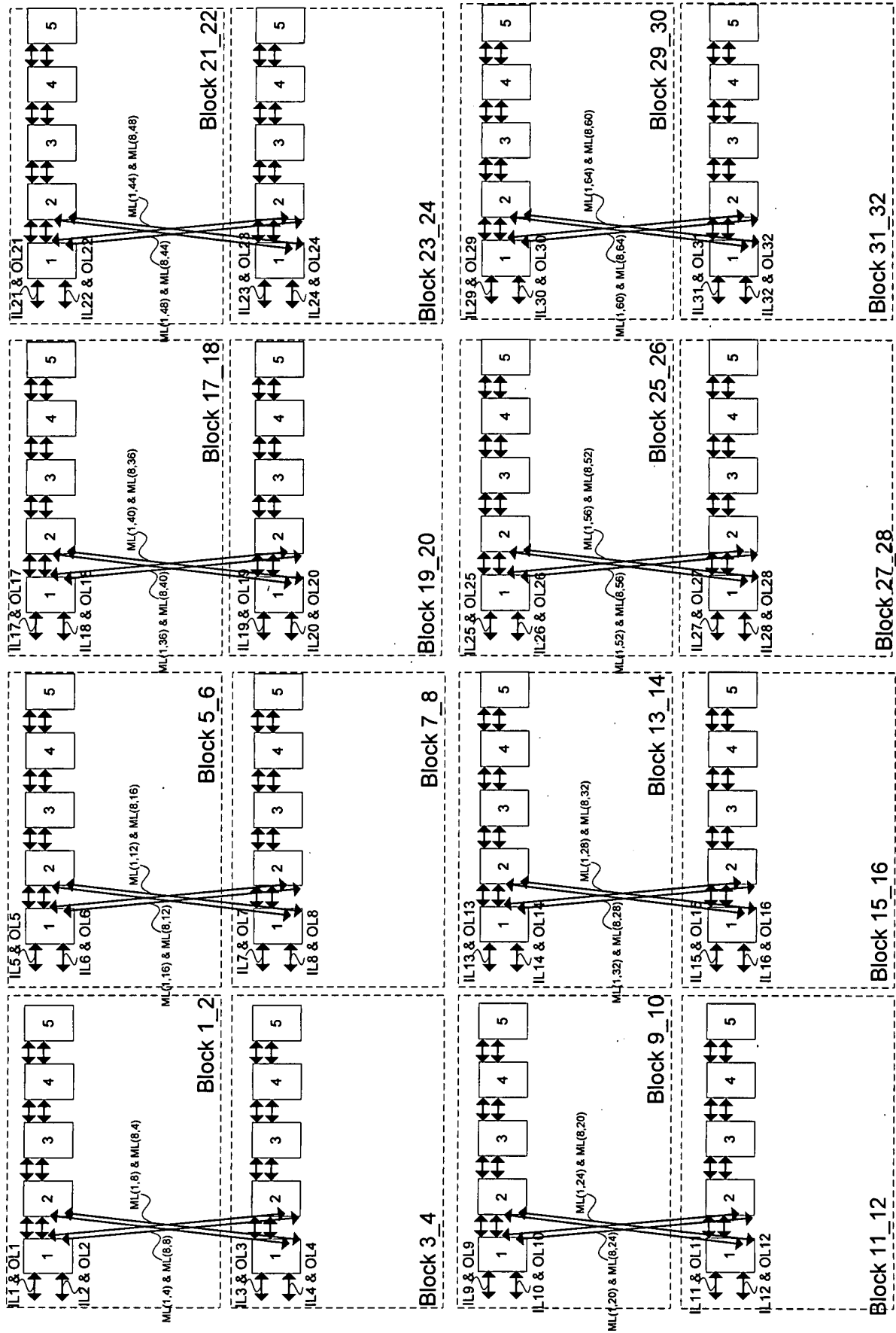


FIG. 1E

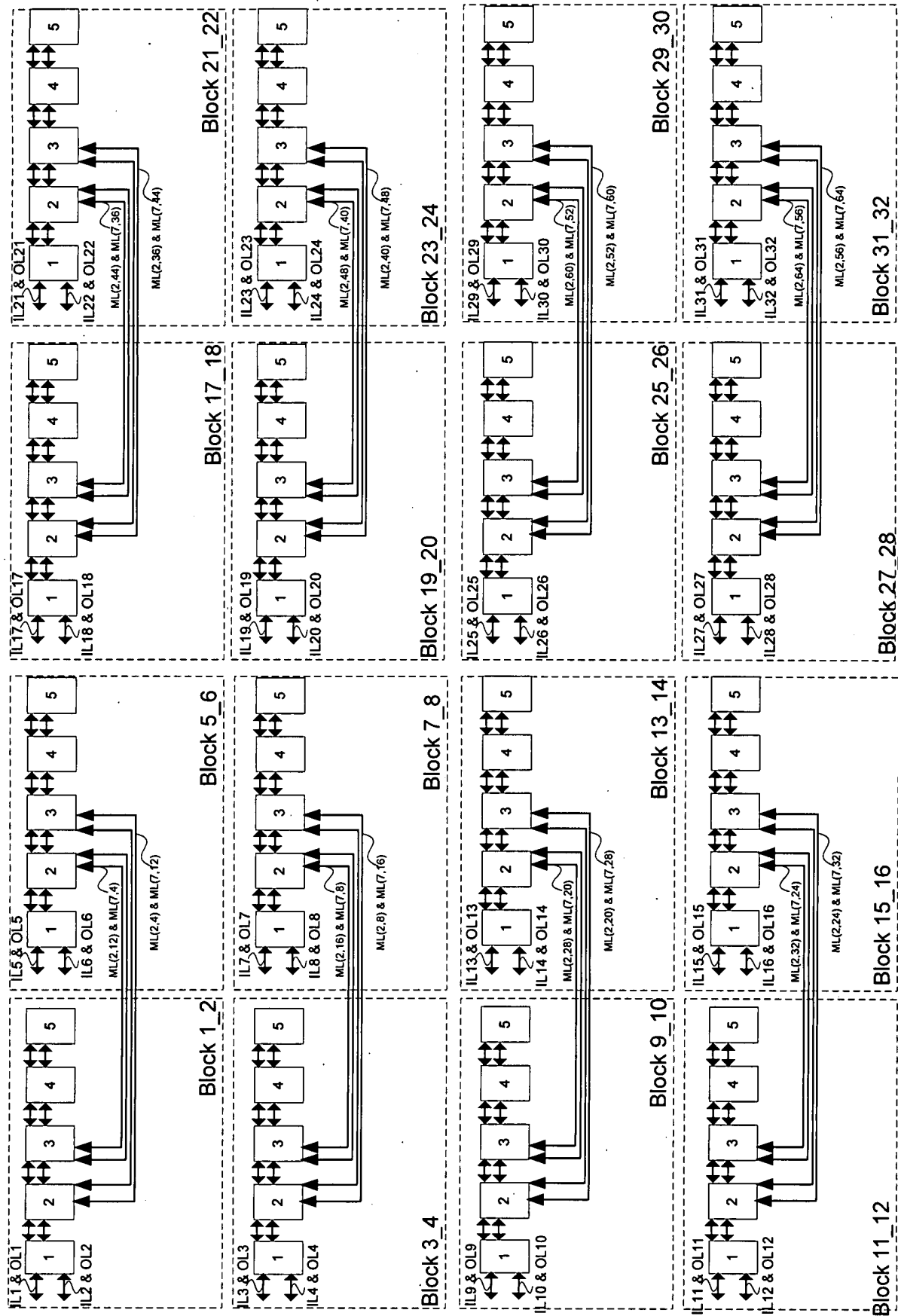


FIG. 1F

100F

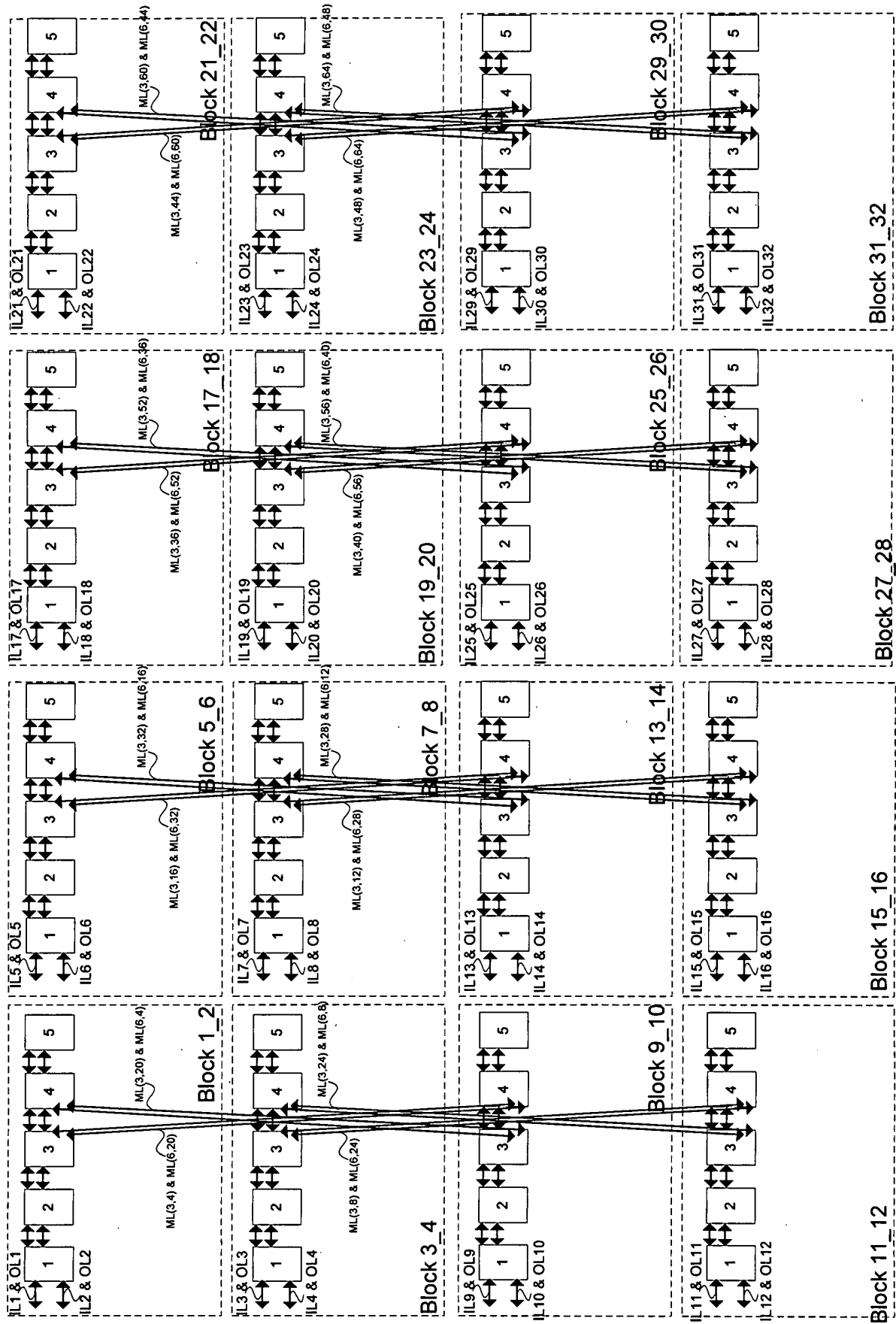


FIG. 1G

100G

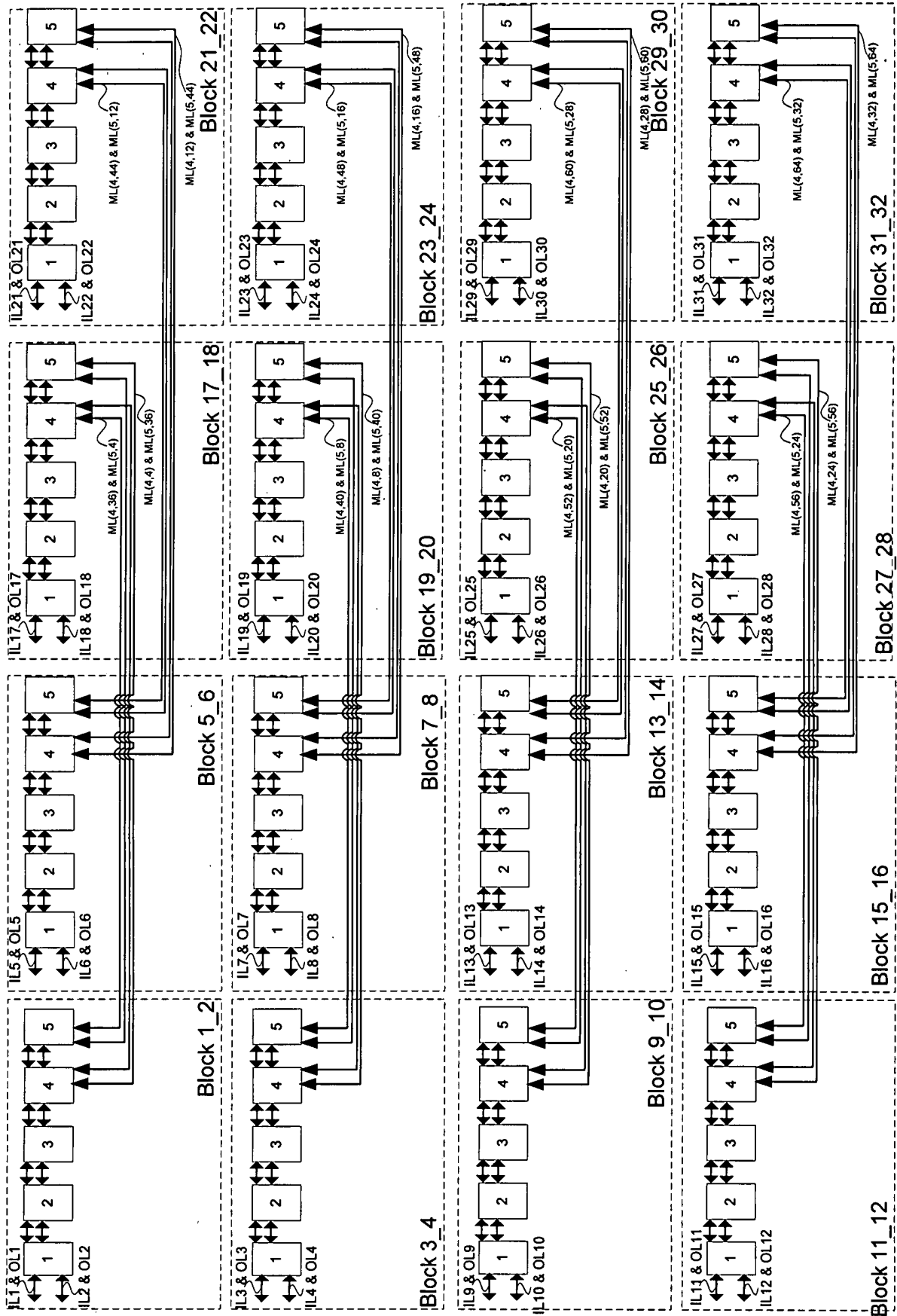
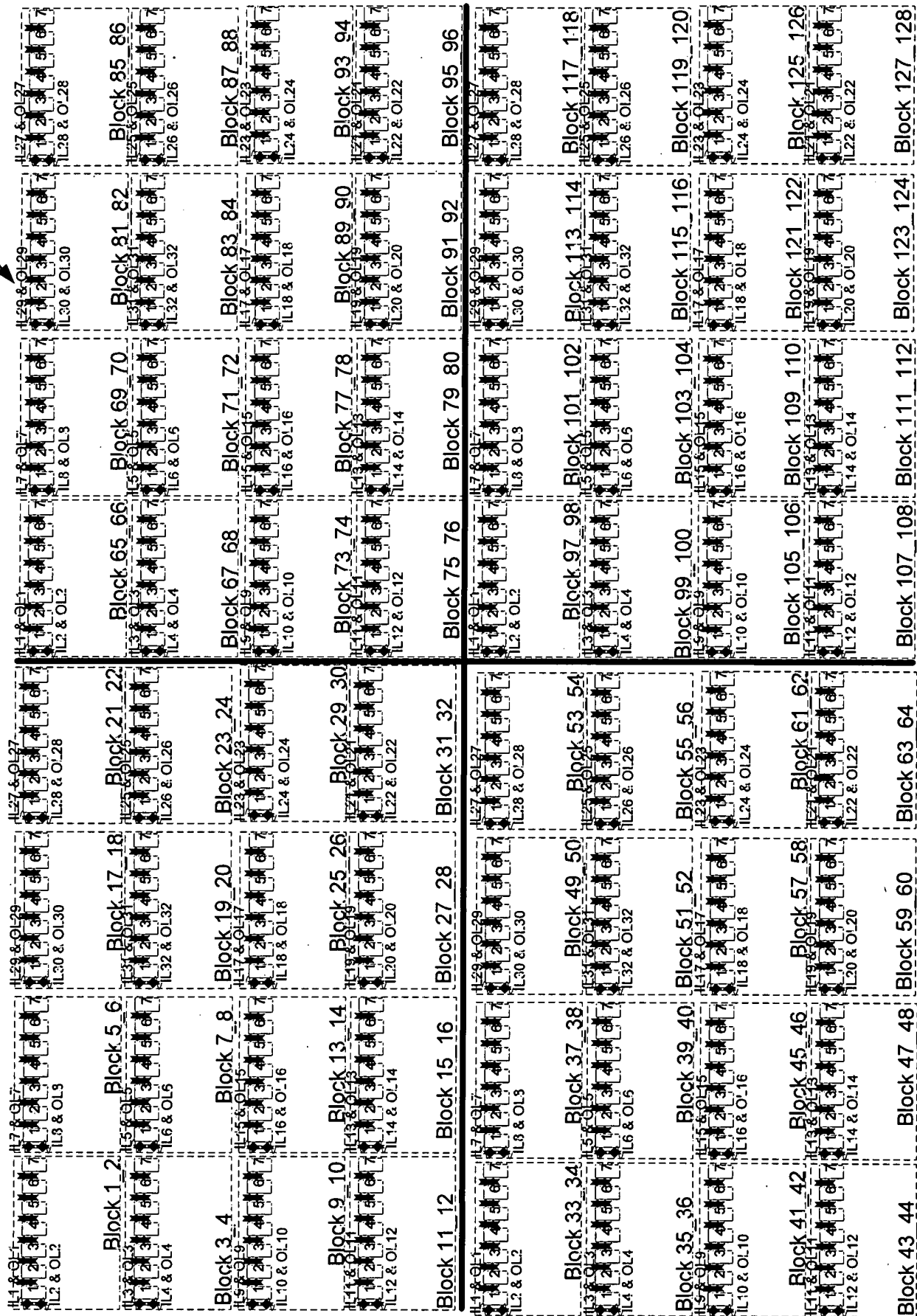


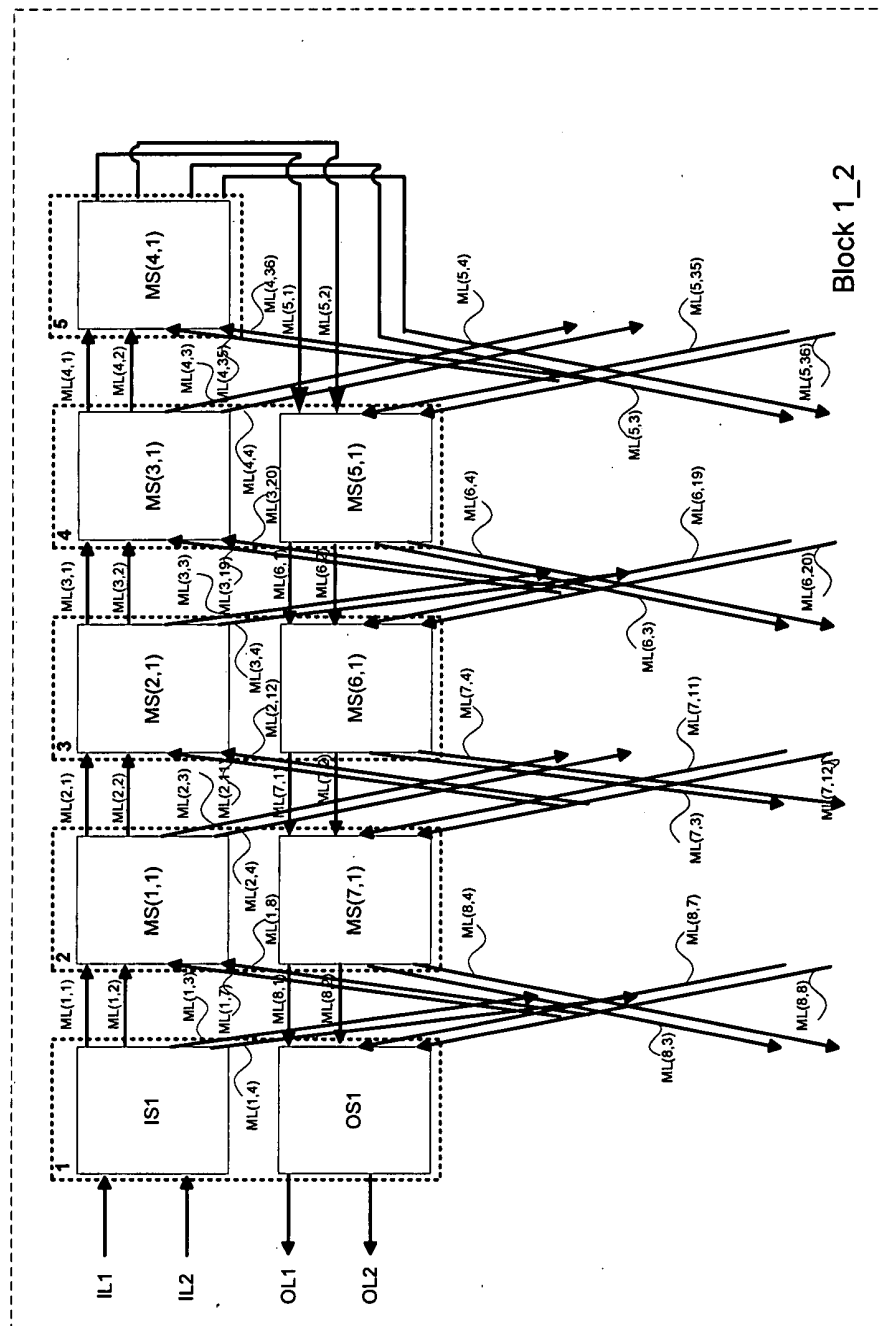
FIG. 1H

100H



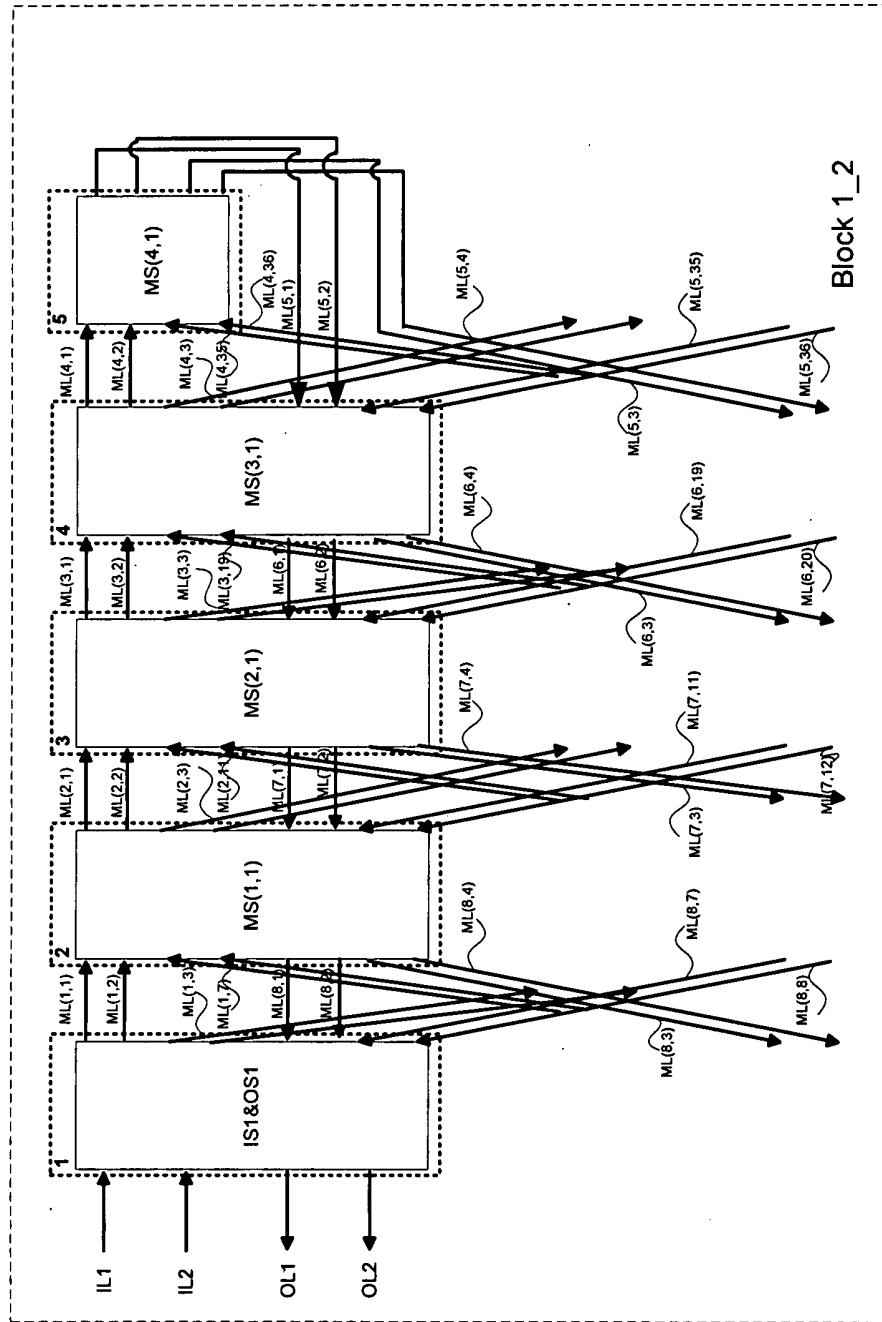
100I

FIG. 1I



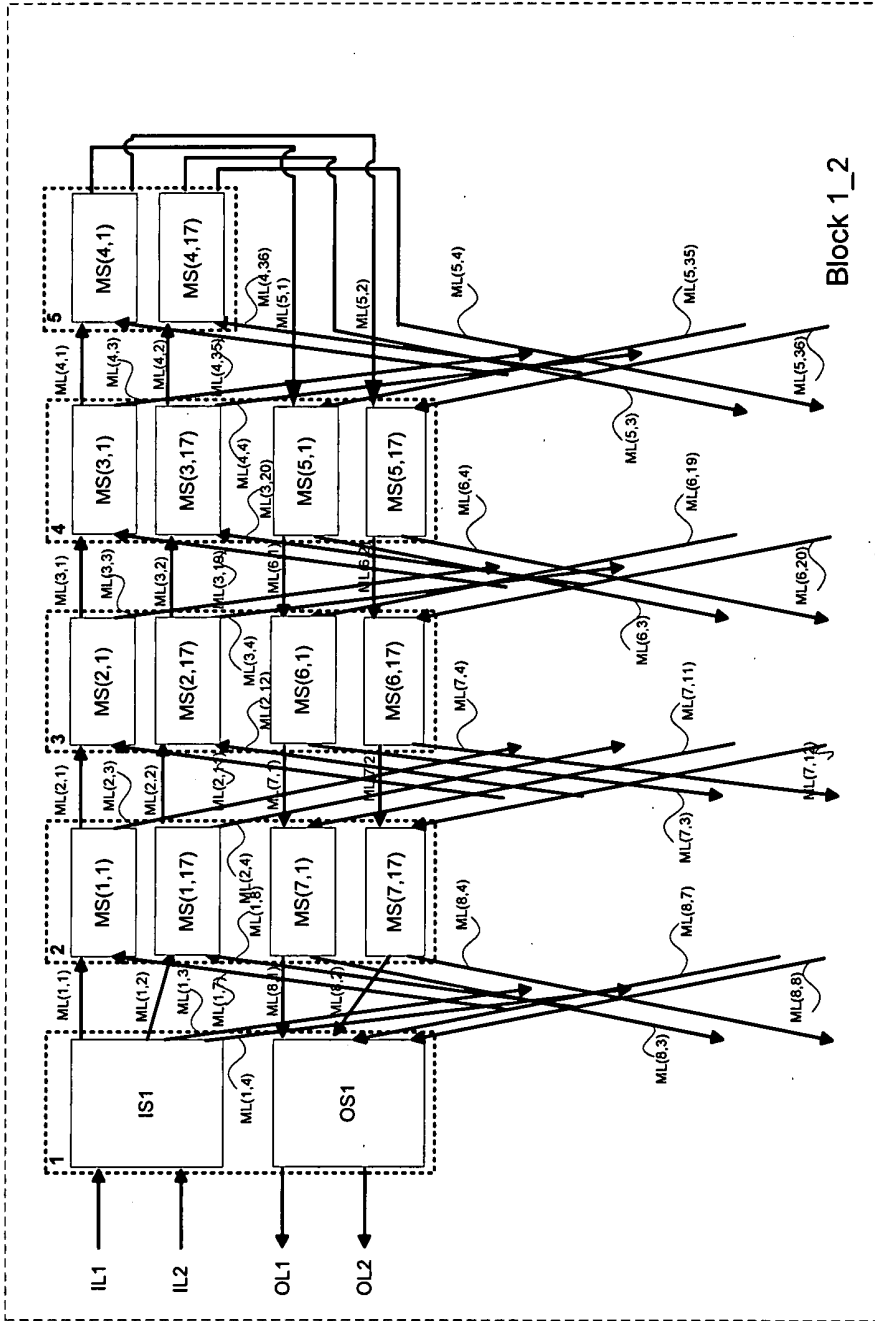
100J

FIG. 1J



100K

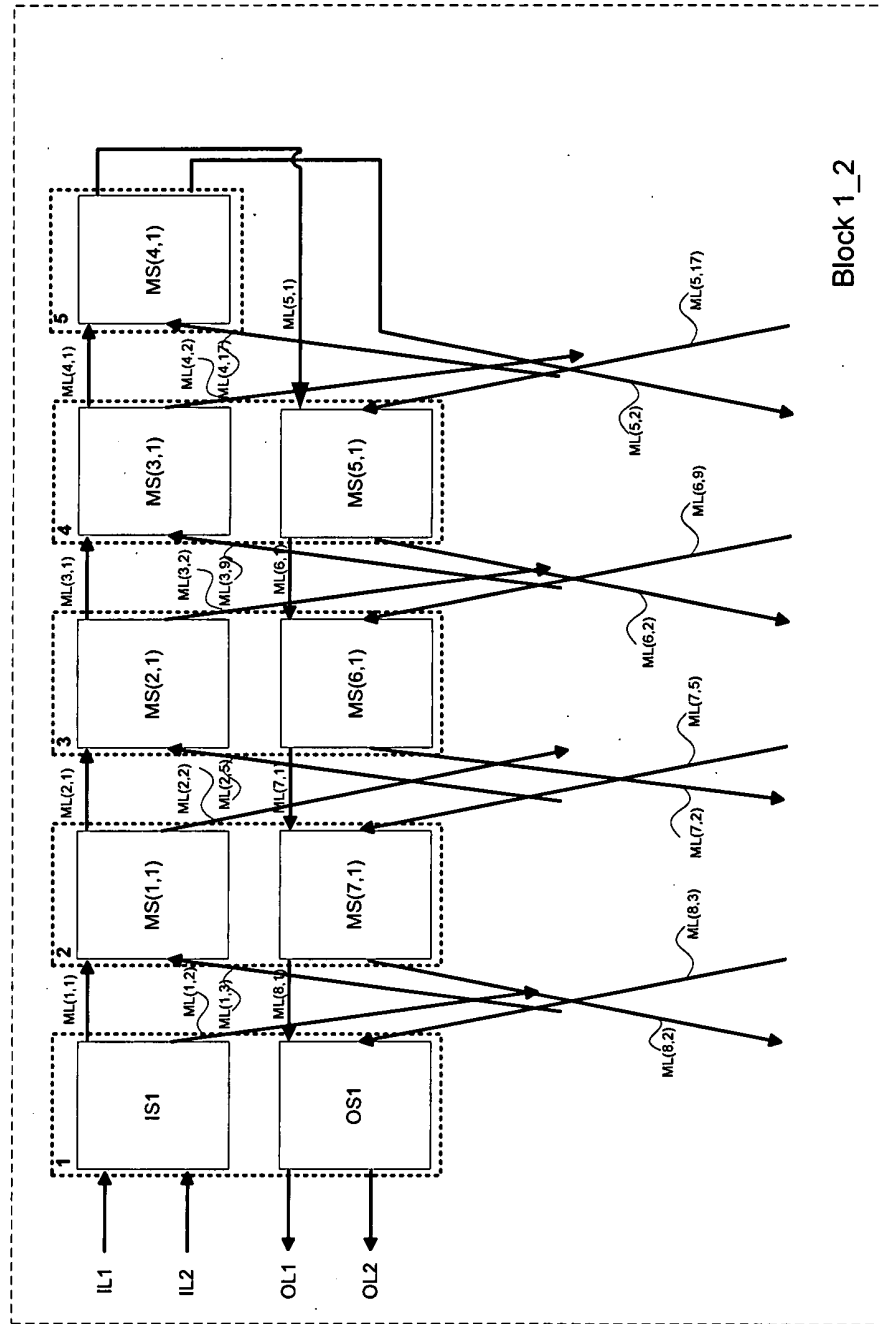
FIG. 1K



Block 1_2

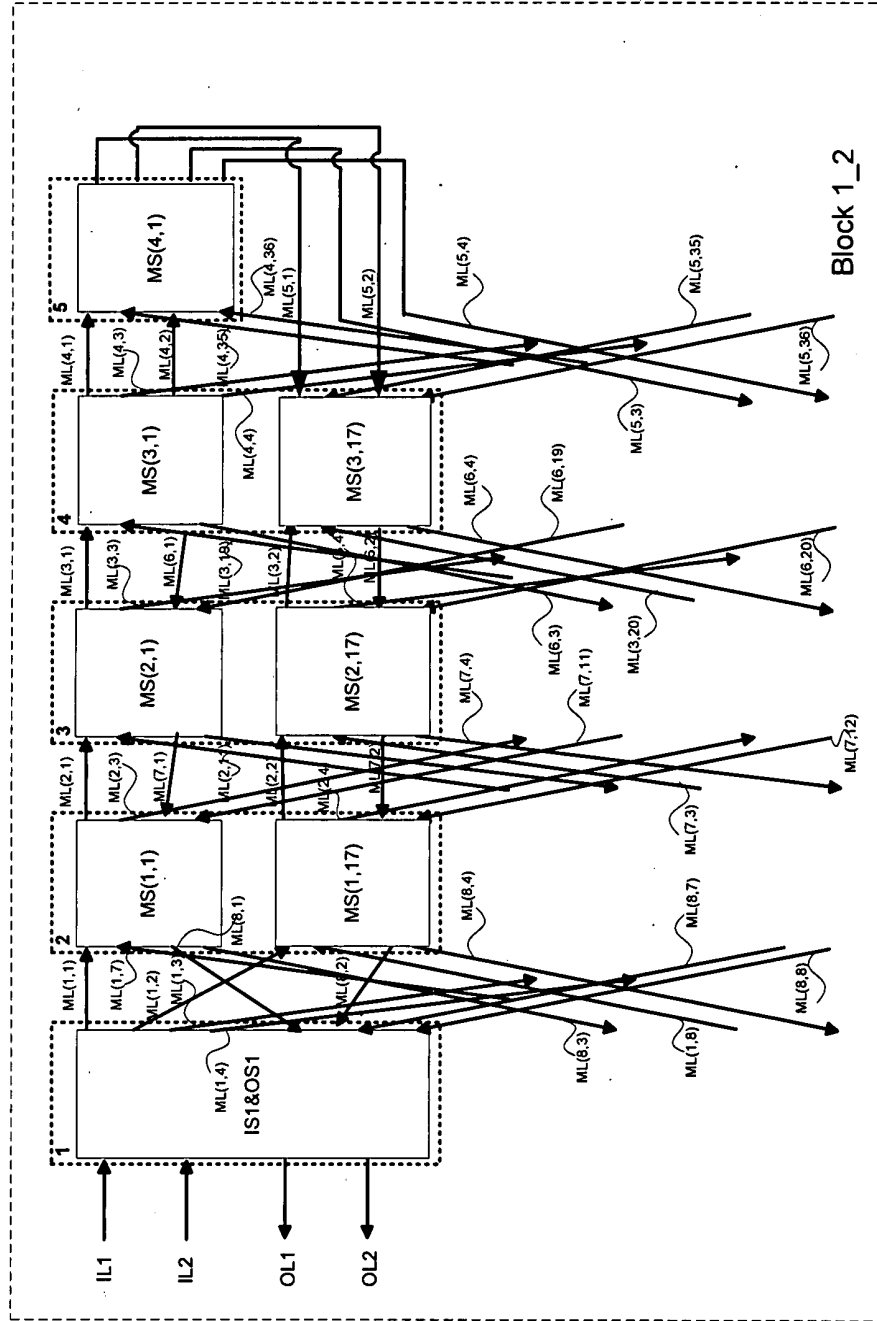
100K1

FIG. 1K1



100L

FIG. 1L



100L1

FIG. 1L1

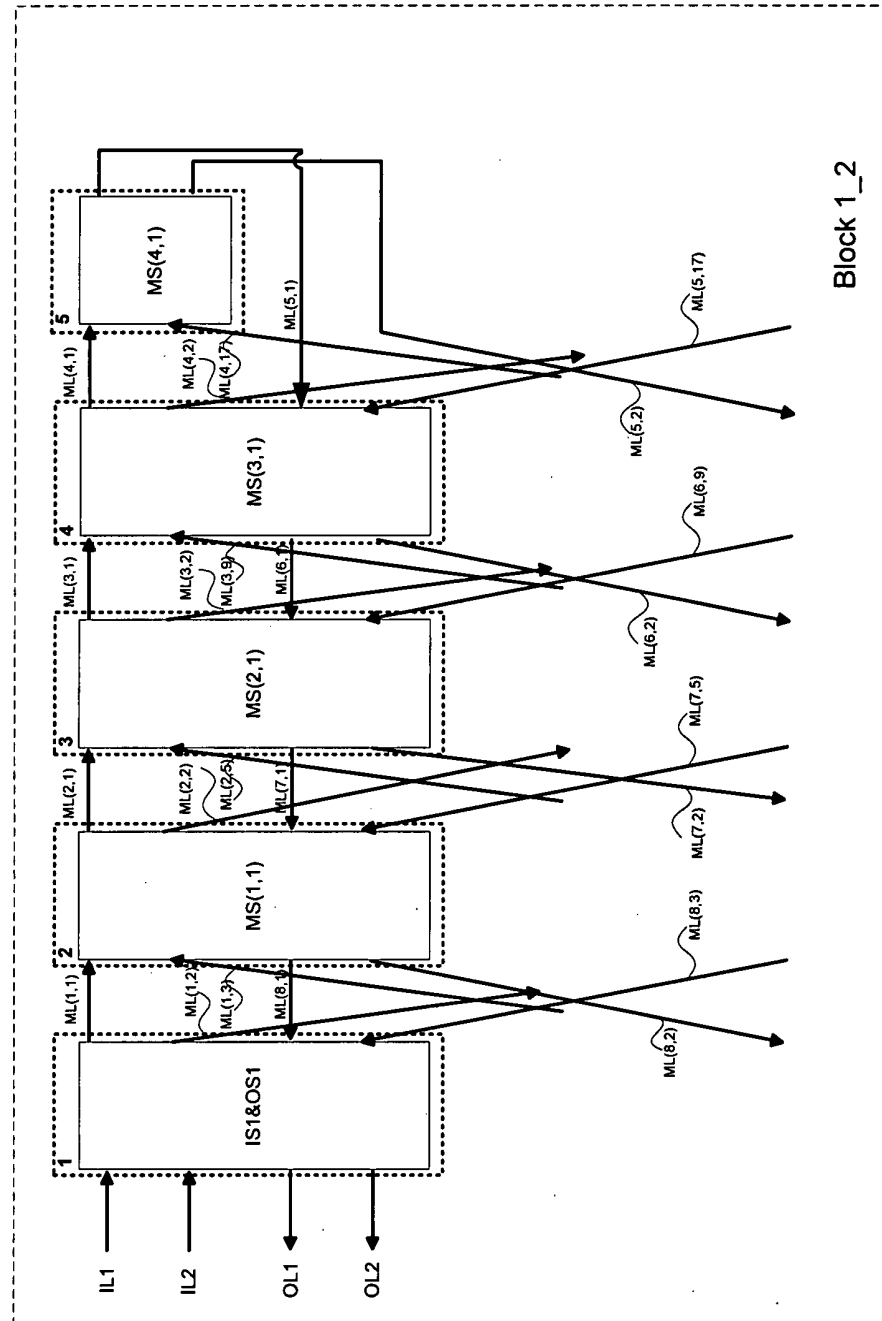


FIG. 2A1

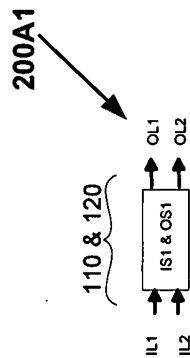


FIG. 2A2

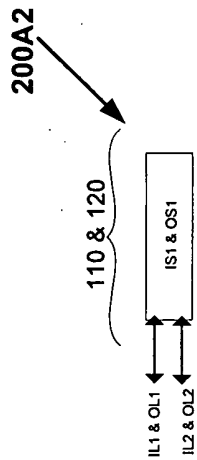


FIG. 2A3

200A3

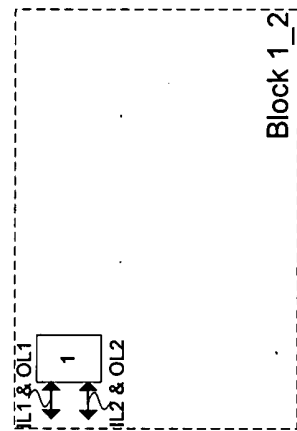


FIG. 2B1

200B1

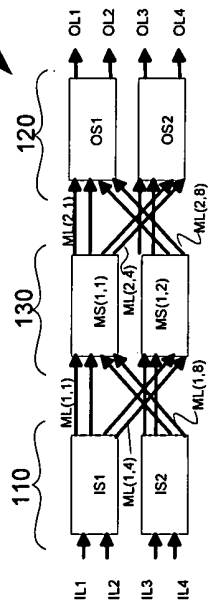


FIG. 2B2

200B2

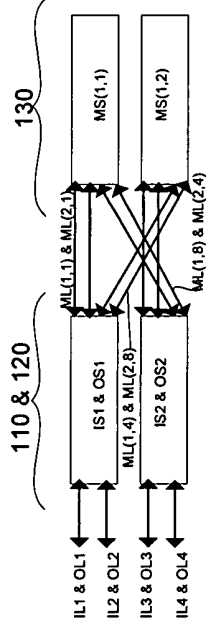


FIG. 2B3

200B3

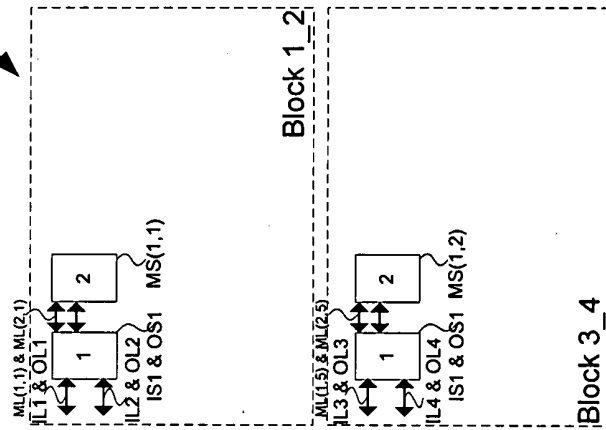
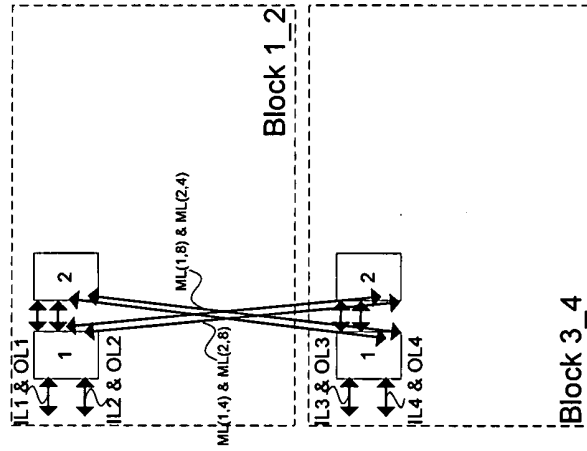


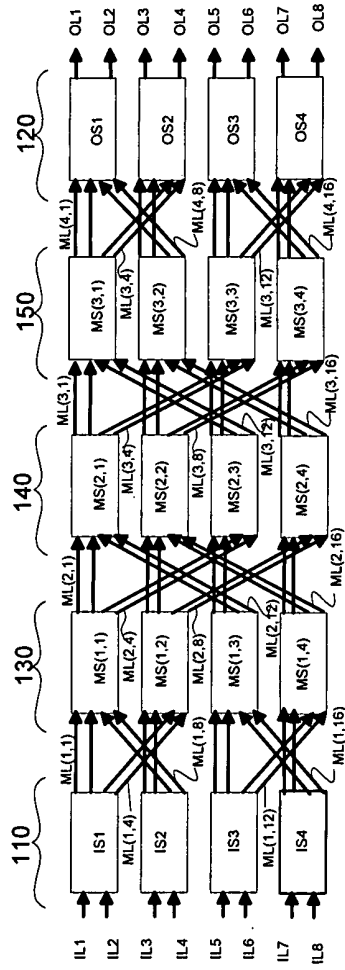
FIG. 2B4

200B4



200C11

FIG. 2C11



200C12

FIG. 2C12

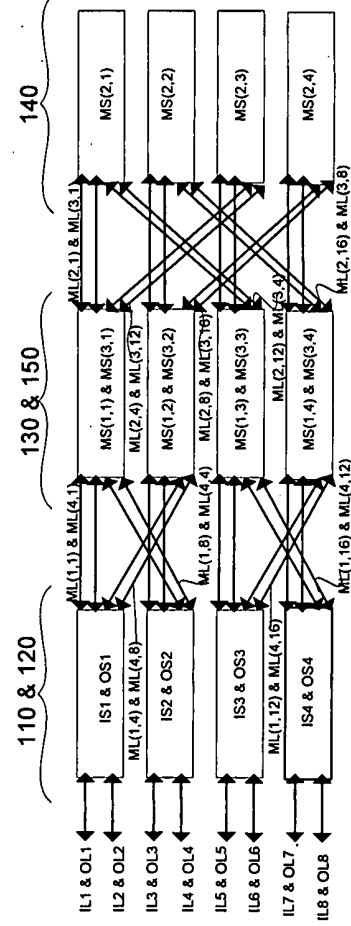


FIG. 2C21

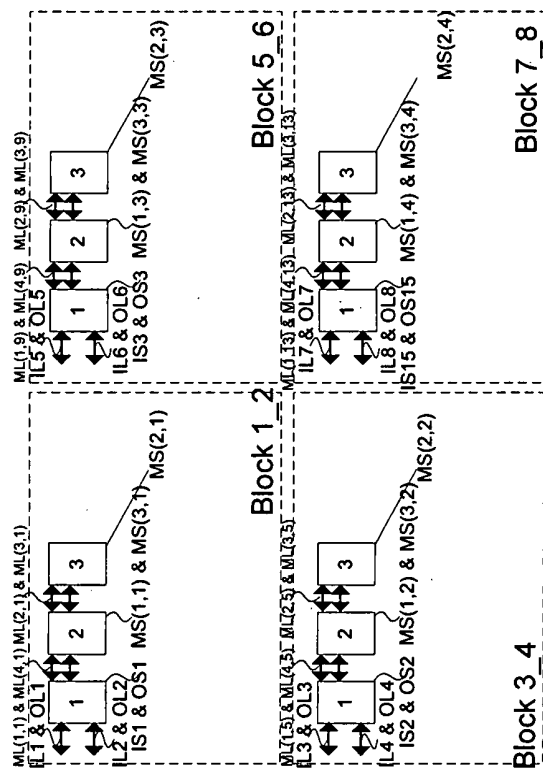


FIG. 2C22

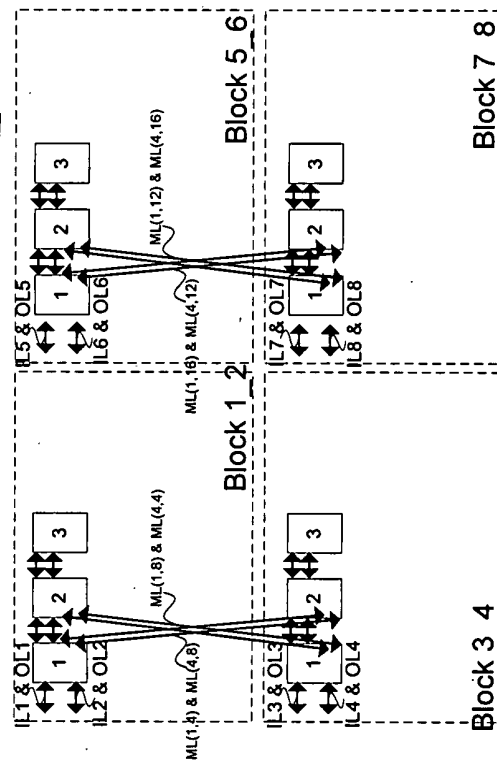


FIG. 2C23

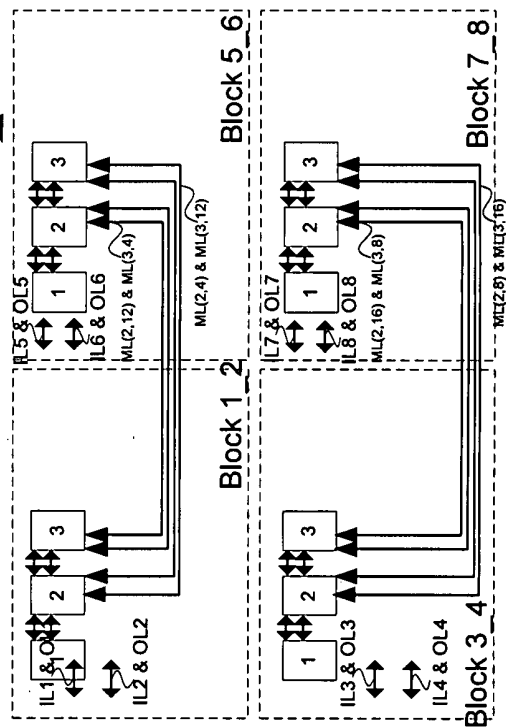


FIG. 2D1

200D1

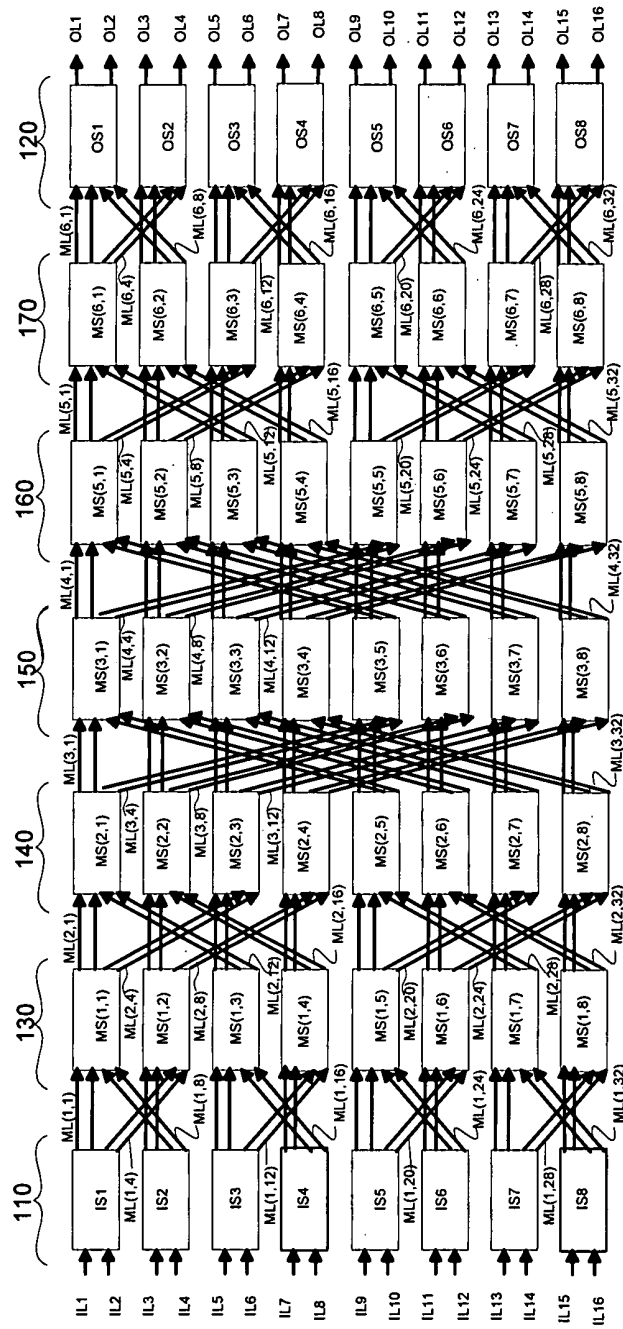


FIG. 2D2

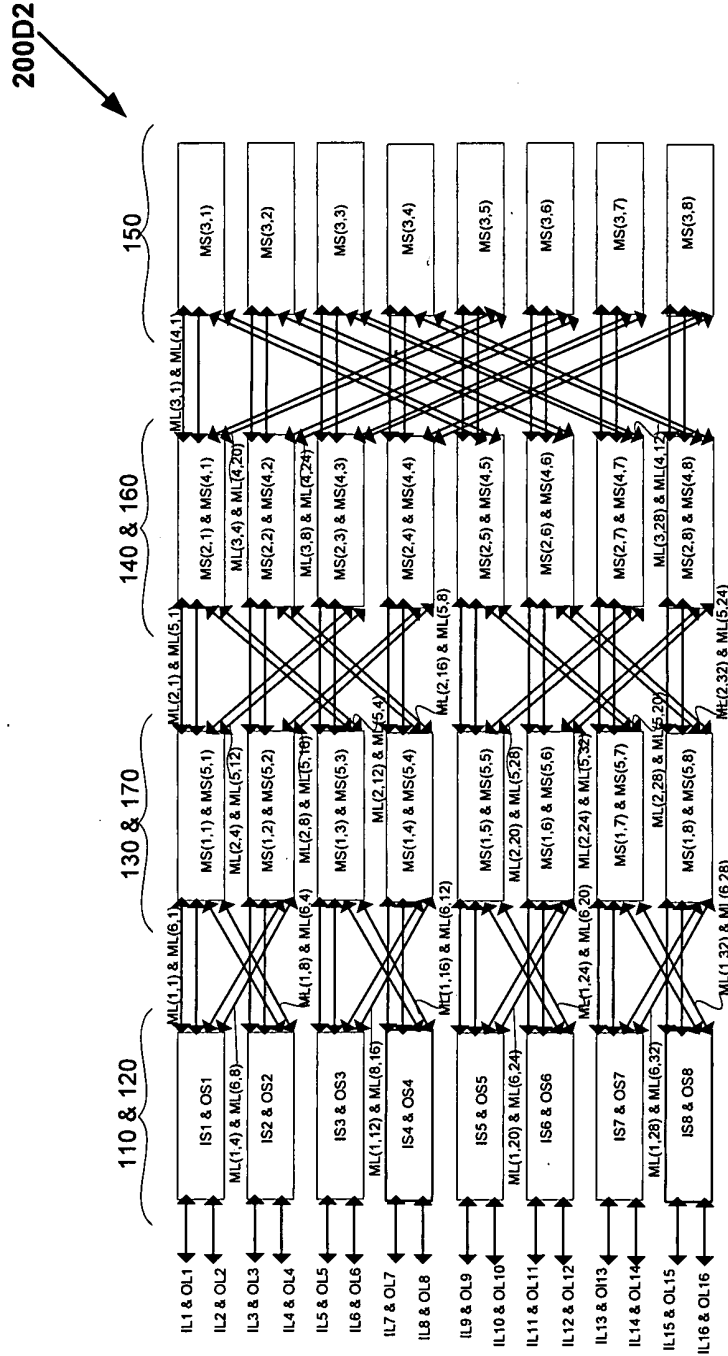
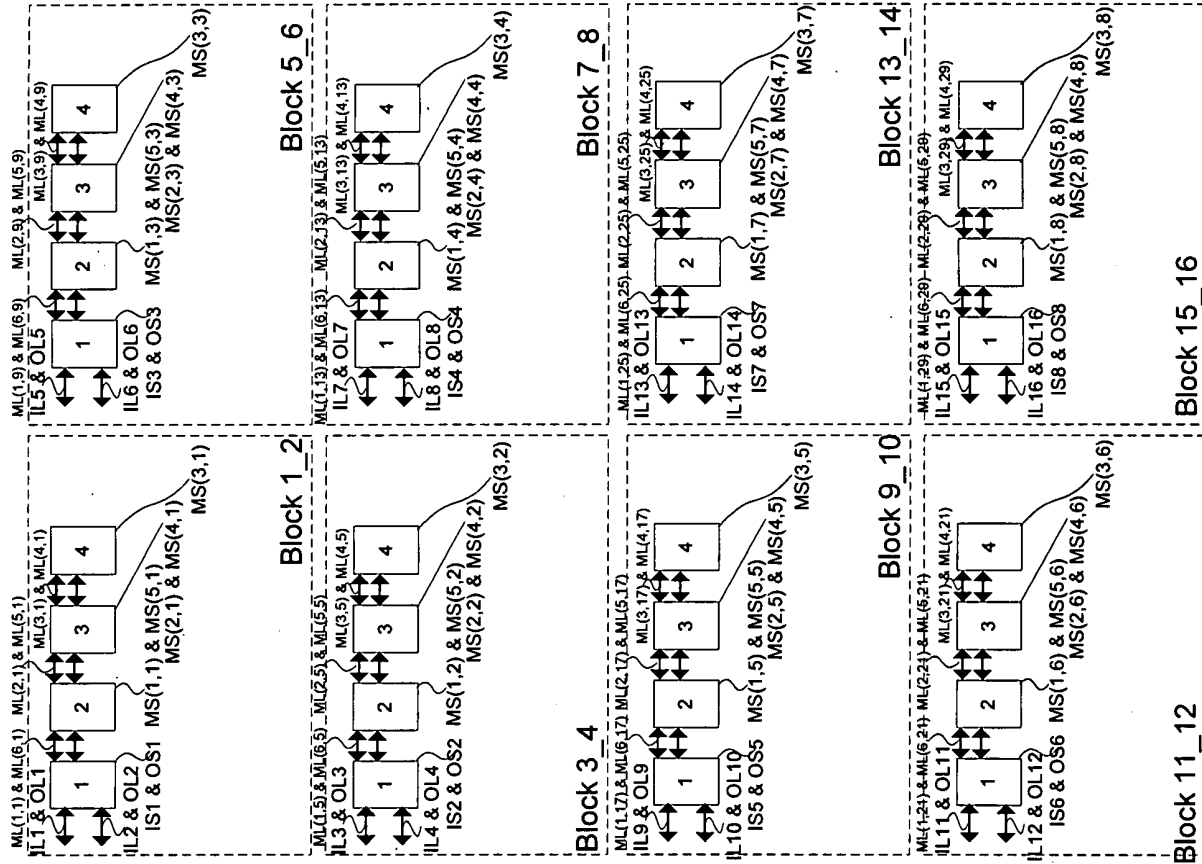
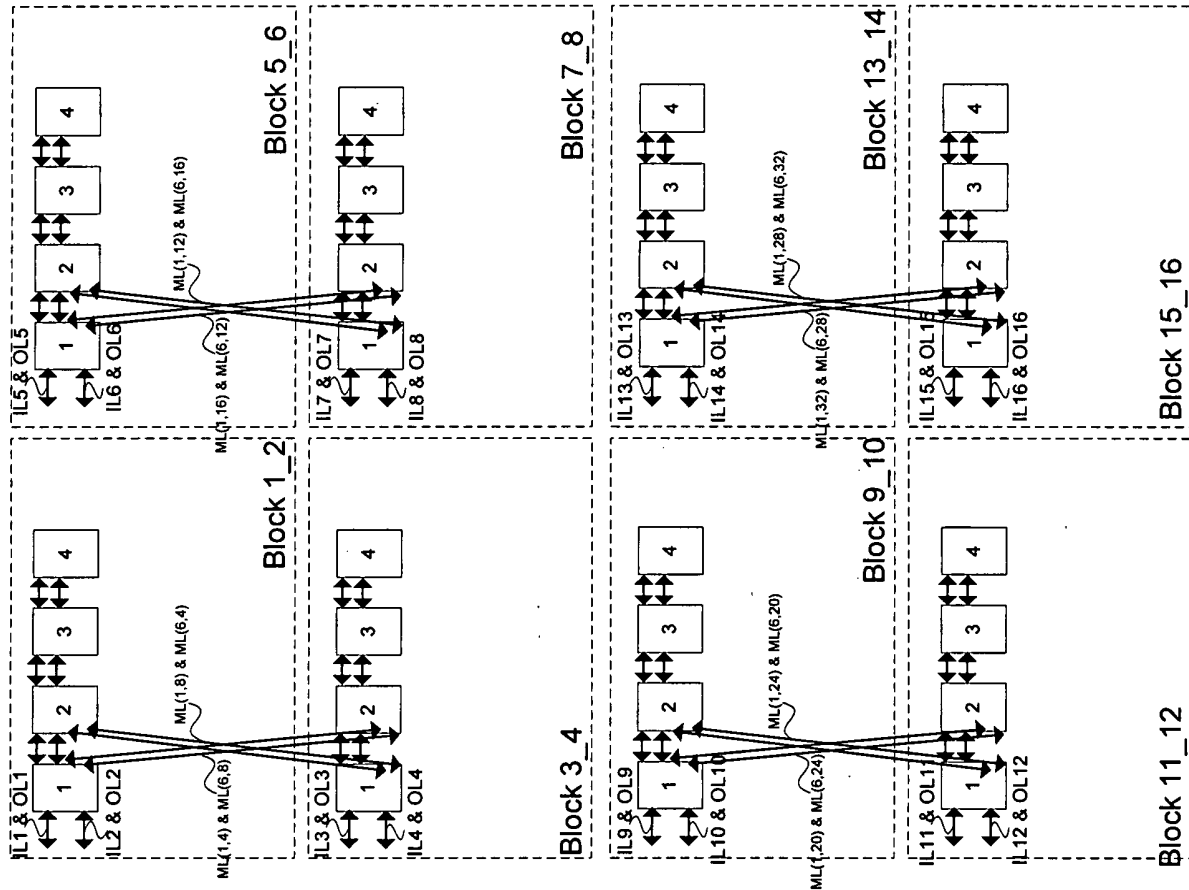


FIG. 2D3



200D3

FIG. 2D4



200D4

200D5

FIG. 2D5

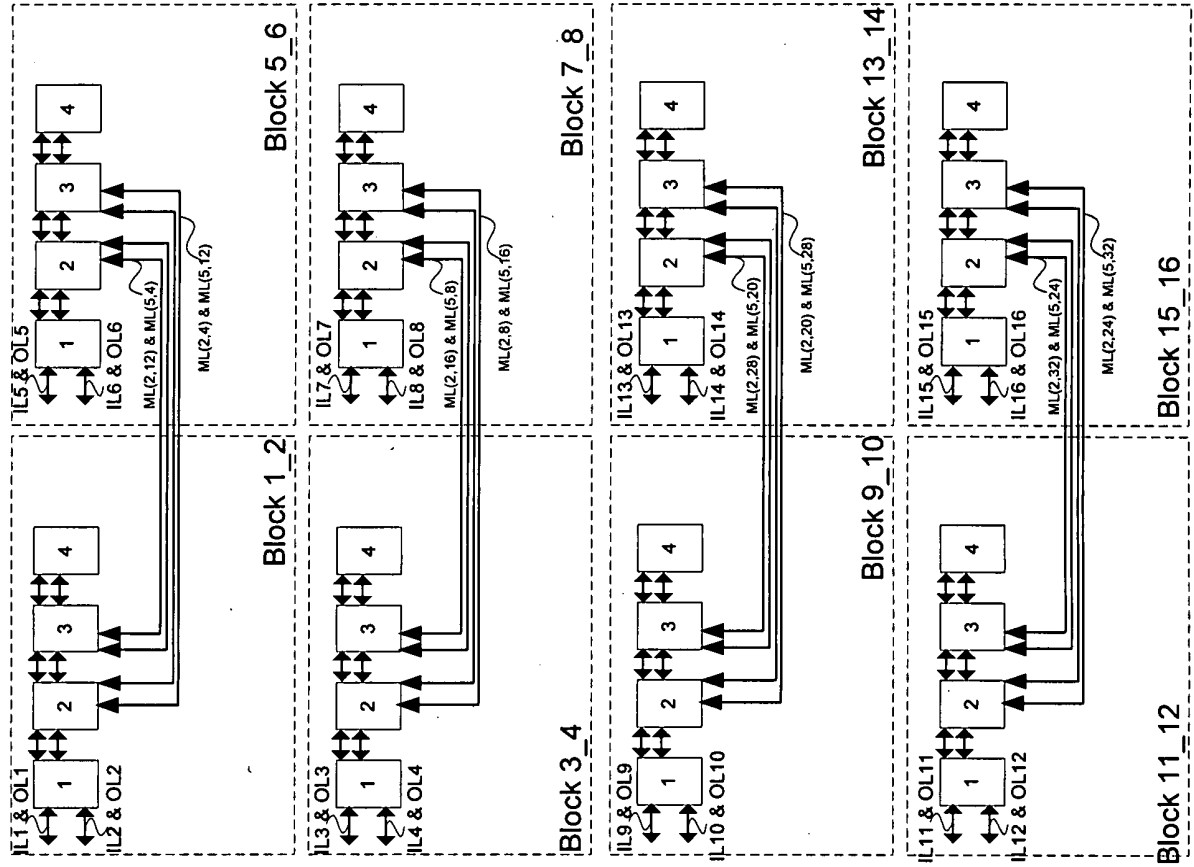
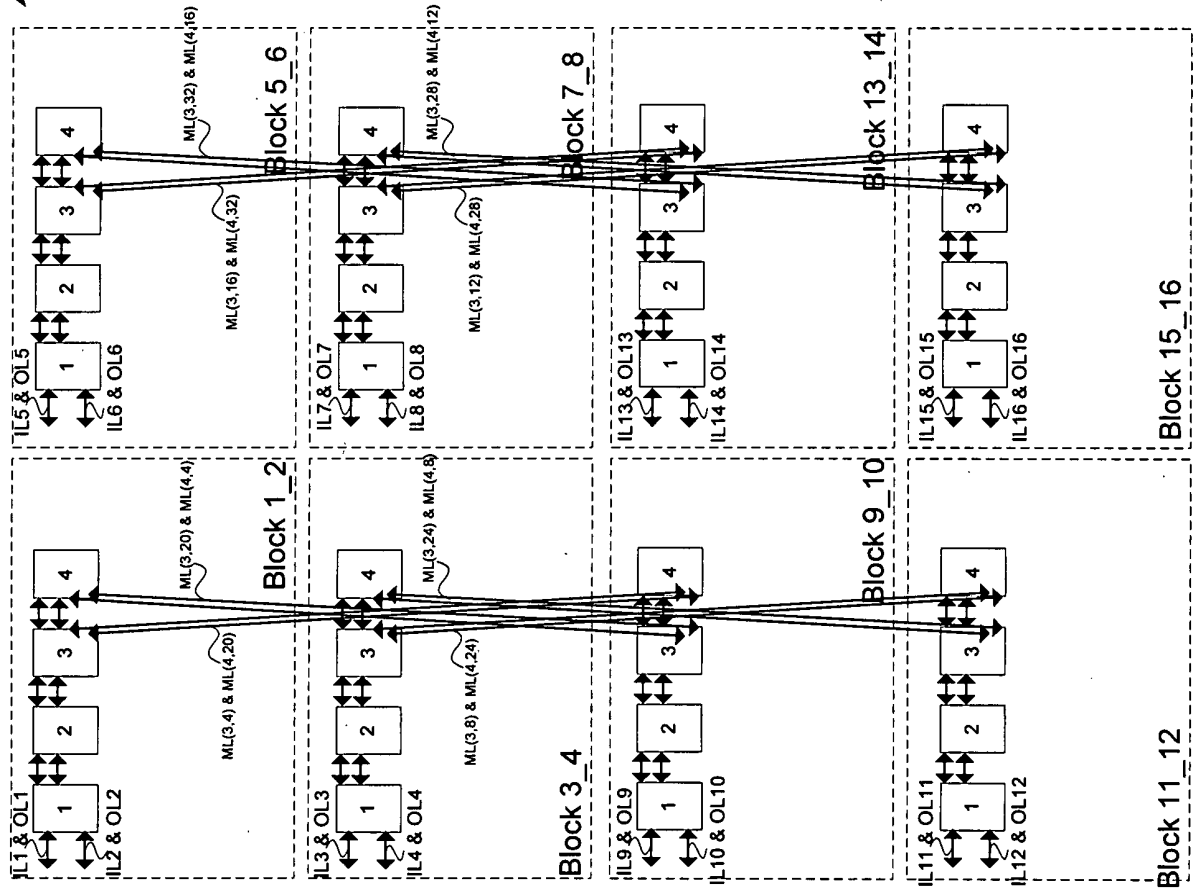


FIG. 2D6

200D6



300A

FIG. 3A

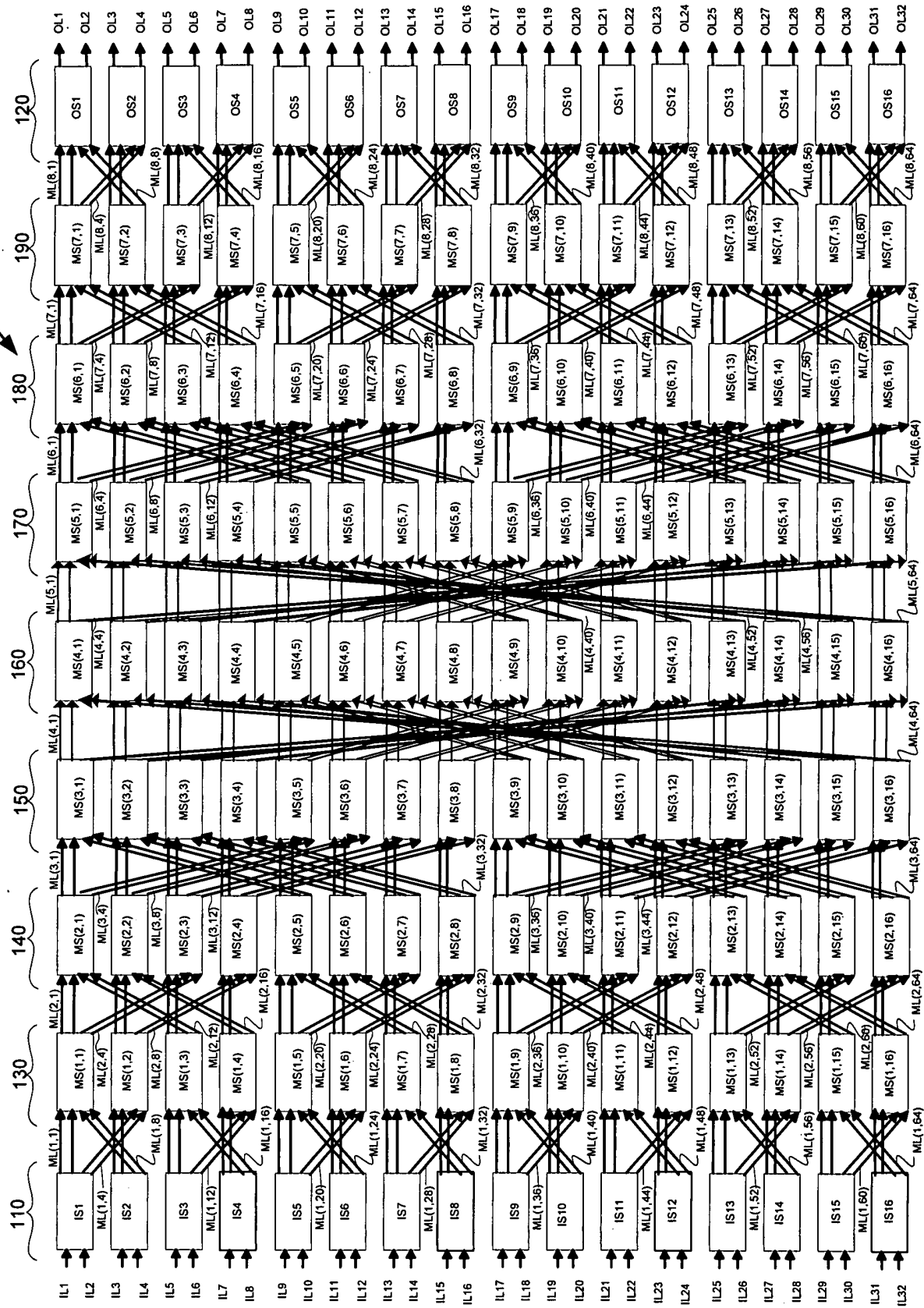


FIG. 3B

300B

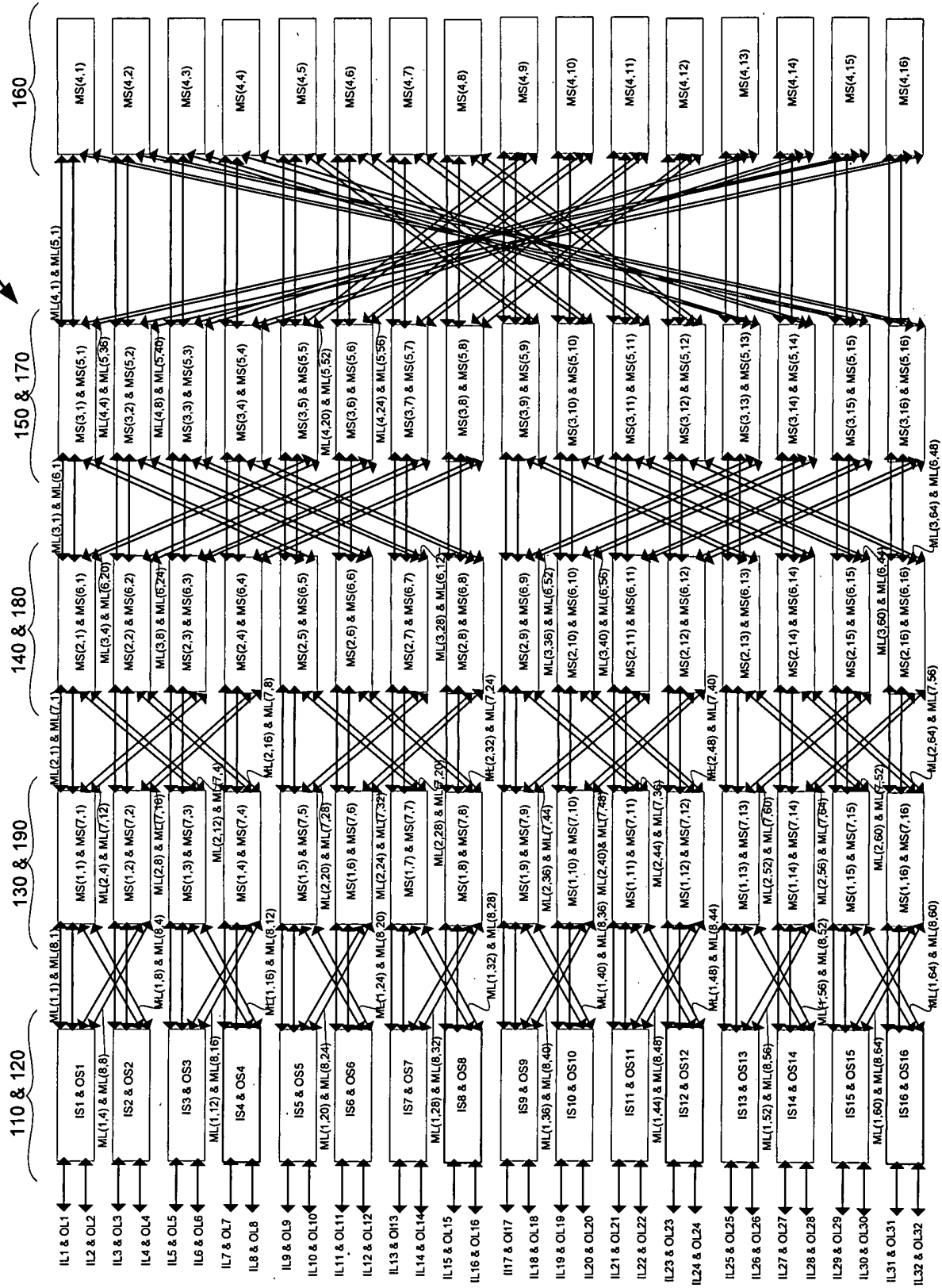


FIG. 3C

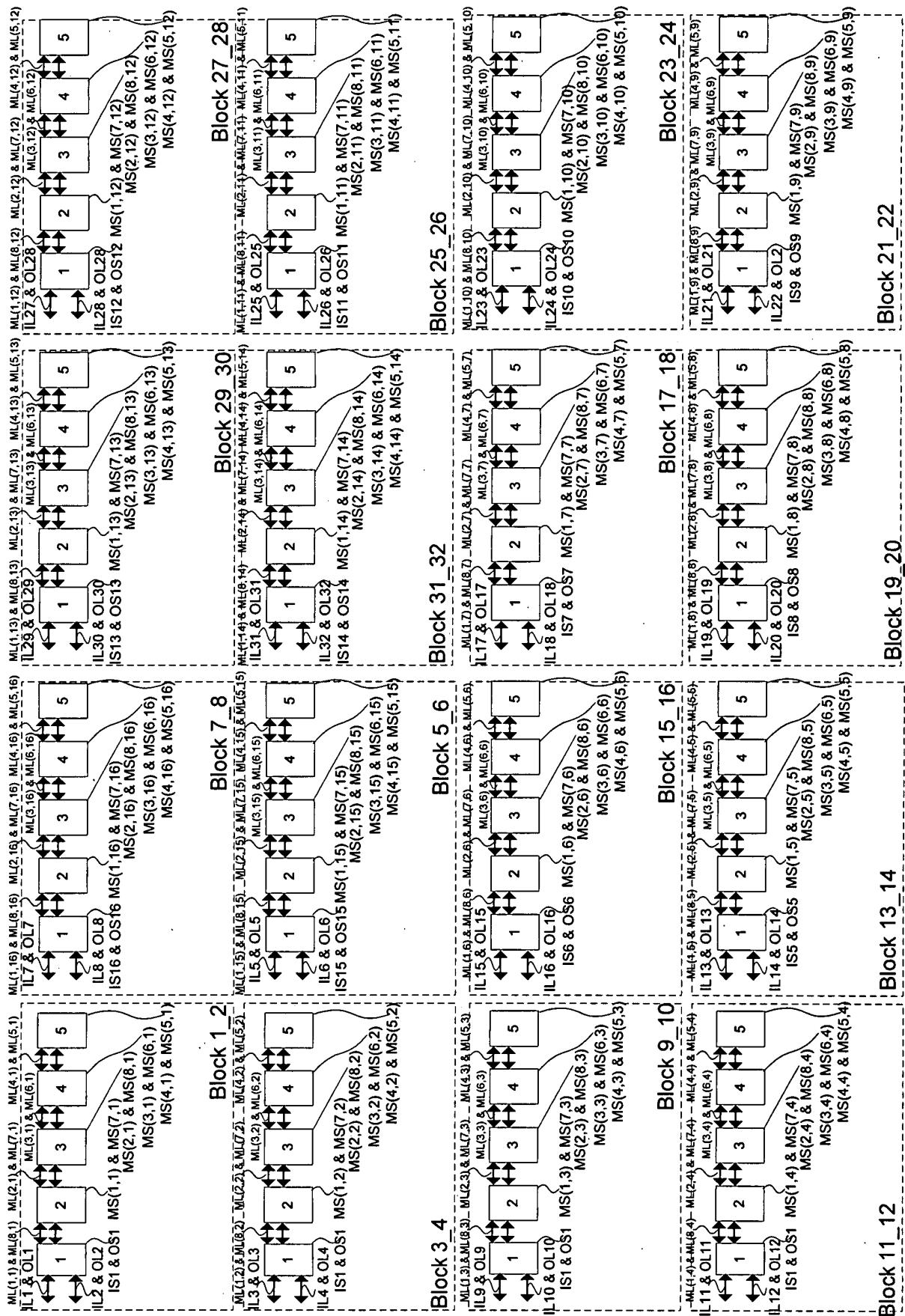


FIG. 3D

300D

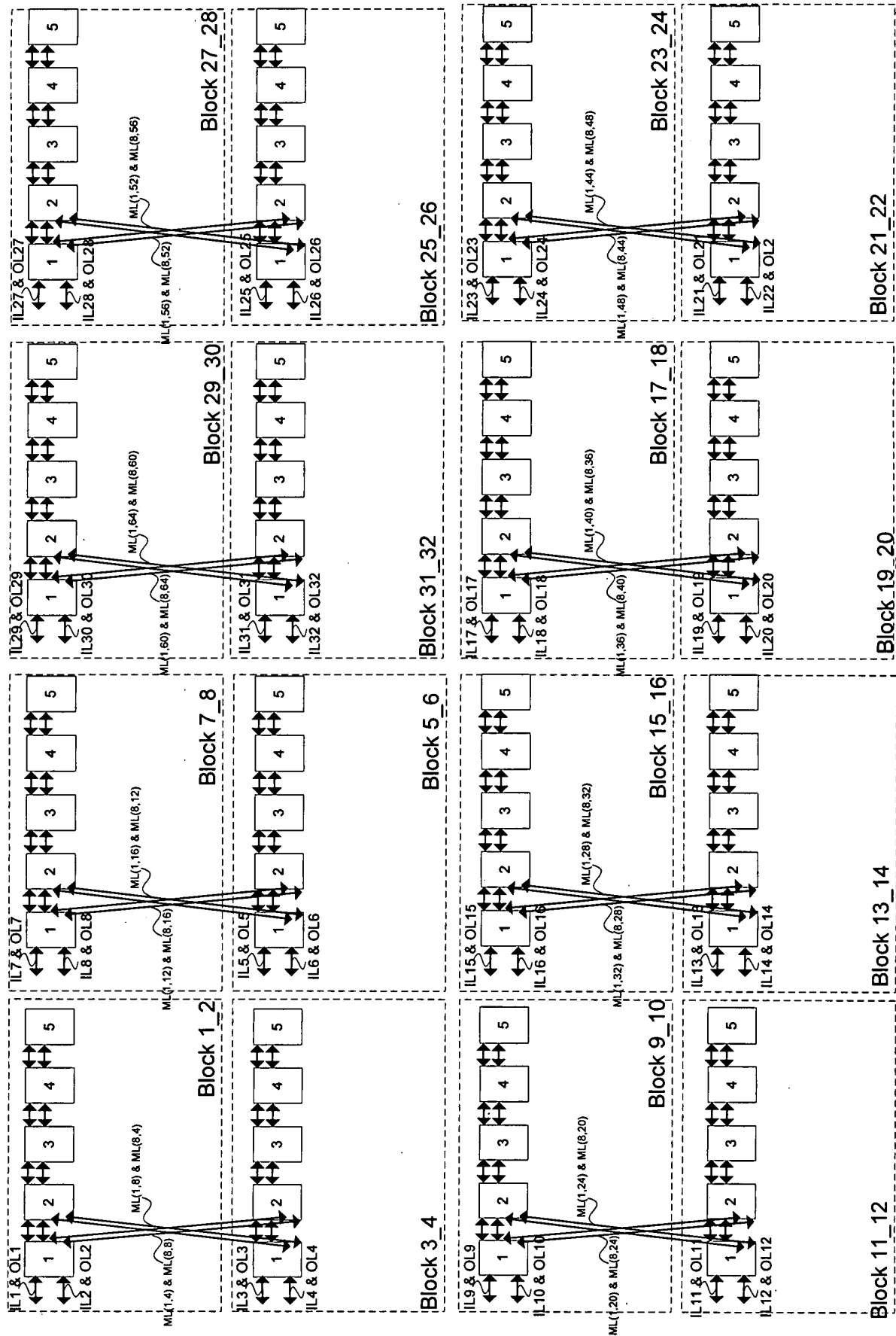


FIG. 3E

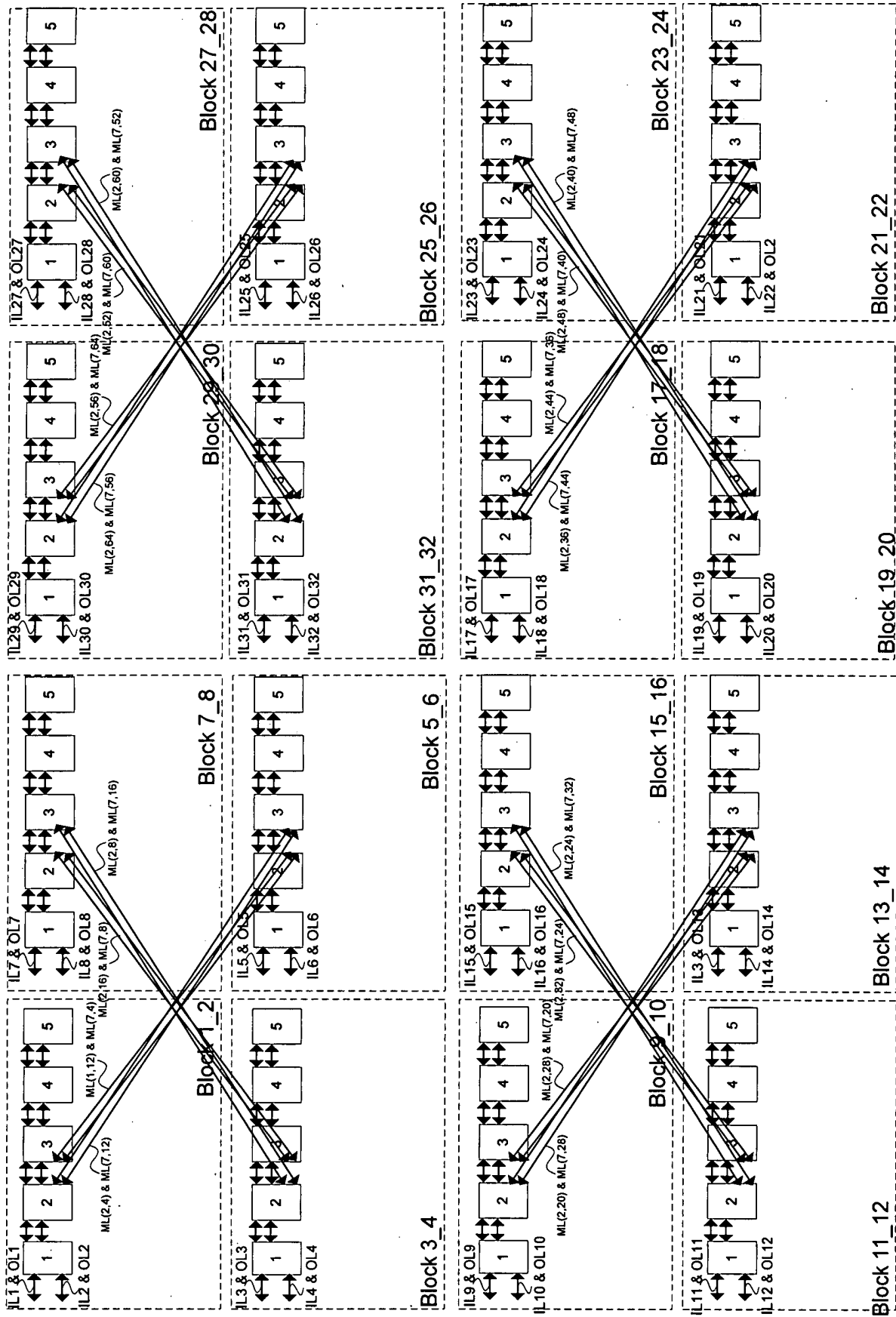


FIG. 3F

300F

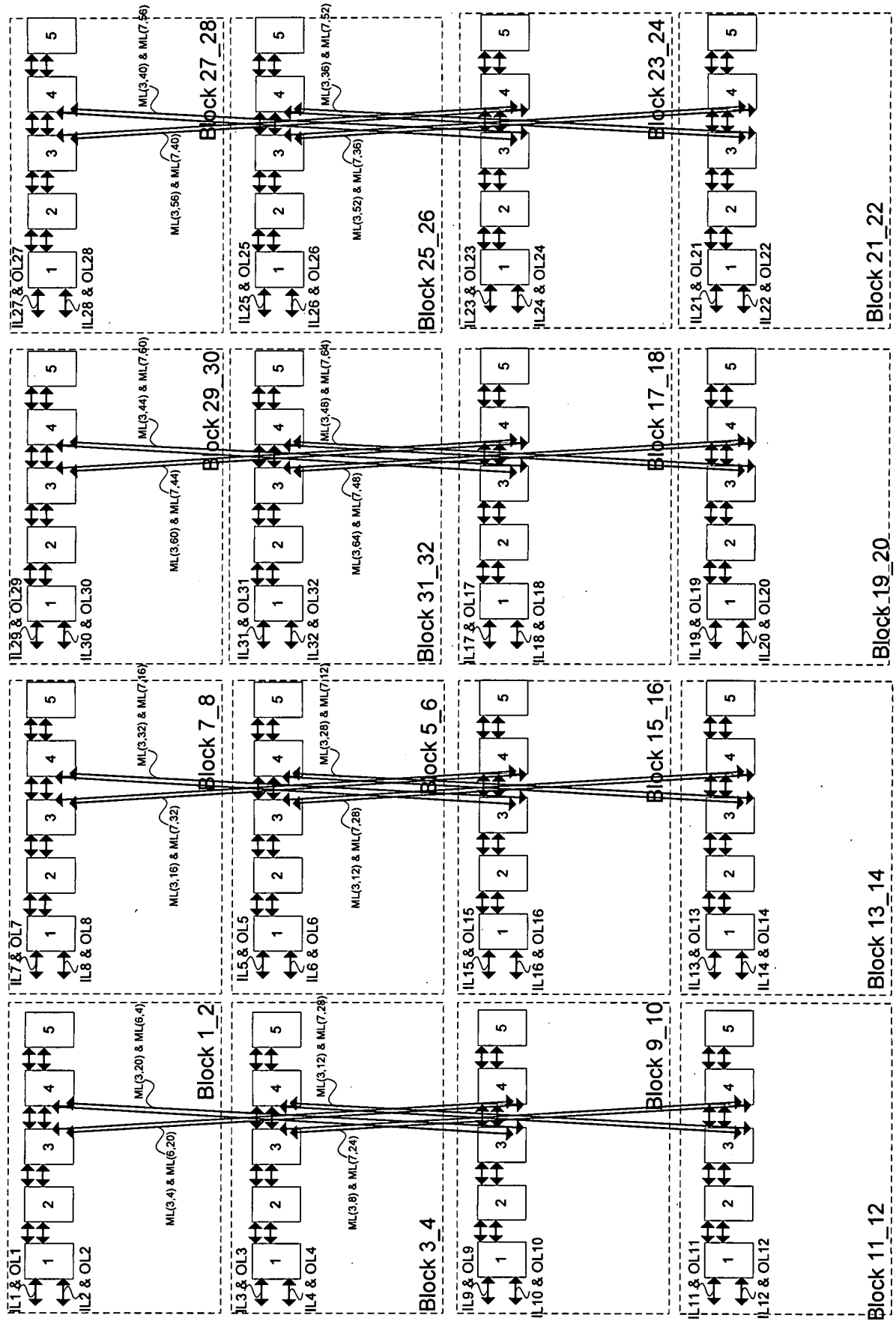


FIG. 3G

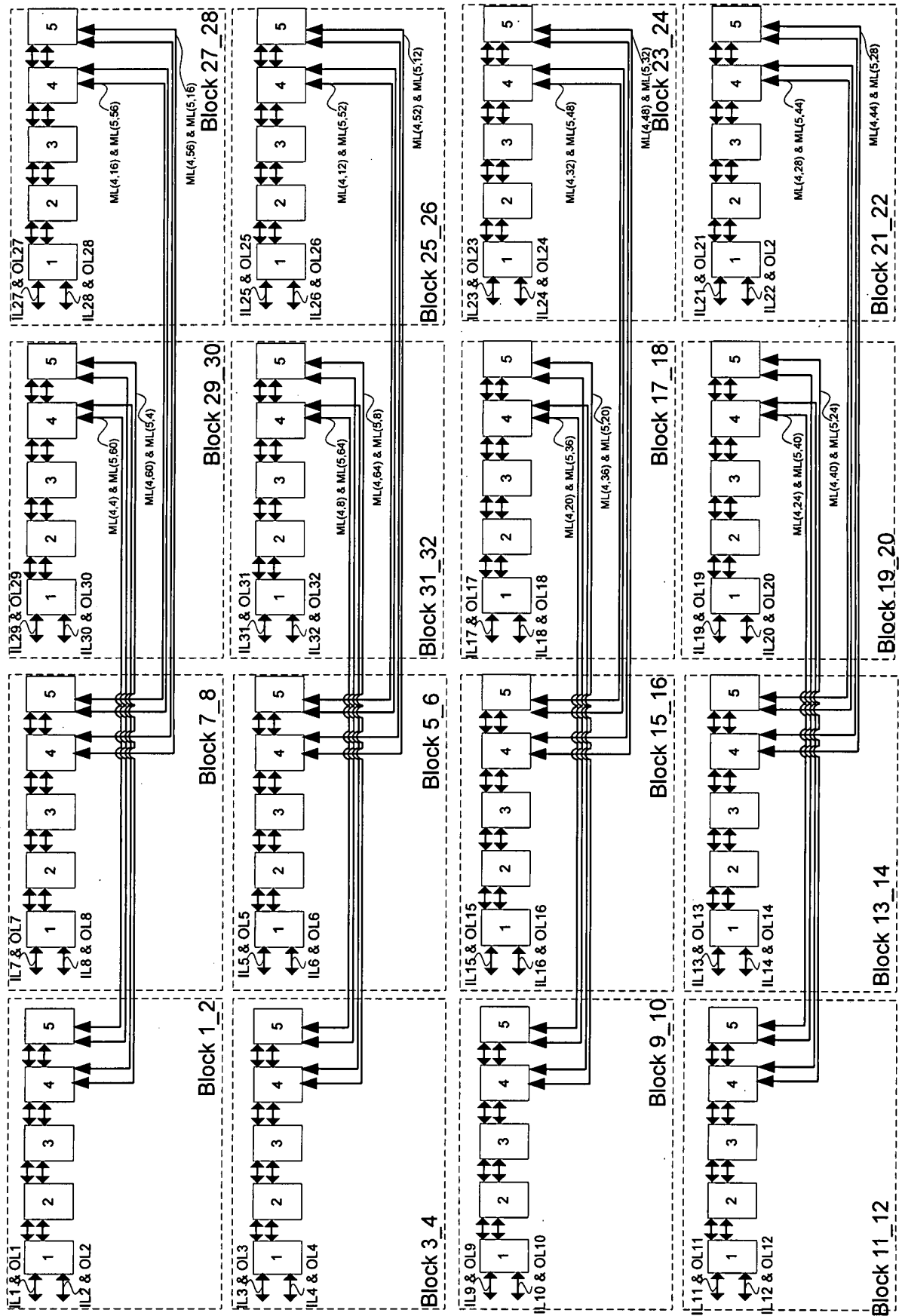


FIG. 3H

300H

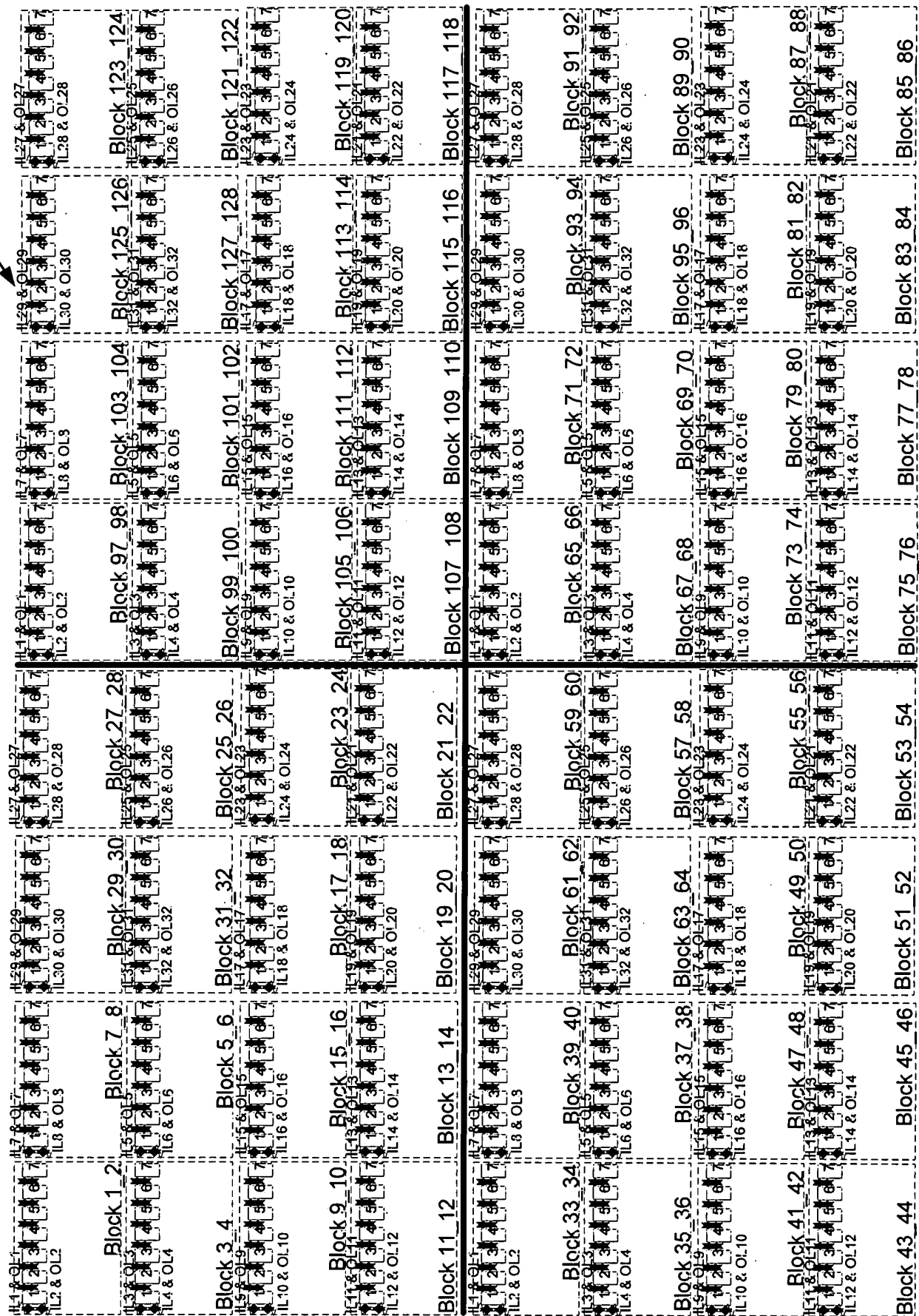


FIG. 4A

400A

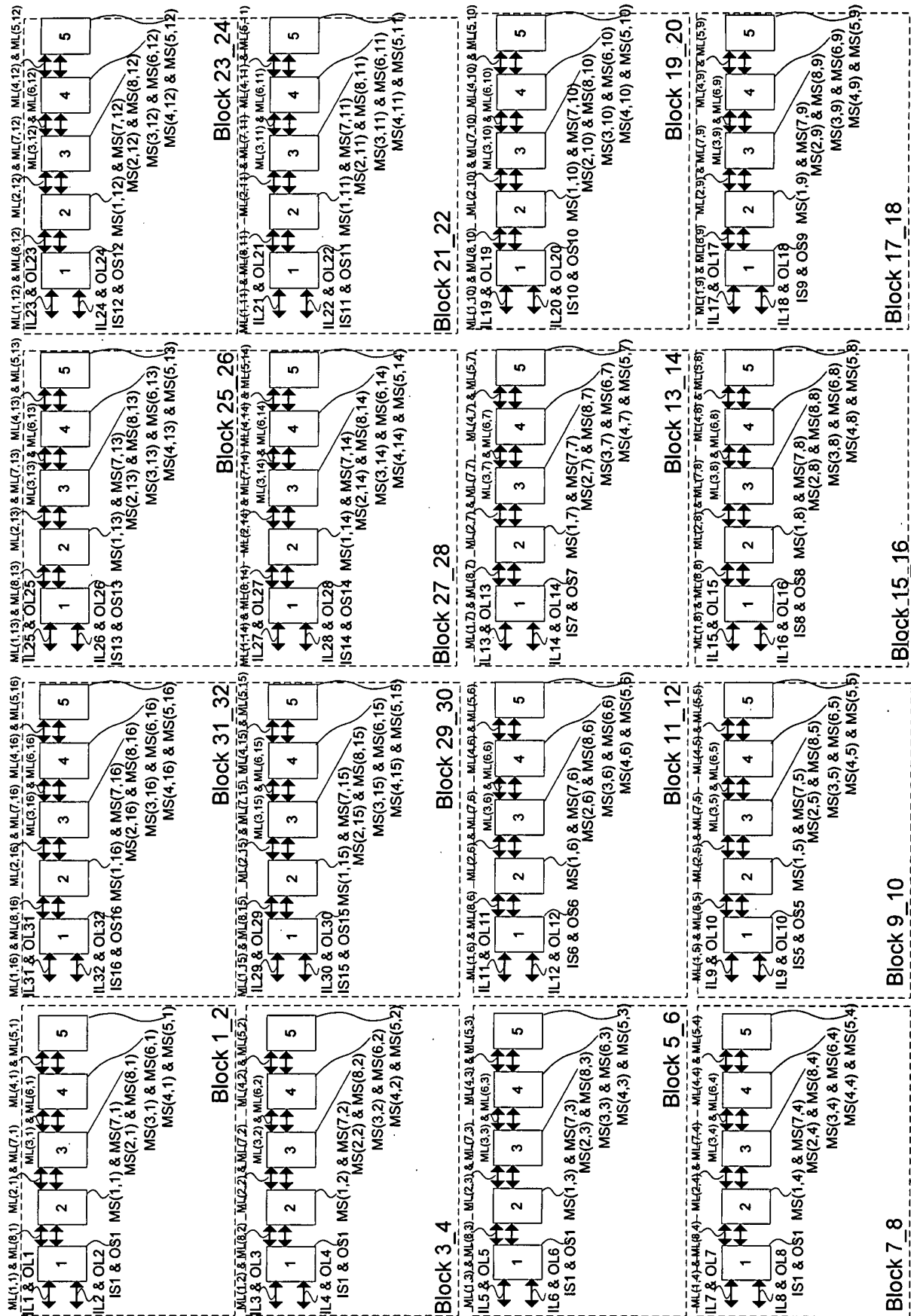


FIG. 4B

400B

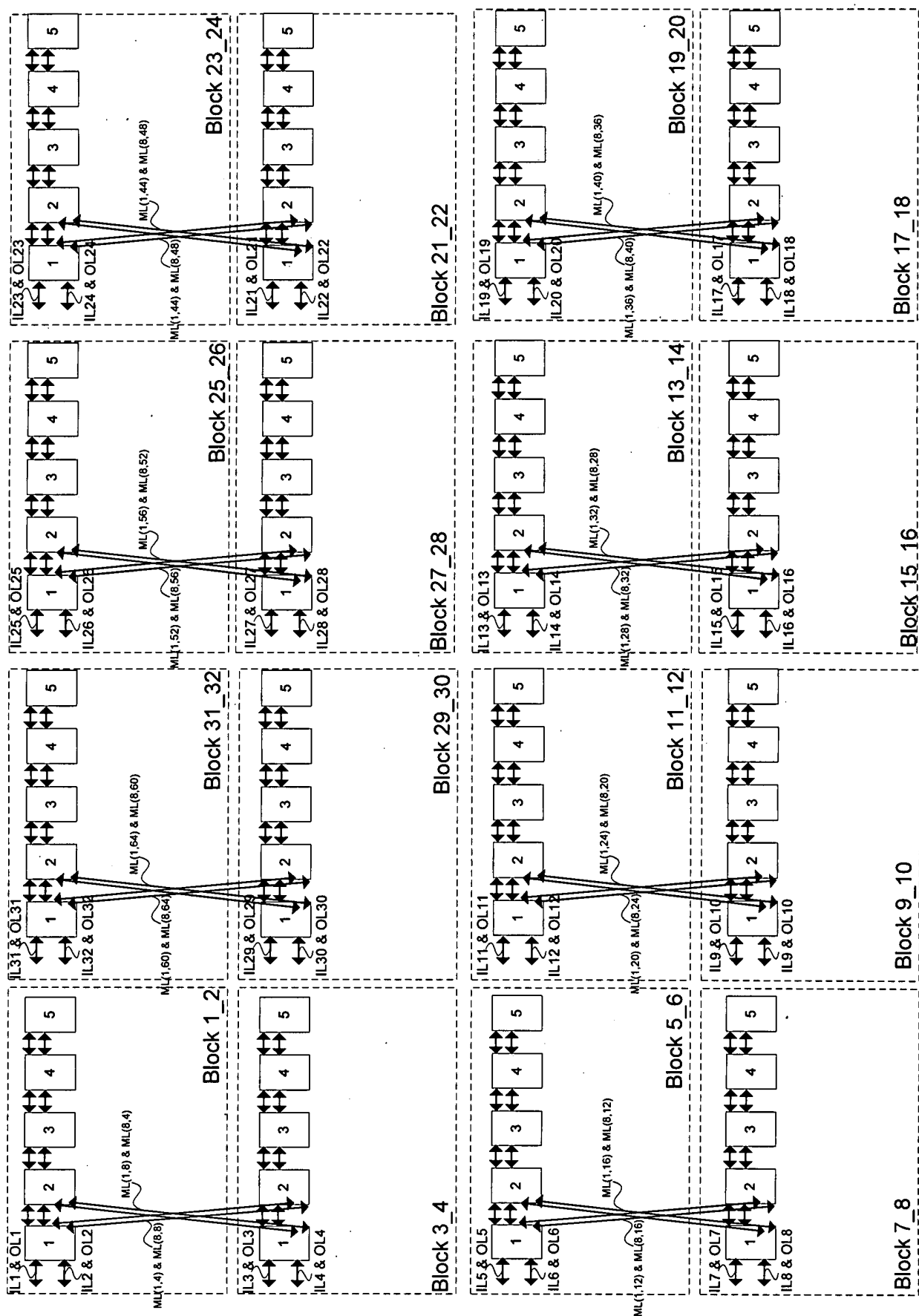


FIG. 4C

400C

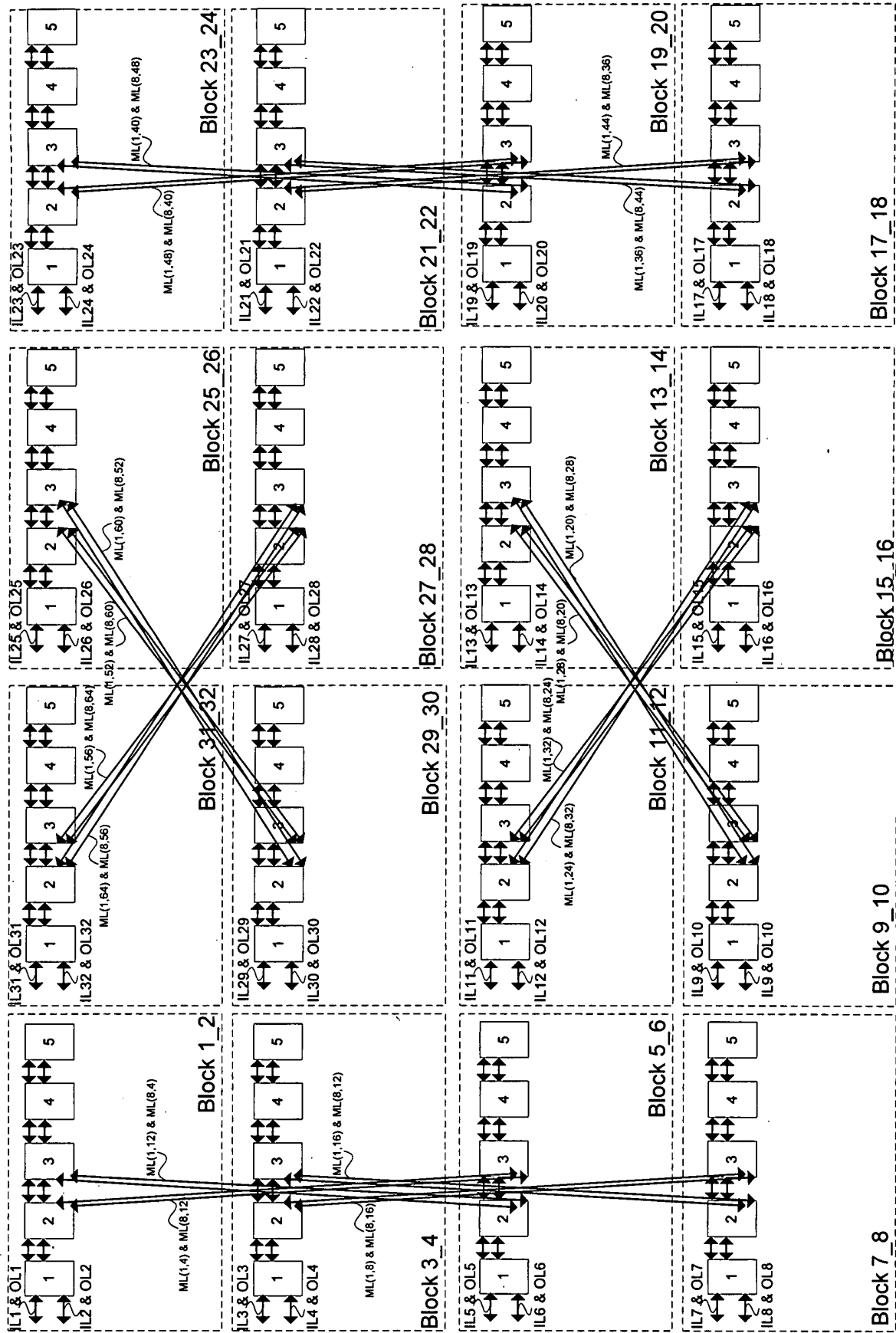


FIG. 4D

400D

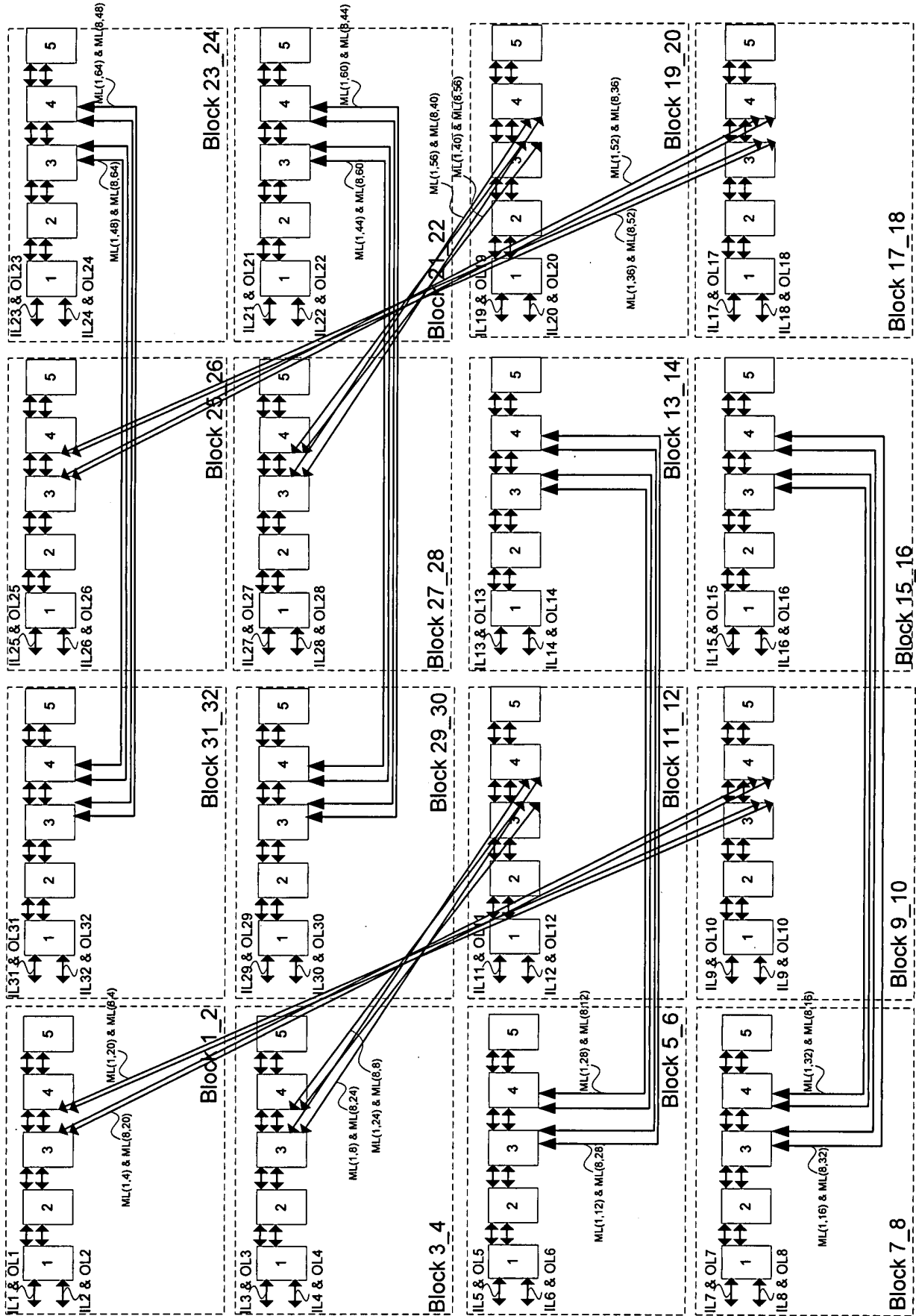


FIG. 4E

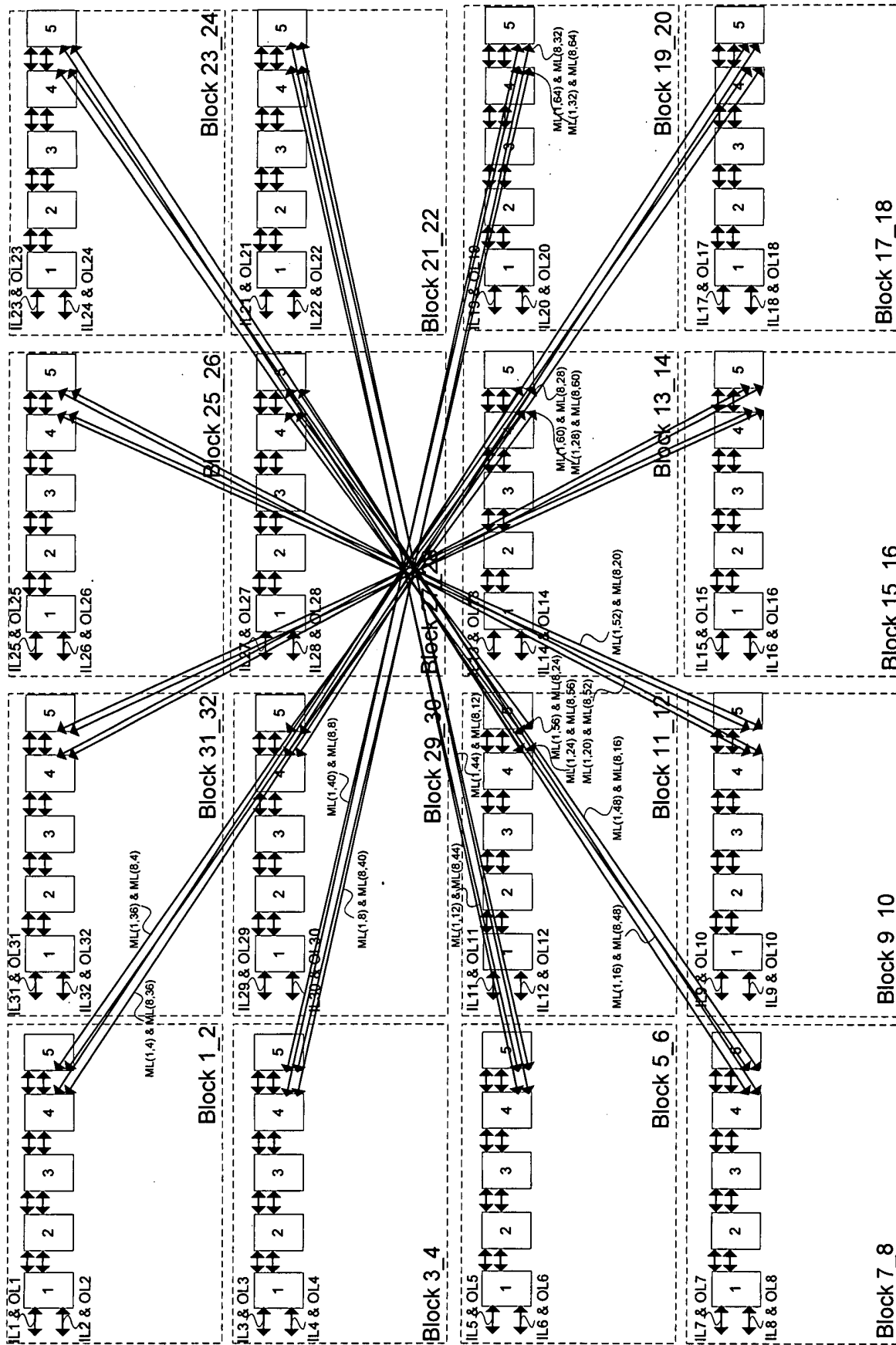
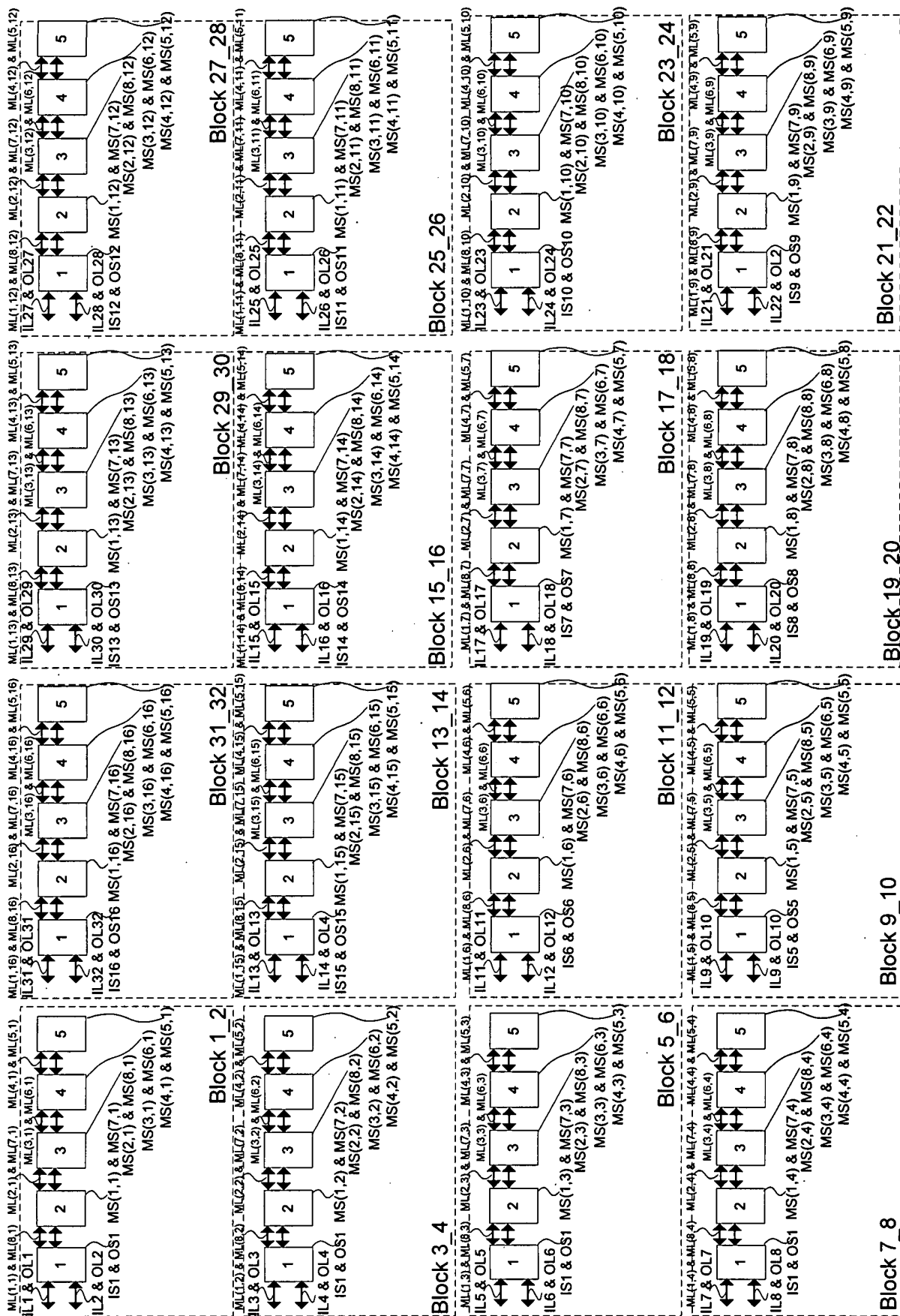


FIG. 4C1

400Ç1





UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
60/940,394	05/25/2007		100	M-0045US		

CONFIRMATION NO. 7100

38139
TEAK NETWORKS, INC.
6278 GRAND OAK WAY
SAN JOSE, CA95135

FILING RECEIPT

Date Mailed: 06/21/2007

Receipt is acknowledged of this provisional Patent Application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Be sure to provide the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION when inquiring about this application. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please mail to the Commissioner for Patents P.O. Box 1450 Alexandria Va 22313-1450. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections (if appropriate).**

Applicant(s)

Venkat Konda, Residence Not Provided;

Power of Attorney: None

If Required, Foreign Filing License Granted: 06/20/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is
US60/940,394

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

** SMALL ENTITY **

Title

VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file

additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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Title 35, United States Code, Section 184

Title 37, Code of Federal Regulations, 5.11 & 5.15

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NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license

under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).



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APPLICATION NUMBER	FILING OR 371 (c) DATE	FIRST NAMED APPLICANT	ATTORNEY DOCKET NUMBER
60/940,394	05/25/2007	Venkat Konda	M-0045US

38139
 TEAK NETWORKS, INC.
 6278 GRAND OAK WAY
 SAN JOSE, CA 95135

CONFIRMATION NO. 7100
FORMALITIES
LETTER

Date Mailed: 06/21/2007

NOTICE TO FILE MISSING PARTS OF PROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(c)

Filing Date Granted

An application number and filing date have been accorded to this provisional application. The items indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The provisional application cover sheet under 37 CFR 1.51(c)(1), which may be an application data sheet (37 CFR 1.76), is required identifying either city and state or city and foreign country of the residence of each inventor and the name(s) of the inventor(s).

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee or cover sheet) as set forth in 37 CFR 1.16(g) of \$25 for a small entity in compliance with 37 CFR 1.27, must be submitted with the missing items identified in this letter.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **\$25** for a small entity

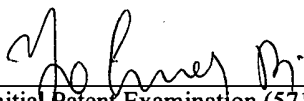
- **\$25 Surcharge.**

Replies should be mailed to: Mail Stop Missing Parts
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Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
<https://sportal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at 1-866-217-9197 or visit our website at <http://www.uspto.gov/ebs>.

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Office of Initial Patent Examination (571) 272-4000, or 1-800-PTO-9199
PART 3 - OFFICE COPY

PROVISIONAL APPLICATION FOR PATENT COVER SHEET – Page 1 of 2

This is a request for filing a PROVISIONAL APPLICATION FOR PATENT under 37 CFR 1.53(c).

Express Mail Label No. _____

INVENTOR(S)		
Given Name (first and middle [if any])	Family Name or Surname	Residence (City and either State or Foreign Country)
Venkat	Konda	San Jose, CA

Additional inventors are being named on the _____ separately numbered sheets attached hereto

TITLE OF THE INVENTION (500 characters max):

VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS

Direct all correspondence to: **CORRESPONDENCE ADDRESS**

☒ The address corresponding to Customer Number: 38139

OR

☐ Firm or Individual Name Teak Networks, Inc.

Address 6278, Grand Oak Way

City San Jose	State CA	Zip 95135
Country USA	Telephone 408-472-3273	Email venkat@teaknetworks.com

ENCLOSED APPLICATION PARTS (check all that apply)

<input type="checkbox"/> Application Data Sheet. See 37 CFR 1.76	<input type="checkbox"/> CD(s), Number of CDs _____
<input type="checkbox"/> Drawing(s) Number of Sheets _____	<input type="checkbox"/> Other (specify) _____
<input type="checkbox"/> Specification (e.g. description of the invention) Number of Pages _____	

Fees Due: Filing Fee of \$200 (\$100 for small entity). If the specification and drawings exceed 100 sheets of paper, an application size fee is also due, which is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).

METHOD OF PAYMENT OF THE FILING FEE AND APPLICATION SIZE FEE FOR THIS PROVISIONAL APPLICATION FOR PATENT

<input type="checkbox"/> Applicant claims small entity status. See 37 CFR 1.27.	
<input type="checkbox"/> A check or money order is enclosed to cover the filing fee and application size fee (if applicable).	
<input type="checkbox"/> Payment by credit card. Form PTO-2038 is attached	
<input type="checkbox"/> The Director is hereby authorized to charge the filing fee and application size fee (if applicable) or credit any overpayment to Deposit Account Number: _____ A duplicative copy of this form is enclosed for fee processing.	

TOTAL FEE AMOUNT (\$)

USE ONLY FOR FILING A PROVISIONAL APPLICATION FOR PATENT

This collection of information is required by 37 CFR 1.51. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11 and 1.14. This collection is estimated to take 8 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**
If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

PROVISIONAL APPLICATION COVER SHEET
Page 2 of 2

PTO/SB/16 (02-07)

Approved for use through 02/28/2007. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

The invention was made by an agency of the United States Government or under a contract with an agency of the United States Government.



No.



Yes, the name of the U.S. Government agency and the Government contract number are: _____

WARNING:

Petitioner/applicant is cautioned to avoid submitting personal information in documents filed in a patent application that may contribute to identity theft. Personal information such as social security numbers, bank account numbers, or credit card numbers (other than a check or credit card authorization form PTO-2038 submitted for payment purposes) is never required by the USPTO to support a petition or an application. If this type of personal information is included in documents submitted to the USPTO, petitioners/applicants should consider redacting such personal information from the documents before submitting them to the USPTO. Petitioner/applicant is advised that the record of a patent application is available to the public after publication of the application (unless a non-publication request in compliance with 37 CFR 1.213(a) is made in the application) or issuance of a patent. Furthermore, the record from an abandoned application may also be available to the public if the application is referenced in a published application or an issued patent (see 37 CFR 1.14). Checks and credit card authorization forms PTO-2038 submitted for payment purposes are not retained in the application file and therefore are not publicly available.

SIGNATURE Venkat Konda Date 8/1/2007

TYPED or PRINTED NAME Venkat Konda REGISTRATION NO. _____
(if appropriate)

TELEPHONE 408-472-3273 Docket Number: M-0045 US

APPLICATION # 60/940,394

Electronic Patent Application Fee Transmittal

Application Number:	60940394			
Filing Date:	25-May-2007			
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS			
First Named Inventor/Applicant Name:	Venkat Konda			
Filer:	Venkar Konda			
Attorney Docket Number:	M-0045US			
Filed as Small Entity				
Provisional Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late provisional filing fee/cover sheet	2052	1	25	25
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				25

Electronic Acknowledgement Receipt

EFS ID:	2038503
Application Number:	60940394
International Application Number:	
Confirmation Number:	7100
Title of Invention:	VLSI LAYOUTS OF FULLY CONNECTED GENERALIZED NETWORKS
First Named Inventor/Applicant Name:	Venkat Konda
Customer Number:	38139
Filer:	Venkar Konda
Filer Authorized By:	
Attorney Docket Number:	M-0045US
Receipt Date:	01-AUG-2007
Filing Date:	25-MAY-2007
Time Stamp:	21:54:09
Application Type:	Provisional

Payment information:

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1	Application Data Sheet	M-0045US-CoverSheet.PDF	147168 7689f582db8f01730bf4a9b31997bc9ef 67182f2	no	2
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2	Fee Worksheet (PTO-06)	fee-info.pdf	8168 1294ae0647827b09bb9cbb04dbff5493 231f267f	no	2
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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
60/940,394	05/25/2007		125	M-0045 US		

CONFIRMATION NO. 7100

38139
TEAK NETWORKS, INC.
6278 GRAND OAK WAY
SAN JOSE, CA 95135

UPDATED FILING RECEIPT

Date Mailed: 09/24/2007

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Applicant(s)

Venkat Konda, San Jose, CA;

Power of Attorney: None**If Required, Foreign Filing License Granted:** 06/20/2007

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is
US60/940,394

Projected Publication Date: None, application is not eligible for pre-grant publication**Non-Publication Request:** No**Early Publication Request:** No

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