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Paper 13
Entered: September 19, 2019

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

FLEX LOGIX TECHNOLOGIES INC.,
Petitioner,

v.

VENKAT KONDA,
Patent Owner.

Case PGR2019-00040
Patent 10,003,553 B2

Before PATRICK M. BOUCHER, CHARLES J. BOUDREAU, and
NORMAN H. BEAMER, *Administrative Patent Judges*.

BOUCHER, *Administrative Patent Judge*.

DECISION
Denying Institution of Post-Grant Review
35 U.S.C. § 324

Flex Logix Technologies, Inc. (“Petitioner”) filed a Petition (Paper 1, “Pet.”) pursuant to 35 U.S.C. §§ 321–329 to institute a post-grant review of claims 1–7, 9–15, and 17–19 of U.S. Patent No. 10,003,553 B2 (“the ’553

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patent”). Venkat Konda (“Patent Owner”)¹ filed a Preliminary Response (Paper 5, “Prelim. Resp.”). For the reasons set forth below, we exercise our discretion under 35 U.S.C. § 324 and deny the Petition.

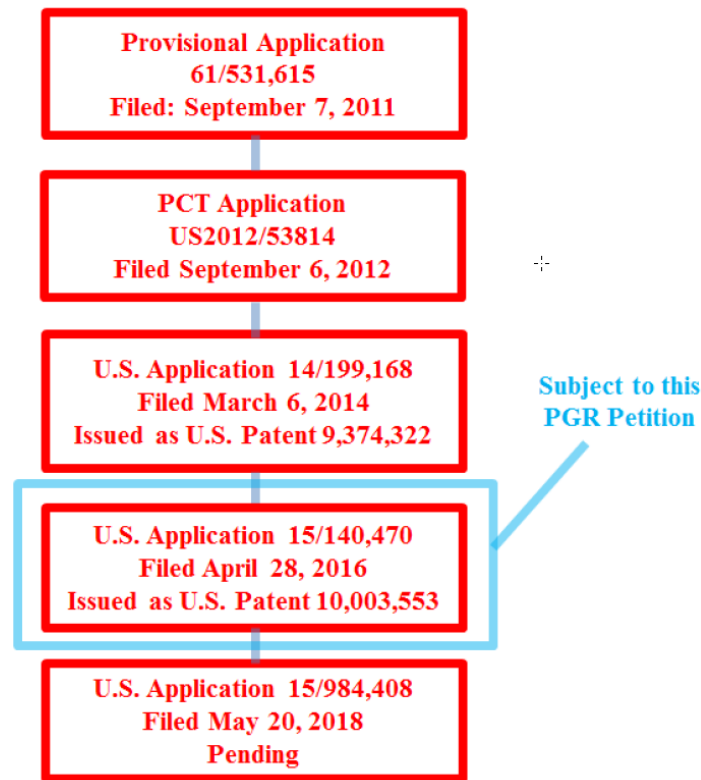
I. BACKGROUND

A. *The ’553 Patent*

The ’553 patent was filed on April 28, 2016, and claims the benefit of the following: (1) the March 6, 2014 filing date of U.S. Patent Appl. No. 14/199,168 (now issued as U.S. Patent No. 9,374,322 (“the ’322 patent”)); (2) the September 6, 2012 filing date of PCT/US12/53814 (“the ’814 PCT application”); and (3) the September 7, 2011 filing date of Provisional Patent Appl. No. 61/531,615 (“the ’615 provisional application”). Ex. 1001, 1:8–14; Ex. 1004, 1 (Certificate of Correction). A summary drawing provided by Petitioner is reproduced below. Pet. 4.

¹ The Petition identifies the owner of the ’553 patent as Konda Technologies, Inc. Pet. 1. This appears to have been correct at the time the Petition was filed, on March 18, 2019. But on April 8, 2019, an assignment was recorded with the Office at reel/frame 048822/0867 assigning the ’553 patent to Venkat Konda. This ownership is also reflected in Patent Owner’s mandatory notices, filed on April 9, 2019. Paper 4.

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Petitioner’s drawing summarizes certain claims to earlier filing dates, and is similar to a drawing provided by Patent Owner that is in substantial agreement. *See* Prelim. Resp. 7. Although the drawing also refers to U.S. Patent Appl. No. 15/984,408, that application is not relevant to this proceeding. In addition, the ’553 patent recites that it incorporates the “entirety” of several additional patents and applications. *Id.* at 1:14–2:62.

The ’553 patent relates to multi-stage interconnection networks that find utility in multiple applications. *Id.* at 2:66–3:1. According to the ’553 patent, very large scale integration (“VLSI”) layouts for integrated circuits with such networks can be “inefficient and complicated.” *Id.* at 3:2–4. For example, prior-art networks of the type identified by the ’553 patent “require large area to implement the switches on the chip, large number of wires, longer wires, with increased power consumption, increased latency of the

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signals which [a]ffect the maximum clock speed of operation.” *Id.* at 3:43–48.

Accordingly, the ’553 patent discloses a number of configurations of multi-stage hierarchical networks. One example is illustrated in Figure 1A of the patent, reproduced below.

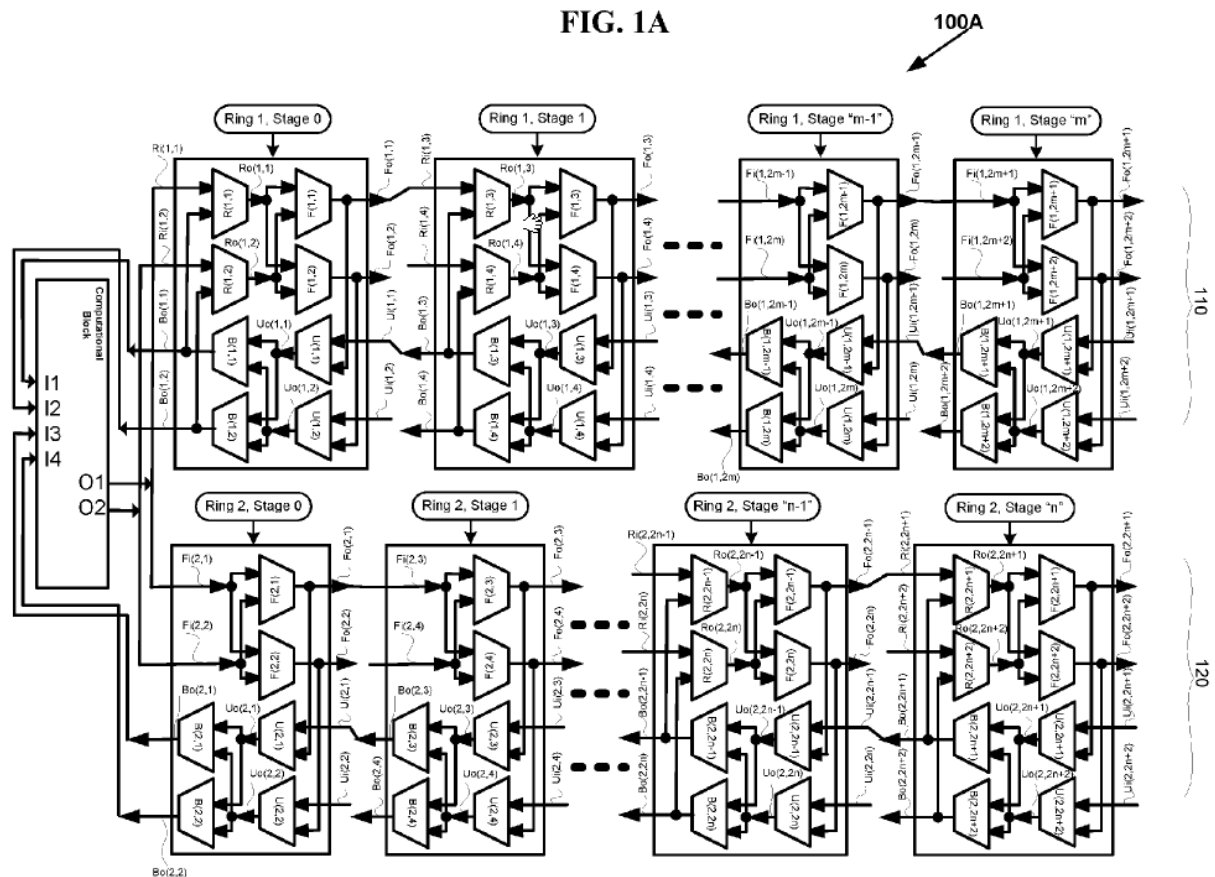


Figure 1A illustrates an exemplary partial multi-stage hierarchical network (or “block”) in which each computational block has four inlet links I1, I2, I3, I4 and two outlet links O1, O2. *Id.* at 8:57–62. For each computational block, a corresponding partial multi-stage hierarchical network has two “rings” 110, 120. *Id.* at 8:62–9:3. Ring 110 has inlet links Ri(1,1), Ri(1,2) and outlet links Bo(1,1), Bo(1,2). *Id.* at 9:4–6. Ring 120 similarly has inlet

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links $Fi(2,1)$, $Fi(2,2)$ and outlet links $Bo(2,1)$, $Bo(2,2)$. *Id.* at 9:5–6. The partial multi-stage hierarchical network thus has four inlet links and four outlet links corresponding to the two rings 110, 120. *Id.* at 9:6–9.

Several connections characterize the specific structure illustrated. First, outlet link O1 is connected to inlet link $Ri(1,1)$ of ring 110 and also to inlet link $Fi(2,1)$ of ring 120. *Id.* at 9:9–11. Second, outlet link O2 is connected to inlet link $Ri(1,2)$ of ring 110 and also to inlet link $Fi(2,2)$ of ring 120. *Id.* at 9:11–13. Third, outlet link $Bo(1,1)$ of ring 110 is connected to inlet link I1. *Id.* at 9:14–15. Fourth, outlet link $Bo(1,2)$ of ring 110 is connected to inlet link I2. *Id.* at 9:15–16. Fifth, outlet link $Bo(2,1)$ of ring 120 is connected to inlet link I3. *Id.* at 9:17–18. Sixth, outlet link $Bo(2,2)$ of ring 120 is connected to inlet link I4. *Id.* at 9:18–20. Because outlet link O1 is connected to both inlet link $Ri(1,1)$ of ring 110 and inlet link $Fi(2,1)$ of ring 120, and outlet link O2 is connected to both inlet link $Ri(1,2)$ of ring 110 and inlet link $Fi(2,2)$ of ring 120, the partial multi-stage hierarchical network has two inlet links and four outlet links. *Id.* at 9:20–26.

The drawing also illustrates multiple “stages.” Ring 110 (i.e., ring 1) consists of $m+1$ stages, and ring 120 (i.e., ring 2) consists of $n+1$ stages. *Id.* at 8:65–9:1. For example, “ring 1, stage 0” has four inputs $Ri(1,1)$, $Ri(1,2)$, $Ui(1,1)$, $Ui(1,2)$ and four outputs $Bo(1,1)$, $Bo(1,2)$, $Fo(1,1)$, $Fo(1,2)$. *Id.* at 9:62–66. That stage also has eight 2:1 multiplexers $R(1,1)$, $R(1,2)$, $F(1,1)$, $F(1,2)$, $U(1,1)$, $U(1,2)$, $B(1,1)$, $B(1,2)$. *Id.* at 9:66–10:2. Multiplexer $R(1,1)$ has two inputs $Ri(1,1)$, $Bo(1,1)$ and one output $Ro(1,1)$. *Id.* at 10:2–3. Multiplexer $R(1,2)$ has two inputs $Ri(1,2)$, $Bo(1,2)$ and one output $Ro(1,2)$. *Id.* at 10:3–6. Multiplexer $F(1,1)$ has two inputs $Ro(1,1)$, $Ro(1,2)$ and one

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output Fo(1,1). *Id.* at 10:5–6. Multiplexer F(1,2) has two inputs Ro(1,1), Ro(1,2) and one output Fo(1,2). *Id.* at 10:6–8. Multiplexer U(1,1) has two inputs Ui(1,1), Fo(1,1) and one output Uo(1,1). *Id.* at 10:9–10. Multiplexer U(1,2) has two inputs Ui(1,2), Fo(1,2) and one output Uo(1,2). *Id.* at 10:10–12. Multiplexer B(1,1) has two inputs Uo(1,1), Uo(1,2) and one output Bo(1,1). *Id.* at 10:12–13. Multiplexer B(1,2) has two inputs Uo(1,1), Uo(1,2) and one output Bo(1,2). *Id.* at 10:13–15. The patent also details the connections of other stages that appear in the drawing, some of which also have eight multiplexers and others of which have only six multiplexers. *Id.* at 10:16–12:59.

As illustrated by Figure 8 of the '553 patent (not reproduced here), multiple blocks like those shown in Figure 1A may be arranged in a two-dimensional grid. *Id.* at 9:27–35. In such an arrangement, each block of the grid is part of the die area of a semiconductor integrated circuit so that the complete two-dimensional grid represents the complete die of the semiconductor integrated circuit. *Id.* at 9:36–39.

Figure 3 of the '553 patent is reproduced below.

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300A

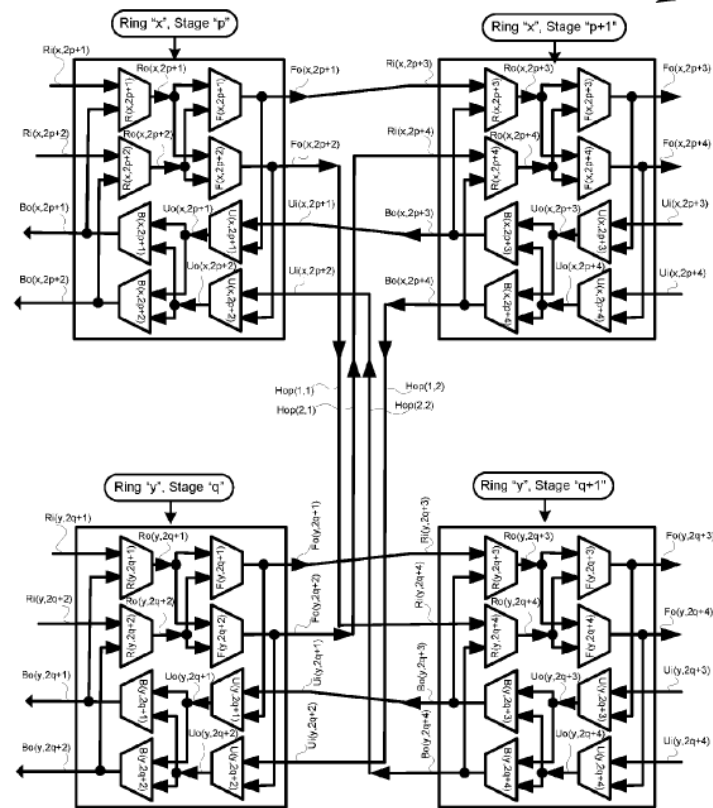


Figure 3A illustrates connections between successive stages of a ring “x” and two successive stages of another ring “y.” *Id.* at 20:42–48. Of particular relevance are the “hop” connections between the distinct rings: Hop(1,1) connects output Fo(x,2p+2) to input Ri(y,2q+4), Hop(1,2) connects output Bo(x,2p+4) to input Ui(y,2q+2), Hop(2,1) connects output Fo(y,2q+2) to input Ri(x,2p+4), and Hop(2,2) connects output Bo(y,2q+4) to input Ui(x,2p+2). *Id.* at 22:15–26. The ’553 patent explains that rings x and y “may or may not belong to the same block of the complete multi-stage hierarchical network.” *Id.* at 22:29–30. If the rings belong to the same block, the hop connections are referred to as “internal hop wires”; conversely, if the rings belong to different blocks, they are referred to as “external hop wires.” *Id.* at 22:29–40. External hop wires may be

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“horizontal wires or vertical wires,” and the length of external hop wires, referred to as “hop length,” is the “manhattan distance between the corresponding blocks,” i.e. the sum of the vertical and horizontal differences separating the blocks. *Id.* at 22:40–63. Hop lengths are “positive integer[s].” *Id.* at 29:40–41, 32:18–19.

B. Illustrative Claim

Independent claim 1 of the '553 patent is illustrative of the challenged claims, and is reproduced below.

1. A network implemented in a non-transitory medium comprising a plurality of subnetworks and a plurality of inlet links and a plurality of outlet links,
said plurality of subnetworks arranged in a two-dimensional grid of rows and columns; and
each subnetwork comprising y stages, where $y \geq 1$; and
each stage comprising a switch of size $d_i \times d_o$, where $d_i \geq 2$ and $d_o \geq 2$ and each switch of size $d_i \times d_o$ having d_i incoming links and d_o outgoing links; and
Said inlet links are connected to one or more of said incoming links of a said switch of a said stage of a said subnetwork, and said outlet links are connected to one of said outgoing links of a said switch of a said stage of a said subnetwork; and
each subnetwork of the plurality of subnetworks may or may not be comprising the same number of said inlet links and may or may not be comprising the same number of said outlet links; each subnetwork of the plurality of subnetworks may or may not be comprising the same number of said stages; each stage may or may not be comprising the same number of switches; and each switch in each stage may or may not be of the same size, each multiplexer in each stage may or may not be of the same size and

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Said incoming links and outgoing links in each switch in each stage of each subnetwork comprising a plurality of forward connecting links connected from switches in a stage to switches in another stage in same said subnetwork or another said subnetwork, and also comprising a plurality of backward connecting links connected from switches in a stage to switches in another stage in same subnetwork or another said subnetwork; and

Said forward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks, and

Said backward connecting links comprising zero or more straight links connected from a switch in a stage in a subnetwork to a switch in another stage in the same subnetwork; and also comprising zero or more cross links connected from a switch in a stage in a subnetwork to a switch in the same numbered stage in one or more other subnetworks.

Ex. 1001, 48:62–49:40.

C. Asserted Grounds of Unpatentability

Petitioner relies on U.S. Patent No. 6,940,308 B2 (“Wong”) to challenge claims 1–7, 9–15, and 17–19 on the following ground:

Claims Challenged	Statutory basis	Reference
1–7, 9–15, and 17–19	§ 102(a)(1)	Wong

Petitioner supports its challenges with a Declaration by R. Jacob Baker, Ph.D., P.E. Ex. 1002.

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D. Real Parties in Interest

The parties identify only themselves as real parties in interest. Pet. 2; Paper 4, 2.

E. Related Proceedings

The '553 patent was involved in *Konda Technologies Inc. v. Flex Logix Technologies, Inc.*, No. 5:18-cv-07581-LHK (N.D. Cal.). See Pet. 3. Subsequent to filing of the Petition, this action has apparently been dismissed without prejudice. Paper 10, 2. The '553 patent is also the subject of concurrently filed petitions in PGR2019-00037 and PGR2019-00042. Pet. 4; Prelim. Resp. 2.

II. ANALYSIS

As noted above, the instant Petition is one of three petitions filed by Petitioner challenging claims of the '553 patent. *Sua sponte*, we ordered Petitioner to submit a ranking of the three petitions in the order it wishes the panel to consider the merits, as well as a succinct explanation of the differences between the petitions and why those differences are material. Paper 9. Petitioner complied with the order and Patent Owner responded. Papers 10, 12.

Under 35 U.S.C. § 314(a), the Director has discretion to deny institution of an *inter partes* review. *Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2140 (2016) (“[T]he agency’s decision to deny a petition is a matter committed to the Patent Office’s discretion.”); *SAS Inst. Inc. v. Iancu*, 138 S. Ct. 1348, 1356 (2018) (“[Section] 314(a) invests the Director with

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discretion on the question whether to institute review” (emphasis omitted)); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he PTO is permitted, but never compelled, to institute an IPR proceeding.”).

Our discretionary determination of whether to institute review takes into consideration guidance in the Patent Office Trial Practice Guide, August 2018 Update, 83 Fed. Reg. 39,989 (August 13, 2018) (hereinafter “2018 Trial Practice Guide Update”), available at <https://go.usa.gov/xU7GP>. In particular, the Trial Practice Guide states

[t]here may be other reasons besides the “follow-on” petition context where the “effect . . . on the economy, the integrity of the patent system, the efficient administration of the Office, and the ability of the Office to timely complete proceedings,” 35 U.S.C. § 316(b), favors denying a petition even though some claims meet the threshold standards for institution under 35 U.S.C. §§ 314(a), 324(a). This includes, for example, events in other proceedings related to the same patent, either at the Office, in district courts, or the ITC.

2018 Trial Practice Guide Update 10–11.² We are also mindful to construe our rules to “secure the just, speedy, and inexpensive resolution of every proceeding.” 37 C.F.R. § 42.1(b); *Deeper, UAB v. Vexilar, Inc.*, IPR2018-01310, Paper 7 at 42 (PTAB Jan. 24, 2019) (informative). Of the three petitions, PGR2019-00037 is directed to challenges raised under 35 U.S.C. § 112, and the other two petitions are directed to prior art challenges raised under 35 U.S.C. §§ 102 and 103. *See* Paper 10, 2. Petitioner asserts that “[g]iven the number of claims, the length thereof (totaling about 2,086

² *See also* Patent Office Trial Practice Guide, July 2019 Update, 84 Fed. Reg. 33,925 (July 16, 2019), 26–28.

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words), and the number of grounds under § 112 alone, Petitioner could not have raised both the § 112 grounds and prior art grounds in the same petition.” *Id.* at 3. “Similarly,” according to Petitioner, “the length of the claims and requirement to demonstrate PGR eligibility . . . prevented Petitioner from combining all the prior art grounds in a single petition.” *Id.* Both parties agree that PGR2019-00037 should be ranked highest in the order of potential consideration. *Id.* at 3; Paper 12, 2 (“Patent Owner concurs with Petitioner’s ‘ranking.’”).

Petitioner’s argument regarding the distinct nature of the § 112 challenges and the prior-art challenges, coupled with the length limitations imposed on petitions for post-grant review, is persuasive. But we agree with Patent Owner that “at most two Petitions would be needed, one to consider the issues under § 112 and the other to consider §§ 102 and 103 issues.” Paper 12, 2–3; *see* H.R. Rep. No. 112-98, pt. 1, at 48 (2011) (warning the AIA’s procedures should not be used as tools for harassment). Accordingly, although we institute post-grant review in both PGR2019-00037 and PGR2019-00042 for the reasons set forth in concurrently issued decisions, we decline also to institute review in this proceeding.

Both PGR2019-00040 and PGR2019-00042 involve the same petitioner and the same claims. Comparison of the petitions in PGR2019-00040 and PGR2019-00042 demonstrates that the anticipation grounds are substantially similar. We do not find any differences between the asserted art and arguments to be sufficiently material to outweigh the inefficiencies and costs of instituting both proceedings. PCT Application No. WO 2008/109756, which is the reference relied on in PGR2019-00042,

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names Patent Owner as inventor and contains terms and expresses concepts that track comparable portions of the '553 patent in a number of respects—thus tipping the balance of discretion towards our initiating review in PGR2019-00042 and declining to do so in this proceeding.

We have considered, but are not persuaded by, Petitioner's argument that it had insufficient "notice before filing that ranking its petitions would be required." Paper 10, 5. As noted above, the Director has always possessed statutory discretion whether to institute an *inter partes* based on a petition, both before and after promulgation of the Trial Practice Guide Update cited in our Order (Paper 9). *See* 35 U.S.C. § 314(a).

III. ORDER

It is

ORDERED that the Petition is *denied* and no trial is instituted.

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