

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

FLEX LOGIX TECHNOLOGIES INC,

Petitioner

V.

VENKAT KONDA,

Patent Owner

Case IPR2020-00262

Patent 8,269,523 B2

PATENT OWNER VENKAT KONDA'S PRELIMINARY RESPONSE
PURSUANT TO 37 C.F.R. § 42.107

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PATENT OWNER'S EXHIBIT LIST 1

Exhibit No.	Description
Ex. 2001	Venkat Konda Declaration
Ex. 2002	2011 paper at VLSI Symposium of circuits, by Co-founders of Petitioner Flex Logix Technologies Inc. plagiarizing the 2D-layouts disclosed in the 8,269,523 patent
Ex. 2003	2009 DARPA Proposal submitted by Co-founders of Petitioner Flex Logix Technologies Inc. illustrating the long felt need and commercial recognition of 2D-layouts disclosed in the 8,269,523 patent
Ex. 2004	2013 PhD Dissertation by Co-founder of Petitioner Flex Logix Technologies Inc. plagiarizing the 2D-layouts disclosed in the 8,269,523 patent
Ex. 2005	File history of the reissue application 16/202,067 for the 8,269,523 patent currently under prosecution
Ex. 2006	Computer Science Notes for Graduate course "Parallel Computing" for Chapter 2 - Parallel Architectures and interconnection networks, by Prof. Stewart Weiss at City University of New York

TABLE OF AUTHORITIES

Cases

<i>Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH</i> , IPR2019-01469, Paper 6 (Feb. 13, 2020) (precedential)	41, 47
<i>Becton, Dickinson and Co. v. B. Braun Melsungen AG</i> , IPR2017-01586, slip op. at 17–18 (Paper 8) (PTAB Dec. 15, 2017) (informative).	41
<i>Daiichi Sankyo Co. v. Apotex, Inc.</i> , 501 F.3d 1254, 1256 (Fed. Cir. 2007)	7
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<i>Envtl. Designs, Ltd. v. Union OilCo.</i> , 713 F.2d 693, 696 (Fed. Cir. 1983)	7
<i>Graham v. John Deere Co.</i> , 383 U.S. 1 (1966).	47
<i>Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.</i> , 707 F.2d 1376, 1381-82 (Fed. Cir. 1983)	7
<i>Stryker Corp v. KFX Medical, LLC</i> , IPR2019-00817 (PTAB Sep. 16, 2019) (Paper 10)	46
<i>Transocean Offshore Deepwater Drilling, Inc. v. Maersk Drilling USA, Inc.</i> , 699 F.3d 1340, 1349 (Fed. Cir. 2012)	47

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I. INTRODUCTION

Patent Owner Venkat Konda (“Patent Owner”) submits this Preliminary Response pursuant to 37 C.F.R. § 42.107 in opposition to the petition for *inter partes* review (“IPR”) IPR2020-00262¹ filed by Flex Logix Technologies Inc. (“Flex Logix” or “Petitioner”) regarding the claims 1, 15-18, 20-22, 32 and 47 (the “Challenged Claims”) of U.S. Patent No. 8,269,523 (Ex. 1001, “the ‘523 Patent”) on December 16, 2019 Paper 1 (“Petition”). This Preliminary Response is filed within three months of the Notice issued December 24, 2019 as extended².

Patent Owner respectfully requests that the Board decline to initiate *inter partes* review of the Challenged Claims of the ‘523 Patent because Petitioner has

¹ Petitioner concurrently filed two additional petitions for IPR of the ‘523 Patent. Those two petitions are IPR2020-00260 and IPR2020-00261.

² The Board first extended the due date of this preliminary response by two weeks i.e., until April 7, 2020, in an email communication due to the shelter-in-place in California and all over the country because of the Covid-19 pandemic and for the second time further extended the due date of this preliminary response by issuing a scheduling Order (Paper 5) until May 6, 2020 since the patent owner requested further extension by email communication in view of CARES act that came into effect on March 31, 2020.

failed to show it has a reasonable likelihood of prevailing with respect to any of the Challenged Claims, 35 U.S.C. § 314(a). Petitioner has submitted proposed grounds for challenge based on anticipation and obviousness. However, for each proposed ground, at least one claim element is missing from the references. Thus, Petitioner has failed to meet its initial burden to show that each element was known, and that the claims are anticipated or obvious, in light of the prior art. The Board should therefore deny institution of *inter partes* review of the Challenged Claims.

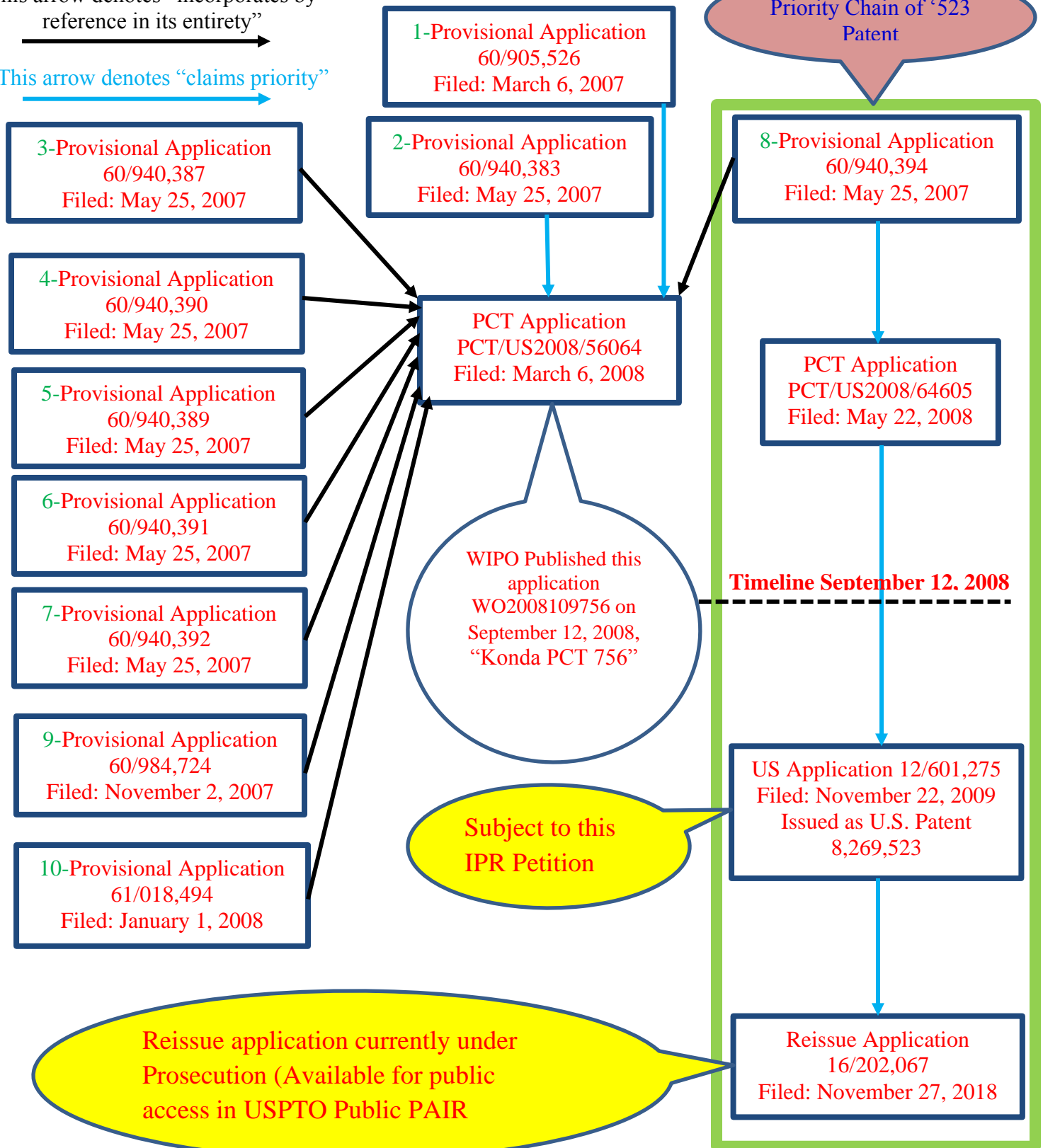
II. BACKGROUND

The '523 Patent along with several other families of patents and/or patent applications incorporated by reference in their entirety in the '523 Patent disclose layouts for integrated circuits including Field Programmable Gate Arrays ("FPGAs") comprising 2D-Mesh-like 2D layouts for multi-stage networks such as Benes Network, Butterfly Fat tree networks and various other multi-stage networks with isomorphic transformations, having 2D-layouts as simple as those of 2D-Mesh networks so that all the wires are horizontal or vertical. **This layout is based on alternate vertical and horizontal wires** and replicability of the partial multi-stage network corresponding to each computational block of an FPGA regardless of the size of the FPGA.

The complete families of patents and/or patent applications incorporated by reference in their entirety in the '523 Patent is illustrated in the priority chain below:

This arrow denotes "incorporates by reference in its entirety"

This arrow denotes "claims priority"



A. The '523 Patent

Petitioner seeks *inter partes* review of claims 1, 15-18, 20-22, 32 and 47 of the '523 Patent. The '523 Patent (Ex. 1001) issued from patent application No. 12/601,275 ("the '275 application", (Ex. 1004) filed on November 22, 2009. (The '523 Patent has only one independent claim i.e., Claim 1. The '523 Patent is a national stage application of international application PCT Application No. PCT/US2008/064605 ("the '605 PCT application"), (Ex. 1007), filed May 22, 2008 which in turn is a continuation-in-part and claims priority to the U.S. Provisional Patent Application Serial No. 60/940,394, filed May 25, 2007 ("the '394 provisional application", Ex. 1026). No new subject matter was added to the specification of the '275 application which issued as the '523 Patent. Thus, the effective filing date of the '523 Patent is the earliest application for which priority was claimed, namely, May 25, 2007.

B. US Application No. 16/202,067 is a reissue application of the '523 Patent currently in prosecution

US Application No. 16/202,067 ("the '067 reissue application") filed on November 27, 2018 is a reissue application of the '523 Patent. The '523 Patent has only one independent claim, i.e., Claim 1. Since the '523 Patent was issued on September 18, 2012 and the '067 reissue application was filed on November 27, 2018 which is more than two years after the '523 Patent was issued, Claim 1 in the '067 reissue application is further narrowed. The '067 reissue application is still

under prosecution and no Office action has issued so far. The file history of the '067 reissue application is submitted as Ex. 2005. In view of the '067 reissue application, to save time and effort, Patent Owner respectfully requests the Board should deny the *inter partes* review for the '523 Patent.

III. PETITIONER PRESENTS A FLAWED DEFINITION OF A PERSON OF ORDINARY SKILL IN THE ART TO ACCOMMODATE ITS UNQUALIFIED WITNESS

Petitioner proposes that a person of ordinary skill in the art ("POSITA") at the time of the alleged invention of the '523 Patent would have had a master's degree in electrical engineering or a similar field, and at least two to three years of experience with integrated circuits and networks. Petition at 6 (Ex. 1002, ¶¶18-19.) Petitioner acknowledges that "[M]ore education can supplement practical experience and vice versa. (*Id.*)".

Petitioner's witness, Dr. Baker states "All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in designing, developing, researching, and teaching regarding circuit design and memory devices referenced in this declaration. (Ex. 1002, ¶3). Notably Petitioner's witness by his own admission has no experience in **networks**.

According to Petitioner, someone with a master's degree in electrical engineering or a similar field, and at least two to three years of experience with "circuit design and memory devices" and no specific experience or education in interconnection networks and Field Programmable Gate Arrays could be one of ordinary skill in the art. Simply having experience in circuits and memory in designing, developing, researching, and teaching regarding circuit design and memory devices, is sufficient according to Petitioner. In Petitioner's view, understanding the different types of interconnections networks and the specific interconnection networks used to build Field Programmable Gate Arrays, is not required. Patent Owner respectfully disagrees with this overly broad definition of a person skilled in the art.

"Factors that may be considered in determining level of ordinary skill in the art include: (1) the educational level of the inventor; (2) type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) educational level of active workers in the field." *Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d 1254, 1256 (Fed. Cir. 2007) (citing *Envtl. Designs, Ltd. v. Union OilCo.*, 713 F.2d 693, 696 (Fed. Cir. 1983), citing *Orthopedic Equip. Co. v. All Orthopedic Appliances, Inc.*, 707 F.2d 1376, 1381-82 (Fed. Cir. 1983). The courts have found that these factors are not exhaustive but are merely a guide to

determining the level of ordinary skill in the art. *Daiichi Sankyo Co. v. Apotex, Inc.*, 501 F.3d at 1256.

In the present case, the sole inventor, Venkat Konda, holds a Ph.D. degree in Computer Science and engineering and had experience in designing, developing, researching and teaching different types of interconnection networks, for over two decades at the time of the effective priority date of the '523 Patent. *See* Ex. 2001.

Patent Owner submits that a person of ordinary skill in the art ("POSITA") at the time of the invention of the '523 Patent would have had a master's degree in electrical engineering or a similar field, and at least two to three years of experience with integrated circuits, **interconnection** networks and **Field Programmable Gate Arrays**. More education can supplement practical experience and vice versa.

The prior art solutions for the '523 Patent include numerous interconnection networks including multi-stage networks. Furthermore, interconnection networks used in Field Programmable Gate Arrays ("FPGAs") is a separate field requiring VLSI layouts and multicast solutions. The designs for an FPGA interconnect have evolved over the years in order to address the issues of area, power, performance, and wiring requirements. And some of the key requirements for FPGA

interconnects are not known in academia unless POSITA has worked in the industry. -Furthermore innovations in this area take years to develop. For example, Dr. Konda, the sole inventor of the '523 Patent, has over two decades of experience in interconnection networks before the priority date of the '523 Patent. *See* Exhibit 2001. Here, a POSITA must have actual experience in industry or as a consultant to industry to understand the intricacies of interconnection networks as they apply to FPGAs.

In contrast, Dr. Baker, Petitioner's exemplar person of ordinary skill in the art, holds a B.S. degree, a M.S. degree, and Ph.D. degree in Electrical Engineering. Dr. Baker has a background of more than 30 years only in designing, developing, researching, and teaching regarding circuit design and memory devices. Dr. Baker also provides no indication that he has any specific experience in designing or developing interconnection networks or Field Programmable Gate Arrays, as disclosed in the '523 Patent. Dr. Baker's qualification states "I am not an attorney and offer no legal opinions, but in the course of my work, I have had experience studying and analyzing patents and patent claims from the perspective of a person skilled in the art. (Ex. 1002 ¶13)

The Curriculum Vitae of Dr. Baker (Ex. 1003) does not list a single publication, a course taught at UNLV or a granted patent either in interconnection networks or in Field Programmable Gate Arrays.

Rather, Dr. Baker simply claims that “The opinions contained in this Declaration are based on the documents I reviewed, my professional judgment, as well as my education, experience, and knowledge regarding integrated circuits, including networks and switches used to implement field-programmable gate arrays (FPGAs)” makes him “qualified to testify as an expert with respect to the interconnection networks described and claimed in the ‘523 Patent”. (Ex. 1002 ¶14). Notably missing is any experience by Dr. Baker in designing or implementing interconnection networks for FPGAs to which the subject matter of the ‘523 Patent is directed.

Along with his lack of educational background and specific experience, statements in Dr. Baker's declaration further demonstrate that Petitioner's definition of ordinary skill in the art—with Dr. Baker as Petitioner's example of such a person—is flawed. Specifically, Dr. Baker lacks a basic understanding of hypercube networks which is required for a POSITA with two to three years of experience with interconnection networks and therefore cannot possibly understand that hypercube networks with dimension zero have only one node (or

Block) and the replication for every doubling of the nodes to build hypercube networks of bigger dimensions.

Hypercube networks of different dimensions (or degrees) are well known for a POSITA. Referring to Computer Science Notes of Graduate course "Parallel Computing" for Chapter 2 - Parallel Architectures and interconnection networks, by Prof. Stewart Weiss at City University of New York (Ex. 2006, at 5), Figure 2.5 illustrates hypercube networks of dimensions 0, 1, 2, and 3. Also refer to the second and third paragraphs in Section 2.2.5 discussing the details of the hypercube networks in Figure 2.5 as

"To start, a single point can be thought of as a 0-cube. Suppose its label is 0. Now suppose that we replicate this 0-cube, putting the copy at a distance of one unit away, and connecting the original and the copy by a line segment of length 1, as shown in Figure 2.5. We will give the duplicate node the label, 1. We extend this idea one step further. We will replicate the 1-cube, putting the copy parallel to the original at a distance of one unit away in an orthogonal direction, and connect corresponding nodes in the copy to those in the original. We will use binary numbers to label the nodes, instead of decimal. The nodes in the copy will be labeled with the same labels as those of the original except for one change: the most significant bit in the original

will be changed from 0 to 1 in the copy, as shown in Figure 2.5. Now we repeat this procedure to create a 3-cube: we replicate the 2-cube, putting the copy parallel to the original at a distance of 1 unit away in the orthogonal direction, connect nodes in the copy to the corresponding nodes in the original, and relabel all nodes by adding another significant bit, 0 in the original and 1 in the copy.”

See Ex. 2006, at 5.

Clearly hypercube network of dimension 0 has only one node and no wires connected as to any other nodes as there is only one node. A POSITA with background and experience in interconnection networks specifically in hypercube networks would understand the claim 1 amendment (as will be discussed in detail later in this Preliminary Response) during the prosecution of the ‘523 Patent by the Examiner.

Furthermore the ‘523 Patent states that “Finally applicant notes that in each quadrant or half the blocks are arranged as a general binary hypercube. Recursively in larger multi-stage network $V_{fold-link}(N_1, N_2, d, s)$ where $N_1 = N_2 > 32$, the layout in this embodiment in accordance with the current invention, will be such that the super-quadrants will also be arranged in d-ary hypercube manner. (In the embodiment of the layout 100C of FIG. 1C, it is binary hypercube manner since d

= 2, in the network $V_{fold-link}(N_1, N_2, d, s)$ 100B of FIG. 1B).” (Ex. 1001, at 48, 14:1-

9). A POSITA would understand that the 2D-layouts disclosed for multi-stage networks in the ‘523 Patent are also applicable for a hypercube network topology scheme of dimension zero with only one block comprising one stage, particularly as shown in FIG. 2A3 of the ‘523 Patent (as will be discussed in detail later in this Preliminary Response). However, since Dr. Baker has no experience in interconnection networks he states that he failed to understand a topology with only one stage in the multi-stage network and the replication in either vertical or horizontal directions in random fashion for every doubling of the nodes to build hypercube networks of bigger dimensions (Ex. 1002, ¶ 132). Instead, if Dr. Baker actually understood the difference between a multi-stage network arranged in a hypercube topology of 2D-layout, it would have been clear to him. This is the first error by Dr. Baker in his declaration.

Dr. Baker states that he failed to understand that column-based layout disclosed in US Patent No. 6,940,308 (“Wong”) that the replication happens first in the column only i.e., vertically only, and then multiple columns are replicated i.e., horizontally (Ex. 1002 ¶ 134). This is Dr. Baker’s second error in his declaration. The failure of Dr. Baker to understand this distinction is understandable in light of his lack of experience in the relevant field.

It is obvious for a POSITA that the column-based layout disclosed in Wong has no commercial applicability even though Wong clearly describes “On the other hand, the weakness of this column floorplan is that the long inter-column connections for Several levels can all pass in parallel over the same area.” (Ex. 1008, at 21, 13:49-51). Dr. Baker's third error is that in column-based layout disclosed in Wong the number of cells in each column needs to be fixed beforehand otherwise column-based layout disclosed in Wong cannot be scaled up regardless of the size of the 2D-grid (Ex. 1002 ¶¶132-138). Again, Dr. Baker, as Petitioner's example of a person of ordinary skill in the art, clearly is not qualified in the correct field.

Thus, Petitioner's overly broad definition of a person of ordinary skill in the art is flawed and would lead to anticipation and obviousness conclusions that one of ordinary skill in the art relevant to the '523 Patent would never reach. Therefore, the Board should reject Petitioner's flawed definition because it disregards the level of skill relevant to the claimed subject matter of the '523 Patent.

IV. PETITIONER HAS FAILED TO SHOW THAT ANY CLAIM IS OBVIOUS OVER THE PRIOR ART

Petitioner alleges that the challenged claims should be canceled as unpatentable on the following grounds:

Ground 1: Claims 1 and 20-22 are unpatentable under pre-AIA 35 U.S.C. § 102(b) as being anticipated by *Wong*.

Ground 2: Claims 15-18, 32, and 47 are unpatentable under pre-AIA 35 U.S.C. § 103 as obvious over *Wong*.

Petitioner also alleges that during prosecution “PO and the Examiner conducted an interview, but it is unclear what was discussed as the interview summary merely reproduces the entirety of claim 1 of the ‘523 Patent. (*Id.*, 57.)” Petition at 8.

After the Claim 1 was amended, in the amendment filed on May 8, 2012 in response to the first Office action in reply to the objections raised by the Examiner, and after the interview between PO and the Examiner, the Examiner issued Notice of allowance stating in the “Allowable Subject Matter” as follows:

The following is an examiner's statement of reasons for allowance: in combination with other limitations of the claims, the cited prior arts fail to teach said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-

integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right, each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, **regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid, as required by amended claim 1.**

Ex. 1004 at 28, ¶ 1. Emphasis added.

Petitioner alleges that Wong discloses:

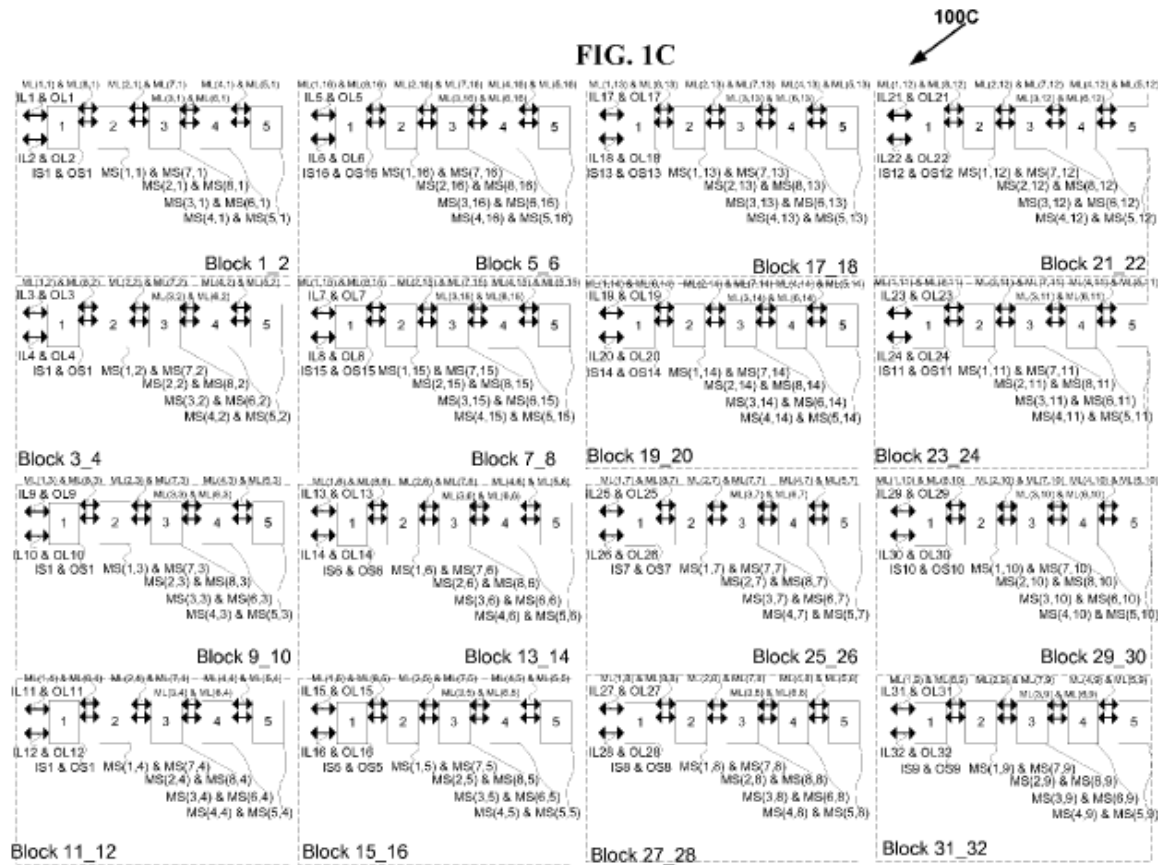
“each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid.”

The Petitioner and Dr. Bakers' arguments are flawed as explained in this section.

In a direct response to all these flawed arguments by the Petitioner, the most relevant points disclosed in the '523 Patent are described below:

- 1. The '523 Patent discloses 2D layouts of multi-stage networks with the alternative vertical and horizontal wiring in a hypercube topology layout scheme in elaborate detail and scalability from one stage to a large number of stages**

a. Illustration of the 2D-layout scalability disclosed in the '523 patent - as N is increased from 2 – 128, the blocks are increased from 1 – 64, and the stages are increased from 1 to 7

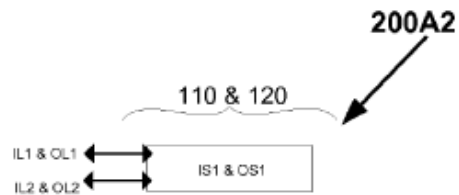
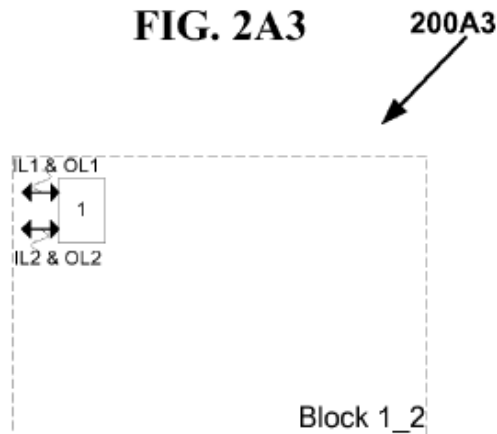


FIGs. 1C - 1G disclose the 2D-layout for a multi-stage network of $N = 32$ with 16 blocks, namely, Block1_2, Block 3_4, ... Block 31_32 and each block comprising 5 stages, namely, 1, 2, 3, 4, 5. The remainder of the details of the diagrams and layouts can be found in the '523 Patent.

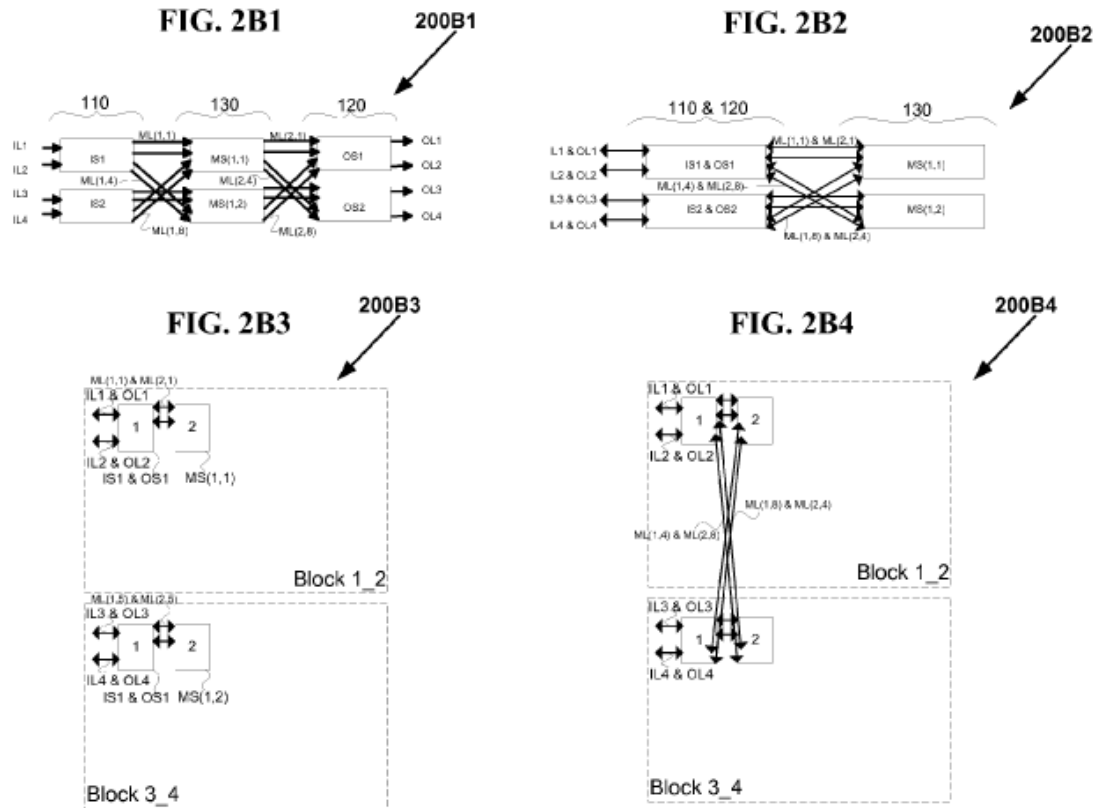


FIG. 1H discloses the 2D-layout for a multi-stage network of $N = 128$ with 64 blocks namely Block1_2, Block 3_4, ... Block 127_128 and each block comprising 7 stages namely 1, 2, 3, 4, 5, 6, 7. The '523 Patent clearly describes that for every doubling in the number blocks there will be an additional stage since the 2D-layout disclosed, for example in FIG. 1C and IH are, arranged in a binary hypercube topology. Accordingly, since N is increased from 32 to 128 which is four times, the 5 stages in FIG. 1C - 1G i.e., 1-5 are first replicated in the complete blocks starting from block 33_34 to Block 63_64 and then stage 6 is added to all

the blocks i.e., Block 1_2 to Block 63_64. Then for the next doubling of the blocks, new blocks starting from Block 65_66 to Block 127_128, all the stages from 1-6 are first replicated and then stage 7 is added to all the blocks i.e., Block 1_2 to Block 127_128. And thus since N is increased from 32 to 128 which is four times, two more stages namely 6 and 7 are added to all the blocks from Block 1_2, Block 3_4, ... , Block 127_128. And this recursive replication is extended for every doubling of N. (Ex. 1001, at 49 from 15:33 – 16:12).

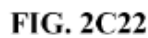
FIG. 2A1**FIG. 2A2****FIG. 2A3**

Similarly FIG. 2A3 illustrates the 2D-layout for a multi-stage network for $N = 2$ wherein there is only one block, namely, Block 1_2 comprising stage 1.

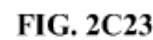


FIGS. 2B3 - 2B4 illustrate the 2D-layout for a multi-stage network for $N = 4$, and since N is doubled, blocks are doubled, and the new block is Block 3_4, so stage 1 is replicated first in Block 3_4, and then a new stage i.e., stage 2 is added for both the blocks i.e., Block 1_2 and Block 3_4.

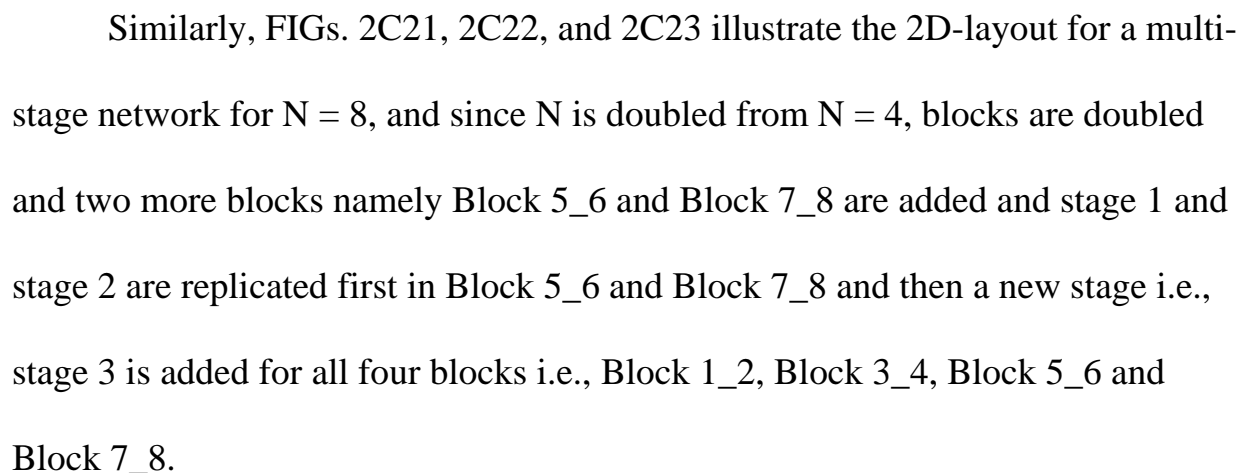
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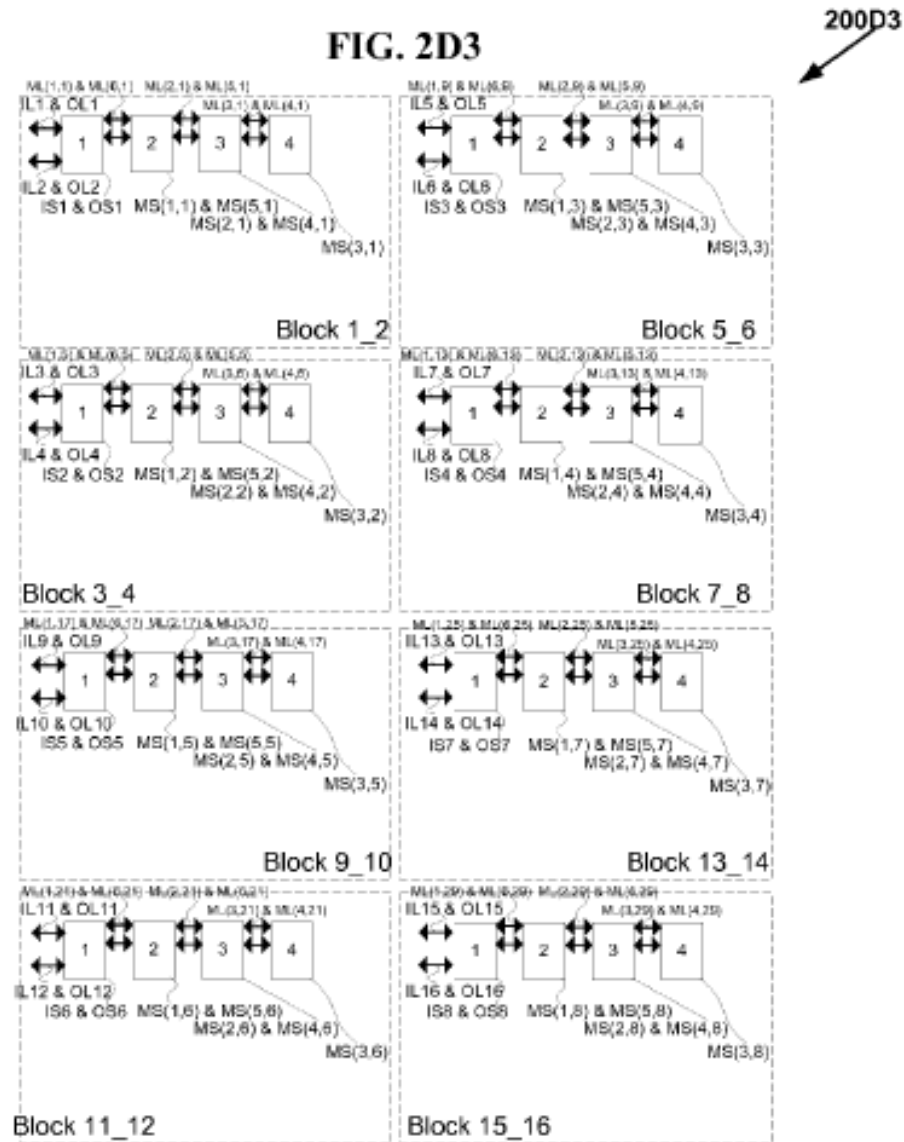


200C22



200C23





Similarly, FIGs. 2D3, 2D4, 2D5, and 2D6 illustrate the 2D-layout for a multi-stage network for $N = 16$, and since N is doubled from $N = 8$, blocks are doubled and four more blocks, namely, Block 9_10, Block 11_12, ..., Block 15_16 are added and stage 1, stage 2 and stage 3 are replicated first in Block 9_10, Block

11-12, ..., Block 15_16 and then a new stage i.e., stage 4 is added for all eight

Blocks i.e., Block 1_2, Block 3_4, ..., Block 15_16.

The foregoing diagrams in the '523 Patent clearly illustrate that as the size N is increased from 2 to 128, the block numbers are increased from Block 1_2 to Block 121_128, stage numbers are increased from 1 to 7 and for each doubling of N, block numbers are doubled by replicating the stages either vertically or horizontally and finally an additional stage is added to all the blocks. The same numbering of blocks, namely, Block 1_2, Block 3_4, etc. and the same numbering of stages, namely, 1, 2, etc. is clearly illustrated in all the layout diagrams.

Key Summary 1: More importantly stage numbers are increased starting from 1 to 7 and there is only one stage i.e. stage 1 in a block i.e., Block 1_2 in only the FIG. 2A3. So a POSITA would clearly understand there is only one stage only when there is one block. A POSITA would clearly understand that in electrical engineering terms or mathematically it is a fundamental case to describe the mathematical rigor or boundary conditions.

Petitioner understands this point as Petitioner (footnote in the Petition 1, 11) corrects the error in the '523 Patent that the number of stages in 2B, 2C, and 2D are more than one. Therefore Petitioner clearly admits that there is only one stage when there is only one block as shown in FIG. 2A3.

b. Illustration of the key differences (and huge benefits) of the 2D-layout disclosed in the '523 patent over the Column-based layout (or Column floorplan) disclosed in US Patent No. 6,940,308 ("Wong")

While continuing from the previous **Section IV.1.a**, the key differences (and huge benefits) of the 2D-layout disclosed in the '523 patent over the Column-based layout disclosed in Wong (i.e., by simultaneously describing the column-based layout in Wong) as follows:

Key Point 1: Furthermore as illustrated in the Section IV.1.a, the replication is performed either vertically or horizontally as N is increased from 1 to 128 at every doubling of N. And then an additional stage is added to all the blocks.

In contrast, in the column-based layout in Wong, the replication happens first in the column only i.e., vertically only, and then multiple columns are replicated i.e., horizontally.

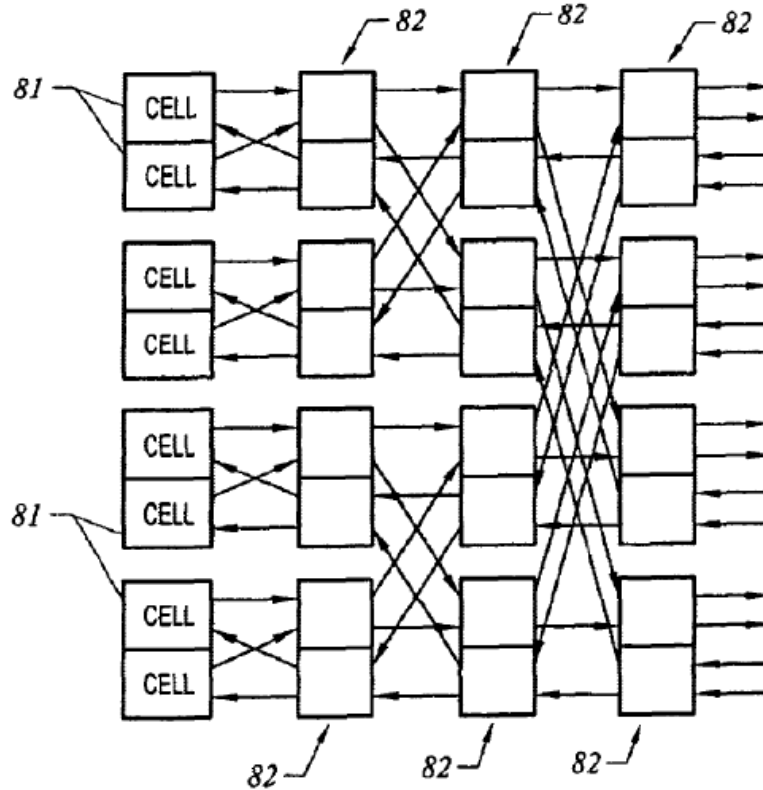


FIG. 13A

This can be easily seen from FIG. 13A and FIG. 13B of Wong. As described in Wong “See FIG. 13B in which a level of Switch cells 83 are added to make the connection between two FIG. 13A column arrays. For each additional doubling of the number of cell columns, an additional column of Switch cells must be added to each of the cell columns” (Ex. 1008, at 21, 13:36-40).

Observe the column in FIG. 13A is consistent with the butterfly pattern of a Benes network as described in Wong “See FIG. 13A. There are two logic cells 81 per Switch cell 82, connected in the so called “butterfly” pattern, consistent with the Benes network topology:” (Ex. 1008, at 21, 13:22-24). So it is clear that to be

consistent with the butterfly pattern, **the doubling in Wong happens first in the columns only.** The size of each column can be any power of two as described in Wong “The strength of this column floorplan is that the number of cells in a column can be any power of 2,” (Ex. 1008, at 21, 13:44-45).

However, once the number of cells in a column (any power of 2) is fixed, then the layout grows in a multiple of columns as described in Wong “For multiple column arrays, levels of Switch cells are added to each column’s Sub-network. The new levels are connected together between columns in a topology consistent with a Benes network.” (Ex. 1008, at 21, 13:33-36).

So in the column-based layout disclosed in Wong “The strength of this column floorplan is that the number of cells in a column can be any power of 2, and the number of rows can also independently be any power of 2.” (Ex. 1008, at 21, 13:44-46), even though the number of cells in a column is fixed (to a power of 2), the number of columns is also fixed for the desired size of Benes network.

So in the column-based layout disclosed in Wong, first the decision of the number of cells in a column is made and the replication of the Benes Network by doubling happens in the first column. Then multiple columns are replicated horizontally.

So this is a severe limitation in Wong, whereas in the ‘523 Patent vertical and horizontal replications are performed in any random fashion (including

alternate vertical and horizontal wiring) at every doubling of N. This is disclosed in the '523 patent for example "It must be noted that all the inter-block links are vertical tracks in this layout. (Alternatively all the inter-blocks can also be implemented as horizontal tracks)." (Ex. 1001, at 50 from 17:16-18).

This is key advantage of the 2D-layout disclosed in the '523 patent over the column-based layout in Wong.

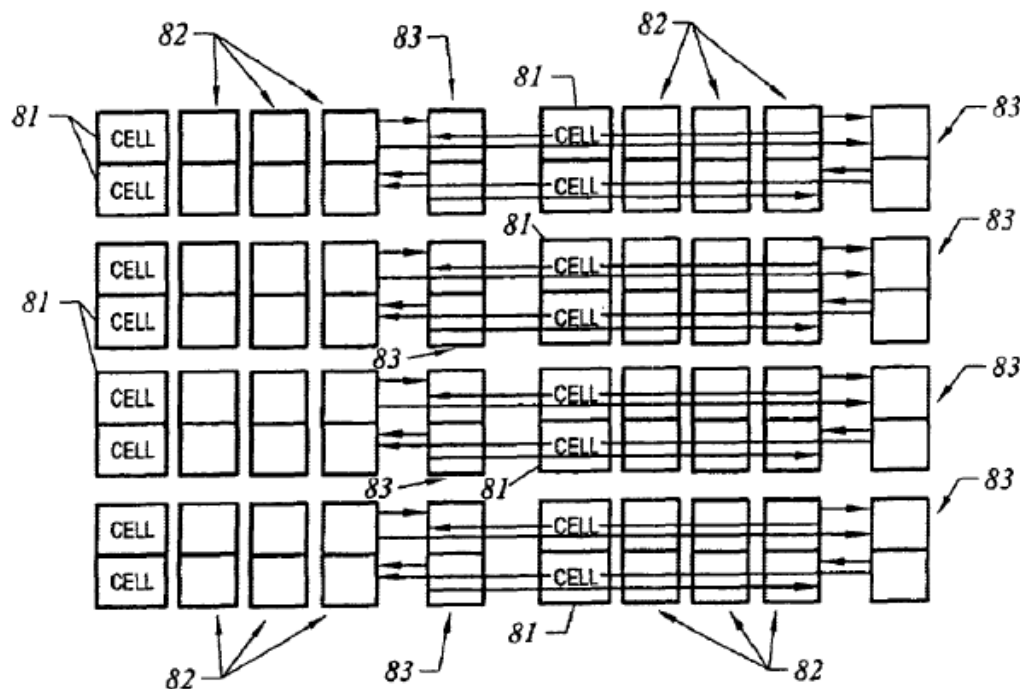


FIG. 13B

Key Point 2: Another key point illustrated in the Section IV.1.a, as disclosed in the 2D-layouts of the '523 Patent, the size of N can be increased to any size without limit on the fly that is no need to know the size of N beforehand.

In contrast, in the column-based layout in Wong, the number of rows and number of columns of the 2D-grid must be known beforehand so that the number of cells in a column (of any power of 2) is decided. Based on the number of cells decided, the number of columns is automatically fixed for a given size of Benes Network. Even if the number of columns is made of any size there is no flexibility to increase the number of cells in a column once the decision is made. So in the column-based layout in Wong, the size of the 2D-grid cannot be increased without limit without fixing the number of rows and number of columns in the column-based layout disclosed in Wong, which is another severe limitation in Wong.

To reemphasize as illustrated in the Section IV.1.a, as disclosed in the 2D-layouts of the '523 Patent, the number of rows and number of columns can be decided on the fly without knowing the size of the Benes Network beforehand.

The above **two Key Points 1) and 2)** are the key differences in the '523 Patent with huge benefits compared to Wong.

And the subject matter of The above **two Key Points 1) and 2)** are added to the Claim 1 in the amendment filed on May 8, 2012 in response to the first Office action in reply to the objections raised by the Examiner, to overcome Wong as follows:

each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of

the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid.

Huge Disadvantage of Column-based layout in Wong: Another huge

disadvantage in the column-based layout described Wong “On the other hand, the weakness of this column floorplan is that the long inter-column connections for Several levels can all pass in parallel over the same area.” (Ex. 1008, at 21, 13:49-51). **This is the key reason for the column-based layout to be impractical for commercial use in FPGAs and never used in a product.**

It is very clear that the 2D-layout with the alternative vertical and horizontal wiring in a hypercube topology layout scheme disclosed in the ‘523 Patent solves this limitation and is a huge breakthrough for Benes networks (including other multi-stage networks) commercial FPGA products.

2. Complete Claim 1 as amended after first Office action to the ‘275 application on May 8, 2012

First Complete Claim 1 as amended after first Office action to the ‘275 application on May 8, 2012 is listed as follows:

Claim 1: An integrated circuit device comprising a plurality of sub-integrated circuit blocks and a routing network, and

Said each plurality of sub-integrated circuit blocks comprising a plurality of inlet links and a plurality of outlet links; and

~~*Said routing network interconnects any one of said outlet link of one of said sub-integrated circuit block to one or more said inlet links of one or more of said sub-integrated circuit blocks; and*~~

Said routing network comprising of a plurality of stages y , in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y , where $y \geq 1$; and

Said routing network comprising a plurality of switches of size $d \times d$, where $d \geq 2$, in each said stage and each said switch of size $d \times d$ having d inlet links and d outlet links; and

~~*Said each sub-integrated circuit block comprising a plurality of said switches corresponding to each said stage; and*~~

Said plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated

circuit block are directly connected from said outlet links of said switches of its
corresponding said lowest stage of 1; and

*Said each sub-integrated circuit block comprising a plurality of
forward connecting links connecting from switches in a lower stage to switches in
~~the~~ its immediate succeeding higher stage, and also comprising a plurality of
backward connecting links connecting from switches in a higher stage to switches
in ~~the~~ its immediate preceding lower stage; and*

*Said each sub-integrated circuit block comprising a plurality straight links
in said forward connecting links from switches in said each lower stage to switches
in ~~the~~ its immediate succeeding higher stage and a plurality cross links in said
forward connecting links from switches in said each lower stage to switches in ~~the~~
its immediate succeeding higher stage, and further comprising a plurality of
straight links in said backward connecting links from switches in said each higher
stage to switches in ~~the~~ its immediate preceding lower stage and a plurality of
cross links in said backward connecting links from switches in said each higher
stage to switches in ~~the~~ its immediate preceding lower stage,*

said plurality of sub-integrated circuit blocks arranged in a two-dimensional
grid of rows and columns, and

said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right,

each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid.

The amendment further narrows the claim 1 as follows:

~~1) Said routing network interconnects any one of said outlet link of one of said sub-integrated circuit block to one or more said inlet links of one or more of said sub-integrated circuit blocks; and~~

The above element is replaced with the following element which narrows the Claim 1. Specifically the outlet links are directly connected only to the inlet links

of the lowest stage 1 and the inlet links are directly connected only to the outlet

links of the lowest stage 1, both narrowing the element.

Said plurality of outlet links of said each sub-integrated circuit block are directly connected to said inlet links of said switches of its corresponding said lowest stage of 1, and said plurality of inlet links of said each sub-integrated circuit block are directly connected from said outlet links of said switches of its corresponding said lowest stage of 1; and

2) Said routing network comprising of a plurality of stages y , in each said sub-integrated circuit block, starting from the lowest stage of 1 to the highest stage of y , where $y \geq 1$; and

The recited language “in each said sub-integrated circuit block” narrows the above element further. The above language does not say if the lowest stage and the highest stage are either the same or different. That means the lowest stage is the same as the highest stage, or alternatively the lowest stage and highest stage are different. So in the case of lowest stage is the same as highest stage there is only one stage. So Petitioner admits that a POSITA understands the case of lowest stage and highest stage being the same stage.

As described in **Section IV.1.a (and also summarized as Key Summary 1 in the same Section)**, it is clear to a POSITA that there is only one stage in the 2D-layout of a multi-stage network disclosed in the '523 Patent when there is only one block in the network with $N = 2$ as illustrated in FIG. 2A3.

(Please also refer to Patent Owner's clarifications below to the amendments made to each of pending claims 8, 12, 25, 29, 40, and 44, which eventually issued as claims 7, 11, 24, 28, 39, and 43 of the '523 Patent, respectively, which makes it crystal clear that when $y = 1$, there is only one block having only one stage and in such case there are no horizontal shuffle exchange links and there are no vertical shuffle exchange links and accordingly there are no cross links when $y = 1$ which reinforces to a POSITA the understanding of Claim 1 explained here.)

~~3) Said each sub-integrated circuit block comprising a plurality of said switches corresponding to each said stage; and~~

This amendment has no effect.

~~4) said plurality of sub-integrated circuit blocks arranged in a two-dimensional grid of rows and columns, and~~

This element is removed from Claim 3 and merged with Claim 1, further narrowing the Claim 1.

- 5) said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right,

This element is removed from Claim 2 completely and merged with Claim 1, further narrowing the Claim 1.

- 6) each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid.

This element is newly added to Claim 1. This element which is essentially the combination of **Key point 1** and **Key Point 2** discussed in detail in the Section **IV.1.b** are added to the claim 1 in the amendment filed on May 8, 2012 in response

to the first Office action in reply to the objections raised by the Examiner to overcome Wong. So thus Petitioner's argument is flawed and Claim 1 is not anticipated by Wong.

The amendment to Claim 8 makes it clear for a POSITA, when $y = 1$ in Claim 2. First, Claim 8 as amended is as follows:

Claim 8: *The integrated circuit device of claim 7, wherein $y \geq (\log_2 N)$, where $N > 1$, so that the length of the horizontal shuffle exchange links in the highest stage is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks and the length of the vertical shuffle exchange links in the highest stage is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks.*

The amendment $N > 1$ means $N = 2$ or more. When $N = 2$, $y \geq (\log_2 N)$ becomes $y \geq (\log_2 2)$ i.e., $y \geq 1$. And when $y = 1$, it means there is only one stage. As disclosed in FIG. 2B3, when there is only one stage there is only one block, namely, Block 1_2. So the horizontal size of said two dimensional grid of sub-integrated circuit blocks is zero and the vertical size of said two dimensional grid of sub-integrated circuit blocks is also zero. It follows that half of the horizontal size of said two dimensional grid of sub-integrated circuit blocks is zero and half

of the vertical size of said two dimensional grid of sub-integrated circuit blocks is also zero.

FIG. 2A1



FIG. 2A2

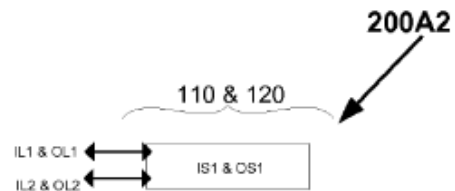
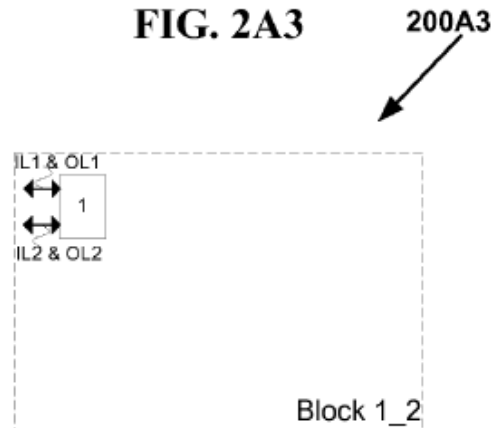


FIG. 2A3



Accordingly, Claim 8 teaches a POSITA that when $y = 1$, the length of the horizontal shuffle exchange links in the highest stage (**clearly since there is only one stage in one block, the lowest stage and highest stage are the same**) is equal to half the size of the horizontal size of said two dimensional grid of sub-integrated circuit blocks (**and since the size of horizontal shuffle exchange links is zero, there are no horizontal shuffle exchange links**) and the length of the vertical

shuffle exchange links in the highest stage (**clearly since there is only one stage in one block, the lowest stage and highest stage are the same**) is equal to half the size of the vertical size of said two dimensional grid of sub-integrated circuit blocks (**and since the size of vertical shuffle exchange links is zero, there are no vertical shuffle exchange links**).

So the amendment to Claim 8 in fact further clarifies that when $y = 1$, there is only one block having only one stage and in such case there are no horizontal shuffle exchange links and there are no vertical shuffle exchange links and accordingly there are no cross links when $y = 1$ which reinforces for a POSITA the understanding of Claim 1.

Just like for Claim 8, a similar amendment was made to each of pending claims 12, 25, 29, 40, and 44, which eventually issued as claims 11, 24, 28, 39, and 43 of the '523 Patent, respectively. Therefore, Patent Owner was consistent in amending the claims to encompass example embodiments where $y=1$ and there is only a single stage in each sub-integrated circuit block in the network. And just as Patent Owner has provided a clear explanation for Claim 8, for each of pending claims 12, 25, 29, 40, and 44, which eventually issued as claims 11, 24, 28, 39, and 43 of the '523 Patent, respectively, the same argument makes it clear to a POSITA. Specifically, the amendment to each of pending claims 12, 25, 29, 40, and 44, which eventually issued as claims 11, 24, 28, 39, and 43 of the '523 Patent,

respectively, clarifies that when $y = 1$, there is only one block having only one stage and in such case there are no horizontal shuffle exchange links and there are no vertical shuffle exchange links and accordingly there are no cross links when $y = 1$ which reinforces for a POSITA the understanding of Claim 1.

Also since Claim 1 is the only independent claim in the '523 patent, since Petitioner's arguments are flawed as described in the foregoing discussion, the Petitioner's arguments for all dependent claims on Claim 1, namely the remaining Challenged Claims 15-18, 20-22, 32, and 47 are also flawed.

In summary, since Petitioner failed to show that any claim is anticipated by Wong or obvious over Wong, the Board should not institute the *inter partes* review for any of the Challenged Claims of the '523 Patent.

V. THE BOARD SHOULD EXERCISE ITS DISCRETION TO DENY INSTITUTION OF *INTER PARTES* REVIEW

A. The Board should deny the Petition because the same prior art or arguments were previously considered by the Office

The Board should exercise its discretion to deny institution of the *inter partes* review of the Challenged Claims of the '523 Patent under 35 U.S.C. § 325(d). The prior art relied on by Petitioner was previously considered and distinguished during prosecution of the application for the '523 Patent, and the

arguments presented by Petitioner add nothing new from what was already known and considered by the Examiner during prosecution of that application.

The Board considers several factors when evaluating whether to exercise its discretion under Section 325(d), including (a) the similarities and material differences between the asserted art and the prior art involved during examination; (b) the cumulative nature of the asserted art and the prior art evaluated during examination; (c) the extent to which the asserted art was evaluated during examination, including whether the prior art was the basis for rejection; (d) the extent of the overlap between the arguments made during examination and the manner in which Petitioner relies on the prior art or Patent Owner distinguishes the prior art; (e) whether Petitioner has pointed out sufficiently how the Examiner erred in its evaluation of the asserted prior art; and (f) the extent to which additional evidence and facts presented in the Petition warrant reconsideration of the prior art or arguments. *Becton, Dickinson and Co. v. B. Braun Melsungen AG*, IPR2017-01586, slip op. at 17–18 (Paper 8) (PTAB Dec. 15, 2017) (informative). In this case, all of the *Becton Dickinson* factors weigh in favor of denying institution. Patent Owner follows the same procedure to address these factors as in *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (Feb. 13, 2020) (*precedential*)

First, the Examiner during prosecution of the '523 Patent stated "the Claims 1-8, 12, 16-25, 29, 33, 40, 44, and 48-49 are rejected under 35 U.S.C. 102(b) as being anticipated by Wong (U. S. PAT. 6,940,308)" (Ex. 1004, at 92). Complete details of reasons for the rejections are found at (Ex. 1004, at 92- 99). The Examiner during prosecution of the '523 Patent also stated "Claims 9-11, 13-15, 26-28, 30-32, 34-39, 41-43, and 45-47 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wong in view of Wu et al. (US. PAT. 7,154,887), hereinafter Wu." (Ex. 1004, at 99). Complete details of reasons for the rejections are found at (Ex. 1004, at 99-117).

Notably, all the claims 1 – 49 were rejected by the Examiner during the prosecution of the application for the '523 Patent either as being anticipated or obvious over Wong. As such, Wong was fully considered and distinguished during prosecution of the application for the '523 Patent. Nonetheless, Petitioner asserts that there are significant differences between the prior art asserted in this Petition and the prior art evaluated during prosecution because "PO and the Examiner conducted an interview, but it is unclear what was discussed as the interview summary merely reproduces the entirety of claim 1 of the '523 Patent. (*Id.*, 57.)" Petition at 8.

Petitioner further asserts “That is because, as noted above in Section I, the Examiner simply erred in allowing the application after the applicant added limitations via amendment. This is not a situation where the Examiner made certain arguments regarding a claim limitation, showing how prior art was being mapped to (or not mapped to) the limitation. Rather, the Examiner apparently did not recognize the relevance of portions of the *Wong* reference with respect to the limitations that the applicant added (e.g., the portions of *Wong* discussed above in Sections IX.A.1(j)-(k)), where Petitioner has clearly mapped *Wong* to limitations 1(j) and 1(k)). Moreover, the present Petition is supported by expert testimony that was not before the Examiner. (*See generally* Ex. 1002.)” Petition at 105-106.

However the 2D-layouts of multi-stage networks claimed in the ‘523 Patent differ and are vastly superior from *Wong* as was elaborately disclosed in the **Section IV.1.b discussed above.** (Please refer to both **Section IV.1.a** and **Section IV.1.b**)

Accordingly there are no differences between the prior art asserted in this Petition and the prior art evaluated during prosecution, because *Wong* fully discloses all of the supposed prior art asserted in this Petition. Indeed, during the prosecution, the Examiner relied completely on *Wong*, which is what Petitioner

asserts, and therefore Petitioner asserts nothing new that the Examiner did not consider.

Second, there is no cumulative prior art because Wong was fully evaluated and distinguished during prosecution of the application for the '523 Patent. Wong is the only prior art Petitioner is asserting.

Third, Wong was fully evaluated and distinguished during the prosecution of the application for the '523 Patent. Furthermore the subject matter being relied upon for this Petition was fully disclosed in Wong and evaluated by the Examiner during prosecution of the application for the '523 Patent.

Fourth, during prosecution of the application for the '523 Patent, the Examiner found that “regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid” overcame Wong.

Petitioner asserts that “But the manner in which Petitioner relies on Wong has minimal or no overlap with the arguments made during the examination of the '275 application.” (Petition at 105.) This is just not true. The Examiner identified exactly the same argument based on Wong that that Petitioner is asserting.

After the Claim 1 was amended as follows: (which the Examiner stated in the "Allowable Subject Matter":

The following is an examiner's statement of reasons for allowance: in combination with other limitations of the claims, the cited prior arts fail to teach said all straight links are connecting from switches in each said sub-integrated circuit block are connecting to switches in the same said sub-integrated circuit block; and said all cross links are connecting as either vertical or horizontal links between switches in two different said sub-integrated circuit blocks which are either placed vertically above or below, or placed horizontally to the left or to the right, each said plurality of sub-integrated circuit blocks comprising same number of said stages and said switches in each said stage, **regardless of the size of said two-dimensional grid so that each said plurality of sub-integrated circuit block with its corresponding said stages and said switches in each stage is replicable in both vertical direction or horizontal direction of said two-dimensional grid, as required by amended claim 1.**

Ex. 1004 at 28, ¶ 1. Emphasis added.

Specifically, only after the above elements were added to Claim 1, the Examiner found all the claims are allowable over Wong and the other prior art.

Fifth, Petitioner has failed to point out sufficiently how the Examiner erred in his evaluation of the asserted prior art. Rather, Petitioner has made erroneous arguments.

Sixth, Petitioner provides no additional evidence and facts in this Petition as grounds to warrants reconsideration of the prior art or arguments.

Wong was evaluated and distinguished during prosecution of the application for the '523 Patent and the subject matter being relied upon for this Petition was fully disclosed in Wong and evaluated by the Examiner. Petitioner provides nothing new from what was already known and considered by the Examiner during prosecution. Therefore, the Board should exercise its discretion and deny institution as to all the Challenged Claims.

B. Petitioner failed to address known evidence of secondary considerations

The Board has repeatedly “cautioned Petitioners in prior proceedings that petitions may be denied if they do not address known evidence of secondary considerations.” *Stryker Corp v. KFX Medical, LLC*, IPR2019-00817 (PTAB Sep. 16, 2019) (Paper 10) (citing cases). However, despite being well aware of the objective evidence of non-obviousness, including the longstanding need, unsuccessful attempts of others, and the commercial success of Patent Owner's 2D-layout of multi-stage networks disclosed in the '523 Patent (including the

Petitioner itself), Petitioner has failed to address a single one of these factors in its Petition. Indeed, Petitioner has publicly acknowledged the commercial benefit of 2D-layouts of multi-stage networks disclosed in the '523 Patent as described in this section.

The copious objective evidence of non-obviousness in this case weighs against any potential finding of obviousness. *See Transocean Offshore Deepwater Drilling, Inc. v. Maersk Drilling USA, Inc.*, 699 F.3d 1340, 1349 (Fed. Cir. 2012) (“evidence of secondary considerations may often be the most probative and cogent evidence in the record.”); *Graham v. John Deere Co.*, 383 U.S. 1 (1966). Here, there was a long-felt and unsolved need for an alternate vertical and horizontal wire based layout for multi-stage networks. Patent Owner here follows the same procedure to address these factors as *Advanced Bionics, LLC v. MED-EL Elektromedizinische Geräte GmbH*, IPR2019-01469, Paper 6 (Feb. 13, 2020) (*precedential*).

Even though Benes/BFT multi-stage networks offer $O(N \cdot \log N)$ crosspoint complexity compared to 2D-Mesh Networks with $O(N^2)$ crosspoint complexity, lack of known 2D-Mesh-like 2D layouts for multi-stage networks was a long felt need and unsolved for years to implement them as an FPGA fabric. And, the lack of 2D-Mesh like layouts for Benes/BFT Multi-stage networks left FPGA manufacturers with no other choice excepting to use 2D-Mesh based fabrics for

years. However, 2D-Mesh based FPGA fabrics consume ~75% of die area, considerable power consumption and slower performance.

There have been several unsuccessful attempts to address these technical issues. However, the prior art VLSI layouts of Benes and butterfly fat tree networks require large area to implement the switches on the chip, a large number of wires, longer wires, with increased power consumption, and increased latency of the signals which effect the maximum clock speed of operation. The column-based layout disclosed in Wong is not practical for implementation of an FPGA. This is validated in 2013 Ph.D. dissertation by Co-founder of Petitioner Flex Logix, Dr. Cheng Wang ("Wang") and his Ph.D. advisor, Dr. Dejan Markovic ("Markovic"), where Wang plagiarized and brazenly claimed it as his invention. (Ex. 2004 titled "Building Efficient, Reconfigurable Hardware using Hierarchical Interconnects" awarded in 2013 by the Department of Electrical Engineering at the University of California, Los Angeles ("UCLA"), at 48-51 in the section 2.5 titled "Prior Attempts at Hierarchical FPGAs". Notably the column-based layout disclosed in Wong is not even cited in this Ph.D. dissertation which validates that the column-based layout of Wong is not commercially viable.

The 2D-layout with alternate horizontal and vertical wiring disclosed in the '523 Patent is the first breakthrough for the commercial success of multi-stage networks as FPGA fabric. This is validated in a 2011 publication by Co-founders

of Petitioner Flex Logix, Wang and Markovic who plagiarized and brazenly

claimed it as their invention. (Ex. 2002 titled “A 1.1 GOPS/mW FPGA Chip with Hierarchical Interconnect Fabric” published in the 2011 VLSI symposium on VLSI Circuits, at 1 in sections titled “Introduction” and “Hierarchical Interconnect Architecture” and at 2, Figure 2b titled “alternated x-y routing”). Notably the column-based layout disclosed in Wong is not even cited in this paper which validates that the column-based layout of Wong is not commercially relevant.

The 2D-layouts disclosed in the ‘523 Patent initiated the commercial success of multi-stage network based FPGA fabrics. Starting with the 2D-layouts disclosed in the ‘523 Patent, commercial FPGAs achieved ~2X area savings with significant power and performance improvements over 2D-Mesh based fabrics. This is validated in a 2009 DARPA Proposal by Co-founder of Petitioner Flex Logix Markovic as principal investigator and assisted by Wang. (Ex. 2003 titled “Energy-Efficient Butterfly FPGA Hardware and Programming Tools”) on various pages **1**) at 8, Figure 4: titled “Hierarchical Konda interconnect architecture” referring to the 2D-layout disclosed in the ‘523 Patent, **2**) at 9 in the section titled “Basis of confidence” in their own words as follows: “Konda network architecture is a patent-protected technology that is recognized by many semiconductor companies including Cisco, Xilinx, Altera, and LSI Logic. To demonstrate the network in hardware, UCLA team has taped out 3 chips (namely *Chip 1 (90nm, LUT-slice*

FPGA, concept demo), Chip 2 (65nm, LUT and DSP slices, small scale), and Chip 3 (45nm, DSP-slice FPGA, small scale)) and successfully implemented variants of Konda network and also variants of processor-block features,” which mentions commercial recognition by various commercial organizations and the implementation of 2D-layouts disclosed in the ‘523 Patent in 3 chips implemented at UCLA and taped out, and **3)** at 11, in the section titled “Proposed Network Architecture” and Figure 7 titled “Konda interconnect network architecture and routing tracks for $N = 8$ LUTs,” again based on the 2D-layouts disclosed in the ‘523 Patent. Petitioner’s failure to even acknowledge, let alone address, these well-known secondary considerations very well-known to Petitioner is a fatal flaw in its Petition. Accordingly, Patent Owner respectfully requests that the Board deny institution as to all the Challenged Claims of the ‘523 Patent.

VI. PETITIONER HAS FAILED TO SHOW THAT ANY CLAIM IS OBVIOUS OVER THE PRIOR ART

Petitioner in this IPR Petition brazenly attempts by **1)** using an unqualified POSITA who made many errors, **2)** falsely claiming that the only amendment made to the ‘523 Patent filed on May 8, 2012 introduced new subject matter and lacks enablement so the effective priority date of the ‘523 Patent is November 22, 2009, **3)** falsely claiming that publication of a co-pending Konda ‘756 PCT by the Patent Owner made the ‘394 provisional application public on September 12, 2008,

4) ignoring the fact that the same prior art and arguments were previously considered by the Office, 5) knowingly not addressing (rather intentionally concealing) the fact that Flex Logix's cofounders Wang and Markovic admitted in their publications, the long felt need, previous unsuccessful attempts and commercial recognition of the 2D-layouts of the '523 Patent and thus ignoring the known evidence of secondary considerations, 6) knowing that the column-based layout disclosed in Wong has no industrial applicability, 7) hiding the fact that Flex Logix' cofounders Wang and Markovic blatantly plagiarized 2D-layouts disclosed the '523 Patent since they clearly knew that the Column-based layout disclosed in Wong has severe drawbacks as an FPGA Fabric, 8) knowingly not addressing (rather intentionally concealing) the fact that Flex Logix's co-founders Wang and Markovic's plagiarization and publication of the 2D-layouts disclosed in the '523 Patent, 9) unnecessarily filing three concurrent petitions with the same false arguments does not meet its burden of demonstrating that there is a standing for *inter partes* review of the '523 Patent. For these reasons, Petitioner has failed to carry its burden of demonstrating that there is standing for *inter partes* review of the '523 Patent.

VII. CLAIM CONSTRUCTION

Since the Petition fails to establish that the '523 Patent is eligible for IPR without requiring construction of any specific claim terms, Patent Owner reserves his rights at this time to contest Petitioner's claim construction positions should an IPR be instituted. Patent Owner disagrees that the challenged claims are fundamentally IPR eligible.

VIII. CONCLUSION

For the foregoing reasons, Petitioner Flex Logix has failed to establish a reasonable likelihood of prevailing as to the Challenged Claims of the '523 Patent, and *inter partes* review of the Challenged Claims should be denied.

Date: May 6, 2020

Respectfully submitted,

/Venkat Konda/

Venkat Konda
Pro Se Counsel
6278 Grand Oak Way
San Jose, CA 95135

CERTIFICATE OF SERVICE

Pursuant to 37 C.F.R. § 42.6(e) and consent of the Petitioner, I certify that on May 6, 2020, a copy of Patent Owner's Preliminary Response under 35 U.S.C. § 313 and 37 C.F.R. § 42.107 and accompanying exhibits was served on counsel of record for Petitioner by email to PH-FlexLogix-Konda-IPR@paulhastings.com

Dated: May 6, 2020

Respectfully submitted,

/Venkat Konda/

Venkat Konda
Pro Se Counsel

CERTIFICATION OF WORD COUNT

Pursuant to 37 C.F.R. § 42.24(d), I certify that the foregoing PO Venkat Konda's Preliminary Response was prepared in Microsoft Word, is proportionally spaced, as a typeface of Times New Roman, 14 point, and contains 10,422 words, (as calculated by the word processing system to prepare this Preliminary Response).

Dated: May 6, 2020

Respectfully submitted,

/Venkat Konda/
Venkat Konda
Pro Se Counsel