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Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a
Computer System

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BACKGROUND OF THE INVENTION

Priority Data

[0001] This application claims benefit of priority to U.S. Provisional Application Serial No. 60/910,863, titled “Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System”, filed on April 10, 2007, whose inventors were Ian Harris and Drew J. Dutton.

Field of the Invention

[0002] This invention relates generally to the field of computing devices, and more specifically to sharing devices, such as non-volatile memory, which are not designed for sharing among processors in a system.

Description of the Related Art

[0003] Many hardware systems include a central processing unit (CPU), i.e., a main processor, and one or more microcontrollers for performing auxiliary functions for the system, such as initialization, management and reset functionality. Each processor or microcontroller, in a system generally has a corresponding non-volatile memory from which the processor or microcontroller reads instructions for performing boot-up, reset, management (such as power state management), or other functions, implemented in firmware. Current solutions for providing controller memory are: (1) to have a separate dedicated/private memory device for each controller/processor; (2) to integrate memory on-chip; or (3) to attempt to arbitrate for the use of an existing memory device.

[0004] However, a problem with attempting to arbitrate for the use of another device is that system performance and user experience may be degraded. Moreover, providing each processor and microcontroller with a separate non-volatile memory is expensive in both cost and time. For example, many current embedded microcontroller solutions for notebook and desktop computers use ROM (read-only memory) solutions that present challenges in time to market and flexibility. The time to market issue is due to the need to finalize the microcontroller firmware and data early enough in the design and

manufacturing process to meet the schedule needs for production. This usually represents at least a month in the time schedule of a development program. In addition, any late error found in the firmware or data means that all existing inventory is out of date and may have to be discarded.

[0005] For the above reasons, some customers or designers prefer using embedded flash or similar memory for storage, since this type of memory allows updates at production test or even in the field. However, use of embedded flash requires a very expensive manufacturing process, because the microcontroller chip integrates flash memory on the same die, and therefore requires a flash manufacturing process. It is typically 30% more expensive to manufacture a chip with this process, and thus makes the chip significantly more expensive. This expense only makes sense if offset by some other factors, e.g., cost savings or product requirements. If a customer only has one set of firmware (code) that is used and if the code never changes, and if the customer is confident that there are no errors in the code that might require an update, ROM and a standard manufacturing process may be used instead of embedded flash memory. If, on the other hand, the customer has multiple firmware codes (e.g., one per product model), then it may be cheaper to use flash. Thus, due to expense, use of embedded flash memory may only be viable if the risk of ROM is too high or if there are multiple codes, low volume or other specific business reasons.

[0006] Thus, as discussed above, current solutions are generally expensive, inflexible, cannot be guaranteed to work reliably, may have occasional errors, and/or can cause significant system performance degradation.

[0007] Other corresponding issues related to the prior art will become apparent to one skilled in the art after comparing such prior art with embodiments of the present invention as described herein.

SUMMARY OF THE INVENTION

[0008] Various embodiments are presented of a system and method for sharing devices such as non-volatile memory between processors in a computer system where one of the processors has control over operating states, e.g., power and/or execution states, of the other processors in the computer system.

[0009] In response to a system state change, such as power on reset or system reset, where a microcontroller in a system is assured of safe access to a shared device, or can prevent the system from entering a state where a processor in the system can access the shared device, the microcontroller may set control signals to cause access to the shared device to be with the microcontroller. In other words, the system may be changed to a state (a “first” state) in which the microcontroller is guaranteed the ability to access the shared device safely, e.g., without interruption or interference by the processor.

[0010] In one embodiment, the microcontroller may be situated between a system interface (and therefore, the processor in the system) and the shared device, e.g., non-volatile memory, e.g., embedded flash memory, and thus may intercept communications between the system interface and the device. The device may include or be associated with an interface whereby access to the device is facilitated or implemented, and where this interface may be configured to direct or restrict access to the device to different system components, e.g., the processor or the microcontroller. In one embodiment, the microcontroller setting control signals to cause access to the shared device to be with the microcontroller comprises the microcontroller setting the interface to the shared device interface with the microcontroller. Said another way, the microcontroller may set one or more control signals to configure or redirect the shared device interface to grant exclusive access to the device to the microcontroller.

[0011] In one embodiment, the microcontroller controls and manages power on reset (POR) for the system, and thus may respond to and/or generate signals related to power on reset or system reset (or other management signals) in a way that preempts access to the device by the main processor of the system, thereby facilitating sharing a device that otherwise could not be shared. In some embodiments, the change in system state may be invoked or indicated by a management signal, e.g., a system reset or POR signal,

generated or received by the microcontroller. It should be noted, however, that in some embodiments, control of the direction of the interface, i.e., control of which component of the system has access to the device, may be independent of the management (e.g., system reset or POR) signal. In other words, the microcontroller may control whether the shared device interface is directed to the processor of the system, or to the microcontroller, independent of the management (e.g., system reset or POR) signal.

[0012] While in the first state, i.e., the state where the microcontroller is ensured safe access to the device, or can prohibit access by the processor in the system to the shared device, and has properly configured access to the device, the microcontroller may retrieve or exchange data with the device. For example, in embodiments where the system state is dependent on or indicated by a management signal, e.g., a system reset signal, the microcontroller may receive or generate the management signal, and hold the management signal in this state, i.e., may maintain assertion of the management signal, and, while this signal is asserted, may read, write, acquire, or otherwise exchange (e.g., via invocation of a read or write by some other component of the system), data or program instructions from, to, or with, the device.

[0013] Once the controller has completed the data retrieval or exchange with the device or has determined that it may no longer be assured of safe access, the microcontroller may reconfigure the interface through control signals to enable access by the processor in the system, e.g., via a switch that controls access to the device, as will be described below in more detail. Once the microcontroller has configured the device to enable access by the processor in the system, the microcontroller may change or allow change of the system state, thereby permitting the processor in the system to access the shared device. For example, in embodiments where the system state is dependent on or indicated by a management signal, e.g., a system reset signal, the microcontroller may de-assert the management signal, thereby putting the system into a state that allows access to the shared device by the processor of the system.

[0014] Thus, using embodiments of the above-described method, the microcontroller may preempt or suspend access to the device by the processor, e.g., the main CPU, of the system, or otherwise configure safe access to the device by the microcontroller; retrieve or otherwise exchange data or program instructions with the device; then return access to

the device to the processor, or otherwise relinquish exclusive or safe access to the device by the microcontroller.

[0015] It should be noted that in various other embodiments where the microcontroller manages or controls operating states of the system (e.g., reset, POR, sleep, and other states related to specific system activities where it is known by the microcontroller that the system cannot or will not access the device), the microcontroller may monitor (or control) such system states, and take advantage of these states to access the device safely, e.g., to take control and use the shared device. Note that these system states should be such that the microcontroller either manages when the system will exit these states or is provided sufficient warning as to when the system will again need control of the shared interface (to the device). As one example, when a system is being shut down, the microcontroller may take over the device interface, i.e., may redirect the device interface to allow (only) access by the microcontroller, before power-off, i.e., before turning off the final power rail. In this way, writes or other exchanges with the shared device may be “saved up” or queued, and their completion (e.g., by the microcontroller) may be guaranteed before final power off.

[0016] Thus, the microcontroller may gracefully share access to the device with the processor of the system. It should be noted that in other embodiments, additional microcontrollers may also share the device with the host or main system CPU, using the techniques described above. In further embodiments, such sharing of devices may also be used in other ways. For example, in some embodiments, a plurality of processors (e.g., microcontrollers) may share such a device, where each processor may in turn suspend or prevent access to the device by the other processors while it accesses the device.

[0017] Below are described more specific embodiments of the above-described general method that are particularly directed to the sharing of non-volatile memory between a main processor and a microcontroller in a system. In other words, in the below embodiments, the shared device comprises a non-volatile memory device. It should be noted, however, that these embodiments are meant to be exemplary only, and are not intended to limit the type or use of the shared device to any particular form or function.

[0018] In response to a power on reset (POR), a microcontroller in a system, e.g., microcontroller, may hold a system reset signal in a reset state, thereby prohibiting a processor in the system from accessing a non-volatile memory in the system. Note that the POR and/or the system reset may or may not be invoked by the microcontroller.

[0019] In other words, in response to the POR, the microcontroller may receive or generate the system reset signal, and hold the signal in a reset state. As described above, in one embodiment, the microcontroller may be situated between the system interface (and therefore, the processor in the system) and the shared device, e.g., non-volatile memory, e.g., embedded flash memory, and thus may intercept communications between the system interface and the device, e.g., the non-volatile memory. As will be described below in more detail, in some embodiments, when the system reset signal is in the reset state, the interface to the non-volatile memory may be configured by the microcontroller to preclude the processor in the system from accessing the non-volatile memory, e.g., via a switch.

[0020] While the system reset signal (or other management signal) is held in the reset state, e.g., is asserted by the microcontroller (e.g., and the interface to the non-volatile memory is configured to only allow access by the microcontroller), the microcontroller may fetch program instructions/data from the non-volatile memory and load the program instructions/data into a memory of the microcontroller, or otherwise access the non-volatile memory. In other words, the microcontroller may generate or receive the system reset signal, and may hold the system reset signal in the reset state (e.g., on the system management bus via a system reset line), i.e., may maintain assertion of the system reset signal, and, while the system reset signal is asserted, may fetch, i.e., read, acquire, or otherwise receive (e.g., via invocation of a read by some other component of the system), program instructions/data from the non-volatile memory and load or write the program instructions/data into the microcontroller's memory. Note that the microcontroller's memory is preferably RAM (random access memory), although any type of re-writeable memory may be used as desired. As noted above, in some embodiments, the program instructions / data may include program firmware code, that may, for example, be usable by the embedded microcontroller for startup or reset functionality, e.g., for initializing the microcontroller, among other uses. In some embodiments, the microcontroller may be or

include a peripheral device controller for a computer system. For example, in one exemplary embodiment, the embedded microcontroller may be a keyboard controller, and the non-volatile memory device 108 may store keyboard controller (KBC) code, although in other embodiments, any other program instructions/code or data may be used as desired.

[0021] In one embodiment, the microcontroller may include or couple to a host memory bus, which may couple to the system interface, and may also include or couple to a device bus, in this embodiment, a non-volatile memory bus, which may couple to the shared non-volatile memory device. In one embodiment, the host memory bus and the non-volatile memory bus are SPI (serial peripheral interface) buses, although other protocols may be used as desired. Note that in some embodiments, the host memory bus and the non-volatile memory bus may be considered the same bus, e.g., a memory bus, where the microcontroller is inserted to switchably intercept and possibly redirect signals on the bus(es).

[0022] In one embodiment, the microcontroller includes or is coupled to a switch controlled by a switch control, for providing switching functionality for the host memory bus and the non-volatile memory bus, e.g., for the memory bus. The microcontroller may thus be operable to switchably preempt and inhibit signal flow on the memory bus (i.e., the host memory bus and the non-volatile memory bus) between the host interface and the non-volatile memory, e.g., by placing the switches into a high-impedance state, and to fetch instructions/data from the non-volatile memory while communication between the host interface and the non-volatile memory is suspended. Thus, the microcontroller may operate to configure the interface to the device (e.g., the switch) to regulate and enforce safe access to the device.

[0023] After the microcontroller has loaded the program instructions/data from the non-volatile memory, the microcontroller may reconfigure the access to the non-volatile memory, e.g., via the switch, and release the system reset signal from the reset state, thereby permitting the processor in the system access to the non-volatile memory. In other words, upon completion of the fetch of instructions/data from the non-volatile memory by the microcontroller, the microcontroller may terminate the suspension or preemption of communications between host interface and the non-volatile memory,

thereby allowing resumption of such communications, e.g., via switch, and de-assert the system reset signal.

[0024] Thus, using embodiments of the above-described method, the microcontroller may preempt or suspend communications with the non-volatile memory by the main CPU and read instructions/data from the non-volatile memory, e.g., to initialize the microcontroller and/or perform other functionality prior to, or independent from, operation of the main system, i.e., the main CPU, thus sharing the non-volatile memory with the main system. For example, in some embodiments, the microcontroller may, in addition to initialization code/data, may also fetch program instructions and/or data related to pre-boot security operations, and may operate to perform such pre-boot security operations prior to boot-up of the main system, thereby providing additional security to the system.

[0025] Thus, the microcontroller may gracefully share use of the main system's non-volatile memory. It should be noted that in other embodiments, additional microcontrollers may also share this non-volatile memory with the host or main system CPU, using the techniques described above. In further embodiments, such sharing of non-volatile memory may also be used in other ways. For example, in some embodiments, a plurality of microcontrollers may share a non-volatile memory (e.g., that is not used by the main system CPU), where each microcontroller may in turn suspend or prevent access to the non-volatile memory by the other microcontrollers while it loads instructions/data from the memory.

[0026] Note that in various embodiments, the system changing to a state where the microcontroller is assured safe access to the non-volatile memory (or device) may be performed or mediated by software or hardware. In other words, in some embodiments, the state change may be in response to hardware signals, such as POR signals, etc. In other embodiments, the state change may be in response to software events, tokens, software conditions, software messages, software handshakes, and so forth. Said another way, embodiments of the present invention are intended to cover virtually any case where the embedded controller can determine that it can safely take control of the shared non-volatile memory, whether the "safe" system state is mediated or signaled via software or

hardware. For example, the system may pass the microcontroller a token, which grants the microcontroller ownership of the memory through a software handshake.

[0027] Thus, various embodiments of the invention described herein may allow an embedded microcontroller and a processor in a system to share a device that is not designed to be shared.

[0028] BRIEF DESCRIPTION OF THE DRAWINGS

[0029] The foregoing, as well as other objects, features, and advantages of this invention may be more completely understood by reference to the following detailed description when read together with the accompanying drawings in which:

[0030] Figure 1A illustrates an exemplary computer system configured to implement one embodiment of the present invention;

[0031] Figure 1B is a high-level block diagram of an exemplary system configured to implement one embodiment of the present invention;

[0032] Figure 2 is a flowchart of a method for sharing a device between a processor and a microcontroller in a system, according to one embodiment;

[0033] Figure 3 is a flowchart of a method for sharing non-volatile memory between a processor and a microcontroller in a system, according to one embodiment.

[0034] Figure 4 illustrates a microcontroller, according to one embodiment of the invention; and

[0035] Figure 5 illustrates an exemplary signal timing diagram, according to one embodiment.

[0036] While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof are shown by way of example in the drawings and will herein be described in detail. It should be understood, however, that the drawings and detailed description thereto are not intended to limit the invention to the particular form disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the present invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Incorporation by Reference

[0037] The following references are hereby incorporated by reference in their entirety as though fully and completely set forth herein:

[0038] U.S. Provisional Application Serial No. 60/910,863, titled “Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System”, filed on April 10, 2007, whose inventors were Ian Harris and Drew J. Dutton.

[0039] Various embodiments of a system and method are presented for sharing devices between processors, e.g., between a one or more main processors and a microcontroller, in a system, e.g., a computer system, where the microcontroller has control over the power or execution states of the main processor(s) or other unique management capabilities relative to the other processors in the system.

[0040] Note that any headings used are for organizational purposes only and are not meant to be used to limit or interpret the description or claims. Furthermore, it should be noted that the word “may” is used throughout this application in a permissive sense (i.e., having the potential to, being able to), not a mandatory sense (i.e., must).” The term “include”, and derivations thereof, mean “including, but not limited to”. The term “coupled” means “directly or indirectly connected”.

[0041] Moreover, as used herein, a “set of instructions” may refer to one or more instructions. More specifically, in some embodiments, “instructions” may refer to programming code, software, and/or functions implemented in the form of a code that is executable by a controller, microprocessor, and/or custom logic circuit adapted to execute these instructions. In some embodiments, these instructions may comprise device drivers, control software, and/or machine code.

[0042] As used herein, a “controller” refers to any type of processor, such as a central processing unit (CPU), microprocessor, microcontroller, or embedded controller or microcontroller, among others.

Overview

[0043] Various embodiments of the invention described herein may provide access by an embedded microcontroller to a device (e.g., non-volatile memory) which allows the microcontroller to access and read or write program instructions / data (meaning program instructions and/or data) from or to the device while holding the system, e.g., the CPU, in a state such as reset where access to the non-volatile memory device will not disrupt the normal system function.

Figure 1A – Exemplary Computer System

[0014] Figure 1 is a high-level block diagram of an exemplary computer system 82 configured to implement some embodiments of the present invention. The system of Figure 1 comprises a computer system, e.g., a personal computer (PC), although in other embodiments, the techniques and systems described herein may be implemented in any other systems as desired.

[0015] In preferred embodiments, the computer system 82 includes a main or central processor, i.e., a host processor, as well as one or more microcontrollers, e.g., each in a respective system-on-chip (SoC), such as, for example, a keyboard controller for managing or controlling communications between a keyboard and the main processor. The memory is preferably included on the SoC with the embedded controller, and in various embodiments, may be a non-volatile memory, e.g., ROM (read only memory), or a volatile memory, such as Flash memory, as desired. As Figure 1 shows, the computer system 82 includes logic 104 for sharing memory, e.g., between the main processor and the microcontroller, according to embodiments of the present invention. Further details regarding exemplary embodiments of the system are provided below with reference to Figures 1B, 2, 4, and 6.

Figure 1B – Exemplary System

[0044] Figure 1B is a high-level block diagram of an exemplary system configured to implement one embodiment of the present invention, specifically to share a device, e.g., non-volatile memory, between a CPU or main processor, and an embedded microcontroller in the system. The system of Figure 1B preferably resides in a computer system, e.g., a personal computer (PC) such as computer system 82 of Figure 1A,

although in other embodiments, the techniques and systems described herein may be implemented in any other systems as desired.

[0045] As Figure 1B shows, the system may include an embedded microcontroller 102, coupled to system interface 106 via a system interface bus 103, whereby the microcontroller 102 may communicate with the CPU of the computer system, referred to as the host CPU or processor. Note that in various embodiments, this system interface 106 may simply be a connection or bus suitable for communications between the microcontroller 102 and the host CPU, or may include additional structure or functionality as desired. As indicated in Figure 1B, the microcontroller 102 may be further coupled to a shared device 108 that may store program instructions or other data that may be uploaded or programmed by the embedded microcontroller, e.g., for startup, general, or reset functionality, via a device bus 107, as shown. The microcontroller 102 may be further coupled to the system interface 106 via a host memory bus 105, whereby the embedded microcontroller 102 may intercept memory requests or other signals transmitted between the system interface (e.g., the host CPU) and the shared device 108. Note that the program instructions/data stored in the shared device (e.g., non-volatile memory) 108 preferably includes program instructions, e.g., firmware code, that may, for example, be usable by the embedded microcontroller 102 for startup, general, or reset functionality, e.g., for initializing the microcontroller 102, among other uses. In some embodiments, the microcontroller 102 may comprise a peripheral device controller for a computer system. For example, in one exemplary embodiment, the embedded microcontroller 102 is a keyboard controller, and the shared device 108 may store keyboard controller (KBC) code, although in other embodiments, any other program instructions, data or code may be used as desired.

[0046] Thus, in the embodiment shown in Figure 1B, the embedded microcontroller 102 is situated between the system interface 106 and the shared device (e.g., non-volatile memory) 108, and so may function as an intermediary or intercept between these two components, thereby facilitating sharing the device 108 between the host processor and the embedded microcontroller 102, as will be described below in more detail. Note that in this embodiment, a system management bus, e.g., a system reset bus, 101 coupling the system interface 106 and the microcontroller 102 may be included for communicating a

reset or other management signal (or other signal) between the two components, although in other embodiments, the system interface bus 103 may be used. In preferred embodiments, the shared device 108 is an embedded flash memory, although other types of devices may be used as desired, e.g., ROM or any other type of memory.

Figure 2 –Method for Sharing a Device Between Processors in a System

[0047] Figure 2 is a high-level flowchart of embodiments of a method for sharing a device, e.g., non-volatile memory, between processors, e.g., between a processor and a microcontroller in a system, e.g., a computer system, where the shared device is not designed to be shared. In various embodiments, some of the method elements shown may be performed concurrently, in a different order than shown, or may be omitted. Additional method elements may also be performed as desired. As shown, this method may operate as follows.

[0048] In 202, in response to a system state change, such as, for example, power on reset (POR), system reset, or sleep mode, where a microcontroller, e.g., microcontroller 102, in a system is assured of safe access to a shared device, or can prevent the system from entering a state where a processor in the system can access the shared device, the microcontroller may set control signals or utilize software to cause access to the shared device to be with the microcontroller. In other words, when the system is changed to a state, e.g., a first state, in which the microcontroller 102 is guaranteed the ability to access the shared device safely, e.g., without interruption or interference by the processor, the microcontroller may hold the system in the state and switch access to the shared device, e.g., the non-volatile memory, from the processor to the microcontroller. Examples of this first state may include one or more of: a power on reset (POR) state, a system reset state, or a sleep state, among others. Holding the system in this first state may prohibit the processor in the system from accessing the shared device, e.g., non-volatile memory in the system.

[0049] Similarly, the state change may be invoked or caused by a management signal, such as a POR, system reset, sleep, signal, etc., which may include a software signal,

event, token, handshake, etc. In one embodiment, holding the system in the first state may include holding a management signal in a corresponding state, e.g., holding a system reset signal in a reset state.

[0050] Note that the management signal, e.g., the POR and/or the system reset, and/or any other type of management signal used, may or may not be invoked by the microcontroller. Thus, for example, in response to a received management signal, e.g., POR signal, or in response to generating the management signal, e.g., the POR signal, the microcontroller may generate or receive another management signal, e.g., the system reset signal, then hold or assert the other management signal in a specified state, e.g., a reset state.

[0051] As noted above with reference to Figure 1B, in one embodiment, the microcontroller 102 may be situated between the system interface 106 (and therefore, the processor in the system) and the shared device 108, e.g., non-volatile memory, e.g., embedded flash memory, and thus may intercept communications between the system interface and the device 108.

[0052] The device 108 may include or be associated with an interface whereby access to the device is facilitated or implemented, and where this interface may be configured to direct or restrict access to the device to different system components, e.g., the processor or the microcontroller. In one embodiment, the microcontroller setting control signals to cause access to the shared device to be with the microcontroller comprises the microcontroller setting the interface to the shared device interface with the microcontroller. Said another way, the microcontroller may set one or more control signals to configure or redirect the shared device interface to grant exclusive access to the device to the microcontroller. In other embodiments, the switching of access to the shared device from the processor to the microcontroller may be performed via software, or a combination of software and hardware. Note that as used herein, the term “signal” may denote a hardware signal and/or a software signal, e.g., a software event, message, token, handshake, etc. Thus, the term “management signal” may refer to a hardware signal or a software signal.

[0053] Note that in a preferred embodiment, the microcontroller controls and manages power on reset (POR) for the system, and thus may respond to and/or generate signals or

software events or messages related to power on reset or system reset (or other management signals) in a way that preempts access to the device by the main processor of the system, thereby facilitating sharing a device that otherwise could not be shared. In some embodiments, the change in system state may be invoked or indicated by a management signal, e.g., a system reset or POR signal, generated or received by the microcontroller. It should be noted, however, that in some embodiments, control of the direction of the interface, i.e., control of which component of the system has access to the device, may be independent of the management (e.g., system reset or POR) signal. In other words, the microcontroller may control whether the shared device interface is directed to the processor of the system, or to the microcontroller, independent of the management (e.g., system reset or POR) signal. Moreover, in some embodiments, instead of, or in addition to, hardware signals, the microcontroller may respond to software events, messages, tokens, handshakes, etc., that may indicate when the system state is such that the microcontroller is assured safe access to the shared device, e.g., to non-volatile memory.

[0054] In 204, while the system is in the first state, i.e., the state where the microcontroller is insured safe access to the device, or can prohibit access by the processor in the system to the shared device, and has properly configured access to the device, the microcontroller may retrieve or exchange data with the device 108. For example, in embodiments where the system state is dependent on or indicated by a management signal, e.g., a system reset signal, the microcontroller may generate or receive the management signal, and hold the management signal in this state, i.e., may maintain assertion of the management signal, and, while this signal is asserted, may read, write, acquire, or otherwise exchange (e.g., via invocation of a read or write by some other component of the system), data or program instructions from, to, or with, the device. In one embodiment, while the system is held in the first state, the microcontroller may fetch program instructions/data from the non-volatile memory and load the program instructions/data into a memory of the microcontroller.

[0055] In 206, once the controller has completed the data retrieval or exchange with the device or has determined that it may no longer be assured of safe access, the microcontroller may reconfigure the interface through control signals to enable access by the processor in the system, e.g., via a switch that controls access to the device, as will be described below in more detail.

[0056] In 208, once the microcontroller has configured the device to enable access by the processor in the system, the microcontroller may change or allow change of the system state, thereby permitting the processor in the system to access the shared device. For example, in embodiments where the system state is dependent on or indicated by a management signal, e.g., a system reset signal, the microcontroller may de-assert the management signal, thereby putting the system into a state that allows access to the shared device by the processor of the system. Said another way, after the program instructions/data have been loaded, the microcontroller may switch access to the shared device, e.g., the non-volatile memory, from the microcontroller to the processor, and release the system from the first state.

[0057] Thus, using embodiments of the above-described method, the microcontroller 102 may preempt or suspend access to the device by the processor, e.g., the main CPU, of the system, or otherwise configure safe access to the device by the microcontroller; retrieve or otherwise exchange data or program instructions with the device; then return access to the device to the processor, or otherwise relinquish exclusive or safe access to the device by the microcontroller.

[0058] It should be noted that in various other embodiments where the microcontroller manages or controls operating states of the system (e.g., reset, POR, sleep, and other states related to specific system activities where it is known by the microcontroller that the system cannot or will not access the device), the microcontroller may monitor (or control) such system states, and take advantage of these states to access the device safely, e.g., to take control and use the shared device. Note that these system states should be

such that the microcontroller either manages when the system will exit these states or is provided sufficient warning as to when the system will again need control of the shared interface (to the device).

[0059] As one example, when a system is being shut down, the microcontroller may take over the device interface, i.e., may redirect the device interface to allow (only) access by the microcontroller, before power-off, i.e., before turning off the final power rail. In this way, writes or other exchanges with the shared device may be “saved up” or queued, and their completion (e.g., by the microcontroller) may be guaranteed before final power off.

[0060] Thus, the microcontroller 102 may gracefully share access to the device 108 with the processor of the system. It should be noted that in other embodiments, additional microcontrollers may also share the device with the host or main system CPU, using the techniques described above. In further embodiments, such sharing of devices may also be used in other ways. For example, in some embodiments, a plurality of processors (e.g., microcontrollers) may share such a device, where each processor may in turn suspend or prevent access to the device by the other processors while it accesses the device.

Other Embodiments

[0061] Below are described more specific embodiments of the above-described general method of Figure 2 that are particularly directed to the sharing of non-volatile memory between a main processor and a microcontroller in a system. In other words, in the below embodiments, the shared device comprises a non-volatile memory device. It should be noted, however, that the embodiments of Figure 3 are meant to be exemplary only, and are not intended to limit the type or use of the shared device to any particular form or function.

Figure 3 –Method for Sharing Non-Volatile Memory Between Processors in a System

[0062] Figure 3 is a high-level flowchart of a method for sharing non-volatile memory between processors, e.g., between a processor and a microcontroller in a system, e.g., a

computer system, according to one embodiment. It should be noted, however, that in other embodiments, any other types of memory may be used as desired, e.g., RAM, ROM, etc. In various embodiments, some of the method elements shown may be performed concurrently, in a different order than shown, or may be omitted. Additional method elements may also be performed as desired. As shown, this method may operate as follows.

[0063] In 302, in response to a system state change, such as, for example, power on reset (POR), system reset, or sleep mode, where a microcontroller, e.g., microcontroller 102, in a system is assured of safe access to a non-volatile memory, or can prevent the system from entering a state where a processor in the system can access the non-volatile memory, the microcontroller may set control signals or utilize software to cause access to the non-volatile memory to be with the microcontroller. In other words, when the system is changed to a state, e.g., a first state, in which the microcontroller 102 is guaranteed the ability to access the non-volatile memory safely, e.g., without interruption or interference by the processor, the microcontroller may hold the system in the state and switch access to the non-volatile memory from the processor to the microcontroller. Examples of this first state may include one or more of: a power on reset (POR) state, a system reset state, or a sleep state, among others.

[0064] Holding the system in this first state may prohibit the processor in the system from accessing the non-volatile memory in the system. Similarly, the state change may be invoked or caused by a management signal, such as a POR, system reset, sleep, signal, etc., which may include a software signal, event, token, handshake, etc. In one embodiment, holding the system in the first state may include holding a management signal in a corresponding state, e.g., holding a system reset signal in a reset state.

[0065] Note that the management signal, e.g., the POR and/or the system reset, and/or any other type of management signal used, may or may not be invoked by the microcontroller. Thus, for example, in response to a received management signal, e.g., POR signal, or in response to generating the management signal, e.g., the POR signal, the microcontroller may generate or receive another management signal, e.g., the system

reset signal, then hold or assert the other management signal in a specified state, e.g., a reset state.

[0066] As noted above with reference to Figure 1B, in one embodiment, the microcontroller 102 may be situated between the system interface 106 (and therefore, the processor in the system) and the shared device 108, e.g., non-volatile memory, e.g., embedded flash memory, and thus may intercept communications between the system interface and the device, e.g., the non-volatile memory. As will be described below in more detail, in some embodiments, when the system is held in the first state, e.g., when the system reset signal is held in the reset state, the interface to the non-volatile memory may be configured by the microcontroller to preclude the processor in the system from accessing the non-volatile memory, e.g., via a switch.

[0067] Figure 4 illustrates an exemplary embodiment of the microcontroller 102 of Figure 1B, where the device 108 comprises non-volatile memory. As Figure 4 shows, in this embodiment, the microcontroller 102 includes a system reset line 403 for communicating a reset signal, i.e., a system reset signal (or other management signal), e.g., to or from the system interface 106 over the system management bus 101 (see Figure 1B). While many of the embodiments described herein reference a reset signal, it should be noted that in other embodiments, as mentioned above, other signals may be used as desired, e.g., any signal that corresponds with or invokes a suspension of non-volatile memory access by the CPU (or other specified processor) of the system, or which indicates a system state in which the microcontroller may have safe access to the non-volatile memory, including software events, tokens, handshakes, signals, etc. Note that Figure 4 only illustrates features of the microcontroller that relate directly to embodiments of the present invention, i.e., components not necessary to understand the present invention have been omitted for brevity and simplicity.

[0068] As discussed above, in various embodiments, the switching of access to the shared device from the processor to the microcontroller may be performed via hardware, via software, or via a combination of software and hardware. As also discussed above, the term “signal” may denote a hardware signal and/or a software signal, e.g., a software event, message, token, handshake, etc., i.e., the term “management signal” may refer to a hardware signal or a software signal.

[0069] As also indicated above, in a preferred embodiment, the microcontroller controls and manages power on reset (POR) for the system, and thus may respond to and/or generate signals or software events or messages related to power on reset or system reset (or other management signals) in a way that preempts access to the device by the main processor of the system, thereby facilitating sharing a non-volatile memory that otherwise could not be shared. In some embodiments, the change in system state may be invoked or indicated by a management signal, e.g., a system reset or POR signal, generated or received by the microcontroller. It should be noted, however, that in some embodiments, control of the direction of the interface, i.e., control of which component of the system has access to the non-volatile memory, may be independent of the management (e.g., system reset or POR) signal. In other words, the microcontroller may control whether the non-volatile memory interface is directed to the processor of the system, or to the microcontroller, independent of the management (e.g., system reset or POR) signal. Moreover, as noted above, in some embodiments, instead of, or in addition to, hardware signals, the microcontroller may respond to software events, messages, tokens, handshakes, etc., that may indicate when the system state is such that the microcontroller is assured safe access to the non-volatile memory.

[0070] In 304, while the system is in the first state, i.e., the state where the microcontroller is insured safe access to the device, or can prohibit access by the processor in the system to the non-volatile memory, and has properly configured access to the non-volatile memory, the microcontroller may retrieve or exchange data with the non-volatile memory. For example, while the system is held in the first state, the microcontroller may fetch program instructions/data from the non-volatile memory and load the program instructions/data into a memory of the microcontroller.

[0071] In one embodiment, holding the system in the first state may include holding a system reset signal (or other management signal) in the reset state, e.g., asserting system reset. While the system reset signal is held in the reset state, and the interface to the non-volatile memory is configured to only allow access by the microcontroller, the microcontroller may fetch program instructions/data from the non-volatile memory and load the program instructions/data into a memory of the microcontroller, or otherwise

access the non-volatile memory. In other words, the microcontroller may hold the system reset signal in the reset state (e.g., on the system management bus 101 via system reset line 403), i.e., may maintain assertion of the system reset signal, and, while the system reset signal is asserted, may fetch, i.e., read, acquire, or otherwise receive (e.g., via invocation of a read by some other component of the system), program instructions/data from the non-volatile memory and load or write the program instructions/data into the microcontroller's memory. Note that the microcontroller's memory is preferably RAM (random access memory), although any type of re-writeable memory may be used as desired. As noted above, in some embodiments, the program instructions / data may include program firmware code, that may, for example, be usable by the embedded microcontroller for startup or reset functionality, e.g., for initializing the microcontroller, among other uses. In some embodiments, the microcontroller may be or include a peripheral device controller for a computer system. For example, in one exemplary embodiment, the embedded microcontroller may be a keyboard controller, and the non-volatile memory device 108 may store keyboard controller (KBC) code, although in other embodiments, any other program instructions/code or data may be used as desired.

[0072] Referring again to Figure 4, as may be seen, in this embodiment, the microcontroller 102 may include or couple to the host memory bus 105, which, as indicated in Figure 1B, may couple to the system interface 106, and may also include or couple to device bus 107, in this embodiment, a non-volatile memory bus 107, which may couple to the shared non-volatile memory device 108. Note that in the embodiment shown, the host memory bus 105 and the non-volatile memory bus 107 each includes three lines, one each for data, clock, and CSb signals, where CSb stands for Chip Select bar, which is a low true version of the Chip Select, and as such is part of the address structure of the block. In one embodiment, the host memory bus 105 and the non-volatile memory bus 107 are SPI (serial peripheral interface) buses, although other protocols may be used as desired. Note that in some embodiments, the host memory bus 105 and the non-volatile memory bus 107 may be considered the same bus, e.g., a memory bus, where the microcontroller 102 is inserted to switchably intercept and possibly redirect signals on the bus(es).

[0073] As Figure 4 indicates, in this embodiment, the microcontroller 102 includes a switch 404 controlled by switch control 406, for providing switching functionality for the host memory bus 105 and the non-volatile memory bus 107, e.g., for the memory bus. In some embodiments, the switch 404 may comprise a Q switch, although it should be noted that the term “Q switch” may refer not only to actual Q switches, but to functional equivalents or analogs, as well. Said another way, the switch 404 may be a “conceptual Q switch”, that may perform the functionality of a Q switch (or functionality similar to a Q switch), but which may implement this functionality in ways different from a Q switch. Note that in the embodiment of Figure 4, the switch 404 includes a respective switch for each of the memory bus lines, as indicates by the “X3” (times three) label. Thus, each line on the memory bus may be switched independently, although in preferred embodiments, these lines may all be switched together, thereby suspending or inhibiting communications between the host interface 106 and the non-volatile memory 108. Of course, in other embodiments, any numbers of bus lines/switches may be used as desired.

[0074] It should be noted that in other embodiments, the microcontroller 102 may not include the switch 404, but rather may couple to a switch that is external to the microcontroller. One benefit of this approach is that it may save pins on the microcontroller.

[0075] As Figure 4 further indicates, each line on the memory bus may be coupled to respective buffers for communicating data/signals between the memory bus (i.e., the device bus) and the microcontroller 102, where, as noted above, most of the internal components of the microcontroller 102 have been omitted from the figure. Thus, as Figure 4 shows, the microcontroller 102 may be operable to switchably preempt and inhibit signal flow on the memory bus (i.e., the host memory bus 105 and the non-volatile memory bus 107) between the host interface 106 and the non-volatile memory 108, e.g., by placing the switches into a high-impedance state, and to fetch instructions/data from the non-volatile memory 108 while communication between the host interface 106 and the non-volatile memory 108 is suspended. Thus, the microcontroller may operate to configure the interface to the device (e.g., the switch) to regulate and enforce safe access to the device.

[0076] In 306, once the controller has completed the data retrieval or exchange with the non-volatile memory, or has determined that it may no longer be assured of safe access, the microcontroller may reconfigure the interface through control signals to enable access by the processor in the system, e.g., via a switch that controls access to the non-volatile memory.

[0077] In a more specific embodiment, after the microcontroller has loaded the program instructions/data from the non-volatile memory, the microcontroller may release the system reset signal from the reset state, thereby permitting the processor in the system access to the non-volatile memory. In other words, upon completion of the fetch of instructions/data from the non-volatile memory 108 by the microcontroller 102, the microcontroller may terminate the suspension or preemption of communications between host interface 106 and the non-volatile memory 108, thereby allowing resumption of such communications, e.g., via switch 404.

[0078] Thus, using embodiments of the above-described method, the microcontroller 102 may preempt or suspend communications with the non-volatile memory by the main CPU and read instructions/data from the non-volatile memory, e.g., to initialize the microcontroller 102 and/or perform other functionality prior to, or independent from, operation of the main system, i.e., the main CPU, thus sharing the non-volatile memory with the main system. For example, in some embodiments, the microcontroller may, in addition to initialization code/data, may also fetch program instructions and/or data related to pre-boot security operations, and may operate to perform such pre-boot security operations prior to boot-up of the main system, thereby providing additional security to the system.

[0079] Figure 5 is a signal timing diagram that illustrates timing aspects of the above method, according to one embodiment. As Figure 5 shows, in this particular embodiment, a VCC, i.e., power supply voltage, is provided, followed by a VCC PWRGD (“power good”) signal indicating that the power supply voltage is valid, i.e., is at a valid level and is stable. It should be noted that the particular names or labels for these signals or voltages are exemplary only, and are not intended to limit the signals or voltages used to any particular names or representations.

[0080] As indicated, once the supply voltage is stable, the microcontroller 102 may hold the (generated or received) system reset signal in a reset state, here shown in the “low” state (e.g., a “low” or negative assertion state), during which time the microcontroller 102 may fetch and load instructions/data, e.g., controller firmware code, from the non-volatile memory, and during which, due to the system reset signal being held in the reset state, the host, i.e., the main system CPU, is inhibited from accessing the non-volatile memory. As Figure 5 also shows, once this loading is done, the reset signal is de-asserted (shown in Figure 5 as being put into the “high” state), after which the non-volatile memory is accessible by the host or main system CPU.

[0081] Thus, the microcontroller 102 may gracefully share use of the main system’s non-volatile memory. It should be noted that in other embodiments, additional microcontrollers may also share this non-volatile memory (or device) with the host or main system CPU, using the techniques described above. In further embodiments, such sharing of non-volatile memory may also be used in other ways. For example, in some embodiments, a plurality of microcontrollers may share a non-volatile memory (e.g., that is not used by the main system CPU), where each microcontroller may in turn suspend or prevent access to the non-volatile memory by the other microcontrollers while it loads instructions/data from the memory. Thus, various embodiments described with reference to Figure 3 may allow an embedded microcontroller to upload its firmware and data from a non-volatile memory device that is already present in the system and therefore save the cost and avoid issues associated with a private flash or ROM storage for the microcontroller.

[0082] Note that in various embodiments, the system changing to a state where the microcontroller is assured safe access to the non-volatile memory (or device) may be performed or mediated by software or hardware. In other words, in some embodiments, the state change may be in response to hardware signals, such as POR signals, etc., but in other embodiments, the state change may be in response to software events, tokens, software conditions, software messages, software handshakes, and so forth. Said another way, embodiments of the present invention are intended to cover virtually any case where the embedded controller can determine that it can safely take control of the shared non-

volatile memory, whether the “safe” system state is mediated or signaled via software or hardware.

[0083] Thus, various embodiments of the invention described herein may allow an embedded microcontroller and a processor in a system to share a device, e.g., a non-volatile memory, that is not designed to be shared.

We Claim:

1. A system, comprising:
a non-volatile memory;
a processor; and
a microcontroller coupled to the non-volatile memory and to the processor,
wherein the microcontroller is configured to:
in response to a change in system state to a first state wherein the microcontroller is assured safe access to the non-volatile memory, hold the system in the first state and switch access to the non-volatile memory from the processor to the microcontroller;
while the system is held in the first state, fetch program instructions/data from the non-volatile memory and load the program instructions/data into a memory of the microcontroller; and
after the program instructions/data have been loaded, switch access to the non-volatile memory from the microcontroller to the processor, and release the system from the first state.
2. The system of claim 1, wherein the change in system state to the first state is performed by software.
3. The system of claim 1, wherein the first state comprises one or more of:
a power on reset (POR) state;
a system reset state; or
a sleep state.
4. The system of claim 1, wherein the program instructions/data comprise firmware code and/or data for the microcontroller.

5. The system of claim 1, the microcontroller is a peripheral device controller for a computer system.

6. A method for sharing a non-volatile memory between a processor and a microcontroller in a system, comprising:

in response to a change in system state to a first state wherein the microcontroller is assured safe access to the non-volatile memory, holding the system in the first state and switching access to the non-volatile memory from the processor to the microcontroller;

while the system is held in the first state, fetching program instructions/data from the non-volatile memory and loading the program instructions/data into a memory of the microcontroller; and

after the program instructions/data have been loaded, switching access to the non-volatile memory from the microcontroller to the processor, and releasing the system from the first state.

7. The method of claim 6, wherein the change in system state to the first state is performed by software.

8. The method of claim 6, wherein the first state comprises one or more of:
a power on reset (POR) state;
a system reset state; or
a sleep state.

9. The method of claim 6, wherein the program instructions/data comprise firmware code and/or data for the microcontroller.

10. The method of claim 6, the microcontroller is a peripheral device controller for a computer system.

11. A system, comprising:
 - a non-volatile memory;
 - a processor; and
 - a microcontroller coupled to the non-volatile memory and to the processor, wherein the microcontroller is configured to:
 - in response to a power on reset, hold a system reset signal in a reset state, thereby prohibiting the processor from accessing the non-volatile memory;
 - while the system reset signal is held in the reset state, fetch program instructions/data from the non-volatile memory and load the program instructions/data into a memory of the microcontroller; and
 - after the program instructions/data have been loaded, permit the processor in the system access to the non-volatile memory, and release the system reset signal from the reset state.
12. The system of claim 11, wherein the program instructions/data comprise firmware code and/or data for the microcontroller.
13. The system of claim 12, the microcontroller is a peripheral device controller for a computer system.
14. The system of claim 11, wherein the microcontroller is coupled to the non-volatile memory via a non-volatile memory bus, and wherein the microcontroller is operable to fetch the program instructions/data from the non-volatile memory via the non-volatile memory bus.
15. The system of claim 14, wherein the microcontroller is coupled to the processor via a host memory bus, and wherein the microcontroller is operable to switchably intercept or pass communications between the processor and the non-volatile memory.

16. The system of claim 15, wherein the microcontroller comprises or is coupled to a switch, interposed between the non-volatile memory bus and the host memory bus, wherein the switch is controllable by the microcontroller to switchably intercept or pass communications between the processor and the non-volatile memory

17. A method for sharing a non-volatile memory between a processor and a microcontroller in a system, comprising:

in response to a power on reset, holding a system reset signal in a reset state, thereby prohibiting the processor from accessing the non-volatile memory;

while the system reset signal is held in the reset state, fetching program instructions / data from the non-volatile memory and loading the program instructions / data into a memory of the microcontroller; and

after the program instructions/data have been loaded, permitting the processor in the system access to the non-volatile memory, and releasing the system reset signal from the reset state.

18. The method of claim 17, wherein the program instructions/data comprise firmware code and/or data for the microcontroller.

19. The method of claim 17, the microcontroller is a peripheral device controller for a computer system.

20. The method of claim 17, wherein the microcontroller is coupled to the processor via a system reset bus, and wherein the microcontroller is operable to assert the system reset signal over the system reset bus.

21. The method of claim 17, wherein the microcontroller is coupled to the non-volatile memory via a non-volatile memory bus, and wherein the microcontroller is operable to fetch the program instructions/data from the non-volatile memory via the non-volatile memory bus.

22. The method of claim 21, wherein the microcontroller is coupled to the processor via a host memory bus, and wherein the microcontroller is operable switchably intercept or pass communications between the processor and the non-volatile memory.

23. The method of claim 22, wherein the microcontroller comprises or is coupled to a switch, interposed between the non-volatile memory bus and the host memory bus, wherein the switch is controllable by the microcontroller to switchably intercept or pass communications between the processor and the non-volatile memory

24. A system, comprising:

a processor;

a microcontroller; and

a device, coupled to the processor and the microcontroller;

wherein the microcontroller is configured to:

in response to a change in system state to a first state wherein the microcontroller is assured safe access to the device, set one or more control signals to cause access to the shared device to be with the microcontroller;

while the system is in the first state, retrieve or exchange data with the device;

when the controller has completed the data retrieval or exchange with the device or has determined that it is no longer assured of safe access, reconfigure the interface through control signals to enable access by the processor; and

change or allow change of the system state, thereby permitting the processor in the system to access the shared device.

25. A method for sharing a device between a processor and a microcontroller in a system, comprising:

in response to a change in system state to a first state wherein the microcontroller is assured safe access to the device, setting one or more control signals to cause access to the shared device to be with the microcontroller;

while the system is in the first state, retrieving or exchanging data with the device;

when the controller has completed the data retrieval or exchange with the device or has determined that it is no longer assured of safe access, reconfiguring the interface through control signals to enable access by the processor; and

changing or allowing change of the system state, thereby permitting the processor in the system to access the shared device.

ABSTRACT OF THE DISCLOSURE

System and method for sharing a device, e.g., non-volatile memory, between a host processor and a microcontroller. In response to system state change to a first state wherein the microcontroller is assured safe access to the non-volatile memory (e.g., in response to power-on reset, system reset, sleep state, etc.), the microcontroller holds the system in the first state (e.g., system reset), and switches access to the non-volatile memory from the processor to the microcontroller. While the system is held in the first state, the microcontroller accesses the device (e.g., non-volatile memory), e.g., fetches program instructions/data from the non-volatile memory and loads the program instructions/data into a memory of the microcontroller. After the access, the microcontroller changes or allows change of the system state, e.g., switches access to the device, e.g., the non-volatile memory, from the microcontroller to the processor, and releases the system from the first state.

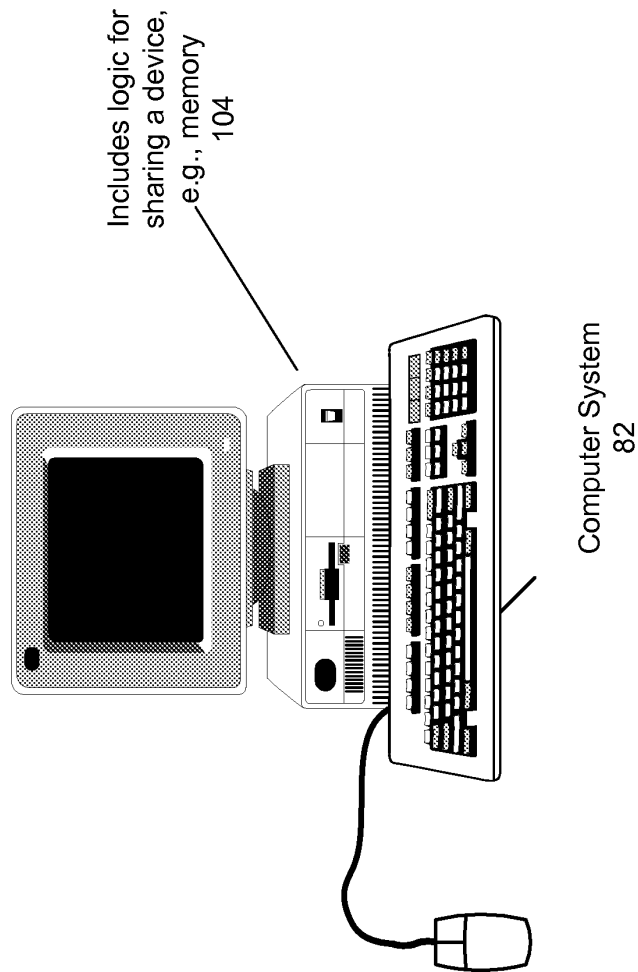


Figure 1A

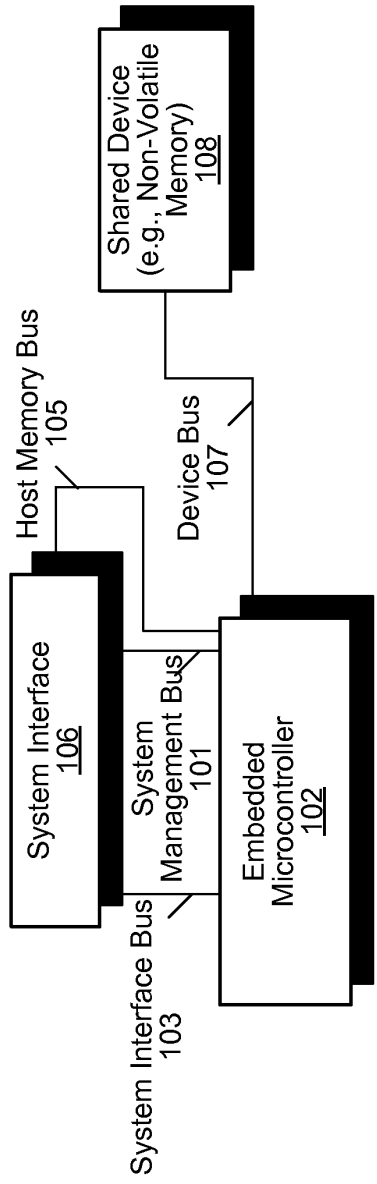


Figure 1B

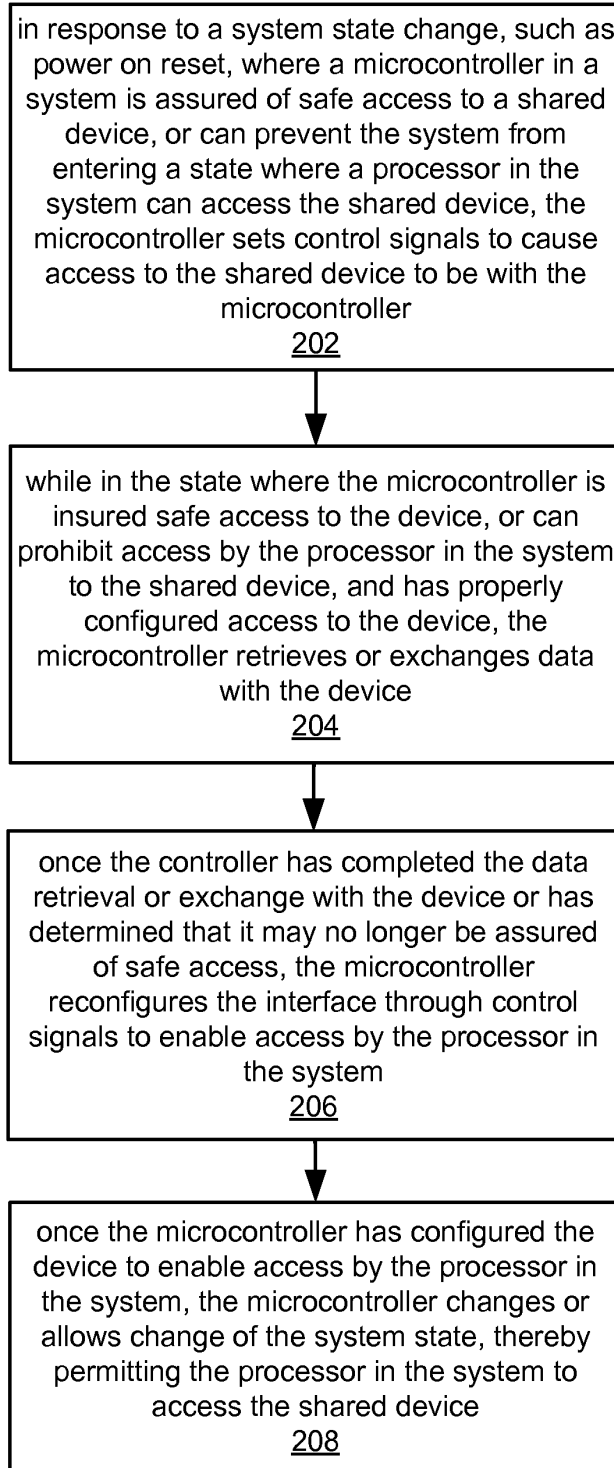


Figure 2

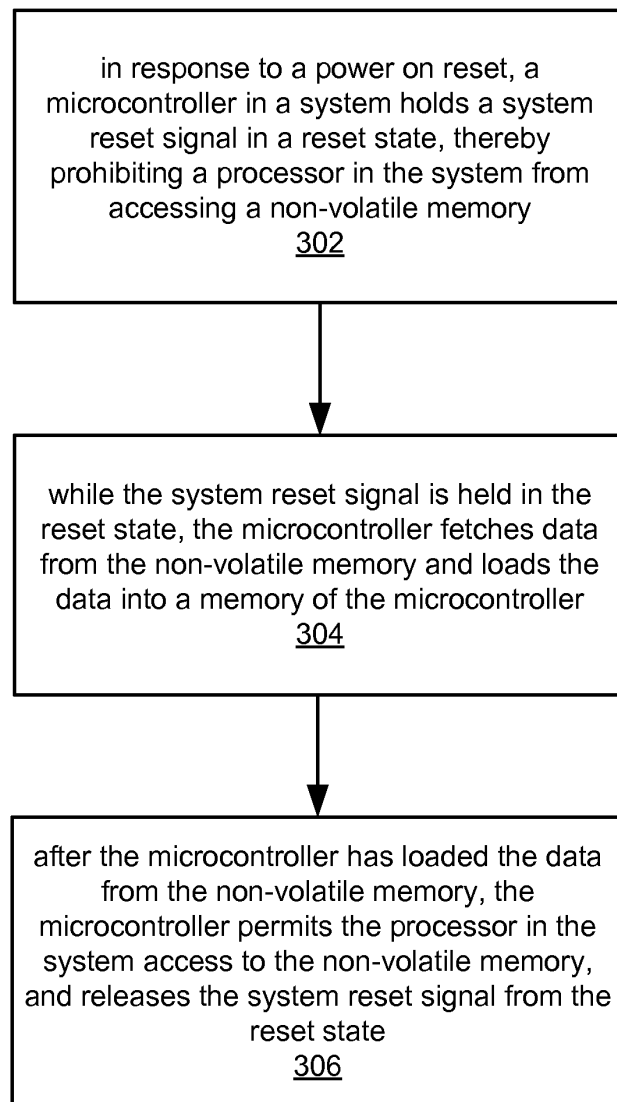


Figure 3

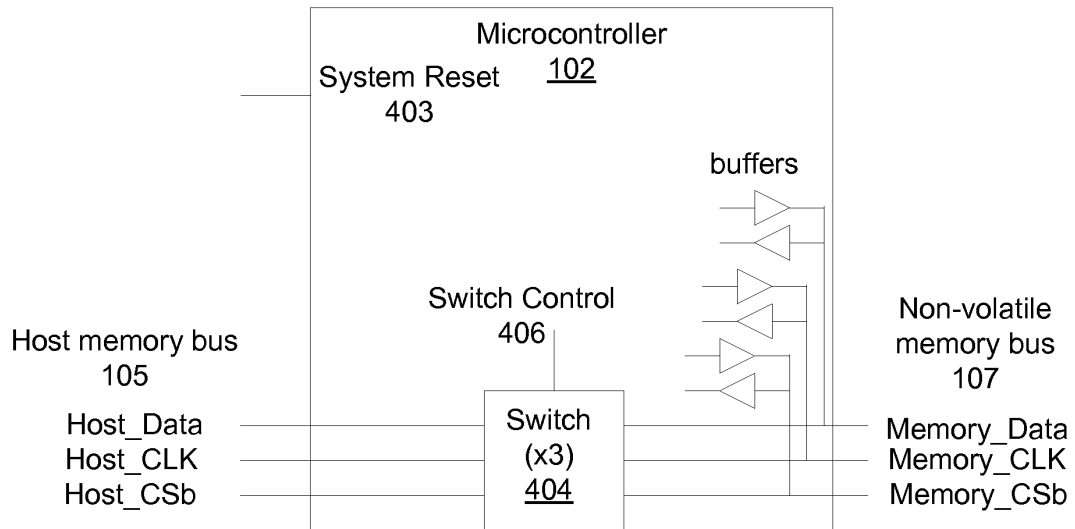


Figure 4

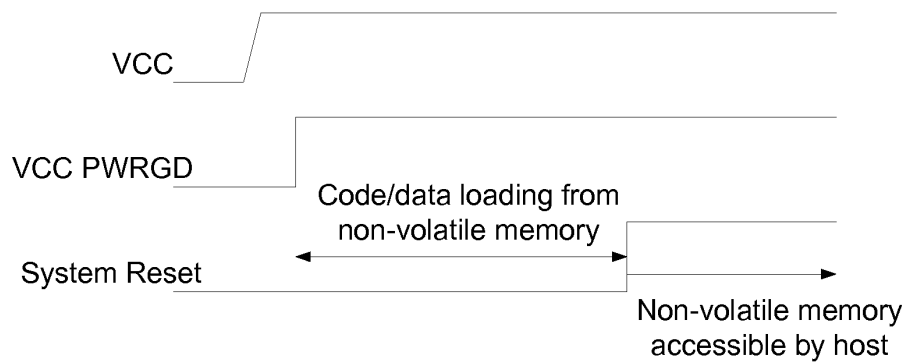


Figure 5

DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled "SHARING NON-SHARABLE DEVICES BETWEEN AN EMBEDDED CONTROLLER AND A PROCESSOR IN A COMPUTER SYSTEM," the specification of which:

☒ is attached hereto.
☐ was filed on _____ as Application Serial No. _____
 and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate listed below, or under § 365(a) of any PCT international application listed below designating at least one country other than the United States of America, and have identified below any foreign application for patent or inventor's certificate, or of any PCT international application, having a filing date before that of the application on which priority is claimed.

<u>Prior Foreign Application No.</u>	<u>Country</u>	<u>Filing Date</u> (mm/dd/yy)	<u>Priority</u> <u>Claimed</u>	<u>Cert. copy</u> <u>Attached</u>
N/A				

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

<u>Provisional Application No.</u>	<u>Filing Date</u> (mm/dd/yy)
60/910,863	04/10/07

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below, or under § 365(c) of any PCT international application listed below designating the United States of America, and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in 37 C.F.R. § 1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application.

<u>Parent Application No.</u>	<u>Filing Date</u> (mm/dd/yy)	<u>Parent Patent No. (if applicable) or Status</u>
N/A		

I hereby revoke any previous Powers of Attorney and appoint **the practitioners at Customer Number 35690**, which currently includes Jeffrey C. Hood, Reg. No. 35,198; B. Noël Kivlin, Reg. No. 33,929; Robert C. Kowert Reg. No. 39,255; Eric B. Meyertons, Reg. No. 34,876; Mark S. Williams, Reg. No. 50,658; Mark K. Brightwell, Reg. No. 47,446; Russell E. Henrichs, Reg. No. 50,354; and Mario J. Lewin, Reg. No. 54,268; with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive the Letters Patent.

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Austin, Texas 78767-0398
Phone: (512) 853-8800

I hereby declare that all statements made herein of my own knowledge are true and that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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DECLARATION AND POWER OF ATTORNEY

As a below named inventor, I hereby declare that:

My residence, post office address, and citizenship are as stated below next to my name.

I believe the inventor(s) named below to be the original and first inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled "SHARING NON-SHARABLE DEVICES BETWEEN AN EMBEDDED CONTROLLER AND A PROCESSOR IN A COMPUTER SYSTEM," the specification of which:

☒ is attached hereto.
☐ was filed on _____ as Application Serial No. _____
 and was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate listed below, or under § 365(a) of any PCT international application listed below designating at least one country other than the United States of America, and have identified below any foreign application for patent or inventor's certificate, or of any PCT international application, having a filing date before that of the application on which priority is claimed.

<u>Prior Foreign Application No.</u>	<u>Country</u>	<u>Filing Date</u> (mm/dd/yy)	<u>Priority</u> <u>Claimed</u>	<u>Cert. copy</u> <u>Attached</u>
N/A				

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

<u>Provisional Application No.</u>	<u>Filing Date</u> (mm/dd/yy)
60/910,863	04/10/07

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s) listed below, or under § 365(c) of any PCT international application listed below designating the United States of America, and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose all information known to me to be material to the patentability of the subject matter claimed in this application, as "materiality" is defined in 37 C.F.R. § 1.56, which became available between the filing date of the prior application and the national or PCT international filing date of this application.

<u>Parent Application No.</u>	<u>Filing Date</u> (mm/dd/yy)	<u>Parent Patent No. (if applicable) or Status</u>
N/A		

I hereby revoke any previous Powers of Attorney and appoint **the practitioners at Customer Number 35690**, which currently includes Jeffrey C. Hood, Reg. No. 35,198; B. Noël Kivlin, Reg. No. 33,929; Robert C. Kowert Reg. No. 39,255; Eric B. Meyertons, Reg. No. 34,876; Mark S. Williams, Reg. No. 50,658; Mark K. Brightwell, Reg. No. 47,446; Russell E. Henrichs, Reg. No. 50,354; and Mario J. Lewin, Reg. No. 54,268; with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive the Letters Patent.

Please direct all communications to:

Jeffrey C. Hood
Meyertons Hood Kivlin Kowert & Goetzel PC
P.O. Box 398
Austin, Texas 78767-0398
Phone: (512) 853-8800

I hereby declare that all statements made herein of my own knowledge are true and that all statements made herein on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. § 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

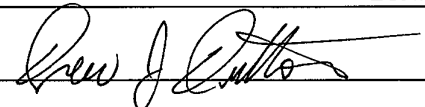
Inventor's Full Name: Ian F. Harris

Inventor's Signature: _____ Date: _____

City and State (or Foreign Country) of Residence: Kings Park, NY Citizenship: U.S.

Post Office and Residence Address: 5 Geoffrey Lane, Kings Park, NY 11754
(Include number, street name, city, state and zip code)

Inventor's Full Name: Drew J. Dutton

Inventor's Signature:  Date: Dec 5, 2007

City and State (or Foreign Country) of Residence: Austin, TX Citizenship: U.S.

Post Office and Residence Address: 1716 Camp Craft Rd., Austin, TX 78746
(Include number, street name, city, state and zip code)

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System		
First Named Inventor/Applicant Name:		Ian F. Harris		
Filer:		Jeffrey C Hood/Jeannie Miranda		
Attorney Docket Number:		5707-16601		
Filed as Large Entity				
Utility Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Utility application filing	1011	1	310	310
Utility Search Fee	1111	1	510	510
Utility Examination Fee	1311	1	210	210
Pages:				
Claims:				
Claims in excess of 20	1202	5	50	250
Independent claims in excess of 3	1201	3	210	630
Miscellaneous-Filing:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				1910

Electronic Acknowledgement Receipt	
EFS ID:	2605818
Application Number:	11958601
International Application Number:	
Confirmation Number:	1387
Title of Invention:	Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System
First Named Inventor/Applicant Name:	Ian F. Harris
Customer Number:	35690
Filer:	Jeffrey C Hood/Jeannie Miranda
Filer Authorized By:	Jeffrey C Hood
Attorney Docket Number:	5707-16601
Receipt Date:	18-DEC-2007
Filing Date:	
Time Stamp:	13:37:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1910
RAM confirmation Number	7880
Deposit Account	501505
Authorized User	
<p>The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)</p>	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		5707-16601_patent_app.pdf	161053	yes	34
			933970ae98c7a9bdb4e3c24feff6c5e91527c6fe		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	27	
	Claims		28	33	
	Abstract		34	34	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	5707-16601_formal_drawing s.pdf	72108	no	5
			ffb753d8d869f9f42887cc9ada21b224627b99b3		
Warnings:					
Information:					
3	Oath or Declaration filed	5707-16601_signed_dec_po a.pdf	190735	no	4
			ba7ae3308f9af7e4f50552a0bb144f658f68cb71		
Warnings:					
Information:					
4	Fee Worksheet (PTO-06)	fee-info.pdf	8590	no	2
			67a208f62a5e09ee77a111a94d7eee2d1168a46c		
Warnings:					
Information:					
Total Files Size (in bytes):			432486		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

Electronic Acknowledgement Receipt	
EFS ID:	2605818
Application Number:	11958601
International Application Number:	
Confirmation Number:	1387
Title of Invention:	Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System
First Named Inventor/Applicant Name:	Ian F. Harris
Customer Number:	35690
Filer:	Jeffrey C Hood/Jeannie Miranda
Filer Authorized By:	Jeffrey C Hood
Attorney Docket Number:	5707-16601
Receipt Date:	18-DEC-2007
Filing Date:	
Time Stamp:	13:37:43
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Deposit Account
Payment was successfully received in RAM	\$ 1910
RAM confirmation Number	7880
Deposit Account	501505
Authorized User	
<p>The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:</p> <p>Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)</p>	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes) /Message Digest	Multi Part /.zip	Pages (if appl.)
1		5707-16601_patent_app.pdf	161053	yes	34
			933970ae98c7a9b4b4e3c24feff6c5e91527c6fe		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Specification		1	27	
	Claims		28	33	
	Abstract		34	34	
Warnings:					
Information:					
2	Drawings-only black and white line drawings	5707-16601_formal_drawing s.pdf	72108	no	5
			ffb753d8d869f9f42887cc9ada21b224627b99b3		
Warnings:					
Information:					
3	Oath or Declaration filed	5707-16601_signed_dec_pos.a.pdf	190735	no	4
			ba7ae3308f9af7e4f50552a0bb144f658f68cb71		
Warnings:					
Information:					
4	Fee Worksheet (PTO-06)	fee-info.pdf	8590	no	2
			67a208f62a5e09ee77a111a94d7eee2d1168a46c		
Warnings:					
Information:					
Total Files Size (in bytes):			432486		

This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

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National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

12/18/07

PTO/SB/06 (12-04)

Approved for use through 7/31/2006. OMB 0651-0032

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD

Substitute for Form PTO-875

Application or Docket Number

11/958,601**APPLICATION AS FILED – PART I**

(Column 1)

(Column 2)

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

FOR	NUMBER FILED	NUMBER EXTRA
BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A
SEARCH FEE (37 CFR 1.16(k), (l), or (m))	N/A	N/A
EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A
TOTAL CLAIMS (37 CFR 1.16(i))	25 minus 20 =	* 5
INDEPENDENT CLAIMS (37 CFR 1.16(h))	6 minus 3 =	* 3
APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR	
MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))		

RATE (\$)	FEE (\$)
N/A	
N/A	
N/A	
X 25=	
X 105=	
N/A	
TOTAL	

RATE (\$)	FEE (\$)
N/A	310
N/A	510
N/A	210
X 50=	250
X 210=	630
N/A	
TOTAL	1910

* If the difference in column 1 is less than zero, enter "0" in column 2.

APPLICATION AS AMENDED – PART II

(Column 1)

(Column 2)

(Column 3)

SMALL ENTITY

OR

OTHER THAN
SMALL ENTITY

AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(i))	*	Minus **	=
Independent (37 CFR 1.16(h))	*	Minus ***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

RATE (\$)	ADDI- TIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL	
ADD'T FEE	

RATE (\$)	ADDI- TIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL	
ADD'T FEE	

(Column 1)

(Column 2)

(Column 3)

OR

AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total (37 CFR 1.16(i))	*	Minus **	=
Independent (37 CFR 1.16(h))	*	Minus ***	=
Application Size Fee (37 CFR 1.16(s))			
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))			

RATE (\$)	ADDI- TIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL	
ADD'T FEE	

RATE (\$)	ADDI- TIONAL FEE (\$)
X =	
X =	
N/A	
TOTAL	
ADD'T FEE	

* If the entry in column 1 is less than the entry in column 2, write "0" in column 3.

** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".

*** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".

The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



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P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
11/958,601	12/18/2007	2612	1910	5707-16601	25	6

CONFIRMATION NO. 1387

Jeffrey C. Hood
Meyertons Hood Kivlin Kowert & Goetzel PC
P.O. Box 398
Austin, TX 78767-0398

FILING RECEIPT



OC000000027685756

Date Mailed: 01/14/2008

Receipt is acknowledged of this non-provisional patent application. The application will be taken up for examination in due course. Applicant will be notified as to the results of the examination. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please write to the Office of Initial Patent Examination's Filing Receipt Corrections. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Ian F. Harris, Kings Park, NY;
Drew J. Dutton, Austin, TX;

Power of Attorney: The patent practitioners associated with Customer Number 35690

Domestic Priority data as claimed by applicant

This appln claims benefit of 60/910,863 04/10/2007

Foreign Applications

If Required, Foreign Filing License Granted: 01/14/2008

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 11/958,601**

Projected Publication Date: 10/16/2008

Non-Publication Request: No

Early Publication Request: No

Title

Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System

Preliminary Class

340

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

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page 2 of 3

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This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign AssetsControl, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	11958601
	Filing Date	2007-12-18
	First Named Inventor	Ian F. Harris
	Art Unit	2612
	Examiner Name	Unknown
	Attorney Docket Number	5707-16601

U.S. PATENTS							Remove	
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1	5925097		1999-07-20	Gopinath, et al.			
	2	5634004		1997-05-27	Gopinath, et al.			
If you wish to add additional U.S. Patent citation information please click the Add button.							Add	
U.S. PATENT APPLICATION PUBLICATIONS							Remove	
Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear		
	1							
If you wish to add additional U.S. Published Application citation information please click the Add button.							Add	
FOREIGN PATENT DOCUMENTS							Remove	
Examiner Initial*	Cite No	Foreign Document Number ³	Country Code ² j	Kind Code ⁴	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear	T ⁵
	1							<input type="checkbox"/>
If you wish to add additional Foreign Patent Document citation information please click the Add button.							Add	
NON-PATENT LITERATURE DOCUMENTS							Remove	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		11958601
	Filing Date		2007-12-18
	First Named Inventor	Ian F. Harris	
	Art Unit	2612	
	Examiner Name	Unknown	
	Attorney Docket Number	5707-16601	

Examiner Initials*	Cite No	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc), date, pages(s), volume-issue number(s), publisher, city and/or country where published.	T ⁵
	1		<input type="checkbox"/>

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	
--------------------	--	-----------------	--

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		11958601
	Filing Date		2007-12-18
	First Named Inventor	Ian F. Harris	
	Art Unit	2612	
	Examiner Name	Unknown	
	Attorney Docket Number	5707-16601	

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ Fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ None

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Jeffrey C. Hood/	Date (YYYY-MM-DD)	2008-10-09
Name/Print	Jeffrey C. Hood	Registration Number	35,198

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Acknowledgement Receipt	
EFS ID:	4085233
Application Number:	11958601
International Application Number:	
Confirmation Number:	1387
Title of Invention:	Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System
First Named Inventor/Applicant Name:	Ian F. Harris
Correspondence Address:	Jeffrey C. Hood Meyertons Hood Kivlin Kowert & Goetzel PC P.O. Box 398 - Austin TX 78767-0398 US 5128538800 -
Filer:	Jeffrey C Hood/Christine Acker
Filer Authorized By:	Jeffrey C Hood
Attorney Docket Number:	5707-16601
Receipt Date:	09-OCT-2008
Filing Date:	18-DEC-2007
Time Stamp:	11:30:33
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Filed (SB/08)	5707-16601_IDS_01.pdf	808695 8c9d5d62a971c1a131c663076b38657622c ef3ee	no	4
Warnings:					
Information:					
Total Files Size (in bytes):			808695		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
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www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
11/958,601	12/18/2007	Ian F. Harris	5707-16601

CONFIRMATION NO. 1387

Jeffrey C. Hood
Meyertons Hood Kivlin Kowert & Goetzel PC
P.O. Box 398
Austin, TX 78767-0398

PUBLICATION NOTICE



Title:Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System

Publication No.US-2008-0256374-A1

Publication Date:10/16/2008

NOTICE OF PUBLICATION OF APPLICATION

The above-identified application will be electronically published as a patent application publication pursuant to 37 CFR 1.211, et seq. The patent application publication number and publication date are set forth above.

The publication may be accessed through the USPTO's publically available Searchable Databases via the Internet at www.uspto.gov. The direct link to access the publication is currently <http://www.uspto.gov/patft/>.

The publication process established by the Office does not provide for mailing a copy of the publication to applicant. A copy of the publication may be obtained from the Office upon payment of the appropriate fee set forth in 37 CFR 1.19(a)(1). Orders for copies of patent application publications are handled by the USPTO's Office of Public Records. The Office of Public Records can be reached by telephone at (703) 308-9726 or (800) 972-6382, by facsimile at (703) 305-8759, by mail addressed to the United States Patent and Trademark Office, Office of Public Records, Alexandria, VA 22313-1450 or via the Internet.

In addition, information on the status of the application, including the mailing date of Office actions and the dates of receipt of correspondence filed in the Office, may also be accessed via the Internet through the Patent Electronic Business Center at www.uspto.gov using the public side of the Patent Application Information and Retrieval (PAIR) system. The direct link to access this status information is currently <http://pair.uspto.gov/>. Prior to publication, such status information is confidential and may only be obtained by applicant using the private side of PAIR.

Further assistance in electronically accessing the publication, or about PAIR, is available by calling the Patent Electronic Business Center at 1-866-217-9197.

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application. No:	11/958,601
Filed:	December 18, 2007
Inventor(s):	
	Ian F. Harris Drew J. Dutton
Title:	Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System

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Examiner:	Unknown
Group/Art Unit:	2612
Atty. Dkt. No:	5707-16601

STATUS INQUIRY

Dear Sir or Madam:

On December 18, 2007, Applicant's undersigned attorney filed the above-referenced patent application with the U.S. Patent and Trademark Office. This application has been pending nearly 2.5 years without having received a first Office Action. Applicant hereby respectfully requests the Patent Office to notify Applicant as to the status of this matter, particularly when we can expect to receive a first Office Action.

Should any fees be required, the Commissioner is hereby authorized to charge such fees to Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 50-1505/5707-16601/JCH.

Respectfully submitted,

/Jeffrey C. Hood/

Jeffrey C. Hood, Reg. #35198
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert & Goetzel PC
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Date: 2010-05-10 JCH/JAM

Electronic Acknowledgement Receipt	
EFS ID:	7581813
Application Number:	11958601
International Application Number:	
Confirmation Number:	1387
Title of Invention:	Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System
First Named Inventor/Applicant Name:	Ian F. Harris
Correspondence Address:	Jeffrey C. Hood Meyertons Hood Kivlin Kowert & Goetzel PC P.O. Box 398 - Austin TX 78767-0398 US 5128538800 -
Filer:	Jeffrey C Hood/Jeannie Miranda
Filer Authorized By:	Jeffrey C Hood
Attorney Docket Number:	5707-16601
Receipt Date:	10-MAY-2010
Filing Date:	18-DEC-2007
Time Stamp:	16:06:35
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for status of Application	5707-16601_status_inquiry_first_office_action.pdf	60306 62f1e8b5a59e4dc9aa3c729e67c20aca61fb a53a	no	1
Warnings:					
Information:					
Total Files Size (in bytes):			60306		
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>					



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/958,601	12/18/2007	Ian F. Harris	5707-16601	1387

7590 09/03/2010
Jeffrey C. Hood
Meyertons Hood Kivlin Kowert & Goetzel PC
P.O. Box 398
Austin, TX 78767-0398

EXAMINER

PATEL, NITIN C

ART UNIT	PAPER NUMBER
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2116

MAIL DATE	DELIVERY MODE
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09/03/2010

PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	11/958,601	HARRIS ET AL.	
	Examiner	Art Unit	
	NITIN C. PATEL	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1) ☒ Responsive to communication(s) filed on 18 December 2007.

2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.

3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4) ☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5) ☐ Claim(s) _____ is/are allowed.

6) ☒ Claim(s) 1-25 is/are rejected.

7) ☐ Claim(s) _____ is/are objected to.

8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9) ☐ The specification is objected to by the Examiner.

10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date <u>10/09/08</u> .	4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s)/Mail Date. _____. 5) <input type="checkbox"/> Notice of Informal Patent Application 6) <input type="checkbox"/> Other: _____.
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DETAILED ACTION

1. This Office Action is sent in response to Applicant's Communication received 18 December 2007 for application number 11/958,601. The Office hereby acknowledges receipt of the following and placed of record in file: Specification, Drawings, Abstract, Oath/Declaration, and claims.
2. Claims 1 – 25 are presented for examination.

Information Disclosure Statement

3. The information disclosure statement (IDS) submitted on 09 October 2008, was filed before the mailing date of the first office action. The submission is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Claim Objections

4. Claim 16 is objected to because of the following informalities:
 5. The period/full stop is missing at the end of the claim 16.
- Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

6. Claims 1 – 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

7. The use of slash symbols ("/) between descriptive elements in the claims 1, 4, 6, 9, 11 - 12, and 17 - 18, renders the scope and meaning of the claims unclear, as the slashes could be construed to mean "and", "Or", or both "and" and "Or". Claims 2 – 23 are directly or indirectly depending upon respective rejected claims, and therefore are rejected too.

8. Claim 24 recites the limitation "The shared device" in line 15 on page 31. There is insufficient antecedent basis for this limitation in the claim.

9. Claim 24 recites the limitation "The controller" in line 11 on page 31. There is insufficient antecedent basis for this limitation in the claim. There are two different/inconsistent nomenclature elements "the microcontroller" and "the controller", and examiner is prosecuting with assumption of they are the same one.

10. Claim 25 recites the limitation "The shared device" in lines 3, and 10 on page 32. There is insufficient antecedent basis for this limitation in the claim. There are two different/inconsistent nomenclature elements "the device" and "the shared device", and examiner is prosecuting with assumption of they are the same one.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

11. Claims 24 – 25 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Le et al. [hereinafter as Le], uS Patent 6,154,838.

12. As to claim 24, Le discloses a system [S, fig. 1A], comprising: a processor [100 CPU] [col. 5, lines 63 – 67]; a microcontroller [174, fig. 2]; and a device [122 Flash ROM] [col. 6, line 42], coupled to the processor [100] and the microcontroller [174][as shown in fig. 1 – 2][col. 9, lines 29 – 31]; wherein the microcontroller [174] is configured to: in response to a change in system state to a first state [power-up or reset] wherein the microcontroller [174] is assured safe access to the device [122], set one or more control signals to cause access to the shared device [122] to be with the microcontroller [174]; while the system is in the first state, retrieve or exchange data with the device [122]; when the controller [174] has completed the data retrieval or exchange with the device [122] [col. 12, lines 8 – 28] or has determined that it is no longer assured of safe access, reconfigure the interface through control signals to enable access by the processor [100][col. 13, lines 45 – 63, col. 16, lines 56 – 67, col. 17, lines 1 - 13, col. 17, lines 33 – 41, col. 18, lines 1 – 16]; and change or allow change [by releasing the reset input] of the system state, thereby permitting [by releasing reset input of processor] the processor [100] in the system to access the shared device [col. 12, lines 8 – 45, col. 13, lines 47 – 63, col. 14, lines 3 – 10, col. 15, lines 1 – 67, col. 17, lines 41 – 55].

13. As to claim 25, Le discloses a system and method for sharing a device [122 flash] between a processor [100 CPU] and a microcontroller [174 microcontroller] in a system [S, fig. 1 – 2], comprising: in response to a change in system state to a first state [power-up or reset] wherein the microcontroller is assured safe access to the device [122] , setting one or more control signals to cause access to the shared device [122] to be with the microcontroller; while the system is in the first state, retrieving or exchanging

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data with the device [col. 12, lines 8 – 28]; when the controller has completed the data retrieval or exchange with the device [122][col. 13, lines 45 – 63, col. 16, lines 56 – 67, col. 17, lines 1 - 13, col. 17, lines 33 – 41, col. 18, lines 1 – 16] or has determined that it is no longer assured of safe access, reconfiguring the interface through control signals to enable access by the processor; and changing or allowing change of the system state, thereby permitting the processor [100] in the system to access the shared device [122] [col. 12, lines 8 – 45, col. 13, lines 47 – 63, col. 14, lines 3 – 10, col. 15, lines 1 – 67, col. 17, lines 41 – 55].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

14. Claims 1 – 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. [hereinafter as Le], uS Patent 6,154,838, and further in view of Pang, US Patent 6,925,522 B2.

15. As to claims 1, 6, 11, and 17, Le teaches a system [S fig. 1 – 2] and method for sharing a non-volatile memory [122 Flash ROM] [col. 1, lines 17 – 20], including a non-volatile memory [122] ; a processor [100 CPU] [col. 5, lines 63 – 67]; and a microcontroller [174] coupled to the non-volatile memory [122] and to the processor [100] , wherein the microcontroller is configured to: in response to a change in system state to a first state wherein the microcontroller is assured safe access to the non-volatile memory, hold the system in the first state and switch access to the non-volatile memory from the processor to the microcontroller; while the system is held in the first state, fetch program instructions/data from the non-volatile memory; and after the program instructions/data have been loaded, switch access to the non-volatile memory from the microcontroller to the processor, and release the system from the first state [col. 3, lines 50 – 67, col. 4, lines 1 – 31, col. 12, lines 8 – 58, col. 13, lines 33 – 67, col. 14, lines 1 – 42, col. 15, lines 1 – 67, col. 16, lines 8 – 67, col. 17, lines 1 – 49, col. 18, lines 6 – 16, fig. 1 – 8].

However, Le fails to teach to load the program instructions/data into a memory of the microcontroller.

Pang teaches a device and method to change [load] codes of memory [3 flash memory] of microcontroller [1 fig. 3] by fetching the program instruction/data from SRAM [4][col. 1, lines 14 – 19, col. 2, lines 37 – 67, col. 3, lines 1 – 67, col. 5, lines 1 – 47, fig. 2 - 11].

It would have been obvious to one of ordinary skill in art, having the teachings of Le and Pang before him at the time of invention was made, to modify/include/replace an

arbiter logic for selectively assigning the ownership of the flash ROM and updating or modifying of non-volatile memory [flash] as disclosed by Le to include a device and method to change [load] codes of memory [3 flash memory] of microcontroller [1 fig. 3] by fetching the program instruction/data from SRAM [4][col. 1, lines 14 – 19, col. 2, lines 37 – 67, col. 3, lines 1 – 67, col. 5, lines 1 – 47, fig. 2 - 11] as taught by Pang in order to obtain a system and method to load and change/upgrade the program instructions/data into a memory of the microcontroller without replacing the original flash memory [col. 4, lines 43 – 47].

One of ordinary skill in the art wanted to be motivated to include a device and method to change [load] codes of memory [3 flash memory] of microcontroller [1 fig. 3] by fetching the program instruction/data from SRAM [4][col. 1, lines 14 – 19, col. 2, lines 37 – 67, col. 3, lines 1 – 67, col. 5, lines 1 – 47, fig. 2 - 11] in order to obtain a system and method to load and change/upgrade the program instructions/data into a memory of the microcontroller without replacing the original flash memory [col. 4, lines 43 – 47].

16. As to claims 2, and 7, Le teaches a system [S fig. 1 – 2] and method for sharing a non-volatile memory [122 Flash ROM] [col. 1, lines 17 – 20] wherein the change in system state to the first state is performed by software [cold boot, warm boot][col 4, lines 7 – 23, , col. 8, lines 60 – 67, col. 9, lines 1 – 67, col. 10, lines 26 – 40, col. 4, lines 7 – 16]

17. As to claims 3, and 8, Le teaches a system [S fig. 1 – 2] and method for sharing a non-volatile memory [122 Flash ROM] [col. 1, lines 17 – 20], wherein the first state comprises one or more of: a power on reset (POR) state [power-up]; a system reset

Art Unit: 2116

state [reset]; or a sleep state [idle mode] [col.3, lines 57 – 62, col. 12, lines 8 -10, col. 4, line 16, col. 10, lines 37 – 40, col. 12, lines 8 – 10].

18. As to claims 4, 9, 12, and 18, Le teaches a system [S fig. 1 – 2] and method for sharing a non-volatile memory [122 Flash ROM] [col. 1, lines 17 – 20], wherein the program instructions/data comprise firmware code [boot-up instructions or executable code] and/or data for the microcontroller [col. 10, lines 26 – 29, col. 15, lines 15 – 21].

19. As to claims 5, 10, 13, and 19, Le teaches a system [S fig. 1 – 2] and method for sharing a non-volatile memory [122 Flash ROM] [col. 1, lines 17 – 20], the microcontroller is a peripheral device controller for a computer system [col. 6, lines 21 – 35, col. 7, lines 14 – 22, col. 12, lines 1 – 2, col. 18, lines 25 – 29, fig. 1—2].

20. As to claims 14, and 21, Le teaches a system [S fig. 1 – 2], wherein the microcontroller [174] is coupled to the non- volatile memory via a non-volatile memory bus, and wherein the microcontroller is operable to fetch the program instructions/data from the non-volatile memory via the non-volatile memory bus [fig. 1 – 2].

21. As to claims 15, and 22, Le teaches a system [S fig. 1 – 2], wherein the microcontroller [174] is coupled to the processor [100] via a host memory bus, and wherein the microcontroller is operable to switchably intercept or pass communications between the processor and the non-volatile memory [col. 10, lines 56 – 65, fig. 2].

22. As to claims 16, and 23, Le teaches a system [S fig. 1 – 2], wherein the microcontroller [174] comprises or is coupled to a switch, interposed between the non-volatile memory bus and the host memory bus, wherein the switch is controllable by the

microcontroller to switchably intercept or pass communications between the processor and the non-volatile memory [col. 10, lines 56 – 65, fig. 2].

23. As to claim 20, Le teaches a system [S fig. 1 – 2] and method for sharing a non-volatile memory [122 Flash ROM] [col. 1, lines 17 – 20], wherein the microcontroller is coupled to the processor via a system reset bus, and wherein the microcontroller is operable to assert the system reset signal over the system reset bus [col. 12, lines 8 – 45, fig. 1 – 2].

24. **Examiner's note:** Examiner has cited particular columns and line numbers in the references as applied to the claims above for the convenience of the applicant.

Although the specified citations are representative of the teachings of the art and are applied to the specific limitations within the individual claim, other passages and figures may apply as well. It is respectfully requested to the applicant in preparing responses, to fully consider the references in entirety as potentially teaching all or part of the claimed invention, as well as the context of the passage as taught by the prior art as disclosed by the Examiner.

25. **Prior Art not relied upon:** Please refer to the references listed in attached PTO-892, which, are not relied upon for the claim rejection, since these references are pertinent to the disclosure.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to NITIN C. PATEL whose telephone number is (571)272-3675. The examiner can normally be reached on 6:30 am - 5:00 pm.

Art Unit: 2116

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on 571-272-3667. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Nitin C. Patel/
Primary Examiner, Art Unit 2116

Notice of References Cited	Application/Control No. 11/958,601	Applicant(s)/Patent Under Reexamination HARRIS ET AL.	
	Examiner NITIN C. PATEL	Art Unit 2116	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
*	A	US-6,154,838	11-2000	Le et al.	713/2
*	B	US-6,925,522	08-2005	Pang, Chia Yuan	711/103
*	C	US-5,819,087	10-1998	Le et al.	713/2
*	D	US-5,949,997	09-1999	Smith, Gregory James	713/2
*	E	US-7,386,326	06-2008	Sundararajan et al.	455/561
*	F	US-5,428,760	06-1995	Ghori et al.	711/149
	G	US-			
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.




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BIB DATA SHEET

CONFIRMATION NO. 1387

SERIAL NUMBER 11/958,601	FILING or 371(c) DATE 12/18/2007 RULE	CLASS 340	GROUP ART UNIT 2116	ATTORNEY DOCKET NO. 5707-16601		
APPLICANTS Ian F. Harris, Kings Park, NY; Drew J. Dutton, Austin, TX; ** CONTINUING DATA ***** This appln claims benefit of 60/910,863 04/10/2007 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 01/14/2008						
Foreign Priority claimed <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No	35 USC 119(a-d) conditions met <input type="checkbox"/> Yes <input checked="" type="checkbox"/> No	<input type="checkbox"/> Met after Allowance ncp Initials	STATE OR COUNTRY NY	SHEETS DRAWINGS 5	TOTAL CLAIMS 25	INDEPENDENT CLAIMS 6
ADDRESS Jeffrey C. Hood Meyertons Hood Kivlin Kowert & Goetzel PC P.O. Box 398 Austin, TX 78767-0398 UNITED STATES						
TITLE Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System						
FILING FEE RECEIVED 1910	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit			


Search Notes 	Application/Control No. 11958601	Applicant(s)/Patent Under Reexamination HARRIS ET AL.
	Examiner NITIN C PATEL	Art Unit 2116

SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor name search in PALM	8/26/10	ncp
EAST search results attached	8/26/10, 8/30/10, 8/31/10, 9/1/10	ncp

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner

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<i>Index of Claims</i> 	Application/Control No. 11958601	Applicant(s)/Patent Under Reexamination HARRIS ET AL.
	Examiner NITIN C PATEL	Art Unit 2116

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant			<input type="checkbox"/> CPA			<input type="checkbox"/> T.D.			<input type="checkbox"/> R.1.47		
CLAIM		DATE									
Final	Original	09/01/2010									
	1	✓									
	2	✓									
	3	✓									
	4	✓									
	5	✓									
	6	✓									
	7	✓									
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	18	✓									
	19	✓									
	20	✓									
	21	✓									
	22	✓									
	23	✓									
	24	✓									
	25	✓									

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
S1	2	("5634004" "5925097"). PN.	USPAT	OR	OFF	2010/08/26 15:54
S2	55	(shar\$4 near3 (non \$volatile or memory or storage or ram or rom or sdram or dram))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 15:58
S3	1592	((shar\$4 or access\$4) near3 (non\$volatile or memory or storage or ram or rom or sdram or dram))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 15:59
S4	1	S3 same((hold\$4 or disabl \$4 or control\$4)near3 (system adj reset))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:00
S5	1739	((hold\$4 or disabl\$4 or control\$4)near3 (system adj reset))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:01
S6	1739	((hold\$4 or disabl\$4 or control\$4)near3 (system adj reset))with reset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:01
S7	24	((hold\$4 or disabl\$4 or control\$4)near3 (system adj reset))with (reset adj state)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:02
S8	82	S3 same embedded	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:08

S9	9	("5949997").URPN.	USPAT	OR	OFF	2010/08/26 16:10
S10	3	("4665536" "5228066" "5521848").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/26 16:11
S11	14	("5623503" "5673276" "5774477" "5935266" "6108807" "6124715" "6378094" "6584590" "6983441" "7017081" "7080789" "7149943" "7251763" "7451367").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/26 16:13
S12	3	S3 same (embedded adj controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:18
S13	6	S3 same (embedded near3 controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:19
S14	24	S6 and ((hold\$4 or disabl \$4 or control\$4)near3 (system adj reset))with (reset adj state)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:20
S15	2	S14 and (embedded adj controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:21
S16	9	("5949997").URPN.	USPAT	OR	OFF	2010/08/26 16:23
S17	65	(shar\$4 near3 (non \$volatile or memory or storage or rom or sdram or dram))with (processor or cpu)with (microcontroller or micro \$controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:51
S18	3	S17 same embedded	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:51

S19	1	(shar\$4 near3 ((non \$volatile or rom or sdram or dram)adj2 (device or apparatus or memory or storage)))with (processor or cpu)with (embedded adj (microcontroller or micro\$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:56
S20	0	(shar\$4 near3 ((unsharable or non\$shar \$5 or ("not" or non) adj sharable))near3 (device or apparatus or memory or storage)))with (processor or cpu)with (embedded adj (microcontroller or micro \$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:58
S21	0	(shar\$4 with ((unsharable or non\$shar \$5 or ("not" or non) adj sharable))near3 (device or apparatus or memory or storage)))with (processor or cpu)with (embedded adj (microcontroller or micro \$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:58
S22	0	(shar\$4 with ((unsharable or non\$shar \$5 or ("not" or non) adj sharable))near3 (device or apparatus or memory or storage)))with (processor or cpu)with ((microcontroller or micro \$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:58
S23	0	(shar\$4 with ((unsharable or non\$shar \$5 or ("not" or non) adj sharable))near3 (device or apparatus or memory or storage)))with (processor or cpu)with ((microcontroller or micro \$controller)).ti.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:59

S24	0	(shar\$4 with ((unsharable or non\$shar \$5 or ("not" or non) adj sharable))near3 (device or apparatus or memory or storage)))same (processor or cpu)with ((microcontroller or micro \$controller)).ti.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:59
S25	0	(shar\$4 with ((unsharable or non\$shar \$5 or ("not" or non) adj sharable))near3 (device or apparatus or memory or storage)))same (processor or cpu)with ((microcontroller or micro \$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:59
S26	0	(shar\$4 with ((unsharable or non\$shar \$5 or ("not" or non) adj sharable))near3 (device or apparatus or memory or storage)))same (processor or cpu)same ((microcontroller or micro \$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:00
S27	0	(shar\$4 with ((unsharable or non\$shar \$5 or non-sharable or ("not" or non) adj sharable))near3 (device or apparatus or memory or storage)))same (processor or cpu)same ((microcontroller or micro \$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:00
S28	526	(shar\$4 with ((unsharable or non\$shar \$5 or non-sharable or ("not" or non) adj sharable))near3 (device or apparatus or memory or storage)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:01
S29	0	S28 same (processor or cpu)same (embedded adj (microcontroller or micro\$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:01

S30	0	S28 same (processor or cpu) same ((microcontroller or micro\$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:01
S31	0	S28 and S17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:02
S32	32	S28 and (processor or cpu) same ((microcontroller or micro\$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:02
S33	0	S28 same ((processor or cpu) same (microcontroller or micro \$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:02
S35	8	S17 same ((load\$4 or writ \$4 or sav\$3) near6 (code or software or firmware or program or instruction41 or data))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:24
S36	0	("7386326").URPN.	USPAT	OR	OFF	2010/08/30 11:31
S37	15	("5428760").URPN.	USPAT	OR	OFF	2010/08/30 12:51
S38	16	("20010014603" "20010055038" "20010055948" "20020034967" "20020049061" "20030003961" "20030040275" "20040092277" "4449248" "5734686" "5864570" "6346911" "6396884" "6549784" "6901270" "7165173"). PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/30 12:53
S39	0	("7386326").URPN.	USPAT	OR	OFF	2010/08/30 12:54

S40	65	(shar\$4 near3 (non \$volatile or memory or storage or rom or sdram or dram))with (processor or cpu)with (microcontroller or micro \$controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 12:55
S41	8	S40 same ((load\$4 or writ \$4 or sav\$3)near6 (program or instruction41 or data))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 12:55
S42	39	S40 and ((load\$4 or writ \$4 or sav\$3)near6 (program or instruction41 or data))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 12:57
S43	10	S40 and (((load\$4 or writ \$4 or sav\$3)near6 (program or instruction41 or data)) with (non\$volatile or flash or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 12:57
S44	22	("5819087").URPN.	USPAT	OR	OFF	2010/08/30 13:00
S45	14	("5022077" "5269022" "5327531" "5327549" "5388267" "5410707" "5603055" "5619726" "5701477" "5794054" "5819087" "5822582" "5887164" "5935242").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/30 13:06
S46	14	("5022077" "5269022" "5327531" "5327549" "5388267" "5410707" "5603055" "5619726" "5701477" "5794054" "5819087" "5822582" "5887164" "5935242").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/30 13:11
S47	18	("6154838").URPN.	USPAT	OR	OFF	2010/08/30 13:11

S48	27	("4030073" "4528634" "4811219" "4896289" "5070450" "5566325" "5583987" "5592616" "5608876" "5740399" "5742758" "5809531" "5835695" "5835784" "5842012" "5850152" "5854937" "5860021" "5892943" "5918047" "5987537" "5999989" "6009522" "6014744" "6101600" "6154838" "6216224").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/30 13:21
S49	1	("6401199").URPN.	USPAT	OR	OFF	2010/08/30 13:24
S50	2	((chang\$3 or alter\$5 or switch\$4 or enabl\$4 or assert\$4 or hold\$4 or disabl\$4 or control\$4) near3 (system adj (mode or state)))with (((microcontroller or micro\$controller)near3 access\$4)adj3 (non \$volatile or flash or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 09:58
S51	1593	((shar\$4 or access\$4) near3 (non\$volatile or memory or storage or ram or rom or sdram or dram))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:00
S52	2	S51 same ((chang\$3 or alter\$5 or switch\$4 or enabl\$4 or assert\$4 or hold\$4 or disabl\$4 or control\$4)near3 (system adj (mode or state)))with (((microcontroller or micro\$controller)near3 access\$4)adj3 (non \$volatile or flash or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:00

S53	2	S51 and ((chang\$3 or alter\$5 or switch\$4 or enabl\$4 or assert\$4 or hold\$4 or disabl\$4 or control\$4)near3 (system adj (mode or state)))with (((microcontroller or micro\$controller)near3 access\$4)adj3 (non \$volatile or flash or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:00
S54	2	S51 and ((chang\$3 or alter\$5 or switch\$4 or enabl\$4 or assert\$4 or hold\$4 or disabl\$4 or control\$4)near3 (system adj (mode or state))) same (((microcontroller or micro\$controller)near3 access\$4)adj3 (non \$volatile or flash or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:00
S55	8	"775281".ap.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:02
S56	4	("5819087" "5794054").pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:02
S57	39	S51 and (((upgrad\$4 or updat\$4 or writ\$4 or load\$4 or stor\$4 or sav\$3 or replac\$4)near3 (data or information or parameter \$1 or value\$1 or program or code or instruction\$1 or software or firmware))with (((microcontroller or micro\$controller)near3 access\$4)adj3 (memory or storage or non \$volatile or flash or rom)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:13

S58	27	S51 same (((upgrad\$4 or updat\$4 or writ\$4 or load\$4 or stor\$4 or sav\$3 or replac\$4)near3 (data or information or parameter\$1 or value\$1 or program or code or instruction\$1 or software or firmware))with (((microcontroller or micro\$controller)near3 access\$4)adj3 (memory or storage or non\$volatile or flash or rom)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:13
S59	46	S51 same (((upgrad\$4 or updat\$4 or writ\$4 or load\$4 or stor\$4 or sav\$3 or replac\$4)near3 (data or information or parameter\$1 or value\$1 or program or code or instruction\$1 or software or firmware))with (((microcontroller or micro\$controller)near3 access\$4)near33 (memory or storage or non\$volatile or flash or rom)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:25
S60	70	S51 and (((upgrad\$4 or updat\$4 or writ\$4 or load\$4 or stor\$4 or sav\$3 or replac\$4)near3 (data or information or parameter\$1 or value\$1 or program or code or instruction\$1 or software or firmware))with (((microcontroller or micro\$controller)near3 access\$4)near33 (memory or storage or non\$volatile or flash or rom)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:25

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S62	2	S59 and ((chang\$3 or alter\$5 or switch\$4 or enabl\$4 or assert\$4 or hold\$4 or disabl\$4 or control\$4)near3 (system adj (mode or state)))with (((microcontroller or micro\$controller)near3 access\$4)adj3 (non \$volatile or flash or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:26
S63	1593	((shar\$4 or access\$4) near3 (non\$volatile or memory or storage or ram or rom or sdram or dram))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 12:53
S64	70	S63 and (((upgrad\$4 or updat\$4 or writ\$4 or load \$4 or stor\$4 or sav\$3 or replac\$4)near3 (data or information or parameter \$1 or value\$1 or program or code or instruction\$1 or software or firmware))with (((microcontroller or micro\$controller)near3 access\$4)near33 (memory or storage or non\$volatile or flash or rom)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 12:53
S65	0	wo2006131134	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:05

S66	6	"2006131134"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:05
S67	5	"2005119184"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:09
S68	11	("5202687" "5630057" "5969632" "6009496" "6144327" "6219729" "6236593" "6324628" "6460172" "6754765" "6839774").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/31 13:11
S69	11	("5202687" "5630057" "5969632" "6009496" "6144327" "6219729" "6236593" "6324628" "6460172" "6754765" "6839774").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/31 13:15
S70	29	("6009496").URPN.	USPAT	OR	OFF	2010/08/31 13:15
S71	2	("6832285").URPN.	USPAT	OR	OFF	2010/08/31 13:22
S72	29	("6009496").URPN.	USPAT	OR	OFF	2010/08/31 13:23
S73	29808	((upgrad\$4 or updat\$4 or writ\$4 or load\$4 or stor\$4 or sav\$3 or replac \$4)near3 (data or information or parameter \$1 or value\$1 or program or code or instruction\$1 or software or firmware))with ((microcontroller or micro \$controller or micro \$processor)near3 (memory or storage or non\$volatile or flash or rom)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:24

S74	55485	((upgrad\$4 or updat\$4 or writ\$4 or load\$4 or stor\$4 or sav\$3 or replac\$4))with ((microcontroller or micro\$controller or micro\$processor)near3 (memory or storage or non\$volatile or flash or rom)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:26
S75	246	S73 and ((shar\$4 or access\$4) near3 (non\$volatile or memory or storage or ram or rom or sdram or dram))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:26
S76	21	S73 and ((shar\$4 or common) near3 (non\$volatile or memory or storage or ram or rom or sdram or dram))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:27
S77	28	S74 and ((shar\$4 or common) near3 (non\$volatile or memory or storage or ram or rom or sdram or dram))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:40
S78	0	("7761644").URPN.	USPAT	OR	OFF	2010/08/31 13:45
S79	13	("4881164" "5535417" "5592677" "5685005" "5727219" "5867726" "5903771" "5933855" "5974493" "6163828" "6353863" "6526462" "6601126").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/31 13:46
S80	26	("4881164").URPN.	USPAT	OR	OFF	2010/08/31 13:47
S81	10	("4177513" "4402046" "4512016" "4665483" "4777595" "4881164" "5077655" "5123101" "5214759" "5218684").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/31 13:50
S82	9	("5410655").URPN.	USPAT	OR	OFF	2010/08/31 13:50
S83	1	"6762635".PN.	USPAT	OR	OFF	2010/08/31 14:51

S84	14	((common or shar\$4) near3 (non\$volatile or flash or rom or sdram or eeprom or prom))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:17
S85	56	((common or shar\$4) near3 (non\$volatile or flash or rom or sdram or eeprom or prom))with (processor or cpu)with (microcontroller or micro \$controller or microprocessor or micro \$processor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:17
S86	1	S85 same ((safe or secur \$3)near2 access)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:18
S87	5	S85 and ((safe or secur \$3)near2 access)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:19
S88	2	(access\$4 or occup\$3 or master)near4((common or shar\$4) near3 (non \$volatile or flash or rom or sdram or eeprom or prom))with (processor or cpu)with microcontroller same (safe\$3 or (without adj (interruption or interference)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:34
S89	1	S85 same ((safe\$3 or (without adj (interruption or interference)))) near4 (occup\$4 or access)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:36
S90	2	S85 and ((safe\$3 or (without adj (interruption or interference)))) near4 (occup\$4 or access)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:36

S91	8	S85 and ((safe\$3 or (without adj (interruption or interference))))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:36
S92	798	(updat\$4 or upgrad\$4 or reprogram\$4)near6 ((rom or eeprom or flash or non\$volatile or memory)adj5 (microcontroller or micro\$controller or microprocessor or micro\$processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:50
S93	1244	(updat\$4 or upgrad\$4 or reprogram\$4)near6 ((rom or eeprom or flash or non\$volatile or memory)near4 (microcontroller or micro\$controller or microprocessor or micro\$processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:51
S94	3	S92 and ((common or shar\$4) near3 (non \$volatile or flash or rom or sdram or eeprom or prom))with (processor or cpu)with (microcontroller or micro\$controller or microprocessor or micro\$processor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:51
S95	6	S93 and ((common or shar\$4) near3 (non \$volatile or flash or rom or sdram or eeprom or prom))with (processor or cpu)with (microcontroller or micro\$controller or microprocessor or micro\$processor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:51
S96	0	S92 and (access\$4 or occup\$3 or master)near4 ((common or shar\$4) near3 (non\$volatile or flash or rom or sdram or eeprom or prom))with (processor or cpu)with microcontroller same (safe\$3 or (without adj (contention\$1 or interruption or interference)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 09:02

S97	0	S93 and (access\$4 or occup\$3 or master)near4 ((common or shar\$4) near3 (non\$volatile or flash or rom or sdram or eeprom or prom))with (processor or cpu)with microcontroller same (safe\$3 or (without adj (contention\$1 or interruption or interference))))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 09:02
S98	8	S93 and ((processor or cpu)with microcontroller same (safe\$3 or (without adj (contention\$1 or interruption or interference))))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 09:02
S99	7	S92 and ((processor or cpu)with microcontroller same (safe\$3 or (without adj (contention\$1 or interruption or interference))))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 09:03
S100	11	("6115814").URPN.	USPAT	OR	OFF	2010/09/01 09:10
S101	1	("6925522").URPN.	USPAT	OR	OFF	2010/09/01 09:13
S102	11	("20050163468" "20060013198" "5999476" "6523755" "6647439" "6785892" "6832269" "6891543" "6898678" "6925522" "7017038").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/09/01 09:14
S103	8	("5381540" "5446864" "5454114" "5455937" "5504903" "5825854" "5890003" "5914543").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/09/01 09:22

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	11958601
	Filing Date	2007-12-18
	First Named Inventor	Ian F. Harris
	Art Unit	2612
	Examiner Name	Unknown
	Attorney Docket Number	5707-16601

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/N.P./	2	5634004		1997-05-27	Gopinath, et al.			
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	Filing Date		2007-12-18
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	Art Unit	2612	
	Examiner Name	Unknown	
	Attorney Docket Number	5707-16601	

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Atty. Dkt. No: 5707-16601

Dear Sir or Madam:

This paper is submitted in response to the Office Action of September 3, 2010, to further highlight why the application is in condition for allowance.

Please amend the case as listed below.

IN THE CLAIMS:

The following listing of claims will replace all prior versions, and listings, of claims in the application.

1. (Currently Amended) A system, comprising:
a non-volatile memory;
a processor; and
a microcontroller coupled to the non-volatile memory and to the processor, wherein the microcontroller is configured to:
in response to a change in system state to a first state wherein the microcontroller is assured safe access to the non-volatile memory, hold the system in the first state and switch access to the non-volatile memory from the processor to the microcontroller;
while the system is held in the first state, fetch program instructions ~~or~~ data from the non-volatile memory and load the program instructions ~~or~~ data into a memory of the microcontroller; and
after the program instructions ~~or~~ data have been loaded, switch access to the non-volatile memory from the microcontroller to the processor, and release the system from the first state.
2. (Original) The system of claim 1, wherein the change in system state to the first state is performed by software.
3. (Original) The system of claim 1, wherein the first state comprises one or more of:
a power on reset (POR) state;
a system reset state; or
a sleep state.

4. (Currently Amended) The system of claim 1, wherein the program instructions ~~and~~ or data comprise firmware code ~~and~~ or data for the microcontroller.

5. (Original) The system of claim 1, the microcontroller is a peripheral device controller for a computer system.

6. (Currently Amended) A method for sharing a non-volatile memory between a processor and a microcontroller in a system, comprising:

in response to a change in system state to a first state wherein the microcontroller is assured safe access to the non-volatile memory, holding the system in the first state and switching access to the non-volatile memory from the processor to the microcontroller;

while the system is held in the first state, fetching program instructions ~~and~~ or data from the non-volatile memory and loading the program instructions ~~and~~ or data into a memory of the microcontroller; and

after the program instructions ~~and~~ or data have been loaded, switching access to the non-volatile memory from the microcontroller to the processor, and releasing the system from the first state.

7. (Original) The method of claim 6, wherein the change in system state to the first state is performed by software.

8. (Original) The method of claim 6, wherein the first state comprises one or more of:

a power on reset (POR) state;

a system reset state; or

a sleep state.

9. (Currently Amended) The method of claim 6, wherein the program instructions ~~and~~ or data comprise firmware code ~~and~~ or data for the microcontroller.

10. (Original) The method of claim 6, the microcontroller is a peripheral device controller for a computer system.

11. (Currently Amended) A system, comprising:
a non-volatile memory;
a processor; and
a microcontroller coupled to the non-volatile memory and to the processor, wherein the microcontroller is configured to:
in response to a power on reset, hold a system reset signal in a reset state, thereby prohibiting the processor from accessing the non-volatile memory;
while the system reset signal is held in the reset state, fetch program instructions ~~not~~ or data from the non-volatile memory and load the program instructions ~~not~~ or data into a memory of the microcontroller; and
after the program instructions ~~not~~ or data have been loaded, permit the processor in the system access to the non-volatile memory, and release the system reset signal from the reset state.

12. (Currently Amended) The system of claim 11, wherein the program instructions ~~not~~ or data comprise firmware code ~~and~~ or data for the microcontroller.

13. (Original) The system of claim 12, the microcontroller is a peripheral device controller for a computer system.

14. (Currently Amended) The system of claim 11, wherein the microcontroller is coupled to the non-volatile memory via a non-volatile memory bus, and wherein the microcontroller is operable to fetch the program instructions ~~not~~ or data from the non-volatile memory via the non-volatile memory bus.

15. (Original) The system of claim 14, wherein the microcontroller is coupled to the processor via a host memory bus, and wherein the microcontroller is operable to

switchably intercept or pass communications between the processor and the non-volatile memory.

16. (Currently Amended) The system of claim 15, wherein the microcontroller comprises or is coupled to a switch, interposed between the non-volatile memory bus and the host memory bus, wherein the switch is controllable by the microcontroller to switchably intercept or pass communications between the processor and the non-volatile memory.

17. (Currently Amended) A method for sharing a non-volatile memory between a processor and a microcontroller in a system, comprising:

in response to a power on reset, holding a system reset signal in a reset state, thereby prohibiting the processor from accessing the non-volatile memory;

while the system reset signal is held in the reset state, fetching program instructions ~~or~~ data from the non-volatile memory and loading the program instructions ~~or~~ data into a memory of the microcontroller; and

after the program instructions ~~or~~ data have been loaded, permitting the processor in the system access to the non-volatile memory, and releasing the system reset signal from the reset state.

18. (Currently Amended) The method of claim 17, wherein the program instructions ~~or~~ data comprise firmware code ~~and/or~~ data for the microcontroller.

19. (Original) The method of claim 17, the microcontroller is a peripheral device controller for a computer system.

20. (Original) The method of claim 17, wherein the microcontroller is coupled to the processor via a system reset bus, and wherein the microcontroller is operable to assert the system reset signal over the system reset bus.

21. (Currently Amended) The method of claim 17, wherein the microcontroller is coupled to the non-volatile memory via a non-volatile memory bus, and wherein the microcontroller is operable to fetch the program instructions ~~or~~ data from the non-volatile memory via the non-volatile memory bus.

22. (Original) The method of claim 21, wherein the microcontroller is coupled to the processor via a host memory bus, and wherein the microcontroller is operable switchably intercept or pass communications between the processor and the non-volatile memory.

23. (Original) The method of claim 22, wherein the microcontroller comprises or is coupled to a switch, interposed between the non-volatile memory bus and the host memory bus, wherein the switch is controllable by the microcontroller to switchably intercept or pass communications between the processor and the non-volatile memory

24. – 25 (Cancelled)

REMARKS

Applicant is in receipt of the Office Action mailed September 3, 2010. Claims 24 and 25 have been cancelled. Claims 1, 4, 6, 9, 11, 12, 14, 16, 17, 18, and 21 have been amended. Claims 1-23 are pending in the case. Reconsideration of the present case is earnestly requested in light of the following remarks.

Objections

Claim 16 was objected to for omitting a period, and has been amended accordingly. Applicant thus requests removal of the objection to this claim

Section 112 Rejections

Claims 1 - 23 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

More specifically, claims 1, 4, 6, 9, 11-12, and 17-18 were rejected for using a slash ("/"), which is intended to denote an "inclusive or", i.e., "any or all". Applicant has amended the claims to replace the slash (as well as the "and/" in any occurrences of "and/or", which Applicant respectfully notes is well understood to mean "inclusive or") with "or", which Applicant notes is intended to be inclusive (rather than exclusive).

Claims 24 and 25 have been cancelled.

Applicant thus respectfully requests removal of the section 112 rejection of the claims.

Section 102 Rejections

Claims 24 - 25 are rejected under 35 U.S.C. 102(b) as being clearly anticipated by Le et al. (hereinafter "Le"), US Patent 6,154,838. Applicant respectfully notes that these claims have been cancelled, thus rendering their rejections moot.

Removal of the section 102 rejection of the claims is earnestly requested.

Section 103 Rejections

Claims 1 - 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Le et al. (US Patent 6,154,838, “Le”), and further in view of Pang, (US Patent 6,925,522 B2). Applicant respectfully disagrees.

As the Examiner is certainly aware, to establish a prima facie obviousness of a claimed invention, all claim limitations must be taught or suggested by the prior art. In re Royka, 490 F.2d 981, 180 U.S.P.Q. 580 (C.C.P.A. 1974), MPEP 2143.03.

Amended claim 1 recites:

1. A system, comprising:
 - a non-volatile memory;
 - a processor; and
 - a microcontroller coupled to the non-volatile memory and to the processor, wherein the microcontroller is configured to:
 - in response to a change in system state to a first state wherein the microcontroller is assured safe access to the non-volatile memory, hold the system in the first state and switch access to the non-volatile memory from the processor to the microcontroller;
 - while the system is held in the first state, fetch program instructions or data from the non-volatile memory and load the program instructions or data into a memory of the microcontroller; and
 - after the program instructions or data have been loaded, switch access to the non-volatile memory from the microcontroller to the processor, and release the system from the first state.

Applicant respectfully notes that in claim 1, the microcontroller switches access to the non-volatile memory from the processor to itself, loads instructions from the non-volatile memory into a memory of the microcontroller, then switches the access back to the processor.

In contrast, in Le, the microcontroller boots up, checks that flash ROM is not corrupted via a checksum, then releases the flash ROM to the microprocessor and goes to

sleep. The microprocessor then boots (using the checked flash ROM), and wakes the microcontroller from sleep.

Thus, an important point of distinction is that in Le the microcontroller never switches access from the microprocessor to itself to load instructions, but rather, starts out with the access and just checks or updates the firmware (“The arbiter assigns the flash ROM initially to the microcontroller when power is initially provided to the system. After the flash ROM boots up and checks the integrity of the flash ROM and updates the content of the flash ROM with valid firmware if necessary, the microcontroller releases the flash ROM to the microprocessor to enable the computer system to proceed with the normal boot-up process.” (Abstract).

In other words, Le's microcontroller *starts out with access*, and just confirms or updates the firmware, which Applicant notes is actually for the *microprocessor* to boot from, and is never loaded into the microcontroller's memory, then switches access to the microprocessor to boot from the checked/updated firmware, whereas in claim 1, the access starts out with the processor, and the microcontroller switches access to itself, loads instructions into its own memory, then switches access back to the microprocessor.

Pang teaches changing codes in the flash memory of a micro-controller, and doesn't appear to be germane to the subject matter of claim 1. More specifically, the flash memory of the micro-controller stores a “renovation program” and a “general program”, where the renovation program in the flash memory is executed by the micro-controller to copy the renovation program to a static random access memory (SRAM), then the micro-controller executes the moved renovation program (in the SRAM) to replace the general program in the flash memory with a new program. Nowhere does Pang disclose that the micro-controller switches access to the flash memory from the processor to itself, loads instructions from the non-volatile memory into a memory of the microcontroller, then switches the access back to the processor

More specifically, nowhere does the cited art teach **in response to a change in system state to a first state wherein the microcontroller is assured safe access to the non-volatile memory, hold the system in the first state and switch access to the non-volatile memory from the processor to the microcontroller**, as recited in claim 1.

Applicant has carefully reviewed the citations of col. 3, lines 50 - 67, col. 4, lines 1 - 31, col. 12, lines 8 - 58, col. 13, lines 33 - 67, col. 14, lines 1 - 42, col. 15, lines 1 - 67, col. 16, lines 8 - 67, col. 17, lines 1 - 49, col. 18, and lines 6 - 16, fig. 1 - 8, and can find no description of the microcontroller holding the system in a first state wherein the microcontroller is assured safe access to the non-volatile memory, and the microcontroller switching access to the non-volatile memory *from the processor to the microcontroller*.

In fact, Le is quite clear that initially the microcontroller, not the processor, has access to the flash ROM, as disclosed in the Abstract, which reads:

The arbiter assigns the flash ROM initially to the microcontroller when power is initially provided to the system. After the flash ROM boots up and checks the integrity of the flash ROM and updates the content of the flash ROM with valid firmware if necessary, the microcontroller releases the flash ROM to the microprocessor to enable the computer system to proceed with the normal boot-up process. (*emphasis added*)

Thus, Le fails to teach or suggest these features. Nor does Pang remedy this deficiency of Le.

Thus, the cited art fails to disclose these features of claim 1.

Nor does the cited art disclose **while the system is held in the first state, fetch program instructions or data from the non-volatile memory and load the program instructions or data into a memory of the microcontroller**, as recited in claim 1.

The Office Action admits that Le fails to disclose this feature, but asserts that Pang remedies this admitted deficiency of Le, citing col. 1, lines 14 - 19, col. 2, lines 37 - 67, col. 3, lines 1 - 67, col. 5, lines 1 - 47, and fig. 2 - 11. This is incorrect.

These citations disclose a micro-controller replacing a “general program” in a flash memory by copying a new program from SRAM (volatile memory) to flash memory (non-volatile memory). In other words, in Pang’s system, the micro-controller specifically does not “fetch program instructions or data from the non-volatile memory and load the program instructions or data into a memory of the microcontroller”, but rather, appears to do the opposite, thus teaching away from claim 1.

Additionally, as noted above, Pang does not appear to be related to switching access to non-volatile memory between a microcontroller and a processor at all, and so is not relevant to the subject matter of claim 1, and thus not properly combinable with Le to make a prima facie case of obviousness.

Applicant respectfully reminds the Examiner that per *Akzo N.V. v. United States Int'l Trade Comm'n*, 1 USPQ 2d 1241, 1246 (Fed. Cir. 1986), cert. denied, 482 U.S. 909 (1987), [P]rior art references ... must be read as a whole and consideration must be given where the references diverge and teach away from the claimed invention...Moreover, appellants cannot pick and choose among individual parts of assorted prior art references “as a mosaic to recreate a facsimile of the claimed invention.”

Applicant respectfully submits that the Examiner has improperly attempted to assemble Applicant's claimed invention by selecting disparate elements from multiple references out of context using Applicant's claim as a blueprint.

Moreover, Applicant respectfully submits that even were Le and Pang properly combinable, which Applicant argues they are not, the resulting combination would still not produce Applicant's invention as recited in claim 1, as explained in detail above.

Thus, for at least the above reasons, Applicant submits that the cited art, taken singly or in combination, fails to teach or suggest all the features and limitations of claim 1, and so claim 1, and those claims respectively dependent therefrom, are patentably distinct and non-obvious over the cited art, and are thus allowable.

Independent claim 6 includes similar limitations as claim 1, and so the above arguments apply with equal force to this claim. Thus, for at least the reasons provided above, Applicant submits that claim 6, and those claims respectively dependent therefrom, are patentably distinct and non-obvious over the cited art, and are thus allowable.

Nor does the cited art disclose a microcontroller configured to **while the system reset signal is held in the reset state, fetch program instructions or data from the non-volatile memory and load the program instructions or data into a memory of the microcontroller**, as recited in claim 11.

The Office Action admits that Le fails to disclose this feature, but asserts that Pang remedies this admitted deficiency of Le, citing col. 1, lines 14 - 19, col. 2, lines 37 - 67, col. 3, lines 1 - 67, col. 5, lines 1 - 47, and fig. 2 - 11.

As discussed above, these citations disclose a micro-controller replacing a “general program” in a flash memory by copying a new program from SRAM (volatile memory) to flash memory (non-volatile memory). In other words, in Pang’s system, the micro-controller specifically does not “fetch program instructions or data from the non-volatile memory and load the program instructions or data into a memory of the microcontroller”, but rather, appears to do the opposite, thus teaching away from claim 11.

Additionally, as also noted above, Pang does not appear to be related to switching access to non-volatile memory between a microcontroller and a processor at all, and so is not relevant to the subject matter of claim 11, and thus not properly combinable with Le to make a prima facie case of obviousness.

Applicant respectfully submits that the Examiner has improperly attempted to assemble Applicant’s claimed invention by selecting disparate elements from multiple references out of context using Applicant’s claim as a blueprint.

Moreover, Applicant respectfully submits that even were Le and Pang properly combinable, which Applicant argues they are not, the resulting combination would still not produce Applicant’s invention as recited in claim 11, as explained in detail above.

Thus, for at least the above reasons, Applicant submits that the cited art, taken singly or in combination, fails to teach or suggest all the features and limitations of claim 11, and so claim 11, and those claims respectively dependent therefrom, are patentably distinct and non-obvious over the cited art, and are thus allowable.

Independent claim 17 includes similar limitations as claim 11, and so the above arguments apply with equal force to this claim. Thus, for at least the reasons provided above, Applicant submits that claim 17, and those claims respectively dependent therefrom, are patentably distinct and non-obvious over the cited art, and are thus allowable.

Applicant also asserts that numerous ones of the dependent claims recite further distinctions over the cited art. However, since the independent claims have been shown

to be patentably distinct, a further discussion of the dependent claims is not necessary at this time.

Removal of the section 103 rejection of the claims is earnestly requested.

CONCLUSION

Applicant submits the application is in condition for allowance, and an early notice to that effect is requested.

If any extensions of time (under 37 C.F.R. § 1.136) are necessary to prevent the above-referenced application(s) from becoming abandoned, Applicant(s) hereby petition for such extensions. The Commissioner is hereby authorized to charge any fees which may be required or credit any overpayment to Meyertons, Hood, Kivlin, Kowert & Goetzel P.C., Deposit Account No. 50-1505/5707-16601/JCH.

Also filed herewith are the following items:

- ☐ Request for Continued Examination
- ☐ Terminal Disclaimer
- ☐ Power of Attorney By Assignee and Revocation of Previous Powers
- ☐ Notice of Change of Address
- ☐ Other:

Respectfully submitted,

/Jeffrey C. Hood/

Jeffrey C. Hood, Reg. #35198
ATTORNEY FOR APPLICANT(S)

Meyertons, Hood, Kivlin, Kowert & Goetzel PC
P.O. Box 398
Austin, TX 78767-0398
Phone: (512) 853-8800
Date: 2010-12-03 JCH/MSW

Electronic Acknowledgement Receipt	
EFS ID:	8966993
Application Number:	11958601
International Application Number:	
Confirmation Number:	1387
Title of Invention:	Sharing Non-Sharable Devices Between an Embedded Controller and A Processor in a Computer System
First Named Inventor/Applicant Name:	Ian F. Harris
Correspondence Address:	Jeffrey C. Hood Meyertons Hood Kivlin Kowert & Goetzel PC P.O. Box 398 - Austin TX 78767-0398 US 5128538800 -
Filer:	Jeffrey C Hood/Jeannie Miranda
Filer Authorized By:	Jeffrey C Hood
Attorney Docket Number:	5707-16601
Receipt Date:	03-DEC-2010
Filing Date:	18-DEC-2007
Time Stamp:	18:25:52
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no
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File Listing:

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)		
1		5707-16601_Resp_OA_2010-09-03.pdf	126532 b62cb17e3f0ef7678af34622b321ca21a16f9cb7	yes	14		
Multipart Description/PDF files in .zip description							
	Document Description	Start	End				
	Amendment/Req. Reconsideration-After Non-Final Reject	1	1				
	Claims	2	6				
	Applicant Arguments/Remarks Made in an Amendment	7	14				
Warnings:							
Information:							
Total Files Size (in bytes):			126532				
<p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p>							

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

PATENT APPLICATION FEE DETERMINATION RECORD Substitute for Form PTO-875					Application or Docket Number 11/958,601		Filing Date 12/18/2007		<input type="checkbox"/> To be Mailed	
APPLICATION AS FILED – PART I										
(Column 1)			(Column 2)			SMALL ENTITY <input type="checkbox"/> OR		OTHER THAN SMALL ENTITY		
FOR	NUMBER FILED	NUMBER EXTRA	RATE (\$)	FEE (\$)	OR	RATE (\$)	FEE (\$)			
<input type="checkbox"/> BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A	N/A			N/A				
<input type="checkbox"/> SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A	N/A			N/A				
<input type="checkbox"/> EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A	N/A			N/A				
TOTAL CLAIMS (37 CFR 1.16(i))	minus 20 =	*	X \$ =		OR	X \$ =				
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*	X \$ =			X \$ =				
<input type="checkbox"/> APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$250 (\$125 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).									
<input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))										
* If the difference in column 1 is less than zero, enter "0" in column 2.										
APPLICATION AS AMENDED – PART II										
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	12/03/2010	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)	
Total (37 CFR 1.16(i))	* 23	Minus	** 25	= 0	X \$ =		OR	X \$52=	0	
Independent (37 CFR 1.16(h))	* 4	Minus	***6	= 0	X \$ =		OR	X \$220=	0	
<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))										
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE	0	
(Column 1)			(Column 2)			SMALL ENTITY OR		OTHER THAN SMALL ENTITY		
AMENDMENT	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)	ADDITIONAL FEE (\$)	OR	RATE (\$)	ADDITIONAL FEE (\$)		
Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =		OR	X \$ =		
Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =		OR	X \$ =		
<input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))										
<input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))										
					TOTAL ADD'L FEE		OR	TOTAL ADD'L FEE		
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.										

Legal Instrument Examiner:
/BRENDA HARRISON/

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
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Alexandria, Virginia 22313-1450
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

7590 12/17/2010

Jeffrey C. Hood
Meyertons Hood Kivlin Kowert & Goetzel PC
P.O. Box 398
Austin, TX 78767-0398

EXAMINER

PATEL, NITIN C

ART UNIT

PAPER NUMBER

2116

DATE MAILED: 12/17/2010

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/958,601	12/18/2007	Ian F. Harris	5707-16601	1387

TITLE OF INVENTION: SHARING NON-SHARABLE DEVICES BETWEEN AN EMBEDDED CONTROLLER AND A PROCESSOR IN A COMPUTER SYSTEM

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	03/17/2011

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.

B. If the status above is to be removed, check box 5b on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above, or

If the SMALL ENTITY is shown as NO:

A. Pay TOTAL FEE(S) DUE shown above, or

B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check box 5a on Part B - Fee(s) Transmittal and pay the PUBLICATION FEE (if required) and 1/2 the ISSUE FEE shown above.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

7590 12/17/2010

Jeffrey C. Hood
Meyertons Hood Kivlin Kowert & Goetzel PC
P.O. Box 398
Austin, TX 78767-0398

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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11/958,601	12/18/2007	Ian F. Harris	5707-16601	1387
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TITLE OF INVENTION: SHARING NON-SHARABLE DEVICES BETWEEN AN EMBEDDED CONTROLLER AND A PROCESSOR IN A COMPUTER SYSTEM

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	03/17/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
PATEL, NITIN C	2116	713-323000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, 1 _____
- (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 _____
- 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The Director is hereby authorized to charge the required fee(s), any deficiency, or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ a. Applicant claims SMALL ENTITY status. See 37 CFR 1.27. ☐ b. Applicant is no longer claiming SMALL ENTITY status. See 37 CFR 1.27(g)(2).

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

Authorized Signature _____

Date _____

Typed or printed name _____

Registration No. _____

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/958,601	12/18/2007	Ian F. Harris	5707-16601	1387
7590 12/17/2010				
Jeffrey C. Hood Meyertons Hood Kivlin Kowert & Goetzel PC P.O. Box 398 Austin, TX 78767-0398			EXAMINER PATEL, NITIN C	
			ART UNIT	PAPER NUMBER
			2116	
DATE MAILED: 12/17/2010				

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment to date is 562 day(s). If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the Patent Term Adjustment will be 562 day(s).

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

<i>Search Notes</i> *1195860 1*	Application/Control No. 11958601	Applicant(s)/Patent Under Reexamination HARRIS ET AL.
	Examiner NITIN C PATEL	Art Unit 2116

SEARCHED			
Class	Subclass	Date	Examiner
713	324, 2, 100	1/15/102	ncp

SEARCH NOTES		
Search Notes	Date	Examiner
Inventor name search in PALM	8/26/10	ncp
EAST search results attached	8/26/10,8/30/10, 8/31/10,9/1/10	ncp
Updated EAST search results attached	12/15/10	ncp
Class subclass with text search results ---attached 713/324, 2,100	12/15/10	ncp
NPL search -- ACM Digital library, IEEE explorer results attached	12/0/109	ncp

INTERFERENCE SEARCH			
Class	Subclass	Date	Examiner
713	324, 2, 100	12/15/10	ncp

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EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L30	534	(system or apparatus or comput\$4) same ((microcontroller or uc or micro\$controller or up or micro\$processor)near6 ((built\$3 or coupl\$4 or connect\$4 or communicat\$4 or joined or attach\$3) adj4 (non\$volatile or flash or dram or sdram or rom)))same (CPU or processor or (process\$4 adj (logic or unit or circuit)))and (((saf\$3 or secur\$4)adj2 access or read\$3 or writ\$4))with (non\$volatile or flash or dram or sdram or rom)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:05
L31	2	l30 and (((load\$4 or stor\$4 or sav\$4 or writ\$4) near3 (program or code or instruction\$1 or command or data or information))with ((microcontroller or uc) adj2 (memory or storage or memory)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:08
L32	131	("5768574" "5944816" "5805840" "5761452"), pn."	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:13
L33	131	("5768574" "5944816" "5805840" "5761452"). pn."	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:13
L34	4	("5768574" "5944816" "5805840" "5761452"). pn."	USPAT	OR	OFF	2010/12/15 08:14

L35	2	(system or apparatus or comput\$4) same ((microcontroller or uc or micro\$controller or up or micro\$processor)near6 ((built\$3 or coupl\$4 or connect\$4 or communicat\$4 or joined or attach\$3) adj4 (non\$volatile or flash or dram or sdram or rom)))same (CPU or processor or (process\$4 adj (logic or unit or circuit)))and (((saf\$3 or secur\$4)adj2 access or read\$3 or writ\$4))with (non\$volatile or flash or dram or sdram or rom) and (((load\$4 or stor\$4 or sav\$4 or writ\$4)near3 (program or code or instruction\$1 or command or data or information))with ((microcontroller or uc) adj2 (memory or storage or memory)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:16
L36	1	(system or apparatus or comput\$4) same ((microcontroller or uc or micro\$controller or up or micro\$processor)near6 ((built\$3 or coupl\$4 or connect\$4 or communicat\$4 or joined or attach\$3) adj4 (non\$volatile or flash or dram or sdram or rom)))same (CPU or processor or (process\$4 adj (logic or unit or circuit)))and (((saf\$3 or secur\$4)adj2 access or read\$3 or writ\$4))with (non\$volatile or flash or dram or sdram or rom) and (((load\$4 or stor\$4 or sav\$4 or writ\$4)near3 (program or code or instruction\$1 or command or data or information))with ((microcontroller or uc) adj2 (memory or storage or memory))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:16

L39	0	("20050228993").pn.	USPAT	OR	OFF	2010/12/15 08:22
L40	1	("20050228993").pn.	US-PGPUB; USPAT	OR	OFF	2010/12/15 08:22
L41	2	("20050228993" "20020166059").pn.	US-PGPUB; USPAT	OR	OFF	2010/12/15 08:23
L42	29	(hold\$4 or delay\$4 or paus\$3 or disabl\$4 or decoupl\$4 or disconnect \$4)near4 (por or (power adj3 reset) or (system adj reset) or (sleep adj (state or mode))) same (((fetch\$4 or access\$4 or read\$4 or load\$4 or writ \$4 or sav\$3)near6 (code or software or firmware or program or instruction \$1 or data))with (non \$volatile or flash or sdram or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:39
L43	31	(hold\$4 or delay\$4 or paus\$3 or disabl\$4 or decoupl\$4 or disconnect \$4)near4 (por or (power adj3 reset) or (system adj reset) or (sleep adj (state or mode))) same (((copy\$3 or copi\$3 or fetch\$4 or access\$4 or read\$4 or load\$4 or writ \$4 or sav\$3)near6 (code or software or firmware or program or instruction \$1 or data))with (non \$volatile or flash or sdram or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:40
L44	11	l43 same (microcontroller or uc or micro\$controller or up or micro \$processor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:41
L45	1	("6401199").pn.	USPAT	OR	OFF	2010/12/15 08:53

L46	27	("4030073" "4528634" "4811219" "4896289" "5070450" "5566325" "5583987" "5592616" "5608876" "5740399" "5742758" "5809531" "5835695" "5835784" "5842012" "5850152" "5854937" "5860021" "5892943" "5918047" "5987537" "5999989" "6009522" "6014744" "6101600" "6154838" "6216224").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/12/15 08:53
L47	134	("5608876").URPN.	USPAT	OR	OFF	2010/12/15 09:00
L48	1	("6401199").URPN.	USPAT	OR	OFF	2010/12/15 09:06
L49	12	("6330667").URPN.	USPAT	OR	OFF	2010/12/15 09:08
L50	21	("20010044875" "5163145" "5423029" "5454117" "5559753" "5592616" "5611063" "5740417" "5768576" "5799179" "5812491" "5815699" "5864692" "5926831" "5941980" "5948095" "6098166" "6216224" "6253288" "6330667" "6338133"). PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/12/15 09:09
L51	2	("6766447").URPN.	USPAT	OR	OFF	2010/12/15 09:11
L52	12	("6216224").URPN.	USPAT	OR	OFF	2010/12/15 09:12
L53	7	("5859987" "5898869" "5925099" "6122746" "6216224" "6292409" "6611882").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/12/15 09:19
L54	12	("6216224").URPN.	USPAT	OR	OFF	2010/12/15 09:21
L55	1	("7464259").URPN.	USPAT	OR	OFF	2010/12/15 09:22
L56	13	("5455918" "5809531" "6185134" "6216224" "6263399" "6356965" "6601167" "7000846" "7082525" "7165137" "7234049" "7234052" "7340566").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/12/15 09:22

L57	7	("5859987" "5898869" "5925099" "6122746" "6216224" "6292409" "6611882").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/12/15 09:26
L58	0	("7290127").URPN.	USPAT	OR	OFF	2010/12/15 09:26
L59	7	("4943911" "5546355" "5572468" "5754863" "5898869" "6216224" "6400717").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/12/15 09:27
L60	2	("7032106").URPN.	USPAT	OR	OFF	2010/12/15 09:28
L61	5	("6925522" "5819087" "5949997" "7386326" "5428760").pn.	USPAT	OR	OFF	2010/12/15 09:35
L62	84354	"713"/("323" "1" "2" "100").ccls.	USPAT	OR	OFF	2010/12/15 09:36
L63	54685	"713"/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 09:36
L64	131319	"713"/("323" "1" "2" "100").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 09:37
L65	2	l63 and (system or apparatus or comput\$4) same((microcontroller or uc or micro\$controller or up or micro\$processor) near6 ((built\$3 or coupl \$4 or connect\$4 or communicat\$4 or joined or attach\$3)adj4 (non \$volatile or flash or dram or sdram or rom)))same (CPU or processor or (process\$4 adj (logic or unit or circuit)))and (((saf \$3 or secur\$4)adj2 access or read\$3 or writ \$4))with (non\$volatile or flash or dram or sdram or rom)and (((load\$4 or stor\$4 or sav\$4 or writ\$4) near3 (program or code or instruction\$1 or command or data or information))with	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 09:37

		((microcontroller or uc) adj2 (memory or storage or memory)))				
L66	0	l64 and (system or apparatus or comput\$4) same((microcontroller or uc or micro\$controller or up or micro\$processor) near6 ((built\$3 or coupl \$4 or connect\$4 or communicat\$4 or joined or attach\$3)adj4 (non \$volatile or flash or dram or sdram or rom)))same (CPU or processor or (process\$4 adj (logic or unit or circuit)))and (((saf \$3 or secur\$4)adj2 access or read\$3 or writ \$4))with (non\$volatile or flash or dram or sdram or rom)and (((load\$4 or stor\$4 or sav\$4 or writ\$4) near3 (program or code or instruction\$1 or command or data or information))with ((microcontroller or uc) adj2 (memory or storage or memory)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 09:37
L67	1	((after or finish\$4 or complet\$4)near4 (copi\$3 or copy\$4 or load\$4 or sav\$4 or writ\$4 or stor\$4) near3 (program or code or instruction\$4 or firmware or software)) with (releas\$4 near3 (system adj reset))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 09:44
L68	1	((after or finish\$4 or complet\$4)near4 (copi\$3 or copy\$4 or load\$4 or sav\$4 or writ\$4 or stor\$4) near3 (program or code or instruction\$4 or firmware or software or data or information)) with (releas\$4 near3 (system adj reset))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 09:45

EAST Search History (I nterference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
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L37	1	(system or apparatus or comput\$4) same ((microcontroller or uc or micro\$controller or up or micro\$processor)near6 ((built\$3 or coupl\$4 or connect\$4 or communicat\$4 or joined or attach\$3) adj4 (non\$volatile or flash or dram or sdram or rom))) same (CPU or processor or (process\$4 adj (logic or unit or circuit)))and (((saf\$3 or secur\$4)adj2 access or read\$3 or writ\$4))with (non\$volatile or flash or dram or sdram or rom)and (((load\$4 or stor\$4 or sav\$4 or writ\$4)near3 (program or code or instruction\$1 or command or data or information)) with ((microcontroller or uc)adj2 (memory or storage or memory))).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2010/12/15 08:16
L38	2	(system or apparatus or comput\$4) same ((microcontroller or uc or micro\$controller or up or micro\$processor)near6 ((built\$3 or coupl\$4 or connect\$4 or communicat\$4 or joined or attach\$3) adj4 (non\$volatile or flash or dram or sdram or rom))) same (CPU or processor or (process\$4 adj (logic or unit or circuit)))and (((saf\$3 or secur\$4)adj2 access or read\$3 or writ\$4))with (non\$volatile or flash or dram or sdram or rom)and (((load\$4 or stor\$4 or sav\$4 or writ\$4)near3 (program or code or instruction\$1 or command or data or information)) with ((microcontroller or uc)adj2 (memory or storage or memory))).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2010/12/15 08:17

12/15/2010 9:46:52 AM

C:\Documents and Settings\npatel3\My Documents\EAST\Workspaces\11958601.wsp

EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L30	534	(system or apparatus or comput\$4) same ((microcontroller or uc or micro\$controller or up or micro\$processor)near6 ((built\$3 or coupl\$4 or connect\$4 or communicat\$4 or joined or attach\$3) adj4 (non\$volatile or flash or dram or sdram or rom)))same (CPU or processor or (process\$4 adj (logic or unit or circuit)))and (((saf\$3 or secur\$4)adj2 access or read\$3 or writ\$4))with (non\$volatile or flash or dram or sdram or rom)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:05
L31	2	I30 and ((load\$4 or stor\$4 or sav\$4 or writ\$4) near3 (program or code or instruction\$1 or command or data or information))with ((microcontroller or uc) adj2 (memory or storage or memory)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:08
L32	131	("5768574" "5944816" "5805840" "5761452"), pn."	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:13
L33	131	("5768574" "5944816" "5805840" "5761452"). pn."	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:13
L34	4	("5768574" "5944816" "5805840" "5761452"). pn.	USPAT	OR	OFF	2010/12/15 08:14

L35	2	(system or apparatus or comput\$4) same ((microcontroller or uc or micro\$controller or up or micro\$processor)near6 ((built\$3 or coupl\$4 or connect\$4 or communicat\$4 or joined or attach\$3) adj4 (non\$volatile or flash or dram or sdram or rom)))same (CPU or processor or (process\$4 adj (logic or unit or circuit)))and (((saf\$3 or secur\$4)adj2 access or read\$3 or writ\$4))with (non\$volatile or flash or dram or sdram or rom) and (((load\$4 or stor\$4 or sav\$4 or writ\$4)near3 (program or code or instruction\$1 or command or data or information))with ((microcontroller or uc) adj2 (memory or storage or memory)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:16
L36	1	(system or apparatus or comput\$4) same ((microcontroller or uc or micro\$controller or up or micro\$processor)near6 ((built\$3 or coupl\$4 or connect\$4 or communicat\$4 or joined or attach\$3) adj4 (non\$volatile or flash or dram or sdram or rom)))same (CPU or processor or (process\$4 adj (logic or unit or circuit)))and (((saf\$3 or secur\$4)adj2 access or read\$3 or writ\$4))with (non\$volatile or flash or dram or sdram or rom) and (((load\$4 or stor\$4 or sav\$4 or writ\$4)near3 (program or code or instruction\$1 or command or data or information))with ((microcontroller or uc) adj2 (memory or storage or memory))).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:16
L39	0	("20050228993").pn.	USPAT	OR	OFF	2010/12/15 08:22

L40	1	("20050228993").pn.	US-PGPUB; USPAT	OR	OFF	2010/12/15 08:22
L41	2	("20050228993" "20020166059").pn.	US-PGPUB; USPAT	OR	OFF	2010/12/15 08:23
L42	29	(hold\$4 or delay\$4 or paus\$3 or disabl\$4 or decoupl\$4 or disconnect \$4)near4 (por or (power adj3 reset) or (system adj reset) or (sleep adj (state or mode))) same (((fetch \$4 or access\$4 or read\$4 or load\$4 or writ\$4 or sav \$3)near6 (code or software or firmware or program or instruction\$1 or data))with (non \$volatile or flash or sdram or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:39
L43	31	(hold\$4 or delay\$4 or paus\$3 or disabl\$4 or decoupl\$4 or disconnect \$4)near4 (por or (power adj3 reset) or (system adj reset) or (sleep adj (state or mode))) same (((copy \$3 or copi\$3 or fetch\$4 or access\$4 or read\$4 or load\$4 or writ\$4 or sav\$3) near6 (code or software or firmware or program or instruction\$1 or data)) with (non\$volatile or flash or sdram or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:40
L44	11	l43 same (microcontroller or uc or micro\$controller or up or micro\$processor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 08:41
L45	1	("6401199").pn.	USPAT	OR	OFF	2010/12/15 08:53

L46	27	("4030073" "4528634" "4811219" "4896289" "5070450" "5566325" "5583987" "5592616" "5608876" "5740399" "5742758" "5809531" "5835695" "5835784" "5842012" "5850152" "5854937" "5860021" "5892943" "5918047" "5987537" "5999989" "6009522" "6014744" "6101600" "6154838" "6216224").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/12/15 08:53
L47	134	("5608876").URPN.	USPAT	OR	OFF	2010/12/15 09:00
L48	1	("6401199").URPN.	USPAT	OR	OFF	2010/12/15 09:06
L49	12	("6330667").URPN.	USPAT	OR	OFF	2010/12/15 09:08
L50	21	("20010044875" "5163145" "5423029" "5454117" "5559753" "5592616" "5611063" "5740417" "5768576" "5799179" "5812491" "5815699" "5864692" "5926831" "5941980" "5948095" "6098166" "6216224" "6253288" "6330667" "6338133").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/12/15 09:09
L51	2	("6766447").URPN.	USPAT	OR	OFF	2010/12/15 09:11
L52	12	("6216224").URPN.	USPAT	OR	OFF	2010/12/15 09:12
L53	7	("5859987" "5898869" "5925099" "6122746" "6216224" "6292409" "6611882").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/12/15 09:19
L54	12	("6216224").URPN.	USPAT	OR	OFF	2010/12/15 09:21
L55	1	("7464259").URPN.	USPAT	OR	OFF	2010/12/15 09:22
L56	13	("5455918" "5809531" "6185134" "6216224" "6263399" "6356965" "6601167" "7000846" "7082525" "7165137" "7234049" "7234052" "7340566").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/12/15 09:22

L57	7	("5859987" "5898869" "5925099" "6122746" "6216224" "6292409" "6611882").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/12/15 09:26
L58	0	("7290127").URPN.	USPAT	OR	OFF	2010/12/15 09:26
L59	7	("4943911" "5546355" "5572468" "5754863" "5898869" "6216224" "6400717").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/12/15 09:27
L60	2	("7032106").URPN.	USPAT	OR	OFF	2010/12/15 09:28
L61	5	("6925522" "5819087" "5949997" "7386326" "5428760").pn.	USPAT	OR	OFF	2010/12/15 09:35
L62	84354	"713"/("323" "1" "2" "100").ccls.	USPAT	OR	OFF	2010/12/15 09:36
L63	54685	"713"/\$.ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 09:36
L64	131319	"713"/("323" "1" "2" "100").ccls.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 09:37
L65	2	l63 and (system or apparatus or comput\$4) same((microcontroller or uc or micro\$controller or up or micro\$processor) near6 ((built\$3 or coupl \$4 or connect\$4 or communicat\$4 or joined or attach\$3)adj4 (non \$volatile or flash or dram or sdram or rom)))same (CPU or processor or (process\$4 adj (logic or unit or circuit)))and (((saf \$3 or secur\$4)adj2 access or read\$3 or writ \$4))with (non\$volatile or flash or dram or sdram or rom)and (((load\$4 or stor \$4 or sav\$4 or writ\$4) near3 (program or code or instruction\$1 or command or data or information))with ((microcontroller or uc)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 09:37

		adj2 (memory or storage or memory)))				
L66	0	l64 and (system or apparatus or comput\$4) same((microcontroller or uc or micro\$controller or up or micro\$processor) near6 ((built\$3 or coupl \$4 or connect\$4 or communicat\$4 or joined or attach\$3)adj4 (non \$volatile or flash or dram or sdram or rom)))same (CPU or processor or (process\$4 adj (logic or unit or circuit)))and (((saf \$3 or secur\$4)adj2 access or read\$3 or writ \$4))with (non\$volatile or flash or dram or sdram or rom)and (((load\$4 or stor \$4 or sav\$4 or writ\$4) near3 (program or code or instruction\$1 or command or data or information))with ((microcontroller or uc) adj2 (memory or storage or memory)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 09:37
L67	1	((after or finish\$4 or complet\$4)near4 (copi\$3 or copy\$4 or load\$4 or sav \$4 or writ\$4 or stor\$4) near3 (program or code or instruction\$4 or firmware or software)) with (releas\$4 near3 (system adj reset))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 09:44
L68	1	((after or finish\$4 or complet\$4)near4 (copi\$3 or copy\$4 or load\$4 or sav \$4 or writ\$4 or stor\$4) near3 (program or code or instruction\$4 or firmware or software or data or information)) with (releas\$4 near3 (system adj reset))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/12/15 09:45
S1	2	("5634004" "5925097"). PN.	USPAT	OR	OFF	2010/08/26 15:54

S2	55	((shar\$4 near3 (non\$volatile or memory or storage or ram or rom or sdram or dram))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 15:58
S3	1592	((shar\$4 or access\$4) near3 (non\$volatile or memory or storage or ram or rom or sdram or dram))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 15:59
S4	1	S3 same((hold\$4 or disabl\$4 or control\$4)near3 (system adj reset))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:00
S5	1739	((hold\$4 or disabl\$4 or control\$4)near3 (system adj reset))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:01
S6	1739	((hold\$4 or disabl\$4 or control\$4)near3 (system adj reset))with reset	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:01
S7	24	((hold\$4 or disabl\$4 or control\$4)near3 (system adj reset))with (reset adj state)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:02
S8	82	S3 same embedded	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:08
S9	9	("5949997").URPN.	USPAT	OR	OFF	2010/08/26 16:10
S10	3	("4665536" "5228066" "5521848").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/26 16:11

S11	14	("5623503" "5673276" "5774477" "5935266" "6108807" "6124715" "6378094" "6584590" "6983441" "7017081" "7080789" "7149943" "7251763" "7451367"). PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/26 16:13
S12	3	S3 same (embedded adj controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:18
S13	6	S3 same (embedded near3 controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:19
S14	24	S6 and ((hold\$4 or disabl \$4 or control\$4)near3 (system adj reset))with (reset adj state)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:20
S15	2	S14 and (embedded adj controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/26 16:21
S16	9	("5949997").URPN.	USPAT	OR	OFF	2010/08/26 16:23
S17	65	(shar\$4 near3 (non \$volatile or memory or storage or rom or sdram or dram))with (processor or cpu)with (microcontroller or micro \$controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:51
S18	3	S17 same embedded	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:51

S19	1	(shar\$4 near3 ((non \$volatile or rom or sdram or dram)adj2 (device or apparatus or memory or storage)))with (processor or cpu)with (embedded adj (microcontroller or micro\$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:56
S20	0	(shar\$4 near3 ((unsharable or non\$shar\$5 or (("not" or non) adj sharable))near3 (device or apparatus or memory or storage)))with (processor or cpu)with (embedded adj (microcontroller or micro\$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:58
S21	0	(shar\$4 with ((unsharable or non\$shar\$5 or (("not" or non) adj sharable)) near3 (device or apparatus or memory or storage)))with (processor or cpu)with (embedded adj (microcontroller or micro\$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:58
S22	0	(shar\$4 with ((unsharable or non\$shar\$5 or (("not" or non) adj sharable)) near3 (device or apparatus or memory or storage)))with (processor or cpu)with ((microcontroller or micro\$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:58
S23	0	(shar\$4 with ((unsharable or non\$shar\$5 or (("not" or non) adj sharable)) near3 (device or apparatus or memory or storage)))with (processor or cpu)with ((microcontroller or micro\$controller)).ti.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:59
S24	0	(shar\$4 with ((unsharable or non\$shar\$5 or (("not" or non) adj sharable)) near3 (device or apparatus or memory or storage)))same (processor or cpu)with ((microcontroller or micro\$controller)).ti.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:59

S25	0	(shar\$4 with ((unsharable or non\$shar\$5 or (("not" or non) adj sharable)) near3 (device or apparatus or memory or storage)))same (processor or cpu)with ((microcontroller or micro \$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 10:59
S26	0	(shar\$4 with ((unsharable or non\$shar\$5 or (("not" or non) adj sharable)) near3 (device or apparatus or memory or storage)))same (processor or cpu)same ((microcontroller or micro \$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:00
S27	0	(shar\$4 with ((unsharable or non\$shar\$5 or non-sharable or (("not" or non) adj sharable))near3 (device or apparatus or memory or storage))) same (processor or cpu) same ((microcontroller or micro\$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:00
S28	526	(shar\$4 with ((unsharable or non\$shar\$5 or non-sharable or (("not" or non) adj sharable))near3 (device or apparatus or memory or storage)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:01
S29	0	S28 same (processor or cpu)same (embedded adj (microcontroller or micro \$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:01
S30	0	S28 same (processor or cpu)same ((microcontroller or micro \$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:01
S31	0	S28 and S17	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:02

S32	32	S28 and (processor or cpu)same ((microcontroller or micro \$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:02
S33	0	S28 same ((processor or cpu)same (microcontroller or micro \$controller))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:02
S35	8	S17 same ((load\$4 or writ \$4 or sav\$3)near6 (code or software or firmware or program or instruction41 or data))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 11:24
S36	0	("7386326").URPN.	USPAT	OR	OFF	2010/08/30 11:31
S37	15	("5428760").URPN.	USPAT	OR	OFF	2010/08/30 12:51
S38	16	("20010014603" "20010055038" "20010055948" "20020034967" "20020049061" "20030003961" "20030040275" "20040092277" "4449248" "5734686" "5864570" "6346911" "6396884" "6549784" "6901270" "7165173"). PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/30 12:53
S39	0	("7386326").URPN.	USPAT	OR	OFF	2010/08/30 12:54
S40	65	(shar\$4 near3 (non \$volatile or memory or storage or rom or sdram or dram))with (processor or cpu)with (microcontroller or micro \$controller)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 12:55
S41	8	S40 same ((load\$4 or writ \$4 or sav\$3)near6 (program or instruction41 or data))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 12:55

S42	39	S40 and ((load\$4 or writ \$4 or sav\$3)near6 (program or instruction41 or data))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 12:57
S43	10	S40 and (((load\$4 or writ \$4 or sav\$3)near6 (program or instruction41 or data))with (non \$volatile or flash or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/30 12:57
S44	22	("5819087").URPN.	USPAT	OR	OFF	2010/08/30 13:00
S45	14	("5022077" "5269022" "5327531" "5327549" "5388267" "5410707" "5603055" "5619726" "5701477" "5794054" "5819087" "5822582" "5887164" "5935242"). PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/30 13:06
S46	14	("5022077" "5269022" "5327531" "5327549" "5388267" "5410707" "5603055" "5619726" "5701477" "5794054" "5819087" "5822582" "5887164" "5935242"). PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/30 13:11
S47	18	("6154838").URPN.	USPAT	OR	OFF	2010/08/30 13:11
S48	27	("4030073" "4528634" "4811219" "4896289" "5070450" "5566325" "5583987" "5592616" "5608876" "5740399" "5742758" "5809531" "5835695" "5835784" "5842012" "5850152" "5854937" "5860021" "5892943" "5918047" "5987537" "5999989" "6009522" "6014744" "6101600" "6154838" "6216224").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/30 13:21
S49	1	("6401199").URPN.	USPAT	OR	OFF	2010/08/30 13:24

S50	2	((chang\$3 or alter\$5 or switch\$4 or enabl\$4 or assert\$4 or hold\$4 or disabl\$4 or control\$4) near3 (system adj (mode or state)))with (((microcontroller or micro\$controller)near3 access \$4)adj3 (non\$volatile or flash or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 09:58
S51	1593	((shar\$4 or access\$4) near3 (non\$volatile or memory or storage or ram or rom or sdram or dram))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:00
S52	2	S51 same ((chang\$3 or alter\$5 or switch\$4 or enabl\$4 or assert\$4 or hold\$4 or disabl\$4 or control\$4)near3 (system adj (mode or state)))with (((microcontroller or micro\$controller)near3 access \$4)adj3 (non\$volatile or flash or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:00
S53	2	S51 and ((chang\$3 or alter\$5 or switch\$4 or enabl\$4 or assert\$4 or hold\$4 or disabl\$4 or control\$4)near3 (system adj (mode or state)))with (((microcontroller or micro\$controller)near3 access \$4)adj3 (non\$volatile or flash or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:00
S54	2	S51 and ((chang\$3 or alter\$5 or switch\$4 or enabl\$4 or assert\$4 or hold\$4 or disabl\$4 or control\$4)near3 (system adj (mode or state))) same (((microcontroller or micro\$controller)near3 access\$4)adj3 (non \$volatile or flash or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:00
S55	8	"775281".ap.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:02

S56	4	("5819087" "5794054"). pn.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:02
S57	39	S51 and (((upgrad\$4 or updat\$4 or writ\$4 or load \$4 or stor\$4 or sav\$3 or replac\$4)near3 (data or information or parameter \$1 or value\$1 or program or code or instruction\$1 or software or firmware)) with (((microcontroller or micro\$controller)near3 access\$4)adj3 (memory or storage or non\$volatile or flash or rom)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:13
S58	27	S51 same (((upgrad\$4 or updat\$4 or writ\$4 or load \$4 or stor\$4 or sav\$3 or replac\$4)near3 (data or information or parameter \$1 or value\$1 or program or code or instruction\$1 or software or firmware)) with (((microcontroller or micro\$controller)near3 access\$4)adj3 (memory or storage or non\$volatile or flash or rom)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:13
S59	46	S51 same (((upgrad\$4 or updat\$4 or writ\$4 or load \$4 or stor\$4 or sav\$3 or replac\$4)near3 (data or information or parameter \$1 or value\$1 or program or code or instruction\$1 or software or firmware)) with (((microcontroller or micro\$controller)near3 access\$4)near33 (memory or storage or non\$volatile or flash or rom)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:25

S60	70	S51 and (((upgrad\$4 or updat\$4 or writ\$4 or load\$4 or stor\$4 or sav\$3 or replac\$4)near3 (data or information or parameter\$1 or value\$1 or program or code or instruction\$1 or software or firmware)) with (((microcontroller or micro\$controller)near3 access\$4)near33 (memory or storage or non\$volatile or flash or rom)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:25
S61	2	S60 and ((chang\$3 or alter\$5 or switch\$4 or enabl\$4 or assert\$4 or hold\$4 or disabl\$4 or control\$4)near3 (system adj (mode or state)))with (((microcontroller or micro\$controller)near3 access\$4)adj3 (non\$volatile or flash or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:26
S62	2	S59 and ((chang\$3 or alter\$5 or switch\$4 or enabl\$4 or assert\$4 or hold\$4 or disabl\$4 or control\$4)near3 (system adj (mode or state)))with (((microcontroller or micro\$controller)near3 access\$4)adj3 (non\$volatile or flash or rom))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 11:26
S63	1593	((shar\$4 or access\$4)near3 (non\$volatile or memory or storage or ram or rom or sdram or dram))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 12:53
S64	70	S63 and (((upgrad\$4 or updat\$4 or writ\$4 or load\$4 or stor\$4 or sav\$3 or replac\$4)near3 (data or information or parameter\$1 or value\$1 or program or code or instruction\$1 or software or firmware)) with (((microcontroller or micro\$controller)near3 access\$4)near33 (memory or storage or non\$volatile or flash or rom)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 12:53

S65	0	wo2006131134	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:05
S66	6	"2006131134"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:05
S67	5	"2005119184"	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:09
S68	11	("5202687" "5630057" "5969632" "6009496" "6144327" "6219729" "6236593" "6324628" "6460172" "6754765" "6839774").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/31 13:11
S69	11	("5202687" "5630057" "5969632" "6009496" "6144327" "6219729" "6236593" "6324628" "6460172" "6754765" "6839774").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/31 13:15
S70	29	("6009496").URPN.	USPAT	OR	OFF	2010/08/31 13:15
S71	2	("6832285").URPN.	USPAT	OR	OFF	2010/08/31 13:22
S72	29	("6009496").URPN.	USPAT	OR	OFF	2010/08/31 13:23
S73	29808	((((upgrad\$4 or updat\$4 or writ\$4 or load\$4 or stor \$4 or sav\$3 or replac\$4) near3 (data or information or parameter \$1 or value\$1 or program or code or instruction\$1 or software or firmware)) with ((microcontroller or micro\$controller or micro \$processor)near3 (memory or storage or non\$volatile or flash or rom))))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:24

S74	55485	((upgrad\$4 or updat\$4 or writ\$4 or load\$4 or stor\$4 or sav\$3 or replac\$4)) with ((microcontroller or micro\$controller or micro\$processor)near3 (memory or storage or non\$volatile or flash or rom)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:26
S75	246	S73 and ((shar\$4 or access\$4) near3 (non \$volatile or memory or storage or ram or rom or sdram or dram))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:26
S76	21	S73 and ((shar\$4 or common) near3 (non \$volatile or memory or storage or ram or rom or sdram or dram))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:27
S77	28	S74 and ((shar\$4 or common) near3 (non \$volatile or memory or storage or ram or rom or sdram or dram))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/08/31 13:40
S78	0	("7761644").URPN.	USPAT	OR	OFF	2010/08/31 13:45
S79	13	("4881164" "5535417" "5592677" "5685005" "5727219" "5867726" "5903771" "5933855" "5974493" "6163828" "6353863" "6526462" "6601126").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/31 13:46
S80	26	("4881164").URPN.	USPAT	OR	OFF	2010/08/31 13:47
S81	10	("4177513" "4402046" "4512016" "4665483" "4777595" "4881164" "5077655" "5123101" "5214759" "5218684").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/08/31 13:50
S82	9	("5410655").URPN.	USPAT	OR	OFF	2010/08/31 13:50
S83	1	"6762635".PN.	USPAT	OR	OFF	2010/08/31 14:51

S84	14	((common or shar\$4) near3 (non\$volatile or flash or rom or sdram or eeprom or prom))with (processor or cpu)with microcontroller	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:17
S85	56	((common or shar\$4) near3 (non\$volatile or flash or rom or sdram or eeprom or prom))with (processor or cpu)with (microcontroller or micro \$controller or microprocessor or micro \$processor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:17
S86	1	S85 same ((safe or secur \$3)near2 access)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:18
S87	5	S85 and ((safe or secur \$3)near2 access)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:19
S88	2	(access\$4 or occup\$3 or master)near4((common or shar\$4) near3 (non \$volatile or flash or rom or sdram or eeprom or prom))with (processor or cpu)with microcontroller same (safe\$3 or (without adj (interruption or interference)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:34
S89	1	S85 same ((safe\$3 or (without adj (interruption or interference))) near4 (occup\$4 or access))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:36
S90	2	S85 and ((safe\$3 or (without adj (interruption or interference))) near4 (occup\$4 or access))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:36

S91	8	S85 and ((safe\$3 or (without adj (interruption or interference))))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:36
S92	798	(updat\$4 or upgrad\$4 or reprogram\$4)near6 ((rom or eeprom or flash or non \$volatile or memory)adj5 (microcontroller or micro \$controller or microprocessor or micro \$processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:50
S93	1244	(updat\$4 or upgrad\$4 or reprogram\$4)near6 ((rom or eeprom or flash or non \$volatile or memory)near4 (microcontroller or micro \$controller or microprocessor or micro \$processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:51
S94	3	S92 and ((common or shar\$4) near3 (non \$volatile or flash or rom or sdram or eeprom or prom))with (processor or cpu)with (microcontroller or micro\$controller or microprocessor or micro \$processor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:51
S95	6	S93 and ((common or shar\$4) near3 (non \$volatile or flash or rom or sdram or eeprom or prom))with (processor or cpu)with (microcontroller or micro\$controller or microprocessor or micro \$processor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 08:51
S96	0	S92 and (access\$4 or occup\$3 or master)near4 ((common or shar\$4) near3 (non\$volatile or flash or rom or sdram or eeprom or prom))with (processor or cpu)with microcontroller same (safe \$3 or (without adj (contention\$1 or interruption or interference)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 09:02

S97	0	S93 and (access\$4 or occup\$3 or master)near4 ((common or shar\$4) near3 (non\$volatile or flash or rom or sdram or eeprom or prom))with (processor or cpu)with microcontroller same (safe\$3 or (without adj (contention\$1 or interruption or interference)))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 09:02
S98	8	S93 and ((processor or cpu)with microcontroller same (safe\$3 or (without adj (contention\$1 or interruption or interference))))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 09:02
S99	7	S92 and ((processor or cpu)with microcontroller same (safe\$3 or (without adj (contention\$1 or interruption or interference))))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	OFF	2010/09/01 09:03
S100	11	("6115814").URPN.	USPAT	OR	OFF	2010/09/01 09:10
S101	1	("6925522").URPN.	USPAT	OR	OFF	2010/09/01 09:13
S102	11	("20050163468" "20060013198" "5999476" "6523755" "6647439" "6785892" "6832269" "6891543" "6898678" "6925522" "7017038").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/09/01 09:14
S103	8	("5381540" "5446864" "5454114" "5455937" "5504903" "5825854" "5890003" "5914543").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2010/09/01 09:22

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp

L37	1	(system or apparatus or comput\$4) same ((microcontroller or uc or micro\$controller or up or micro\$processor)near6 ((built\$3 or coupl\$4 or connect\$4 or communicat\$4 or joined or attach\$3) adj4 (non\$volatile or flash or dram or sdram or rom))) same (CPU or processor or (process\$4 adj (logic or unit or circuit)))and (((saf\$3 or secur\$4)adj2 access or read \$3 or writ\$4))with (non \$volatile or flash or dram or sdram or rom)and (((load\$4 or stor\$4 or sav\$4 or writ\$4) near3 (program or code or instruction\$1 or command or data or information))with ((microcontroller or uc)adj2 (memory or storage or memory))).clm.	US-PGPUB; USPAT; UPAD	OR	OFF	2010/12/15 08:16
L38	2	(system or apparatus or comput\$4) same ((microcontroller or uc or micro\$controller or up or micro\$processor)near6 ((built\$3 or coupl\$4 or connect\$4 or communicat\$4 or joined or attach\$3) adj4 (non\$volatile or flash or dram or sdram or rom))) same (CPU or processor or (process\$4 adj (logic or unit or circuit)))and (((saf\$3 or secur\$4)adj2 access or read \$3 or writ\$4))with (non \$volatile or flash or dram or sdram or rom)and (((load\$4 or stor\$4 or sav\$4 or writ\$4) near3 (program or code or instruction\$1 or command or data or information))with ((microcontroller or uc)adj2 (memory or storage or memory)))	US-PGPUB; USPAT; UPAD	OR	OFF	2010/12/15 08:17

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3 [Receiver imperfections and CYCLOPS: an alternative description](#)

[Ottavio Peichert](#), [Günter Hempel](#)

February 2002

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Publisher: John Wiley and Sons Ltd.

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 0

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4 [One-phase Riemann problem and wave interactions in systems of conservation laws of mixed type](#)

[Haitao Fan](#)

July 1993

SIAM Journal on Mathematical Analysis, Volume 24 Issue 4

Publisher: Society for Industrial and Applied Mathematics

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Keywords: Riemann problem, conservation laws, phase transitions, shocks, travelling wave criterion, vanishing viscosity method

5 [Similarity Measurement Between Images](#)

[Chaur-Chin Chen](#), [Hsueh-Ting Chu](#)

July 2005

COMPSAC '05: Proceedings of the 29th Annual International Computer Software and Applications Conference - Volume 02, Volume 02

Publisher: IEEE Computer Society

Full text available:  [Publisher Site](#)

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Experimental results of applying two similarity measurements, Euclidean distance and chord distance, to test a set of six Brodatz's textures are reported. Experiments show that in addition to feature extraction, A similarity measurement between images ...

Also published in:

July 2005 **COMPSAC '05: Proceedings of the 29th Annual International Computer Software and Applications Conference - Volume 02** Volume 02

6 [Meromorphic connections on \$P^1\$ and the multiplicity of Abelian integrals](#)

[H. Movasati](#)

April 2006

Journal of Dynamical and Control Systems, Volume 12 Issue 2

Publisher: Kluwer Academic Publishers

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 0

In this paper, we introduce the notion of Abelian integrals in differential equations for an arbitrary vector bundle on P^1 with a meromorphic connection. In this general context, we give an upper bound for the maximum multiplicity of Abelian ...


Keywords: Abelian integrals, Gauss-Manin connection, meromorphic connection

7 [The Fuzzy Evaluation of E-Commerce Customer Satisfaction Utilizing Fuzzy TOPSIS](#)

[Mehdi Fasanghari, Navid Ghojamy, S. Kamal Chaharsoghi, Shohre Qadami, Mohamad Soltani Delgosha](#)

August 2008 **ISECS '08: Proceedings of the 2008 International Symposium on Electronic Commerce and Security**

Publisher: IEEE Computer Society

Full text available:  [Publisher Site](#)

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Effective customer satisfaction investigation is a very important precondition for e-commerce. It is the problem which needs to be solved for e-commerce customer satisfaction through use of advanced methods to evaluate the customer satisfaction. This ...

Keywords: Fuzzy Evaluation, E-Commerce, Customer Satisfaction, Fuzzy TOPSIS

8 [Authorization specification and enforcement in federated database systems](#)

[Sabrina De Capitani di Vimercati, Pierangela Samarati](#)

March 1997 **Journal of Computer Security**, Volume 5 Issue 2

Publisher: IOS Press

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 14


Keywords: access control, authorization administration, authorization autonomy, federated systems

9 [Overfitting Avoidance as Bias](#)

[Quiten Schaffer](#)

February 1993 **Machine Learning**, Volume 10 Issue 2

Publisher: Kluwer Academic Publishers

Full text available:  [Publisher Site](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 42

Strategies for increasing predictive accuracy through selective pruning have been widely adopted by researchers in decision tree induction. It is easy to get the impression from research reports that there are statistical reasons for believing that these ...

Keywords: Overfitting avoidance, decision tree pruning, inductive bias

10 [Supporting RFID-based item tracking applications in Oracle DBMS using a bitmap datatype](#)

[Yimo Hu, Seema Sundara, Timothy Chorma, Jagannathan Srinivasan](#)

August 2005 **VLDB '05: Proceedings of the 31st international conference on Very large data bases**

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2 Etude du comportement et des émotions dans un contexte de multisollicitations: approche exploratoire avec la Plateforme d'Evaluation, de prototypage et de tests d'usageS (PEPSS) Nadine Couture, Marion Wolff, Régis Mollard, Laurent Todeschini October 2010 Ergo'IA '10: Proceedings of the Ergonomie et Informatique Avancee Conference Publisher: ACM Request Permissions Full text available: Pdf (1.90 MB) Bibliometrics: Downloads (6 Weeks): 7, Downloads (12 Months): 7, Downloads (Overall): 7, Citation Count: 0		
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Publisher: Society for Industrial and Applied Mathematics

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Publisher: IEEE Computer Society

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Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 4

An algorithm for evaluating the square root of integers and real numbers is developed. The procedure consists of two parts: one to obtain a close estimate of the square root and the other to modify the initial value, iteratively, until a precise root ...

Keywords: bit-shift operation, close estimate, digital arithmetic, division by 2, fast converging iteration, floating-point numbers, initial value modification, integer numbers, iterative methods, number theory., precise root, real numbers, square rooting algorithms

14 [Covering morphisms and unique minimal D-schemes](#)


[R. Tindell](#)

September 1991 **Acta Cybernetica**, Volume 10 Issue 1-2

Publisher: Acta Cybernetica


Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 0

15 [Anvil next generation: a multi-format variable data printtemplate based on PPML-T](#)

 [Fabio Giannetti](#)

August 2007 **DocEng '07: Proceedings of the 2007 ACM symposium on Document engineering**

Publisher: ACM [Request Permissions](#)

Full text available:  Pdf (2.18 MB)

Bibliometrics: Downloads (6 Weeks): 5, Downloads (12 Months): 14, Downloads (Overall): 64, Citation Count: 2

Anvil Next Generation is a toolset enabling the usage of multiple formats, as templates. It is mainly based on the Personalized Print Markup Language Template (PPML-T) workflow. The possibility of supporting several template formats within the same workflow ...

Keywords: PPML, PPMLT, XSL-FO, XSLT, template, variable data print

16 [Efficient impleimentation of pseudorandom functions for electronic seal protection protocols](#)

[Mun-Kyu Lee](#), [Jung Ki Min](#), [Seok Hun Kang](#), [Sang-Hwa Chung](#), [Howon Kim](#), [Dong Kyue Kim](#)

August 2006 **WISA'06: Proceedings of the 7th international conference on Information security applications: PartI**

Publisher: Springer-Verlag

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 1

One of the most promising applications of active RFID tags is electronic seal, which is an electronic device to guarantee the authenticity and integrity of freight containers and also provides physical protection like a lock. There are already many commercial ...

Keywords: AES, RFID, electronic seal, message authentication code, pseudorandom function

17 [Linking SMEs' clusters: A view of the information infrastructure](#)

[M. E. León](#), [R. Salamoni](#), [J. Amato Neto](#)

December 2000 **Proceedings of the IFIP TC5/WG5.3 Second IFIP Working Conference on Infrastructures for Virtual Organizations: Managing Cooperation in Virtual Organizations and Electronic Business towards Smart Organizations: E-Business and Virtual Enterprises: Managing Business-to-Business Cooperation**

Publisher: Kluwer, B.V.

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 0

18 [Coordinated Optimization of Bus Headways for Passenger Corridors](#)

[Jing Teng](#), [Xiaoquang Yang](#), [Xuan Li](#), [Ming Zhao](#)

April 2009 **CSO '09: Proceedings of the 2009 International Joint Conference on Computational Sciences and Optimization - Volume 02**, Volume 02

Publisher: IEEE Computer Society

Full text available:  [Publisher Site](#)

Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 0

Passenger corridors carry high-density passenger volumes and they are intensive superposition sections of passenger OD demands in the transit network. In order to balance supply and demand distribution between different bus routes on the same passenger ...

Keywords: Passenger corridor, Bus headway, Coordination dispatching, Optimization, Genetic algorithm

- 19 [Setup check](#)
[James W. Meritt](#)
May 1998 **Sys Admin** , Volume 7 Issue 5
Publisher: Miller Freeman, Inc.
Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 0

- 20 [High Performance Computational Steering of Physical Simulations](#)
[Jeffrey S. Veiter](#), [Karsten Schwan](#)
April 1997 **IPPS '97: Proceedings of the 11th International Symposium on Parallel Processing**
Publisher: IEEE Computer Society
Full text available: [Publisher Site](#)
Bibliometrics: Downloads (6 Weeks): n/a, Downloads (12 Months): n/a, Downloads (Overall): n/a, Citation Count: 9

Computational steering allows researchers to monitor and manage long running, resource intensive applications at runtime. Limited research has addressed high performance computational steering. High performance in computational steering is necessary ...

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Publication Year: [1872 - 2007](#)

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SEARCHES FOR THIS SESSION

- [\(\(sharing non-sharable un-sharable device memory between embedded controller\) AND processor cpu\) \(0\)](#)
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Issue Classification *11958601*	Application/Control No. 11958601	Applicant(s)/Patent Under Reexamination HARRIS ET AL.
	Examiner NITIN C PATEL	Art Unit 2116

ORIGINAL						INTERNATIONAL CLASSIFICATION												
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED							
713			324			G	0	6	F	1 / 26 (2006.01.01)								
CROSS REFERENCE(S)						G	0	6	F	15 / 177 (2006.01.01)								
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)																	
713	2	100																

<input type="checkbox"/> Claims renumbered in the same order as presented by applicant <input type="checkbox"/> CPA <input type="checkbox"/> T.D. <input type="checkbox"/> R.1.47															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	17	17												
2	2	18	18												
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14	14														
15	15														
16	16														

NONE		Total Claims Allowed:	
		23	
(Assistant Examiner)	(Date)		
/NITIN C PATEL/ Primary Examiner.Art Unit 2116	12/15/10	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	4

PART B - FEE(S) TRANSMITTAL

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Jeffrey C. Hood
Meyertons Hood Kivlin Kowert & Goetzel PC
P.O. Box 398
Austin, TX 78767-0398

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(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

11/958,601 12/18/2007 Ian F. Harris 5707-16601 1387

TITLE OF INVENTION: SHARING NON-SHARABLE DEVICES BETWEEN AN EMBEDDED CONTROLLER AND A PROCESSOR IN A COMPUTER SYSTEM

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1510	\$300	\$0	\$1810	03/17/2011

EXAMINER	ART UNIT	CLASS-SUBCLASS
PATEL, NITIN C	2116	713-323000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).
☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

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1. _____ & Goetzel, P.C.
2. Jeffrey C. Hood
3. Mark S. Williams

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Standard Microsystems Corporation

Hauppauge, New York

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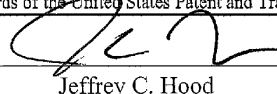
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Jeffrey C. Hood

Date 2011-03-11

Typed or printed name

PTO # 35,198

Registration No.

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<p align="center">CHANGE OF CORRESPONDENCE ADDRESS <i>Application</i></p> <p>Address to: Commissioner for Patents P.O. Box 1450 Alexandria, VA 22313-1450</p>	Application Number	11/958,601	
	Filing Date	December 18, 2007	
	First Named Inventor	Ian F. Harris	
	Art Unit	2116	
	Examiner Name	Patel, Nitin C.	
	Attorney Docket Number	5707-16601	
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Electronic Patent Application Fee Transmittal				
Application Number:	11958601			
Filing Date:	18-Dec-2007			
Title of Invention:	SHARING NON-SHARABLE DEVICES BETWEEN AN EMBEDDED CONTROLLER AND A PROCESSOR IN A COMPUTER SYSTEM			
First Named Inventor/Applicant Name:	Ian F. Harris			
Filer:	Jeffrey C Hood/Jeannie Miranda			
Attorney Docket Number:	5707-16601			
Filed as Large Entity				
Utility under 35 USC 111(a) Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
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Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
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Miscellaneous:				
Printed copy of patent - no color	8001	2	3	6
Total in USD (\$)				1816

Electronic Acknowledgement Receipt	
EFS ID:	9644075
Application Number:	11958601
International Application Number:	
Confirmation Number:	1387
Title of Invention:	SHARING NON-SHARABLE DEVICES BETWEEN AN EMBEDDED CONTROLLER AND A PROCESSOR IN A COMPUTER SYSTEM
First Named Inventor/Applicant Name:	Ian F. Harris
Correspondence Address:	Jeffrey C. Hood Meyertons Hood Kivlin Kowert & Goetzel PC P.O. Box 398 - Austin TX 78767-0398 US 5128538800 -
Filer:	Jeffrey C Hood/Jeannie Miranda
Filer Authorized By:	Jeffrey C Hood
Attorney Docket Number:	5707-16601
Receipt Date:	11-MAR-2011
Filing Date:	18-DEC-2007
Time Stamp:	17:09:55
Application Type:	Utility under 35 USC 111(a)

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Bib Data Sheet

CONFIRMATION NO. 1387

SERIAL NUMBER 11/958,601	FILING OR 371(c) DATE 12/18/2007 RULE	CLASS 713	GROUP ART UNIT 2116	ATTORNEY DOCKET NO. 5707-16601	
APPLICANTS Ian F. Harris, Kings Park, NY; Drew J. Dutton, Austin, TX; ** CONTINUING DATA ***** This appln claims benefit of 60/910,863 04/10/2007 ** FOREIGN APPLICATIONS ***** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 01/14/2008					
Foreign Priority claimed <input type="checkbox"/> yes <input type="checkbox"/> no 35 USC 119 (a-d) conditions <input type="checkbox"/> yes <input type="checkbox"/> no <input type="checkbox"/> Met after met Allowance Verified and Acknowledged _____ Examiner's Signature Initials		STATE OR COUNTRY NY	SHEETS DRAWING 5	TOTAL CLAIMS 25	INDEPENDENT CLAIMS 6
ADDRESS 35690					
TITLE SHARING NON-SHARABLE DEVICES BETWEEN AN EMBEDDED CONTROLLER AND A PROCESSOR IN A COMPUTER SYSTEM					
FILING FEE RECEIVED 2210	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:		<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		



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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
11/958,601	04/19/2011	7930576	5707-16601	1387

35690 7590 03/30/2011
MEYERTONS, HOOD, KIVLIN, KOWERT & GOETZEL, P.C.
P.O. BOX 398
AUSTIN, TX 78767-0398

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 684 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Ian F. Harris, Kings Park, NY;
Drew J. Dutton, Austin, TX;

UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 7,930,576 C1

DATED: September 4, 2012

INVENTOR(S): Ian F. Harris and Drew J. Dutton

It is certified that an error or errors appear in the above-identified patent and that said EX PARTE REEXAMINATION CERTIFICATE is hereby corrected as shown below:

In the Claims:

Column 12

Lines 24-25, in claim 181, delete “host memory and” and insert -- host memory bus and --, therefor.

MAILING ADDRESS OF SENDER:
Jeffrey C. Hood, Esq.,
Meyertons, Hood, Kivlin, Kowert & Goetzel PC
P.O. Box 398
Austin, Texas 78767-0398

PATENT NO. 7,930,576 C1

Certificate of Correction (PTO Form 1050)

Copied from 90011754 on 08/16/2013

***EX PARTE* REEXAMINATION**

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Reexamination Control. No.:	90/011,754	§	Atty.Dkt.No.:	5707-26200
Inventor:	Ian F. Harris, et al.	§	Examiner:	Peikari, Behzad
Request Filing Date:	June 21, 2011	§	Group/Art Unit:	3992
U.S. Patent No.:	7,930,576	§	Conf. No.:	4071
Title:	SHARING NON-SHARABLE DEVICES BETWEEN AN EMBEDDED CONTROLLER AND A PROCESSOR IN A COMPUTER SYSTEM	§ § § § § § § § § §		

TRANSMITTAL LETTER

Transmitted herewith for filing in the captioned case is the following:

- (1) Form PTO-1050. Errors which occur at important points in the captioned patent or which may otherwise affect the understanding or interpretation of the patent are thereon corrected.

All of the errors shown in PTO-1050 are due to Patent Office oversights. A Certificate of Correction is requested under 35 U.S.C. § 254. Applicants believe that no fees are required, however, should any fees be required, please deduct them from Meyertons, Hood, Kivlin, Kowert & Goetzel PC Deposit Account No. 501505/5707-26200/JCH.

Respectfully submitted,

/Jeffrey C. Hood/
Jeffrey C. Hood, Reg. #35198

Meyertons, Hood, Kivlin, Kowert & Goetzel PC
P.O. Box 398
Austin, Texas 78767-0398
(512) 853-8800
DATE: 2012-09-26 JCH/kmm

SPE RESPONSE FOR CERTIFICATE OF CORRECTION

Paper No.:20130816

DATE : August 16, 2013

TO SPE OF : ART UNIT 2116

SUBJECT : Request for Certificate of Correction on Patent No.: 7930576

A response is requested with respect to the accompanying request for a certificate of correction.

Please complete this form and return with file, within **7** days to:

Certificates of Correction Branch - ST (South Tower) 9A22

Palm location **7590** - Tel. No. (703) 305-8309

With respect to the change(s) requested, correcting Office and/or Applicant's errors, should the patent read as shown in the certificate of correction? No new matter should be introduced, nor should the scope or meaning of the claims be changed.

Thank You For Your Assistance

Certificates of Correction Branch

The request for issuing the above-identified correction(s) is hereby:

Note your decision on the appropriated box.

☒ **Approved**

All changes apply.

☐ **Approved in Part**

Specify below which changes **do not** apply.

☐ **Denied**

State the reasons for denial below.

Comments:

OK to enter

/KIM HUYNH/
Supervisory Patent Examiner.Art Unit 2116