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(54) **METHOD AND APPARATUS FOR ALLOCATING CRC CODES IN A FLASH ROM**

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(57) **ABSTRACT**

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A method and apparatus for allocating CRC (Cyclic Redundancy Check) codes in a flash ROM (Read-Only Memory). The apparatus comprises a flash ROM (40) and a microprocessor (10). The flash ROM is logically divided into a plurality of data blocks (41). Each data block contains a CRC code block (42) that comprises a plurality of bytes for saving CRC codes. The microprocessor can write to and read from the flash ROM, calculate a complement code (51) of a sum (50) of all the bytes of the data block, and add the complement code to data of a selected byte. The microprocessor thus generates new CRC codes (52) and writes them to the corresponding CRC code block. The new CRC codes generated can meet the critical requirement of CRC. That is, the sum of all the bytes of the data block (including the CRC code block) is null.

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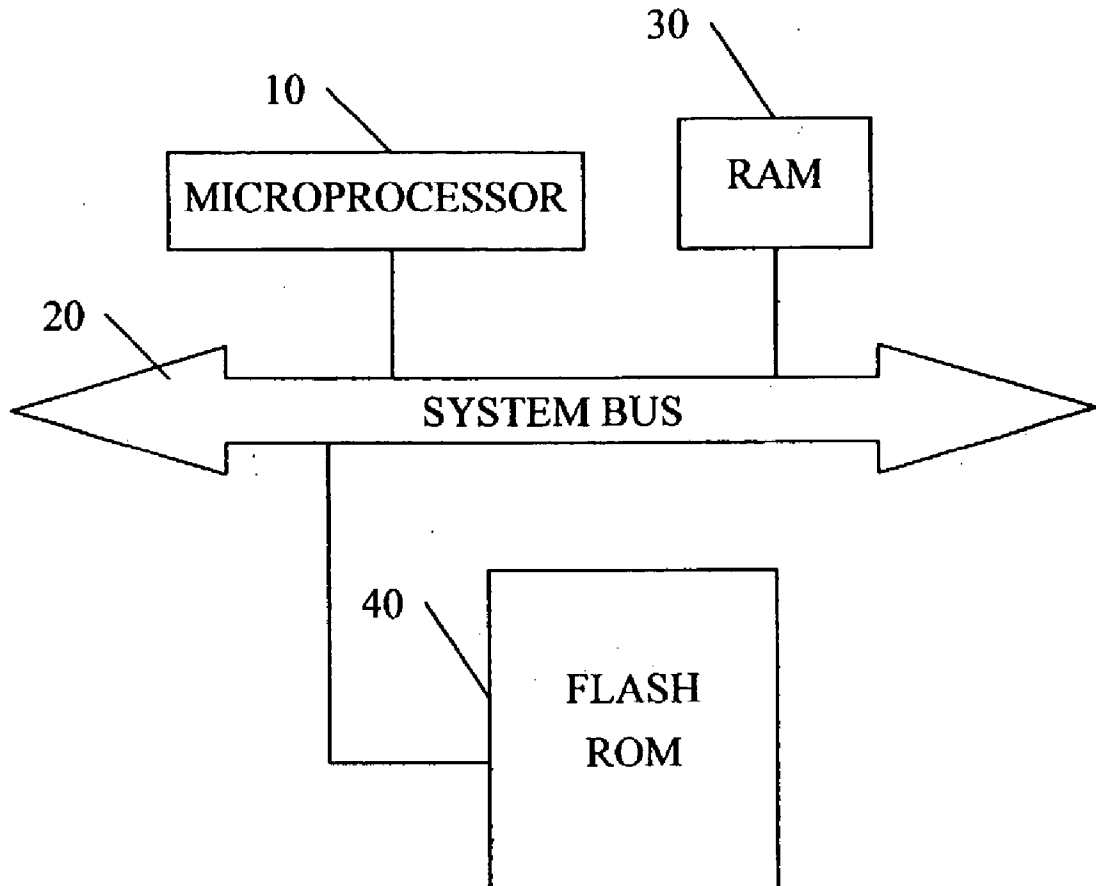
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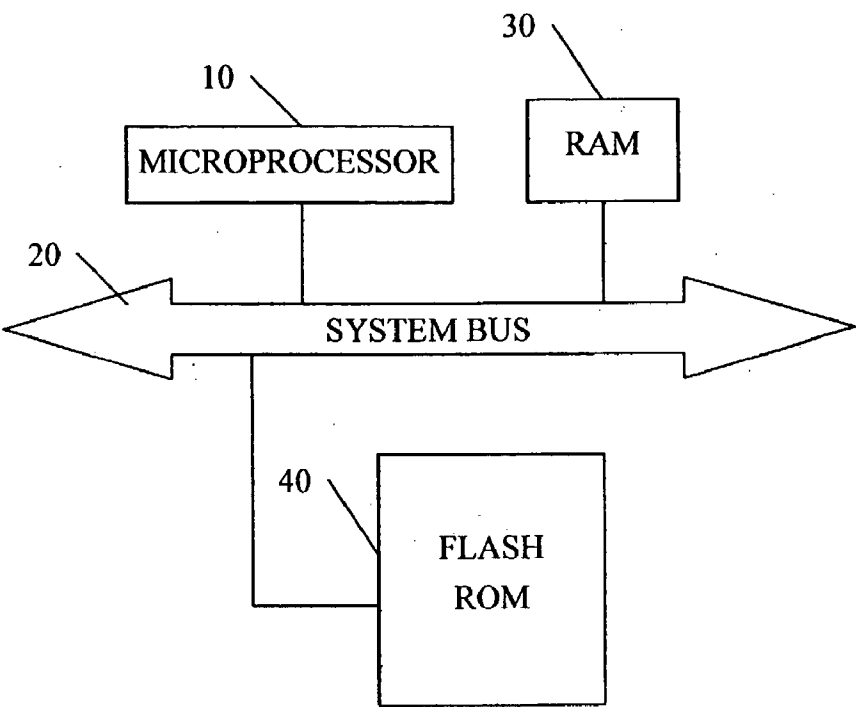


FIG. 1

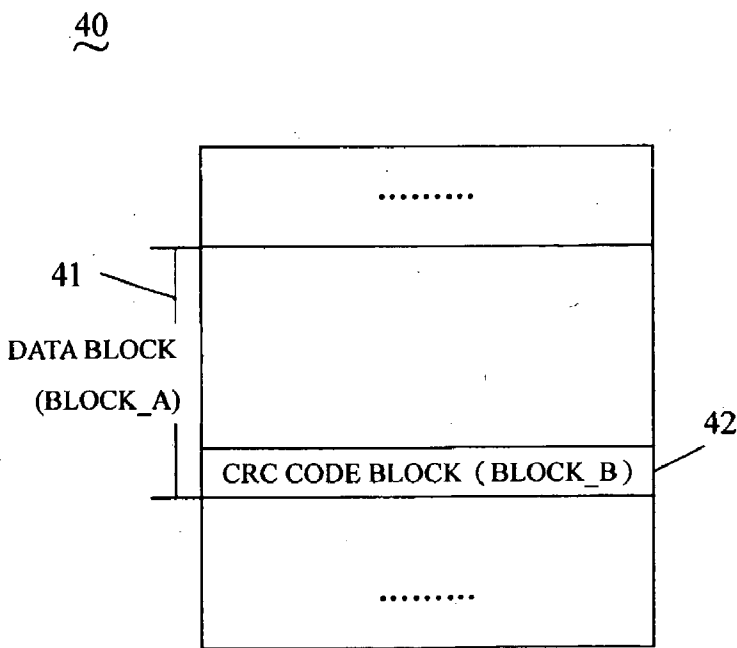


FIG. 2

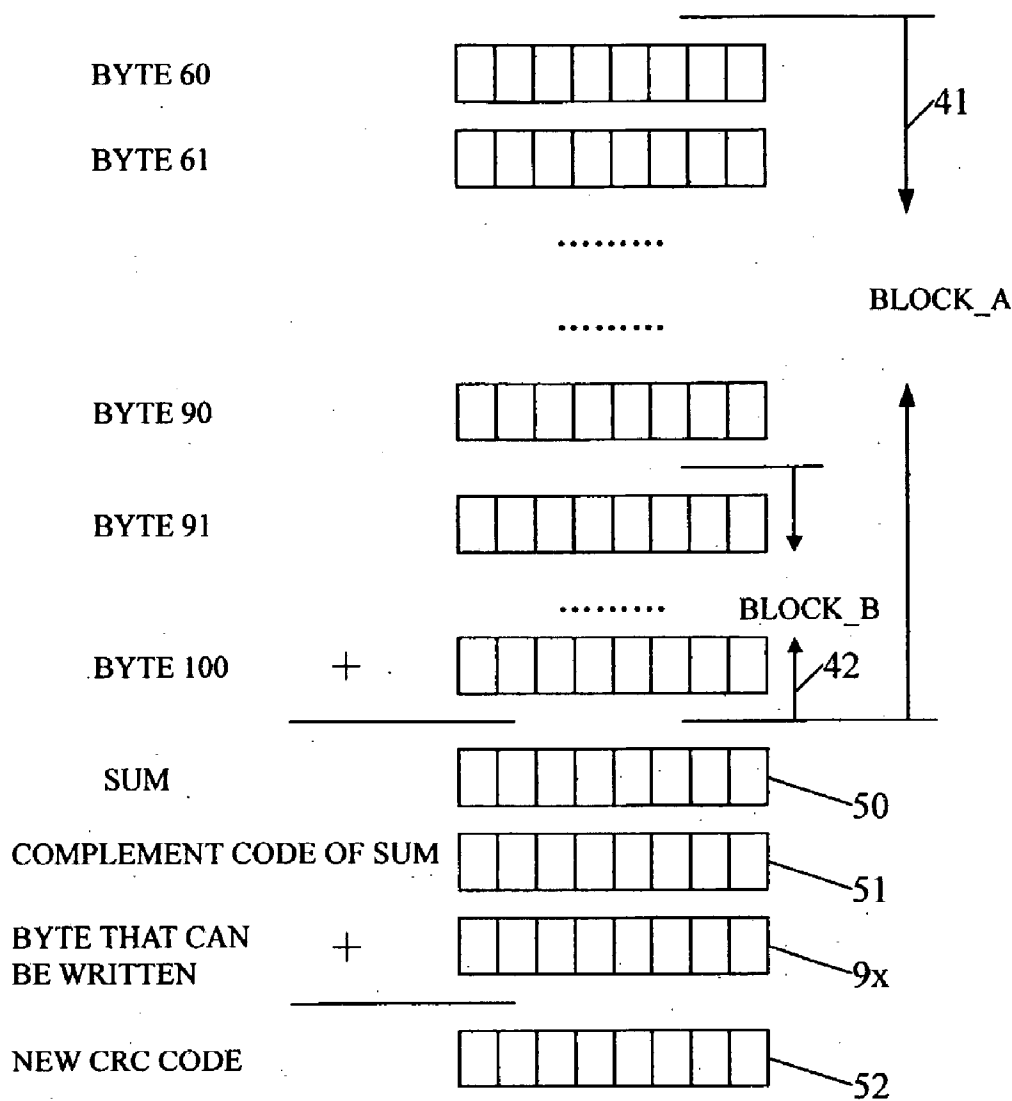


FIG. 3

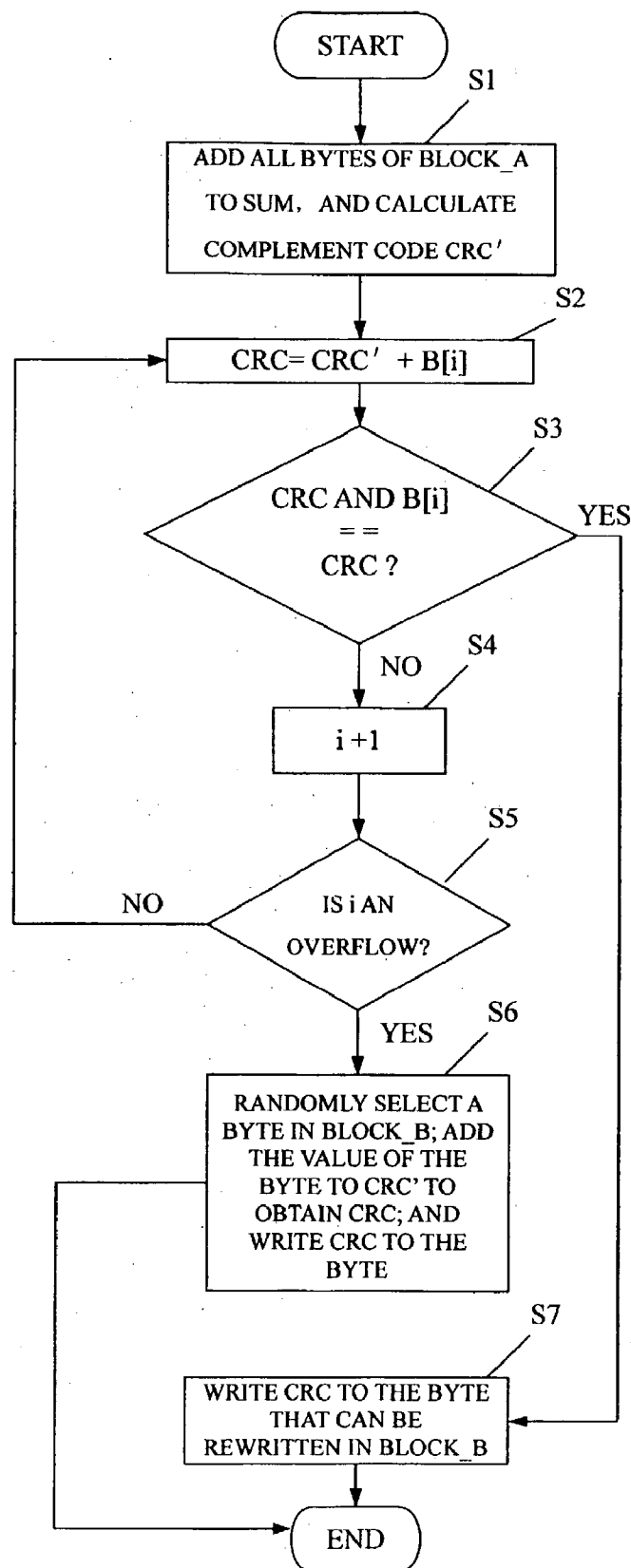


FIG. 4

METHOD AND APPARATUS FOR ALLOCATING CRC CODES IN A FLASH ROM

BACKGROUND OF THE INVENTION

[0001] 1. Field of the Invention

[0002] This invention relates to a method and apparatus for allocating CRC (Cyclic Redundancy Check) codes in a flash ROM (Read-Only Memory), and more specifically a method and apparatus that can effectively reduce the times of erasing CRC codes.

[0003] 2. Description of Related Art

[0004] It is very important for organizations and private users alike that electronic data be written to and read from a storage system quickly and reliably. A storage system may be logically divided into a plurality of data blocks, with each data block being further divided into a plurality of bytes. One method widely used to ensure reliable reading and writing of data is to perform a CRC (Cyclic Redundancy Check) on the data. When the data is written to the storage system, CRC codes are generated and saved in one or more bytes that are predefined in position. And when the data is read from the storage system, its CRC codes are read as well and compared to the newly calculated CRC codes associated with data read. If the newly calculated CRC codes match the stored CRC codes, the data is likely to be correct. Should the newly calculated CRC codes not match the stored CRC codes, there is something wrong with data read.

[0005] A conventional storage system may use semiconductors, magnetic devices or optical devices as its storage medium. A typical storage system generally comprises erasable read only memory, such as flash ROM and EEPROM (Electrically Erasable Programmable Read Only Memory). Flash ROM and EEPROM can both retain data while power is off, and can update the data according to new input data. There are some differences between flash ROM and EEPROM. EEPROM needs a voltage higher than normal to erase the data, so an additional device is always needed to accomplish erasing of data. Flash ROM can work under a normal voltage while erasing the data. In addition, only one byte at a time can be erased in an EEPROM, while a plurality of bytes at a time can be erased in a flash ROM. However, flash ROM has problems such as a limited number of erasures, limited erasing speed and bad tracks. A flash ROM has a lifetime of about 100,000 erasures.

[0006] The drawback of saving CRC codes in a flash ROM or an EEPROM is that the CRC code has to be erased and rewritten every time any data is updated, even when only one byte is updated. Conventional methods typically handle this problem in one of two ways. The first way is to increase the physical capability of the flash ROM or EEPROM, such as improving erasure lifetime and erasing speed. The second way is to maintain a plurality of CRC codes for related data. In this way, the occasions of erasing one CRC code are distributed to a plurality of CRC codes.

[0007] With the increasing popularity of network and portable devices, the demand for storage capacity has been increasing commensurately. For example, downloading of data such as software and music requires updating of data stored in a storage system. These days, erasing of CRC codes is more frequent than ever.

[0008] In a flash ROM, a bit can be rewritten from the value 1 to the value 0, and can be erased from the value 0 to the value 1. Rewriting means changing a bit from a high level voltage that represents 1 to a low level voltage that represents 0. Erasing refers to changing a bit to a high level voltage that can be rewritten. One byte comprises 8 bits, and may for example have a binary numerical value 11110101. This byte can be rewritten as 101000101, since any corresponding bit having a value 1 can be rewritten to the value 0. Said byte cannot for example be rewritten as 10011101, since the fifth bit of the byte has a value 0 that cannot be rewritten as the value 1. So it is necessary to erase the byte to 11111111, and then rewrite it to 10011101. Conventional methods have not adequately taken advantage of this characteristic of flash ROMs. Thus, there exists a need for a method and apparatus that can reduce the number of erasures of CRC codes in a flash ROM.

SUMMARY OF THE INVENTION

[0009] It is an object of the present invention to provide a method for allocating CRC codes in a flash ROM which can reduce the number of erasures of CRC codes.

[0010] It is another object of the present invention to provide an apparatus for allocating CRC codes in a flash ROM which can reduce the number of erasures of CRC codes.

[0011] According to one aspect of the present invention, a method for allocating CRC codes in a flash ROM is provided. A microprocessor is used to control the generation of CRC codes and data reading and writing. The method comprises the steps of: (a) logically dividing a flash ROM into a plurality of data blocks, each data block comprising a CRC code block, the CRC code block comprising a plurality of bytes for saving CRC codes; (b) reading data from a data block of the flash ROM and calculating a complement code of sum of all the bytes of the data block; (c) adding a value of each byte of the CRC code block of the data block to said complement code and obtaining a first sum, and performing an AND-operation on a bit by bit basis between said first sum and the value of the byte; (d) writing said first sum to the byte as a new CRC code if any one of the results of the AND-operation is equal to said first sum; and (e) randomly selecting a byte in the CRC code block if none of the results of the AND-operation is equal to said first sum, adding the value of the selected byte with said complement code and obtaining a second sum, erasing the selected byte, and writing said second sum to the selected byte as a new CRC code. The new CRC code generated by following the above-described method can meet the critical requirement of CRC. That is, the sum of all the bytes of the data block (including the CRC code block) is null.

[0012] In accordance with another aspect of the present invention, an apparatus for allocating CRC codes in a flash ROM comprises: a flash ROM logically divided into a plurality of data blocks, each data block comprising a CRC code block, the CRC code block comprising a plurality of bytes for saving CRC codes; and a microprocessor capable of writing to and reading from the flash ROM, reading data from a data block of the flash ROM and calculating a complement code of a sum of all the bytes of the data block, and adding the complement code to data of a selected byte. The microprocessor thus generates new CRC codes, and

writes them to the corresponding CRC code block. The new CRC codes generated by the above-described apparatus can meet the critical requirement of CRC. That is, the sum of all the bytes of the data block (including the CRC code block) is null.

[0013] Other objects, advantages and novel features of the present invention will be drawn from the following detailed description of the present invention with the attached drawings, in which:

BRIEF DESCRIPTION OF THE DRAWINGS

[0014] FIG. 1 is a block diagram of hardware of an apparatus for allocating CRC codes in a flash ROM according to the present invention, said apparatus comprising a flash ROM;

[0015] FIG. 2 schematically illustrates storage space of the flash ROM of FIG. 1 where the CRC codes are saved, according to the present invention;

[0016] FIG. 3 illustrates a method according to the present invention for generating CRC codes of data in a flash ROM; and

[0017] FIG. 4 is a flow chart of a method according to the present invention for allocating CRC codes in a flash ROM.

DETAILED DESCRIPTION OF THE INVENTION

[0018] FIG. 1 is a block diagram of hardware of an apparatus for allocating CRC codes in a flash ROM according to the present invention. The apparatus comprises a microprocessor 10, a system bus 20, a RAM (Random-access memory) 30 and a flash ROM 40. The microprocessor 10 controls the operation of data output and input, and has the function of adding and performing AND-operation bit by bit. The system bus 20 can be any kind of appropriate data/control bus over which the signals are transmitted. The microprocessor 10 sends controlling signals over the system bus 20 to the RAM 30 and the flash ROM 40, and transports data between the RAM 30 and the flash ROM 40. The RAM 30 is an internal memory capable of supplying operating programs and a space for the microprocessor 10 to save data temporarily. The flash memory 40 is an external memory. Data saved in the flash memory 40 can be updated frequently. Such data may be system information, programs, personal data, and so on. The microprocessor 10 can read data from the flash ROM 40, and transmit the data to the RAM 30. The microprocessor 10 can also receive data from external data sources (not shown) through the system bus 20, and save the data to the flash ROM 40.

[0019] FIG. 2 schematically illustrates storage space of the flash ROM 40 where the CRC codes are saved, according to the present invention. The storage space comprises a storage system logically divided into a plurality of data blocks 41, with each data block 41 being further divided into a plurality of bytes. That is, the flash ROM 40 is divided into a plurality of data blocks 41, with each data block 41 containing a CRC code block 42. The CRC code block 42 contains a plurality of bytes to save the CRC codes, and each CRC code occupies one byte.

[0020] While reading data, the microprocessor 10 reads from the data blocks 41 of the flash ROM 40, and tempo-

rarily saves the data in the RAM 30. The data that is read contains data of the CRC code block 42. Before outputting the data, the microprocessor 10 performs a cyclic redundancy check on the data that has been read. All bytes are added up to a sum. If the sum is 0, this represents that the data has been read correctly. If the sum is not 0, this represents that there is something wrong with the data that has been read. Conventional methods as known in the art can be used to modify the data, or to return a message indicating that something is wrong and reread the data.

[0021] When the microprocessor 10 writes data to the assigned data block 41, the CRC codes must be rebuilt. By following the method of the present invention, appropriate bytes of the corresponding CRC code block 42 can be found and rewritten as new CRC codes, or can be erased and then written as new CRC codes. In the following description, "erasing" means changing a byte to a status such that the byte is rewritable.

[0022] FIG. 3 illustrates a method according to the present invention for generating CRC codes of data in a flash ROM. In the flash ROM 40 described above, each data block 41 comprises a plurality of bytes. In the example shown in FIG. 3, forty-one bytes are contained in one data block 41, and these are designated as byte 60 through byte 100. The data block 41 contains the CRC code block 42, which contains a plurality of bytes that are designated as byte 91 through byte 100. The microprocessor 10 adds all bytes of the data block 41 up to a sum 50, calculates a complement code 51 of the sum 50, and finds a byte 9x that can be rewritten (as detailed in the following paragraph). Rewriting means changing a bit from a high level voltage that represents 1 to a low level voltage that represents 0. One byte comprises 8 bits, and may for example have a binary numerical value 11110101. This byte can be rewritten as 101000101, since any corresponding bit having a value 1 can be rewritten to the value 0. Said byte cannot for example be rewritten as 10011101, since the fifth bit of the byte has a value 0, which cannot be rewritten as the value 1. The sum of the byte 9x that can be rewritten and the complement code 51 is a new CRC code 52.

[0023] FIG. 4 is a flow chart of a method according to the present invention for allocating CRC codes in a flash ROM. In FIG. 4, "BLOCK_A" represents a data block such as the data block 41 shown in FIG. 2. "BLOCK_B" represents the CRC code block of a data block, such as the CRC code block 42 shown in FIG. 2. "SUM" represents the sum of all the bytes of a data block. "CRC" represents the complement code of SUM. "CRC" represents the CRC codes of the data of a data block. "i" represents the address of one of the bytes in the CRC code block. "B[i]" represents the data of one of the bytes in BLOCK_B.

[0024] The microprocessor 10 writes data to the flash ROM 40 and generates related CRC codes. If any data of BLOCK_A are modified, in step S1, the microprocessor 10 adds all bytes of BLOCK_A up to SUM, and calculates the complement code CRC' of SUM. "i" is initialized as the address of the first byte of BLOCK_B. In step S2, the microprocessor 10 adds CRC' and B[i] up to CRC, and performs an AND-operation on a bit by bit basis between CRC and B[i]. In step S3, the microprocessor 10 determines whether the result of the AND-operation is equal to CRC. If the result of the AND-operation is equal to CRC, this means

that B[i] can be rewritten, and the "i" of B[i] represents the byte that can be rewritten. Accordingly, in step S7, the microprocessor 10 writes CRC to the byte, and in this way the CRC codes are generated, whereupon the procedure is ended. If the result of the AND-operation is not equal to CRC, in step S4, the microprocessor 10 adds 1 to "i," so that "i" relates to the address of the next byte in BLOCK_B. In step S5, the microprocessor 10 determines whether "i" is an overflow; that is, whether "i" is larger than the address of the last byte of BLOCK_B. If "i" is an overflow, this means that there is no byte left to be rewritten. Accordingly, in step S6, the microprocessor 10 randomly selects a byte of BLOCK_B and adds it to CRC, and the sum obtained is the new CRC. The microprocessor 10 writes the new CRC to the byte, whereupon the procedure is ended. If "i" is not an overflow, the procedure returns to step S2 to continue searching for bytes that can be rewritten. By this means according to the present invention, the new CRC codes are generated.

[0025] Although the invention has been described in language specific to structural features and/or methodological steps, it is to be understood that the invention defined in the appended claims is not necessarily limited to the specific features or steps described. Rather, the specific features and steps are disclosed as preferred forms of implementing the claimed invention.

What is claimed is:

1. A method for allocating Cyclic Redundancy Check (CRC) codes in a flash ROM (Read-Only Memory) via a microprocessor, the method comprising the steps of:

logically dividing a flash ROM into a plurality of data blocks, each of the data blocks comprising a CRC code block, the CRC code block comprising a plurality of bytes for saving CRC codes;

reading data from a data block of the flash ROM and calculating a complement code of sum of all the bytes of the data block;

adding a value of each of the bytes of the CRC code block of the data block to said complement code and obtaining a first sum, and performing an AND-operation on a bit by bit basis between said first sum and the value of the byte;

writing said first sum to the byte as a new CRC code if any one of the results of the AND-operation is equal to said first sum; or

randomly selecting a byte in the CRC code block if none of the results of the AND-operation is equal to said first sum, adding the value of the selected byte with said complement codes and obtaining a second sum, erasing the selected byte, and writing said second sum to the selected byte as a new CRC code.

2. The method as defined in claim 1, wherein any bit of a byte having a value 1 can be rewritten to have the value 0.

3. An apparatus for allocating Cyclic Redundancy Check (CRC) codes in a flash Read-Only Memory (ROM), the apparatus comprising:

a flash ROM logically divided into a plurality of data blocks, each of the data blocks comprising a CRC code block, the CRC code block comprising a plurality of bytes for saving CRC codes; and

a microprocessor capable of writing to and reading from the flash ROM, reading data from a data block of the flash ROM and calculating a complement code of a sum of all the bytes of the data block, and adding the complement code to data of a selected byte.

4. The apparatus as defined in claim 3, wherein the microprocessor is capable of performing an AND-operation on a bit by bit basis between the data of each of the bytes in the CRC code block and new CRC codes.

5. The apparatus as defined in claim 4, wherein the microprocessor can write the new CRC codes to selected bytes.

6. The apparatus as defined in claim 4, wherein the microprocessor can write the new CRC codes after erasing the bytes.

7. The apparatus as defined in claim 6, wherein any bit of a byte having a value 1 can be rewritten to have the value 0.

8. A method for allocating Cyclic Redundancy Check (CRC) codes in a flash ROM (Read-Only Memory) via a microprocessor, the method comprising the steps of:

logically dividing a flash ROM into a plurality of data blocks, each of the data blocks comprising a CRC code block, the CRC code block comprising a plurality of bytes for saving CRC codes;

reading data from a data block of the flash ROM and calculating a complement code of a first value generated by a designated mathematics formula of all the bytes of the data block;

combining a second value of each of the bytes of the CRC code block of the data block to said complement code and obtaining a third value generated by said formula, and performing an AND-operation on a bit by bit basis between said third value and the data of one of the bytes of said data block;

writing said third value to the byte as a new CRC code if any one of the results of the AND-operation is equal to said third value; or

randomly selecting a byte in the CRC code block if none of the results of the AND-operation is equal to said third value, combining a fourth value of the selected byte, generated by said formula, with said complement code and obtaining a fifth value, erasing the selected byte, and writing said fifth value to the selected byte as a new CRC code.

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