

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

**SAMSUNG ELECTRONICS CO., LTD, and
SAMSUNG ELECTRONICS AMERICA, INC.,**

Petitioners,

v.

CELLECT, LLC,

Patent Owner.

U.S. Patent No. 9,186,052

**DECLARATION OF DEAN P. NEIKIRK, PH.D. IN SUPPORT OF
PETITION FOR *INTER PARTES* REVIEW OF
U.S. PATENT NO. 9,186,052**

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I, Dean P. Neikirk, Ph.D., hereby declare under penalty of perjury:

I. INTRODUCTION

1. I have been retained on behalf of Samsung to provide assistance regarding U.S. Patent No. 9,186,052 (“the ’052 patent,” Ex. 1001) in connection with Samsung’s Petition for *Inter Partes* Review.¹ Specifically, I have been asked to consider the validity of claims 1-3 and 7 of the ’052 patent (the “Challenged Claims”). I have personal knowledge of the facts and opinions set forth in this declaration, and, if called upon to do so, I would testify competently thereto.

2. I am being compensated for my time at my standard rate of \$600/hr. My compensation is based solely on the amount of time that I devote to activity related to this case and is in no way contingent on the nature of my findings, the presentation of my findings in testimony, or the outcome of this or any other proceeding. I have no other financial interest in this proceeding. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials, including those cited herein.

3. I may rely upon these materials, my knowledge and experience, and/or additional materials to rebut arguments raised by the Patent Owner. Further, I may

¹ Where appropriate, I refer to exhibits that I understand are filed with the Petitions for *Inter Partes* Review of the ’052 Patent.

also consider additional documents and information in forming any necessary opinions, including documents that may not yet have been provided to me.

4. My analysis of the materials produced in this proceeding is ongoing and I will continue to review any new material as it is provided. This declaration represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. BACKGROUND AND QUALIFICATIONS

5. All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in designing, developing, researching, and teaching image sensor technology.

6. I received a Bachelor of Science degree from Oklahoma State University, in physics and mathematics, in 1979.

7. Following my undergraduate studies, I attended the California Institute of Technology, where I earned a Master's degree and Doctorate degree in Applied Physics, in 1981 and 1984, respectively.

8. Each of my academic degrees involved significant studies in sensors, including image sensors; optical systems; solid state physics; semiconductor devices; electrical engineering; electronic systems; electromagnetics; radio frequency

systems; and antennas. For example, courses relating to these fields that I took include two years of study in electromagnetics and optics, one year of study in solid state and semiconductor physics, as well as four years of graduate research in electronic devices, antenna design, antenna fabrication, and optical systems.

9. My Ph.D. thesis was on the design and fabrication of high frequency electromagnetic detectors and quasi-optical imaging antenna arrays, including research on integrated-circuit fabrication, semiconductor devices, integrated circuits, antennas, sensors, and IC packaging. I designed and fabricated the first monolithic integrated-circuit imaging antenna array for use in an electronic camera operating at wavelengths in the far infrared (sometimes referred to as the terahertz) region of the electromagnetic spectrum. For this work on the first high resolution focal plane array for use at wavelengths between 0.1 mm and 1 mm, I was awarded the 1984 Marconi International Fellowship Young Scientist Award “for contributions to the development of millimeter wave integrated circuits especially in the area of detectors and imaging arrays.”

A. Research and Teaching Experience

10. My work as a professor began in 1984, when I joined the University of Texas at Austin as an assistant professor. In 1988, I became an associate professor, and in 1992 became a full professor. Today, I continue to be a full professor in the Department of Electrical and Computer Engineering at the University of Texas.

11. Over the years, I have taught a variety of electrical engineering courses at the University of Texas. These include Integrated Circuit Fabrication, VLSI Fabrication Techniques, Ultra Large Scale Integrated Circuit Fabrication Techniques, Integrated Circuit Nanomanufacturing Techniques, Electromagnetics in Packaging, Simulation Methods in CAD/VLSI, Micro-Electromechanical Systems, Electromagnetic Engineering, and Microwave and Radio Frequency Engineering. I have also taught several continuing education courses in these fields.

12. I currently conduct research with students and research scientists in the Microelectromagnetics Research Group in the Microelectronics Research Center at The University of Texas at Austin. My research areas include the fabrication and modeling of electromagnetic micro-machined sensors and actuators. I am also involved in research relating to integrated circuit processing and the high frequency properties of transmission lines. Over the years, I conducted research in the area of wireless sensors for identifying failing bridges and improving the safety of new bridges. I have also conducted research in the areas of electromagnetics, optical devices for use in electronic cameras, manufacturing systems engineering, and solid-state electronics.

13. For over ten years, I served as the Graduate Advisor for the Department of Electrical and Computer Engineering at the University of Texas at Austin, as well as serving for over five years as an Associate Chairman of the Electrical and

Computer Engineering Department. In addition to my current position as a professor in the Electrical and Computer Engineering Department at The University of Texas at Austin, I am also an Associate Dean of Graduate Studies at The University of Texas at Austin.

14. I have also devoted a significant portion of my time at the University to contributing to various technical journals and other publications. My work has been included in 93 referenced archival journal publications, 165 referenced conference proceedings, and 24 published abstracts. I have also contributed to book chapters and technical reports relating to various electrical engineering topics. My publications have addressed technologies such as chemical sensors, integrated circuits for antenna arrays, determining conductor loss in transmission lines, optical and electromagnetic devices for infrared detection, multilayer interconnection lines for high speed digital integrated circuits, RF oscillator circuits, memory-switching double-barrier quantum-well diodes circuits, RF and infrared detection circuits, and other topics related to sensors and optical systems.

15. More information on my research and teaching experience, and my contribution to technical publications, is included in my *curriculum vitae* (Appendix A).

B. Patents Awarded

16. Through my work on sensors and electronic systems, I have been named an inventor on seventeen U.S. patents. These are summarized in my *curriculum vitae* attached as Appendix A.

17. My issued patents include, for example, U.S. Patent No, 5,408,107, titled “Semiconductor Device Apparatus Having Multiple Current-Voltage Curves and Zero-Bias Memory.” This patent is directed to a semiconductor device that can be switched between current-voltage curve settings at higher positive or negative voltages and can be read at lower voltages. As another example, U.S. Patent No. 9,291,586, titled “Passive Wireless Self-Resonant Sensor,” relates to a sensor for detecting materials, including a substrate, a passivation layer formed on the substrate, a high surface area material disposed on the passivation layer, and a self-resonant structure that includes a planar spiral inductor and a plurality of planar interdigitated capacitor electrodes disposed within the passivation layer.

18. Many of my patents are related to sensor arrays used for chemical testing. These include, for example, U.S. Patent 6,589,779: “General signaling protocol for chemical receptors in immobilized matrices,” U.S. Patent 6,602,702: “Detection system based on an analyte reactive particle,” U.S. Patent 7,316,899, “Portable sensor array system,” and U.S. Patent 8,105,849, “Integration of fluids and reagents into self-contained cartridges containing sensor elements.” These patents

resulted from research by my group and my collaborators into new sensor arrays with the capability to use optical effects to perform multi-analyte chemical analysis.

19. Two companies have been founded based on technology developed and patented by my research group and collaborators in the area of chemical sensing arrays. In both cases the technology was developed at The University of Texas at Austin and licensed to start-ups. In one case LabNow, Inc. received \$14 million in first-round venture investment for its point-of-care diagnostic system from the Soros Group, Austin Ventures and other investors to develop the company's technology and to launch its initial product, CD4NowTM, a point-of-care diagnostic tool for HIV/AIDS patients.

C. Other Awards

20. My work as a professor of electrical engineering, and my scholarship in various fields relating to sensors and electronic systems, have been recognized through several awards I have received over the years. As noted in my curriculum vitae (Appendix A), these include the Marconi International Fellowship Young Scientist Award, the Engineering Foundation Faculty Award from the University of Texas at Austin, the General Motors Foundation Centennial Teaching Fellowship, the IBM Corporation Faculty Development Award, the National Science Foundation Presidential Young Investigator, the Lockheed Martin Aeronautics Company Award for Excellence in Engineering Teaching, and various other academic awards.

D. Industry Experience

21. While the majority of my professional experience in electrical engineering has involved research and teaching, I have also provided technical consulting to numerous companies and been involved in academic-industry partnerships. For example, I have provided consulting to Teltech Resource Network, Ardex, Inc., E.P. Hamilton Associates, Burnett Company, Microelectronics and Computer Technology Corporation, and Baker-Hughes. In addition, my work on electro-chemical sensors was selected as a commercialization venture between the University of Texas and LabNow, Inc. Further, my work together with a graduate student relating to actuator stacked microbolometer arrays for multispectral infrared detection was selected for sponsorship by Coventor, Inc., a company that provides software tools for developing microelectromechanical systems, microfluidics, and semiconductor process applications.

E. Professional Society Involvement

22. I have been a Senior Member of the Institute of Electrical and Electronics Engineers ("IEEE") for more than fifteen years. From March 1991 to October 1994, I served as an Associate Editor for the IEEE publication called "IEEE Transactions on Education." I also served as a member of the Editorial Board on the IEEE Transactions on Microwave Theory and Techniques in the 1990-2000 timeframe.

23. A detailed description of my professional qualifications, including a listing of my specialties/expertise and professional activities, are contained in my *curriculum vitae* (Appendix A).

III. BASIS OF MY OPINIONS AND MATERIALS CONSIDERED

24. In reaching the conclusions described in this declaration, I have relied on the documents and materials cited herein as well as those identified in Appendix B attached to this declaration. These materials comprise patents, related documents, and printed publications. Each of these materials is a type of document that experts in my field would have reasonably relied upon when forming their opinions and would have had access to either through the applicable patent offices and/or well-known libraries, conferences, publications, organizations and websites in the field as further discussed herein.

25. My opinions are also based upon my education, training, research, knowledge, and personal and professional experience.

IV. LEGAL STANDARDS

A. Obviousness Under 35 U.S.C. §103(a)

26. I understand that a claim may be invalid under 35 U.S.C. §103(a) if the subject matter described by the claim as a whole would have been obvious to a hypothetical person of ordinary skill in the art in view of a prior art reference or in view of a combination of references at the time the claimed invention was made. Therefore, I understand that obviousness is determined from the perspective of a

hypothetical person of ordinary skill in the art and that the asserted claims of the patent should be read from the point of view of such a person at the time the claimed invention was made. I further understand that a hypothetical person of ordinary skill in the art is assumed to know and to have all relevant prior art in the field of endeavor covered by the patent in suit.

27. I have also been advised that an analysis of whether a claimed invention would have been obvious should be considered in light of the scope and content of the prior art, the differences (if any) between the prior art and the claimed invention, and the level of ordinary skill in the pertinent art involved. I understand as well that a prior art reference should be viewed as a whole.

28. I have also been advised that in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the market place, and/or the background knowledge possessed by a person having ordinary skill in the art. I understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious, and that these principles include the following:

- A combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results;

- When a device or technology is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or in a different one, so that if a person of ordinary skill can implement a predictable variation, the variation is likely obvious;
- If a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill;
- An explicit or implicit teaching, suggestion, or motivation to combine two prior art references to form the claimed combination may demonstrate obviousness, but proof of obviousness does not depend on or require showing a teaching, suggestion, or motivation to combine;
- Market demand, rather than scientific literature, can drive design trends and may show obviousness;
- In determining whether the subject matter of a patent claim would have been obvious, neither the particular motivation nor the avowed purpose of the named inventor controls;
- One of the ways in which a patent's subject can be proved obvious is by noting that there existed at the time of invention a known problem for which there was an obvious solution encompassed by the patent's claims;

- Any need or problem known in the field of endeavor at the time of invention and addressed by the patent can provide a reason for combining the elements in the manner claimed;
- “Common sense” teaches that familiar items may have obvious uses beyond their primary purposes, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle;
- A person of ordinary skill in the art is also a person of ordinary creativity, and is not an automaton;
- A patent claim can be proved obvious by showing that the claimed combination of elements was “obvious to try,” particularly when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions such that a person of ordinary skill in the art would have had good reason to pursue the known options within his or her technical grasp; and
- One should be cautious of using hindsight in evaluating whether a claimed invention would have been obvious.

29. I further understand that, in making a determination as to whether or not the claimed invention would have been obvious to a person of ordinary skill, the Board may consider certain objective factors if they are present, such as: commercial

success of products practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. These factors are generally referred to as “secondary considerations” or “objective indicia” of nonobviousness. I understand, however, that for such objective evidence to be relevant to the obviousness of a claim, there must be a causal relationship (called a “nexus”) between the claim and the evidence and that this nexus must be based on a novel element of the claim rather than something in the prior art. I also understand that even when they are present, secondary considerations may be unable to overcome primary evidence of obviousness (such as motivation to combine with predictable results) that is sufficiently strong.

30. I have been asked to consider the validity of the Challenged Claims. I understand that for *inter partes* reviews, invalidity must be shown under a preponderance of the evidence standard. I have concluded that each of the Challenged Claims is invalid at least under 35 U.S.C. §103 based on the references described below and as explained herein.

B. Claim Construction

31. I have been informed that patent claims are construed from the viewpoint of a person of ordinary skill in the art of the patent at the time of the invention. I have been informed that patent claims generally should be interpreted consistent with their plain and ordinary meaning as understood by a person of

ordinary skill in the art in the relevant time period (*i.e.*, at the time of the purported invention, or the so called “effective filing date” of the patent application), after reviewing the patent claim language, the specification and the prosecution history (*i.e.*, the intrinsic record).

32. I have further been informed that a person of ordinary skill in the art must read the claim terms in the context of the claim itself, as well as in the context of the entire patent specification. I understand that in the specification and prosecution history, the patentee may specifically define a claim term in a way that differs from the plain and ordinary meaning. I understand that the prosecution history of the patent is a record of the proceedings before the U.S. Patent and Trademark Office, and may contain explicit representations or definitions made during prosecution that affect the scope of the patent claims. I understand that an applicant may, during the course of prosecuting the patent application, limit the scope of the claims to overcome prior art or to overcome an examiner’s rejection, by clearly and unambiguously arguing to overcome or distinguish a prior art reference, or to clearly and unambiguously disavow claim coverage.

33. In interpreting the meaning of the claim language, I understand that a person of ordinary skill in the art may also consider “extrinsic” evidence, including expert testimony, inventor testimony, dictionaries, technical treatises, other patents, and scholarly publications. I understand this evidence is considered to ensure that a

claim is construed in a way that is consistent with the understanding of those of ordinary skill in the art at the time of the claimed invention. This can be useful for a technical term whose meaning may differ from its ordinary English meaning. I understand that extrinsic evidence may not be relied on if it contradicts or varies the meaning of claim language provided by the intrinsic evidence, particularly if the applicant has explicitly defined a term in the intrinsic record.

V. PRIORITY DATE AND A PERSON OF ORDINARY SKILL

34. In rendering the opinions set forth in this declaration, I was asked to consider the patent claims and the prior art through the eyes of a person of ordinary skill in the art at the time of the alleged invention, which I understand is asserted to be October 6, 1997.

35. I understand that the factors considered in determining the ordinary level of skill in a field of art include the level of education and experience of persons working in the field; the types of problems encountered in the field, the teachings of the prior art, and the sophistication of the technology at the time of the alleged invention. I understand that a person of ordinary skill in the art is not a specific real individual, but rather is a hypothetical individual having the qualities reflected by the factors above. I understand that a person of ordinary skill in the art would also have knowledge from the teachings of the prior art, including the art cited below.

36. Taking these factors into consideration, in my opinion, on or before October 6, 1997, a person of ordinary skill in the art relating to the technology of the '052 patent would have had a minimum of a Bachelor's degree in Electrical Engineering, Physics, or a related field, and approximately two years of professional experience in the field of imaging devices. Additional graduate education could substitute for professional experience, or significant experience in the field could substitute for formal education.

37. Well before October 6, 1997, my level of skill in the art was at least that of a person of ordinary skill in the art. I am qualified to provide opinions concerning what a person of ordinary skill in the art would have known and understood at that time, and my analysis and conclusions herein are from the perspective of a person of ordinary skill in the art as of October 6, 1997.

VI. BACKGROUND ON THE STATE OF THE ART

38. As discussed in Section VII, the '052 patent is generally directed to a particular configuration of a CMOS-based imager with separate processing circuitry. As discussed in the subsequent sections, each of these components was well-known in the prior art, and the claims of the '052 patent are generally directed to simple combinations of these prior art elements.

39. As further discussed in the sections below, various arrangements of imager components was known in the prior art. For example, the prior art discusses

examples of: (1) an imager array grouped with the timing and control circuitry and separate from the processing circuitry (Ackland (Ex. 1006), Fig. 6 (*e.g.*, depicting an array and timing and control circuitry separate from the processing circuitry)); (2) timing and control circuitry grouped with the processing circuitry but separate from the array (Hurwitz (Exs. 1042, 1046, 1047), 120, Fig. 1 (*e.g.*, depicting a single ASIC for the timing and control and processing circuitry); Ricquier (Exs. 1038, 1033), 2-3 (*e.g.*, discussing “off-chip” timing and control relative to the pixel array)); or (3) the array, timing and control circuitry, and processing circuitry each being separate from one another (Ricquier, 2-3; Stam (Ex. 1043), 6:25-28, Fig. 5 (*e.g.*, illustrating “Timing and Control” 203 as separate from “Image Array Sensor” chip 106 and “Microprocessor” 204)). All of these various combinations were known in the art, and a person of ordinary skill would have known that components could be placed apart from each other or placed in different locations based on the design needs and intended applications of a given device.

40. Similarly, the prior art discloses various physical arrangements of an image sensor relative to the other components. For example, the prior art discloses: (1) an imager that is positioned parallel or perpendicular to a circuit board on which the processing circuitry is mounted (Swift (Ex. 1005), 8:33-9:21, Fig. 2 (*e.g.*, depicting image sensor 51 and circuit board 52 and 53)); (2) three stacked circuit boards or chips that can contain the various components (Suzuki (Ex. 1015), 2:51-

55, 3:15-19, Fig. 2 (*e.g.*, depicting “chip-connecting board 226,” “circuit board 227,” and “connector board 228” arranged in a stacked configuration), Fig. 3c; Chamberlain (Ex. 1044), 5:47-50, 6:21-35, Fig. 2, Fig. 17 (*e.g.*, depicting “driver board 13,” “logic board 16,” and “option boards 19” arranged in a stacked configuration)); (3) an image sensor stacked on a circuit board, which is offset from another circuit board (Wakabayashi (Ex. 1027), Fig 3, Fig. 7 (*e.g.*, depicting “circuit board 39” offset from the “imager device 27” stacked on “circuit board 29”)); or (4) a circuit board with processing circuitry that is placed in a control box remote from the image sensor (Monroe (Ex. 1007), 3:57-62, 8:8-11, Fig. 3 (*e.g.*, depicting “power supply and lighting unit 14,” having “video processing circuitry,” remote from “video otoscope 12” having “solid state imager 36”)). All of these various combinations were known in the art, and a person of ordinary skill would have known that components could be placed on a number of circuit boards and arranged in any number of different “planes” based on the design needs and intended applications of a given device.

41. Further, it was well-known that “[f]itting of the components into the available space” while maintaining “orientation of the components relative to one another,” including “placement” of circuitry on “various layers” arranged “stackwise,” is a mere design choice. Ex. 1045 (A Guide to Printed Circuit Board Design, 1984), 15, 20.

A. CMOS Imager Arrays

42. As set forth in the “Background Art” section of the ’052 patent, solid state imaging technology typically employs one of three types of sensors including charged coupled devices (CCD), charge injection devices (CID), and photo diode arrays (PDA). ’052 patent, 1:52-65. The ’052 patent further admits that “[i]n the mid-1980s, complementary metal oxide semiconductors (CMOS) were developed for industrial use.” ’052 patent, 1:60-63.

43. In general, each pixel in a solid-state imager (including CMOS based imagers) will convert the light it receives into an electrical charge proportional to the amount of light that it receives. After a certain amount of time has elapsed, the signal produced by the charge accumulated by the pixel is measured, and this measured information from all the pixels is combined together and processed to create a single digital image. This process (*i.e.*, measuring the signal produced by charge on each of the pixels over time) is traditionally controlled by “timing and control” circuitry connected to the pixel array, and the output from the pixel array is communicated to the rest of the device through “read out circuitry” where it can be processed into a convenient data format.

44. As explained by the ’052 patent, “active pixel-type CMOS imagers” and “passive pixel-type CMOS imagers” were already well known in the art. *See, e.g.*, ’052 patent, 1:66-2:1, 2:20-22. These types of CMOS based imagers had

various advantages over other types of solid-state imagers. For example, the '052 patent states that it was well known that “[o]ne advantage of active pixel-type imagers is that the amplifier placement results in lower noise levels than CCDs or other solid state imagers.” *See, e.g.*, '052 patent, 2:2-4. It was also known, as recognized in the '052 patent, that “[a]nother major advantage is that these CMOS imagers can be mass produced on standard semiconductor production lines.” *See, e.g.*, '052 patent, 2:4-6. In addition, it was known that CMOS imagers “can incorporate a number of other electronic controls that are usually found on multiple circuit boards of much larger size”—“[f]or example, timing circuits, and special functions such as zoom and anti-jitter controls can be placed on the same circuit board containing the CMOS pixel array without significantly increasing the overall size of the host circuit board.” *See, e.g.*, '052 patent, 2:12-15. Further, it was known in the art that CMOS imagers require significantly less power (*e.g.*, 100 times less power) than a CCD-type imager. *See, e.g.*, '052 patent, 2:15-17.

45. The '052 patent itself is replete with examples of prior art systems that make use of CMOS pixel arrays and the accompanying timing, control, and readout circuitry required to operate the array. *See e.g.*, '052 patent, 2:6-19 (discussing that “the CMOS imager described in U.S. Pat. No. 5,471,515 to Fossum, et al. ... can incorporate a number of other different electronic controls that are usually found on multiple circuit boards”); 2:25-34 (“One example of a manufacturer which has

developed a passive pixel array with performance nearly equal to known active pixel devices and being compatible with the read out circuitry disclosed in the U.S. Pat. No. 5,471,515 is VLSI Vision, Ltd., 1190 Saratoga Avenue, Suite 180, San Jose, Calif. 95129"); 2:35-42 ("In addition to the active pixel-type CMOS imager which is disclosed in U.S. Pat. No. 5,471,515, there have been developments in the industry for other solid state imagers which have resulted in the ability to have a 'camera on a chip.' For example, Suni Microsystems, Inc. of Mountain View, Calif., has developed a CCD/CMOS hybrid which combines the high quality image processing of CCDs with standard CMOS circuitry construction"); 13:55-60 ("A further discussion of the timing and control circuitry which may be used in conjunction with an active pixel array is disclosed in U.S. Pat. No. 5,471,515 and is also described in an article entitled "Active Pixel Image Sensor Integrated With Readout Circuits" appearing in NASA Tech Briefs, October 1996, pp. 38 and 39.").

B. Image Processing Circuitry

46. The data produced by an imager/image sensor will generally need to be processed further in order to convert the data into a standard video format. In the context of the '052 patent, this is described as converting the "pre-video" signal produced by the imager into a "post-video" signal that is suitable for a standard video device. *See e.g.*, '052 patent, 9:29-37 ("Once the pre-video signal has been electrically transmitted from image sensor ... [V]ideo processing board 50 then

carries out all the necessary conditioning.... The signal produced by the video processing board 50 can be further defined as a post-video signal which can be accepted by a standard video device.”).

47. These video processing circuits (*e.g.*, for doing white balancing and/or converting the single into a standard format) were well known prior to the '052 patent. For example, U.S. 4,700,219 (Ex. 1009, “Tanaka”) was published in October of 1987 and discloses a functionally identical circuit as the preferred embodiment of the “video processing circuitry” disclosed in the '052 patent. The '052 patent itself also concedes that video processing circuitry was already known in the art, stating that the detailed “example of circuitry which may be used in the video processing board ... is very similar to the circuitry which is found in a miniature quarter-inch Panasonic camera, Model KS-162.” '052 patent, 15:7-19.

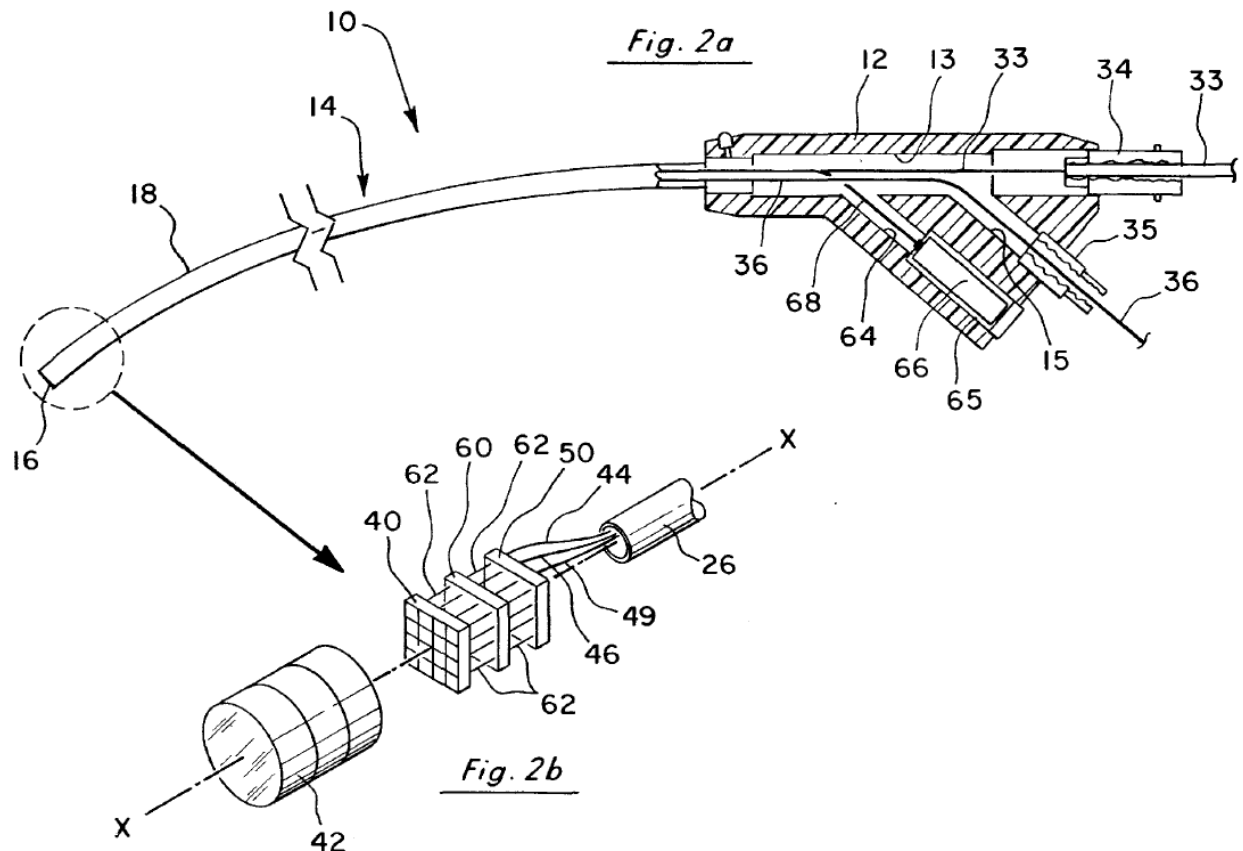
VII. ANALYSIS OF THE '052 PATENT

A. Overview of the '052 Patent

48. The '052 patent describes endoscopic instruments utilizing solid state imaging technology that allows for the imaging sensor to be placed at the distal end of an endoscope. '052 patent, 1:52-57. The '052 patent acknowledges that different types of solid state image sensors including charged coupled devices (CCD) and complementary metal oxide semiconductors (CMOS) were known. '052 patent, 1:57-2:34. The '052 patent also acknowledges that it was known for a CMOS imager

utilizing active pixels to incorporate a number of other different electronic controls (*e.g.*, timing circuits) that are usually found on multiple circuit boards of much larger size. '052 patent, 2:9-19. Such a CMOS imager is referred to as a “camera on a chip.” '052 patent, 2:15-19. The '052 patent also acknowledges that image sensors utilizing active pixels “with an amplifier at each pixel site” were known. '052 patent, 1:66-2:9. The '052 patent further acknowledges it was known to form image sensors on semiconductor substrates. '052 patent, 2:42-46.

49. The '052 patent acknowledges that preexisting “camera on a chip” systems could combine elements “usually found on multiple circuit boards of much larger size ... without significantly increasing the overall size” of the device. '052 patent, 2:9-15. The '052 patent allegedly improves on these “camera on a chip” concepts by “rearrang[ing] the circuitry [into] a stacked relationship so that there is a minimum profile presented when used within a surgical instrument or other investigative device.” '052 patent, 3:34-36. Supposedly, this enabled the creation of a “very small imaging device” that could be used in “even the smallest ... endoscopic instruments.” '052 patent, 3:24-30, 3:51-55. An example of such a device is the endoscope depicted in Figures. 2a and 2b reproduced below.

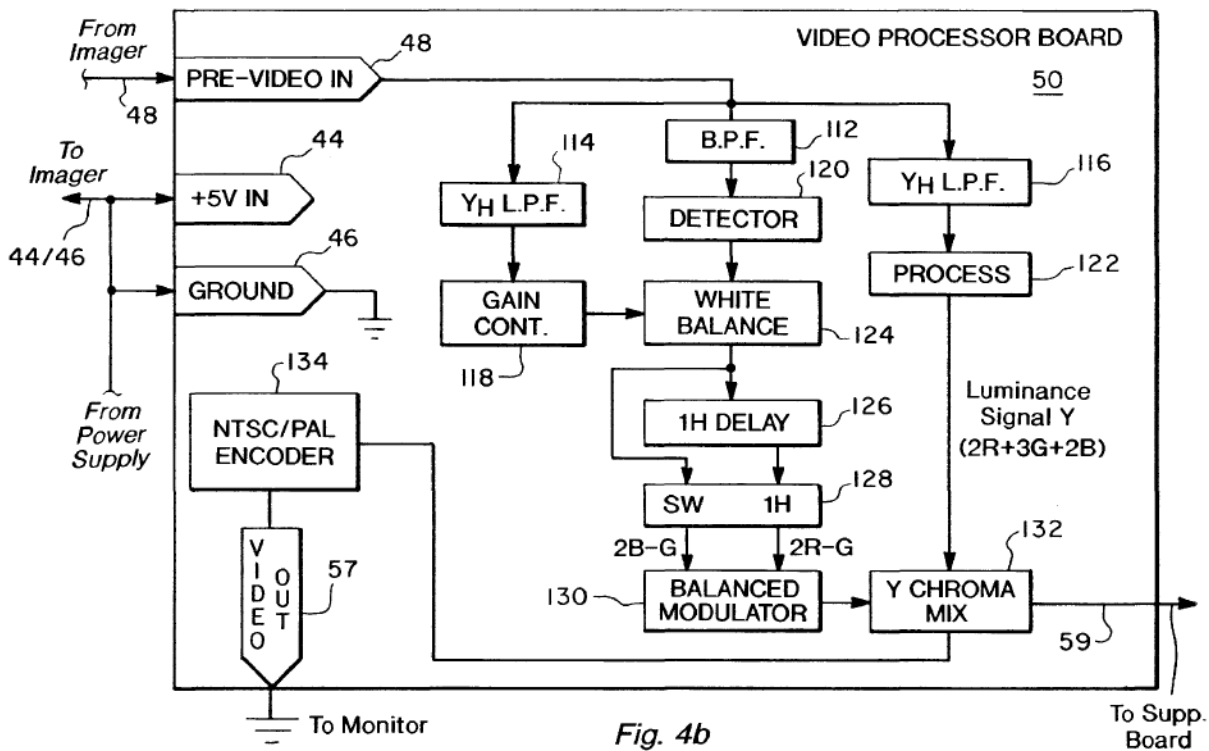


'052 patent, Figs. 2a, 2b.

50. In the endoscope 10 depicted above, an “[i]mage sensor 40 is illustrated as ... planar and square shaped” as opposed to “planar and circular shape[d].” ’052 patent, 9:3-6. Image sensor 40 is connected to boards 50 and 60 that are “longitudinally aligned with image sensor 40 along longitudinal axis XX” in a stacked relationship such that planes, respectively defined by the lengths and widths of image sensor 40 and boards 50 and 60, are offset from one another in a parallel configuration. ’052 patent, 10:4-8. The image is focused onto the image sensor by a lens group or system 42. ’052 patent, 9:8-13. The boards 50 and 60 contain processing circuitry that conditions the pre-video signal to place the signal in a form

that can be viewed directly on a standard video device. '052 patent, 9:31-37, 9:65-10:2; *see also* '052 patent, 10:29-57, 12:39-62, Fig. 2b. Timing and control circuitry for controlling the timing of operation of the image sensor can be on board 50 or on the image sensor 40 itself. '052 patent, 11:50-12:21. The imaging device may use a “wired connection[] for transferring video images to a video display.” '052 patent, 4:32-35. A battery 66 provides power for the camera system. '052 patent, Fig. 2a, 9:53-57, 10:20-36.

51. The '052 patent discloses specific structures for converting a pre-video signal to a post-video signal in its discussion of Figures 4b and 5a-e. '052 patent, 13:62-14:27, 15:7-19. For example, as shown in Figure 4b (reproduced below) the “pre-video signal” is passed through a series of filters and mixers to perform white balancing before being fed to a “NTSC/PAL encoder 134” that will “produce the post-video signal which may be accepted by a television.” '052 patent, 13:62-14:27.



'052 patent, Fig. 4b.

B. Prosecution History

52. The '052 patent issued from U.S. Patent Application No. 14/705,334, filed May 6, 2015 (the '334 Application). The '334 Application claims priority to a number of prior applications as a "continuation" or a "continuation-in-part."

53. The Examiner issued a Non-Final Office Action on August 13, 2015 rejecting prosecuted independent claims 1, 7, 13, and 19 and several dependent claims as obvious, including dependent claims specifying the image sensor has a generally square shape along the first plane. '052 Patent File History (Ex. 1002), 50. Applicant cancelled all claims and submitted new claims 25-31 on September 10, 2015. The new claims added limitations to the previously rejected claims reciting:

the “largest dimension of said image sensor along said first plane is between 2 and 12 millimeters” (claims 25, 26, 27); the “image sensor has a generally square shape along said first plane” (claim 25); and “said second circuit board being positioned in a stacked arrangement with respect to said first circuit board” rather than “offset from said first circuit board” (claim 26). ’052 Patent File History, 35-41. Notably, the Examiner previously found limitations requiring “a generally square shape” and the “second circuit board...in a stacked arrangement with respect to said first circuit board” obvious. ’052 Patent File History, 50 (rejecting prosecuted claim 2); US 9,667,896 File History (Ex. 1028), 120-122 (rejecting prosecuted claims 7 and 19). A Notice of Allowance issued September 21, 2015 and the ’052 patent issued November 17, 2015.

C. Claim Construction

54. I understand that for purposes of this *Inter Partes* Review, the standard for claim construction is the same as the standard used in federal district court litigation: claim terms should generally be given their ordinary and customary meaning as understood by one of ordinary skill in the art at the time of the invention and after reading the patent and its prosecution history.

55. I have interpreted the claims according to their plain and ordinary meaning consistent with the specification.

VIII. THE CHALLENGED CLAIMS ARE INVALID

56. It is my opinion that the Challenged Claims of the '052 patent are unpatentable as explained below.

Ground	References	Basis	Claims
1	Wakabayashi in view of Ackland	§103	1
2	Wakabayashi in view of Ackland and Suzuki	§103	1
3	Wakabayashi in view of Ricquier and Dierickx	§103	3 and 7
4	Swift in view of Ricquier and Suzuki	§103	2
5	Larson in view of Swift, Ricquier, and Suzuki	§103	2

A. Claim 1 Is Obvious Under §103 over Wakabayashi in View of Ackland (Ground 1)

1. Overview of U.S. Patent 5,903,706 (“Wakabayashi”) (Ex. 1027)

57. Wakabayashi (Ex. 1027) was filed August 22, 1995 and issued May 11, 1999, and I understand, is prior art to the '052 patent.

58. Wakabayashi describes a portable imager apparatus that includes both a video camera 22 and a liquid crystal display within its housing, enabling it to be “reduced in size and weight.” *See, e.g.,* Wakabayashi, Abstract (“An upside-down image, generated when a video camera is rotated about a horizontal axis to face to substantially the same direction as a display unit does, is electrically corrected to be an upright image. A video camera unit made compact to realize a reduction in weight of a video camera rotating mechanism.”), 1:6-9 (“The present invention

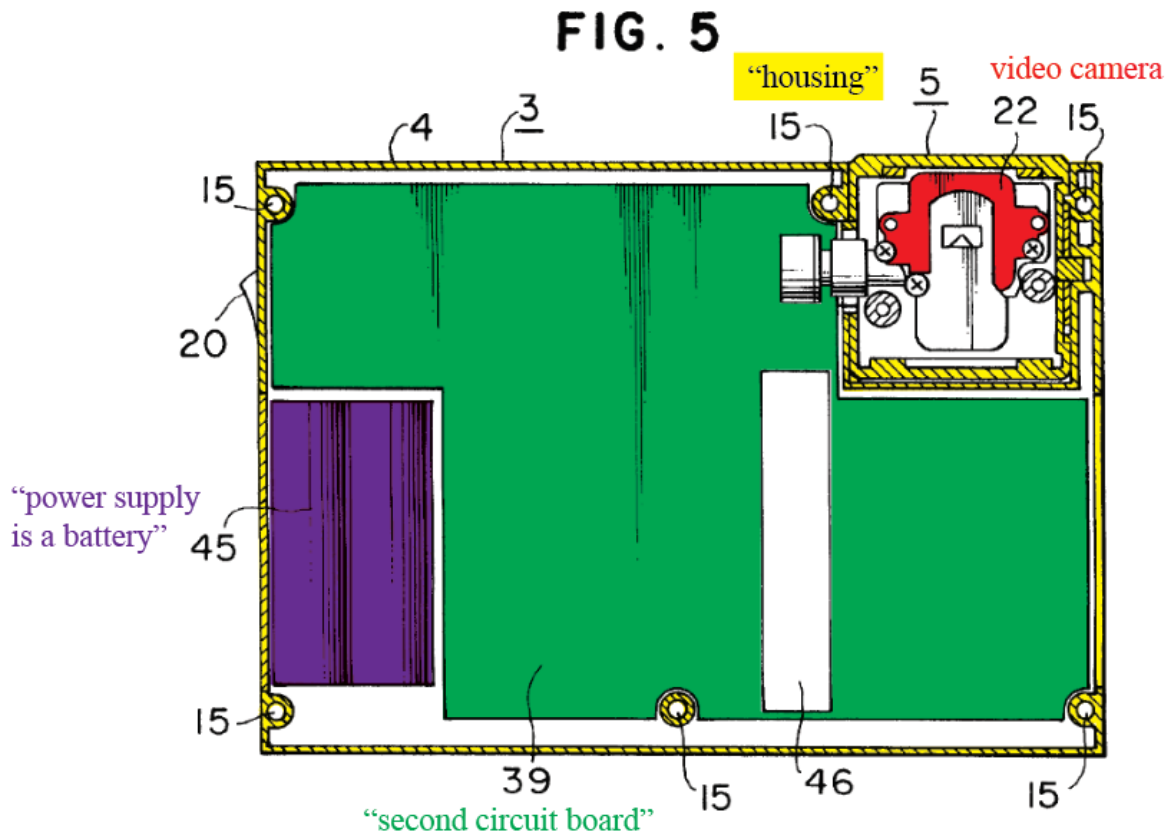
relates to a portable imager apparatus which includes a video camera as an imager unit, a direct-view type flat display as an electronic view finder or display, and a semiconductor memory or video tape recorder (VTR) as a storage or recording unit”), Fig. 1.²

59. Wakabayashi’s video camera unit includes an image sensor having both an “imager device 27” and a “circuit board 29.” *See, e.g.*, Wakabayashi, 5:56-59 (“The video camera 22 includes a shutter 23, a lens case 24, a lens 25, a quartz filter 26, an imager device 27, a mounting plate 28, and a camera circuit board 29.”), 6:47-49 (“[W]hile the imager device 27 is electrically connected to the camera circuit board 29 by soldering with the mounting plate 28 interposed therebetween.”), 9:10-14 (“FIG. 22 shows a block diagram of a circuit used in the first-third embodiments of the present invention. A camera head 100, which includes a light receiving lens, a solid-state imager device, a circuit for driving the solid-state imager device, and so on, generates an opto-electrically converted signal 101 which is inputted to a camera circuit 102.”), Fig. 7.

60. As shown in Figure 5 below, Wakabayashi discloses that its portable imager apparatus has, mounted within its housing (yellow), a video camera 22 (red)

² All emphasis and annotations herein are added unless otherwise noted. My annotations generally apply the language of the Challenged Claims.

(including “imager device 27” and “circuit board 29”), a second circuit board 39 (green) in a position offset from that of the video camera unit, and a battery 45 (purple).

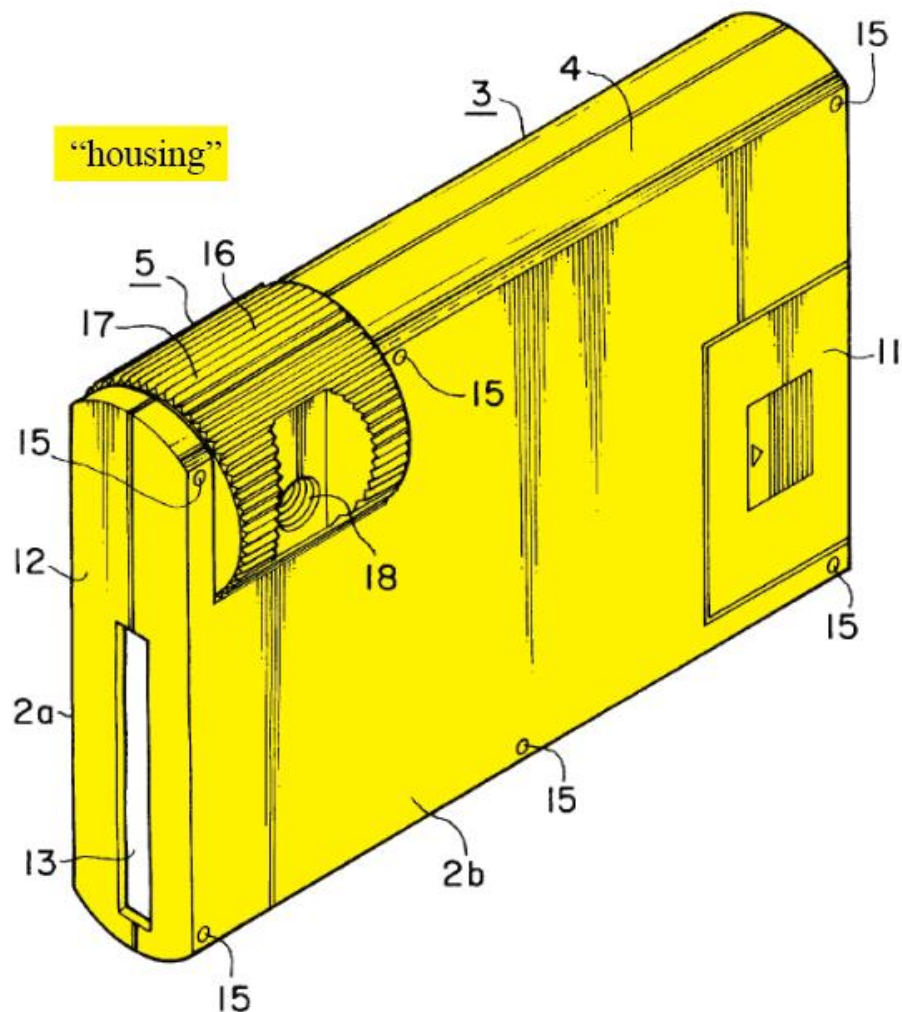


Wakabayashi, Fig. 5 (annotated).

61. As shown in Figure 2 below, the housing of the imager apparatus is formed by the assembly of “front panel 2a,” “rear panel 2b,” “camera case 16” and “battery cover 11.” See, e.g., Wakabayashi, 4:44-54 (“The imager apparatus 1 has a video camera unit 5 rotatably pivoted on a right end portion of an upper edge 4, a liquid crystal display 6 accommodated in the housing 3, a selection button 7 and a cursor key 8 arranged on the front panel 2a, a power supply switch 10 and a battery-

cover 11 arranged on a left side surface 9 of the housing 3, and a card slot 13 formed in a right side surface 12 of the housing 3 for inserting a PCMCIA card 14. The rear panel 2b of the housing 3 are formed with six screw holes 15 for assembling the housing 3. The video camera unit 5 has a camera case 16 formed with anti-slip knurl 17 on the surface thereof.”), Figs. 1-3, 5-6.

FIG. 2



Wakabayashi, Fig. 2 (annotated), *see also* Figs. 1, 3, 5-6.

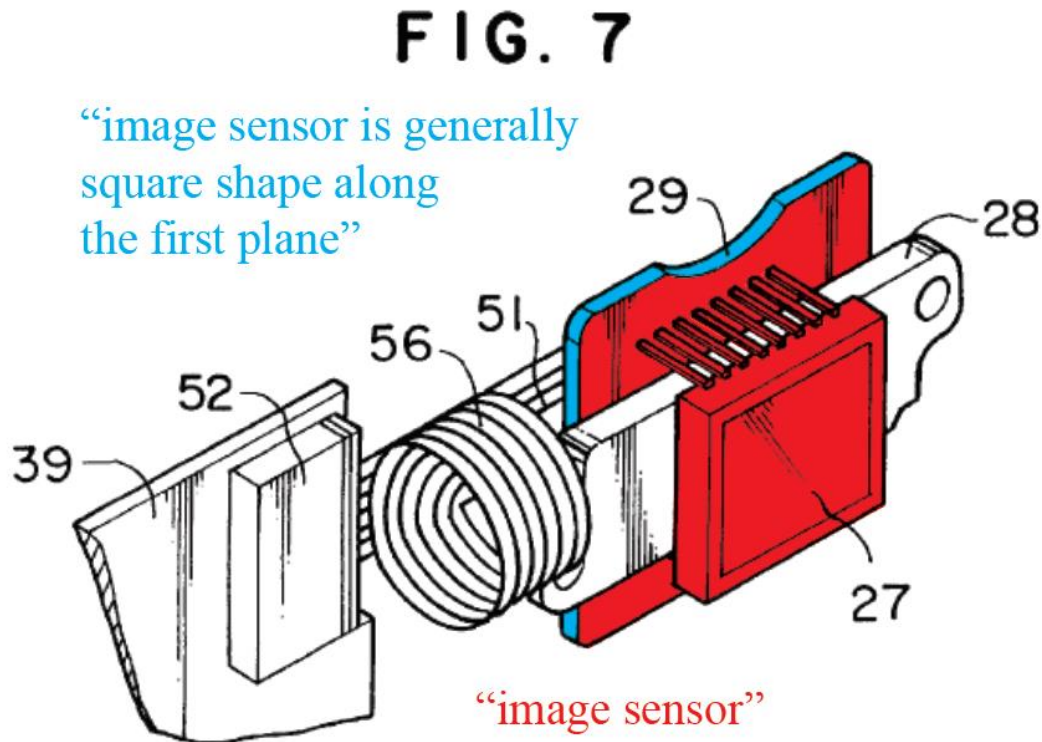
62. As illustrated in Figures 3 and 7 below, the image sensor is mounted in this housing and includes a first circuit board having a length and a width thereto (defining a first plane), as Wakabayashi discloses that the “imager device 27” is soldered on “circuit board 29” (having a length and width that define a first plane) that is “fixed on the mounting plate 28 with screws 30,” which “in turn is fixed to the camera case 16 with screws.” *See, e.g.,* Wakabayashi, 5:62-65 (“The camera circuit board 29 is fixed on the mounting plate 28 with screws 30, and the mounting plate 28 in turn is fixed to the camera case 16 with screws (*see* FIG. 6).”), 6:5-10 (“A liquid crystal panel 38 and a circuit board 39 are disposed in the housing 3. The circuit board 39 includes a signal processing circuit for the video camera unit 5, a driver circuit for the liquid crystal panel 38, a system circuit, a power supply circuit, and so on.”), 6:20-27 (“FIG. 5 is a cross-sectional view taken along a line B--B in FIG. 1. It can be seen that the circuit board 39 is disposed in the housing 3, a battery 45 is disposed in a left side portion of the housing 3, and the video camera unit 5 is rotatably pivoted on a right end portion of the upper edge 4. The housing 3 further includes a power supply switch 10, six screw holes 15, and a host connector 46 for the PCMCIA card 14.”), Fig. 3.

63. Wakabayashi’s “imager device 27” is a “solid state imager device.” *See, e.g.,* Wakabayashi, 9:10-14 (“FIG. 22 shows a block diagram of a circuit used in the first-third embodiments of the present invention. A camera head 100, which includes

a light receiving lens, a solid-state imager device, a circuit for driving the solid-state imager device, and so on, generates an opto-electrically converted signal 101 which is inputted to a camera circuit 102.”). A person of ordinary skill in the art would have understood “imager device 27” includes a planar semiconductor substrate on which the imager device is fabricated. *See, e.g.,* Ackland, Abstract, 1:44-49 (“In a typical CMOS active pixel, charge collection and transfer is accomplished as follows. The charge carriers can be collected in the photo site via a photo gate. The charge packet is stored in the photo site in spatially defined depletion regions or potential wells in the semiconductor substrate beneath the photo site.”); Mendis (Ex. 1036, publicly available through University of Wisconsin Memorial Library 5/27/1994, and I understand is prior art to the ’052 patent), 23 (disclosing that “electrons [] are generated in the substrate below a photogate” of the CMOS APS); Dickinson (Ex. 1037, publicly available at the Sixteenth Conference on Advanced Research in VLSI 3/29/1995, and I understand is prior art to the ’052 patent), 216-218 (explaining that the CMOS pixel includes “semiconductor substrate surface regions under the photo-gate (PG) and the transfer gate (TG)”), Figure 2 (illustrating the flow of charged carriers within the substrate regions).

64. As illustrated in Figure 7, the image sensor of Wakabayashi is a generally square shape along the first plane—defined by the length and width of

either the imaging device 27 or the circuit board 29, is generally square. *See, e.g.,* Wakabayashi, Fig. 7.



Wakabayashi, Fig. 7 (annotated).

65. Furthermore, to the extent it is argued that Wakabayashi’s imager device 27 is not of a “generally square shape along the first plane,” at minimum, a person of ordinary skill in the art would have been motivated to make Wakabayashi’s “imager device 27” and “circuit board 29” a generally square shape along the first plane, as the shape of the image sensor is an engineering consideration, and generally square shaped image sensors were well known in the art. *See, e.g.,* VM 5402 (Ex. 1035, publicly available on 6/8/1997 as recorded by Internet Archive, and I understand is prior art to the ’052 patent), 4-5 (illustrating the circuitry on the

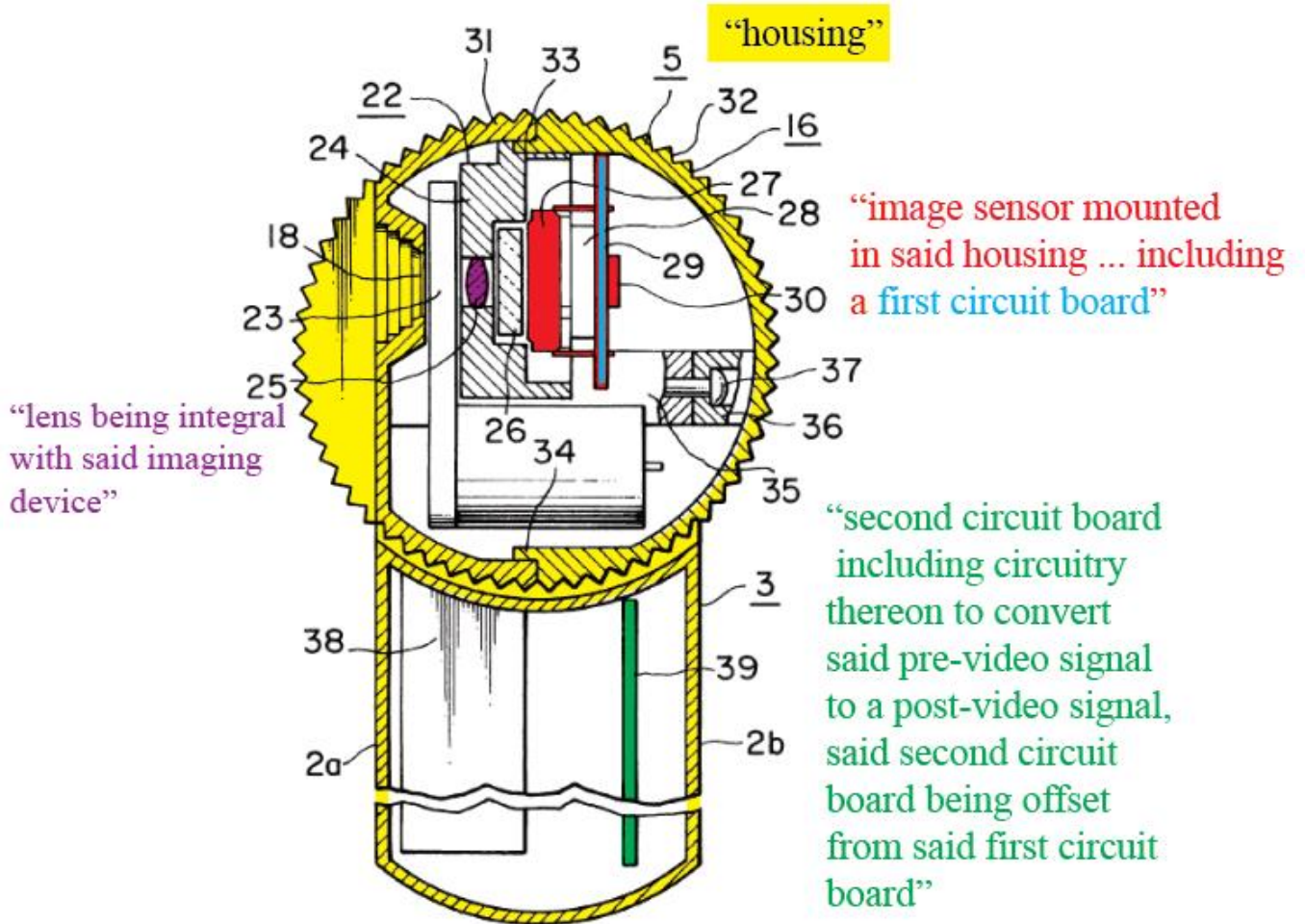
component side of the printed circuit board (PCB) to which the sensor package is mounted); Chamberlain (Ex. 1044, issued 6/22/1993, and I understand is prior art to the '052 patent), 4:20-22 (“[T]he camera casing 10 is basically a square tube when viewed in the cross section.”), 3:55-56 (“The driver board means 13 is adapted to receive any of a plurality of image sensors 17 therein....”), Fig. 2 (illustrating a “image sensor 17” mounted to a square “driver board” within the square camera casing); Mendis, 20-21 (Fig 1 illustrates a “Photograph of ... 128×128 array” having generally square dimensions, and discloses “die areas of the large and small arrays [as] $6.8 \text{ mm} \times 6.8 \text{ mm}$ and $2.20 \text{ mm} \times 2.25 \text{ mm}$ respectively”).

66. In addition, while Wakabayashi does not expressly disclose the dimensions of “circuit board 29,” it would have been an obvious implementation choice to use a circuit board having a largest dimension between 2 and 12 millimeters because boards of such size were well-known at the time for mounting to an image sensor. For example, as I discussed in Section VIII.B, Suzuki teaches that “chip connecting board 226,” to which “image pickup chip 221” is mounted, is between 2 and 12 millimeters. *See, e.g.,* Suzuki, 4:6-11 (“Further, in this embodiment of the invention, in the case where the solid-state image pickup chip of $1/3$ inch (8.5 mm) is used, the outer diameter of the camera head is about 10 mm, and therefore is smaller about 5 mm than that of the conventional camera head.”), 4:58-65 (“[T]here is provided an advantage that the outer diameter of the camera

head can be reduced to a small size close to the diagonal length of the solid-state image pickup chip. This provides an advantage that an image of a narrow portion, such as the interior of a pipe and the interior of a precision machine, can be picked up, which has not heretofore been achieved”), 1:53-56 (“It is an object of this invention provide a camera head for a solid-state image pickup device which camera head has an outer diameter closer to a diagonal length of a solid-state image pickup chip.”), 3:15-31 (“The chip-connecting board 226, the circuit board 227 and the connector board 228 are arranged in such a manner that their side electrodes 226e, 227e and 228e are disposed in registry with one another, and these three boards are aligned with each other. They are connected together by the connection pins 229 to provide the circuit module 222. A surface of the solid-state image pickup chip 221 opposite to the light-receiving surface thereof is bonded to the chip-connecting board 226 through the adhesive 225. [¶] Each outer-lead 221m is bent through about 90 at a point near the chip 221, and is soldered to the side electrodes 226e, 227e and 228e of the boards 226, 227 and 228 to make electrical connections among the boards, thereby constituting the image pickup unit 22.”), 4:58-61 (“[T]here is provided an advantage that the outer diameter of the camera head can be reduced to a small size close to the diagonal length of the solid-state image pickup chip.”), Fig. 2.

67. The camera head, which includes the solid-state imager device, generates a pre-video signal in the form of “an opto-electrically converted signal,” which is then converted to a post-video signal. *See, e.g.,* Wakabayashi, 9:10-14 (“FIG. 22 shows a block diagram of a circuit used in the first-third embodiments of the present invention. A camera head 100, which includes a light receiving lens, a solid-state imager device, a circuit for driving the solid-state imager device, and so on, generates an opto-electrically converted signal 101 which is inputted to a camera circuit 102.”), Fig. 22.

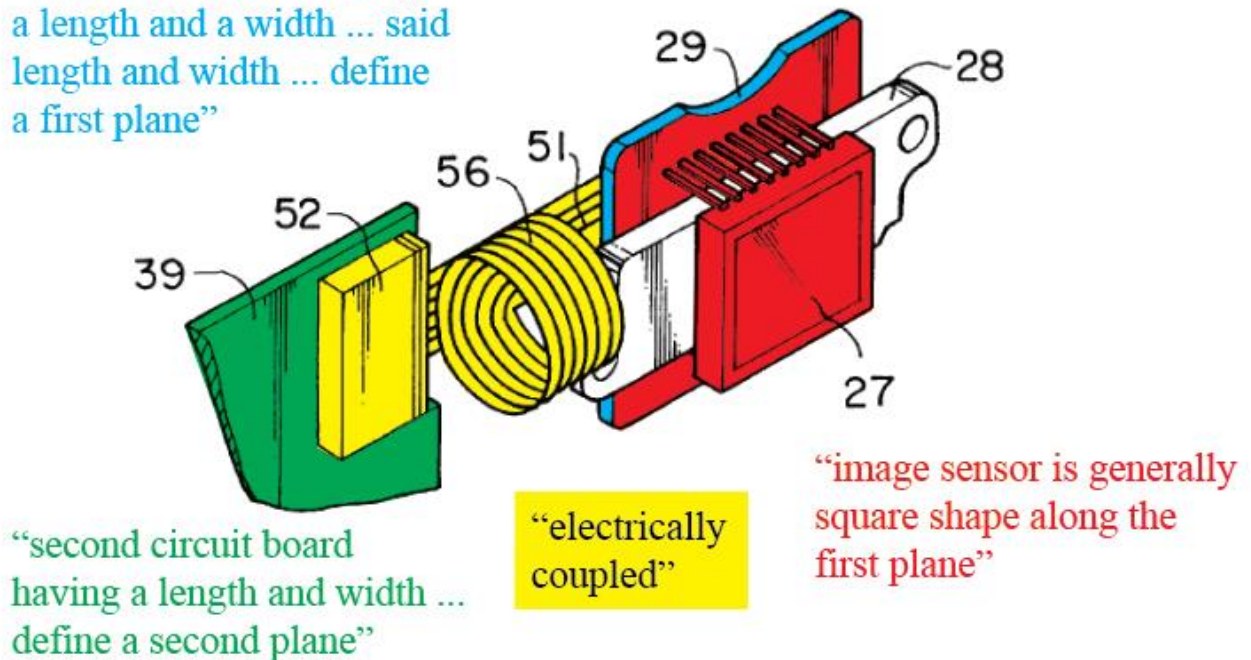
FIG. 3



Wakabayashi, Fig. 3 (annotated).

FIG. 7

“first circuit board having a length and a width ... said length and width ... define a first plane”



Wakabayashi, Fig. 7 (annotated).

68. Figures 3 and 7 (above) also illustrate a second circuit board having a length and a width thereto (defining a second plane), mounted in the housing, and electrically coupled to the first circuit board, as Wakabayashi discloses “circuit board 39 is disposed in the housing” and electrically connected to circuit board via “flexible board 51” to process the signal from the video camera unit. *See, e.g.,* Wakabayashi, 6:5-10 (“A liquid crystal panel 38 and a circuit board 39 are disposed in the housing 3. The circuit board 39 includes a signal processing circuit for the video camera unit 5, a driver circuit for the liquid crystal panel 38, a system circuit,

a power supply circuit, and so on.”), 6:20-27 (“FIG. 5 is a cross-sectional view taken along a line B--B in FIG. 1. It can be seen that the circuit board 39 is disposed in the housing 3, a battery 45 is disposed in a left side portion of the housing 3, and the video camera unit 5 is rotatably pivoted on a right end portion of the upper edge 4. The housing 3 further includes a power supply switch 10, six screw holes 15, and a host connector 46 for the PCMCIA card 14.”), 6:35-38 (“The flexible board 51 has one end connected to the camera circuit board 29 by soldering and the other end connected to a connector 52 on the circuit board 39.”), Figs. 3, 7. As can be seen in Figures 3 and 7, circuit board 39 is vertically and horizontally offset from circuit board 29 and the plane defined by the length and width of circuit board 39 is substantially parallel with the plane defined by the length and width of circuit board 29. *See, e.g., Wakabayashi, Figs. 3, 7.*

69. Wakabayashi provides the rough dimensions of its imager apparatus and explains that the user holds the part of the housing 3 of the camera where circuit board 39 is located in one hand, while the video camera unit where circuit imaging device 27 and circuit board 29 are located is “made small” such that it may be manipulated by a finger and thumb. *See, e.g., Wakabayashi, 3:39-45 (“The video camera unit is made small and pivoted on an edge of the housing for rotation about an axis parallel to the edge, so that a less strength is required for joining members and accordingly the joining members can be reduced in size and weight. This*

structure also allows the user to manipulate the video camera with a thumb or index finger for setting an imaging angle of the video camera unit.”), 7:20-24 (“[S]ince the imager apparatus 1 allows the user to hold the housing 3 with the left hand and rotate the video camera unit 5 with the thumb and index finger of the left hand for adjusting an imaging angle, the user can manipulate the imager apparatus 1 only with a single hand.”), 4:58-5:2 (“FIG. 1 shows a state of the imager apparatus 1 in which ... the user may support the housing 3 with his left hand to hold the liquid crystal display 6 at an angle which facilitates the viewing, and hold and rotate the video camera unit 5 with the thumb and index finger of his right hand.”), Abstract (“A video camera unit made compact to realize a reduction in weight of a video camera rotating mechanism. ... This structure also allows the user to adjust the angle of the video camera unit only with the thumb and index finger.”).

70. Wakabayashi discloses that “circuit board 39 includes a signal processing circuit for the video camera unit 5” that outputs a “continuous television signal” to the “video monitor unit” (*i.e.*, “liquid crystal display”). *See, e.g.*, Wakabayashi, 1:6-15, 5:7-12, 6:5-10 (“A liquid crystal panel 38 and a circuit board 39 are disposed in the housing 3. The circuit board 39 includes a signal processing circuit for the video camera unit 5, a driver circuit for the liquid crystal panel 38, a system circuit, a power supply circuit, and so on.”), 10:2-7 (“For producing a continuous television signal, the RAM 105 may be provided with a capacity of

storing two field portions of video signal 103, such that a field of a video signal written into the RAM 105 one field period before is read therefrom at the same time the current field of the video signal is written thereinto.”), 10:15-17 (“The video signal 111 is outputted to a video monitor unit 113, a video recording unit 119, and a video signal output unit 120 through an output terminal 117.”).

71. Wakabayashi further discloses that “circuit board 39” is coupled to the “liquid crystal display 6,” and includes a “driver circuit” for the display’s “liquid crystal panel 38.” See, e.g., Wakabayashi, 6:5-10 (“A liquid crystal panel 38 and a circuit board 39 are disposed in the housing 3. The circuit board 39 includes a signal processing circuit for the video camera unit 5, a driver circuit for the liquid crystal panel 38, a system circuit, a power supply circuit, and so on.”). Wakabayashi discloses that the “liquid crystal display serv[es] as a display unit” to display images from the “video signal 111 [] outputted” from “circuit board 39” and “allows a user to monitor an image.” See, e.g., Wakabayashi, Abstract, 10:15-17 (“The video signal 111 is outputted to a video monitor unit 113, a video recording unit 119, and a video signal output unit 120 through an output terminal 117.”), 1:6-15 (“The present invention relates to a portable imager apparatus which includes a video camera as an imager unit, a direct-view type flat display as an electronic view finder or display, and a semiconductor memory or video tape recorder (VTR) as a storage or recording unit, wherein the video camera, the flat display, and the recording unit are

integrated with each other, and more particularly to an imager apparatus which allows a user to monitor an image on a flat display to adjust the angle of the video camera apparatus while imaging a subject.”), 5:7-12 (“For example, when the cursor 20 is moved to ‘Camera’ within the items 19 and the selection button 7 is depressed to select a camera function, the imager apparatus 1 functions as a video camera. In response, the video camera unit 5 is powered on to display an imaged subject on the liquid crystal display 6.”).

72. Wakabayashi discloses “camera circuit 102” receives “an opto-electrically converted signal” generated by the “solid-state imager device” in the “camera head 100.” See, e.g., Wakabayashi, 9:10-18 (“A camera head 100, which includes a light receiving lens, a solid-state imager device, a circuit for driving the Solid-State imager device, and so on, generates an opto-electrically converted signal 101 which is inputted to a camera circuit 102. The camera circuit 102, which includes a camera signal processing circuit, a synchronization signal generator circuit, and so on, generates a video signal 103 in a television signal format from the opto-electrically converted signal 101.”). In describing Figure 22, Wakabayashi explains that the camera circuit 102 converts the opto-electrically converted signal into a “video signal 103 in a television signal format” and outputs the signal to the “video monitor unit.” See, e.g., Wakabayashi, 9:10-18 (“A camera head 100, which includes a light receiving lens, a solid-state imager device, a circuit for driving the

Solid-State imager device, and so on, generates an opto-electrically converted signal 101 which is inputted to a camera circuit 102. The camera circuit 102, which includes a camera signal processing circuit, a synchronization signal generator circuit, and so on, generates a video signal 103 in a television signal format from the opto-electrically converted signal 101.”), Fig. 22. Wakabayashi further explains that “camera head 100” and “camera circuit 102” constitute the “video camera” unit of the imager apparatus. *See, e.g.*, Wakabayashi 9:18-21 (“The camera head 100 and the camera circuit 102 surrounded by dotted rectangles constitute the video camera of the present invention.”).

73. In addition, while Wakabayashi discloses that the video camera “includes a camera signal processing circuit, a synchronization signal generator circuit, and so on,” that “generates a video signal 103 in a television signal format from the opto-electrically converted signal 101” (Wakabayashi, 9:15-19), for the reasons I provide below, it would have been an obvious implementation choice to instead locate this circuitry to convert the pre-video signal to a post-video signal on circuit board 39 and couple it to the power supply circuit.

74. A person of ordinary skill in the art would have been motivated and found it obvious and straightforward to locate the processing circuitry to convert the pre-video signal to a post-video signal on Wakabayashi’s “circuit board 39 [which] includes a signal processing circuit..., a driver circuit..., a system circuit, a power

supply circuit, and so on” because it is the larger of two circuit boards in the imager apparatus and there is more space where circuit board 39 is mounted than in the camera head where circuit board 29 is mounted. *See, e.g., Wakabayashi, 6:5-10 (“A liquid crystal panel 38 and a circuit board 39 are disposed in the housing 3. The circuit board 39 includes a signal processing circuit for the video camera unit 5, a driver circuit for the liquid crystal panel 38, a system circuit, a power supply circuit, and so on.”), 9:15-19 (The camera circuit 102, which includes a camera signal processing circuit, a synchronization signal generator circuit, and so on, generates a video signal 103 in a television signal format from the opto-electrically converted signal 101.”), Figs. 3, 5. Furthermore, by mounting this processing circuitry on circuit board 39 instead of circuit board 29, the size of circuit board 29 is advantageously reduced and the video camera unit that rotates is made smaller. *See, e.g., Wakabayashi, Abstract (“A video camera unit made compact to realize a reduction in weight of a video camera rotating mechanism. ... Since the video camera unit is composed of minimally necessary parts and is rotatably pivoted on an edge of the housing, a rotatable joining portion of the video camera unit with the housing can be reduced in size and weight. This structure also allows the user to adjust the angle of the video camera unit only with the thumb and index finger.), 2:37-39 (“It is another object of the present invention to provide an imager apparatus which only requires small and light joining members for joining a camera**

with a housing.”), 3:40-44 (*“The video camera unit is made small and pivoted on an edge of the housing for rotation about an axis parallel to the edge, so that a less strength is required for joining members and accordingly the joining members can be reduced in size and weight.”*), 14:6-10 (“Fourth, *since the video camera unit is made compact* and pivoted for rotation about an axis parallel to an edge of the housing, a less strength is required for joining members to join the video camera with the housing. Therefore, the *joining members can be reduced in size and weight.*”), Figs. 3, 5. Wakabayashi teaches one objective is to make “the video camera unit... small,” “composed of minimally necessary parts,” and “compact to realize a reduction in weight of [the] ... rotating mechanism,” so that “less strength is required” for the “rotatable joining portion” to “join the video camera with the housing” portion of the imager apparatus. *See, e.g.,* Wakabayashi, Abstract, 2:37-39, 3:40-44, 14:6-10. Placement of the processing circuitry on circuit board 39 furthers this objective.

75. The number of circuit boards and configuration of circuitry across the circuit boards was a well-known engineering consideration guided by the dimensions of the intended housing. For example, Swift teaches that “the rear housing portion 30 may be replaced by another portion of different configuration, designed to accommodate additional components or different components of different configuration.” Swift, 10:12-16. As another example, Roustaei similarly

teaches that “the number of printed circuit boards is a design choice” and that “all the hardware could be contained on one board or ... whatever quantity [of boards] permits the device's components to be fitted into the dimensions of the intended housing.” Roustaei (Ex. 1030, which was filed 08/1/1996 and issued 5/26/1998, and I understand is prior art to the '052 patent), 43:38-44 ; *see also, e.g.,* Roustaei, 54:7-11 (disclosing that “it will be apparent to those skilled in the art that the choice of number of boards depends on many factors such as packaging constraints.”); Cotton (Ex. 1031, which issued 12/16/1986, and I understand is prior art to the '052 patent), 13:30-35 (“[T]he fact that certain of the I/O devices are included on the CPU board ... and others are included on the video board ... is merely a matter of design choice.”); Crosetto (Ex. 1032, which was published 8/17/94, and I understand is prior art to the '052 patent), 15:35-46 (“[P]lacement and arrangement of processors and connectors upon the PCB is a matter of design choice.”).

76. Even with respect to circuitry to convert pre-video signals to post-video signals, it was a well-known engineering consideration to move the circuitry from a circuit board directly attached to the image sensor chip to one that is remote to the image sensor chip. For example, Ackland teaches that it was known to “route[]” the “output signals...to suitable processing circuitry,” which as Ackland’s Figure 6 shows, is not part of the “active pixel imaging system.” Ackland, 8:48-53 (“Output signals from the amplifiers 18 are provided to the common output line 19 in serial

fashion based on timing control signals from the timing control 20. The output signals *are routed to suitable processing circuitry*, not shown.”), Fig. 6.

77. In addition, the following references further confirm that a person of ordinary skill in the art would have been motivated to move the circuitry for converting pre-video signals to post-video signals to circuit board 39 and would have had a reasonable expectation of success that such an implementation would work and provide the expected functionality. Swift teaches the implementation choice of mounting the “circuitry components ... [to] process signal images received” from the CMOS image sensor 51 on either the same board on which the image sensor 51 is mounted—circuit board 52 when circuit boards 52 and 53 are combined, or a second circuit board 53 when both circuit board 52 and circuit board 53 are provided. See e.g., Swift, 8:33-9:21 (“An image sensor 51 is mounted on a circular printed circuit board 52.... A further printed circuit board 53 is mounted on the first printed circuit board 52, substantially at right angles thereto. Various circuitry components are mounted on the circuit board 53, to provide power to the image sensor 51, process image signals received therefrom, and also to process audio signals from a miniature microphone 54 which is mounted within the radially extending passage 28 and connected to the printed circuit board 52 and/or 53. ... [¶] A single circuit board (e.g. circular) may be provided, instead of the two circuit boards 52 and 53.”), 10:12-16 (“If desired, the rear housing portion 30 may be replaced by another portion of

different configuration, designed to accommodate additional components or different components of different configurations.”), 18:25-33 (“In this specification, terms of absolute orientation are used conveniently to denote the usual orientation of items in normal use and/or as shown in the accompanying drawings. However, such items could be disposed in other orientations, and in the context of this specification, terms of absolute orientation, such as ‘top’, ‘bottom’, ‘left’, ‘right’, ‘vertical’ or ‘horizontal’, etc. are to be construed accordingly, to include such alternative orientations.”), Fig. 2. Swift further discloses additional “processing circuitry” can be located “external” to the camera. *See, e.g.*, Swift, 9:13-17 (“A cable 55 is connected to the printed circuit board 53, and passes through the rear 15 bores 32, 33, to provide a connection between the miniature video camera 50 and external processing circuitry (not shown).”). Monroe teaches a CMOS imager with the choice of including “video processing circuitry...within the circuit board contained within the diagnostic instrument” or “[a]lternately,...within the combined power supply and lighting unit” that is remote from the CMOS image sensor. *See, e.g.*, Monroe (Ex. 1007, filed 3/17/1997 and issued 7/6/1999, and I understand is prior art to the ’052 patent), 3:36-62 (“A circuit board is connected to the imager which extends into the elongated body portion and includes processing circuitry for converting a raw video output signal from the imager into a monitor ready standard format signal suitable for displaying the image of the target object or area on a

monitor or ... other known display interface. [¶] ...The present video otoscope, as used in this system, also includes a flexible conduit for carrying light and power from the power supply and lighting unit to the tip segment. The flexible conduit also transmits a monitor ready video signal from the imager through the video processing circuitry to the video monitor. Alternately, the video processing circuitry can be contained within the combined power supply and lighting unit rather than within the circuit board contained within the diagnostic instrument”), 8:8-11 (“It should be noted that the processing circuitry should not be limited to the plug-in connector, for example, circuitry could be contained within the peripheral device 16 or the combined light box/power supply 14.”), Fig. 3 (illustrating “light box/power supply” external to the video otoscope). And, as discussed above, a person of ordinary skill in the art would have been motivated to locate the processing circuitry to convert the pre-video signal to a post-video signal on Wakabayashi’s “circuit board 39 because it is the larger of the two circuit boards, and would have reduced the size of the video camera unit, and would have had a reasonable expectation of success it would work as expected.

78. In addition, Wakabayashi’s Figure 3 illustrates a lens mounted in the housing and integral with Wakabayashi’s imager apparatus, as “lens 25” in “lens case 24” is “secured” to the “mounting plate 28 ... with a screw.” *See, e.g.*, Wakabayashi, 5:56-58 (“The video camera 22 includes a shutter 23, a lens case 24,

a lens 25, a quartz filter 26, an imager device 27, a mounting plate 28, and a camera circuit board 29.”), 6:17-19 (“The shutter 23 is secured to the lens case 24 with a screw 43. The mounting plate 28 is also secured to the lens case 24 with a screw 44.”). Wakabayashi discloses that “lens 25” is used to “focus[]” an “image ... on the imager device 27.” See, e.g., Wakabayashi, 5:56-61 (“The video camera 22 includes a shutter 23, a lens case 24, a lens 25, a quartz filter 26, an imager device 27, a mounting plate 28, and a camera circuit board 29. When the shutter 23 is opened, light penetrates through the imaging hole 18, and an image of a subject is focused on the imager device 27 by the lens 25.”).

79. Figure 5 of Wakabayashi (above) also discloses that the portable imager apparatus is powered by “battery 45 [] disposed in ... housing 3.” See, e.g., Wakabayashi, 6:21-27 (“FIG. 5 is a cross-sectional view taken along a line B--B in FIG. 1. It can be seen that the circuit board 39 is disposed in the housing 3, a battery 45 is disposed in a left side portion of the housing 3, and the video camera unit 5 is rotatably pivoted on a right end portion of the upper edge 4. The housing 3 further includes a power supply switch 10, six screw holes 15, and a host connector 46 for the PCMCIA card 14.”). Wakabayashi teaches that the imager apparatus has a “power supply switch 10 on the housing” and that the “video camera unit” is “powered on” in order to “display an imaged subject on the liquid crystal display.” See, e.g., Wakabayashi, 5:9-11 (“In response, the video camera unit 5 is powered on

to display an imaged subject on the liquid crystal display 6.”). A person of ordinary skill in the art would have understood that, as a portable device, with a battery as the only disclosed source of power, the battery provides power to both the “circuit board 29,” providing power to circuitry thereon and the imaging device 27, and to the second circuit board 39, which includes a “power supply circuit.” *See, e.g.,* Wakabayashi, 6:21-27 (“FIG. 5 is a cross-sectional view taken along a line B--B in FIG. 1. It can be seen that the circuit board 39 is disposed in the housing 3, a battery 45 is disposed in a left side portion of the housing 3, and the video camera unit 5 is rotatably pivoted on a right end portion of the upper edge 4. The housing 3 further includes a power supply switch 10, six screw holes 15, and a host connector 46 for the PCMCIA card 14.”), 6:7-10 (“The circuit board 39 includes a signal processing circuit for the video camera unit 5, a driver circuit for the liquid crystal panel 38, a system circuit, a power supply circuit, and so on.”), Fig. 5.

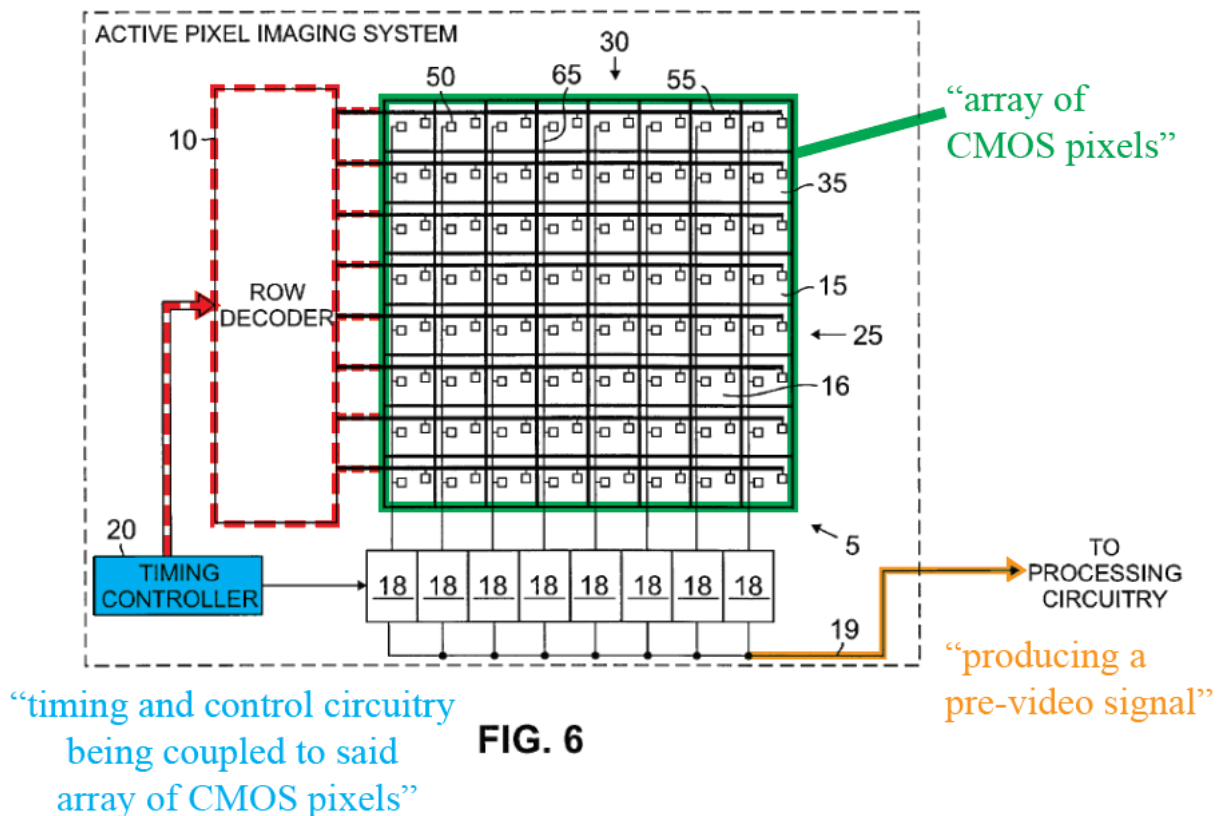
80. I note that Wakabayashi discloses additional embodiments that provide optional configurations that selectively power an arrangement converter based upon camera orientation. No aspect of those options is relied upon in the ground herein.

2. Overview of U.S. Patent 5,835,141 (“Ackland”) (Ex. 1006)

81. Ackland (Ex. 1006) was filed July 3, 1996 and issued November 10, 1998, and I understand, is prior art to the ’052 patent.

82. Ackland describes an active pixel imaging system using a “CMOS active pixel array” that may be used as a solid-state camera. *See, e.g.*, Ackland, 1:35-38, 7:62-63.

83. Ackland describes circuitry for timing and control of the array of CMOS pixels to generate a pre-video signal that is output in serial fashion over a pre-video conductor. *See, e.g.* Ackland, 8:24-35, 8:45-52, Fig. 6. As shown in the exemplary active pixel image sensor shown in Figure 6 below, Ackland teaches a timing controller coupled to the CMOS pixel array through row decoder 10. Ackland teaches that “[i]n operation, a timing controller 20 provides timing signals to the row decoder 10” and “[i]n response, the decoder 10 sequentially activates each row 25 of active pixels 35 via the control lines 55 to detect light intensity and to generate corresponding output voltage signals during each frame interval.” Ackland, 8:24-35. The output voltage signals are amplified by amplifiers 18 and “[o]utput signals from the amplifiers 18 are provided to the common output line 19 in serial fashion based on timing control signals from the timing controller 20.” Ackland, 8:45-52, 7:59-8:9, Fig. 6.



Ackland, Fig. 6 (annotated).

3. Motivation to Combine Wakabayashi and Ackland

84. A person of ordinary skill in the art would have been motivated and found it obvious and straightforward to employ Ackland’s express implementation detail teachings of an array of CMOS active pixels including its timing controller and pre-video conductor in implementing Wakabayashi’s imager apparatus.

85. While Wakabayashi discloses that the image sensor uses a “solid-state imager device” and a “circuit for driving the solid-state imager device” to “generate[] an opto-electrically converted signal” (Wakabayashi, 9:11-15 (“A camera head 100, which includes a light receiving lens, a solid-state imager device, a circuit for driving

the solid-state imager device, and so on, generates an opto-electrically converted signal 101 which is inputted to a camera circuit 102.”), Wakabayashi does not expressly state that its “imager device 27 [] electrically connected to the camera circuit board 29” includes an array of CMOS pixels. Ackland expressly provides this additional implementation detail for “an imaging system ... used as a solid-state camera,” which includes a “CMOS ... pixel array” for receiving images thereon—a feature the ’052 patent recognizes was well known. *See, e.g.*, Ackland, 1:35-38 (“Like charge coupled devices and MOS diode arrays, each pixel in a CMOS active pixel array includes a sensing element capable of converting optical images into electronic signals.”), 2:19-23 (“A CMOS active pixel characterized by a single layer of polysilicon for forming the photo gate and the transfer gate (‘single-polysilicon active pixel’), a method for operating the pixel, and pixel arrays based on such a pixel are disclosed.”), 7:44-47 (“The single-polysilicon CMOS active pixel 36 of the present invention may be comprised of the same elements that are used in a double polysilicon active pixel for providing read-out, reset and buffering functions.”), 7:59-65 (“A plurality of single polysilicon active pixels 36 according to the present invention may be arranged to form a single-polysilicon active pixel imaging system, such as the exemplary imaging system 1 shown in FIG. 6. Such an imaging system may be used as a solid-state camera.”), Fig. 6; ’052 patent, 2:6-9 (“One particularly

notable advance in the area of CMOS imagers including active pixel-type arrays is the CMOS imager described in U.S. Pat. No. 5,471,515 to Fossum, et al.”).

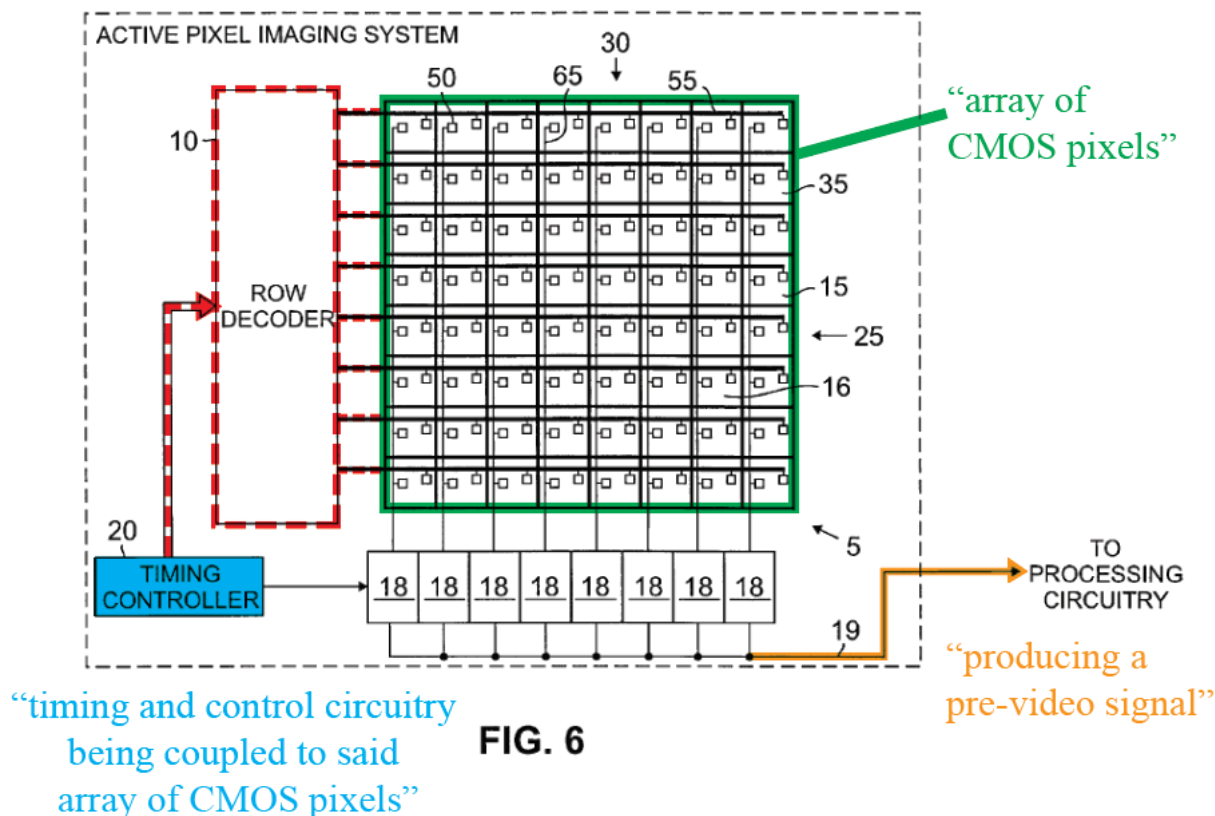
86. In addition, while Wakabayashi does not expressly disclose that its pixels each include an amplifier, Ackland provides this additional implementation detail—another feature the ’052 patent recognizes was known. *See, e.g.*, Ackland, 5:7-10 (“The voltage-follower transistor 125 amplifies the video signal by an amount sufficient to overcome the relatively large load offered by the common output conductor 65.”), 3:20-25 (“Referring to FIG. 1, the active pixel 35 includes a photo gate 101 charge-coupled to a transfer gate 107 that is charge-coupled to a diffusion region 110. The active pixel 35 further includes a reset transistor 120, an amplifier formed by a voltage follower-transistor 125, and a select transistor 130.”), Fig. 6; ’052 patent, 1:66-2:1 (“active pixel-type CMOS imagers which consist of randomly accessible pixels with an amplifier at each pixel site”)).

87. Similarly, while Wakabayashi does not detail the timing and control circuitry of its “imager device 27 [] electrically connected to the camera circuit board 29,” Ackland describes circuitry including a “timing controller 20 provid[ing] timing signals” that control the imaging system “to achieve a desired frame rate”—another feature the ’052 patent recognizes was well known. *See, e.g.*, Ackland, 8:24-35 (“In operation, a timing controller 20 provides timing signals to the row decoder 10. In response, the decoder 10 sequentially activates each row 25 of active pixels 35 via

the control lines 55 to detect light intensity and to generate corresponding output voltage signals during each frame interval. In the context of an array of pixels, the term 'frame' refers to a single complete cycle of activating and sensing the output from each pixel 35 in the array a single time over a predetermined frame time period. The timing of the imaging system is controlled to achieve a desired frame rate, such as 30 frames per second.”); ’052 patent, 2:6-19 (“One particularly notable advance in the area of CMOS imagers including active pixel-type arrays is the CMOS imager described in U.S. Pat. No. 5,471,515 to Fossum, et al. ... can incorporate a number of other different electronic controls that are usually found on multiple circuit boards of much larger size ... timing and control circuits ... can be placed on the same circuit board containing the CMOS pixel array without significantly increasing the overall size of the host circuit board ... requires 100 times less power ... enabled the development of a ‘camera on a chip’”), 12:54-65 (“Although the active pixel array disclosed in U.S. Pat. No. 5,471,515 is mentioned herein, it will be understood that the hybrid CCD/CMOS described above, or any other solid state imaging device may be used wherein timing and control circuits can be placed either on the same planar structure with the pixel array, or may be separated and placed remotely. Furthermore, it will be clearly understood that the invention claimed herein is not specifically limited to an image sensor as disclosed in the U.S. Pat. No. 5,471,515, but encompasses any image sensor which may be configured for use in conjunction

with the other processing circuitry which makes up the imaging device of this invention.”).

88. As shown in Figure 6 in red, the timing controller 20 is coupled to the CMOS pixel array for timing and control of the pixels.



Ackland, Fig. 6 (annotated).

89. Ackland further describes how the active pixel imaging system produces an output signal. Ackland describes how the active pixel imaging system formed of rows and columns of active pixels produces an output signal provided in serial fashion to the common output line 19 along which the output signals are transmitted from the active pixel imaging system (the image sensor) on the first end

of the line to the processing circuitry on the second end. *See, e.g., Ackland, 8:45-52* (“The output voltage signals generated by the activated row 35 are simultaneously provided to the corresponding amplifiers 18 via the column output line 65. Output signals from the amplifiers 18 are provided to the common output line 19 in serial fashion based on timing control signals from the timing control 20. The output signals are routed to suitable processing circuitry, not shown.”), 7:59-8:9, Fig. 6.

90. As the '052 patent acknowledges, CMOS image sensors and readout circuitry for operating such sensors, as disclosed in Ackland, were well-known in the art. '052 patent, 2:9-15 (“This [known] CMOS imager can incorporate a number of other different electronic controls that are usually found on multiple circuit boards of much larger size. For example, timing circuits...”), 2:25-36. Further, the '052 patent admits that it was known that CMOS active pixel sensor imagers result in lower noise than CCD or other solid state imagers, can be mass produced on standard semiconductor productions lines, can incorporate a number of other different electronic controls that are usually found on multiple circuit boards of much larger size, and require less power than CCD imagers. '052 patent, 1:66-2:19; *see also* NASA (Ex. 1060, publicly available 03/06/1995 through Business Week, and I understand is prior art to the '052 patent) (describing benefits of active pixel image sensor over CCD sensors, including lower power consumption, smaller size, no need for a custom manufacturing process, and can tolerate lower material quality).

91. A person of ordinary skill in the art would have been motivated to apply Ackland's known teachings described above in implementing Wakabayashi's "imager apparatus." As the '052 patent acknowledges, CMOS image sensors and readout circuitry for operating such sensors, as disclosed in Ackland, were well known in the art. *See, e.g., '052 patent, 2:9-15* ("*This CMOS imager can incorporate a number of other different electronic controls* that are usually found on multiple circuit boards of much larger size. *For example, timing circuits*, and special functions such as zoom and anti jitter controls can be placed *on the same circuit board containing the CMOS pixel array* without significantly increasing the overall size of the host circuit board."), 2:25-34.

92. Both Wakabayashi and Ackland are in the same field of art and are analogous art to the '052 patent—all are in the same field related to solid state image sensors for use in cameras. *See, e.g., '052 patent, Abstract, 1:32-36* ("This invention relates to *solid state image sensors* incorporated within wireless endoscopes, and more particularly, to solid state image sensors which are incorporated within wireless endoscopes that wirelessly transmit *video images* for viewing."), 7:65-8:1 ("In accordance with one arrangement of the imaging device as shown in FIG. 1a, an endoscope 10 in the first embodiment is provided which *incorporates a reduced area imaging device 11*, shown in FIG. 1b."); Wakabayashi, Abstract, 9:10-14 ("... A camera head 100, which includes a light receiving lens, a *solid-state imager device*,

a circuit for driving the solid-state imager device, and so on, generates an opto-electrically converted signal 101 which is inputted to a camera circuit 102.”); Ackland, 1:35-38 (“Like charge coupled devices and MOS diode arrays, each pixel in a CMOS active pixel array includes a sensing element capable of converting optical images into electronic signals.”), 3:27-29, 7:59-65 (“...active pixel imaging system, such as the exemplary imaging system 1 shown in FIG. 6. Such an imaging system may be used as a solid-state camera.”).

93. In addition, Wakabayashi and Ackland are also reasonably pertinent to the alleged problem(s) identified in the '052 patent of arranging the circuitry of an image sensor, including to minimize the size of the device and for the device to be “low cost.” See, e.g., '052 patent, 3:31-39 (“It is one general object of this invention to provide a wireless endoscope incorporating reduced area imaging devices which take advantage of “camera on a chip” technology, but rearrange the circuitry in a stacked relationship so that there is a minimum profile presented when used within a surgical instrument or other investigative device. It is another object of this invention to provide a wireless endoscope utilizing low cost imaging devices which may be ‘disposable.’”); Wakabayashi, Abstract (“A video camera unit made compact to realize a reduction in weight of a video camera rotating mechanism”), 2:37-39, 3:40-44 (“The video camera unit is made small”), 14:6-10; Ackland, 2:10-15 (“It would be desirable to form an active pixel using a process wherein only

one polysilicon deposition is required. This simple process would result in lower per chip fabrication cost. Furthermore, it would be desirable to operate such a pixel in a manner that minimizes hardware requirements while maintaining optimal pixel performance.”).

94. Moreover, '052 patent's stated goals of producing a “very small” or “low cost” imaging device were well known objectives that a person of ordinary skill in the art designing imaging devices would have been aware of. *See, e.g., '052 patent, 3:37-55; Wakabayashi, Abstract; Ackland, 2:10-15.* For example, Wakabayashi is explicitly directed to a device where the video camera unit is “reduced in size and weight.” Wakabayashi, Abstract.

95. A person of ordinary skill in the art would have been further motivated to apply Ackland's known teachings in implementing Wakabayashi imager apparatus because, relative to other image sensor options, Ackland's teachings of an array of single-polysilicon active pixels requires no active drive signal for charge transfer. *See, e.g., Ackland, 2:34-45.* This advantageously allows the image sensor to operate with less power because it does not require “separate bias supply or clocking circuitry” which would require driving additional circuitry and result in greater drain on battery power. *See, e.g., Ackland, 2:34-41, Abstract (“By virtue of the structure of the single-polysilicon active pixel, this mode of operation results in the same timing as if the transfer transistor were clocked, but neither a clock nor the*

associated driving circuitry are required.”). In battery powered devices, less power consuming circuitry is desirable. In addition, through the use of single-polysilicon active pixels, a simpler fabrication process is possible, which lowers costs. *See, e.g., Ackland, 2:10-15 (“It would be desirable to form an active pixel using a process wherein only one polysilicon deposition is required. This simple process would result in lower per chip fabrication cost. Furthermore, it would be desirable to operate such a pixel in a manner that minimizes hardware requirements while maintaining optimal pixel performance.”)*. Such a design also reduces image lag that “is observed in a double-polysilicon active pixel.” *See, e.g., Ackland, 2:34-45.*

96. In addition, a person of ordinary skill in the art would have been motivated to apply Ackland’s known teachings of an array of CMOS active pixels each including an amplifier in implementing Wakabayashi’s “imager apparatus” to advantageously amplify the “video signal,” for example, in order to “overcome the relatively large load offered by the common output conductor 65.” Ackland, 5:7-10.

97. In light of the above, a person of ordinary skill in the art would have found it routine, straightforward and advantageous to apply Ackland’s known teachings of an array of CMOS active pixels in an image sensor outputting a pre-video signal in implementing Wakabayashi’s imager apparatus, and would have known that such a combination (yielding the claimed limitations) would predictably work and provide the expected functionality. In addition, as I discussed in Section

VIII.A.1, a person of ordinary skill in the art would have found it routine, straightforward and advantageous to locate the circuitry to convert the pre-video signal, as taught by Ackland, to a post-video signal on Wakabayashi's circuit board 39, and would have known that such a design choice (yielding the claimed limitations) would predictably work and provide the expected functionality.

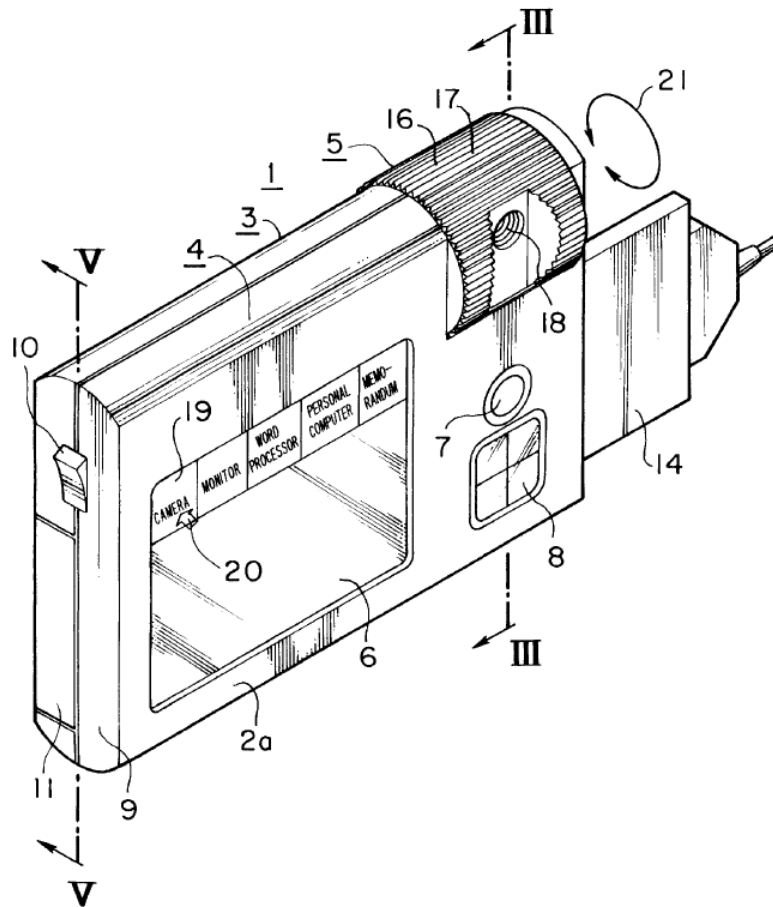
4. Invalidity of Claim 1 Over Wakabayashi in view of Ackland (Ground 1)

a. Element [1.pre]

98. Element [1.pre] recites "An imaging device." To the extent the preamble is limiting, Wakabayashi discloses an imaging device (*e.g.*, "a portable imager apparatus").

99. For example, Wakabayashi discloses that "[t]he present invention relates to a portable imager apparatus which includes a video camera as an imager unit, a direct-view type flat display as an electronic view finder or display...." Wakabayashi, 1:6-9. Wakabayashi further discloses that "[a] video camera unit made compact to realize a reduction in weight of a video camera rotating mechanism. An image arrangement convertor circuit is provided between the video camera unit and a liquid crystal display serving as a display unit or a recording unit." Wakabayashi, Abstract.

FIG. 1



Wakabayashi, Fig. 1.

b. Element [1.a]

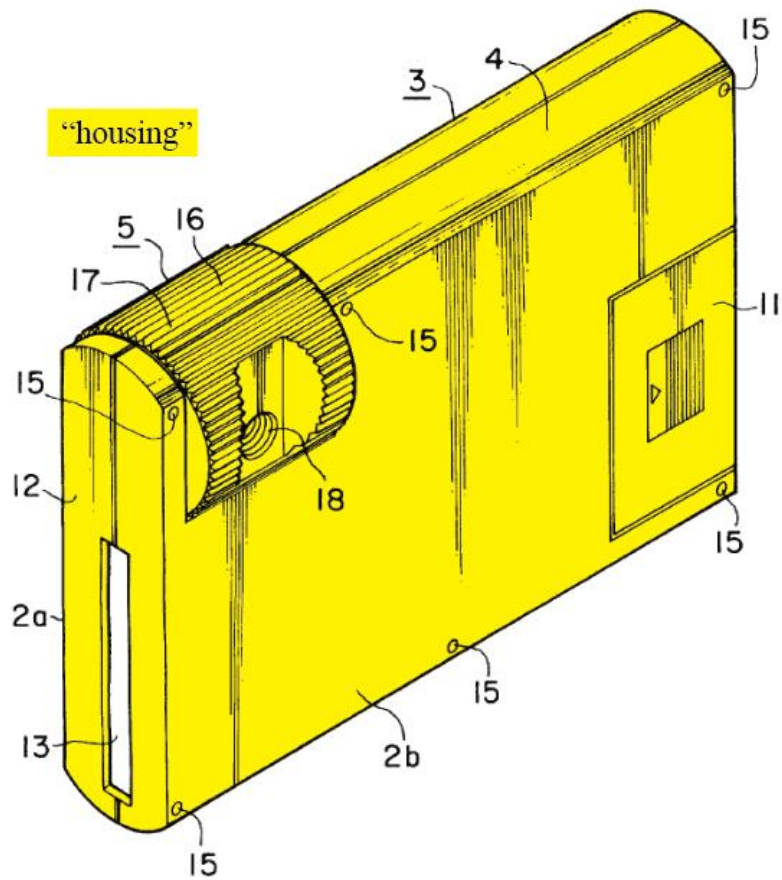
100. **Element [1.a] recites “a housing.”** Wakabayashi discloses element [1.a]. Wakabayashi discloses a housing (e.g., “imager apparatus 1” enclosure formed by “front panel 2a,” “rear panel 2b,” “camera case 16,” and “battery-cover 11”).

101. Wakabayashi discloses a housing of the imager apparatus formed by the “housing 3” (including the “front panel 2a” and “rear panel 2b”), “camera case

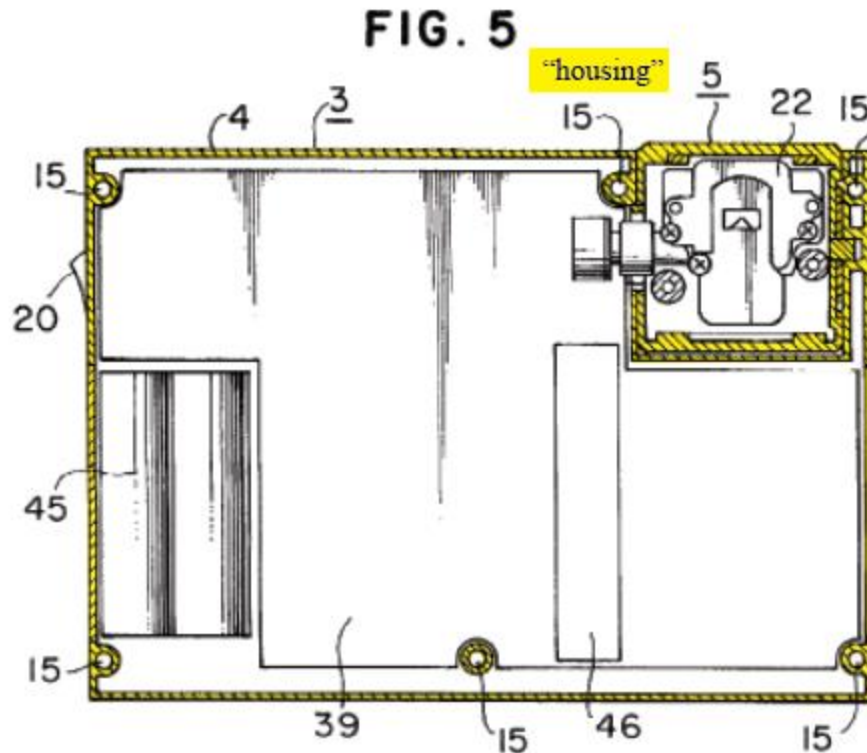
16,” and “battery-cover 11.” These components collectively form the housing, as depicted in Figs. 1, 2 and 5.

102. For example, Wakabayashi discloses “[t]he imager apparatus 1 has a video camera unit 5 rotatably pivoted on a right end portion of an upper edge 4, a liquid crystal display 6 accommodated in the housing 3, a selection button 7 and a cursor key 8 arranged on the front panel 2a, a power supply switch 10 and a battery-cover 11 arranged on a left side surface 9 of the housing 3, and a card slot 13 formed in a right side surface 12 of the housing 3 for inserting a PCMCIA card 14. The rear panel 2b of the housing 3 are formed with six screw holes 15 for assembling the housing 3. The video camera unit 5 has a camera case 16 formed with anti-slip knurl 17 on the surface thereof.” Wakabayashi, 4:44-54. Wakabayashi further explains “[t]he camera case 16 has a cylinder 47 at one end and a shaft 48 on the other end,” “cylinder 47 is fitted into a hole 49 formed through the housing 3, while the shaft 48 is rotatably fitted into a recess 50 extending into a side wall of the housing 3,” and “[a] flexible board 51 passes through the cylinder 47.” Wakabayashi, 6:29-33.

FIG. 2



Wakabayashi, Fig. 2 (annotated).



Wakabayashi, Fig. 5 (annotated), *see also* Fig. 1 (perspective view of imager apparatus), Fig. 3 (illustrating side-view of enclosure), Fig. 6 (illustrating magnified view of the imager apparatus).

c. Element [1.b]

103. Element [1.b] recites “an image sensor mounted in said housing, said image sensor including a first circuit board having a length and a width thereto, wherein said length and width of said first circuit board define a first plane, said first circuit board including an array of CMOS pixels thereon.”

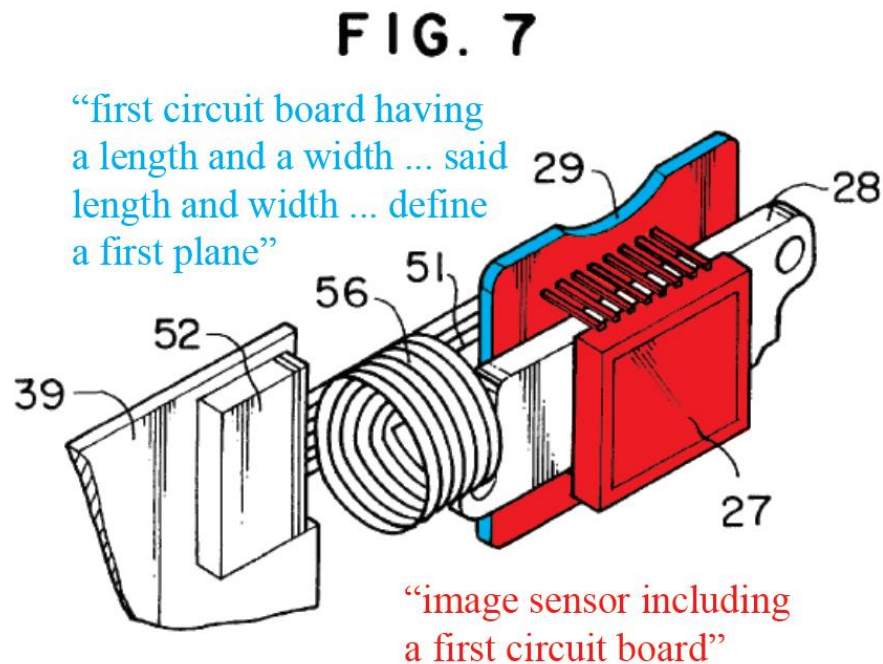
Wakabayashi in view of Ackland renders obvious element [1.b]. Wakabayashi discloses an image sensor (*e.g.*, “imager device 27 [] electrically connected to the []

board 29 by soldering”) mounted in said housing (e.g., “circuit board 29 is fixed on the mounting plate 28 ... fixed to the camera case 16”), said image sensor including a first circuit board having a length and a width thereto, wherein said length and width of said first circuit board define a first plane (e.g., plane defined by length and width of “circuit board 29” as shown in Figure 7), said first circuit board including an image sensor chip thereon (e.g., “imager device 27” is “solder[ed]” onto “the camera circuit board 29”). Ackland discloses an image sensor (e.g., “active pixel imaging system”) including an array of CMOS pixels thereon (e.g., “CMOS ... pixel array”).

104. Wakabayashi discloses an image sensor including a “solid-state” “imager device 27” (an image sensor chip) mounted on a “circuit board 29” (a first circuit board having a length and width that define a first plane) as depicted in Figure 7. *See, e.g.,* Wakabayashi, 5:56-59, 6:47-49, 9:10-14, Fig. 7. “Imager device 27” and “circuit board 29” are soldered onto “mounting plate 28,” which is “fixed” “to the camera case 16”—thus, the image sensor is mounted in the housing as depicted in Figures 3 and 7. *See, e.g.,* Wakabayashi, 5:62-65, 6:47-49, Fig. 3, Fig. 7.

105. For example, Wakabayashi discloses “the video camera 22 includes a shutter 23, a lens case 24, a lens 25, a quartz filter 26, an imager device 27, a mounting plate 28, and a camera circuit board 29. When the shutter 23 is opened, light penetrates through the imaging hole 18, and an image of a subject is focused

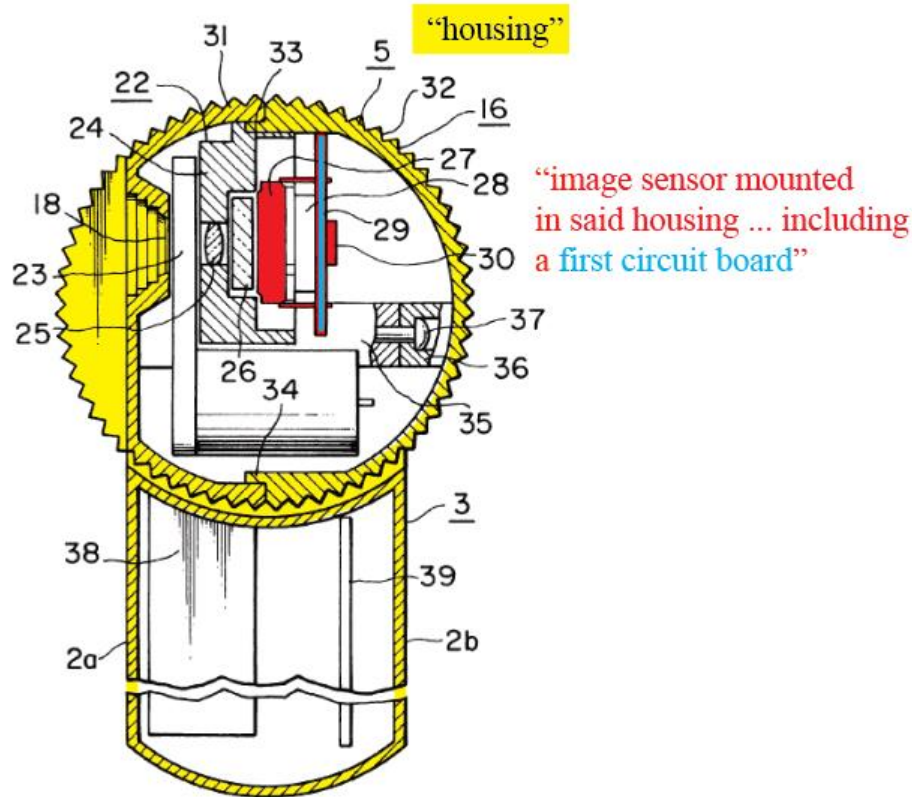
on the imager device 27 by the lens 25.” Wakabayashi, 5:56-61. Wakabayashi also explains “[a] camera head 100, which includes a light receiving lens, a solid-state imager device, a circuit for driving the solid-state imager device, and so on, generates an opto-electrically converted signal 101 which is inputted to a camera circuit 102.” Wakabayashi, 9:10-14. “[T]he imager device 27 is electrically connected to the camera circuit board 29 by soldering with the mounting plate 28 interposed therebetween.” Wakabayashi, 6:47-49.



Wakabayashi, Fig. 7 (annotated).

106. Wakabayashi explains “[t]he camera circuit board 29 is fixed on the mounting plate 28 with screws 30, and the mounting plate 28 in turn is fixed to the camera case 16 with screws (see FIG. 6).” Wakabayashi, 5:62-65.

FIG. 3



Wakabayashi, Fig. 3 (annotated).

107. While Wakabayashi discloses that the image sensor uses a “solid-state imager device” and a “circuit for driving the solid-state imager device” to “generate[] an opto-electrically converted signal” (Wakabayashi, 9:11-15 (“A camera head 100, which includes a light receiving lens, a solid-state imager device, a circuit for driving the solid-state imager device, and so on, generates an opto-electrically converted signal 101 which is inputted to a camera circuit 102.”)), Wakabayashi does not expressly state that its “imager device 27 [] electrically connected to the camera circuit board 29” includes an array of CMOS pixels. Ackland provides additional

implementation detail for an “active pixel imaging system,” which includes a “CMOS ... pixel array” for receiving images thereon. *See, e.g.*, Ackland, 1:35-38, 7:62-63.

108. Ackland’s teaches a “CMOS active pixel characterized by a single layer of polysilicon for forming the photo gate and the transfer gate (‘single-polysilicon active pixel’), a method for operating the pixel, and pixel arrays based on such a pixel.” Ackland, 2:19-23. Ackland’s “CMOS active pixel 36 ... may be comprised of the same elements that are used in a double polysilicon active pixel for providing read-out, reset and buffering functions.” Ackland, 7:44-47.

109. For example, Ackland discloses an “active pixel imaging system, such as the exemplary imaging system 1 shown in FIG. 6,” which “may be used as a solid-state camera.” Ackland, 7:59-65. Ackland’s active pixel imaging system, as shown in Figure 6 below, for example, “includes an array 5 of active pixels, a row decoder 10 and a plurality of output amplifiers 18.” Ackland, 7:59-8:9.

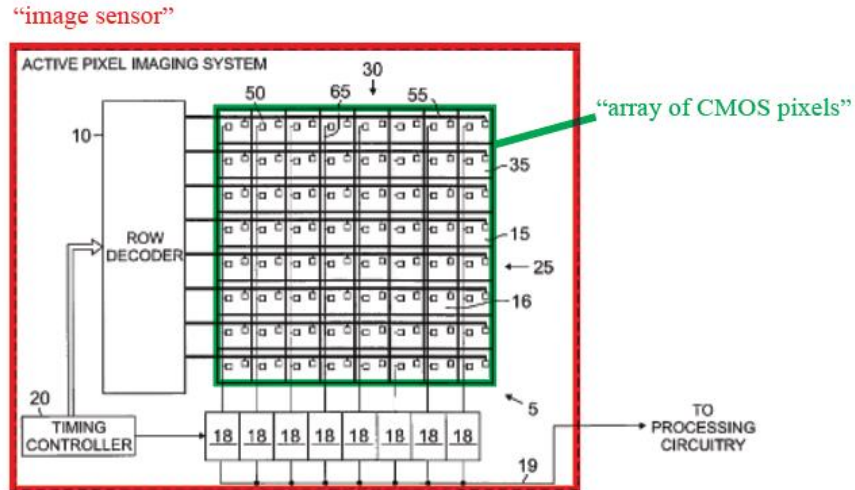


FIG. 6

Ackland, Fig. 6 (annotated).

110. As discussed in Section VIII.A.3, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to apply Ackland’s known teachings of an array of CMOS active pixels in an image sensor in implementing Wakabayashi’s imager apparatus and would have recognized this combination (yielding the claimed limitation) would work as expected.

d. Element [1.c]

111. **Element [1.c] recites “wherein a plurality of CMOS pixels within said array of CMOS pixels each include an amplifier.”** Ackland discloses element [1.c]. Ackland discloses a plurality of CMOS pixels within said array of CMOS pixels each include an amplifier (*e.g.*, “active pixel ... includes ... an amplifier formed by a voltage follower-transistor 125”).

112. While Wakabayashi does not expressly disclose that its pixels each include an amplifier, Ackland provides additional implementation detail for an “active pixel imaging system” wherein each “CMOS active pixel 36” of the “array 5 of active pixels” “further includes ... an amplifier formed by a voltage follower-transistor 125.” Ackland, 3:20-25. Additionally, Figure 3 of Ackland is a schematic of a “single-polysilicon active pixel” that shows an exemplary amplifier used with each pixel. Ackland, 2:66-67.

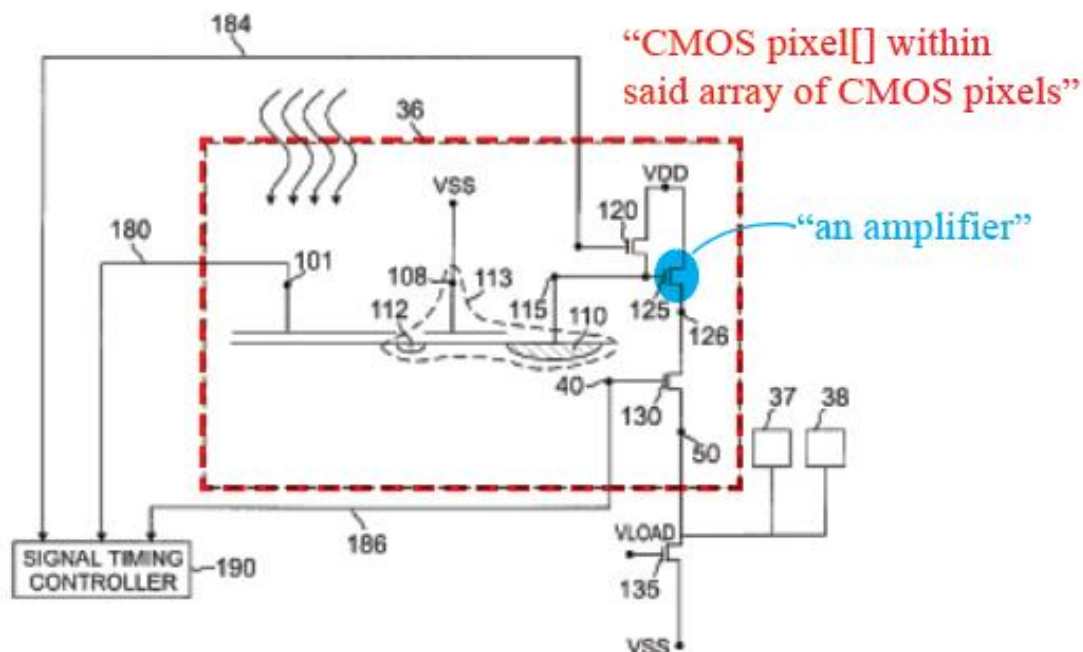


FIG. 3

See Ackland, Fig. 3 (annotated); *see also* Ackland, 7:44-47 (“The single-polysilicon CMOS active pixel 36 of the present invention may be comprised of the same elements that are used in a double polysilicon active pixel for providing read-out, reset and buffering functions.”), 7:59-8:8, 8:16-17.

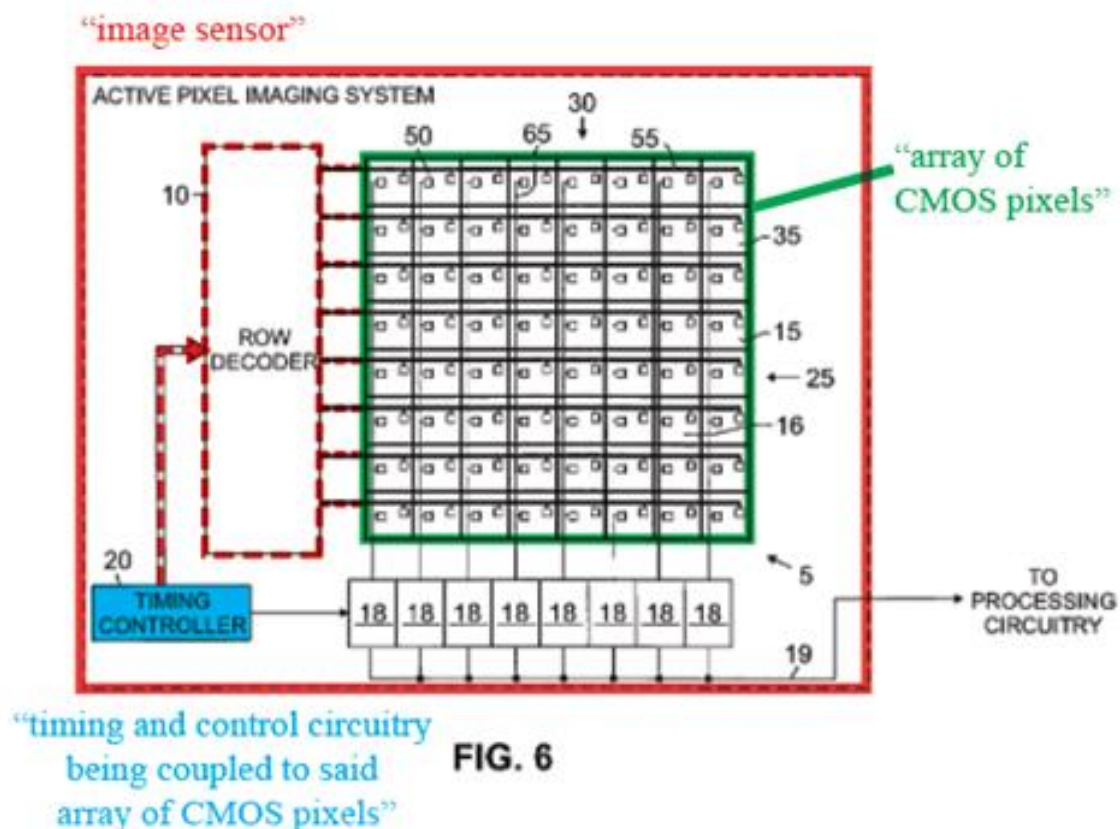
113. As discussed in Section VIII.A.3, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to apply Ackland's known teachings of an array of CMOS active pixels each including an amplifier in implementing Wakabayashi's "imager apparatus" to advantageously amplify the "video signal" in order to, for example, "overcome the relatively large load offered by the common output conductor 65." Ackland, 5:7-10. A person of ordinary skill in the art would have recognized this combination (yielding the claimed limitation) would work as expected.

e. Element [1.d]

114. **Element [1.d] recites "said first circuit board further including timing and control circuitry thereon, said timing and control circuitry being coupled to said array of CMOS pixels."** Wakabayashi in view of Ackland renders obvious element [1.d]. Wakabayashi discloses said first circuit board (*e.g.*, "circuit board 29"). Ackland discloses said image sensor (*e.g.*, "active pixel imaging system") including timing and control circuitry (*e.g.*, "timing controller 20"), said timing and control circuitry being coupled to said array of CMOS pixels (*e.g.*, "timing controller 20" coupled to the "CMOS ... pixel array" through "row decoder 10" in the "exemplary active pixel image sensor" shown in Figure 6).

115. As discussed in relation to element [1.b], Wakabayashi discloses a first circuit board 29.

116. While Wakabayashi does not detail the timing and control circuitry of its “imager device 27 [] electrically connected to the camera circuit board 29,” Ackland describes circuitry including a “timing controller 20 provides timing signals” that control the imaging system “to achieve a desired frame rate.” Ackland, 8:24-35. As shown in Figure 6, the timing controller 20 is coupled to the CMOS pixel array for timing and control of the pixels.



Ackland, Fig. 6 (annotated), 3:6-7 (“FIG. 6 is a schematic of an exemplary active pixel image sensor according to the present invention.”), 7:59-8:9 (“The imaging

system 1 includes an array 5 of active pixels, a row decoder 10 and a plurality of output amplifiers 18.”).

117. Specifically, Ackland discloses that the “timing controller 20 provides timing signals to the row decoder 10” and “[i]n response, the decoder 10 sequentially activates each row 25 of active pixels 35 via the control lines 55 to detect light intensity and to generate corresponding output voltage signals during each frame interval.” Ackland, 8:24-30. Ackland explains that “[i]n the context of an array of pixels, the term ‘frame’ refers to a single complete cycle of activating and sensing the output from each pixel 35 in the array a single time over a predetermined frame time period.” Ackland, 8:30-33. Ackland’s “timing controller 20” controls the timing of the imaging system “to achieve a desired frame rate, such as 30 frames per second.” Ackland, 8:24-35.

118. Ackland teaches that the signals output from the amplifiers 18, shown in Figure 6, “are provided to the common output line 19 in serial fashion based on timing control signals from the timing control 20. The output signals are routed to suitable processing circuitry.” Ackland, 8:47-52. *See also* Ackland, 3:39-54, 4:45-49.

119. As discussed above in Section VIII.A.3, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to apply Ackland’s known teachings of an image sensor including timing and control

circuitry in implementing Wakabayashi's imager apparatus, and would have recognized this combination (yielding the claimed limitation) would work as expected.

f. Element [1.e]

120. **Element [1.e] recites “said image sensor producing a pre-video signal.”** Ackland discloses element [1.e]. Ackland discloses said image sensor producing a pre-video signal (*e.g.*, “output signal” produced by the “active pixel imaging system”).

121. Ackland describes how the active pixel imaging system produces an output signal, which is a pre-video signal. For example, Ackland teaches that “[t]he output voltage signals generated by the activated row 35 are simultaneously provided to the corresponding amplifiers 18 via the column output line 65” and the “[o]utput signals from the amplifiers are provided to the common output line 19 in serial fashion.” Ackland, 8:45-52, 7:59-8:9. These output signals are “routed to suitable processing circuitry.” Ackland, 8:45-52.

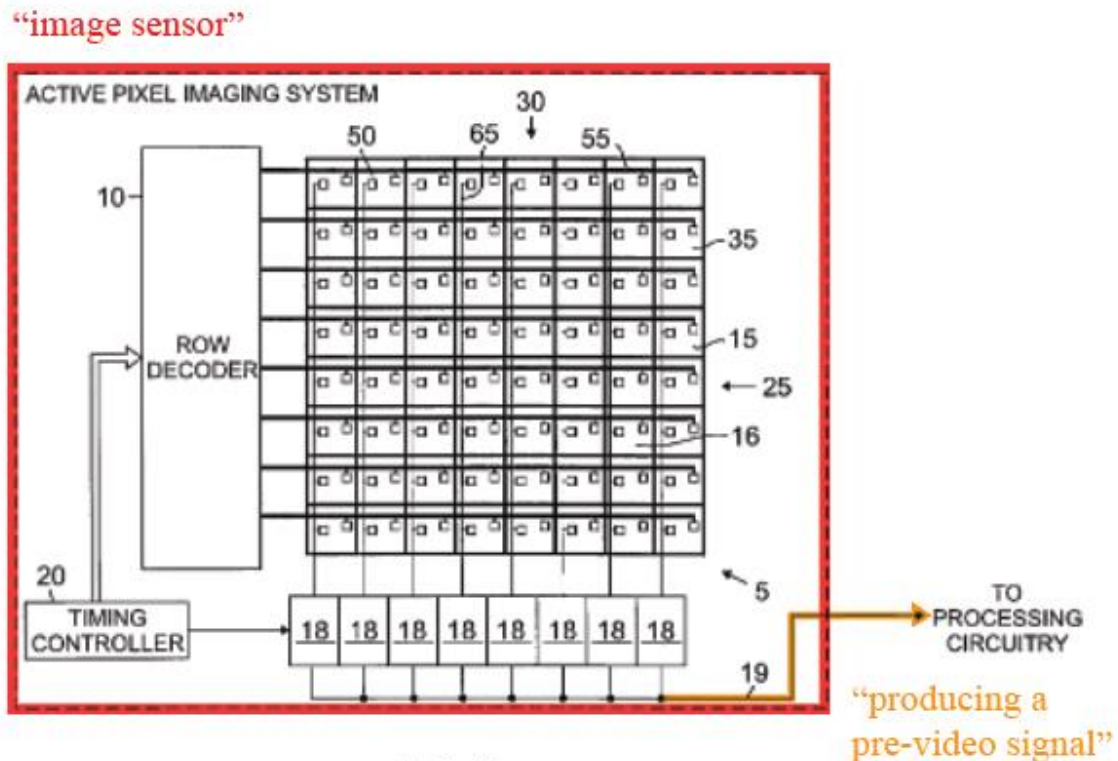


FIG. 6

Ackland, Fig. 6 (annotated).

122. As discussed in Section VIII.A.3, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to apply Ackland’s known teachings of an image sensor producing a pre-video signal in implementing Wakabayashi’s imager apparatus, and would have recognized this combination (yielding the claimed limitation) would work as expected.

g. Element [1.f]

123. **Element [1.f] recites “a second circuit board mounted in said housing, said second circuit board being electrically coupled to said first circuit board, said second circuit board having a length and a width thereto, wherein**

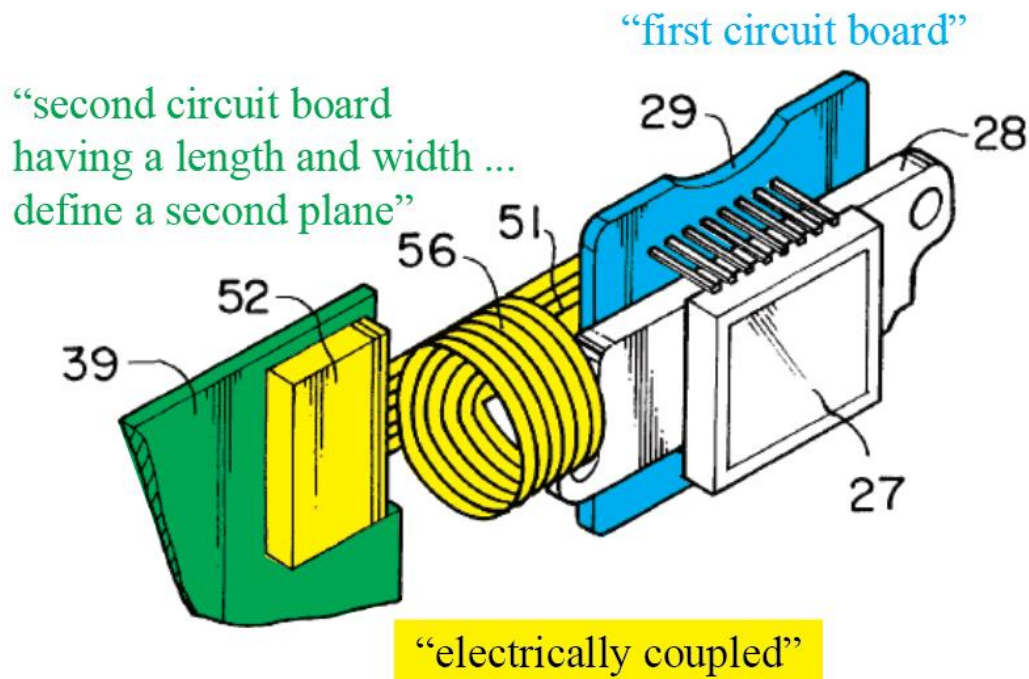
said length and width of said second circuit board define a second plane, said second circuit board including circuitry thereon to convert said pre-video signal to a post-video signal, said second circuit board being offset from said first circuit board, said second plane of said second circuit board being substantially parallel to said first plane of said first circuit board.” Wakabayashi renders obvious element [1.f]. Wakabayashi discloses a second circuit board mounted in said housing (*e.g.*, “circuit board 39 is disposed in the housing”), said second circuit board being electrically coupled to said first circuit board (*e.g.*, “flexible board 51 connects ... circuit board 29 to the ... circuit board 39” to “process[]” the “signal” from the “video camera unit”), said second circuit board having a length and a width thereto, wherein said length and width of said second circuit board define a second plane (*e.g.*, plane defined by length and width of “circuit board 39” as shown in Fig. 7), said second circuit board including circuitry thereon to convert said pre-video signal to a post-video signal (*e.g.*, “circuit board 39 includes a signal processing circuit ..., a driver circuit ..., a system circuit, a power supply circuit, and so on” and it would have been obvious to include “camera signal processing circuit ... [that] generates a video signal 103 in a television signal format from the opto-electrically converted signal 101” on circuit board 39), said second circuit board being offset from said first circuit board (*e.g.*, “circuit board 39” is vertically and laterally offset from “circuit board 29” as illustrated in Figs. 3 and 7, respectively), said second

plane of said second circuit board being substantially parallel to said first plane of said first circuit board (*e.g.*, plane defined by length and width of “circuit board 39” parallel with plane defined by length and width of “circuit board 29” as shown in Figs. 3 and 7).

124. Wakabayashi discloses that “circuit board 39” is “disposed in the housing 3.” Wakabayashi, 6:5-10, 6:20-27.

125. Wakabayashi also discloses that “imager device 27 [] electrically connected to the camera circuit board 29” is connected to a “circuit board 39” of the imager apparatus, as shown in Figure 7. Wakabayashi, 6:47-49. Wakabayashi explains that a “flexible circuit board” that “passes through the cylinder 47” is soldered at one end to the “circuit board 29” and “connects ... to the connector 52 on the circuit board 39,” which is mounted in the “housing” of the imager apparatus, as illustrated in Figure 3. *See, e.g.*, Wakabayashi, 6:29-38 (“The flexible board 51 has one end connected to the camera circuit board 29 by soldering and the other end connected to a connector 52 on the circuit board 39.”), 6:49-51, Fig. 3.

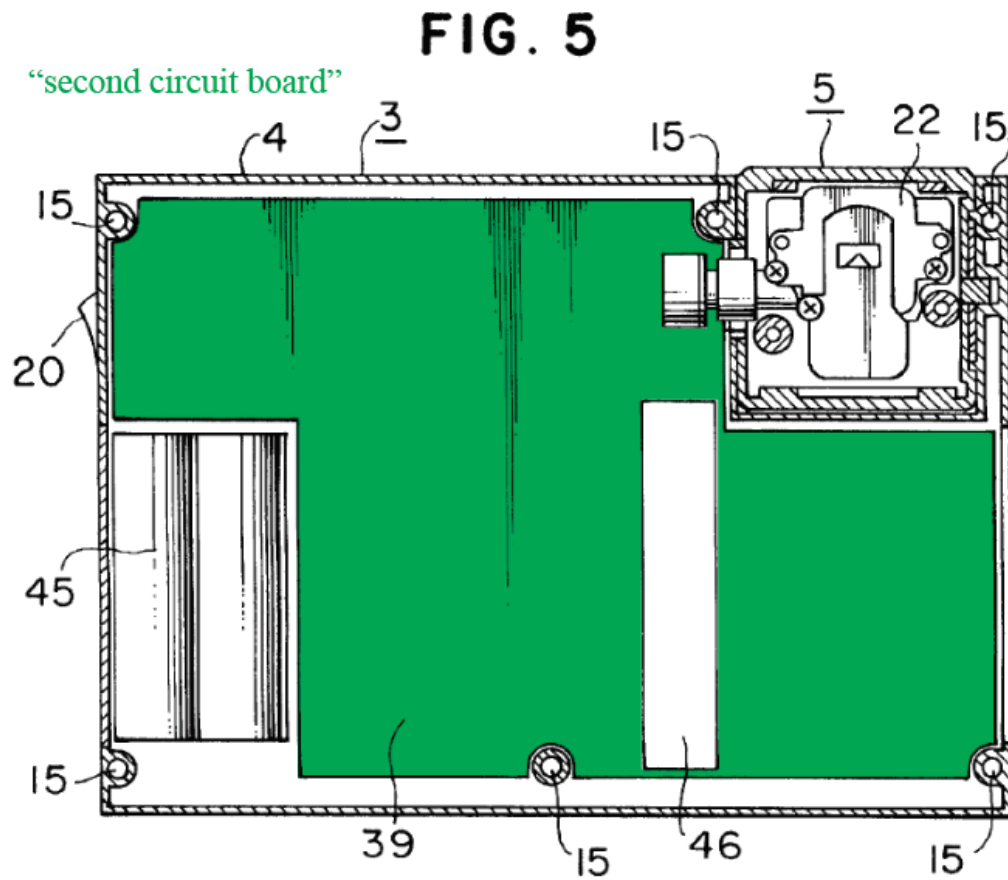
FIG. 7



Wakabayashi, Fig. 7 (annotated).

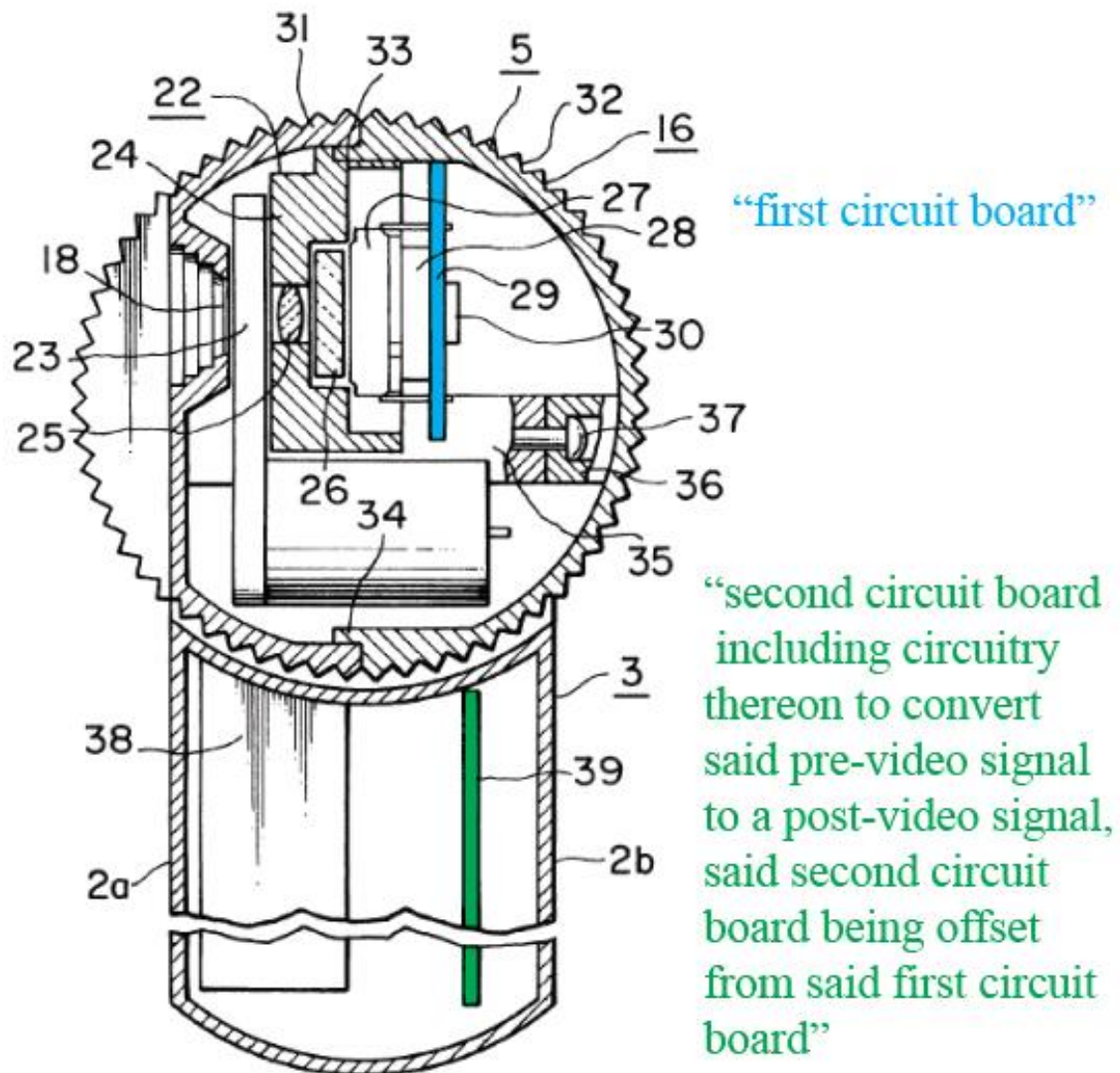
126. Wakabayashi also discloses that “circuit board 39,” as illustrated in Figure 5, has a length and a width that define a second plane. Figures 3 and 7, further illustrate that this plane is substantially parallel to the first plane defined by the length and width of “circuit board 29,” and that the “circuit board 39” is offset from “circuit board 29.” Specifically, Figure 7 illustrates the perspective view of the components of Wakabayashi’s imager apparatus and Figure 3 illustrates its cross section. From these two figures Wakabayashi shows that the length and width of the “circuit board 39” defines a plane that is parallel to the plane defined by the length and width of “circuit board 29.” Additionally, the two figures also show that

the “circuit board 39” is not stacked behind “circuit board 29,” but rather, “circuit board 39” is arranged in an offset position from “circuit board 29.”



Wakabayashi, Fig. 5 (annotated).

FIG. 3



Wakabayashi, Fig. 3 (annotated).

127. In addition, Wakabayashi explains that “circuit board 39 includes a signal processing circuit for the video camera unit 5, a driver circuit for the liquid crystal panel 38, a system circuit, a power supply circuit, and so on.” Wakabayashi, 6:5-10. Further, Wakabayashi explains “[t]he camera circuit 102, which includes a

camera signal processing circuit, a synchronization signal generator circuit, and so on, generates a video signal 103 in a television signal format from the opto-electrically converted signal 101"). Wakabayashi, 9:15-19.

128. As discussed in Section VIII.A, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to locate the circuitry that “generates a video signal 103” by converting the pre-video signal to a post-video signal on Wakabayashi’s “circuit board 39” and couple it to the power supply circuit, and would have recognized this combination (yielding the claimed limitation) would work as expected.

h. Element [1.g]

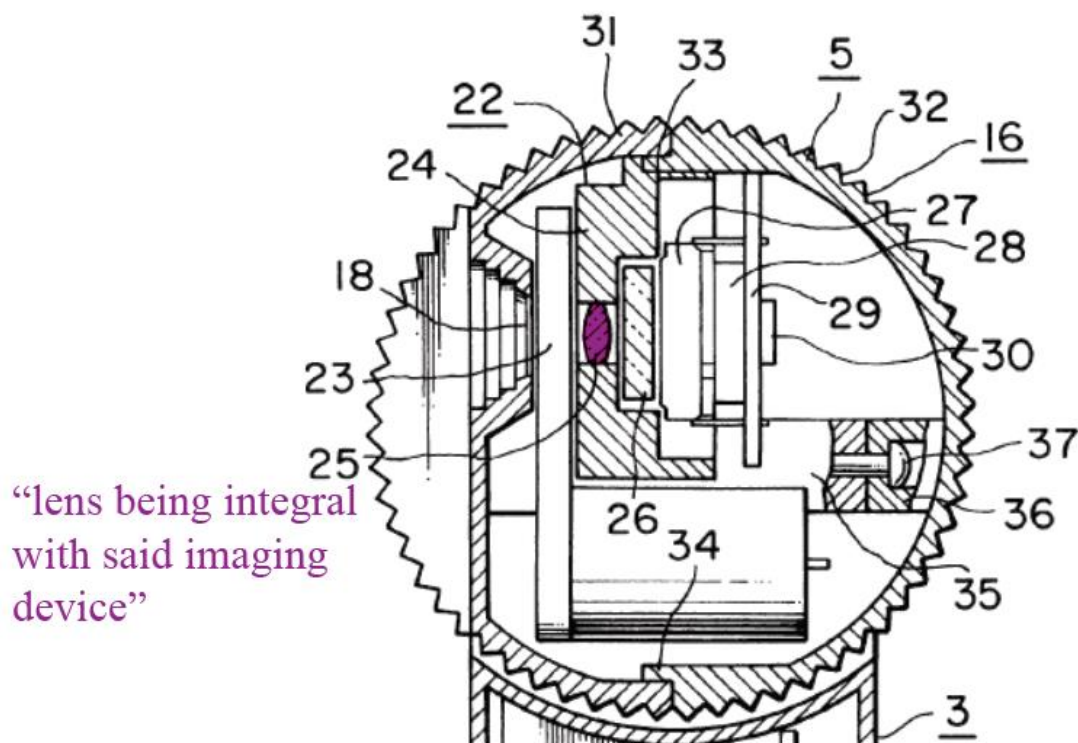
129. **Element [1.g] recites “a lens mounted in said housing, said lens being integral with said imaging device, said lens focusing images on said array of CMOS pixels of said image sensor.”** Wakabayashi in view of Ackland renders obvious element [1.g]. Wakabayashi discloses a lens mounted in said housing, said lens being integral with said imaging device (*e.g.*, “lens 25” in “lens case 24” “secured to” “the mounting plate 28 ... fixed to the camera case 16” of the “imager apparatus”), said lens focusing images on the image sensor chip (*e.g.*, “image ... is focused on the imager device 27 by the lens 25”). As discussed above, Ackland discloses an array of CMOS pixels.

130. Wakabayashi discloses a “lens 25” in a “lens case 24” which is “secured” to the “mounting plate 28” “with a screw.” Wakabayashi, 5:56-61, 6:11-19. Wakabayashi’s “mounting plate 28 ... is fixed to the camera case 16.” Wakabayashi, 5:62-65. Thus, lens 25 is integral with Wakabayashi’s imager apparatus. Wakabayashi further explains that “lens 25” is used to “focus[]” an “image ... on the imager device 27.” Wakabayashi, 5:56-61.

131. For example, Wakabayashi explains “[a] video camera unit is composed of a lens and an imager device.” Wakabayashi, 2:51-54. Wakabayashi also explains that “[w]hen the shutter 23 is opened, light penetrates through the imaging hole 18, and an image of a subject is focused on the imager device 27 by the lens 25.” Wakabayashi, 5:56-61.

132. Wakabayashi explains that, as shown in Figure 4, “[t]he video camera 22 includes the shutter 23, the lens case 24, the mounting plate 28, and the camera circuit board 29. ... The mounting plate 28 is also secured to the lens case 24 with a screw 44.” Wakabayashi, 6:11-19. Further, “[t]he camera circuit board 29 is fixed on the mounting plate 28 with screws 30, and the mounting plate 28 in turn is fixed to the camera case 16 with screws (see FIG. 6).” Wakabayashi, 5:62-65.

FIG. 3



Wakabayashi, Fig. 3 (annotated).

133. As discussed in Section VIII.A.3, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to apply Ackland’s known teachings of an array of CMOS pixels in implementing Wakabayashi’s imager apparatus—such that the lens of Wakabayashi’s imager apparatus focuses images on said array of CMOS pixels, and would have recognized this combination (yielding the claimed limitation) would work as expected.

i. Element [1.h]

134. Element [1.h] recites “a video screen, said video screen being electrically coupled to said second circuit board, said video screen receiving said

post-video signal and displaying images from said post-video signal.”

Wakabayashi discloses element [1.h]. Wakabayashi discloses a video screen (*e.g.*, “liquid crystal panel 38” of “liquid crystal display 6”), said video screen being electrically coupled to said second circuit board (*e.g.*, “liquid crystal panel 38” is coupled to “circuit board 39” in order to display “video signal 103”), said video screen receiving said post-video signal and displaying images from said post-video signal (*e.g.*, “liquid crystal panel 38” displays “video signal 103”).

135. Wakabayashi discloses a “liquid crystal display 6” having a “liquid crystal panel 38” coupled to the “circuit board 39.” *See, e.g.*, Wakabayashi, 4:44-46, 6:6-10. The “circuit board 39” includes a “driver circuit for the liquid crystal panel 38.” Wakabayashi, 6:6-10. Wakabayashi explains that the “liquid crystal display serv[es] as a display unit” to display images from the “video signal 111 [] outputted” from “circuit board 39” and “allows a user to monitor an image.” Wakabayashi, 1:6-15, 10:15-17.

136. For example, Wakabayashi explains that “[*a liquid crystal panel 38 and a circuit board 39 are disposed in the housing 3. The circuit board 39 includes a signal processing circuit for the video camera unit 5, a driver circuit for the liquid crystal panel 38, a system circuit, a power supply circuit, and so on.*]” Wakabayashi, 6:6-10, Abstract. Wakabayashi further explains “[t]he present invention relates to a *portable imager apparatus* which *includes* a video camera as an imager unit, *a*

direct-view type flat display as an electronic view finder or display, and a semiconductor memory or video tape recorder (VTR) as a storage or recording unit, *wherein the* video camera, *the flat display*, and the recording unit *are integrated with each other*, and more particularly to an imager apparatus which *allows a user to monitor an image on a flat display* to adjust the angle of the video camera apparatus while imaging a subject.” Wakabayashi, 1:6-15, *see also* 4:44-46. Wakabayashi also explains that the “video signal 103” generated by the camera is “stored in RAM 105” and subsequently “read from the RAM 105.” *See, e.g.*, Wakabayashi, 9:14-38.

137. Wakabayashi discloses that “[t]o achieve the above objects, the present invention provides an imager apparatus which comprises a signal switch means in a housing for switching a signal when detecting that a video camera is directed to a monitor side, and *an image arrangement convertor circuit disposed between a camera circuit and image display means....*” Wakabayashi, 2:40-45.

138. Wakabayashi explains that, “when the cursor 20 is moved to ‘Camera’ within the items 19 and the selection button 7 is depressed to select a camera function, the imager apparatus 1 functions as a video camera. In response, *the video camera unit 5 is powered on to display an imaged subject on the liquid crystal display 6.*” Wakabayashi, 5:7-12. *See also* Wakabayashi, 10:2-17, Figs. 1-3, 10-11.

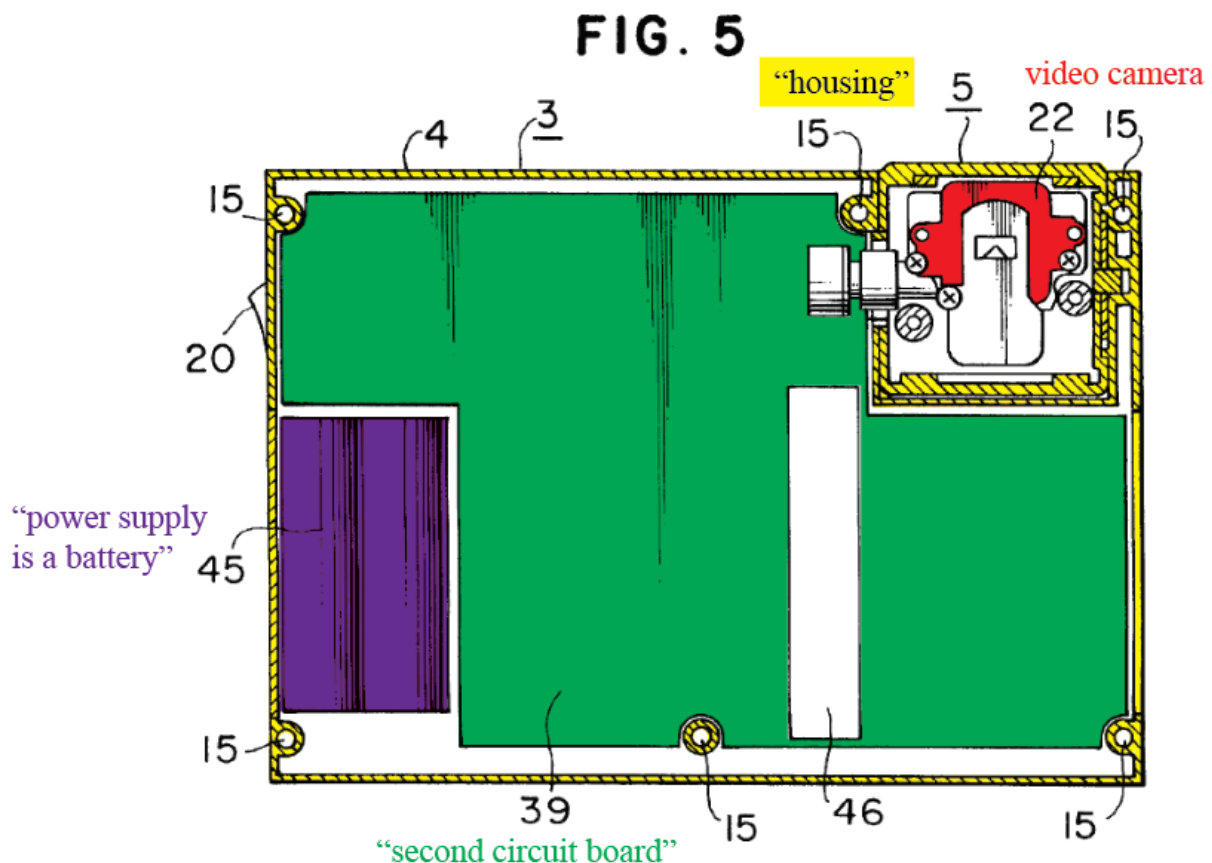
j. Element [1.i]

139. Element [1.i] recites “a power supply mounted in said housing, said power supply being electrically coupled to said first circuit board to provide power to said array of CMOS pixels and said timing and control circuitry, said power supply also being electrically coupled to said second circuit board to provide power thereto.” Wakabayashi in view of Ackland renders obvious element [1.i]. Wakabayashi discloses a power supply mounted in said housing (*e.g.*, “battery 45 is disposed in ... housing 3”), said power supply being electrically coupled to said first circuit board to provide power to the image sensor (*e.g.*, battery powers “imager device 27 [] electrically connected to [] circuit board 29”), said power supply also being electrically coupled to said second circuit board to provide power thereto (*e.g.*, battery coupled to “circuit board 39” to power “driver circuit” and “power supply circuit”). As discussed above, Ackland discloses an array of CMOS pixels.

140. Wakabayashi discloses the portable imager apparatus is powered by “battery 45 [] disposed in ... housing 3.” Wakabayashi, 6:21-27. Wakabayashi further explains that “[t]he circuit board 39 includes a signal processing circuit for the video camera unit 5, a driver circuit for the liquid crystal panel 38, a system circuit, a power supply circuit, and so on.” Wakabayashi, 6:7-10. In addition, “[t]he

imager apparatus 1 has ... a power supply switch 10 and a battery-cover 11 arranged on a left side surface 9 of the housing 3...” Wakabayashi, 4:44-49.

141. A person of ordinary skill in the art would have understood that, as a standalone device with a battery as the only disclosed source of power, the battery provides power to the “circuit board 29” to provide power to circuitry thereon, including the “imager device 27.” Additionally, this battery provides power to the second circuit 39 board, which includes a “power supply circuit.”



Wakabayashi, Fig. 5 (annotated).

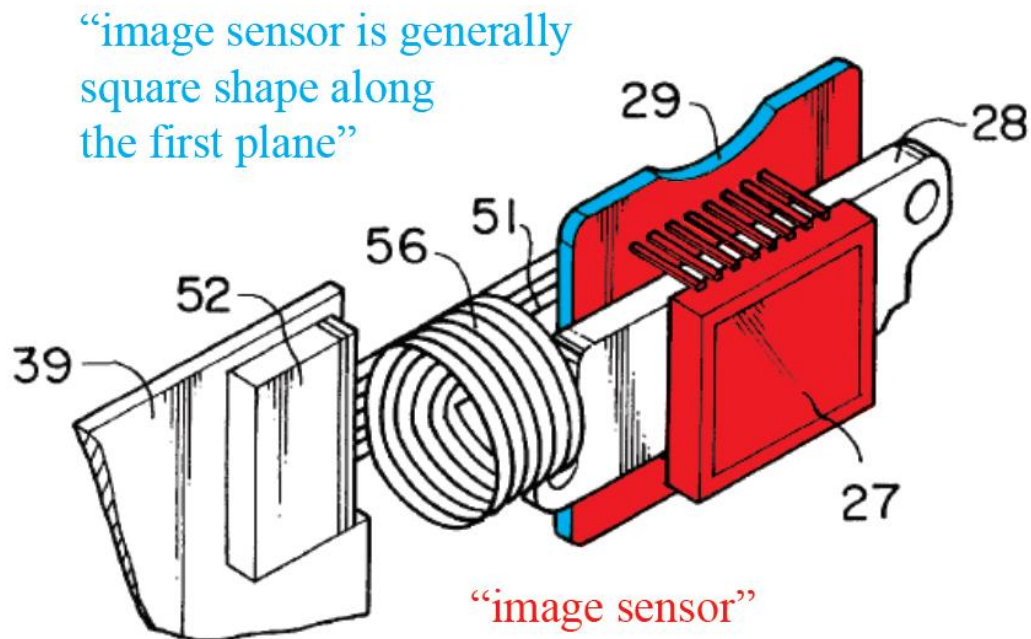
142. As discussed in Section VIII.A.3, it would have been obvious to apply Ackland's known teachings of an array of CMOS pixels in implementing Wakabayashi's imager apparatus—such that the power supply of Wakabayashi's imager apparatus provides power to said array of CMOS pixels and timing and control circuitry.

k. Element [1.j]

143. **Element [1.j] recites “wherein said image sensor has a generally square shape along said first plane.”** Wakabayashi discloses and/or renders obvious element [1.j]. Wakabayashi discloses the image sensor has a generally square shape along said first plane (*e.g.*, “imager device 27 [] electrically connected to the camera circuit board 29 by soldering” is generally square shaped along the first plane as illustrated in Figure 7).

144. Wakabayashi discloses the “circuit board 29” is generally square shape along the first plane, as shown in Figure 7, and not circular. *See* '052 patent, 9:3-6 (“Image sensor 40 is illustrated as being a planar and square shaped member. However, the image sensor may be modified to be in a planar and circular shape to better fit within the channel defined by inner tube 20”).

FIG. 7



Wakabayashi, Fig. 7 (annotated).

145. As discussed above in Section VIII.A.1, to the extent it is argued that additional disclosure is required, at minimum, it would have been an obvious implementation choice to use a square shaped circuit board along the first plane as it was well known in the art to use square shaped circuit boards.

I. Element [1.k]

146. Element [1.k] recites “wherein a largest dimension of said image sensor along said first plane is between 2 and 12 millimeters.” Wakabayashi renders obvious element [1.j]. Wakabayashi discloses the image sensor along said first plane (“circuit board 29”).

147. As discussed in relation to element [1.b], Wakabayashi discloses a first circuit board 29.

148. While Wakabayashi does not expressly disclose the dimensions of “circuit board 29,” as discussed in §VIII.A.1, it would have been an obvious implementation choice to use a circuit board having a largest dimension between 2 and 12 millimeters because boards of such size were well-known at the time for mounting to an image sensor. *See, e.g.,* Suzuki, 4:6-11 (“Further, in this embodiment of the invention, in the case where the solid-state image pickup chip of 1/3 inch (8.5 mm) is used, the outer diameter of the camera head is about 10 mm, and therefore is smaller about 5 mm than that of the conventional camera head.”), 4:58-65 (“[T]here is provided an advantage that the outer diameter of the camera head can be *reduced to a small size close to the diagonal length of the solid-state image pickup chip*. This provides an advantage that an image of a narrow portion, such as the interior of a pipe and the interior of a precision machine, can be picked up, which has not heretofore been achieved”), 1:53-56 (“It is an object of this invention provide a camera head for a solid-state image pickup device which camera head has an outer diameter closer to a diagonal length of a solid-state image pickup chip.”), 3:15-31 (“The chip-connecting board 226, the circuit board 227 and the connector board 228 are arranged in such a manner that their side electrodes 226e, 227e and 228e are disposed in registry with one another, and these three boards are aligned with

each other. They are connected together by the connection pins 229 to provide the circuit module 222. A surface of the solid-state image pickup chip 221 opposite to the light-receiving surface thereof is bonded to the chip-connecting board 226 through the adhesive 225. [¶] Each outer-lead 221m is bent through about 90 at a point near the chip 221, and is soldered to the side electrodes 226e, 227e and 228e of the boards 226, 227 and 228 to make electrical connections among the boards, thereby constituting the image pickup unit 22.”), 4:58-61 (“[T]here is provided an advantage that the outer diameter of the camera head can be reduced to a small size close to the diagonal length of the solid-state image pickup chip.”), Fig. 2. A person of ordinary skill in the art would have been motivated to use a circuit board having a largest dimension between 2 and 12 millimeters because it would further Wakabayashi’s express desire that the “video camera unit is made small” such that it may be “manipulate[d] ... with a thumb or index finger,” as I discussed above in Section VIII.A.1. See, e.g., Wakabayashi, 3:39-45 (“The video camera unit is made small and pivoted on an edge of the housing for rotation about an axis parallel to the edge, so that a less strength is required for joining members and accordingly the joining members can be reduced in size and weight. This structure also allows the user to manipulate the video camera with a thumb or index finger for setting an imaging angle of the video camera unit.”), 7:20-24 (“[S]ince the imager apparatus 1 allows the user to hold the housing 3 with the left hand and rotate the video camera

unit 5 with the thumb and index finger of the left hand for adjusting an imaging angle, the user can manipulate the imager apparatus 1 only with a single hand.”), 4:58-5:2 (“FIG. 1 shows a state of the imager apparatus 1 in which ... the user may support the housing 3 with his left hand to hold the liquid crystal display 6 at an angle which facilitates the viewing, and hold and rotate the video camera unit 5 with the thumb and index finger of his right hand.”), Abstract (“A video camera unit made compact to realize a reduction in weight of a video camera rotating mechanism. ... This structure also allows the user to adjust the angle of the video camera unit only with the thumb and index finger.”); Section VIII.A.1.

B. Claim 1 Is Obvious Under §103 over Wakabayashi in View of Ackland and Suzuki (Ground 2)

149. As discussed in Section VIII.A, Wakabayashi in view of Ackland (Ground 1) renders obvious claim 1.

150. To the extent it is argued that further disclosure is required for limitation [1.k] reciting “a largest dimension of said image sensor along said first plane is between 2 and 12 millimeters,” this limitation would have been obvious in further view of Suzuki’s teachings.

151. U.S. Patent No. 5,233,426 (“Suzuki”) (Ex. 1015) is a patent titled “Reduced Diameter Camera Head for Solid-State Image Pickup Device And Method of Producing the Same,” filed December 12, 1991 and issued August 3, 1993, and I understand is prior art to the ’052 patent.

152. Suzuki discloses a camera head for a solid-state image pickup device and expressly discloses that the largest dimension of the image sensor, having a “solid-state image pickup chip 221...bonded to the chip-connecting board 226,” is between 2 and 12 millimeters. Suzuki discloses that “in this embodiment of the invention, ... where the solid-state image pickup chip of inch (8.5 mm) is used, the outer diameter of the camera head is about 10 mm, and therefore is smaller about 5 mm than that of the conventional camera head.” Suzuki, 4:6-11. Suzuki further explains, through a series of production steps describing Figures 3A-3D and Figure 2, that the “image pickup chip 221” bonded to “chip connecting board 226,” “circuit board 227,” and “connector board 228” are “disposed in registry with one another” so that they are all “aligned with each other,” and are “inserted into the chassis 24”:

(i) First Step (FIG. 3A)

The inner-leads 221s are connected respectively to the electrodes of the solid-state image pickup chip 221, and the outer-leads 221m are connected respectively to the inner-leads 221s.

(ii) Second step (FIG. 3B)

The optical glass plate 224 is bonded to the light-receiving surface of the solid-state image pickup chip 221 by the adhesive 223 to protect the light-receiving surface.

(iii) Third step (FIG. 3C)

The chip-connecting board 226, the circuit board 227 and the connector board 228 are arranged in such a manner that their side electrodes 226e, 227e and 228e are disposed in registry with one

another, and these three boards are aligned with each other. They are connected together by the connection pins 229 to provide the circuit module 222. A surface of the solid-state image pickup chip 221 opposite to the light-receiving surface thereof is bonded to the chip-connecting board 226 through the adhesive 225.

(iv) Fourth step (FIG. 3D)

Each outer-lead 221m is bent through about 90° at a point near the chip 221, and is soldered to the side electrodes 226e, 227e and 228e of the boards 226, 227 and 228 to make electrical connections among the boards, thereby constituting the image pickup unit 22.

(v) Fifth step (FIG. 2)

The image pickup unit 22 is inserted into the chassis 24, and the optical glass plate 224 is fixed at its outer periphery to the chassis 24 by an adhesive 230. Subsequently, the optical filter 21 is inserted into the chassis 24 through one open end thereof, and the adhesive 25 is filled in the gap between the optical filter 21 and the chassis 24. Further, the seal plate 23 is inserted into the other open end of the chassis 24, and the adhesive 25 is filled in the gap between the seal plate 23 and the chassis 24. With the above procedure, the assembling of the camera head is completed.

As described above, in this embodiment, the electrodes of the solid-state image pickup chip are directly connected through the outer-leads with the inner-leads to the electrodes of the chip-connecting board, the circuit board, the connector board.

Suzuki, 3:1-49; *see also, e.g.,* Suzuki, Figs. 3A-3D, Fig. 2. Suzuki illustrates this in Figure 2 below, which shows a completed image pickup unit where the boards 226,

FIG. 2

153. Suzuki teaches that by configuring the image pick up chip and boards in this stacked configuration, when a “solid-state image pickup chip of...8.5 mm[] is used,” the “outer diameter of the camera head,” or chassis 24, “is about 10 mm.” See, e.g., Suzuki, 4:6-11 (“Further, in this embodiment of the invention, in the case where the solid-state image pickup chip of 1/3 inch (8.5 mm) is used, the outer diameter of the camera head is about 10 mm, and therefore is smaller about 5 mm than that of the conventional camera head.”), 1:53-56 (“It is an object of this

invention to provide a camera head for a solid-state image pickup device which camera head has an outer diameter closer to a diagonal length of a solid-state image pickup chip.”), 4:58-61 (“With the above construction, there is provided an advantage that the outer diameter of the camera head can be reduced to a small size close to the diagonal length of the solid-state image pickup chip.”). These boards are, therefore, the same size as “solid-state image pickup chip 221” in order to couple the side electrodes to the outer lead that runs at a 90° angle from the pick-up chip. Thus, the greatest dimension of the “chip-connecting board 226” of the image sensor is between 2 and 12 millimeters.

154. A person of ordinary skill in the art would have been motivated to apply Suzuki’s known teachings of an image sensor comprising a “chip-connecting board 226” between 8.5 and 10mm in implementing Wakabayashi’s imager apparatus (as modified by Ackland’s teachings) because, as Suzuki expressly discloses, this arrangement of its image sensor and circuit board allows for the “camera head [to have] an outer diameter closer to a diagonal length of a solid-state image pickup chip”—thus realizing Wakabayashi’s objective of making the camera unit “compact,” and to improve the camera’s “stability and reliability,” as discussed further below. See, e.g., Suzuki, 1:53-56, 4:6-11 (“...the solid-state image pickup chip of 1/3 inch (8.5 mm) is used, the outer diameter of the camera head is about 10 mm, and therefore is smaller about 5 mm than that of the conventional camera head.”), 4:58-

65 (“...the outer diameter of the camera head can be reduced to a small size close to the diagonal length of the solid-state image pickup chip. This provides an advantage that an image of a narrow portion, such as the interior of a pipe and the interior of a precision machine, can be picked up”); Wakabayashi, Abstract (“A video camera unit made compact to realize a reduction in weight of a video camera rotating mechanism. ... allows the user to adjust the angle of the video camera unit only with the thumb and index finger.”), 3:39-46 (“The video camera unit is made small ... so that a less strength is required for joining members and accordingly the joining members can be reduced in size and weight. This structure also allows the user to manipulate the video camera with a thumb or index finger for setting an imaging angle of the video camera unit.”), 14:6-10.

155. Like Wakabayashi and Ackland, Suzuki is in the same field of art and is analogous art to the '052 patent—both are in the same field related to solid-state image sensors for cameras. See, e.g., '052 patent, Abstract (“A reduced area imaging device...”), 1:32-36 (“...solid state image sensors ...video images for viewing.”); Suzuki, Abstract (“The present invention provides a compact camera head for a solid-state image pickup device, a dimension of which is not so limited by a package for a solid-state image pickup element.”), 1:8-11 (“This invention relates to a camera head for a solid-state image pickup device which camera head uses a solid-state image pickup chip, and also relates to a method of producing such

a camera head.”), 1:53-56 (“It is an object of this invention to provide a camera head for a solid-state image pickup device which camera head has an outer diameter closer to a diagonal length of a solid-state image pickup chip.”).

156. Suzuki is also reasonably pertinent to the alleged problem(s) identified in the '052 patent of arranging the circuitry of an image sensor, including, for example, to minimize the size of the device. *See, e.g., '052 patent, 3:31-39* (“It is one general object of this invention to provide a wireless endoscope incorporating reduced area imaging devices which take advantage of “camera on a chip” technology, but rearrange the circuitry in a stacked relationship so that there is a minimum profile presented when used within a surgical instrument or other investigative device. It is another object of this invention to provide a wireless endoscope utilizing low cost imaging devices...”); 5:52-54; Suzuki, Abstract (“The present invention provides a compact camera head for a solid-state image pickup device, a dimension of which is not so limited by a package for a solid-state image pickup element.”), 1:53-56 (“It is an object of this invention to provide a camera head for a solid-state image pickup device which camera head has an outer diameter closer to a diagonal length of a solid-state image pickup chip.”), 3:61-4:12.

157. Suzuki expressly discloses that its arrangement of the image sensor and circuit board allows for the “camera head [to have] an outer diameter closer to a diagonal length of a solid-state image pickup chip.” *See, e.g., Suzuki, 1:53-56* (“It

is an object of this invention provide a camera head for a solid-state image pickup device which camera head has an outer diameter closer to a diagonal length of a solid-state image pickup chip.”), 4:6-11 (“Further, in this embodiment of the invention, in the case where the solid-state image pickup chip of 1/3 inch (8.5 mm) is used, the outer diameter of the camera head is about 10 mm, and therefore is smaller about 5 mm than that of the conventional camera head.”), 4:58-65 (“[T]here is provided an advantage that the outer diameter of the camera head can be reduced to a small size close to the diagonal length of the solid-state image pickup chip. This provides an advantage that an image of a narrow portion, such as the interior of a pipe and the interior of a precision machine, can be picked up, which has not heretofore been achieved.”).

158. Suzuki further discloses its arrangement of its image sensor and circuit board allows “not only the solid-state image pickup chip but also the boards including the electric circuits parts can be sealed, and therefore the stability and reliability of the circuit are advantageously enhanced.” See, e.g., Suzuki, 4:30-45 (“With this arrangement, not only the solid-state image pickup chip but also the boards including the electric circuits parts can be sealed, and therefore the stability and reliability of the circuit are advantageously enhanced”), 3:61-4:6 (“With this arrangement, the parts (including the electric circuit board) contained in the chassis

can be sealed, and therefore the stability and reliability of the circuit can be enhanced.”).

159. In light of the above, a person of ordinary skill in the art would have been motivated and found it routine, straightforward and advantageous to apply Suzuki’s known teachings of an image sensor comprising a “chip-connecting board 226” between 8.5 and 10mm in implementing Wakabayashi’s imager apparatus (as modified by Ackland’s teachings) such that size of the image sensor is between 8.5 and 10 mm and the overall size of Wakabayashi’s camera head is reduced, thus allowing the improving the camera device’s “stability and reliability.” *See, e.g.,* Suzuki, 1:53-56, 3:1-49, 3:61-4:12, 4:30-65. A person of ordinary skill in the art would have known that such a combination (yielding the claimed limitations) would predictably work and provide the expected functionality.

C. Claims 3 and 7 Are Obvious Under §103 over Wakabayashi in View of Ricquier and Dierickx (Ground 3)

1. Overview of U.S. Patent 5,903,706 (“Wakabayashi”) (Ex. 1027)

160. As discussed in Section VIII.A.1, Wakabayashi teaches a portable imager apparatus that includes a video camera and a display within its housing. *See* Section VIII.A.1.

2. Overview of N. Ricquier et al., “The CIVIS Sensor: A Flexible Smart Imager with Programmable Resolution” (“Ricquier”) (Ex. 1038)

161. Ricquier (Ex. 1038) is a conference paper presented at the Proceedings of SPIE – The International Society of Optical Engineering in May 1994, and I understand, is prior art to the '052 patent. *See* Section X.

162. Ricquier describes a dedicated imager for a camera programmed to operate in several resolutions. *See, e.g.*, Ricquier, 2.

163. Ricquier’s imager includes a CMOS photodiode array of 256*256 pixels that are addressable by column and row (*i.e.*, “X-Y addressable”) using a timing controller implemented on an off-chip driving unit. *See, e.g.*, Ricquier, 2, 3, 5, 9, Fig. 1. Figure 1 is a schematic representation of 2*2 of the 256*256 CMOS pixel array:

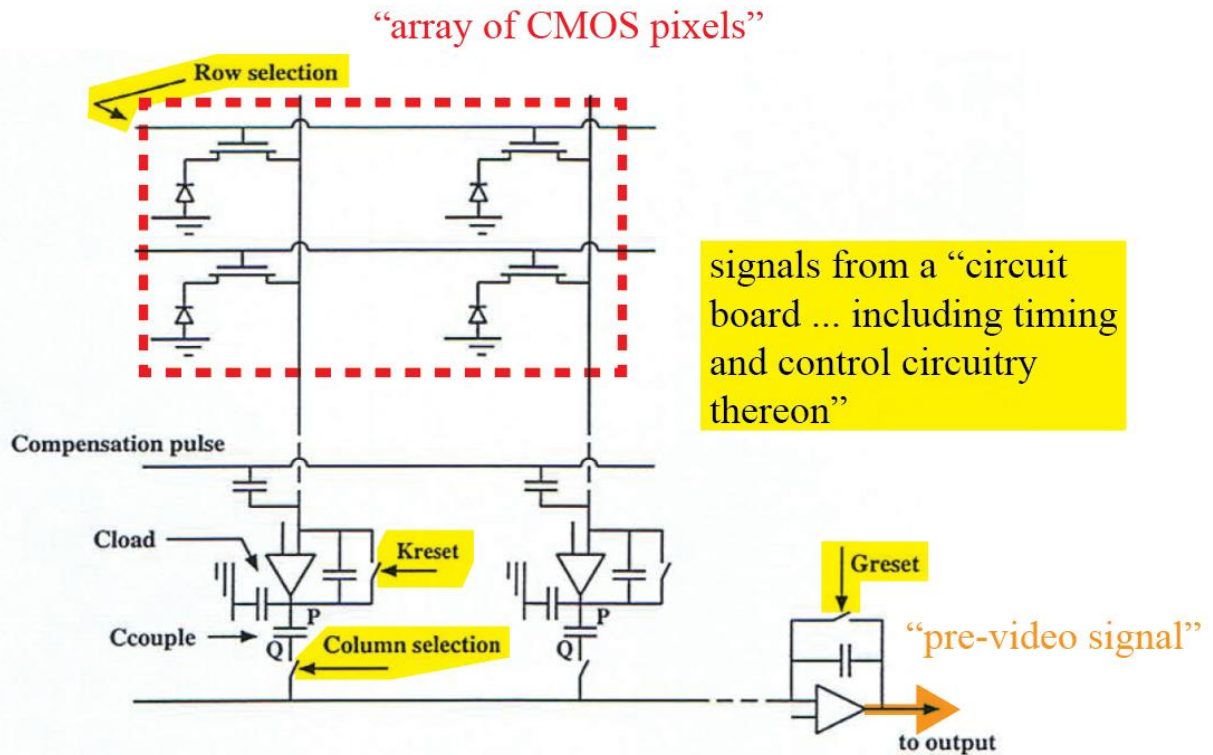


Figure 1: Schematic representation of the sensor architecture

Ricquier, Fig. 1 (annotated).

164. Ricquier teaches that the “256*256 X-Y addressable photodiode array” acquires image data by sequentially driving row selection signals to “transfer[] in parallel a row of 256 charges to 256 charge sensitive amplifiers” and outputting these signals from the array, as shown in Figure 1. *See, e.g., Ricquier, 2-3.* For each row, the “charges are converted simultaneously to a voltage at the output[s] of...amplifiers located at the end of the column readout lines.” *See, e.g., Ricquier, 3.*

165. A person of ordinary skill in the art would have understood Ricquier’s “image data” “output” as shown in Figure 1 is a pre-video signal produced by

Ricquier's timing and control circuitry. *See, e.g.*, Ricquier, 2-4. Ricquier teaches that the readout of the X-Y addressable photodiode array is done by "controlling the clocking scheme" using a "timing controller" on "an off-chip driving unit" for driving the "row selection," "column selection," and reset signal inputs (highlighted in Figure 1 above). *See, e.g.*, Ricquier, 3-4.

3. Overview U.S. Patent Publication 2001/0010551 ("Dierickx") (Ex. 1041)

166. U.S. Patent Publication 2001/0010551 ("Dierickx") (Ex. 1041) is a patent publication titled "Circuit, Pixel, Device and Method for Reducing Fixed Pattern Noise in Solid State Imaging Devices," filed October 31, 1996 and published August 2, 2001, and I understand, is prior art to the '052 patent.

167. Dierickx teaches "CMOS ... image sensors with active pixels" where each "active pixel is configured with means integrated in the pixel to amplify the charge that is collected on the light sensitive element." Dierickx, ¶6.

168. Dierickx teaches "solid state imaging devices" including "CMOS ... image sensors with active pixels." Dierickx, ¶¶2, 6. Dierickx teaches that "active pixels" include, in its "most simple form, ... [a] photo detector[] ... [and] the amplifying part of the pixel." Dierickx, ¶53. Dierickx illustrates two such pixels, each with an "amplifier" 91 or 92, in Figure 6:

“individual active CMOS pixels ...
each includes an amplifier”

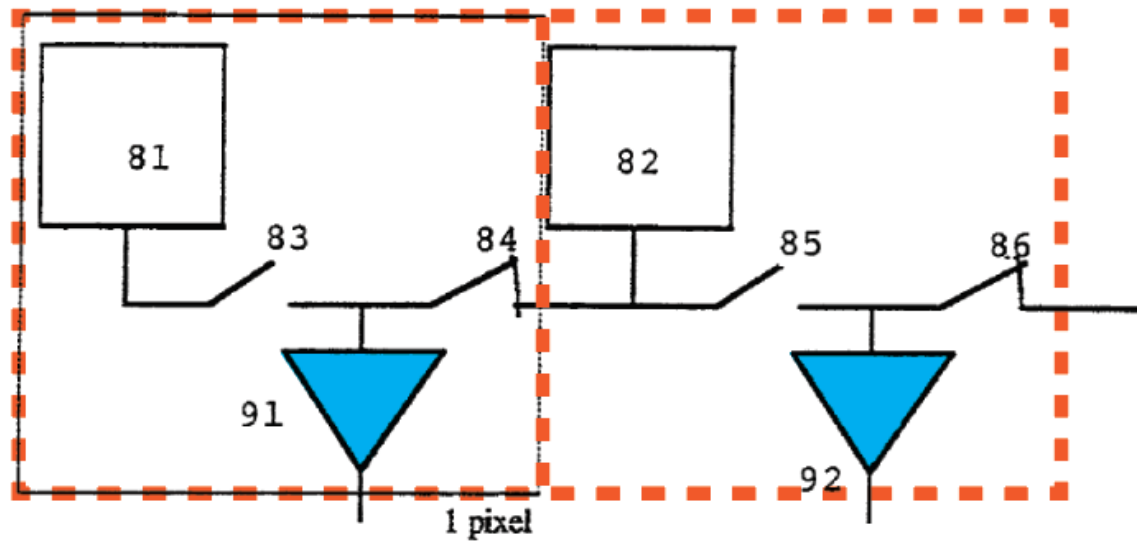


Fig. 6

Dierickx, Figure 6 (annotated). *See also, e.g.,* Dierickx, Figure 5, ¶¶25, 53.

4. Motivation to Combine Wakabayashi and Ricquier

169. While Wakabayashi discloses that the image sensor uses a “solid-state imager device” and a “circuit for driving the solid-state imager device” to “generate[] an opto-electrically converted signal” (Wakabayashi, 9:11-15), Wakabayashi does not expressly state that its “imager device 27 [] electrically connected to the camera circuit board 29” includes an array of CMOS pixels. Ricquier expressly provides this additional implementation detail of the “acquisition of image data” using a “256*256 X-Y addressable photodiode array...realised in a 1.5 μm standard CMOS technology.” *See, e.g.,* Ricquier, 9. Similarly, while Wakabayashi does not detail

the timing and control circuitry of its “imager device 27 [] electrically connected to the camera circuit board 29,” Ricquier discloses that the readout from the “256*256 imager” is driven by a “timing controller (realised in an off-chip driving unit).” *See, e.g., Ricquier, 2-4, 9.*

170. A person of ordinary skill in the art would have been motivated to apply Ricquier’s known teachings described above in implementing Wakabayashi’s portable imager apparatus. Like Wakabayshi, Ricquier is in the same field of art and is analogous art to the ’052 patent—all are in the same field related to active CMOS image sensors for use in cameras. *See, e.g., ’052 patent, Abstract, 1:33-36, 7:65-8:1; Ricquier, 2-3, 5, 9.* Ricquier is also reasonably pertinent to the alleged problem(s) identified in the ’052 patent of arranging the circuitry of a CMOS image sensor, including, *e.g.,* to minimize the size of the device, to be “low cost,” and to reduce image noise in CMOS sensors. *See, e.g., ’052 patent, 3:31-37, 5:52-54, 12:11-14; Ricquier, 2-3, 8 (noise reduction).* A person of ordinary skill in the art would have been further motivated to apply Ricquier’s known teachings in implementing Wakabayashi’s solid state imager device because of Ricquier’s express advantages of “selective addressability” and “multiple resolutions...[and] data rates upto 10 MHz.” *See, e.g., Ricquier, 2.* By implementing Ricquier’s teachings, an electronic shutter and the ability to change the captured resolution and frame rate were realized. *See, e.g., Ricquier, 9.* As a result of this ability to change resolution, the frame rate

of the image sensor can be advantageously be changed on the fly. Ricquier, 4. A person of ordinary skill in the art would have been further motivated to apply Ricquier's teachings in implementing Monroe's CMOS imager teachings because of Ricquier's advantages of using a "timing controller" located off-chip, which adds flexibility in selecting from the several design choices for "fitting ... the components into the available space" and "placement" of circuitry to "allow for a more compact camera head." Ricquier, 3, 4; A Guide to Printed Circuit Board Design, 15, 20; *see also* Tanuma (Ex. 1016, published 5/14/1987, and I understand is prior art to the '052 patent), 4-5 (placing circuit components on opposite side of circuit board from image sensor results in "compact camera head"), Fig. 2.

171. A person of ordinary skill in the art would have found it routine, straightforward and advantageous to apply Ricquier's known teachings of an array of CMOS pixels and of placing a "timing controller" "off-chip" in implementing Wakabayashi's solid state imager device, and would have known that such a combination (yielding the claimed limitations) would predictably work and provide the expected functionality.

5. Motivation to Combine Wakabayashi, Ricquier, and Dierickx

172. While Ricquier discloses the pixels in its CMOS pixel array "consist of a photodiode and a switch" (*see, e.g.*, Ricquier, 3), Dierickx teaches "CMOS ... image sensors with active pixels" where each "active pixel is configured with means

integrated in the pixel to amplify the charge that is collected on the light sensitive element.” Dierickx, ¶6.

173. A person of ordinary skill in the art would have been motivated to apply Dierickx’s known teachings described above in implementing Wakabayashi’s “imager apparatus” (as modified by the teachings of Ricquier). Like Wakabayashi, and Ricquier, Dierickx is in the same field of art and is analogous art to the ’052 patent—both are in the same field related to active CMOS image sensors for use in cameras. *See, e.g.*, ’052 patent, Abstract (“[a] reduced area imaging device...”), 1:32-36 (“...solid state image sensors...”), 7:65-8:1; Dierickx, ¶¶4 (“Commonly solid state image sensors are implemented in ... CMOS ... Solid state image sensors find a widespread use in camera systems.”), 6, 19 (“The imaging device of the present invention is configured as a pixel matrix that is used as a focal plane image sensor.”). In addition, like Wakabayashi and Ricquier, Dierickx is also reasonably pertinent to the alleged problem identified in the ’052 patent of providing a “low cost imaging device[.]” ’052 patent, 3:31-39 (“It is one general object of this invention to provide ... reduced area imaging devices.... It is another object of this invention to provide ... low cost imaging devices....”); Dierickx, ¶5 (“CMOS is a technology being offered by most foundries whereas CCD-technology is ... more ... expensive.”).

174. A person of ordinary skill in the art would have been motivated to apply Dierickx's known teachings of an array of active CMOS pixels, each including an amplifier, in implementing Wakabayashi's "video camera" (as modified by the teachings of Ricquier) to advantageously provide "high image quality" (*see, e.g.*, Dierickx ¶19 ("The imaging device of the present invention is configured as a pixel matrix that is used as a focal plane image sensor.")) improving the functionality of Wakabayashi's "video camera" without "lead[ing] to a larger size and increased weight" (*see, e.g.*, Wakabayashi, 2:27-29, 3:39-45). Dierickx explains that by using "CMOS ... image sensors with active pixels" instead of "passive pixels," such as those taught by Ricquier, the pixels of the image sensor advantageously "amplify the charge ... collected on the light sensitive element" and are, therefore, "less sensitive to noise fluctuations." *See, e.g.*, Dierickx, ¶6. Moreover, a person of ordinary skill in the art would have been motivated to apply Dierickx's known teachings of a "CMOS ... image sensors with active pixels" in implementing Wakabayashi's "imager apparatus" because Dierickx teaches that "active pixel[s]" can include "additional electronics" such that the "image sensor may be equipped to execute more sophisticated functions" such as "operation at higher speed or operation in more extreme illumination conditions." *See, e.g.*, Dierickx, ¶6.

175. In light of the above, a person of ordinary skill in the art would have found it routine, straightforward and advantageous to apply Dierickx's known

teachings of “CMOS ... image sensors with active pixels” in implementing Wakabayashi’s teachings of an “imager apparatus” (as modified by the teachings of Ricquier) and would have known that such a combination (yielding the claimed limitations) would predictably work and provide the expected functionality.

6. Invalidity of Claims 3 and 7 Over Wakabayashi in view of Ricquier and Dierickx (Ground 3)

a. Element [3.pre]

176. **Element [3.pre] recites “An imaging device.”** To the extent the preamble is limiting, Wakabayashi discloses an imaging device (*e.g.*, “a portable imager apparatus”).

177. My analysis of [1.pre] with respect to similar language is equally applicable to [3.pre]. *See* Section VIII.A.4.a.

b. Element [3.a]

178. **Element [3.a] recites “a housing.”** Wakabayashi discloses element [3.a]. Wakabayashi discloses a housing (*e.g.*, “imager apparatus 1” enclosure formed by “front panel 2a,” “rear panel 2b,” “camera case 16,” and “battery-cover 11”).

179. My analysis of [1.a] with respect to similar language is equally applicable to [3.a]. *See* Section VIII.A.4.b.

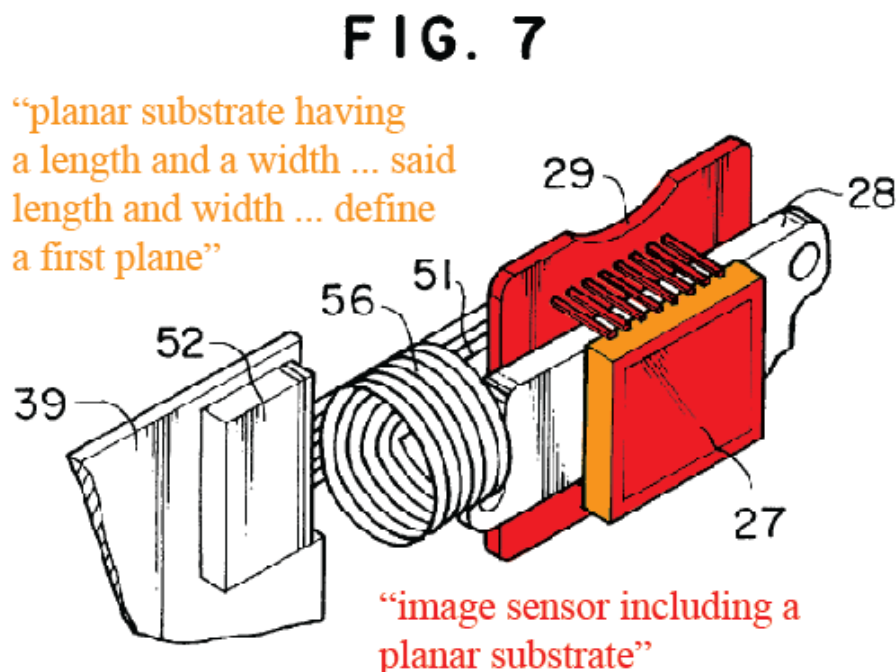
c. Element [3.b]

180. Element [3.b] recites “an image sensor mounted in said housing, said image sensor including a planar substrate having a length and a width thereto, wherein said length and width of said planar substrate define a first plane, said planar substrate including an array of CMOS pixels thereon.”

Wakabayashi in view of Ricquier renders obvious element [3.b]. Wakabayashi discloses an image sensor (*e.g.*, “imager device 27 [] electrically connected to the camera circuit board 29 by soldering”) mounted in said housing (*e.g.*, “circuit board 29 is fixed on the mounting plate 28 ... fixed to the camera case 16”), said image sensor including a planar substrate having a length and a width thereto, wherein said length and width of said planar substrate define a first plane (*e.g.*, plane defined by length and width of “imager device 27” as shown in Fig. 7), said planar substrate including an [image sensing area] thereon (*e.g.*, area of “imager device 27” upon which the “image of the subject is focused”). Ricquier discloses a planar substrate (*e.g.*, substrate for “fabricat[ing] in a standard 1.5 μm CMOS technology”) including an array of CMOS pixels thereon (*e.g.*, “pixel array...realised in...CMOS technology”).

181. My analysis of [1.b] with respect to similar language is equally applicable to [3.b]. *See* Section VIII.A.4.c.

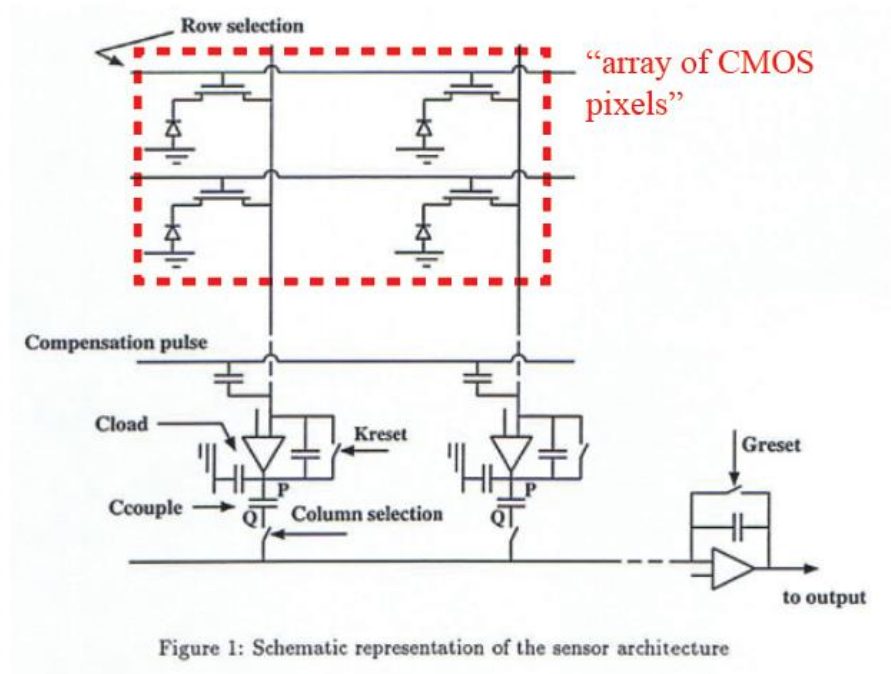
182. In addition, Wakabayashi discloses that its “imager device 27” is a “solid state imager device.” For example, Wakabayashi also explains “[a] camera head 100, which includes a light receiving lens, a solid-state imager device, a circuit for driving the solid-state imager device, and so on, generates an opto-electrically converted signal 101 which is inputted to a camera circuit 102.” Wakabayashi, 9:10-14. As discussed in §VIII.A.1, a person of ordinary skill in the art would have understood “imager device 27” includes a planar semiconductor substrate on which the image sensing region, for converting light into charge, is fabricated. And, as illustrated in Figure 7, Wakabayashi discloses that the “imager device 27” has a length and width that defines a first plane:



Wakabayashi, Fig. 7 (annotated).

183. While Wakabayashi discloses that the image sensor uses a “solid-state imager device” and a “circuit for driving the solid-state imager device” to “generate[] an opto-electrically converted signal” (Wakabayashi, 9:11-15 (“A camera head 100, which includes a light receiving lens, a solid-state imager device, a circuit for driving the solid-state imager device, and so on, generates an opto-electrically converted signal 101 which is inputted to a camera circuit 102.”)), Wakabayashi does not expressly state that its “imager device 27” includes an array of CMOS pixels. Ricquier provides this additional implementation detail of the “acquisition of image data” using a “256*256 X-Y addressable photodiode array...realised in a 1.5 μm standard CMOS technology.” *See, e.g., Ricquier, 9.*

184. Ricquier describes a “dedicated imager” that “can be programmed to operate in several resolutions.” *See, e.g., Ricquier, 2.* For this imager, “an X-Y addressable architecture was selected.” Ricquier, 3. In the imager, “[a] pixel consists of a photodiode and a switch.” *See, e.g., Ricquier, 3, Fig. 1.* “The pixel array consists of 256 by 256 square pixels arranged on a pixel pitch of 19 μm and realised in a 1.5 μm n-well CMOS technology,” and “images are formed on the sensor plane.” *See, e.g., Ricquier, 5-6.*



Ricquier, Fig. 1 (annotated).

185. As discussed in Section VIII.C.4, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to apply Ricquier’s known teachings of a CMOS implemented “X-Y addressable photodiode array” in implementing Wakabayashi’s imager apparatus, and would have recognized this combination (yielding the claimed limitation) would work as expected.

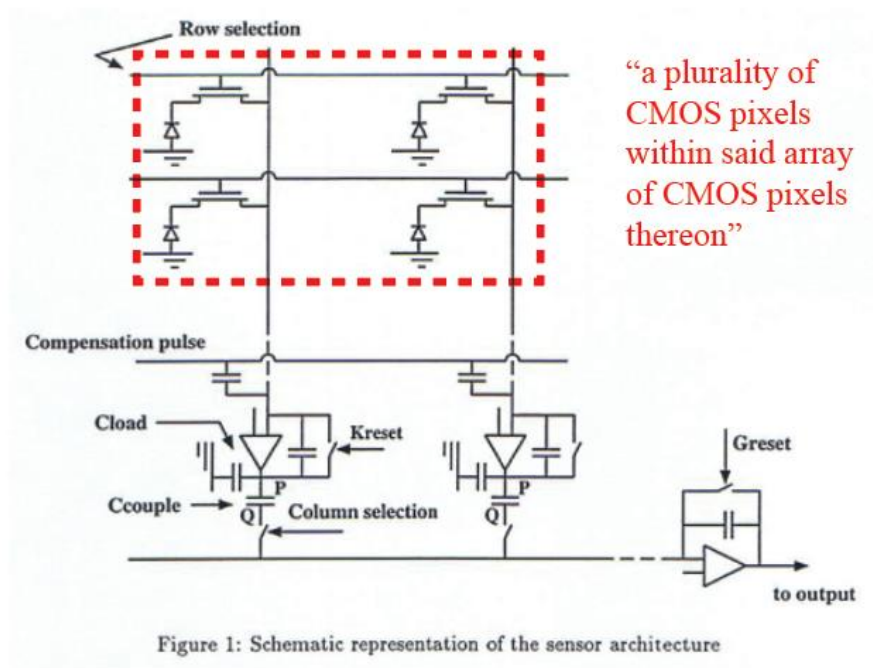
d. Element [3.c]

186. **Element [3.c] recites “wherein a plurality of CMOS pixels within said array of CMOS pixels each include an amplifier.”** Wakabayashi in view of Ricquier and Dierickx renders obvious element [3.c]. Ricquier discloses a plurality

of CMOS pixels within said array of CMOS pixels thereon (*e.g.*, “pixel array consists of 256 by 256 square pixels ... realised in ... CMOS technology”). Deirickx discloses CMOS pixels each include an amplifier (*e.g.*, “amplifying part of the pixel”).

187. As discussed in relation to element [3.b], Ricquier discloses a CMOS pixel array.

188. Ricquier discloses that the “square 256*256 imager was fabricated in a standard 1.5 μm CMOS technology” where the “pixels [are] on the plane itself.” *See, e.g.*, Ricquier, 2, 5 (“pixel array consists of 256 by 256 square pixels arranged on a pixel pitch of 19 μm and realised in a 1.5 μm n-well CMOS technology”). Figure 1 of Ricquier further illustrates the arrangement of the plurality of CMOS pixels in an array:



Ricquier, Figure 1 (annotated).

189. While Ricquier discloses the pixels in its CMOS pixel array “consist of a photodiode and a switch” (*e.g.*, Ricquier, 3), Ricquier does not disclose that its CMOS pixels each include an amplifier. Dierickx teaches “CMOS ... image sensors with active pixels” where each “active pixel is configured with means integrated in the pixel to amplify the charge that is collected on the light sensitive element.” Dierickx, ¶6.

190. Dierickx teaches “solid state imaging devices” including “CMOS ... image sensors with active pixels.” Dierickx, ¶¶2, 6. Dierickx teaches that “active pixels” include, in its “most simple form, ... [a] photo detector[] ... [and] the

amplifying part of the pixel.” Dierickx, ¶53. Dierickx illustrates two such pixels, each with an “amplifier” 91 or 92, in Figure 6:

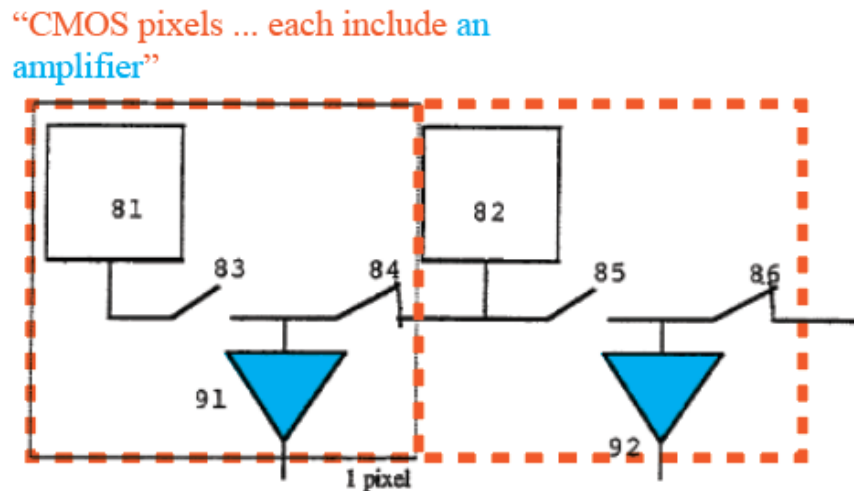


Fig. 6

Dierickx, Figure 6 (annotated). *See also, e.g.,* Dierickx, Figure 5, ¶¶25, 53.

191. As discussed in Sections VIII.C.4-5, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to apply Dierickx’s known teachings of “CMOS ... image sensors with active pixels” in implementing Wakabayashi’s teachings of an “imager apparatus” (as modified by the teachings of Ricquier) and would have recognized this combination (yielding the claimed limitation) would work as expected.

e. Element [3.d]

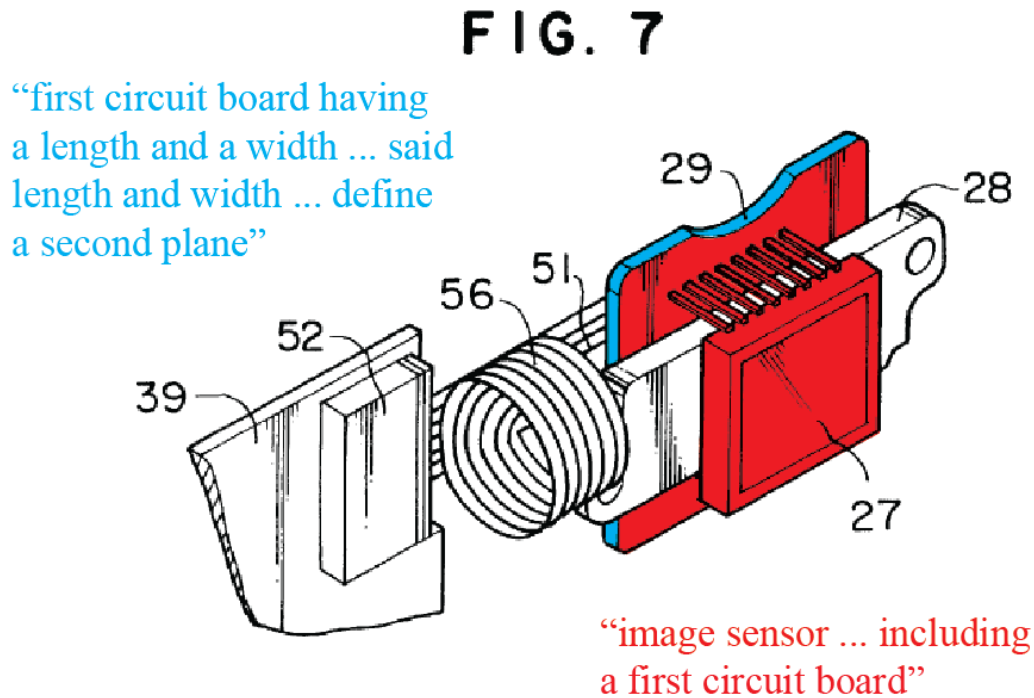
192. **Element [3.d]** recites “said image sensor further including a first circuit board having a length and a width thereto, wherein said length and

width of said first circuit board define a second plane, said first circuit board including timing and control circuitry thereon, said timing and control circuitry being coupled to said array of CMOS pixels.” Wakabayashi in view of Ricquier renders obvious element [3.d]. Wakabayashi discloses said image sensor further including a first circuit board having a length and a width thereto, wherein said length and width of said first circuit board define a second plane (*e.g.*, plane defined by length and width of “circuit board 29” as shown in Figure 7). Ricquier discloses circuitry (*e.g.*, “off-chip driving unit”) including timing and control circuitry thereon (*e.g.*, “timing controller” to “drive...row selection and column selection signal[s]” of “X-Y addressable photodiode array”), said timing and control circuitry being coupled to said array of CMOS pixels (*e.g.*, “timing controller” “controlling the sequence of addresses and reset pulses of” “photodiode array” as illustrated in Figure 1).

193. My analysis of [1.b] and [1.d] with respect to similar language is equally applicable to [3.d]. *See* Section VIII.A.4.e.

194. As discussed in [1.b], Wakabayashi discloses an image sensor including a “solid-state” “imager device 27” (an image sensor chip) mounted on a “circuit board 29” (a first circuit board having a length and width) as depicted in Figure 7. *See, e.g.*, Wakabayashi, 5:56-59, 6:47-49, 9:10-14, Fig. 7. With regards

to the analysis of [3.d], however, the length and width of “circuit board 29,” as illustrated in Figure 7, defines a *second* plane:



Wakabayashi, Fig. 7 (annotated).

195. While Wakabayashi discloses the image sensor uses a “solid-state imager device” and “circuit for driving the solid-state imager device” to “generate[] an opto-electrically converted signal” (Wakabayashi, 9:11-15), Wakabayashi does not expressly disclose the how timing of its “imager device 27” is controlled. Ricquier expressly provides this additional implementation detail and discloses that a “timing controller” generates the “X-Y addresses and control pulses” and uses “decoders [to] drive...row selection and column selection signal” from the “X-Y addressable photodiode array.” *See, e.g.,* Ricquier, 3, 4, 9. Ricquier further discloses

that this “timing controller,” while electrically coupled to the photodiode array to provide the selection signals, is “off-chip.” Ricquier, 4. A person of ordinary skill in the art would have understood that Ricquier’s Figure 1 (annotated below) depicts timing and control signals (yellow) from the off-chip timing controller applied to the read-out circuitry of the array:

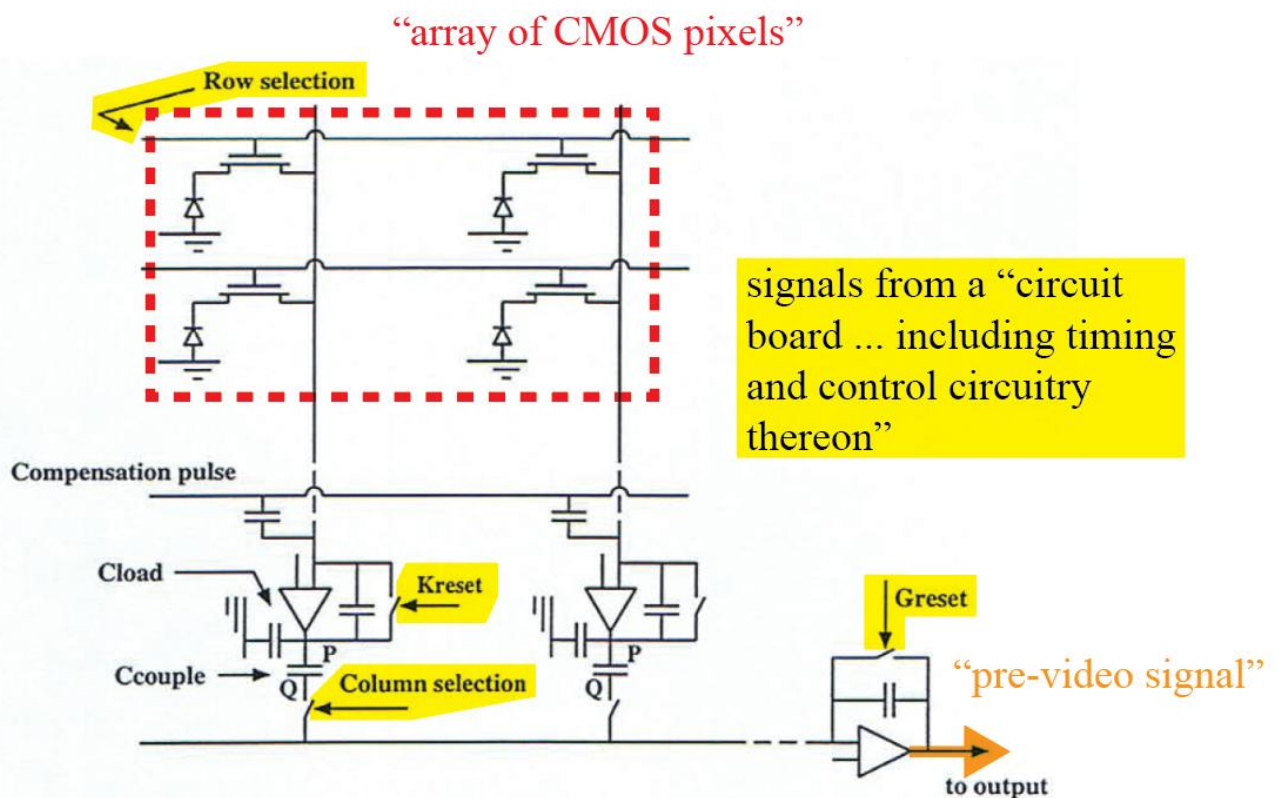


Figure 1: Schematic representation of the sensor architecture

Ricquier, Fig. 1 (annotated).

196. For example, Ricquier explains that “[b]y controlling the sequence of addresses and reset pulses of the amplifiers, charges of different pixels are accumulated.” Ricquier, 2. Control pulses generated by “two decoders drive one

particular row selection and column selection signal” based on “X-Y addresses.” Ricquier, 3, 9. Ricquier teaches that “[a]fter selecting one particular row of pixels, these charges are converted simultaneously to a voltage at the output of the different charge sensitive amplifiers located at the end of the column readout lines.” Ricquier, 3. Then, “[b]ased on the column selection signals, these nodes Q are again discharged to their starting value, at the same time creating a voltage variation at the output amplifier proportional to the charges at that column.” Ricquier, 3. Every column selection is “followed by a reset pulse on the Greset switch bringing back the output amplifier into its initial state” and “after that, another charge packet can be received.” Ricquier, 3. After reading out a particular row of pixels, “the Kreset switch is closed causing the integration capacitor to discharge.” Ricquier, 3. Ricquier further teaches that “[b]y using the Kreset switches and the Greset switch in an appropriate way, it is possible to accumulate charge packets of different pixels or of different column amplifiers on the integration capacitors according to different patterns.” Ricquier, 3. By “controlling the clocking scheme, the resolution of the imager can be altered and it is even possible to create rectangular pixel patterns with a resolution varying across the rows. In order to limit the complexity of the timing controller (realised in an off-chip driving unit) only timing configurations of some very common patterns are provided: apart from the normal resolution (1 * 1) also the

addition of pixel charges in 2*2, 4*4 and 8*8 neighbourhoods was foreseen.”

Ricquier, 4, Fig. 1.

197. Ricquier further discloses that this “timing controller,” while electrically coupled to the photodiode array to provide the selection signals, is “off-chip.”

198. As discussed in Section VIII.C.4, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to apply Ricquier’s known teachings of placing a “timing controller” “off-chip” in implementing Wakabayashi’s imager apparatus such that the timing controller is located on the circuit board 29—i.e., off-chip from imager device 27, and would have recognized this combination (yielding the claimed limitation) would work as expected.

f. Element [3.e]

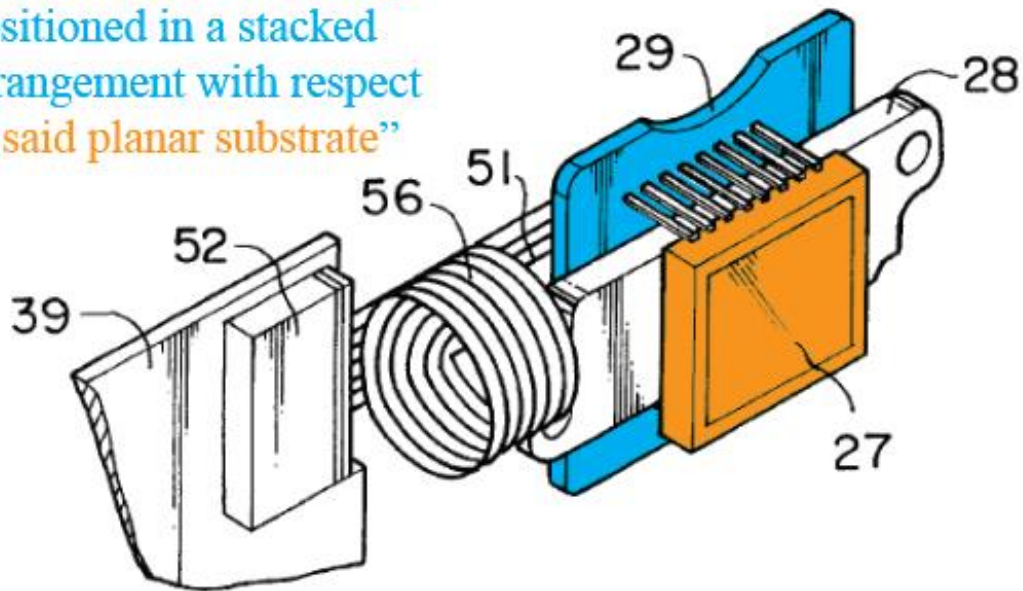
199. **Element [3.e] recites “said first circuit board being positioned in a stacked arrangement with respect to said planar substrate, said second plane of said first circuit board being substantially parallel to said first plane of said planar substrate.”** Wakabayashi discloses element [3.e]. Wakabayashi discloses that said first circuit board being positioned in a stacked arrangement with respect to said planar substrate (*e.g.*, “imager device 27 [] electrically connected to [] circuit board 29 by soldering” in a stacked arrangement as illustrated in Figs. 3 and 7), said

second plane of said first circuit board being substantially parallel to said first plane of said planar substrate (*e.g.*, plane defined by length and width of “circuit board 29” parallel with plane defined by length and width of “imager device 27” as shown in Figs. 3 and 7).

200. Wakabayashi Figures 3 and 7 illustrate the planes defined by length and width of “circuit board 29” is substantially parallel to the plane defined by the length and width of “imager device 27,” and that “circuit board 29” is in a stacked arrangement with respect to “imager device 27.” Specifically, Figure 7 illustrates the perspective view of the components of Wakabayashi’s imager apparatus and Figure 3 illustrates its cross section. From these two figures Wakabayashi shows that the length and width of the “circuit board 29” defines a second plane that is parallel to the first plane defined by the length and width of “imager device 27.” Additionally, the two figures also show that the “circuit board 29” is stacked behind “imager device 27:

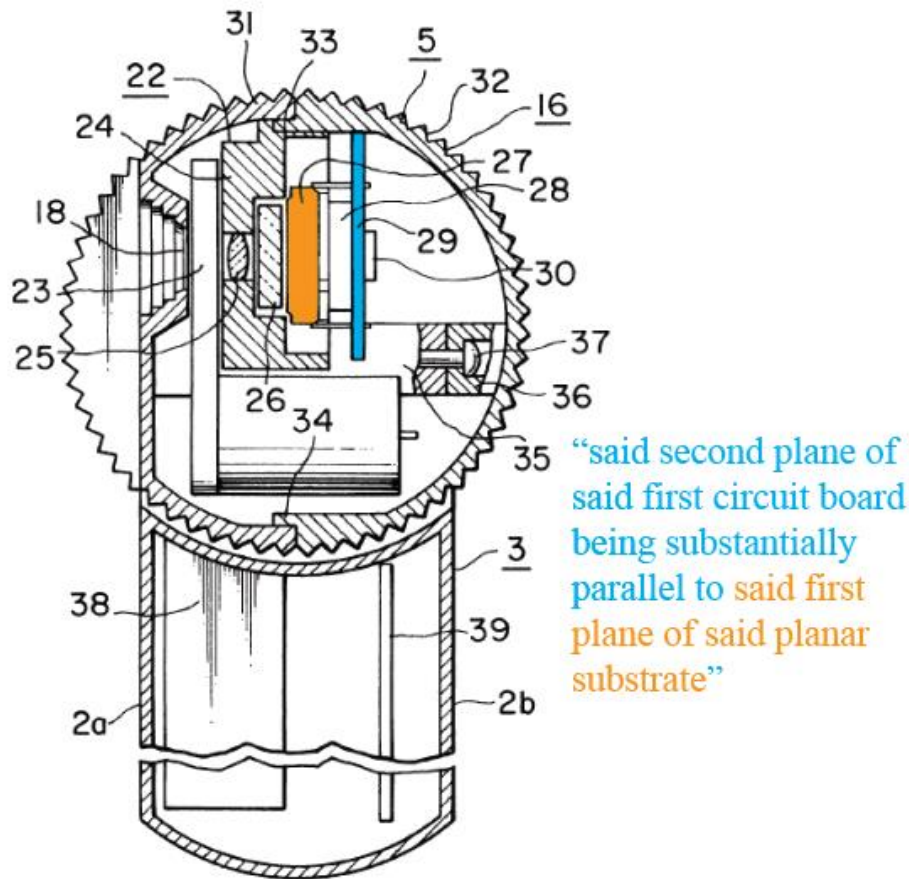
FIG. 7

“first circuit board being
positioned in a stacked
arrangement with respect
to said planar substrate”



Wakabayashi, Fig. 7 (annotated).

FIG. 3



Wakabayashi, Fig. 3 (annotated).

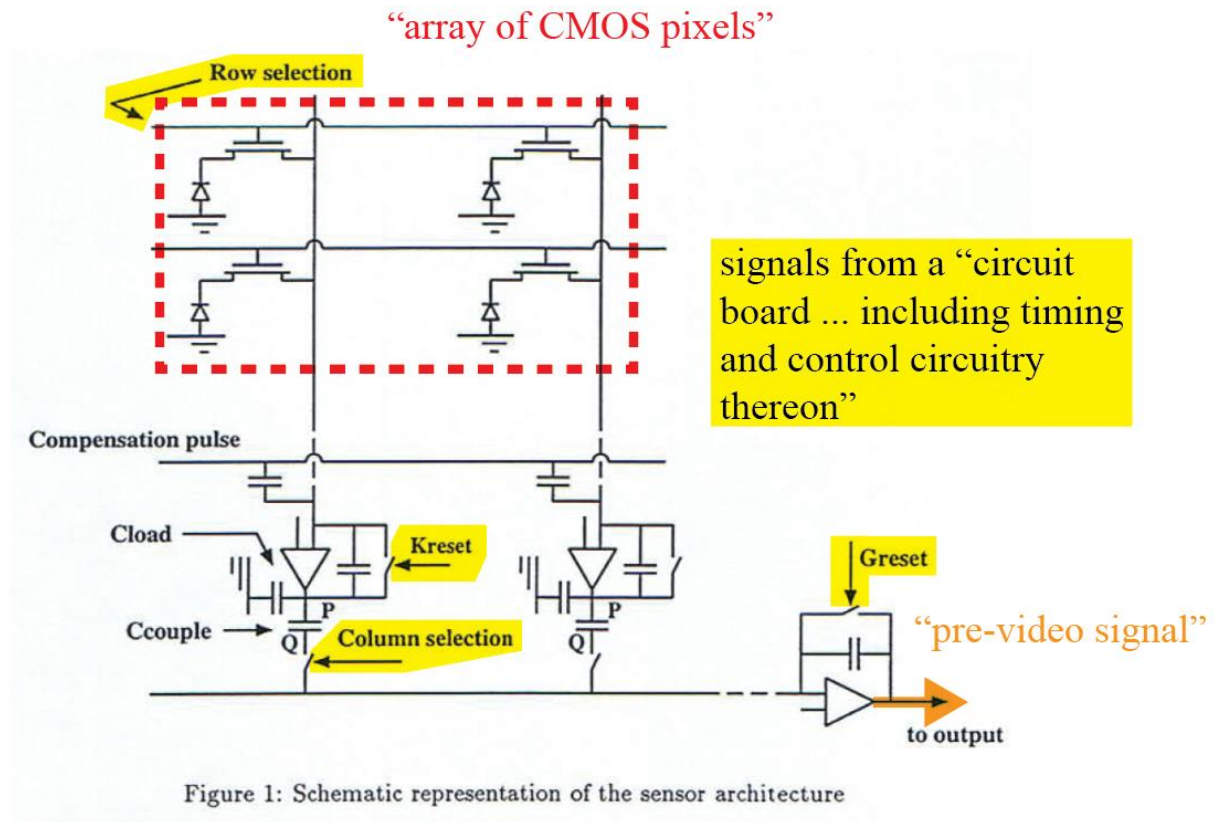
g. Element [3.f]

201. **Element [3.f]** recites “said image sensor producing a pre-video signal.” Ricquier discloses element [3.f]. Ricquier discloses said image sensor producing a pre-video signal (*e.g.*, “image data” “output,” as shown in Figure 1).

202. While Wakabayashi does not expressly disclose its image sensor produces a pre-video signal, Ricquier discloses image data readout from the “256*256 imager” is “output” from the array. Ricquier, Fig. 1, Abstract, 4. A person

of ordinary skill in the art would have understood Ricquier's "output" as shown in Figure 1 is a pre-video signal produced by Ricquier's image sensor.

203. For example, Ricquier discloses that "[t]he readout occurs in two phases"—"[a]fter transferring in parallel a row of charges to 256 charge sensitive amplifiers, these signals are coupled to a single output amplifier." See, e.g., Ricquier, 2. Ricquier teaches that "[t]he readout of the charge packets that are accumulated during the integration time, proceeds as follows"—"[a]fter selecting one particular row of pixels, these charges are converted simultaneously to a voltage at the output of the different charge sensitive amplifiers located at the end of the column readout lines." Ricquier, 4. As illustrated in Figure 1, Ricquier discloses that the pre-video signal at the "output" is controlled by the "timing controller" "off-chip." See, e.g., Ricquier, 4; Fig. 1.



Ricquier, Fig. 1 (annotated).

204. As discussed in Section VIII.C.4, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to apply Ricquier's known teachings of an image sensor producing a pre-video signal in implementing Wakabayashi's imager apparatus, and would have recognized this combination (yielding the claimed limitation) would work as expected.

h. Element [3.g]

205. Element [3.g] recites "a second circuit board mounted in said housing, said second circuit board being electrically coupled to said planar substrate and to said first circuit board, said second circuit board having a

length and a width thereto, wherein said length and width of said second circuit board define a third plane, said second circuit board including circuitry thereon to convert said pre-video signal to a post-video signal, said second circuit board being offset from said first circuit board and from said planar substrate, said third plane of said second circuit board being substantially parallel to said second plane of said first circuit board and to said first plane of said planar substrate.” Wakabayashi discloses element [3.g]. Wakabayashi discloses a second circuit board mounted in said housing (*e.g.*, “circuit board 39 is disposed in the housing”), said second circuit board being electrically coupled to said planar substrate and to said first circuit board (*e.g.*, “imager device 27 [] electrically connected to the camera circuit board 29” is coupled to “circuit board 39” via a “flexible board 51”), said second circuit board having a length and a width thereto, wherein said length and width of said second circuit board define a third plane (*e.g.*, plane defined by length and width of “circuit board 39” as shown in Fig. 7), said second circuit board including circuitry thereon to convert said pre-video signal to a post-video signal (*e.g.*, “circuit board 39 includes a signal processing circuit ..., a driver circuit ..., a system circuit, a power supply circuit, and so on” and it would have been obvious to include “camera signal processing circuit ... [that] generates a video signal 103 in a television signal format from the opto-electrically converted signal 101” on circuit board 39), said second circuit board being offset from said

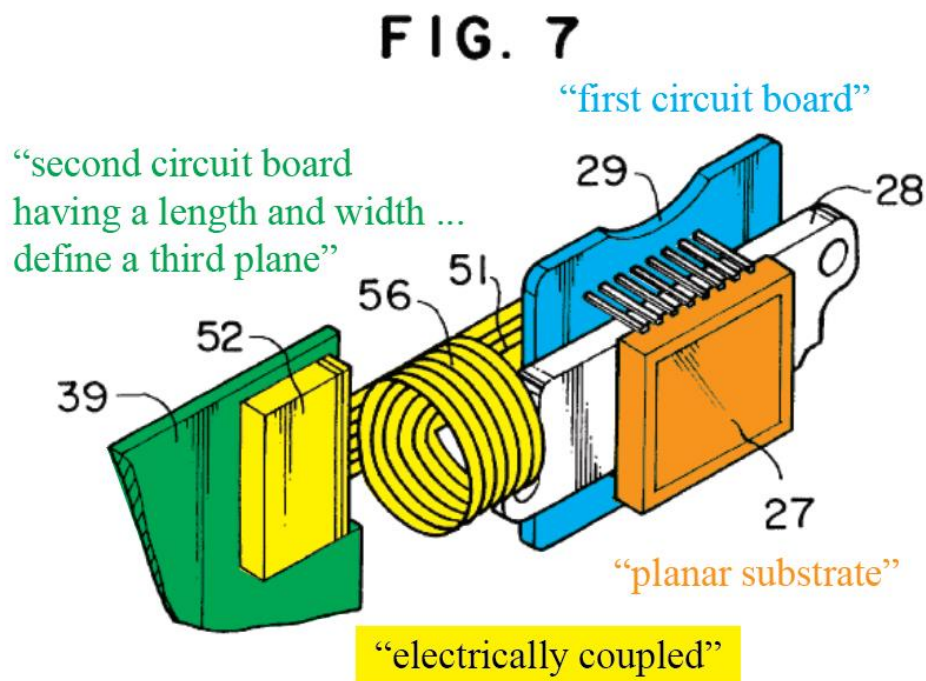
first circuit board and from said planar substrate (*e.g.*, “circuit board 39” is vertically and laterally offset from “circuit board 29” and from “imager device 27” as illustrated in Figs. 3 and 7, respectively), said third plane of said second circuit board being substantially parallel to said second plane of said first circuit board and to said first plane of said planar substrate (*e.g.*, plane defined by length and width of “circuit board 39” parallel with plane defined by length and width of “circuit board 29” and plane defined by length and width of “imager device 27” as shown in Figs. 3 and 7).

206. My analysis of [1.f] with respect to similar language is equally applicable to [3.g]. *See* Section VIII.A.4.g.

207. In addition, as discussed in regards to [1.f], Wakabayashi discloses that “imager device 27 [] electrically connected to the camera circuit board 29” is connected to a “circuit board 39” of the imager apparatus, as shown in Figure 7.

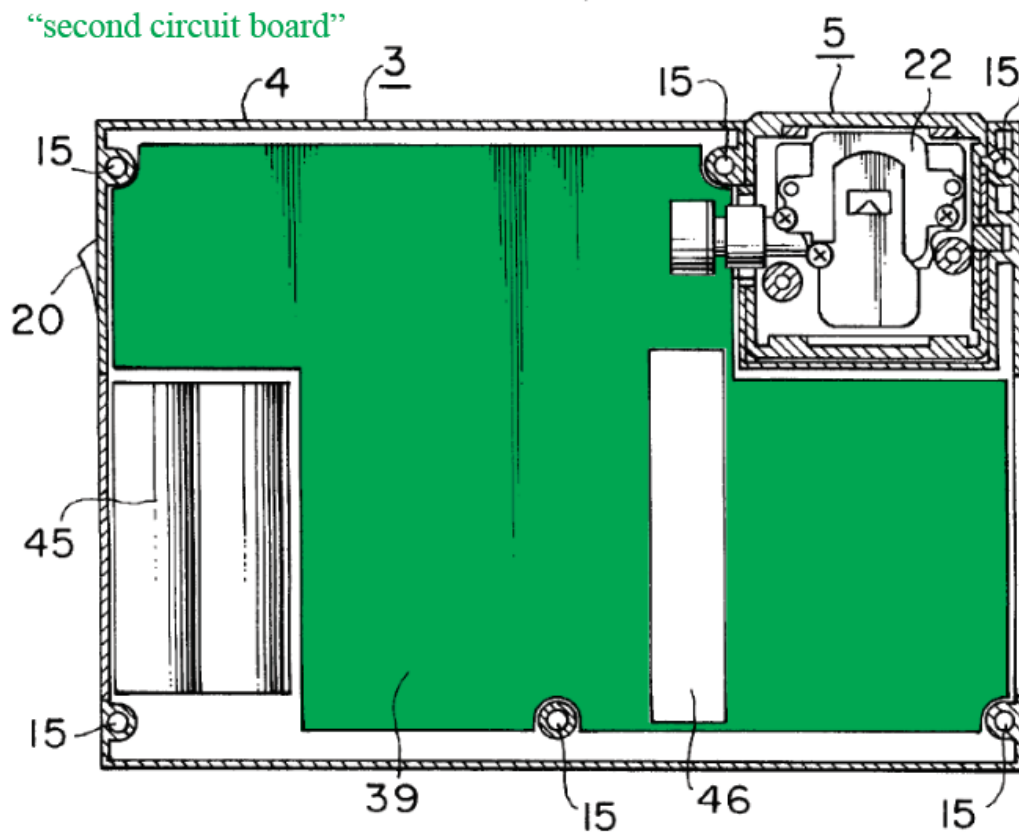
208. As also discussed in [1.f], Wakabayashi discloses that “circuit board 39,” as illustrated in Figure 5, has a length and a width that define a plane. With regards to [3.g], however, the length and width of “circuit board 39” defines a ***third*** plane. Figures 3 and 7 further illustrate that this plane is substantially parallel to the first plane defined by the length and width of “circuit board 29,” and that the “circuit board 39” is offset from “circuit board 29” and “imager device 27.” Specifically, Figure 7 illustrates the perspective view of the components of Wakabayashi’s imager apparatus and Figure 3 illustrates its cross section. From these two figures

Wakabayashi shows that the length and width of the “circuit board 39” defines a plane that is parallel to the plane defined by the length and width of “circuit board 29” and the plane defined by the length and width of “imager device 27.” Additionally, the two figures also show that the “circuit board 39” is not stacked behind “circuit board 29” and “imager device 27,” but rather, “circuit board 39” is arranged in an offset position from “circuit board 29” and “imager device 27.”



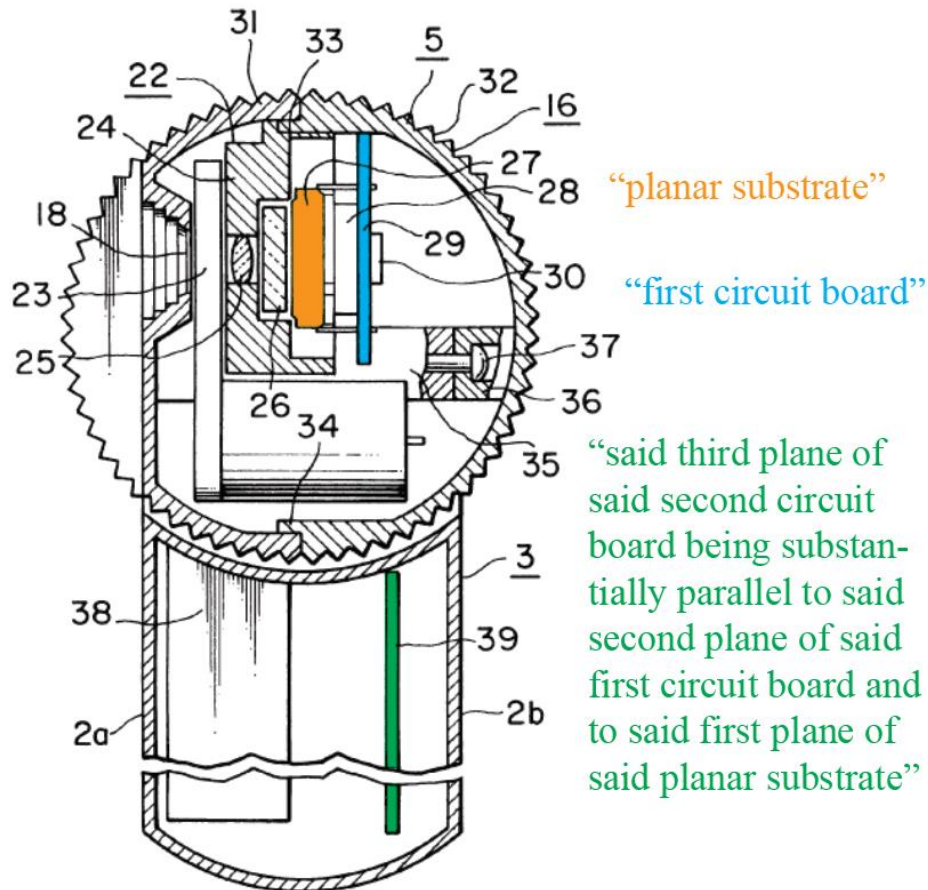
Wakabayashi, Fig. 7 (annotated)

FIG. 5



Wajabayashi, Fig. 7 (annotated)

FIG. 3



Wajabayashi, Fig. 3 (annotated)

209. As discussed in Section VIII.A, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to locate the circuitry that “generates a video signal 103” by converting the pre-video signal to a post-video signal on Wakabayashi’s “circuit board 39” and couple it to the power supply circuit, and would have recognized this combination (yielding the claimed limitation) would work as expected.

i. Element [3.h]

210. **Element [3.h] recites “a lens mounted in said housing, said lens being integral with said imaging device, said lens focusing images on said array of CMOS pixels of said image sensor.”** Wakabayashi in view of Ricquier renders obvious element [3.h]. Wakabayashi discloses a lens mounted in said housing, said lens being integral with said imaging device (*e.g.*, “lens 25” in “lens case 24” “secured to” “the mounting plate 28 ... fixed to the camera case 16” of the “imager apparatus”), said lens focusing images on the image sensor chip (*e.g.*, “image ... is focused on the imager device 27 by the lens 25”).

211. My analysis of [1.g] with respect to similar language is equally applicable to [3.h]. *See* Section VIII.A.4.h.

212. As discussed in Section VIII.C.4, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to apply Ricquier’s known teachings of an array of CMOS pixels in implementing Wakabayashi’s imager apparatus—such that the lens of Wakabayashi’s imager apparatus would focus images on said array of CMOS pixels, and would have recognized this combination (yielding the claimed limitation) would work as expected.

j. Element [3.i]

213. **Element [3.i] recites “a video screen, said video screen being electrically coupled to said second circuit board, said video screen receiving said post-video signal and displaying images from said post-video signal.”**

Wakabayashi discloses element [3.i]. Wakabayashi discloses a video screen (*e.g.*, “liquid crystal panel 38” of “liquid crystal display 6”), said video screen being electrically coupled to said second circuit board (*e.g.*, “liquid crystal panel 38” is coupled to “circuit board 39” in order to display “video signal 103”), said video screen receiving said post-video signal and displaying images from said post-video signal (*e.g.*, “liquid crystal panel 38” displays “video signal 103”).

214. My analysis of [1.h] with respect to similar language is equally applicable to [3.i]. *See* Section VIII.A.4.i.

k. Element [3.j]

215. **Element [3.j] recites “a power supply mounted said housing, said power supply being electrically coupled to said planar substrate to provide power to said array of CMOS pixels, said power supply also being electrically coupled to said first circuit board to provide power to said timing and control circuitry, said power supply also being electrically coupled to said second circuit board to provide power thereto.”** Wakabayashi in view of Ricquier renders obvious element [3.j]. Wakabayashi discloses a power supply mounted in said

housing (*e.g.*, “battery 45 is disposed in ... housing 3”), said power supply being electrically coupled to said first circuit board to provide power to the image sensor (*e.g.*, battery powers “imager device 27 [] electrically connected to [] circuit board 29”), said power supply also being electrically coupled to said second circuit board to provide power thereto (*e.g.*, battery coupled to “circuit board 39” to power “driver circuit” and “power supply circuit”). As discussed above, Ricquier discloses an array of CMOS pixels.

216. My analysis of [1.i] with respect to similar language is equally applicable to [3.j]. *See* Section VIII.A.4.j.

217. As discussed in Section VIII.C.4, it would have been obvious to apply Ricquier’s known teachings of an array of CMOS pixels and of placing a “timing controller” “off-chip” in implementing Wakabayashi’s imager apparatus—such that power is supplied to the pixels and related timing and control circuitry, and would have recognized this combination (yielding the claimed limitation) would work as expected.

I. Element [3.k]

218. **Element [3.k] recites “wherein a largest dimension of said image sensor along said first plane is between 2 and 12 millimeters.”** Wakabayashi in view of Ricquier and Dierickx renders obvious element [3.k]. Wakabayashi discloses the image sensor along said first plane (“imager device 27”). Dierickx

discloses the largest dimension of said image sensor chip is between 2 and 12 millimeters. (*e.g.*, “size of...image sensor...is 6.3x5.7 mm”).

219. As discussed in regards to element [3.b] above, Wakabayashi discloses that the “imager device 27” has a length and width that defines a first plane. *See* Section VIII.C.6.c.

220. My analysis of [1.k] with respect to similar language is equally applicable to [3.k]. *See* Section VIII.A.4.1.

221. Dierickx discloses the size of its image sensor is “6.3x5.7 mm” and, therefore, the largest dimension of said image sensor is between 2 and 12 millimeters. *See, e.g.*, Dierickx ¶32 (“The size of such image sensor with 384x288 pixels is 6.3x5.7 mm....”).

222. As discussed in Section VIII.C.5, a person of ordinary skill in the art would have been motivated to apply Dierickx’s known teachings of an “6.3x5.7 mm” image sensor in implementing Wakabayashi’s imager apparatus (as modified by the teachings of Ricquier) to advantageously provide a small image sensor chip such that the size of the camera head could be reduced.

m. Claim [7]

223. Claim 7 recites “The imaging device of claim 3, wherein: said image sensor has a generally square shape along said first plane.” Wakabayashi in view of Ricquier and Dierickx renders obvious claim 7. Wakabayashi discloses the image

sensor along said first plane (*e.g.*, plane defined by length and width of “imager device 27” as shown in Fig. 7). Dierickx discloses the said image sensor has a generally square shape. (*e.g.*, “image sensor with 384x288 pixels is 6.3x5.7 mm”).

224. My analysis of [1.j] with respect to similar language is equally applicable to claim 7. *See* Section VIII.A.4.k.

225. As discussed in regards to element [3.b] above, Wakabayashi discloses that the “imager device 27” has a length and width that defines a first plane. *See* Section VIII.C.6.c.

226. As discussed in regards to element [3.k] above, Dierickx discloses that the size of the image sensor is “6.3x5.7 mm” and, therefore, generally square shape. To the extent it is argued that an “image sensor with 384x288 pixels” and chip dimensions of “6.3x5.7 mm” is not generally square, however, it would have been obvious to change the number of pixels to “256x256,” as taught by Ricquier, which would have produced a “square 256*256 image[]” sensor chip. *See, e.g.*, Ricquier, 2 (“This square 256*256 imager was fabricated in a standard 1.5 μm CMOS technology.”), 9 (“A dedicated image sensor for time critical industrial applications was presented. It consists of a 256*256 X-Y addressable photodiode array integrated together with a readout structure that allows the addition of charges of different pixels.”). A person of ordinary skill in the art would have understood that since Ricquier’s image sensor’s disclosed dimensions (6.3x5.7 mm) are proportional to

the pixel array (384x288 pixels), that by making the array square (*e.g.*, 256x256 pixels) the chip's dimensions would be square. A person of ordinary skill in the art would also understand that the largest dimension of such a square image sensor chip would still be between 2 and 12 mm.

227. As discussed in Section VIII.C.5, a person of ordinary skill in the art would have been motivated to apply Dierickx's known teachings of small square image sensor in implementing Wakabayashi's imager apparatus (as modified by the teachings of Ricquier) to advantageously provide a small image sensor chip such that the size of the camera head could be reduced.

D. Claim 2 Is Obvious Under §103 over Swift in View of Ricquier and Suzuki (Ground 4)

1. Overview of WO 95/34977 ("Swift") (Ex. 1005)

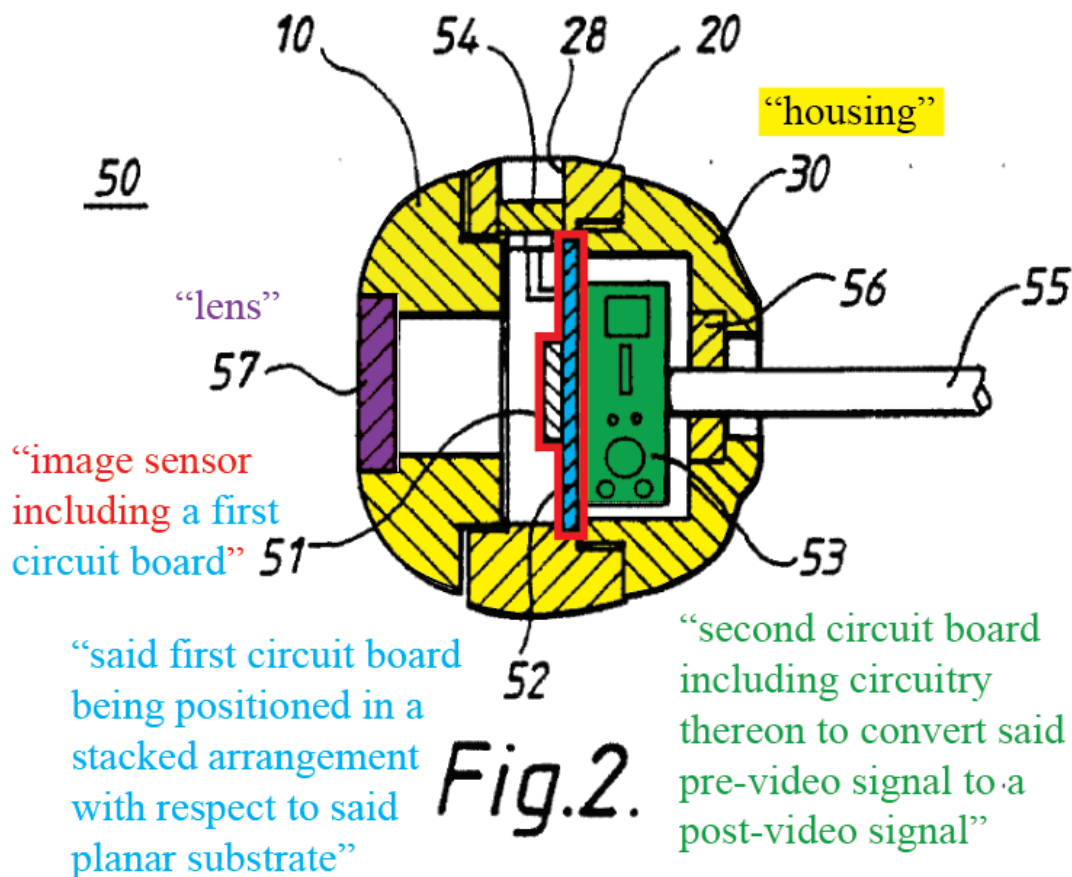
228. Swift (Ex. 1005) was published on December 21, 1995, and I understand, is prior art to the '052 patent.

229. Swift teaches a miniature video camera that includes a housing and an image sensor mounted in the housing. *See, e.g.*, Swift, Abstract, 4:11-15 ("In a camera ... [the] image sensor is preferably a CMOS sensor," "an active pixel sensor."), 8:31-9:5 ("Figure 2 shows the three housing portions 10, 20 and 30 engaged with one another, to make up the housing...."), Fig. 2. As shown in Figure 2 (below), the miniature video camera, includes housing, image sensor 51 mounted on a circular circuit board 52 lying in a first plane, and a rectangular circuit board

53, which includes various circuitry components “to provide power to the image sensor 51,” and “process image signals received therefrom,” including a video processor for converting the pre-video signal generated by the image sensor to a post-video signal. See, e.g., Swift, 8:31-9:13 (“An image sensor 51 is mounted on a circular printed circuit board 52.... A further printed circuit board 53 is mounted on the first printed circuit board 52 ... to provide power to the image sensor 51, [and] process image signals received therefrom...”), 3:31-4:4 (disclosing “an image sensor assembly for a miniature camera, the assembly comprising a printed circuit board and, mounted thereon, the image sensor, a video processor, ... and a voltage regulator to ... provide a substantially constant supply voltage to components on the printed circuit board.”).

230. Swift’s image sensor 51 is a CMOS Active Pixel Sensor (APS) type chip. Swift, 10:1-6. As the ’052 patent recognizes, each pixel of a “CMOS/APS (Active Pixel Sensor)” includes an amplifier. ’052 patent, 1:66-2:1 (“One particular advance in CMOS technology has been in the active pixel-type CMOS imagers which consist of randomly accessible pixels with an amplifier at each pixel site.”), 2:23-25 (“[T]he major difference between passive and active CMOS pixel arrays is that a passive pixel-type imager does not perform signal amplification at each pixel site.”). Swift confirms this, as it provides that “information on APS-type sensor can be found in [Fossum93 (Ex. 1048) at Page 83],” which states that “[i]n the active-

pixel sensor, several active transistors are monolithically integrated in the pixel.... These transistors are used for ... amplifying ... the pixel output signal.” Swift, 10:1-6; Fossum93, 83. Similarly, Dierickx further confirms that “[a]n active pixel is configured with means integrated in the pixel to amplify the charge....” Dierickx, ¶6 (“An active pixel is configured with means integrated in the pixel to amplify the charge that is collected on the light sensitive element.”).



Swift, Fig. 2 (annotated).

231. Swift explains that image sensor 51 and circular circuit board 52 are mounted within the camera's housing by clamping the circular circuit board in position with the housing's rear portion. Swift, 8:33-9:5. Circuit board 53 is electrically connected to both circuit board 52 and image sensor 51, and has circuitry to process the image signals received from image sensor 51 and audio signals from microphone 54 connected to circuit board 52. Swift, 9:7-13.

232. Swift discloses configuring circuit boards 52 and 53 and their associated circuitry in multiple different ways. Swift, 19:8-29. In one example configuration of circuit boards 52 and 53, Swift teaches disposing its components in other orientations. Swift, 18:25-33. Thus, while Swift shows circuit board 53 at a right angle to image sensor 51 in Figure 2, a person of ordinary skill in the art would have understood Swift to also teach circuit board 53 parallel to circuit board 52. Specifically, Swift states that “[i]n this specification, terms of absolute orientation are used conveniently to denote the usual orientation of items in normal use and/or as shown in the accompanying drawings” and “such items could be disposed in other orientations, and in the context of this specification, terms of absolute orientation, such as ‘top’, ‘bottom’, ‘left’, ‘right’, ‘vertical’ or ‘horizontal’, etc. are to be construed accordingly, to include such alternative orientations.” Swift, 18:25-33. Accordingly, while Swift shows circuit board 53 at a right angle to image sensor 51 in Figure 2, a person of ordinary skill in the art would have understood Swift to also

teach circuit board 53 parallel to circuit board 52. Indeed, given that Swift explicitly discloses that rear housing portion 30” can be changed to “accommodate ... [the] different configuration[],” circuit board 53 with the video processing circuitry also fits in housing 30 parallel to board 52. Swift, 10:12-16. A person of ordinary skill in the art would have understood that the orientation of circuit boards is often dictated by the shape and dimensions of the housing. Thus, a more compact housing with less depth would naturally suggest stacking circuit boards parallel to one another. At minimum, a person of ordinary skill in the art would have been motivated to orient the circuit board 53 in this manner to allow the device to be more compact.

233. The configuration of the circuitry and design of the housing are engineering considerations. For example, Swift teaches that “the rear housing portion 30 may be replaced by another portion of different configuration, designed to accommodate additional components or different components of different configuration.” Swift, 10:12-16. As another example, Roustaei similarly teaches that “the number of printed circuit boards is a design choice” and that “all the hardware could be contained on one board or ... whatever quantity [of boards] permits the device's components to be fitted into the dimensions of the intended housing.” Roustaei (Ex. 1030, which was filed 08/1/1996 and issued 5/26/1998, and I understand is prior art to the '052 patent), 43:38-44; *see also, e.g.*, Roustaei, 54:7-

11 (disclosing that “it will be apparent to those skilled in the art that the choice of number of boards depends on many factors such as packaging constraints.”); Cotton (Ex. 1031, which issued 12/16/1986, and I understand is prior art to the ’052 patent), 13:30-35 (“[T]he fact that certain of the I/O devices are included on the CPU board ... and others are included on the video board ... is merely a matter of design choice.”); Crosetto (Ex. 1032, which was published 8/17/94, and I understand is prior art to the ’052 patent), 15:35-46 (“[P]lacement and arrangement of processors and connectors upon the PCB is a matter of design choice.”).

234. Swift also teaches that to power the sensor, Swift’s miniature camera uses a battery and a voltage regulator that provide power to the components on the printed circuit board(s) and the image sensor. *See, e.g.,* Swift, 3:32-4:4 (“image sensor assembly for a miniature camera, the assembly comprising a printed circuit board and, mounted thereon, the image sensor, a video processor, ... and a voltage regulator to accept a plurality of different input voltages and provide a substantially constant supply voltage to components on the printed circuit board”), 4:21-22 (“camera ... may incorporate a battery...”), 9:7-13 (“Various circuitry components are mounted on the circuit board 53, to provide power to the image sensor 51...”). Swift’s battery and voltage regulator provide power to (and thus are electrically coupled to and drive) the “image sensor 51” (including its pixels) and the alternatives of the “single circuit board” and circuit boards 52 and 53. In addition, Swift

discloses the voltage regulator is mounted on an assembly in the camera's housing. And based on Swift's disclosure that "the housing 50" has "sufficient room to house a battery," a person of ordinary skill in the art would have understood that the battery is mounted in the housing.

235. Swift describes a wide angle lens mounted on a front housing portion so that the lens focuses the image onto the image sensor. *See, e.g.,* Swift, Fig. 2 (above), 9:23-28 ("A wide-angle lens 57 is mounted in the front bore 12 of the front housing portion 10.... The lens 57 is so positioned as to focus an image onto the image sensor 51.").

236. Swift also discloses that the "signal ... from the camera" is received by a "display" connected by a "cabling system" "to the camera." *See, e.g.,* Swift, 15:7-14, 17:34-18:2. Thus, image signals received from image sensor 51 are processed and output from the circuit board in a form that can be viewed directly by a display. The "video monitor" is electrically coupled to "circuit board 53" to allow the "process[ed] image signals" to be transmitted to the video monitor. While Swift discloses the "video monitor" as a separate device from the miniature camera, a person of ordinary skill in the art would have found it to be an obvious implementation choice to include the camera and the display within close proximity (*e.g.,* a short cable), such that they are within the same enclosure. For example, a person of ordinary skill in the art would have been motivated to mount the camera

through a wall or door, for example, with a display on the other side of the wall/door to advantageously view the video of the other side for surveillance or security purposes.

2. Motivation to Combine Swift and Ricquier

237. As discussed in Section VIII.C.2 above, Ricquier describes a dedicated imager for a camera programmed to operate in several resolutions, with a CMOS pixel array and a timing controller implemented on an off-chip driving unit. *See* Section VIII.C.2.

238. While Swift does not expressly state that its CMOS active pixels are in an array, Ricquier provides this additional implementation detail of a “256*256 X-Y addressable photodiode array ... realised in a 1.5 µm standard CMOS technology.” *See, e.g.,* Ricquier, 9. Similarly, while Swift does not expressly disclose how the timing of its pixels is controlled other than referring to sensor “selection and readout” circuitry, Ricquier discloses that the readout from the “256*256 imager” is driven by a “timing controller (realised in an off-chip driving unit),” by “transferring ... charges of different pixels” “to a single output amplifier.” *See, e.g.,* Ricquier, 2-4, 9. Ricquier also teaches that its timing controller is “off-chip” from the array of pixels. *See, e.g.,* Ricquier, 3, 4.

239. A person of ordinary skill in the art would have been motivated to apply Ricquier’s known teachings described above in implementing Swift’s CMOS image

sensor. Like Swift, Ricquier is in the same field of art and is analogous art to the '052 patent—all are in the same field related to solid-state image sensors for use in cameras. *See, e.g.*, Ricquier, 2-3, 5, 9. In addition, like Swift, Ricquier is also reasonably pertinent to the alleged problem(s) identified in the '052 patent of arranging the circuitry of a CMOS image sensor, including to minimize the device's size or profile area, and to reduce image noise in CMOS sensors. *See, e.g.*, Ricquier, 2-3, 8 (noise reduction). A person of ordinary skill in the art would have been further motivated to apply Ricquier's known teachings in implementing Swift's image sensors because of Ricquier's advantages of using an "timing controller" that can be located off-chip, which adds flexibility in selecting from the several design choices for "fitting ... the components into the available space" and "plac[ing]" circuitry on "various layers" arranged "stackwise" to "allow for a more compact camera head." Ricquier, 3, 4. Specifically, a person of ordinary skill in the art would have been motivated to apply Ricquier's teachings of an off-chip timing and control circuitry in implementing Swift's image sensor by locating the timing and control circuitry on, for example, on the opposite side of Swift's "circuit board 52" to "image sensor 51" in order to minimize the camera's overall size. *See, e.g.*, Tanuma, 4-5 (benefits of mounting image sensor chip on one side of a circuit board and other circuit components on the circuit board's underside include that it "does not require many lead wires, so there is a high degree of reliability, and excellent matching

characteristics...[and] allow[s] for a more compact camera head”); Suzuki, Fig. 2 (mounting circuitry on the opposite side of chip-connecting board 226 from image pickup chip 221). Furthermore, it was well-known in the art that “fitting of the components into the available space” and “placement” of circuitry on “various layers” arranged “stackwise,” is a common design consideration for portable devices. PCB Design, 15, 20. In addition, a person of ordinary skill in the art would have been further motivated to apply Ricquier’s known teachings in implementing Swift’s CMOS solid-state imager because of Ricquier’s express advantages of “selective addressability” and “multiple resolutions ... [and] data rates upto 10 MHz.” *See, e.g., Ricquier, 2.*

240. In light of the above, a person of ordinary skill in the art would have found it routine, straightforward and advantageous to apply Ricquier’s teachings of arranging CMOS pixels in an array and an off-chip timing controller in implementing Swift’s image sensor, and would have known that such a combination (yielding the claimed limitations) would predictably work and provide the expected functionality.

3. Motivation to Combine Swift, Ricquier, and Suzuki

241. As discussed in Section VIII.B above, Suzuki discloses a camera head for a solid-state image pickup device and expressly discloses configuring an image

sensor and multiple circuit boards such that they are parallel and longitudinally aligned. *See* Section VIII.B.

242. A person of ordinary skill in the art would have been motivated to apply Suzuki's known teachings of an image sensor comprising a first circuit board lying in a first plane and second circuit board lying in a second plane parallel to the first, such that the first and second circuit boards are in a stacked arrangement with one another, in implementing Swift's teachings of a miniature camera (as modified by Ricquier's teachings) where Swift's circuit board 53 is oriented parallel to circuit board 52 to reduce the camera's overall size and to improve the camera device's "stability and reliability." *See, e.g.,* Suzuki, 1:53-56, 3:61-4:12, 4:30-65.

243. As discussed above, while Swift describes "circuit board 53" as being "substantially at right angles" to "circuit board 52," Swift also explains its "specification...denote[s] the usual orientation of items in normal use and/or as shown in the accompanying drawing" and that "such items could be disposed in other orientations." Swift, 18:25-33. Swift further acknowledges that the "rear housing portion 30 may be replaced by another portion of different configuration ... to accommodate ... components of different configurations." Swift, 10:12-16. By arranging the image sensor and circuit boards so that they are "aligned with each other" as illustrated in Figure 2, Suzuki explains that its camera head "has an outer diameter closer to a diagonal length of a solid-state image pickup chip" which,

Suzuki demonstrates, is “10 mm, ... small [by] about 5 mm than that of the conventional camera head.” Suzuki, 1:53-56 (“It is an object of this invention to provide a camera head for a solid-state image pickup device which camera head has an outer diameter closer to a diagonal length of a solid-state image pickup chip.”), 3:15-19, 4:6-11 (“[I]n the case where the solid-state image pickup chip of 1/3 inch (8.5 mm) is used, the outer diameter of the camera head is about 10 mm...”). By applying the above teaching of Suzuki in implementing Swift’s teachings of a miniature camera (as modified by Ricquier’s teachings) the camera’s overall size would be reduced, furthering Swift’s express objective of make the “camera ... as small as possible, so that it may be located discretely in such a way that it is not readily observed.” Swift, 1:10-13.

244. A person of ordinary skill in the art would have been motivated to apply Suzuki’s known teachings of an image sensor comprising a “chip-connecting board 226” between 8.5 and 10 mm in implementing Swift’s teachings of a miniature camera (as modified by Ricquier’s teachings) such that the miniature camera’s overall size is reduced thus improving the camera device’s “stability and reliability.” *See, e.g.*, Suzuki, 1:53-56, 3:1-49, 3:61-4:12, 4:30-65. Suzuki explains that its arrangement of image sensor and circuit boards allows “not only the solid-state image pickup chip but also the boards, including the electric circuits parts, [to] be

sealed, and therefore ... advantageously enhance[]” “the stability and reliability of the circuit.” *See, e.g.*, Suzuki, 4:30-45; 3:61-4:6.

245. A person of ordinary skill in the art also would have been motivated apply Suzuki’s known teaching in implementing Swift’s imager apparatus because, as Suzuki expressly discloses, this arrangement of its image sensor and circuit board allows for the “camera head [to have] an outer diameter closer to a diagonal length of a solid-state image pickup chip” (*see, e.g.*, Suzuki, 1:53-56, 4:6-11, 4:58-65)—thus furthering Swift’s objective of making the “camera ... as small as possible” (*see, e.g.*, Swift, 1:10-18, 9:30-33). While Suzuki uses a generic “solid-state image pickup chip of ... 8.5 mm,” Suzuki’s teachings are applicable to CMOS image sensor chips of similar diagonal lengths, well known at the time. *E.g.*, Dierickx, ¶32 (disclosing CMOS image sensor chip with 8.5-mm diagonal length); Mendis, 21 (disclosing CMOS image sensor with 9.6-mm diagonal length); Dickinson, 222 (disclosing CMOS image sensor with 6.7-mm diagonal length).

246. In light of the above, a person of ordinary skill in the art would have found it routine, straightforward and advantageous to apply Suzuki’s known teachings of arranging an 8.5-mm image pickup chip, a chip-connecting board, and a second circuit board, in parallel planes and in a stacked configuration to fit within a 10-mm diameter casing, in implementing Swift’s teachings of an miniature camera (as modified by Ricquier’s teachings), and would have known that such a

combination (yielding the claimed limitations) would predictably work and provide the expected functionality.

4. Invalidity of Claim 2 over Swift in View of Ricquier and Suzuki (Ground 4)

a. Element [2.pre]

247. **Element [2.pre]** recites “An imaging device comprising.” To the extent the preamble is limiting, Swift discloses an imaging device (e.g., “miniature camera” and “video monitor ... to display a signal received from the camera”).

248. Swift discloses “miniature cameras” for various applications, including surveillance and security systems. For example, Swift discloses that it is “concerned particularly, although not exclusively, with miniature cameras” where a “video monitor or TV 154 is provided, to display a signal received from the camera 152.” *See, e.g.,* Swift, 1:2-5, 15:7-9. Swift also explains that these “[m]iniature cameras are finding increasing application in surveillance and security systems, and also in automated inspection apparatus, and for incorporation in other devices.”) *See, e.g.,* Swift, 1:7-10.

249. To the extent the claimed “imaging device” requires Swift’s “video monitor” to be within the same physical housing as its “camera”—as opposed to the two components connected via a cable as disclosed in Swift, as discussed in Section VIII.D.1, a person of ordinary skill in the art would have found it to be an obvious implementation choice to include the camera and the display within close proximity

(*e.g.*, a short cable), such that they are within the same enclosure. For example, Swift explains that the “[m]iniature cameras are finding increasing application in incorporation in other devices.” *See, e.g.*, Swift, 1:7-10.

b. Element [2.a]

250. **Element [2.a] recites “a housing.”** Swift discloses element [2.a]. Swift discloses a housing (*e.g.*, “housing”).

251. Swift discloses that the “miniature camera” has a “housing” comprised of “three housing portions ... engaged with one another.” For example, Swift explains that the “camera 60 comprises a housing 61,” as illustrated in Figures 2 and 3, is formed using “three housing portions 10, 20 and 30” having a “circular cross-section” and “engage with one another.” *See, e.g.*, Swift, 8:31-33, 10:26-29. Specifically, the “central housing portion 20” is threaded to so that the “front and rear housing portions 10 and 30” can be screwed in to form the housing. *See, e.g.*, Swift, 8:15-16.

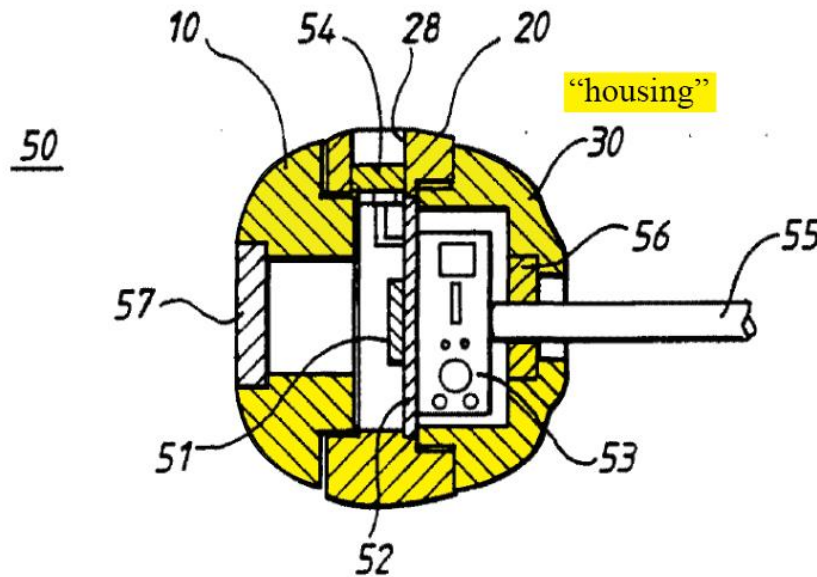


Fig.2.

Swift, Fig. 2 (annotated); *see also, e.g.*, Swift, Figs. 1a-1c (separately illustrating the front, central, and rear housing portions), Fig. 3 (illustrating the exterior of housing 61).

c. Element [2.b]

252. **Element [2.b] recites “an image sensor mounted in said housing, said image sensor including a first circuit board having a length and a width thereto, wherein said length and width of said first circuit board define a first plane, said first circuit board including an array of CMOS pixels thereon.”**

Swift in view of Ricquier renders obvious element [2.b]. Swift discloses an image sensor (*e.g.*, “image sensor 51,” “a CMOS sensor” “mounted on a circular printed circuit board 52”) mounted in said housing (*e.g.*, “mounted ... in the central housing

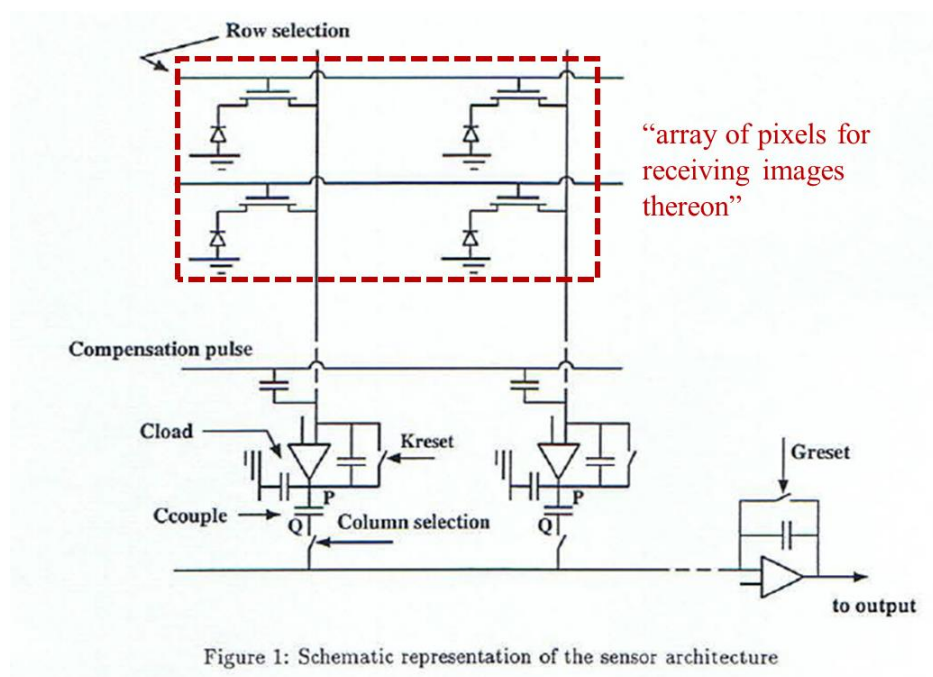
portion 20”), said image sensor including a first circuit board (*e.g.*, “circular printed circuit board 52”) having a length and a width thereto, wherein said length and width of said first circuit board define a first plane (*e.g.*, as shown in Figure 2 and Figure 7), said first circuit board including [image sensor 51] thereon (*e.g.*, “image sensor 51,” “a CMOS sensor” “mounted on a circular printed circuit board 52”). Ricquier discloses an array of CMOS pixels (*e.g.*, “pixel array ... realized in ... CMOS technology”), said array of said CMOS pixels for receiving images thereon (*e.g.*, “[t]o realise the acquisition of image data” “images are formed on the sensor plane”).

253. Swift discloses the miniature camera includes an “image sensor 51 [] mounted on a circular printed circuit board 52,” mounted in the miniature camera’s “housing.” *See, e.g.*, Swift, 8:33-9:5. Swift explains that the image sensor, comprising the “image sensor 51” and “printed circuit board 52,” is “clamped in position” within the “axial extent [] of the intermediate bore” of the “centre housing” when the “rear housing portion 30 ... enterengages with the centre housing portion” and “bares against” the outer diameter of the “circuit board 52.” *See, e.g.*, Swift, 8:31-9:5, Fig. 2. Because Swift’s circuit board 52 is “circular,” it has a length and a width equal to the board’s diameter. *See, e.g.*, Swift, 8:31-9:5, Fig. 2.

254. Swift’s CMOS image sensor 51 is a CMOS Active Pixel Sensor (APS) type chip. *See, e.g.*, Swift, 10:1-6 (“The image sensor 51 is preferably of a CMOS/APS (Active Pixel Sensor) type. An APS acts similarly to a random access

memory (RAM) device, wherein each pixel contains its own selection and readout transistors. Further information on APS-type sensors may be found in the publication “Laser Focus World”, June 1993, Page 83.”), 4:11-13 (“[S]aid image sensor is preferably a CMOS sensor”).

255. While Swift does not expressly state that its CMOS active pixels for receiving images thereon are in an array, Ricquier provides this additional implementation detail of the “acquisition of image data” in an “image sensor” using a “256*256 X-Y addressable photodiode array ... realised in a 1.5 μm standard CMOS technology.” See, e.g., Ricquier, 2-3, 9. Specifically, Figure 1 of Ricquier illustrates a portion of the “pixel array [that] consists of 256 by 256 square pixels arranged on a pixel pitch of 19 μm and realised in a 1.5 μm n-well CMOS technology”:



Ricquier, 5, Figure 1 (annotated). Ricquier explains that “an X-Y addressable architecture was selected” in order to “realise the acquisition of image data” and that “images are formed on the sensor plane.” *See, e.g.*, Ricquier, 3, 6.

256. As discussed in Section VIII.D.2, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to apply Ricquier’s known teachings of arranging pixels in an array in implementing Swift image sensor 51 of a CMOS/APS type such that the active pixels in Swift’s image sensor are arranged in an array, and would have recognized this combination (yielding the claimed limitation) would work as expected.

d. Element [2.c]

257. **Element [2.c] recites “wherein a plurality of CMOS pixels within said array of CMOS pixels each include an amplifier.”** Swift discloses element [2.c]. Swift discloses a plurality of CMOS pixels each include an amplifier (*e.g.*, amplifier for each “active pixel” of the “CMOS/APS (Active Pixel Sensor)”).

258. Swift discloses that the preferable image sensor for “image sensor 51” is a “CMOS/APS (Active Pixel Sensor) type” such as those “found in the publication ‘Laser Focus World’, June 1993, Page 83” (Fossum93). As discussed in Section VIII.D.1, each active pixel in a CMOS active pixel sensor includes an amplifier. Indeed, the inclusion of an amplifier in each pixel is what distinguishes an “active pixel sensor” from an “passive pixel sensor.” *See, e.g.*, ’052 patent, 1:66-2:1, 2:23-

25 (“[T]he major difference between passive and active CMOS pixel arrays is that a passive pixel-type imager does not perform signal amplification at each pixel site.”); Dierickx, ¶6 (“An active pixel is configured with means integrated in the pixel to amplify the charge that is collected on the light sensitive element. Passive pixels do not have said means and require a charge-sensitive amplifier that is not integrated in the pixel and is connected with a long line towards the pixel.”). Swift further confirms that each of its pixels includes an amplifier by referring to Fossum93 for “[f]urther information on APS-type sensors” which states that “[i]n the active-pixel sensor, several active transistors are monolithically integrated in the pixel.... These transistors are used for ... amplifying ... the pixel output signal.” Swift, 10:1-6; Fossum93, 83.

e. Element [2.d]

259. **Element [2.d] recites “said first circuit board further including timing and control circuitry thereon, said timing and control circuitry being coupled to said array of CMOS pixels.”** Swift in view of Ricquier renders obvious element [2.d]. Swift discloses said first circuit board (e.g., “circuit board 52”). Ricquier discloses circuitry (e.g., “off-chip driving unit”) including timing and control circuitry thereon (e.g., “timing controller” to “drive ... row selection and column selection signal[s]” of “X-Y addressable photodiode array”), said timing and control circuitry being coupled to said array of CMOS pixels (e.g., “timing controller”

“controlling the sequence of addresses and reset pulses of” “photodiode array” as illustrated in Figure 1).

260. As discussed with respect to [2.b], Swift discloses said first circuit board. *See* Section VIII.D.4.c.

261. While Swift discloses that it’s “image sensor 51” is preferably a “CMOS ... Active Pixel Sensor” (Swift, 10:1-6), Swift does not expressly disclose the how timing of its “image sensor 51” is controlled other than referring to sensor “selection and readout” circuitry. Ricquier expressly provides this additional implementation detail and discloses that a “timing controller” generates the “X-Y addresses and control pulses” and uses “decoders [to] drive ... row selection and column selection signal” from the “X-Y addressable photodiode array.” *See, e.g.,* Ricquier, 2 (“By controlling the sequence of addresses and reset pulses of the amplifiers, charges of different pixels are accumulated. This way multiple resolutions can be programmed....”), 3 (“The readout of the charge packets that are accumulated during the integration time, proceeds as follows. After selecting one particular row of pixels, these charges are converted simultaneously to a voltage at the output of the different charge sensitive amplifiers located at the end of the column readout lines. ... Based on the column selection signals these nodes Q are again discharged to their starting value, at the same time creating a voltage variation at the output amplifier proportional to the charges at that column. Every column

selection is followed by a reset pulse on the Greset switch bringing back the output amplifier into its initial state. After that, another charge packet can be received. *After reading out a particular row of pixels, the Kreset switch is closed* causing the integration capacitor to discharge.”), 4, 9.

262. Ricquier further discloses that this “timing controller,” while electrically coupled to the photodiode array to provide the selection signals, is “off-chip.” See, e.g., Ricquier, 3 (“Based on *X-Y addresses and control pulses generated by an external driving unit, two decoders drive one particular row selection and column selection signal.*”), 4 (“In order to limit the complexity of *the timing controller (realised in an off-chip driving unit)* only timing configurations of some very common patterns are provided: apart from the normal resolution (1*1) also the addition of pixel charges in 2*2, 4*4 and 8*8 neighbourhoods was foreseen.”). Figure 1 of Ricquier, illustrates the selection and reset signals from the “off-chip” “timing controller” to read out the image data from the pixel array:

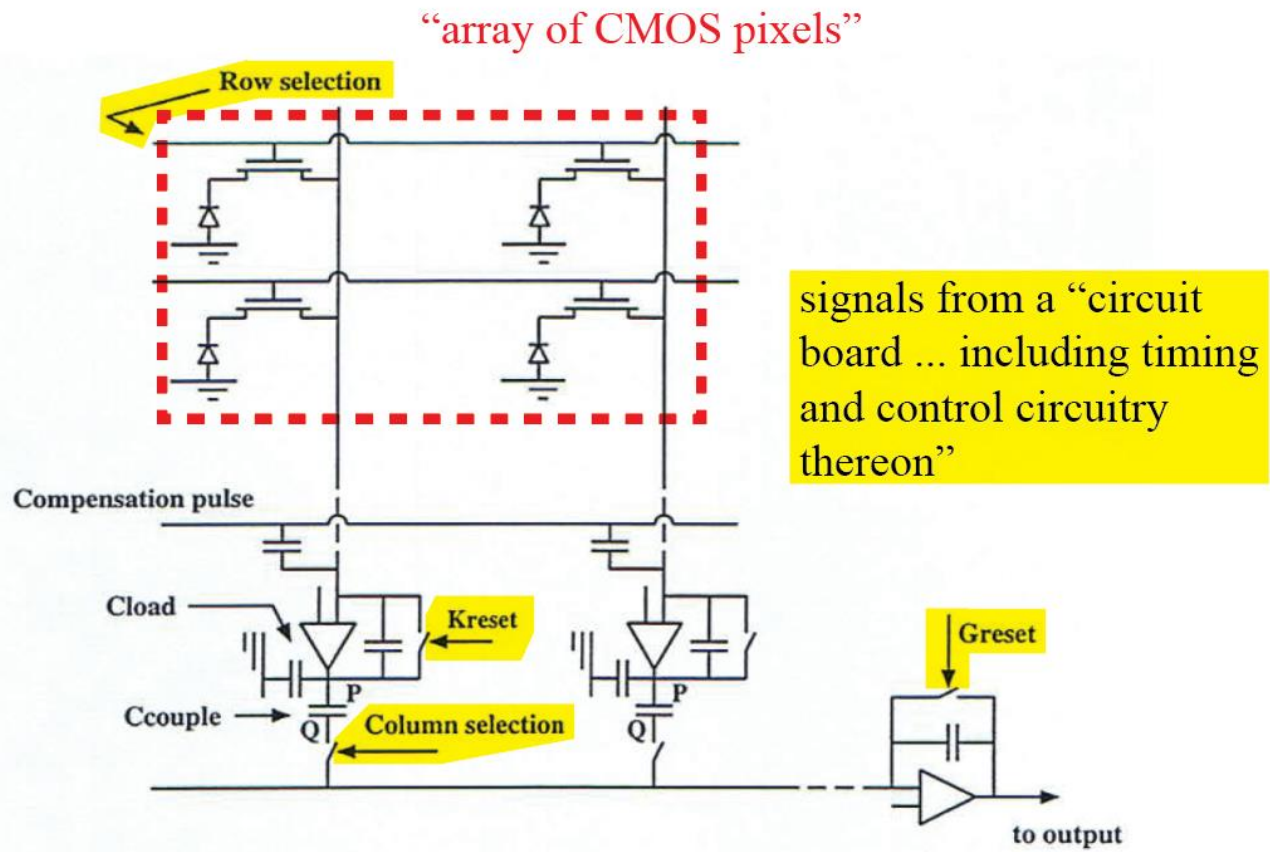


Figure 1: Schematic representation of the sensor architecture

Ricquier, Figure 1 (annotated).

263. As discussed in Section VIII.D.2, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to apply Ricquier's known teachings of an imager including an "off-chip" "timing controller" in implementing Swift's "image sensor 51 [] mounted on a circular printed circuit board 52," for example, such that the timing and control circuitry is mounted on the other side of circuit board 52 relative to the image sensor 51 in order to make the camera more compact.

f. Element [2.e]

264. **Element [2.e]** recites “said image sensor producing a pre-video signal.” Ricquier discloses element [2.e]. Ricquier discloses said image sensor producing a pre-video signal (*e.g.*, “image data” “output,” as shown in Figure 1).

265. While Swift does not expressly disclose the image sensor outputs a pre-video signal, Ricquier discloses that the readout from the “256*256 imager” is “output” from the array. Ricquier, Fig. 1, Abstract (“...[R]eadout occurs in two phases. After transferring in parallel a row of charges to 256 charge sensitive amplifiers, these signals are coupled to a single output amplifier...”), 4. A person of ordinary skill in the art would have understood Ricquier’s “output” as shown in Figure 1 is a pre-video signal produced by Ricquier’s image sensor.

266. While Swift discloses communicating an “image signal” from its image sensor to its image processor (*see, e.g.*, Swift, 9:5-18, Fig. 2), Ricquier describes how the active pixel imaging system produces an output signal, which is a pre-video signal. For example, Ricquier teaches that the array is arranged into rows and columns. *See* Ackland, 7:59-8:9 (“The array 5 includes a series of columns 30 and rows 25 of closely spaced active pixels 35”). As illustrated in Ricquier’s Figure 1 (below), the “image data,” in the form of “charge packets ... accumulated during the integration time” at each of the pixels, is “readout” from the columns and rows of the pixel array and “converted ... to a voltage at the output.” *See, e.g.*, Ricquier, 2

(“...[R]eadout occurs in two phases. After transferring in parallel a row of charges to 256 charge sensitive amplifiers, these signals are coupled to a single output amplifier...”), 3 (“To realise the acquisition of image data only in specific regions of interest, an X-Y addressable architecture was selected.” “[R]eadout of the charge packets that are accumulated during the integration time, proceeds as follows. After selecting one particular row of pixels, these charges are converted simultaneously to a voltage at the output of the different charge sensitive amplifiers located at the end of the column readout lines.”). A person of ordinary skill in the art would have understood Ricquier’s “output” as shown in Figure 1 is a pre-video signal produced by Ricquier’s image sensor:

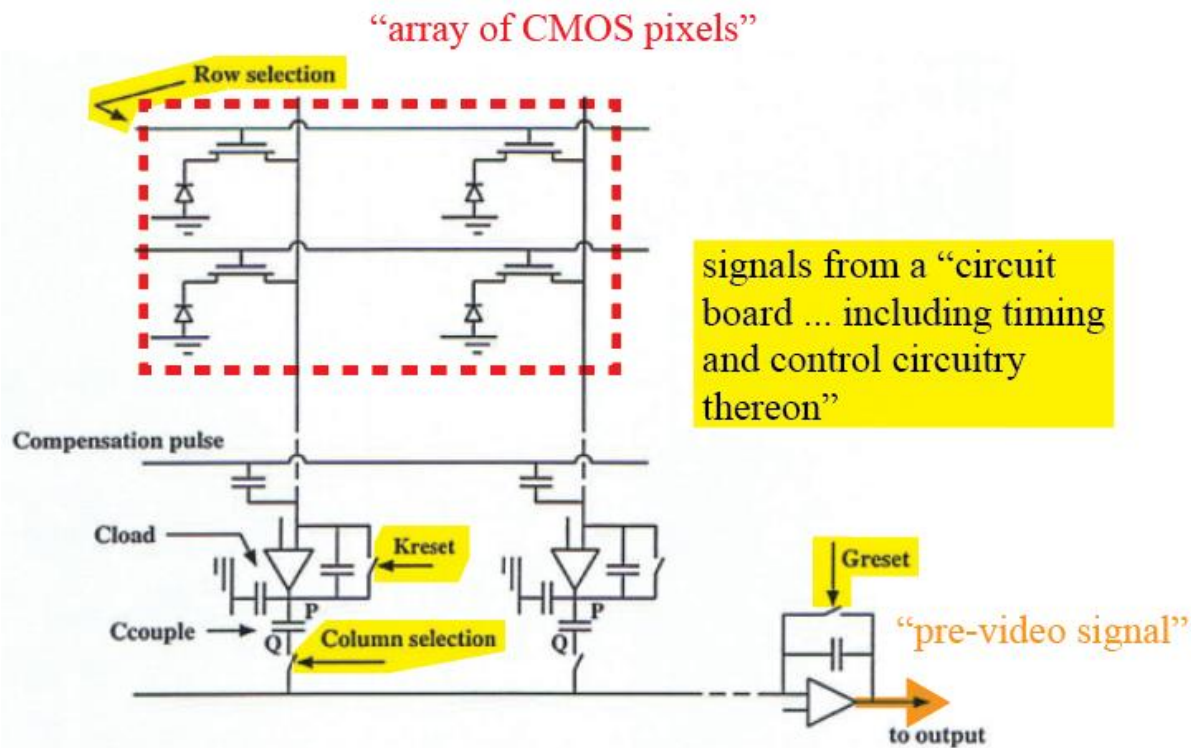


Figure 1: Schematic representation of the sensor architecture

Ricquier, Fig. 1 (annotated).

267. As discussed in Section VIII.A.3, a person of ordinary skill in the art would have been motivated and found it obvious and straightforward to apply Ricquier's known teachings of an "image sensor producing a pre-video signal" in implementing Swift's "image signals" from the "image sensor 51," and would have recognized this combination (yielding the claimed limitation) would work as expected.

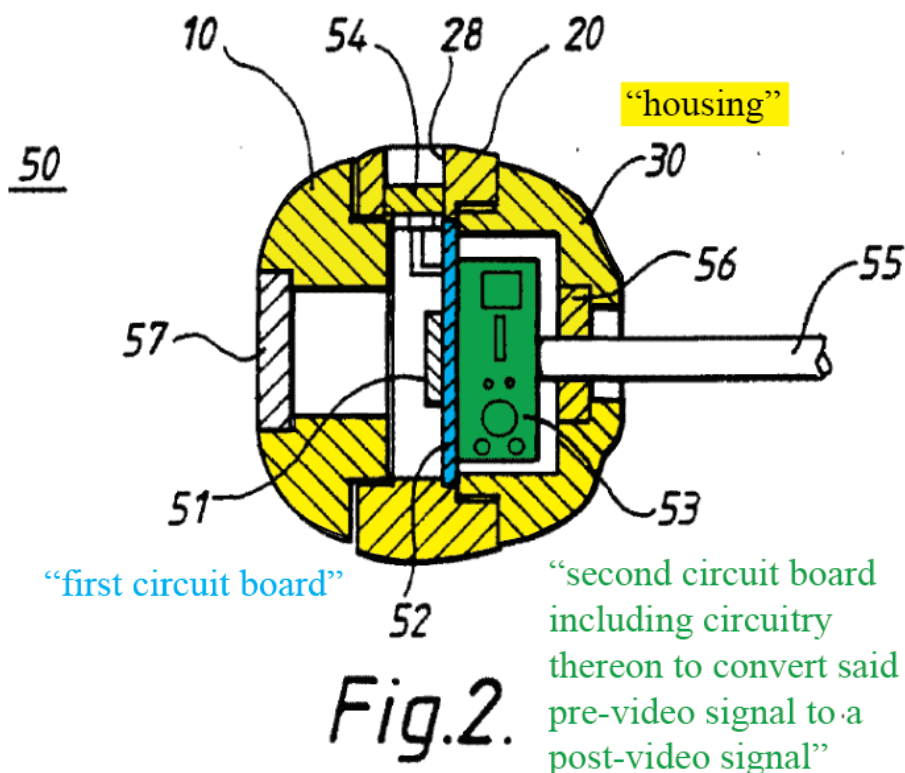
g. Element [2.f]

268. **Element [2.f] recites "a second circuit board mounted in said housing, said second circuit board being electrically coupled to said first circuit board, said second circuit board having a length and a width thereto, wherein said length and width of said second circuit board define a second plane, said second circuit board including circuitry thereon to convert said pre-video signal to a post-video signal, said second circuit board being positioned in a stacked arrangement with respect to said first circuit board, said second plane of said second circuit board being substantially parallel to said first plane of said first circuit board."** Swift discloses, and Swift in view of Suzuki renders obvious element [2.f]. Swift discloses a second circuit board (*e.g.*, "printed circuit board 53") mounted in said housing (*e.g.*, "printed circuit board 53" mounted in "rear housing portion 30" as shown in Figure 2), said second circuit board being electrically

coupled to said first circuit board (*e.g.*, “circuit board 53” connected to “circuit board 52” “to ... process image signals received” from “image sensor 51...mounted on...circuit board 52”), said second circuit board having a length and a width thereto, wherein said length and width of said second circuit board define a second plane (*e.g.*, length and width of “circuit board 53” define a second plane), said second circuit board including circuitry thereon to convert said pre-video signal to a post-video signal (*e.g.*, “video processor”; “circuitry components are mounted on the circuit board 53, to ... process image signals received [from image sensor 51]” into a “video signal” for a “video monitor or TV 154” to “display”), said second circuit board being positioned in a stacked arrangement with respect to said first circuit board (*e.g.*, “board 53” rotated parallel to and in a stacked arrangement with respect to “board 52”), said second plane of said second circuit board being substantially parallel to said first plane of said first circuit board (*e.g.*, plane of “board 53” being substantially parallel to plane of “board 52”). To the extent further disclosure of the arrangement of the circuit boards is required, Suzuki discloses a circuit board positioned in a stacked arrangement with respect to another circuit board attached to an image sensor chip, where the planes defined by the lengths and widths of the circuit boards are substantially parallel to one another (*e.g.*, “circuit board 227” and “chip connecting board 226” “bonded” to “solid-state image pickup chip” “are aligned with each other” as shown in Figures 2, 3C), wherein the planes defined by

the lengths and widths of the circuits boards are substantially parallel (e.g., as shown in Figures 2, 3C).

269. Swift discloses the “circuit board 53” is electrically connected to and receives the “image signals” (pre-video signal) from “image sensor 51” and includes a “video processor” and “circuitry components” that convert the received signal into a signal that may be received by a monitor or television. Figure 2 of Swift shows that “printed circuit board 53” is mounted within the housing, but on the opposite side of “circuit board 52” as “image sensor 51”:



Swift, Fig. 2 (annotated). Swift explains that mounted on “circuit board 53” are “various circuitry components” that “provide power to” and “process image signals

received” from the “image sensor 51” via circuit board 52. *See, e.g., Swift, 9:5-13.* Additionally, Swift discloses that circuitry mounted on “circuit board 53” “process[es] audio signals from a miniature microphone 54 which is mounted within the radially extending passage 28 and connected to the printed circuit board 52.” *See, e.g., Swift, 9:5-13.* Swift explains that the “circuit board 53” has a “video processor” that converts the “image signals received” from the image sensor to “video ... signals” to be “distribute[d] ... to the [] TV” or “video monitor” that “display[s]” the signal “from the camera.” *See, e.g., Swift, 3:31-4:4* (“[T]here is provided an image sensor ... comprising a printed circuit board and, mounted thereon, the image sensor, a video processor, an audio processor, and a voltage regulator...”), 15:7-8 (“A video monitor or TV 154 is provided, to display a signal received from the camera 152.”), 15:13-14 (“The camera 152 and monitor 154 are connected by means of a cabling system 160.”) 17:34-18:3 (“The monitor 154 may comprise a domestic television set. With the video signals provided from the camera 152 as either video or UHF signals, viewing of an image from the camera 152 may be selected on the television at will, and need not interrupt normal television viewing.”), 18:8-11 (“Any of the cameras mentioned above may be connected to such a terminal box, in order to distribute the video signals from the camera(s) to the or each TV in the dwelling.”).

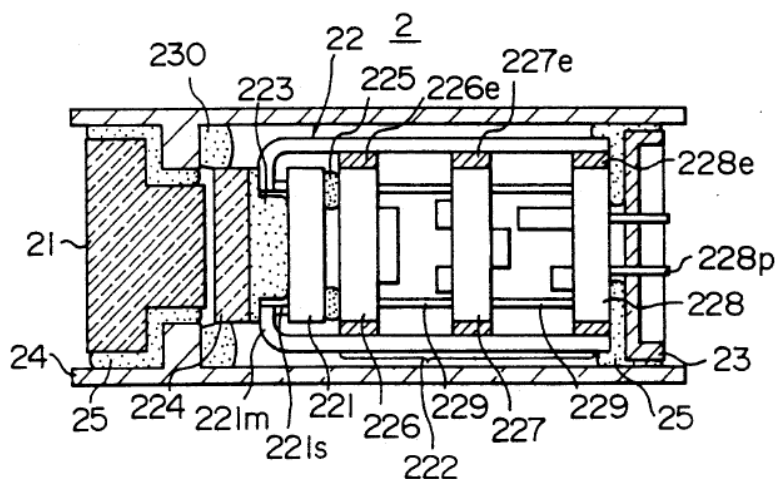
270. Swift discloses configuring circuit boards 52 and 53 and their associated circuitry in multiple different ways, at least one of which meets the

limitation. For instance, while Swift shows circuit board 53 at a right angle to image sensor (51) in Figure 2, Swift teaches disposing its components in various orientations. Swift, 18:25-33 (“In this specification, terms of absolute orientation are used conveniently to denote the usual orientation of items in normal use and/or as shown in the accompanying drawings. However, such items could be disposed in other orientations, and in the context of this specification, terms of absolute orientation, such as ‘top’, ‘bottom’, ‘left’, ‘right’, ‘vertical’ or ‘horizontal’, etc. are to be construed accordingly, to include such alternative orientations.”). Indeed, given that Swift explicitly discloses that “rear housing portion 30” can be changed to “accommodate ... [the] different configuration[,]” circuit board 53 with the video processing circuitry also fits in housing 30 parallel to board 52. Swift, 10:12-16; *see also, e.g.*, 19:8-29 (“Each feature disclosed in this specification (including any accompanying claims, abstract and drawings), may be replaced by alternative features serving the same, equivalent or similar purpose, unless expressly stated otherwise. Thus, unless expressly stated otherwise, each feature disclosed is one example only of a generic series of equivalent or similar features.”). Therefore, a person of ordinary skill in the art would have understood Swift to also teach circuit board 53 parallel to circuit board 52, such that circuit board 53 is positioned in a stacked arrangement with respect to circuit board 52 and the plane defined by circuit board 53 is parallel to the plane defined by circuit board 52. And, at minimum, a

person of ordinary skill in the art would have been motivated to orient the circuit board 53 in this manner as discussed in Section VIII.D.1.

271. While Swift discloses that “printed circuit board 53 is mounted on the first printed circuit board 52, substantially at right angles thereto,” Suzuki teaches arranging “the boards” such that they are “aligned with each other.” Specifically, “circuit board 227” is positioned such that its “electrodes [227e] ... are disposed in registry” with the “electrodes 226e” of the “chip-connecting board 226.” Suzuki, 3:15-19. Suzuki’s Figure 2 shows that the circuit boards are in a stacked configuration and are in parallel planes:

FIG. 2



Suzuki, Fig. 2; *see also, e.g.*, Suzuki, Fig. 3C.

272. Suzuki discloses that “the image pickup unit 22 comprises a solid-state image pickup chip (solid-state image pickup semiconductor device) 221, and a circuit module 222,” where “circuit module 222 comprises a chip-connecting board

226, a circuit board 227 including a circuit for driving the solid-state image pickup chip 221 and a circuit for amplifying the video signal from the solid state image pickup chip 221, and a connector board 228.” Suzuki, 2:38-55; *see also, e.g.,* Suzuki 1:57-2:5 (“[A] camera head for a solid-state image pickup device comprising a chassis which has opposite open ends, and an image pickup unit housed in the chassis. The image pickup unit includes a solid-state image pickup chip constituted by a solid-state image pickup semiconductor device, chip-connecting board disposed adjacent to said solid-state image pickup chip and having an electric circuit mounted thereon, a connector board having external lead pins, leads connecting electrodes provided at an outer peripheral edge of at least one of said chip-connecting board and said connector board to electrodes of said solid-state image pickup chip, and a protective member sealing a light-receiving surface of said solid-state image pickup chip, said protective member being one of an optical glass plate and an optical filter.”). Suzuki teaches that “[s]ignals are fed between these boards via connection pins 229, and signals are fed between the solid-state image pickup chip 221 and each of these boards via the outer-leads 221m and side electrodes 226e, 227e and 228e of the boards. External lead pins 228p are mounted on the connector board 228, and are adapted to be connected to the plug 4 so as to send the signals to the camera control unit 3.” Suzuki, 2:55-63. Suzuki teaches “[t]he chip-connecting board 226, the circuit board 227 and the connector board 228 are arranged in such a manner

that their side electrodes 226e, 227e and 228e are disposed in registry with one another, and these three boards are aligned with each other. They are connected together by the connection pins 229 to provide the circuit module 222. A surface of the solid-state image pickup chip 221 opposite to the light-receiving surface thereof is bonded to the chip-connecting board 226 through the adhesive 225.” Suzuki, 3:15-25.

273. As discussed in Section VIII.D.3, a person of ordinary skill in the art would have been motivated to apply Suzuki’s known teachings of an image sensor comprising a first circuit board lying in a first plane and second circuit board lying in a second plane parallel to the first in implementing Swift’s teachings of a miniature camera (as modified by Ricquier’s teachings) where Swift’s circuit board 53 is oriented parallel to and stacked with respect to circuit board 52 to reduce the camera’s overall size and to improve the camera device’s “stability and reliability.” *See, e.g.*, Suzuki, 1:53-56, 3:61-4:12, 4:30-65.

h. Element [2.g]

274. **Element [2.g] recites “a lens mounted in said housing, said lens being integral with said imaging device, said lens focusing images on said array of CMOS pixels of said image sensor.”** Swift discloses element [2.g]. Swift discloses a lens mounted in said housing (*e.g.*, “wide-angle lens 57 ... mounted in the ... front housing portion 10”), said lens being integral with said imaging device

(e.g., as shown in Figure 2; “image sensor 201 engaged with a lens holder 202 ... to hold the lens 204 at a fixed ... distance from the sensor”), said lens focusing images on ... said image sensor (e.g., “positioned as to focus an image onto the image sensor 51”).

275. Swift discloses a “wide angled lens” “fixed” in the housing at a “predetermined distance from the sensor” and thus integral with said imaging device for focusing images on the “light-sensitive area” on said image sensor. Specifically, Swift discloses that “image sensor 201 (e.g. of APS type), engaged with a lens holder 202 ... the holder 202 serves to hold the lens 204 at a fixed, predetermined distance from the sensor 201, in order properly to focus an image onto the sensor 201.” Swift, 18:13-18.

276. As shown in Figure 2 below, Swift’s lens is mounted on a front housing portion so that the lens focuses the image onto the image sensor 51. Swift, 9:23-26 (“A wide-angle lens 57 is mounted in the front bore 12 of the front housing portion 10... The lens 57 is so positioned as to focus an image onto the image sensor 51.”).

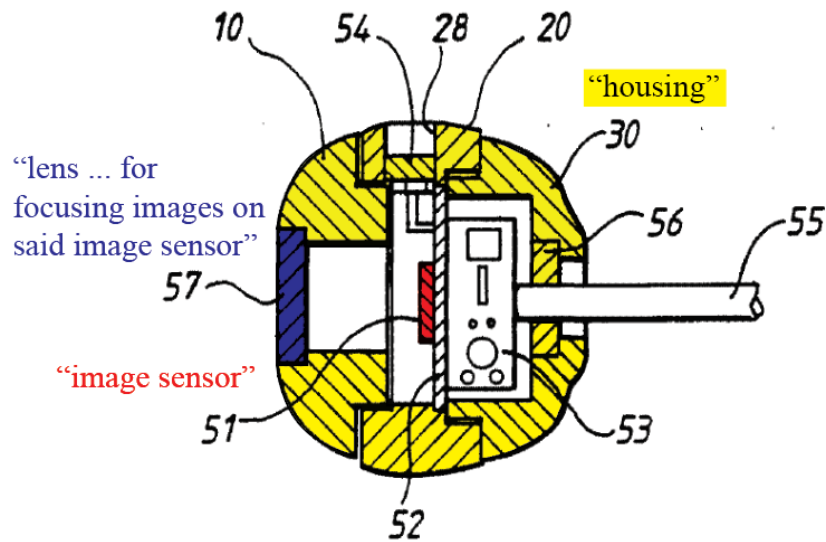


Fig.2.

Swift, Fig. 2 (annotated); *see also, e.g.,* Fig. 3 (showing exterior of housing with mounted lens).

277. As discussed in Section VIII.D.2, a person of ordinary skill in the art would have been motivated and found it obvious to apply Ricquier’s known teachings of arranging pixels in an array in implementing Swift image sensor 51 of a CMOS/APS type such that the active pixels in Swift’s image sensor are arranged in an array and Swift’s lens focuses images on said array of CMOS pixels.

i. Element [2.h]

278. **Element [2.h] recites “a video screen, said video screen being electrically coupled to said second circuit board, said video screen receiving said post-video signal and displaying images from said post-video signal.”** Swift discloses element [2.h]. Swift discloses a video screen (*e.g.,* “video monitor”), said

video screen being electrically coupled to said second circuit board (*e.g.*, “cable 55 is connected to the printed circuit board 53,” “[t]he camera 152 and monitor 154 are connected by ... a cabling system 160”), said video screen receiving said post-video signal and displaying images from said post-video signal (*e.g.*, “video monitor ... to display a signal received from the camera”).

279. Swift discloses a “video monitor” is “connected by ... a cabling system” “to the camera” to “display a signal received from the camera.” *See, e.g.*, Swift, 15:7-14. Swift further discloses that the cable is connected to the printed circuit board 53. *See, e.g.*, Swift, 9:5-18. The “video signals [are] provided from the camera 152 as ... video” from the “circuit board 53,” which “process[es]” “image signals received” from the “image sensor.” While Swift further discloses that there can be additional “external processing circuitry (not shown),” for example, to convert the signal to UHF, this circuitry is not required to create the video signal that is output from the camera and, more specifically, board 53. Swift, 15:13-18. This “printed circuit board 53,” which as discussed above with regards to [2.f], includes “circuitry components” to “process image signals received” from the image sensor. *See, e.g.*, 9:5-13. Swift explains that a “monitor 154 may comprise a domestic television set” and that “the video signals [are] provided from the camera 152 as [] video [] signals” so that “viewing of an image from the camera 152 may be selected on the television at will.” *See, e.g.*, Swift, 17:34-18:2. Swift also explains that

“video signals from” “[a]ny of the cameras mentioned” may be “distribute[d] ... to the ... TV.” *See, e.g.,* Swift, 18:8-11.

j. Element [2.i]

280. **Element [2.i]** recites “**a power supply mounted in said housing, said power supply being electrically coupled to said first circuit board to provide power to said array of CMOS pixels and said timing and control circuitry, said power supply also being electrically coupled to said second circuit board to provide power thereto.**” Swift discloses element [2.i]. Swift discloses a power supply (*e.g.*, “battery,” “voltage regulator”) mounted in said housing (*e.g.*, “provided within the housing”), said power supply being electrically coupled to said first circuit board to provide power to said array of CMOS pixels and said timing and control circuitry, said power supply also being electrically coupled to said second circuit board to provide power thereto (*e.g.*, “a voltage regulator to ... provide a substantially constant supply voltage to components” including “an image sensor assembly” and “a video processor” on the “circuit board”).

281. Swift’s battery and voltage regulator provide voltage to (and thus are electrically coupled to and drive) the “image sensor 51” (including its pixels) and the components of circuit boards 52 and 53. For example, Swift discloses that its image sensor assembly includes a “battery” and “a voltage regulator,” which “provide[s] a substantially constant supply voltage to components on the printed

circuit board,” including the image sensor 51. Swift, 4:21-22 (“A camera as above may incorporate a battery or voltage transformer means.”), 3:31-4:4 (“[I]mage sensor assembly ... comprising a printed circuit board and, mounted thereon, the image sensor ... a voltage regulator to accept a plurality of different input voltages and provide a substantially constant supply voltage to components on the printed circuit board.”), 10:12-20, 9:7-13 (“Various circuitry components are mounted on the circuit board 53, to provide power to the image sensor 51”).

282. Furthermore, at minimum, a person of ordinary skill in the art would have understood that Swift’s battery and voltage regulator provide voltage to (and thus are electrically coupled to and drive) the “image sensor 51” (including its pixels) and circuit boards 52 and 53.

283. In addition, Swift discloses the voltage regulator is mounted on an assembly in the camera’s housing. And based on Swift’s disclosure that “the housing 50” has “sufficient room to house a battery,” a person of ordinary skill in the art would have understood that the battery is mounted in the housing.

284. As discussed in Section VIII.D.2, a person of ordinary skill in the art would have been motivated and found it obvious to apply Ricquier’s known teachings of CMOS-implemented “X-Y addressable photodiode array” in implementing Swift image sensor 51 of a CMOS/APS type— thus the power supply

of Swift would provide power to the array of CMOS pixels thus the power supply of Swift would provide power to the array of CMOS pixels.

k. Element [2.j]

285. **Element [2.j] recites “wherein a largest dimension of said image sensor along said first plane is between 2 and 12 millimeters.”** Swift in view of Suzuki renders obvious element [2.j]. Swift discloses an image sensor along said first plane. Suzuki discloses a largest dimension of an image sensor along said first plane is between 2 and 12 millimeters (*e.g.*, image sensor along the first plane is at least “8.5 mm” and no greater than “10mm”).

286. As discussed with respect to [2.b], Swift discloses said image sensor along said first plane. *See* Section VIII.D.4.c.

287. While Swift discloses the image sensor including “circuit board 52” (to which the image sensor chip is mounted) on a first plane, Swift does not expressly disclose the circuit board’s dimensions. Suzuki discloses this implementation detail. As discussed in Section VIII.B, Suzuki discloses that the “chip-connecting board 226”’s largest dimension is between 8.5 and 10 mm.

288. Suzuki discloses that “in this embodiment of the invention, ... where the solid-state image pickup chip of inch (8.5 mm) is used, the outer diameter of the camera head is about 10 mm, and therefore is smaller about 5 mm than that of the conventional camera head.” Suzuki, 4:6-11. Suzuki further explains, through a

series of production steps describing Figures 3A-3D and Figure 2, that the “image pickup chip 221” bonded to “chip connecting board 226,” “circuit board 227,” and “connector board 228” are “disposed in registry with one another” so that they are all “aligned with each other,” and are “inserted into the chassis 24”:

(iii) Third step (FIG. 3C)

The chip-connecting board 226, the circuit board 227 and the connector board 228 are arranged in such a manner that their side electrodes 226e, 227e and 228e are disposed in registry with one another, and these three boards are aligned with each other. They are connected together by the connection pins 229 to provide the circuit module 222. A surface of the solid-state image pickup chip 221 opposite to the light-receiving surface thereof is bonded to the chip-connecting board 226 through the adhesive 225.

(iv) Fourth step (FIG. 3D)

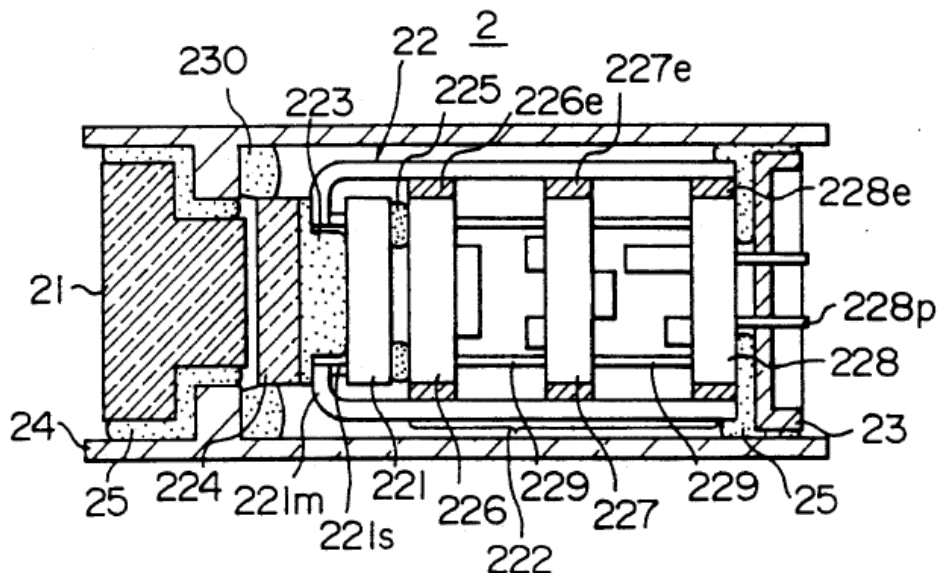
Each outer-lead 221m is bent through about 90° at a point near the chip 221, and is soldered to the side electrodes 226e, 227e and 228e of the boards 226, 227 and 228 to make electrical connections among the boards, thereby constituting the image pickup unit 22.

(v) Fifth step (FIG. 2)

The image pickup unit 22 is inserted into the chassis 24, and the optical glass plate 224 is fixed at its outer periphery to the chassis 24 by an adhesive 230. ... [¶] As described above, in this embodiment, the electrodes of the solid-state image pickup chip are directly connected through the outer-leads with the inner-leads to the electrodes of the chip-connecting board, the circuit board, the connector board.

Suzuki, 3:1-49; *see also, e.g.*, Suzuki, Figs. 3A-3D, Fig. 2. Suzuki illustrates this in Figure 2 below, which shows a completed image pickup unit where each of the boards 226, 227, and 228 is in alignment with one another so that their outer edges line up so that their “side electrodes 226e, 227e and 228e” can be “soldered” to the “outer-lead 221m [which] is bent through about 90° at a point near the chip 221” and runs parallel to the chassis of the camera.

FIG. 2



Suzuki, Fig. 2. Suzuki teaches that by configuring the image pick up chip and boards in this stacked configuration, when a “solid-state image pickup chip of...8.5 mm[] is used,” the “outer diameter of the camera head,” or chassis 24, “is about 10 mm.” *See, e.g.*, Suzuki, 4:6-11 (“Further, in this embodiment of the invention, in the case where the solid-state image pickup chip of 1/3 inch (8.5 mm) is used, the outer diameter of the camera head is about 10 mm, and therefore is smaller about 5 mm

than that of the conventional camera head.”), 1:53-56 (“It is an object of this invention to provide a camera head for a solid-state image pickup device which camera head has an outer diameter closer to a diagonal length of a solid-state image pickup chip.”), 4:58-61 (“With the above construction, there is provided an advantage that the outer diameter of the camera head can be reduced to a small size close to the diagonal length of the solid-state image pickup chip.”). These boards are, therefore, the same size as “solid-state image pickup chip 221” in order to couple the side electrodes to the outer lead that runs at a 90° angle from the pick-up chip. Thus, the greatest dimension of the “chip-connecting board 226” of the image sensor is between 2 and 12 millimeters.

289. As discussed in Section VIII.D.3, a person of ordinary skill in the art would have found it routine, straightforward and advantageous to apply Suzuki’s known teachings of arranging an 8.5-mm image pickup chip, a chip-connecting board, and a second circuit board, in parallel planes and in a stacked configuration to fit within a 10-mm diameter casing, in implementing Swift’s teachings of an miniature camera (as modified by Ricquier’s teachings), and would have known that such a combination (yielding the claimed limitations) would predictably work and provide the expected functionality.

E. Claim 2 is Obvious under §103 over Larson in View of Swift, Ricquier, and Suzuki (Ground 5)

290. As discussed in Section VIII.D, Swift in view of Ricquier and Suzuki (Ground 4) renders obvious claim 2.

291. To the extent further disclosure of a physical camera within the same physical housing as the video monitor to form the claimed “imaging device” is required as discussed with respect to [2.pre], Larson (Ex. 1029) discloses the implementation details for an imaging device (*e.g.*, “A videophone includes a video camera” that is “mounted in a tilt and swivel housing” with a “flat panel liquid crystal display (LCD) for displaying images”) with a physical camera and a display screen contained in a single housing. *See, e.g.*, Larson, Abstract, 7:8-27 (“[T]he videophone ... incorporates a flat panel liquid crystal display (LCD) for displaying images ... [¶] For example, the LCD can be a 128×112 picture element (pixel) color LCD. ... The images are transduced and digitized by a charge coupled device (CCD) chip video camera having a plastic lens. ... The LCD and the CCD video camera are preferably mounted in a tilt and swivel housing for ease of positioning the video camera and viewing screen to facilitate use of the videophone in accordance with one embodiment of the invention. This also enables the videophone of the invention to be housed in a compact housing.”). For example, Figure 8B1 of Larson illustrates a single “housing 131 for the CCD camera lens 44A and the LCD panel 56B.” *See, e.g.*, Larson, 26:43-54 (“As shown in FIG. 8B1, a housing 131 for the CCD camera

lens 44A and the LCD panel 56B can be swiveled, as indicated by the double headed arrows, to rotatably position the CCD camera lens and the LCD panel. Also, the housing 131 for the CCD camera lens 44A and the LCD panel 56B can be tilted, as indicated by the double headed arrow shown in FIG. 8B2, to set the angle of the CCD camera lens and the LCD panel. Therefore, the person can swivel and tilt the housing 131 to obtain the desired field of view of the CCD camera lens 44A and, consequently, the image that is transmitted to the remote videophone 10' shown in FIG. 6.”).

292. Although Larson is primarily concerned with displaying video transmissions received from other users, Larson also discloses that a user can use a “local viewing button” to make the LCD display the image that is being captured by the local camera. *See, e.g.,* Larson, 26:37-43 (“The person at the local station can press a local viewing button 130 labeled ‘MONITOR’ in FIG. 8A to view on the LCD panel 56B shown in FIG. 8B1 the image that the local videophone 10 shown in FIG. 6 is transmitting. The ‘MONITOR’ button 130 is preferably located adjacent to the ‘VIDEO’ button 126.”); Fig. 8A, 8B1-8B2 (illustrating the tilt and swivel camera and display integrated in the videophone).

293. Like Swift, Ricquier, and Suzuki, Larson is in the same field of art and is analogous to the ’052 patent—all are in the same field related to solid state image sensors for use in cameras. *See, e.g.,* ’052 patent, Abstract, 1:32-36, 7:65-8:1;

Larson Abstract (“A videophone includes a video camera for transducing and digitizing images....”); 26:43-54 (“[T]he person can swivel and tilt the housing 131 to obtain the desired field of view of the CCD camera lens 44A and, consequently, the image that is transmitted to the remote videophone 10’ shown in FIG. 6.”), 1:13-23 (“The present invention relates in general to telecommunications and, more particularly, to telecommunication systems for transmitting both audio and video signals....”), 3:31-42 (“[A] videophone comprising a video camera means for transducing and digitizing images....”). Like the ’052 patent, Larson is directed to the display of images from an image capturing device. *See, e.g.*, ’052 patent, 4:32-35, 16:10-14, 15:7-14; Larson, Abstract (“[T]he station further includes a display connected to the video processor for reproducing images....”), 26:37-43 (“The person at the local station can press a local viewing button 130 labeled ‘MONITOR’ in FIG. 8A to view on the LCD panel 56B shown in FIG. 8B1 the image that the local videophone 10 shown in FIG. 6 is transmitting.”). Larson is also reasonably pertinent to the problem identified in the ’052 patent of minimizing the profiles of devices utilizing imaging devices. As Larson explains, using a single “tilt and swivel housing” can be used “for ease of positioning the video camera and viewing screen,” and also “enables the videophone of the invention to be housed in a compact housing.” Larson, 7:14-27. Moreover, Larson teaches that this design “enables the videophone of the invention to be much more compact and require less power.” Larson, 7:6-13.

294. While Larson teaches a “videophone” using a “CCD camera” (Larson, 7:22-26), as discussed in Section VIII.D.1, Swift teaches “incorporati[ng]” a “miniature camera” using a CMOS image sensor (Swift, 1:7-13). As discussed in Sections VIII.B, VIII.C.2, and VIII.D, Ricquier and Suzuki provide additional implementation details concern the camera and image sensor that would have been obvious to apply in implementing Swift’s camera. As the ’052 patent acknowledges, CMOS image sensors and readout circuitry for operating such sensors, as disclosed in Swift and Ricquier, were well-known in the art. ’052 patent, 2:9-15, 2:25-34. Further, the ’052 patent admits that it was known that CMOS active pixel sensor imagers result in lower noise than CCD or other solid state imagers, can be mass produced on standard semiconductor productions lines, can incorporate a number of other different electronic controls that are usually found on multiple circuit boards of much larger size, and require less power than CCD imagers. ’052 patent, 1:66-2:19; *see also* NASA (Ex. 1060, publicly available 03/06/1995 through Business Week, and I understand is prior art to the ’052 patent) (“low power-consumption,” “small[er] size,” “made on standard semiconductor production lines,” “cost[s] much less than CCDs,” and can tolerate lower material quality). Moreover, Swift teaches “[m]iniature cameras are finding increasing application ... for incorporation in other devices” where “it is often desirable for a camera to be as small as possible, so that

it may be located discretely in such a way that it is not readily observed.” Swift, 1:7-13.

295. Thus, a person of ordinary skill in the art would have been motivated and found it advantageous to apply the teachings of Swift’s miniature camera (as modified by Ricquier’s and Suzuki’s teachings as discussed in Section VIII.D) in implementing Larson’s “camera” in the “videophone” with a “compact housing.” Larson 7:14-27 (“The LCD and the CCD video camera are preferably mounted in a tilt and swivel housing for ease of positioning the video camera and viewing screen... This also enables *the videophone of the invention to be housed in a compact housing.*”). In light of the above, a person of ordinary skill in the art would have found it routine, straightforward and advantageous to apply Swift’s miniature camera (as modified by Ricquier’s and Suzuki’s teachings as discussed above) in implementing Larson’s camera and would have known that such a combination (yielding the claimed limitations) would predictably work and provide the expected functionality.

IX. SECONDARY CONSIDERATIONS

296. The Challenged Claims of the ’052 patent are obvious under §103 based on the references presented herein.

297. Patent Owner submitted a declaration from the inventor in related prosecution (prosecution of the ’839 patent—related to the ’052 patent through

multiple continuation and continuation-in-part applications) ('839 Patent File History (Ex. 1003), 83-95) that argued an unexpected result of decreased interference. Specifically, when image processing circuitry is removed from the same board or plane as the pixel array, decreased interference was argued as an unexpected result. In particular, inventor Jeffrey Adair asserted that:

CCD devices cannot be used near an electrical surgical generator without requiring significant shielding for the CCD device. Such shielding requires intense grounding techniques for the CCD camera cables/conductors which trail the CCD imager, and also grounding for the actual CCD pixel array. These shielding techniques not only add significantly to the size of the CCD device, but also to the overall cost of the CCD camera system. Even when such shielding is incorporated, RFI levels are only brought to a reasonable level which may still result in an obstructed view of the surgical area.

'839 Patent File History, 85.

298. The Patent Owner further asserted that, "Even with standard CMOS devices which have processing circuitry on chip with the CMOS pixel array, at least some shielding is required to prevent RFI in order to optimize the image." '839 Patent File History, 86. It does not appear that the examiner relied upon this argument in finding patentability, nonetheless, I have been asked to address this Patent Owner argument.

299. My understanding of these noise benefits is that they were not unexpected, but were instead predictable. For example, as the declaration notes,

they were using endoscopic cameras around an “electrosurgical generator” that was used to “cut or cauterize” tissue. ’839 File History, 85. It would have been understood by a person of ordinary skill in the art that such an electrosurgical generator would create a large amount of electromagnetic (“EM”) radiation. Moreover, while the declaration does not clearly state how many wires were in the CCD system at issue, a person of ordinary skill in the art would have understood that such EM radiation would cause radio frequency interference (“RFI”) in a system, and would have a more significant adverse effect on a system with more wires than a system with fewer wires. It was also known that a CCD sensor could have many more wires than a CMOS sensor. For example, according to the declaration, the prior art CCD sensor identified in the declaration (“Pelchy”) includes “a large number of transmissions wires 33 which interconnect the circuit boards placed perpendicular to the pixel array with an external processor 13.” ’839 File History, 92. Thus, in a CCD sensor with many wires, the radio frequency interference would have a relatively large effect on the quality of images produced by the image sensor. On the other hand, CMOS sensors require only a few wires to connect to the pixel array, and thus interference created in a CMOS image sensor would be much smaller than in such a CCD arrangement. Moreover, while the declaration does not specify what the structure of the processing circuitry was that was removed from the plane with the image sensor, it would have been understood

that removing processing circuitry from the image sensor would further reduce interference for various reason, depending on the circuitry removed. As but one example, it was well understood that interference would be caused by placing analog and digital circuitry too close to each other, and that a way to reduce interference was to place analog and digital circuitry on separate circuit boards. *See* Phillips (Ex. 1085) (“The PCRM 100 handles internal EMI between analog and digital circuitry using separate circuit boards, shielding and isolation.”). Thus, it was known that EMI/RFI could be further reduced by removing the processing circuitry from the image sensor. Importantly, because, as explained above, Swift discloses placing the processing circuitry on a separate circuit board placed closely adjacent the CMOS pixel array (*see* Section VIII.D) and Monroe discloses removing the processing circuitry from the image sensor and placing it in a remote control box (*see, e.g.,* Monroe, 3:57-62, 8:8-11, Fig. 3), it was already known to locate the processing circuitry away from the image sensor, and the results of doing so (*e.g.,* decreased interference) were already known and utilized in the field.

300. In addition, the benefits of using CMOS image sensors instead of CCD image sensors, including reduced cost, low noise, small size, easier manufacturing process and a higher tolerance of lower quality material, were not unexpected, and were explicitly noted by those in the field at the time, as well as their applicability to medical devices. *See, e.g.,* ’052 patent, 1:60-2:19; NASA (Ex. 1060) (describing

benefits of active pixel image sensor over CCD sensors, including lower power consumption, smaller size, no need for a custom manufacturing process, and can tolerate lower material quality); Monroe (Ex. 1007), 1:7-17, 7:59-65 (describing a medical otoscope (similar to an endoscope) with a CMOS image sensor with separate video processing circuitry).

301. Patent Owner did not present any other evidence of secondary considerations during prosecution and the clear teachings. In light of the above, to the extent this aspect of the prosecution history can be considered “secondary considerations,” such would not change my opinions expressed herein.

X. PUBLIC ACCESSIBILITY OF RICQUIER (EXS. 1033, 1038)

302. I have been informed that a reference is publicly accessible if it has been disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it.

303. I have been informed that Ricquier is a conference paper that was presented at the Charge-Coupled Devices and Solid State Optical Sensors IV 1994 conference, which was a part of the Electronic Imaging 1994 symposium, and published in volume 2172 of the Proceedings of SPIE. In the 1990s, SPIE’s journals, conferences, and conference proceedings were among the most prominent sources of information on optics, photonics, optoelectronics, lasers, and electronic imaging,

and this remains true today. The Proceedings of SPIE contained papers presented at SPIE conferences, and these papers were known to be especially useful because they represented recent advances in their respective fields. The Proceedings of SPIE was a known source of research in the area of digital imaging in the 1990s. Since 1982, I have personally attended over thirty SPIE Conferences and have published over sixty papers in the Proceedings of SPIE. By 1997, I had read hundreds of papers published in the Proceedings of SPIE.

304. Persons of ordinary skill would have known that in the late 1990s the full set of the Proceedings of SPIE was available in libraries or available for purchase from SPIE, whether as a single volume or as part of a subscription service for all volumes and would have further known that individual articles within the Proceedings were available for purchase from SPIE. In this timeframe, I regularly accessed the Proceedings of SPIE from the libraries at Caltech and UT Austin.

305. The International Symposium on Electronic Imaging: Science and Technology, 1994, and the Charge-Coupled Devices and Solid State Optical Sensors IV 1994 conference within the symposium, was a well-known, respected conference in the area of solid-state imaging. Persons of ordinary skill and other members of the public with an interest in advances in the area of digital imaging would have attended this conference.

306. Exs. 1033 and 1038 confirm that Ricquier was included on pages 2-10

of volume 2172 of the Proceedings of SPIE, which served as the record of the Charge-Coupled Devices and Solid State Optical Sensors IV 1994 conference.

307. Ex. 1038 at Pages 3 of 16, as marked by the exhibit labels, confirms that volume 2172 of the Proceedings was available at the University of Wisconsin library as of May 27, 1994.

308. Ex. 1033 at Page 1 of 18, as marked by the exhibit labels, confirms that SPIE published Volume 2172 by April 4, 1994 and began shipping Volume 2172 of the Proceedings of SPIE as of April 5, 1994. According to the declaration, I am informed that SPIE shipped 100-120 print copies of Volume 2172 to library customers by May 1, 1994, which is consistent with the availability date at the University of Wisconsin library as of May 27, 1994.

309. Based on its inclusion in the Proceedings of SPIE, Ricquier was disseminated by SPIE and made readily available to persons of ordinary skill in the art at libraries, including the University of Wisconsin library, and through distribution by SPIE, at least one year prior to the earliest October 6, 1997 priority date.

XI. CONCLUSION

310. In summary, I have concluded that each of the Challenged Claims is unpatentable as obvious under 35 U.S.C. §103 in light of the prior art references as

discussed above and the knowledge of one of ordinary skill in the art, as described above.

311. Specifically, in my opinion, for at least the reasons above, the Challenged Claims are rendered obvious as shown in the chart below:

Ground	References	Basis	Claims
1	Wakabayashi in view of Ackland	§103	1
2	Wakabayashi in view of Ackland and Suzuki	§103	1
3	Wakabayashi in view of Riquier and Dierickx	§103	3, 7
4	Swift in view of Ricquier and Suzuki	§103	2
5	Larson in view of Swift, Ricquier, and Suzuki	§103	2

312. To the extent it is argued that any further disclosure is required for a limitation in claims 1, 2, 3 and 7 that I have identified as being disclosed (explicitly or inherently) by Wakabayashi, Ackland, Suzuki, Ricquier, and Dierickx, a person of ordinary skill in the art would certainly have found that limitation obvious to include based on the same explicit disclosure or inherent disclosures and analysis I have identified above.

313. I reserve the right to supplement my opinions in the future to respond to any arguments that Patent Owner or its expert(s) may raise and to take into account new information as it becomes available to me.

314. I hereby declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that all statements made

of my own knowledge are true and that all statements made on information and belief are believed to be true.

315. Sworn to this 17th day of February 2020 in Austin, Texas.

A handwritten signature in black ink, appearing to read "Dean Neikirk", written over a horizontal line.

Dean P. Neikirk, Ph.D.

APPENDIX A (CURRICULUM VITAE)

Dean P. Neikirk

Professor, Cullen Trust for Higher Education Professorship in Engineering (No. 7)
Department of Electrical and Computer Engineering
Cockrell School of Engineering
The University of Texas at Austin
The Graduate School
110 Inner Campus Dr Stop G0400
Austin, TX 78712

Education:

Oklahoma State University (Physics and Mathematics; with Honors)	B.S.	1979
California Institute of Technology (Applied Physics)	M.S.	1981
California Institute of Technology (Applied Physics)	Ph.D.	1984

Professional Experience:

Assistant Professor, University of Texas at Austin, Jan. 1984 - Aug. 1988
Associate Professor, University of Texas at Austin, Sept. 1988- Aug. 1992
Full Professor, University of Texas at Austin, Sept. 1992-present
Associate Dean of Graduate Studies, August 2014 - present

Honors and Awards:

- 1984 Marconi International Fellowship Young Scientist Award "for contributions to the development of millimeter wave integrated circuits especially in the areas of detectors and imaging arrays."
- Listed in the Second Edition of Who's Who in Frontiers of Science and Technology, 5th Edition of Who's Who in Technology Today, 1994 American Men & Women of Science; 1985 Outstanding Young Man of America, 1989 Outstanding Young Man of America; 7th Edition of Who's Who in Technology.
- 1984-85 Engineering Foundation Faculty Award, University of Texas at Austin Engineering Foundation Advisory Council.
- 1985-90 General Motors Foundation Centennial Teaching Fellowship, University of Texas at Austin.
- 1985-86 IBM Corporation Faculty Development Award
- 1986 National Science Foundation Presidential Young Investigator.

- 1987 Award for Outstanding Engineering Teaching by an Assistant Professor, College of Engineering, University of Texas at Austin.
- 1990-1992 Temple Foundation Endowed Faculty Fellowship (No. 1), University of Texas at Austin.
- 1992-present Cullen Trust for Higher Education Professorship in Engineering (No. 7), University of Texas.
- 1997 College of Engineering Award for Outstanding Teaching in the Department of Electrical and Computer Engineering, University of Texas at Austin.
- 2003 Department of Electrical and Computer Engineering Gordon T. Lepley IV Endowed Memorial Teaching Award, University of Texas at Austin.
- 2007 Lockheed Martin Aeronautics Company Award for Excellence in Engineering Teaching
 - each year since 1956, Lockheed Martin and its predecessor, has sponsored an award for excellence in engineering teaching to reward one College of Engineering faculty member for exceptional teaching. This prestigious award is given to a faculty member dedicating time and energy in abundance to teaching undergraduate and graduate students. As a result, his or her work leaves a mark of excellence on the entire College of Engineering. Nominations for this award are made by The University of Texas at Austin engineering students and faculty. Final selection is made by a committee composed the five most recent faculty recipients of the award and the student presidents of the Student Engineering Council (SEC) and the Graduate Engineering Council (GEC).
- 2015 Civitatis Award: The University of Texas at Austin Civitatis Award was established in 1997 to recognize outstanding faculty citizenship. The Civitatis Award is conferred upon a member of the faculty in recognition of dedicated and meritorious service to the University above and beyond the regular expectations of teaching, research, and writing. The award is made by the President upon the recommendation of the Faculty Council Executive Committee. Prof. Neikirk was nominated for the award for his “extensive, effective and distinguished service record to his department, college and [the] University of Texas.”

Vita for Dean P. Neikirk:

Dean P. Neikirk was born in Oklahoma City, Oklahoma, on October 31, 1957. He received the B.S. degree (1979) in physics from Oklahoma State University, and the M.S. (1981) and Ph.D. (1984) degrees in applied physics from the California Institute of Technology. He joined the faculty of The University of Texas at Austin in 1984, and is currently a Professor in the Department of Electrical and Computer Engineering, holding the Cullen Trust for Higher Education Professorship in Engineering (No. 7). Dr. Neikirk developed the first monolithic, high resolution focal plane detector array for use at wavelengths between 0.1 mm and 1 mm, and in 1984 received the Marconi International Fellowship Young Scientist Award "for contributions to the development of millimeter

wave integrated circuits especially in the area of detectors and imaging arrays." He has also been named a 1986 National Science Foundation Presidential Young Investigator.

Dr. Neikirk's current research interests concentrate on the fabrication and modeling of electromagnetic and micromachined sensors and actuators. His work also includes projects involving integrated circuit processing and the high frequency properties of transmission lines. His work concentrates on the use of advanced fabrication techniques, including silicon micromachining, for new device and sensor development. Dr. Neikirk developed the teaching laboratory for semiconductor device fabrication at The University of Texas at Austin, and is an active member of The University of Texas at Austin Microelectronics Research Center. Recently Dr. Neikirk's research project related to the development of new chemical sensors (an "electronic taste" sensor) was selected for a commercialization venture between the University of Texas and LabNow, Inc. Dr. Neikirk has also served as the Graduate Advisor of the Department of Electrical and Computer Engineering at UT-Austin, an Associate Chairman of the ECE Department, the Chair of the UT-Austin Graduate Assembly, the Chair of the UT-Austin Faculty Council, the Secretary of the General Faculty at UT-Austin, and is currently Associate Dean of the University of Texas at Austin Graduate School.

Professional Societies:

Senior Member, Institute of Electrical and Electronics Engineers

- Associate Editor for Solid State and VLSI Electronics, **IEEE Transactions on Education** (March 1991- Oct. 1994)

Commercialization of Technology:

Two companies have been founded based on technology developed by Dr. Neikirk's research group. In both cases the technology was developed at The University of Texas at Austin and licensed to start-ups.

From a University of Texas news release:

Firm commercializing University of Texas technology rounds up \$14 million venture capital investment (October 1, 2004)

AUSTIN, Texas—LabNow Inc. has received \$14 million in first-round venture investment for its point-of-care diagnostic system from the Soros Group, Austin Ventures and other investors.

The money will be used to develop the company's technology and to launch its initial product, CD4Now™, a point-of-care diagnostic tool for HIV/AIDS patients.

The device, which is based on technology developed at The University of Texas at Austin, quickly and accurately analyzes complex fluids such as blood.

Patents

1. US Patent 5,080,870: "Sublimating and Cracking Apparatus," Jan. 14, 1992; Inventors: B. G. Streetman, T. J. Mattord, D. P. Neikirk
2. US Patent 5,408,107: "Semiconductor Device Having Multiple Current-Voltage Curves and Zero-Bias Memory," April 18, 1995; Inventors: Dean P. Neikirk and Kiran Kumar Gullapalli
3. US Patent 6,589,779: "General signaling protocol for chemical receptors in immobilized matrices," July 8, 2003; Inventors: McDevitt; John T.; Anslyn; Eric V.; Shear; Jason B.; Neikirk; Dean P. Assignee: Board of Regents, The University of Texas System (Austin, TX)
4. US Patent 6,602,702: "Detection system based on an analyte reactive particle," August 5, 2003 Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)

Assignee: The University of Texas System (Austin, TX)

5. US Patent 6,649,403: "Method of preparing a sensor array," November 18, 2003
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas Systems (Austin, TX)
6. US Patent 6,680,206, "Sensor arrays for the measurement and identification of multiple analytes in solutions," January 20, 2004
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas Systems (Austin, TX)
7. US Patent 6,713,298, "Method and apparatus for the delivery of samples to a chemical sensor array," March 30, 2004
Inventors: McDevitt; John T. (Travis, TX); Anslyn; Eric V. (Travis, TX); Shear; Jason B. (Travis, TX); Neikirk; Dean P. (Travis, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
8. US Patent 6,908,770, "Fluid based analysis of multiple analytes by a sensor array," June 21, 2005
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
9. US Patent 7,022,517, "Method and apparatus for the delivery of samples to a chemical sensor array," April 4, 2006, filed: July 14, 2000
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX); Borich; Damon V. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
10. US Patent 7,316,899, "Portable sensor array system," January 8, 2008, filed: January 31, 2001
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
11. US Patent 7,491,552, "Fluid based analysis of multiple analytes by a sensor array," February 17, 2009, filed: January 20, 2005
Inventors: McDevitt; John T. (Austin, TX); Anslyn; Eric V. (Austin, TX); Shear; Jason B. (Austin, TX); Neikirk; Dean P. (Austin, TX)
Assignee: Board of Regents, The University of Texas System (Austin, TX)
12. United States Patent 7,651,868, "Method and system for the analysis of saliva using a sensor array," January 26, 2010, Filed: December 13, 2004

Inventors: McDevitt; John T. (Austin, TX), Anslyn; Eric V. (Austin, TX), Shear; Jason B. (Austin, TX), Neikirk; Dean P. (Austin, TX), Christodoulides; Nick J. (Austin, TX)

Assignee: The Board of Regents of The University of Texas System (Austin, TX)

13. United States Patent 8,101,431, "Integration of fluids and reagents into self-contained cartridges containing sensor elements and reagent delivery systems," January 24, 2012, Filed: December 22, 2004

Inventors: McDevitt; John T. (Austin, TX), Ballard; Karri L. (Pflugerville, TX), Floriano; Pierre N. (Austin, TX), Christodoulides; Nick J. (Austin, TX), Neikirk; Dean (Austin, TX), Anslyn; Eric (Austin, TX), Shear; Jason (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

14. United States Patent 8,105,849, "Integration of fluids and reagents into self-contained cartridges containing sensor elements," January 31, 2012, Filed: December 22, 2004

Inventors: McDevitt; John T. (Austin, TX), Ballard; Karri L. (Pflugerville, TX), Floriano; Pierre N. (Austin, TX), Christodoulides; Nick J. (Austin, TX), Neikirk; Dean (Austin, TX), Anslyn; Eric (Austin, TX), Shear; Jason (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

15. United States Patent 8,257,967, "Method and system for the detection of cardiac risk factors," September 4, 2012, Filed: April 28, 2003

Inventors: McDevitt; John T. (Austin, TX), Anslyn; Eric V. (Austin, TX), Shear; Jason B. (Austin, TX), Neikirk; Dean P. (Austin, TX), Christodoulides; Nick J. (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

16. United States Patent 9,291,586, "Passive wireless self-resonant sensor," March 22, 2016, Filing Date: May 5, 2013

Inventors: Neikirk, Dean P. (Austin, TX, US), Pasupathy, Praveenkumar (Austin, TX, US), Zhang, Sheng (Austin, TX, US), Leonhardt, Brad (Austin, TX, US), Ekerdt, John G. (Austin, TX, US), Korgel, Brian A. (Austin, TX, US), Holmberg, Vincent C. (Seattle, WA, US), Shipman, Catherine D. (Reston, TX, US), Bogart, Timothy D. (Oxford, GB), Chockla, Aaron (Chicago, IL, US)

Assignee: Board of Regents, The University of Texas System (Austin, TX, US)

17. United States Patent 9,581,559, "Corrosion detection sensor embedded within a concrete structure with a diffusion layer placed over the sacrificial transducer," February 28, 2017, Filing Date: August 14, 2014

Inventors: Neikirk; Dean P. (Austin, TX), Wood; Sharon L. (Austin, TX), Pasupathy; Praveenkumar (Austin, TX), Yosef; Ali Abu (Austin, TX)

Assignee: Board of Regents, The University of Texas System (Austin, TX)

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3. P. E. Young, W.A. Peebles, N.C. Luhmann, Jr., R.J. Taylor, D. B. Rutledge, D. P. Neikirk, and P.P. Tong, "Current Profile Measurements in a Tokamak Plasma," 25th Ann. APS Meeting, Div. of Plasma Physics, Nov., 1983.

4. D. B. Rutledge, D. P. Neikirk, P.P. Tong, P.E. Young, W.A. Peebles, N.C. Luhmann, Jr., and R.J. Taylor, "Demonstration of a FIR Imaging System as a Multi-Channel Interferometer," 25th Ann. APS Meeting, Div. of Plasma Physics, Nov., 1983.

5. P.E. Young, N.C. Luhmann, Jr., R.J. Taylor, D. P. Neikirk, and D. B. Rutledge, 26th Annual Meeting of the Division of Plasma Physics, Boston, MA, Oct 29- Nov 2, 1984.
6. D.L. Brower, W.A. Peebles, S. Kim, R.L. Savage, Jr., T. Lehecka, N.C. Luhmann, Jr., J. Wagner, D. B. Rutledge, D. P. Neikirk, P.E. Young, and H.K. Park, "Recent advances in multichannel far-infrared collective scattering and interferometry systems," Eleventh Symposium on Fusion Engineering, Austin, TX, Nov. 18-22, 1985.
7. A.C. Campbell, V.P. Kesan, G.E. Crook, C.M. Maziar, D. P. Neikirk, and B. G. Streetman, "Capacitive Hysteresis Effects in 5.0nm single and double barrier AlAs Tunneling Structures," 8th Molecular Beam Epitaxy Workshop, Los Angeles CA, September 9-11, 1987.
8. A.C. Campbell, V.P. Kesan, G.E. Crook, D. P. Neikirk, and B. G. Streetman, "Capacitance Transient Analysis of GaAs/AlAs Tunneling Structures," 1988 Electronics Materials Conference, University of Colorado, Boulder, Colorado, June 22-24, 1988.
9. V.P. Kesan, A. Dodabalapur, D. P. Neikirk, and B. G. Streetman, "Influence of MBE Growth and Rapid Thermal Annealing Conditions on the Electrical Properties of Normal and Inverted AlGaAs/InGaAs Pseudomorphic HEMT Structures," IEEE 46th Annual Device Research Conference, June 20-22, 1988, Boulder, CO.
10. A. Dodabalapur, V.P. Kesan, T.R. Block, D. P. Neikirk, and B. G. Streetman, "Optical and Electrical Characteristics of Normal and Inverted AlGaAs/InGaAs Pseudomorphic HEMT Structures Processed by RTA," 9th Molecular Beam Epitaxy Workshop, West Lafayette, Indiana, September 21-23, 1988.
11. A. Sharif, D. P. Neikirk, and D.R. Diller, "Design and Fabrication of a Multi-Sensor Cryomicroscope Stage using VLSI Technology," Cryo 89, Charleston, SC, June 1989, published in **Physics in Medicine and Biology** 33.
12. A. Dodabalapur, V.P. Kesan, D. P. Neikirk, B. G. Streetman, M.H. Herman, and I.D. Ward, "Photoluminescence and Electreflectance Characterization of Modulation-Doped Quantum Wells," Journal of Electronic Materials 18, July 1989, p. 51.
13. V.K. Reddy and D. P. Neikirk, "Influence of Growth Interruption on I - V Characteristics of AlAs/GaAs Double Barrier Resonant Tunneling Diodes," 11th Annual Molecular Beam Epitaxy Workshop, Austin TX, Sept. 16-18, 1991.
14. A.J. Tsao, V.K. Reddy, D.R. Miller, K.K. Gullapalli, and D. P. Neikirk, "The effect of barrier thickness asymmetries on the electrical characteristics of AlAs/GaAs double barrier resonant tunneling diodes," 11th Annual Molecular Beam Epitaxy Workshop, Austin TX, Sept. 16-18 1991.
15. T.R. Block, D. P. Neikirk, and B. G. Streetman, "MBE growth condition dependence

of RHEED dampening and QW photoluminescence," Twelfth North American Conference on Molecular Beam Epitaxy, Ottawa, Canada, Oct. 12-14, 1992.

16. T.J. Mattord, D. P. Neikirk, A. Srinivasan, A. Tang, K. Sadra, Y.C. Shih, and B. G. Streetman, "Real time flux monitoring and feedback control of a valved arsenic source" Twelfth North American Conference on Molecular Beam Epitaxy, Ottawa, Canada, Oct. 12-14, 1992.

17. Y.C. Shih, D. P. Neikirk, and B. G. Streetman, "Effects of As flux on Si δ -doped GaAs," Twelfth North American Conference on Molecular Beam Epitaxy, Ottawa, Canada, Oct. 12-14, 1992.

18. Y. Kim and D. P. Neikirk, "Monolithically integrated optically interrogated pressure microsensor," **J. Acoust. Soc. Am.**, Vol. 92, No. 4 (pt. 2), October 1992, p. 2353.

19. O. Hartin, D. P. Neikirk, A. Anselm, and B. Streetman, "Memory Switching Simulation in Resonant Tunneling Devices," 1997 American Physical Society March Meeting, Kansas City, MO, March 17-21, Bulletin of the American Physical Society, Vol. 42, No. 1, 1997, p. 548.

20. O. Hartin and D. P. Neikirk, "Tight Binding Simulation of Memory Switching in Resonant Tunneling Devices," 1997 American Physical Society International Conference on Computational Physics, University of California, Santa Cruz, Aug. 25, 1997.

21. D. Neikirk, "Embedded Passive Sensors for State Monitoring," presented at NSF Workshop on Exploring the Uses of Autoadaptive Media in Geotechnical Earthquake Engineering, Austin, TX, January 10-12 2001.

22. Lavigne, John J.; Savoy, Steve; Best, Michael; Anslyn, Eric V.; Shear, Jason B.; McDevitt, John T.; Neikirk, Dean, "Toward the development of an 'electronic tongue'," Book of Abstracts, 219th ACS National Meeting, San Francisco, CA, March 26-30, 2000 (2000), AGFD-193.

23. Wood, Sharon; Neikirk, Dean, "Development of a passive sensor to detect cracks in welded steel construction," US-Japan Joint Workshop and Third Grantees Meeting, US-Japan Cooperative Research in Urban Earthquake Disaster Mitigation, Monbu-Kgagku-sho and The National Science Foundation, Seattle, August 15-16, 2001.

24. McCleskey, Shawn C.; Goodey, Adrian P.; Rodriguez, Marc D.; McDevitt, John T.; Anslyn, Eric V.; Neikirk, Dean P., "Development of a multi-component sensor array for the simultaneous detection of various analytes in solution," Abstracts of Papers, 222nd ACS National Meeting, Chicago, IL, United States, August 26-30, 2001.

D. Other Major Publications

V. Kesan and D. P. Neikirk, "Quantum Well Devices," **Microwaves and RF**, vol. 25, July 1986, pp. 93-97.

D. P. Neikirk, P. Cheung, M.S. Islam, and T. Itoh, "Optically Controlled Coplanar Waveguide Phase Shifters," **Microwave Journal**, Dec. 1989, pp. 77-88.

D. P. Neikirk, "Quantum Wells and Other Deep Subjects," **Discovery**, Vol. 11, No. 3, 1989, pp. 5-8.

S. M. Wentworth, J. M. Lewis, and D. P. Neikirk, "Antenna-Coupled Thermal Detectors of mm-Wave Radiation," **Microwave Journal**, Jan. 1993, pp. 94-103.

E. Book Chapter

D. B. Rutledge, D. P. Neikirk, and D. Kasilingam "Integrated- Circuit Antennas," in **Infrared and Millimeter Waves**, vol. 11, editor K.J. Button, 1984.

Nicolaos Christodoulides, Priya Dharshan, Jorge Wong, Pierre N. Floriano, Dean Neikirk and John T. McDevitt, "A Microchip-Based Assay for Interleukin-6," In: *Methods in Molecular Biology*, Volume 385: Microchip-Based Assay Systems, Humana Press, ISBN 978-1-58829-588-0 (Print) 978-1-59745-426-1 (Online), Copyright 2008, pages 131-144.

F. Technical Reports

C-K Tzuang, D. P. Neikirk, and T. Itoh, "Finite Element Analysis of Slow-Wave Schottky Contact Printed Lines," Microwave Laboratory Report No. 87-P-2, AFOSR Grant 86-0036, Feb., 1987.

D. P. Neikirk and T. Itoh, "Monolithic Phase Shifter Study," Microwave Laboratory Report No. 87-P-3, AFOSR Grant 86-0036, Jan., 1987.

V. P. Kesan and D. P. Neikirk, "Quantum Well Devices," Electrical Engineering Research Laboratory Report No. 87-P-8, Joint Services Electronics Program Research Contract AFOSR F49620-86-C-0045, August 7, 1987.

Stuart M. Wentworth and D. P. Neikirk, "High Frequency Characteristics of Tape Automated Bonding (TAB) Interconnects," Microwave Laboratory Report No. 87-P-7, August 26, 1987.

Stuart M. Wentworth and D. P. Neikirk, "Characterization of Tape Automated Bonding (TAB) Interconnects at High Frequency ," Microwave Laboratory Report No. 87-P-9, October 23, 1987.

D. P. Neikirk and T. Itoh, "Monolithic Phase Shifter Study," Microwave Laboratory Report No. 90-P-1, Final Technical Report for AFOSR Grant 86-0036, Feb., 1990.

A. Mortazawi, D. Neikirk, and T. Itoh, "Microwave and millimeter wave oscillators and planar power combining structures for QWITT and Gunn diodes," Microwave Laboratory Report No. 90-P-4, Technical Report for ARO Grant DAAL03-88-K-0005 and JSEP Grant F49620-89-0044, Aug., 1990.

Oral Presentations

A. Professional Society Presentation

D. B. Rutledge and D. P. Neikirk, "Imaging Antenna Arrays," Invited Keynote Speakers, Sixth International Conference on Infrared and Millimeter Waves, Miami, Fl., Dec. 7-12, 1981.

D. P. Neikirk and D. B. Rutledge, "Advances in Microbolometers," Invited Keynote Speakers, Eighth International Conference on Infrared and Millimeter Waves, Miami, Fl., Dec. 12-17, 1983.

D. P. Neikirk, "Optically Controlled Coplanar Waveguide Millimeter Wave Phase Shifter," Tenth International Conference on Infrared and Millimeter Waves, Lake Buena Vista, Fl., Dec. 9-13, 1985.

D. P. Neikirk, "Picosecond Response of an Optically Controlled Millimeterwave Phase Shifter," Second Topical Meeting on Picosecond Electronics and Optoelectronics, Jan., 1987.

D. P. Neikirk, "Influence of Transit Time Effects on the Optimum Design and Maximum Oscillation Frequency of Quantum Well Oscillators," 12th International Conference on Infrared and Millimeter Waves, Dec. 14-18, 1987.

D. P. Neikirk, "Measurements of an Optically Controlled Coplanar Waveguide Phase-Shifter," 12th International Conference on Infrared and Millimeter Waves, Dec. 14-18, 1987.

D. P. Neikirk, "High Frequency Characterization of Tape-Automated Bonding Interconnects," 5th Annual Texas Regional Symposium, International Society of Hybrid Manufacturing, April 11, 1988.

D. P. Neikirk, "Time Dependent Simulation of the Quantum Well Injection Transit Time Diode," 13th International Conference on Infrared and Millimeter Waves, Dec. 5-9, 1988.

D. P. Neikirk, "Experimental Performance of a Periodically Illuminated Optically Controlled Coplanar Waveguide Phase Shifter," 13th International Conference on Infrared and Millimeter Waves, Dec. 5-9, 1988.

B. Invited Lectures

1. D. P. Neikirk, "Exotic Heterojunction Devices for Microwave Circuits," NSF Workshop on Future Research Opportunities in Electromagnetics, Arlington, TX., January 29-31, 1986.
2. D. P. Neikirk, "Optical Control of a Monolithic Millimeter Phase Shifter," ARO Workshop on Fundamental Issues in Millimeter and Submillimeter Waves, Los Angeles, Ca., Sept. 15-16, 1986.
3. Dean P. Neikirk, "Quantum Well Oscillators for Millimeter Wave Applications," 1987 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), Hilton Head Island, S.C., March 2-4, 1987.
4. S.M. Wentworth and D. P. Neikirk, "High Frequency Tape-Automated Bonding (TAB) Interconnect Characterization," IEEE 6th Annual VLSI and GaAs Packaging Workshop, Sept. 14-16, 1987.
5. D. P. Neikirk, "The quantum well injection transit time diode," Engineering Foundation Conference on Advanced Heterostructure Transistors, Keauhou-Kona, Hawaii, Dec. 5-10, 1988.
6. D. P. Neikirk, "The High Frequency Characteristics of Tape Automated Bonding (TAB) Interconnects," presented to the Microelectronics and Computer Technology Corporation, April 19, 1989.
7. Dean P. Neikirk, "Impedance measurements of quantum well diodes for millimeter wave applications," 1990 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), San Francisco, CA., Feb. 12-14, 1990.
8. Dean P. Neikirk, "Twin-slot multi-layer substrate-supported antennas and detectors for terahertz imaging," First International Symposium on Space Terahertz Technology, University of Michigan, Ann Arbor, Mich., March 5-6, 1990.
9. Dean P. Neikirk, "Microwave and Millimeterwave Oscillators using Quantum Well Diodes," Joint IEEE MTT/ED Dallas Chapter meeting, Sept. 27, 1990.
10. Dean P. Neikirk, "Quantum Transport Simulations of Resonant Tunneling Diodes," 1991 Workshop on Compound Semiconductor Microwave Materials and Devices (WOCSEMMAD), Ft. Lauderdale, FL., Feb. 18-20, 1991.

11. Dean P. Neikirk, "The Application of Physics in Electrical Engineering (or is it Engineering in Physics?): Electromagnetics in Very High Frequency Semiconductor Devices," Physics Colloquium, Oklahoma State University, March 5, 1992.
12. D. P. Neikirk and B. G. Streetman, "MBE growth of multilayer heterostructures for photonic and high-speed electronic devices," Engineering Foundation Conference on High Speed Optoelectronic Devices and Circuits II, Banff, Alberta, Canada, Aug. 9-13, 1992.
13. L. T. Pillage, D. P. Neikirk, and R. Mercer, "Design automation techniques and algorithms for application specific electronic modules (ASEMs)," ARPA Electronic Packaging & Interconnect Principle Investigator Meeting, Marina del Ray, CA, Feb. 14-18, 1994.
14. D. P. Neikirk, "Micro-sensors - What happens when you make classical devices small?: Integrated Bolometric Radiation Detectors," Texas Instruments, Dallas, Texas, Oct. 20, 1994.
15. Dean P. Neikirk, "Micromachined sensors," Motorola Sensors Steering Committee, Albuquerque, New Mexico, March 28, 1995.
16. D. P. Neikirk, E. Tuncer, and B.-T. Lee, "The Use of Effective Internal Impedance Approximations in Lossy Transmission Line Modeling," *Progress in Electromagnetics Research Symposium PIERS 95*, The University of Washington, Seattle, Washington, July 28, 1995.
17. D. P. Neikirk, M. S. Islam, and E. Tuncer, "Accurate Quasi-Static Modeling of Transmission Lines on Semiconducting Substrates," *Progress in Electromagnetics Research Symposium PIERS 95*, The University of Washington, Seattle, Washington, July 28, 1995.
18. D. P. Neikirk, "Impact of Finite Metal Conductivity on Inductance Extraction of Interconnects and Packages," Sematech meeting on Electrical Modeling Challenges Faced by Packaging Designers, Austin, Texas, Nov. 19, 1995.
19. D. P. Neikirk, "Micromachined Fabry-Perot Pressure Transducers," Hughes Research Laboratory, Malibu, California, Nov. 21, 1995.
20. D. P. Neikirk, "Classical Devices Made Small; or 'What's the big deal about little machines?'"', Manufacturing 2000, University of Texas at Austin, Feb. 23, 1996.
21. D. P. Neikirk, "Interconnect Inductance Modeling from DC to the Skin Effect Limit," Quad Designs, Camarillo, CA, July 10, 1996.
22. D. P. Neikirk, "Efficient Conductor Boundary Conditions in the dc to Skin Effect Limit," DARPA MAFET Program Review, Fairfax, VA, Oct. 27-31, 1997.

23. Micromachined Array-based Multi-analyte Chemical Sensors: Towards the Fabrication of an "Electronic Tongue" South, Texas Local Section of The Electrochemical Society Meeting, April 17, 1999.

24. D. P. Neikirk, "Resonant Chemical Surveillance Tags," IEEE Electron Device Chapter, Central Texas Section, September 25, 2008.

25. D.P. Neikirk, "Near Borehole Condition Sensing," Nanotechnology Conference and Trade Show - Nanotech 2009, Houston, TX May 3-7, 2009, Nanotech & Cleantech for Oil & Gas Session, (Session chair: Sean Murphy, Advanced Energy Consortium), May 5, 2009.

26. D.P. Neikirk, "Integrated Threshold Nanosensor Systems," Advanced Oil Consortium Microfabricated Sensors Workshop, Houston Research Center, Bureau of Economic Geology, University of Texas at Austin, September 8th-9th, 2010.

27. D. P. Neikirk, "Sensing systems for "harsh" environments," Engineering Challenges for Deepwater Drilling at the "U.S. Offshore Oil Exploration: Managing Risks to Move Forward," James A. Baker III Institute for Public Policy and PFC Energy, Rice University, Houston, TX, February 11, 2011.

C. Other Conference Presentations

Praveen Pasupathy, Mingxiang Zhuzhou, Shasi K. Munukutla, Dean P. Neikirk, and Sharon L. Wood, "Resonant Wireless Sensor Nets for Civil Infrastructure Health Monitoring," 2009 National Science Foundation Division of Civil, Mechanical and Manufacturing Innovation (CMMI) Engineering Research and Innovation Conference, Honolulu, Hawaii, June 22-25, 2009.

Technical Consulting

Teltech Resource Network (1985-1993)
Ardex, Inc. (1986-88)
University and Polytechnic Grants Committee, Consultancy to examine Equipment Requirements for the Hong Kong University of Science and Technology, July, 1989
E. P. Hamilton Associates, (1987-90)
Burnett Company, Microwave Heating for Secondary Oil Recovery, July, 1990
Microelectronics and Computer Technology Corporation, June, 1990
Microelectronics and Computer Technology Corporation, Oct., 1994 - Sept., 1996
Baker-Hughes

University Committee Assignments

Departmental:

Graduate Student Financial Aid, Sept. 1984- Sept. 1987
Faculty Recruiting, Sept. 1984- Aug. 1985
Microelectronics Jr. Faculty Recruiting, Sept. 1985- Sept. 1987 (chairman)
ECE Safety Committee, Sept. 1985- Aug. 1993 (chairman, 1985-89)
ECE Electronics Shop Coordinating Committee, March 1986- Aug. 1993
Solid State Electronics Area Graduate Advisor, Aug. 1986- Aug. 89
ECE Space Allocation Committee, Sept. 1989-Aug. 1993 (chairman)
ECE Facilities Committee, Sept. 1993- Aug. 1996 (chairman)
ECE Areas Committee, Electromagnetics/Acoustics, Sept. 1993-present
ECE Ad Hoc Committee to Review the Undergraduate Curriculum, Jan. 1995- Aug. 1995
ECE World Wide Web Home Page Committee, Sept. 1995-Aug. 1996
ECE Ad Hoc Committee to Review the Undergraduate Curriculum, Jan. 1997- Aug. 1997
ECE Areas Committee, Materials and Quantum Electronics, Sept. 1993-present; chairman, Sept. 1996-present
Chair of ECE Graduate Studies Committee, May 1998-August 2006
ECE Chair's council, November 1999-2010
ECE Graduate Advisor, Sept. 1999- 2010
ECE Associate Chair, Sept. 2001-Dec. 2010
ECE peer Faculty Annual Review Committee, Sept. 2012-Aug. 2013

College:

Engineering Scholastic Appeals, Sept. 1984- Aug. 1985
Engineering Safety Committee, Sept. 1985- Aug. 1994 (chairman, Sept. 1989-Aug. 1994)

Aerospace Engineering Machine Shop, Sept. 1989-Aug. 1993
College Annual Report Quality Team, Jan. 1994- Aug. 1994
College Multimedia Committee, Sept. 1995-Aug. 2000
Equal Opportunity in Engineering (EOE) Program, 1995-Dec. 1996
Graduate Fellowship Review Committee, Sept. 2011-Aug. 2013

University:

Presidential Ad Hoc Committee on Research Infrastructure Enhancement, Jan. 1988 - Aug. 1994
Research Safety Advisory Committee, Oct. 1991-present (chairman, Sept. 1996-1999)
Ad Hoc Consultative Committee for the Selection of a Dean of the College of Engineering, Nov. 1995-May 1996
Faculty Building Advisory Committee, Sept. 1995-Aug. 2000; Aug. 2003-Aug. 2004
Ad Hoc Project Committee for Parking Garage # 4A, Sept. 1996-Aug. 2000
Faculty Council, Sept. 1996-Aug. 2000; Sept. 2002 - Aug. 2004
Faculty Advisory Committee on the Budget, Sept. 99 - Aug. 2000; Sept. 2008 – Aug. 2011 (vice chair Sept. 2009- Aug. 2010)
Graduate Assembly, April 1997- Aug. 2000; Sept. 2001 - Aug. 2008
Administrative sub-committee of GA, Sept. 1997-Aug. 1998; Sept. 2006-Aug. 2007
Academic sub-committee of GA, Sept. 1998-Aug. 2000; Sept. 2001-Aug. 2006; Sept. 2007-Aug. 2008
Chair, Graduate Assembly, 2004-2005
Academy of Distinguished Teachers selection committee, academic year 1999-2000
Outstanding Graduate Adviser selection committee, academic year 1999-2000
Outstanding Graduate Coordinator selection committee, academic year 1999-2000
Faculty Council, Sept. 2008 – Aug. 2012; Chair-elect Sept. 2009- Aug. 2010; Chair Sept. 2010- Aug. 2011; past chair: Sept. 2011-Aug. 2012
Faculty Council Executive Committee, Sept. 2009 – Aug. 2012
General Faculty Rules and Governance Committee, Sept. 2010 – Aug. 2015 (Chair, Sept. 2011 – Aug. 2013)
Ad Hoc Consultative Committee for the Selection of a Dean of the Graduate School, Nov. 2012 – Sept. 2012
Secretary of the General Faculty and Faculty Council, Sept. 2013 – Aug. 2015
Committee on Undergraduate Degree Program review, Sept. 2013 – Aug. 2015
Faculty Council Executive Committee, Sept. 2013 – Aug. 2015
Faculty Committee on Committees, *ex officio* member, Sept. 2013 – Aug. 2015

UT System:

Task Force on Doctoral Programs and Post-Doctoral Experience, Spring-Fall 2006

University of Texas System Faculty Advisory Council, Sept. 2009- Aug. 2011

State of Texas:

Texas Higher Education Coordinating Board Graduate Education Advisory Committee (GEAC), September 1, 2015 - August 31, 2018.

Evidence of Teaching Effectiveness

Senior Design Projects:

Umer Yousafzai and Venuka Jayatilaka, Spring 1994

Chris Eiting and Sonny Gonzalez, Spring 1994

David Lee and David Onsongo, Fall 1996

Dave Pyle and Aruna Murthy, Spring 1999

Hitesh Mehta and Edward Zhu, Spring 1999, "Giving the electronic tongue a sense of good taste: image analysis tools and GUI"

Gus Espinosa and Donnie Garcia, Spring 1999, "Design and Implementation of a Computer Interfacing Circuit to Control LED's for use with a Chemical Sensor"

Natthanant Pon Skulkaew and Prem Nainani, Spring 2001, "PC-based data acquisition and wireless transmission system"

Matthew Andringa and Allen Hall, Spring 2001, "Non-Invasive RFID Weld Inspection"

Michael Amalfitano and Sapun Parekh, Spring 2002, "Output circuitry for a transmitter used in an Electronic Structural Surveillance system"

Kunal Patel and Jacy Little, Spring 2002, "Swept, high frequency oscillator to work in an Electronic Structural Surveillance (ESS) system"

Dong Pak, Spring 2002, "Automated image-processing software of an electronic chemical sensor"

Rajesh Nerlikar, Jonathan Solomon, Spring 2003, "Wireless Data Acquisition System for Bluetooth-enabled RFID Readers"

Nola Li, Judith Chen, Maria Huang, Fall 2003, "Design and build a tuning network for a swept frequency reader used in structural health analysis"

Tuenlap (Daniel) Chan, Imranul Islam, Derek Choi, Spring 2004, "Design and build an RFID Interrogator Receiver"

John McKee and Terence Man, Spring 2007, "Improved Corrosion Sensors"

Abdulaziz Beayeyz , Sravan Bhagavatula, Rahul Mitra, Shasi Munukutla, Spyder Spann, Fall 2009, "Portable Corrosion Detector"

Jonathan Pham, Po-Han Wu, Josh Schulte, Pritesh Solanki, Mesele Bedasa, Spring 2011- Fall 2011, "Multi-Sensor Robotics Platform"

Raymund Lee, Simon Chow, Connor Landy, Kevin Woo, and Anirudh Kashyap, Fall 2012-Spring 2013, "Variable Frequency RFID Tag and Reader"

Javier Chacon, Joshua Poncik, Joshua Orozco, Sebastian Salomon, Yongcong Zou, Fall 2013-Spring 2014, "Environmental Sensor Monitoring Network"

Organized Classes Taught:

EE 363M Introduction to Microwaves, Spring 1984, # 16455
EE 396K VLSI Fabrication Techniques, Fall 1984, # 16255
EE 379K Integrated Circuit Fabrication, Spring 1985, # 16055
EE 396K VLSI Fabrication Techniques, Fall 1985, # 16275
EE 379K Integrated Circuit Fabrication, Fall 1985, # 16070
EE 396K VLSI Fabrication Techniques, Spring 1986, # 17680
EE 379K Integrated Circuit Fabrication, Spring 1986, # 17450
EE 396K VLSI Fabrication Techniques, Fall 1986, # 15245
EE 379K Integrated Circuit Fabrication, Fall 1986, # 15020
EE 396K VLSI Fabrication Techniques, Spring 1987, # 15205
EE 379K Integrated Circuit Fabrication, Spring 1987, # 14970
EE 396K VLSI Fabrication Techniques, Fall 1987, # 15010
EE 440 Integrated Circuit Fabrication, Fall 1987, # 14545
EE 363M Introduction to Microwaves, Spring 1988, # 14535
EE 396K VLSI Fabrication Techniques, Spring 1988, # 14865
EE 440 Integrated Circuit Fabrication, Spring 1988, # 14390
EE 396K VLSI Fabrication Techniques, Fall 1988, # 15165
EE 440 Integrated Circuit Fabrication, Fall 1988, # 14705
EE 363M Introduction to Microwaves, Spring 1989, # 14525
EE 396K VLSI Fabrication Techniques, Spring 1989, # 14855
EE 396K VLSI Fabrication Techniques, Fall 1989, # 15165
EE 440 Integrated Circuit Fabrication, Fall 1989, # 14705
EE 363M Introduction to Microwaves, Spring 1990, # 14050
EE 396K VLSI Fabrication Techniques, Spring 1990, # 14355, 14360
EE 440 Integrated Circuit Fabrication, Spring 1990, # 13915, 13920
EE 396K VLSI Fabrication Techniques, Fall 1990, # 14630, 14635
EE 440 Integrated Circuit Fabrication, Fall 1990, # 14200, 14205
EE 363M Introduction to Microwaves, Spring 1991, # 14365
EE 396K VLSI Fabrication Techniques, Spring 1991, # 14660, 14665, 14670
EE 440 Integrated Circuit Fabrication, Spring 1991, # 14220, 14225, 14230
EE 396K VLSI Fabrication Techniques, Fall 1991, # 14865, 14860
EE 440 Integrated Circuit Fabrication, Fall 1991, # 14425, 14430
EE 363M Introduction to Microwaves, Spring 1992, # 14270
EE 396K VLSI Fabrication Techniques, Spring 1992, # 14545, 14550, 14555
EE 440 Integrated Circuit Fabrication, Spring 1992, # 14130, 14135
EE 396K VLSI Fabrication Techniques, Fall 1992, # 15095, 15100, 15105
EE 440 Integrated Circuit Fabrication, Fall 1992, # 14670, 14675
EE 397K Microwave Devices, Spring 1993, # 14805
EE 396K VLSI Fabrication Techniques, Fall 1993, # 14800, 14805, 14810
EE 440 Integrated Circuit Fabrication, Fall 1993, # 14385, 14390
EE 363M Introduction to Microwaves, Spring 1994, # 14370
EE 396K VLSI Fabrication Techniques, Fall 1994, # 14365

EE 440 Integrated Circuit Fabrication, Fall 1994, # 13870
 EE 397K Electromagnetics in Packaging, Spring 1995, # 14555
 EE 396K VLSI Fabrication Techniques, Fall 1995, # 14765
 EE 440 Integrated Circuit Fabrication, Fall 1995, # 14260
 EE 397K Electromagnetics in Packaging, Spring 1996, # 14695
 EE 382M Simulation Methods in CAD/VLSI, Spring 1996, # 14500
 EE 396K VLSI Fabrication Techniques, Fall 1996, # 14535
 EE 440 Integrated Circuit Fabrication, Fall 1996, # 14090
 EE 382M Simulation Methods in CAD/VLSI, Spring 1997, # 14325
 EE 363M Introduction to Microwaves, Spring 1997, # 14120
 EE 396K VLSI Fabrication Techniques, Fall 1997, # 15315
 EE 440 Integrated Circuit Fabrication, Fall 1997, # 14820
 EE 363M Introduction to Microwaves, Spring 1998, # 14530
 EE 397K Microwave Devices, Spring 1998, # 14950
 EE 396K VLSI Fabrication Techniques, Fall 1998, # 15475
 EE 440 Integrated Circuit Fabrication, Fall 1998, # 14965
 EE 363M Introduction to Microwaves, Spring 1999, # 14825
 EE 397K Microwave Devices, Spring 1999, # 15260
 EE 396K VLSI Fabrication Techniques, Fall 1999, # 15340
 EE 440 Integrated Circuit Fabrication, Fall 1999, # 14820
 EE 363M Introduction to Microwaves, Spring 2000, # 14755
 EE 396K VLSI Fabrication Techniques, Fall 2000, # 15600
 EE 440 Integrated Circuit Fabrication, Fall 2000, # 15100
 EE 397K Micro-electromechanical Systems (MEMS), Spring 2001, #15170
 EE 396K VLSI Fabrication Techniques, Fall 2001, # 15725
 EE 440 Integrated Circuit Fabrication, Fall 2001, # 15230
 EE 397K Micro-electromechanical Systems (MEMS), Spring 2002, #15330
 EE 396K VLSI Fabrication Techniques, Fall 2002, # 16050
 EE 440 Integrated Circuit Fabrication, Fall 2002, # 15485
 EE 397K Microwave Devices, Spring 2003, # 15110
 EE 396K VLSI Fabrication Techniques, Fall 2003, # 15580
 EE 440 Integrated Circuit Fabrication, Fall 2003, # 15095
 EE 325 Electromagnetic Engineering, Spring 2004, # 14345
 EE 396K VLSI Fabrication Techniques, Fall 2004, # 16250
 EE 440 Integrated Circuit Fabrication, Fall 2004, # 15715
 EE 396K 26-Microelectromechanical Systems, Spring 2005, # 15690
 EE 396K VLSI Fabrication Techniques, Fall 2005, # 16455
 EE 440 Integrated Circuit Fabrication, Fall 2005, # 15930
 EE 396K VLSI Fabrication Techniques, Fall 2006, # 17040
 EE 440 Integrated Circuit Fabrication, Fall 2006, # 16430
 EE 325 Electromagnetic Engineering, Spring 2007, # 15765
 EE 396K VLSI Fabrication Techniques, Fall 2007, # 17425
 EE 440 Integrated Circuit Fabrication, Fall 2007, # 16770
 EE 396K-26 Microelectromechanical Systems, Spring 2008, # 16815
 EE 396K VLSI Fabrication Techniques, Fall 2008, # 17380
 EE 325 Electromagnetic Engineering, Spring 2009, # 16000

EE 396K-24 Microwave Devices, Spring 2010, # 16975
 EE 396K VLSI Fabrication Techniques, Fall 2010, # 17075, 17080, 17085, 17090
 EE 440 Integrated Circuit Fabrication, Fall 2010, # 16540, 16545, 16550, 16555
 EE 396K VLSI Fabrication Techniques, Fall 2011, # 17295, 17300, 17305, 17310
 EE 440 Integrated Circuit Fabrication, Fall 2011# 16760, 16765, 16770, 16775
 EE 396K 26-Microelectromechanical Systems, Spring 2012, #17070
 EE 396K VLSI Fabrication Techniques, Fall 2012, # 17185, 17190, 17195, 17200
 EE 440 Integrated Circuit Fabrication, Fall 2012, # 16640, 16645, 16650, 16665
 EE 363M Introduction to Microwaves, Spring 2013, # 16605
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2013, # 17425, 17430, 17435, 17440
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2013, # 16790, 16795, 16800, 16805
 EE 396K-24 Microwave Devices. Spring 2014, #17440
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2014, #17525, 17530, 17535, 17540
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2014, #16960, 16965, 16970, 16975
 EE 363M Microwave and Radio Frequency Engineering, Spring 2015, #16355
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2015, #16965, 16970, 16975
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2015, #16480, 16485, 16490
 EE 363M Microwave and Radio Frequency Engineering, Spring 2016, #16550
 EE 396K Ultra Large Scale Integrated Circuit Fabrication Techniques, Fall 2016
 EE 440 Integrated Circuit Nanomanufacturing Techniques, Fall 2016
 EE 396K 26-Microelectromechanical Systems, Spring 2017
 EE 363M Microwave and Radio Frequency Engineering, Spring 2018, #15890

Continuing Education Courses Taught

"Microelectronics Fabrication - Chemical Aspects," with Isaac Trachtenberg,
 Continuing Engineering Studies, College of Engineering, The University of
 Texas at Austin, June 1-4, 1987.
 "Integrated Circuit Process & Design," with M. R. Mercer, Motorola short course,
 Continuing Engineering Studies, College of Engineering, The University of

Texas at Austin:

- Aug.-Sept., 1987
- Nov.-Dec., 1987
- Nov.-Dec., 1988
- March-April, 1989
- Aug.-Sept., 1989
- Nov.-Dec., 1989
- Feb.-March, 1990
- April, 1990
- Aug., 1990

"Integrated Circuit Processing and Design," with L. T. Pillage, Advanced Micro Devices short course, Continuing Engineering Studies, College of Engineering, The University of Texas at Austin:

- Oct.-Nov., 1990
- June-July, 1991

"Microelectronics Fabrication," for the Fellows of the Senior Service College Fellowship Program, Continuing Engineering Studies, College of Engineering, The University of Texas at Austin, yearly 1993-2003.

Cases: Dean P. Neikirk

Trial experience: five jury trials (Federal District Court); two ITC bench trials; two California State Court trials (trade secrets)

Expert reports: over 40

Depositions: over 30

1. Jan. 2003-June 2003: Vinson & Elkins, counsel for International Rectifier, Patent infringement case: Hitachi Ltd., et. al. v. International Rectifier

Corporation, in the United States District Court for the Central District of California, Case No. CV-02-0077-R; [no testimony or depositions]

Semiconductor / IC processing

2. August 2003-August 2004: Wilmer Cutler Pickering Hale and Dorr LLP, counsel for Analog

Devices, patent infringement case: Motorola, Inc. v. Analog Devices, Inc. TX Eastern - Beaumont Civil Action No. 1:03-cv-131 (RHC); case settled [three depositions]

Semiconductor / IC processing

3. April 2004-March 2005: Fish & Richardson P.C., counsel for Micron, patent infringement case:

Micron Technology, Inc. adv. Motorola, Inc. USDC-W.D. TX (Austin) - Civil Action No. A04 CA 007; case settled [no testimony or depositions]

Semiconductor / IC processing

4. Jan 2004- July 2004: Howrey Simon Arnold & White, counsel for ASM in patent litigation with Applied Materials; case settled [no testimony or depositions]

Semiconductor processing equipment

5. May 2004-Dec. 2006: Vinson & Elkins, counsel for Advanced Micro Devices, patent infringement case: Advanced Micro Devices, Inc. v Oki America, Inc., et al.

Originally TX Eastern District Marshall, Civil action No. 2:03-CV-373, transferred to Northern California; case settled [depositions and expert reports]

Semiconductor / IC processing

6. April 2004-May 2006: Fish & Richardson P.C., counsel for AVID Identification Systems, patent

infringement case: Avid v. Crystal Import Corporation, et al., USDC-EDTX Marshall Div. Case No. 2:04-cv-183; [depositions and expert reports; jury trial May 2006]

RFID

7. November 2005 – 2006: Keker & Van Nest, LLP, counsel for Intel, patent infringement case:

Ohmi v. Intel Corp., et al.- 2:05CV-209 TJW [no testimony or depositions].

Semiconductor / IC processing

8. July 2006 – March 2007: Fish & Richardson P.C., counsel for Applied Materials, patent

infringement case: Semiconductor / IC processing SEZ Holdings AG, et al. vs. Applied Materials, Inc. USDC-D. Del. - C.A. No. 05-552-SL; case settled [expert report submitted, otherwise no

depositions or testimony]; case settled

Semiconductor / IC processing

9. July 2006 – May 2007: Kenyon & Kenyon, counsel for FCI; patent infringement case: FCI USA, Inc. v. Tyco Electronics, Case No. 2:06cv128; case settled [no testimony or depositions]

Printed circuit board connector design

10. January 2007 – Dec. 2007: Vinson & Elkins, counsel for Lutron Electronics Co., Inc. in ITC matter Lutron Electronics Co. vs. Leviton Manufacturing Co., Inc., United States International Trade Commission, Honorable Carl C. Charneski, Investigation No. 337-TA-599, In the matter of certain lighting control devices including dimmer switches and/or switches and parts thereof. [no testimony or depositions]; case closed

RF lighting controls

11. February 2007 – Dec. 2007: LATHAM & WATKINS LLP counsel for FLIR Systems, Inc and Indigo Systems Corp. (plaintiff) v. William Parrish, E. Timothy Fitzgibbons, Superior Court of the State of California, County of Santa Barbara, case no. 1220581. [expert report, deposition; trial testimony]

Infrared sensors

12. May 2007 – Feb. 2008: Vinson & Elkins L.L.P., on behalf of Silicon Labs ("SiLabs") in connection with Analog Devices, Inc., Plaintiff, v. Silicon Laboratories, Inc., Defendant, United States District Court, District of Massachusetts, Civil Action No. 06-12240 (WGY) [expert reports, deposition]; case settled

Digital isolators

13. November 2006 – January 2010: Jones Day, counsel for Sercel, Input/Output, Inc., et al. v. Sercel, Inc., Case No. 5:06-CV-236-DF/CMC, [deposition; trial testimony (jury trial)]; trial January 2010, July 2010.

MEMS sensors and fabrication

14. February 2007 – Dec 2008: Vinson & Elkins, counsel for Lutron Electronics Co., Inc. in *Lutron Electronics Co., Inc. vs. CONTROL4 Corp. Case No. 2:06-CV-00401 DAK, US District Court, District of Utah* ; case settled [deposition].

RF lighting controls

15. June 2007 – July 2011: Kirkland & Ellis LLP, counsel for AVID, in Allflex USA, Inc. v. AVID Identification Systems, Inc., UNITED STATES DISTRICT COURT CENTRAL DISTRICT OF CALIFORNIA Case No. EDCV-06-1109-SGL (OPx) [declaration, expert report]

RFID

16. January 2008 – May 2009: Gibbs & Bruns, L.L.P., counsel for LONESTAR INVENTIONS, L.P., Plaintiff, v. NINTENDO OF AMERICA, INC., Defendant, UNITED STATES DISTRICT COURT FOR THE EASTERN DISTRICT OF TEXAS, TYLER DIVISION, CASE NO. 6:07-CV-261-LED; case settled [deposition].

Semiconductor devices.

17. May 2008 – Dec 2009: Heller Ehrman LLP, counsel for Maxim Integrated Products, Inc. v. Freescale Semiconductor, Inc., United States District Court, Northern District of California, Case No.: 3:08-cv-00979-BZ [no depositions or testimony]
Semiconductor / IC processing / electronic packaging

18. January 2008 – November 2008: Gibbs & Bruns, L.L.P., counsel for LONESTAR INVENTIONS, L.P., Plaintiff, v. SANDISK CORPORATION, Defendant, UNITED STATES DISTRICT COURT FOR THE EASTERN DISTRICT OF TEXAS, TYLER DIVISION, CASE NO. 6:07-CV-374; LONESTAR INVENTIONS, L.P., Plaintiff, v. XILINX, INC., Defendant, UNITED STATES DISTRICT COURT FOR THE EASTERN DISTRICT OF TEXAS, TYLER DIVISION, CASE NO. 6:07-CV-0393-LED. Case settled.
Semiconductor devices.

19. November 2008 – April 2009: Wilson Sonsini Goodrich & Rosati, counsel for Luna Innovations, Incorporated, in Hansen Medical, Inc. v. Luna Innovations, Incorporated, Superior Court of the State of California County of Santa Clara Case No. 107 CV 088551.[expert report; deposition; trial testimony]
Optical devices.

20. February 2009 – Dec 2009: Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P., Fish & Richardson P.C., Howrey LLP, Kenyon & Kenyon, LLP, and Hartline, Dacus, Barger, Dreyer & Kern, L.L.P. (collectively, “Defendants’ Counsel”) representing Audi/VW, BMW, Hyundai/Kia, Isuzu, Nissan, Porsche, and Subaru (collectively, the “Defendant Companies”) in MHL TEK, LLC v. Nissan Motor Company, et al., Civil Action No. 2:07-cv-00289, U.S. District Court for the Eastern District of Texas. Summary judgment of non-infringement [two expert reports; one deposition]
Pressure sensors

21. January 2010 – April 2010: King & Spalding LLP, counsel for Spansion in Complaint in United States International Trade Commission Investigation No. 337-TA-664, respondents Samsung, Apple, Hon Hai Precision Industry, Asus, Kingston, Lenovo, PNY, Research In Motion, Sony, Beijing SE Putian Mobile Communication Co, Transcend, Verbatim. [one deposition]
Semiconductor devices.

22. December 2010-April 2011: Thompson & Knight LLP, counsel for STMicroelectronics, Inc. (ST) in ST v. Avago, Civil Action No. 3:10-cv-1460, United States District Court, Northern District of Texas, Dallas Division.
Semiconductor devices.

23. October 2010-June 2011: McDermott Will & Emery, counsel for Spansion in Spansion LLC v. Samsung Electronics Co. Civil Action No. 08-855 (D. Del.).
[Case settled]
Semiconductor devices.

24. October 2010-June 2011: McDermott Will & Emery, counsel for Spansion in Spansion, LLC, et al. v. Samsung Electronics Co., et al., Civil Action Nos. 3:10-cv-453 and 3:10-cv-685 (W.D. Wisc.).

[Case settled]

Semiconductor devices.

25. June 2007-July 2011: Kirkland & Ellis LLP, counsel for AVID in Allflex USA, Inc. v. AVID Identification Systems, Inc., UNITED STATES DISTRICT COURT CENTRAL DISTRICT OF CALIFORNIA Case No. EDCV-06-1109-SGL (OPx) [expert reports]

[Case settled]

RFID tags.

26. August 2011- September 2011: Patterson & Sheridan, LLP, counsel for Silicon Laboratories, Case No. 1:10-cv-0607-LY; Silicon Laboratories, Inc. v. Airoha Technology Corp.; In the United States District Court for the Western District of Texas

[case settled]

Semiconductor devices.

27. March-April 2012-: Fish & Richardson P.C., counsel for Cypress Semiconductor Corporation in Commonwealth Research Group, LLC v. Microchip Technology Incorporated, et al., USDC-D. Del. – C.A. No. 11-655-RGA

[case closed]

Semiconductor devices.

28. September 2010 – December 2013: Vinson & Elkins and Hatch, James, & Dodge, counsel for Lutron Electronics Co., Inc. in *Lutron v. Crestron, et al.*, Case No. 2:09cv707, pending in the United States District Court for Utah; [expert reports; two depositions].

[case settled]

RF lighting controls

29. March 2011-August 2012: SNR Denton US LLP, counsel for Kilopass Technology, Inc. in Kilopass Technology, Inc. v. Sidense Corporation -- Case No. 3:10-CV-02066-SI, Northern District of California (San Francisco Division). [three expert reports, one deposition]

[Summary judgment, case closed]

Semiconductor devices.

30. April 2011- August 2012: Alston & Bird counsel for X2Y Attenuators, LLC ("X2Y") in the Matter of CERTAIN MICROPROCESSORS, COMPONENTS THEREOF, AND PRODUCTS CONTAINING SAME, International Trade Commission Investigation No. 337-TA-781, X2Y v. Intel Corporation. [two expert reports; deposition; ITC trail August 2012]

Semiconductor packaging.

31. July 2012 – September 2013: Vinson & Elkins L.L.P. counsel for Silicon Laboratories, in SILICON LABORATORIES INC., Plaintiff, vs. MAXLINEAR, INC., Defendant Case No. 3:12CV1765-WQH-WVG UNITED STATES DISTRICT COURT SOUTHERN DISTRICT OF CALIFORNIA, SAN DIEGO. [expert report; deposition]

[case settled]

RF ICs

32. February 2012 – October 2013: Haynes and Boone, LLP, counsel for L-3, in L-3 COMMUNICATIONS CORPORATION, Plaintiff/Counterclaim Defendant, v. SONY CORPORATION, SONY ELECTRONICS INC. and SONY ERICSSON MOBILE COMMUNICATIONS (USA) INC., Defendants/Counterclaim Plaintiffs., C.A. No. 10-734-RGA IN THE UNITED STATES DISTRICT COURT FOR THE DISTRICT OF DELAWARE. [expert reports; depositions; jury trial October 2013]

Image sensors

33. February 2013-October 2013: McKool Smith, counsel for Ericsson, Inc., in the Matter of CERTAIN WIRELESS COMMUNICATIONS EQUIPMENT AND ARTICLES THEREIN, Investigation No. 337-TA-866 in UNITED STATES INTERNATIONAL TRADE COMMISSION. [expert reports; ITC trial October 2013]

Microwave amplifiers

34. January 2013-March 2013: Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P., counsel for Axis Communications AB and Axis Communications, Inc. in the case of patent infringement litigation and inter partes review proceedings, Network-I Security Solutions Inc. v. Alcatel-Lucent USA Inc., et al., No. 6:11-cv-00492-LED-JDL and Sony Corporation of America; Axis Communications AB; and Axis Communications, Inc. v. Patent of Network-I Security Solutions, Case IPR2013-00092. [case inactive pending IPR]

35. April 2013- August 2013: Alston & Bird LLP, counsel for AmTran, in the matter of Freescale v. Vizio (Defendants Amtran Technology Co., Ltd., Amtran Logistics, Inc., Vizio, Inc. , MediaTek, Inc., Zoran Corporation, CSR Technology, Inc. Sanyo Electric Co., Ltd., Sanyo North America Corporation, Sanyo Manufacturing Corporation, TPV Technology Limited TPV International (USA) Inc., Top Victory Electronics Co., Ltd., Envision Peripherals, Inc., Marvell Semiconductor, Inc.) Case No. A-12-CV-644-LY.

36. February 2013-February 2014: Quinn Emanuel, counsel for STMicroelectronics, in the matter of STMICROELECTRONICS, INC., Plaintiff, vs. INVENSENSE, INC., Defendant, UNITED STATES DISTRICT COURT NORTHERN DISTRICT OF CALIFORNIA SAN FRANCISCO DIVISION, CASE NO. 12-CV-2475-JSW [expert reports]

[case settled]

MEMS accelerometers

37. November 2012 – August, 2013: Haynes and Boone, LLP, counsel for Xilinx, Inc., in the matter of the Inter Partes Review of Patent 7,566,960 Title: INTERPOSING STRUCTURE, before the UNITED STATES PATENT AND TRADEMARK OFFICE BEFORE THE PATENT TRIAL AND APPEAL BOARD, INTELLECTUAL VENTURES MANAGEMENT, LLC, Petitioner, v. Patent of XILINX, INC., Patent Owner, Case IPR2012-00018. [expert report; deposition]

IC packaging

38. May 2014 – December 2014: Taylor Dunham and Rodriguez LLP, counsel for Andrew Katrinecz and David Byrd, in Civil Action No. 1:12-cv-235-LY, Andrew Katrinecz and David

Byrd v. Motorola Mobility LLC, in the United States District Court for the Western District of Texas, Austin Division, [expert reports, deposition] [expert report; deposition] [case settled].
Data entry devices

39. February 2015 – February 2016: Ropes & Gray, counsel for Samsung Electronics, in in Civil Action No. 4:14-cv-00371 (E.D. Tex.), Imperium IP Holdings (Cayman), Ltd. v. Samsung Electronics Co., Ltd., Samsung Electronics America, Inc., Samsung Telecommunications America, LLC, and Samsung Semiconductor, Inc. [expert report; deposition; jury trial]
Cell phone cameras

40. March 2015 – September 2015: Baker Botts LLP, on behalf of Dell, in Certain Electronic Products, Including Products with Near-Field Communication (“NFC”) System-Level Functionality and/or Battery Power-up Functionality, Components thereof, and Products Containing Same 337-TA-950 (International Trade Commission) and NXP B.V. v. Dell Inc., 1:14-cv-00146-UNA [case settled]
laptop power and data communications

41. March 2015 – September 2015: Baker Botts LLP, in Inter Partes Review of U.S. Patents 7412230, 6590365, 8065389, 8204959.

42. October 2015 – December 2015: Baker Botts LLP, in Inter Partes Review of U.S. Patent 7,926,978, “Light Set with Surface Mounted Light Emitting Components” by Kenneth Tsai, owned by Real Bonus Ltd. [declaration]
String LED lights

43. January 2013 – November 2017: Finnegan, Henderson, Farabow, Garrett & Dunner, L.L.P., on behalf of Axis Communications AB and Axis Communications, and McDermott Will & Emery on behalf of Hewlett-Packard, in Network-1 Technologies Inc. v. Alcatel-Lucent USA Inc., et al., No. 6:11-cv-00492-RWS-KNM and Network-1 Technologies Inc. v. Axis Communications AB., et al., No. 6:13-cv-00080-RWS-KNM. Trial 11/6/17 - 11/13/17. [jury trial]
Power over Ethernet

44. November 2015 – July 2016: DLA Piper LLP on behalf of Samsung Electronics Co., Ltd., Samsung Electronics America, Inc. and Samsung Telecommunications America, LLC, in UNITED STATES INTERNATIONAL TRADE COMMISSION, In the Matter of CERTAIN RF CAPABLE INTEGRATED CIRCUITS AND PRODUCTS CONTAINING THE SAME, Investigation No. 337-TA-982 [reports] [case settled]
RF mixers

45. February 2016: Baker & Hostetler on behalf of Sony, in Raytheon Company v. Sony Corporation, et al., C.A. No. 2:15-cv-342 (E.D. Tex.) and Raytheon Company v. Samsung Electronics Co., Ltd., et al., C.A. No. 2-15-cv-00341 (E.D. Tex.). [case closed]
Cell phone cameras

46. October-November 2016: Baker & McKenzie LLP on behalf of Continental Automotive, in IN THE UNITED STATES DISTRICT COURT FOR THE EASTERN DISTRICT OF MISSOURI,

WATLOW ELECTRIC MANUFACTURING COMPANY Plaintiff, v. CONTINENTAL AUTOMOTIVE SYSTEMS, INC. and CONTINENTAL AUTOMOTIVE SYSTEMS US, INC. Defendants. [case closed]

47. Sept. 2016 – May 2017: Alston & Bird on behalf of Nokia in ITC action In the Matter of Certain Electronic Devices, Including Mobile Phones, Tablet Computers and Components Thereof, Inv. No. 337-TA-1039. [case settled]

48. Dec. 2016 – August 2017: Jones Day on behalf of Bio-Rad Laboratories in Thermo Fisher Scientific Inc. v. Bio-Rad Laboratories, Inc. CIPR2017-00054 and IPR2017-00055, and Bio-Rad Laboratories, Inc. v. Thermo Fisher Scientific Inc. (1:17-cv-00469-RGA, USDC - Wilmington, DC). [declaration, deposition]

49. March 2017: Baker Botts L.L.P. on behalf of AMD. [related to ASETTEK DANMARK A/S, Plaintiff, VS. CMI USA, INC., fka COOLER MASTER USA, INC., Defendant]

50. April 2017 – present: Baker & Hostetler LLP, on behalf of Renesas Electronics Corp., in Lone Star Silicon Innovations LLC v. Renesas Electronics Corp., et al. (E.D. TX), and associated IPRs. [declarations and depositions]

51. October 2017: Dorsey & Whitney LLP on behalf of Global Foundries.

52. September 2017 – September. 2018: Bunsow De Mory Smith & Allison LLP on behalf of VLSI Technology LLC.

53. June 2018 – Nov. 2018: O'Melveny & Myers LLP on behalf of Samsung in Certain Wafer-Level Packaging Semiconductor Devices and Products Containing Same (Including Cellular Phones, Tablets, Laptops, and Notebooks) and Components Thereof, ITC No. 337-3262; Tessera Advanced Techs., Inc. v. Samsung Elecs. Co., Ltd., et al., No. 2:17-cv-00671 (E.D. Tex.); Tessera Advanced Techs., Inc. v. Samsung Elecs. Am., Inc., et al., No. 2:17-cv-07621 (D.N.J.); Invensas Corp. v. Samsung Elecs. Co., Ltd., et al., No. 2:17-cv-00670 (E.D. Tex.); Invensas Corp. v. Samsung Elecs. Co., Ltd., et al., No. 1:17-cv-01363 (D. Del.); Invensas Bonding Techs., Inc. v. Samsung Elecs. Am., Inc., et al., No. 1:17-cv-07609 (D.N.J.); FotoNation Ltd. et al. v. Samsung Elecs. Co., Ltd., et al., No. 2:17-cv-00669 (E.D. Tex.). [case settled]

54. October 2018 – present: Irell & Manella LLP on behalf of VLSI Technology LLC. [IPRs] [semiconductor devices, processing, and packaging]

55. March 2019 – present: Alston & Bird LLP, on behalf of Cellco Partnership d/b/a Verizon Wireless in FRACTUS, S.A., Plaintiff, v. AT&T MOBILITY LLC, Defendant. SPRINT COMMUNICATIONS COMPANY, L.P., ET AL., Defendants. T-MOBILE US, INC. ET AL., Defendants. VERIZON COMMUNICATIONS INC. ET AL., Defendants. [reports, deposition]

56. Dec. 2018- present: Fish & Richardson P.C., on behalf of Wasica Finance

GMBH and Bluearc Finance AG in WASICA FINANCE GMBH and BLUEARC FINANCE AG,
Plaintiffs, v. SCHRADER INTERNATIONAL, INC. and SCHRADER-BRIDGEPORT
INTERNATIONAL, INC., Defendants, C.A. No. 13-1353-LPS. [reports, deposition]
[TPMS]

APPENDIX B (LIST OF MATERIALS CONSIDERED)

Ex. 1001	U.S. Patent No. 9,186,052 (“’052 patent”)
Ex. 1002	U.S. Patent No. 9,186,052 File History (“’052 Patent File History”)
Ex. 1003	File History of U.S. Patent No. 6,043,839
Ex. 1005	WO Application Publication No. 95/34988 (“Swift”)
Ex. 1006	U.S. Patent No. 5,835,141 (“Ackland”)
Ex. 1007	U.S. Patent No. 5,919,130 (“Monroe”)
Ex. 1009	U.S. Patent No. 4,700,219 (“Tanaka”)
Ex. 1015	U.S. Patent No. 5,233,426 (“Suzuki”)
Ex. 1016	JP Unexamined Patent Publication No. S62-104075 (“Tanuma”)
Ex. 1017	Plaintiff Collect LLC’s Amended and Supplemental Objections and Responses to Defendants Samsung Electronics Co., Ltd., and Samsung Electronics America, Inc.’s Interrogatory No. 2
Ex. 1027	U.S. Patent No. 5,903,706 (“Wakabayashi”)
Ex. 1028	File History of U.S. Patent No. 9,667,896
Ex. 1029	U.S. Patent No. 5,541,640 (“Larson”)
Ex. 1030	U.S. Patent No. 5,756,981 (“Roustaei”)
Ex. 1031	U.S. Patent No. 4,630,110 (“Cotton”)
Ex. 1032	European Patent Application Publication EP0610938 (“Crosetto”)
Ex. 1033	Ricquier, N., <i>et al.</i> “CIVIS sensor: a flexible smart imager with programmable resolution,” Charge-Coupled Devices and Solid State Optical Sensors IV. Vol. 2172. International Society for Optics and Photonics, 1994. (“Ricquier SPIE”)
Ex. 1035	Butler Affidavit (VISION VM5402 Camera Module Product Datasheet)

Ex. 1036	Mendis, S.K., <i>et al.</i> “Progress in CMOS active pixel image sensors,” in M.M. Blouke (Ed.), <i>Charge-Coupled Devices and Solid State Optical Sensors IV</i> , pp. 19-29, 1994 (“Mendis”)
Ex. 1037	Dickinson, A., <i>et al.</i> , “Standard CMOS Active Pixel Image Sensors for Multimedia Applications,” <i>Proceedings Sixteenth Conference on Advanced Research in VLSI</i> . IEEE, 1995.
Ex. 1038	Ricquier, N., <i>et al.</i> “CIVIS sensor: a flexible smart imager with programmable resolution,” <i>Charge-Coupled Devices and Solid State Optical Sensors IV</i> . Vol. 2172. International Society for Optics and Photonics, 1994. (“Ricquier”)
Ex. 1041	U.S. Patent Publication No. 2001/0010551 (“Dierickx”)
Ex. 1042	Hurwitz, et al., “An 800K-Pixel Color CMOS Sensor For Consumer Still Cameras” (“Hurwitz”)
Ex. 1043	U.S. Patent No. 5,837,994 (“Stam”)
Ex. 1044	U.S. Patent No. 5,221,964 (“Chamberlain”)
Ex. 1045	Charles Hamilton, <i>A Guide to Printed Circuit Board Design</i> (1984)
Ex. 1046	Hurwitz, <i>et al.</i> , “An 800K-Pixel Color CMOS Sensor For Consumer Still Cameras” (“Hurwitz Cornell”)
Ex. 1047	Hurwitz, <i>et al.</i> , “An 800K-Pixel Color CMOS Sensor For Consumer Still Cameras” (“Hurwitz SPIE”)
Ex. 1048	Fossum, E.R., “Active-pixel sensor challenge CDDs,” <i>Laser Focus World</i> 29(6), p. 83-87, June 1993 (“Fossum93”)
Ex. 1060	“NASA’s Tiny Camera Has A Wide-Angle Future,” <i>Business Week</i> (March 6, 1995)
Ex. 1085	U.S. Patent No. 5,859,878 (“Phillips”)

* I also considered any additional materials referenced in my declaration.