

FA 11.1: 256x256 CMOS Active Pixel Sensor Camera-on-a-Chip

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A CMOS imaging sensor integrates the sensor technology and digital control functions on a single chip. This demonstrates the viability of producing a camera-on-a-chip suitable for commercial, military, and scientific applications. Good imaging performance has been demonstrated with high quantum efficiency, low noise, no lag, no smear and good blooming control. The chip is characterized by random access, simple clocks, low system power, simple power supplies and fast read-out rates. The simple digital interface permits easy restructuring of windows-of-interest and integration times. The measured performance indicates that this technology will become competitive with CCDs in many applications, resulting in enhanced system performance and reduced cost.

The sensor uses active transistors at each pixel site to achieve a local conversion from charge-collection mode to voltage-readout mode. This active pixel sensor (APS) technology has advantages over CCDs [1, 2]. In this implementation, the pixel contains a photogate imaging element along with four transistors to perform readout, selection, and reset (Figure 1). At the bottom of each column of pixels, there is a load transistor VLN and two output branches to store the reset and signal levels. Each branch consists of a sample-and-hold capacitor (CS or CR) with a sampling switch (SHS or SHR) and a second source-follower with a column-selection switch (COL). The reset and signal levels are read out differentially, allowing correlated double sampling to suppress 1/f noise and fixed-pattern noise (not kTC noise) from the pixel. A double delta sampling (DDS) circuit shorts the sampled signals during the readout cycle reducing column fixed pattern noise. These readout circuits are common to an entire column of pixels. The load transistors of the second set of source followers (VLP) and the subsequent clamp circuits and output source followers are common to the entire array.

A block diagram of the chip architecture is shown in Figure 2. The chip inputs are a single +5V power supply, clock, start command, mode control, and parallel data load command for defining integration time and windowing parameters. The output consists of two differential analog channels, VS_OUT (signal) and VR_OUT (reset).

The chip can be commanded to read out any window of interest within the 256x256 array. A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32b counter via the input data bus. The input clock frequency can be adjusted to achieve a readout rate of 30frame/s. The chip can run in a differencing mode whereby the readout timing is altered so the value of each pixel output is the difference between the current frame and the previous frame [3].

The chip is processed by MOSIS in the HP 1.2 μ m linear capacitor process. The designed fill factor of the photogate pixel is approximately 21% with a 20.4x20.4 μ m² pixel. A sample image produced for a 256x256 window is shown in Figure 3.

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Performance is measured for a broad range of parameters. The results are shown in Table 1. Saturation is determined by the difference between the reset level on the floating diffusion node (approximately 3V) and the minimum voltage allowed on the pixel source follower gate (e.g. threshold voltage of approx. 0.8V). This corresponds to a full well of approximately 75,000 electrons. Conversion gain is obtained per pixel by plotting the variance in pixel output as a function of mean signal for flat field exposure. Measured output-referred conversion gain is 10.6 μ V/e-, which is in reasonable agreement with the estimated photogate pixel parasitic capacitance. Dark current is measured by varying the master clock rate and thus linearly controlling the integration period in the dark. Noise in the chip is measured by sampling a small window at 100kpixels/s and calculating the variance in the pixel output signal over 1000 frames of data. The fixed pattern noise arising from dispersion in conversion gain is under 1% - similar to the value found in CCDs and consistent with the well-controlled gain of a source-follower buffer amplifier. The measured quantum efficiency of a pixel is shown in Figure 4. Figure 5 is a chip micrograph.

Additional work is in progress for integrating the ADC function on-chip [4, 5]. Other functions such as automatic exposure and electronic shutter are also planned for subsequent designs.

References:

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- [2] Mendis, S., S.E. Kemeny, E.R. Fossum, "CMOS active pixel image sensor," *IEEE Transactions On Electron Devices*, Vol. 41, No.3, March 1994.
- [3] Dickinson, A., et al., "A 256x256 CMOS Active Pixel Image Sensor with Motion Detection," *ISSCC Digest of Technical Papers*, pp. 226-227, Feb., 1995.
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- [5] Pain, B., E. R. Fossum, "Approaches and analysis for on-focal-plane analog-to-digital conversion," *Infrared Readout Electronics II*, *Proc. SPIE*, vol. 2226, pp.208-218, 1994.

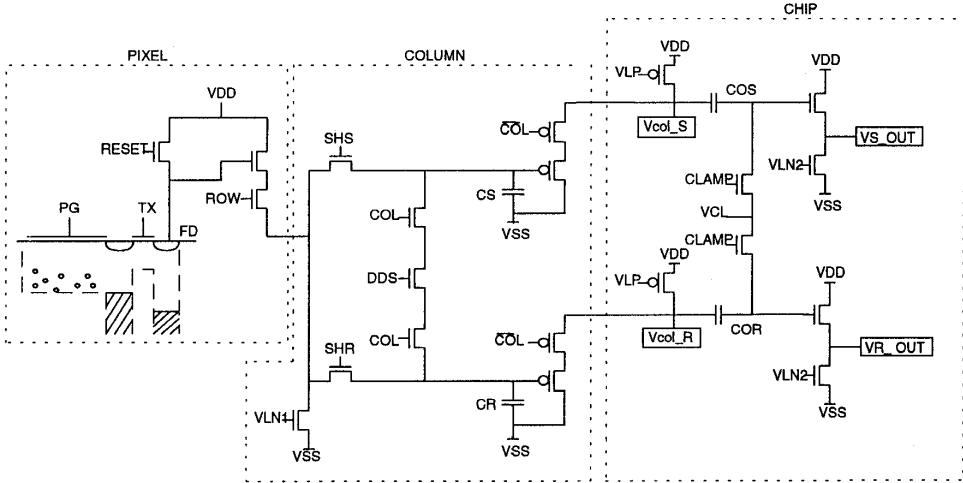


Figure 1: Schematic of active pixel unit cell and readout circuitry.

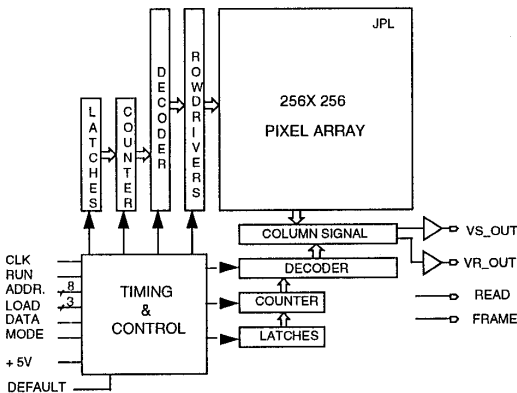


Figure 2: CMOS APS chip block diagram.

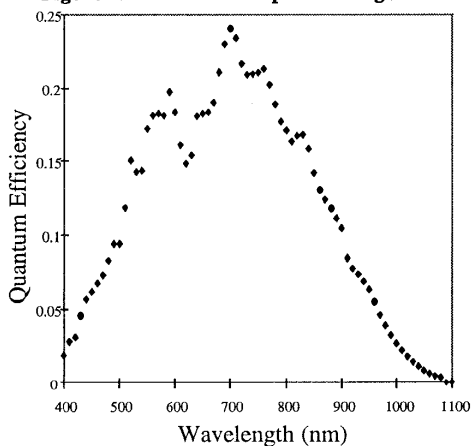


Figure 4: Absolute quantum efficiency of sensor.

Figure 5: See page 440.

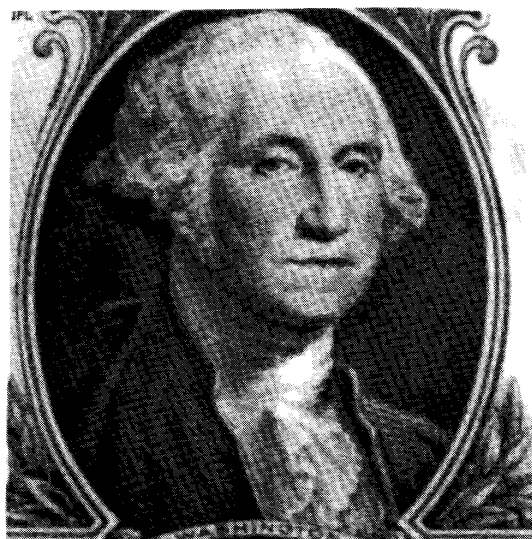


Figure 3: Sample raw image from sensor.

Saturation level	800mV	75,000e-
Conversion gain	10.6mV/e-	
Read noise	138mV	13e- rms
Dynamic range	75db	5800:1
Peak QE	20-25%	
Fixed-pattern noise	0.2% sat p-p	<2mVp-p
Dark current	29mV/dark	~500pA/cm ²

Table 1: Performance characteristics.

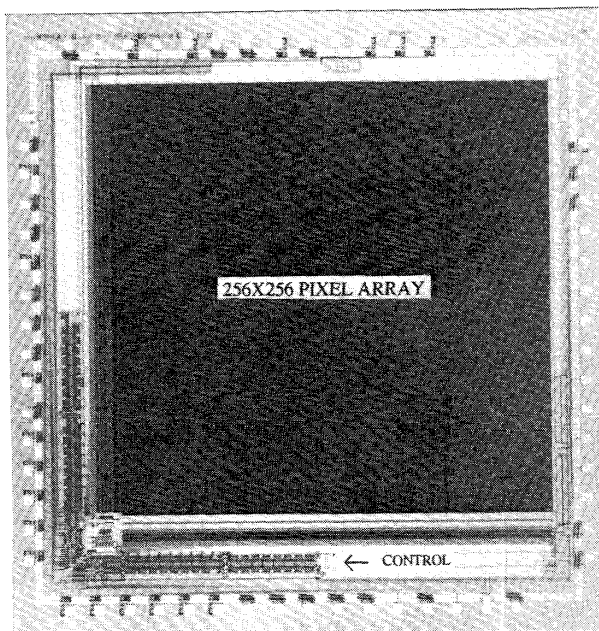


Figure 5: 256x256 CMOS APS image sensor micrograph.

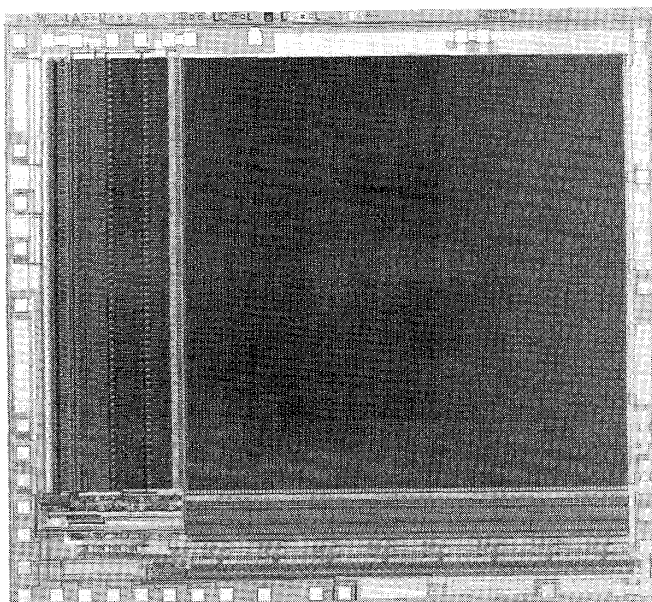


Figure 7: Chip micrograph.