

October 1996

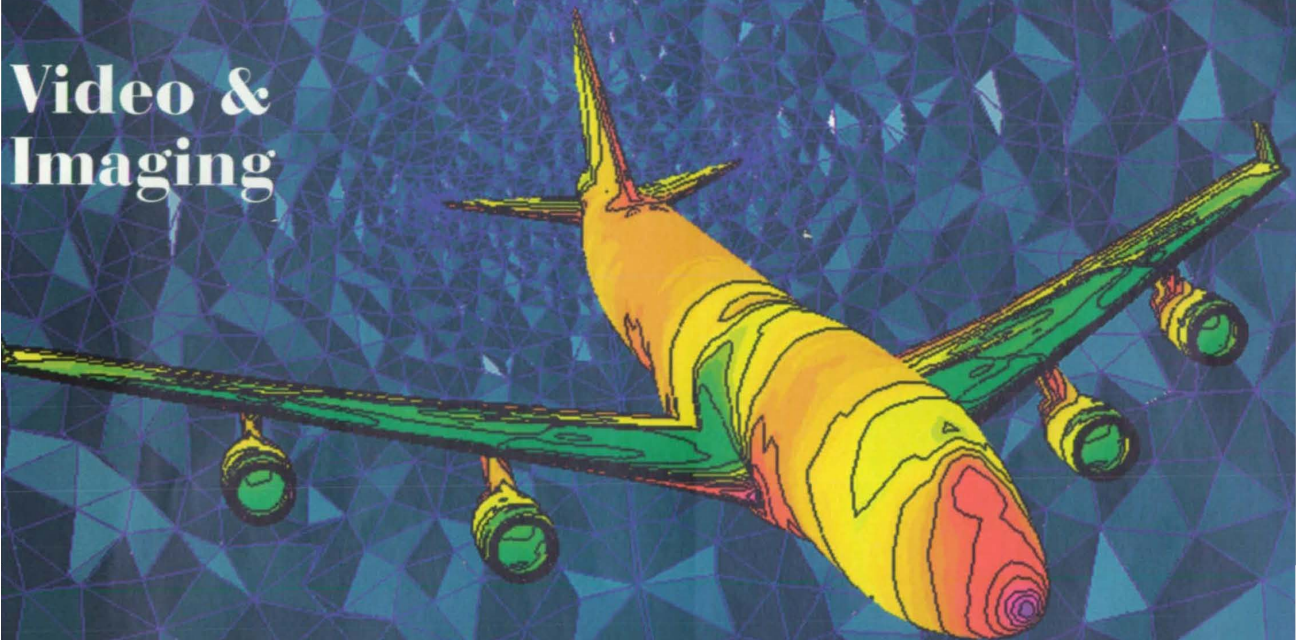
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# NASA Tech Briefs

*The Design/Engineering Technology Digest*

**NASA Software  
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**Video &  
Imaging**





## ▶ Active-Pixel Image Sensor Integrated With Readout Circuits

A single chip performs most of the functions of a video camera.

NASA's Jet Propulsion Laboratory, Pasadena, California

A single-chip complementary metal oxide/semiconductor (CMOS) integrated circuit comprises an active-pixel image sensor with timing, control, and readout circuits. This chip performs the electronic functions of a video camera of  $128 \times 128$  pixels with control of integration time, selection of a readout window (a subset of the full array of pixels), and frame activation. This chip offers an alternative to charge-coupled devices (CCDs). It is difficult to integrate control and signal-processing functions into CCDs, and fabrication of CCDs is expensive in comparison with fabrication of devices like the present one.

The chip features a  $1.2\text{-}\mu\text{m}$  design rule implemented in an n-well CMOS process. The pixel pitch is  $19.2\text{ }\mu\text{m}$ . The chip operates from a 5-V power supply. An externally-generated clock signal is needed to produce video output. Readout is implemented with a column-parallel architecture; the outputs of the pixels are multiplexed, one row at a time and then one column at a time through a single on-chip amplifier/buffer. Digital circuits employ common logic elements to control row and address decoders and delay counters. In addition to the clock and power, the required inputs to the chip are a single +5-V power supply, start command, and parallel data load commands for defining integration time and windowing parameters.

Figure 1 illustrates the major functional blocks. The analog outputs are VS\_OUT (signal) and VR\_OUT (reset), and the digital outputs are FRAME and READ. The inputs to the chip are asynchronous digital signals. To command the chip to read out from only a specified area of interest within the  $128 \times 128$  array, the decoder counters are preset to start and stop at values that have been loaded into the chip via the 8-bit data bus. Alternatively, when the DEFAULT input line is used, all counters are set to read out from the full  $128 \times 128$  array.

A programmable integration time is set by adjusting the delay between the end of one frame and the beginning of the next. This parameter is set by loading a 32-bit latch via the input data bus. A 32-bit counter operates from one-fourth the input clock frequency and is preset each frame from the latch; thus, very long integration times are achievable. The input clock signal can have any frequency up to about 10 MHz. The

pixel readout rate is tied to one-fourth the clock rate. Thus, the frame rate is determined by the clock frequency, the window settings, and the integration time. A frame rate of 30 Hz can be achieved without difficulty.

The chip is idle when the RUN command is deactivated. It is recommended to set operating parameters while the chip is idle, but because of the asynchronous nature of operation of the chip, it is also possible to set the operat-

of a sample-and-hold capacitor (CS for the signal level; CR for the reset level) with a sampling switch (SHR and SHS for the reset and signal level, respectively), and a second source follower with a column-selection switch (COL). The reset and signal levels from each pixel are read out differentially, enabling correlated double sampling to suppress  $1/f$  noise and fixed-pattern noise. These readout circuits are common to an entire column of pixels. The load transistors

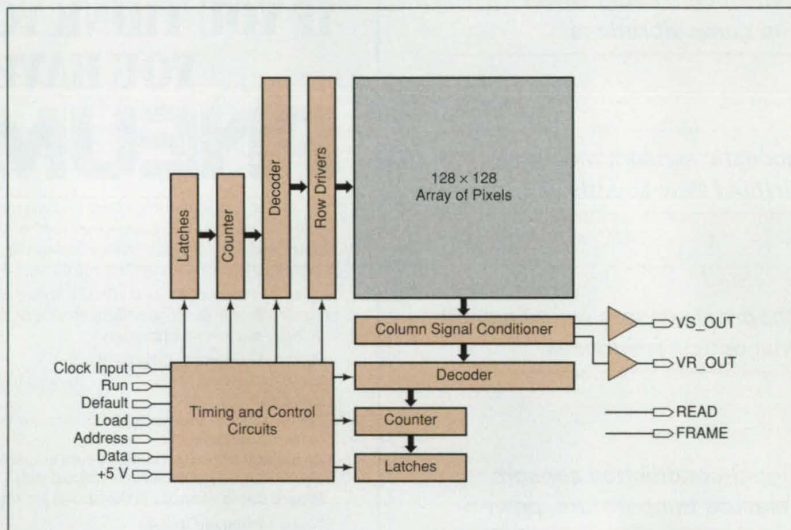


Figure 1. The **Active-Pixel Image Sensor** includes not only the photosensors but also the timing, control, and readout circuits, integrated on one chip.

ing parameters at any time. When RUN is activated, the chip repeatedly reads out frames based on the parameters loaded in the control registers. When RUN is deactivated, the frame in progress runs to completion, then operation stops.

The photosensor in each pixel is a photodiode. The pixels in this device are said to be active because each pixel also contains active components; namely, three transistors that are parts of the readout circuitry. Figure 2 illustrates one active pixel along with readout circuits external to the pixels. The pixel unit cell consists of the photodiode, a source-follower input transistor, a row-selection transistor, and a reset transistor, which controls lateral blooming through proper biasing of the reset gate.

At the bottom of each column of pixels, there is a load transistor VLN1 and two output branches to store the reset and signal levels. Each branch consists

(VLP) of a second set of source followers and associated clamp circuits are common to the entire array.

The readout circuits perform correlated double sampling (CDS) to suppress pixel fixed-pattern noise and an improved version of double-delta sampling (DDS) to suppress column fixed-pattern noise. After a row has been selected for readout, the signal that is present on each column from each pixel in that row is sampled (SHS) onto the holding capacitor CS. Next, each pixel in the row is reset (RESET). This is followed by sampling the reset level (SHR) onto holding capacitor CR.

The pixels in the chosen row are then read out by reading out the columns in sequence. After a column has been selected, there is a settling time equivalent to one-half the column selection period. Then DDS is performed: Prior to DDS, reset and signal column outputs (Vcol\_R and Vcol\_S) contain their





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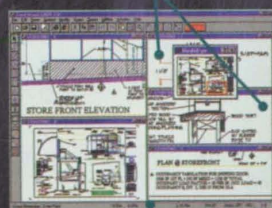
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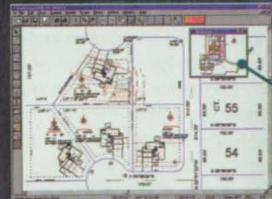
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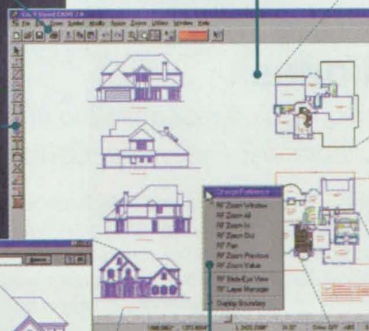
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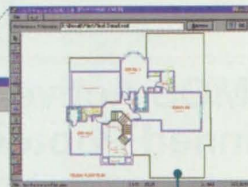
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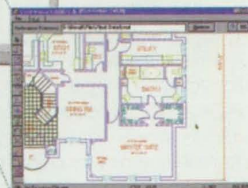
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respective values plus a source-follower voltage threshold component. Immediately after CLAMP is turned off, the DDS switch (the transistor labeled "DDS" in Figure 2) and two column-selection switches (COL) on opposite sides are used to short CR and CS together. The result is a difference voltage coupled to the output drivers (VR\_OUT and VS\_OUT) that is free of the voltage threshold component.

This work was done by Robert Nixon, Eric Fossum, and Sabrina Kemeny of Caltech for **NASA's Jet Propulsion Laboratory**. For further information, **write in 5** on the TSP Request Card.

In accordance with Public Law 96 517, the contractor has elected to retain title to this invention. Inquiries concerning rights for its commercial use should be addressed to:

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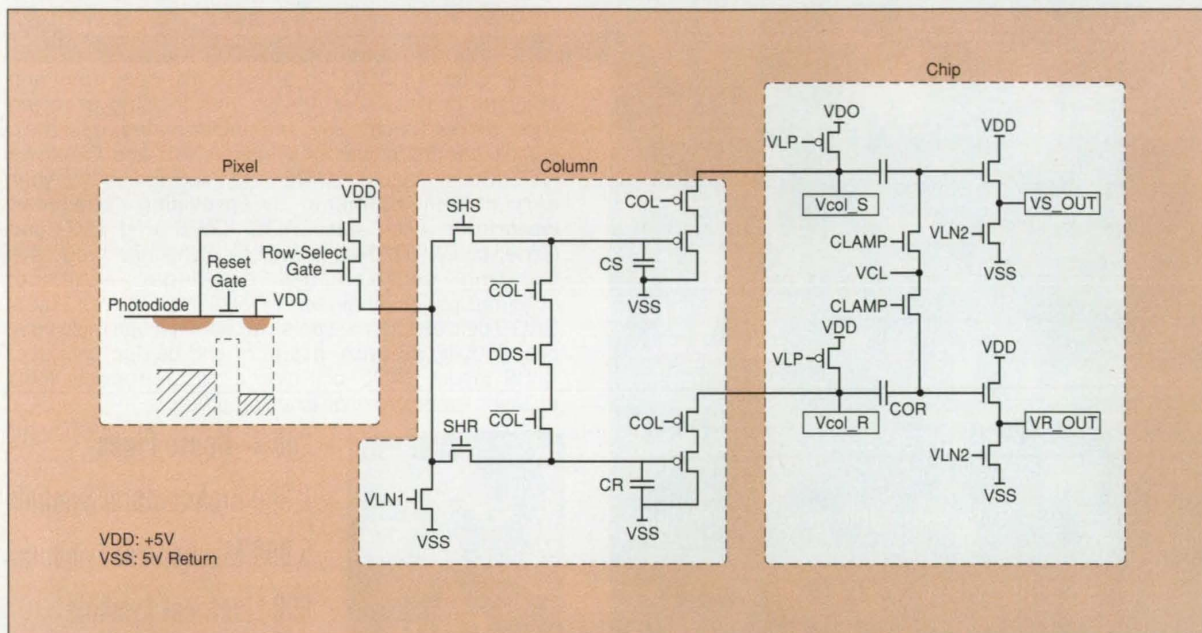


Figure 2. Each Active Pixel Contains Part of the Readout Circuitry, while some of the readout circuitry is common to all the pixels in a column and some serves all the columns on the chip.

## ► CMOS Active-Pixel Image Sensor Containing Pinned Photodiodes

Lower dark current and higher blue response are anticipated.

NASA's Jet Propulsion Laboratory, Pasadena, California

A complementary metal oxide/semiconductor (CMOS) active-pixel image sensor containing pinned photodiodes has been built (but not yet tested) in an effort to improve on a silicon-based active-pixel image sensor that was developed previously and is now in use at NASA's Jet Propulsion Laboratory. The older sensor operates with high quantum efficiency except in the blue part of the spectrum, where the response is diminished by photogates made of polycrystalline silicon ("poly" for short). In addition, the dark current ( $1 \text{ nA/cm}^2$ ) of the older sensor is greater than desired. Accordingly, the present sensor was designed to incorporate pinned photodiodes as its photoelements because pinned photodiodes

can be fabricated without overlying poly. Pinned photodiodes are characterized by no lag, low reset noise, low dark current, and high quantum efficiency.

The sensor contains an array of  $256 \times 256$  pixels on an integrated-circuit chip with an overall size of  $1.2 \times 1.2 \text{ cm}$  and with a 40-pin pad frame. All of the row and column addressing of the pixels is accomplished via 8-input NAND gates (one such gate for the rows, the other for the columns). Each 8-input NAND gate contains eight n-channel transistors in series, implemented by use of overlaid

poly-1/poly-2 gates, somewhat as in a charge-coupled device.

A column-control logic circuit generates a column-selection signal, which is used to control the serial readout of data and is used with a crowbar signal to perform an operation that reduces fixed pattern noise. Each column-readout circuit contains two sample-and-hold capacitors; one for the signal level and one for the reset level. The crowbar signal activates a crowbar switch, which is a transistor switch in each column-readout circuit that is used to selectively short-circuit the two sample-and-hold capacitors together to reduce the fixed pattern noise generated by threshold-voltage offsets in p-channel source followers in the readout circuitry.