

Self-Scanned Silicon Image Detector Arrays

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Abstract—The basic principle of operation of each bit in a matrix of image detectors is described, together with the derivation of appropriate operating formulas. The necessary circuitry to make a functional two-dimensional array is also described, including the scanning circuitry integrally constructed with the photodetector matrix. The necessary design considerations for operation of the matrix are discussed in the context of the currently operating 10-by-10 array. Extension of the principles to larger arrays is outlined in the two modes of array scanning considered, with special reference to spatial noise problems. The paper concludes with reference to other applications of the basic principle, such as card reading.

INTRODUCTION

WITH THE ADVENT of the integrated circuit and the inherent light sensitivity of the p - n junction, it was only a matter of time before solid-state image detection would be realized. However, not until the metal oxide silicon transistor (MOST) was developed could the full possibilities of solid-state image detection be determined. The only known exception to this is the work of Weimar,^[1] who makes use of thin-film techniques. This paper describes the development work at these laboratories which was designed to extend the basic MOSAIC¹ process to allow optical input. The basic diode design, with reasons for adopting this in preference to alternative devices, is described, as well as the development of the scanning circuitry. We believe it is essential to include this integrally with the detector array.

THE PHOTODIODE

The photodiode that has generally been used is the one generated "accidentally" by the boron source and drain diffusion. Lately, however, a shallower diffused diode has been used as an aid to device control, chiefly for circuit reasons. However, this shallow diffusion has similar optical characteristics to the deep diffusion. The shallow diffusion is of the order $1.2\ \mu$, and the deep diffusion $3\ \mu$. The planar diode has been treated theoretically in the conventional fashion to yield theoretical quantum efficiency versus wavelength curves. A study of oxide optical interference effects based on the original work of MacSwan^[2] has been added to this analysis so that the planar diode may be completely simulated and thus help to optimize diode design for appropriate wavelengths. This work could be extended very simply to include multiple interference films in order to obtain

narrow optical response. A program of actual diode measurements has been carried out in parallel with the theoretical studies. The measurement technique adopted was to use a monochromator image-splitting system and a thermopile as the comparison device, as shown schematically in Fig. 1. An all-dc system was employed, and the planar diode structure used was that shown in Fig. 2, which is one planar diode mounted and bonded in a TO-5 can. The results obtained, both theoretical and experimental, are shown in Fig. 3. The double peak is caused by the oxide interference at $0.5\ \mu$ and the natural p - n junction peak at $0.8\ \mu$.

Some studies of a buried diode structure have resulted in computer simulation and measurement. This program was aimed at achieving improved reverse-biased leakage currents and higher packing density. Early in the program it was discovered that leakage current tended to be almost entirely dependent on perimeter rather than area. This led to the concept of a large area device with small contact diffusion to reduce this perimeter in relation to the device area. In addition, if the device is buried below a suitable epitaxial layer, the MOST devices associated with each diode could be constructed over the diode, rather than alongside it, thus saving area. However, our present development of simple diode structure is such that the leakage current is well below the levels introduced by circuit noise, as explained later. In addition, the advent of multilayer metalization has meant that a significant increase in packing density can be obtained without recourse to more sophisticated structures. The buried diode structure is shown in Fig. 4 and has the quantum efficiency curve shown in Fig. 5. The buried diode leakage current values achieved at present are similar to those of surface diodes and will no doubt be reduced further. The leakage current in surface diodes $50\ \mu$ square is a few picoamps at 10 volts reverse bias, which is sufficiently low for most applications.

DIODE OPERATION PHILOSOPHY

The signal current generated by photodiodes $50\ \mu$ square is such as to make the simple multiplexing of each bit to access the reverse leakage current (and, hence, obtain a video signal) impossible, since currents of a few tens of picoamperes have to be considered. In the light of this, an alternative mode of operation was used, known as the "integrating mode," in which the self-capacitance of the diode is charged by a series switch (MOST). On switching off the MOST, the rate of decay of charge is dependent on the carriers generated by light energy. The rate of decay of the bias voltage on the

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¹ Metal Oxide Semiconductor Arrays of Integrated Circuits. (Plessey trademark applied for.)

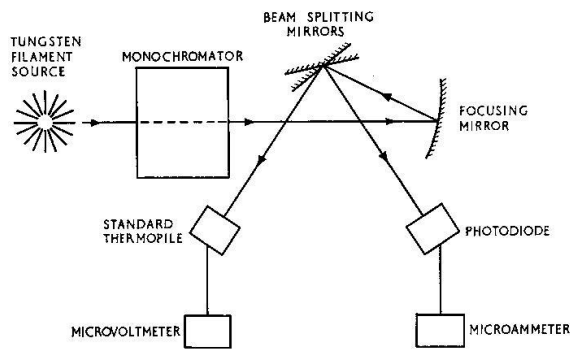


Fig. 1. Optical measurement system.

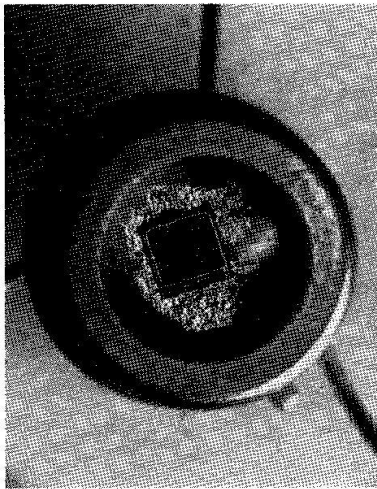


Fig. 2. Single planar diode.

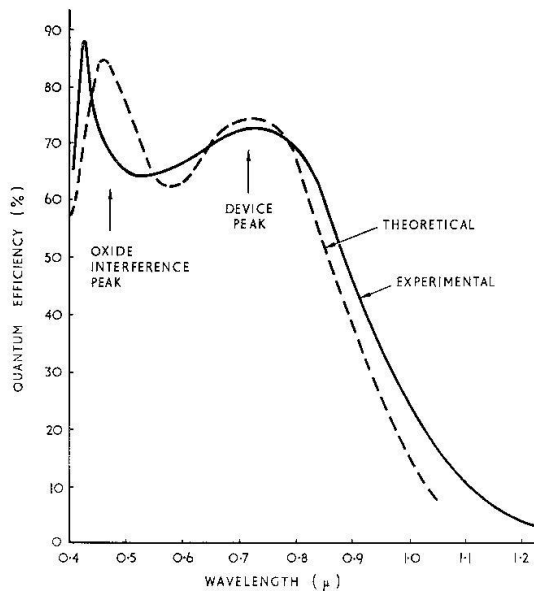
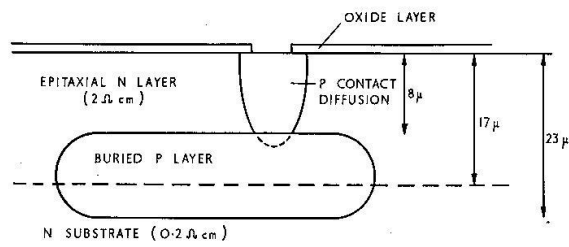
Fig. 3. Optical response; 3 μ surface photodiode.

Fig. 4. Buried diode structure.

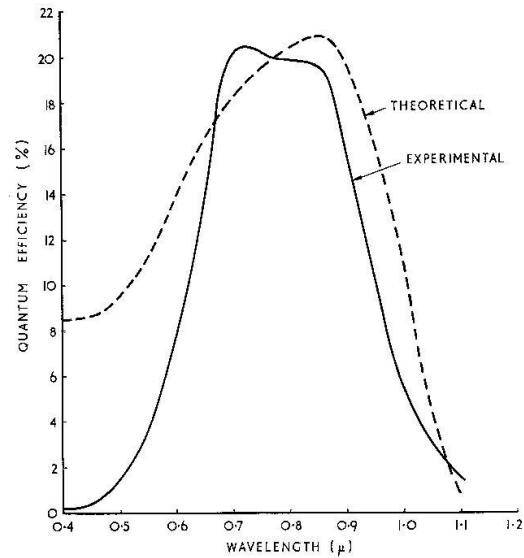


Fig. 5. Optical response; buried photodiode.

diode can be shown to be

$$\left(\frac{dV}{dt}\right)_v = \frac{1.2\lambda P\eta}{c} \quad (1)$$

where 1.2 incorporates various constants and a proportionality factor, and λ is the wavelength in microns, P is the incident power in watts, η is the quantum efficiency, and C is the diode capacity in $\text{F}\cdot\text{cm}^{-2}$ at 5 volts. It is noted here that perimeter effects have been ignored, and the junction has been assumed to be abrupt. Inserting experimentally determined values into the equation yields a value of $84 \text{ V}\cdot\text{s}^{-1}\cdot\mu\text{W}^{-1}\cdot\text{cm}^{-2}$. In practice, values for $(dV/dt)_v$ of $73 \text{ V}\cdot\text{s}^{-1}\cdot\mu\text{W}^{-1}\cdot\text{cm}^{-2}$ have been measured. The argument for using photodiodes as opposed to phototransistors as used by Weckler,^[4] Schuster,^[5] and others is that of variations in device-to-device sensitivity. We have found this to be ± 2.5 percent from diode to diode in a small array, since we do not have to contend with transistor h_{FE} variations. Another major advantage is that of processing simplicity because only one diffusion is required, and we have shown experimentally that lower leakage currents are

obtained for one diffusion (e.g., less temperature effects causing stress in junctions) as opposed to two or more diffusions. It is also well known that higher yields are obtained with MOSAICs than with conventionally diffused integrated circuits. In addition to this, the work of Crowell^[6] has resulted in photodiode arrays, scanned by an electron beam, producing acceptable pictures, thus demonstrating small device variations for diode structures.

The dark current of the diode has the effect of causing the voltage to decay at an average rate of about $1 \text{ V} \cdot \text{s}^{-1}$. Cooling the device to -70°C improved the leakage current by a factor of 10^3 , thus implying that each bit in the array is capable of detecting light levels of the order $10^{-10} \text{ W} \cdot \text{cm}^{-2}$. However, the scanning circuitry introduces noise equivalent to $10^{-7} \text{ W} \cdot \text{cm}^{-2}$; therefore, cooling can produce no benefits until improved scanning techniques are developed.

The basic integration mode can be incorporated into an array in two fundamentally different ways. The first of these is the "recharge sample" method, as adopted by other workers to phototransistor arrays, and is simply the monitoring of the current necessary to reinstate the diode bias. The second is to sample the voltage across the diode at the end of a frame time using an MOS source follower at every point in the array. In each case, access to the diode "bit" is by coordinate scanning, as discussed later. As will be demonstrated, both of these modes of operation have particular spatial noise problems.

OPERATION OF THE RECHARGE METHOD

Fig. 6 shows the basic schematic of a "bit" in a two-dimensional recharge array. The sampling of such a bit is by coordinate scanning by means of MOSAIC ring counters constructed at the periphery of the array.

At the end of a frame period, a diode is sampled by closing the series line and bit switches. Recharge current flows through the diode from the amplifier virtual earth, and a voltage—appearing at the amplifier output terminal (Fig. 7)—is given by

$$V_0 = v_i \frac{C_d}{C_f} \quad (2)$$

where v_i is the amount by which the diode bias has decayed, C_d is the diode capacity, and C_f is the amplifier feedback capacity. In other words, the signal gain through the charge amplifier is C_d/C_f . The amount of charge required to reinstate the diode bias is given by

$$q = C_d \cdot v_i \quad (3)$$

and the recharge current is then

$$i_c = \frac{q \cdot 10^{19}}{1.6} \text{ electrons.} \quad (4)$$

Expressing recharge current in terms of electrons rather than in amperes is more convenient, since there is no need to introduce time.

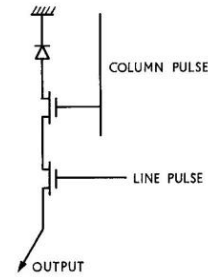


Fig. 6. Bit of recharge array.

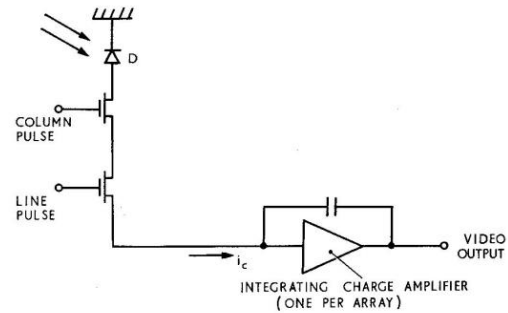


Fig. 7. Elements of recharge method.

When the bit switch is opened and prior to the succeeding bit switch being closed, the charge on the integrating capacitor is maintained. The discharge time constant depends on the input resistance of the amplifier and the OFF resistance of the bit switch. This residual charge must be deliberately removed at the end of the diode sample time before the next diode is sampled.

Effects of Stray Capacitance

Assuming that the array consists of a 100 by 100 matrix of detectors, the arrangement would be essentially as shown in Fig. 8. Thus, there will be 100 line switches in parallel across the charge amplifier input terminals. At any instant, one of these line switches will be closed, connecting further 100 bit switches in parallel across the amplifier input. Each OFF switch has capacity to earth; hence, the total capacity of 198 OFF switches appears across the input terminals of the amplifier. An approximate equivalent circuit is shown in Fig. 9.

In order to charge the diodes from the feedback capacitor and not from this spurious capacity (a process which would cause the signal to be lost), the feedback capacity, when referred across the amplifier input, should be much greater than the total stray capacity; i.e.,

$$C_f = (1 + A)C_s \gg C_s \quad (5)$$

where A is the amplifier forward path gain.

Additionally, if the available signal is not to be attenuated through the charge amplifier, it follows from (2) that the feedback capacitor should not be greater than

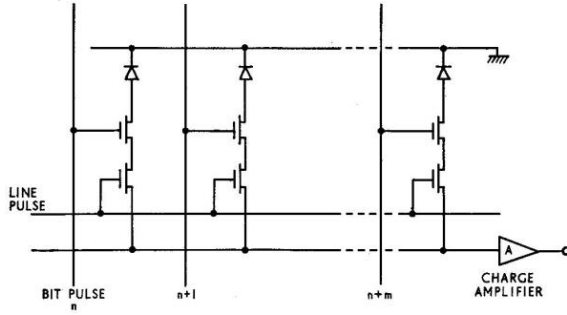
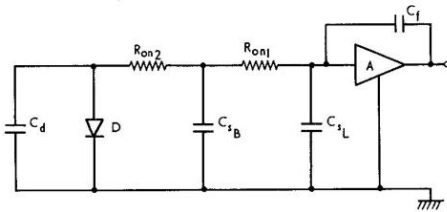


Fig. 8. Arrangement of outputs from recharge array.

Fig. 9. Equivalent circuit showing OFF channel capacitance. C_d = diode capacitance, C_{tL} = total capacitance of OFF line switches, C_{tB} = total capacitance of f bit switches, R_{on1} = ON resistance of line switch, and R_{on2} = ON resistance of bit switch.

the diode capacity; i.e.,

$$C_f' \leq C_d \quad (6)$$

Both (5) and (6) may be satisfied by choosing the value of A appropriately. However, the relationship expressed in (5) must be satisfied up to the highest signal frequency of interest.

It has been calculated that the cumulative stray capacity across the amplifier input terminals could be as much as 20 pF for a 100 by 100 array. Since the capacity of individual diodes is 0.5 pF, C_f must be limited to 0.5 pF for unity gain.

If we let $C_f' = (1 + A)C_f = 10C$, then $A \approx 400$ or 52 dB. At a frame rate of 25 frames per second, each bit time is equivalent to 4 μ s; hence, the fundamental signal frequency is 250 kHz. If the amplifier is to be stable, this 52 dB forward path gain must be maintained out to at least 250 KHz and then reduced at a controlled rate. This implies controlled gain roll off to beyond 100 MHz.

Spatial Noise

An obvious source of spatial noise results from array variations in diode capacity. Equation (2) shows that the signal gain is given by C_d/C_f ; therefore, C_d variations must give rise to spatial noise.

A major source of noise is the spurious charge injected into the signal path via the gate-to-channel capacitances of the bit switches. These are MOSTs which require gate swings in excess of ten volts to ensure full channel conduction. Assume that the gate-to-channel capacitance is 0.01 pF; the injected charge will then be

$$q_s = \frac{0.01}{10^{-12}} 0.10 = 10^{-13} \text{ C.}$$

It is interesting to calculate what level of radiation would cause the diode bias to decay by an amount requiring 10^{-13} C of charge to reinstate it:

If $C_d = 0.5$ pF, frame rate = 25 frames per second

$$10^{-13} = \frac{0.5}{10^{12}} v_i$$

$$v_i = 200 \text{ mV.}$$

Thus, for a frame period of 40 ms, the decay rate is $5 \text{ V} \cdot \text{s}^{-1}$, this rate being equivalent to an incident radiation level of $10^{-7} \text{ W} \cdot \text{cm}^{-2}$. At this level, the SNR is unity.

The particular limitation may perhaps be substantially overcome by using the available bit time to perform two separate functions. The diode is first recharged by closing the bit switch, an action which injects spurious charge into the signal path. Since the diode charging time constant may be measured in tens of nanoseconds, the bit switch may be opened after only a fraction of the available bit time has elapsed. The spurious charge previously injected should now be removed entirely, since the net charge transferred through the gate-to-channel capacitance must be zero. The remainder of the bit time may now be used to sample the required signal charge, provided that this charge is integrated over a sufficiently long time. As stated earlier, the discharge time constant of the integrating capacitor depends on the amplifier input resistance, which must therefore be extremely high.

The effects of stray capacitance were discussed earlier in the paper. Since complete removal of stray capacitance effects seems unlikely, variations in this stray capacitance as the array is multiplexed must be considered a further cause of spatial noise. This should be particularly noticeable at line rather than bit frequency.

Leakage Current

The equivalent circuit of Fig. 9 may be extended to include the effects of leakage currents. Referring now to Fig. 10, if the diode leakage current is ignored, the total leakage current is $(I_L + I_B)$. However, just as stray capacitance varies as the array is multiplexed, so will the total leakage current, which induces further spatial noise. Leakage current effects may be reduced by cooling the array, perhaps to the point where it may be considered negligible compared to other noise sources. However, there still remains the physical consideration of leakage paths around the circuit.

Fig. 10 shows the leakage path via the feedback leakage resistance, the gate resistance of the amplifier input MOST being considered infinite. However, it is probable that the leakage of the feedback capacitor will be comparable with that of an MOST gate because of the physical construction of such a capacitor. The result of

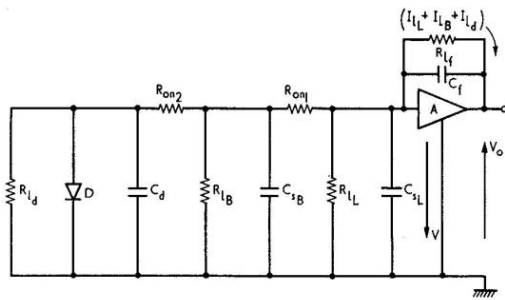


Fig. 10. Equivalent circuit showing leakage paths.

this will be to drive the amplifier output stage to the limit of its dynamic range.

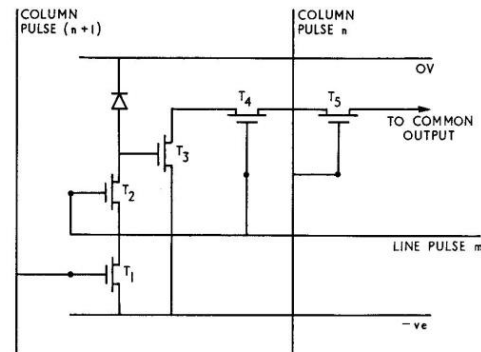
Consideration of all of these effects leads to the conclusion that very precise masking and construction techniques for making such an array are essential to obtain high sensitivity with low spatial noise. In view of these considerations, first arrays constructed by the author and colleagues were based on the voltage sampling principle described below.

THE VOLTAGE SAMPLING PRINCIPLE

The diode capacitance is charged by the MOST switches T_1 , T_2 (Fig. 11), and the decaying diode voltage is monitored by T_3 , which acts for all practical purposes as a perfect buffer, since its input impedance is greater than 10^{13} ohms. After a frame time has elapsed, sample pulses applied to T_4 , T_5 will transfer the voltage at the source of T_3 , itself related to the diode voltage, onto the output load. Thus, a small photocurrent in the diode is converted to a large output voltage signal. It is worth noting that the light generated current in the diode is proportional to the area of the diode and approximately proportional to the diode capacity; thus, the rate of decay of any diode voltage is constant, irrespective of area for a given intensity of illumination.

Spatial Noise

As indicated earlier, device-to-device variations of not more than ± 2.5 percent have been measured for the optical response of diodes in an array. The dark current variations of such diodes are between a few $\text{mV} \cdot \text{s}^{-1}$ and a few $\text{V} \cdot \text{s}^{-1}$, so that a maximum figure for dark variations due to diodes alone is the order of $\pm 3 \text{ V} \cdot \text{s}^{-1}$, or an equivalent optical input variation of $4 \times 10^{-8} \text{ W} \cdot \text{cm}^{-2}$ at 25°C . As indicated, cooling can reduce this to very low values. The chief source of noise in an array of this nature is caused by variations in the amplifying MOST T_3 (Fig. 11). There are two fundamental parameters which are critical; these are TV_{GSS} (turn on voltage of the MOST, about -4.5 volts) and β (transfer gain of MOST) measured in μAV^{-2} . In our normal arrays, TV_{GSS} introduces variation in the array of the order $\pm 100 \text{ mV}$ per frame, which is equivalent to a dark current decay rate of $2.5 \text{ V} \cdot \text{s}^{-1}$ at 25 frames per second. This, added to the dark current variations, gives rise to

Fig. 11. Voltage sampled "bit" of array (m nmth bit).

a dark level spatial noise of the order $\pm 5 \text{ V} \cdot \text{s}^{-1}$, or about $7 \times 10^{-8} \text{ W} \cdot \text{cm}^{-2}$ equivalent optical signal.

In addition to this form of spatial noise, there is the spatial noise of the sampling circuitry, such as capacitive variations in output leads and leakage current variations. All these considered, a level of dark current noise equivalent to an optical input variation of $10^{-7} \text{ W} \cdot \text{cm}^{-2}$ is achieved at present. By means of a modified sampling technique and cooling, levels of $10^{-9} \text{ W} \cdot \text{cm}^{-2}$ are anticipated in the near future.

Variation in device β can be reduced by using a virtual earth amplifier instead of load resistance (which also allows an increased scan rate). Very little work on the measurement of β variation effects has been done, but indications are that variations in signal level of less than ten percent have been achieved. The voltage sampling mode was used in our first arrays.

THE SCANNING CIRCUITRY

Two ring counters, one providing the X scan and the other the Y scan, are all that are required.

Circuit Operation

The circuits are designed with MOSAICs and are of the type commonly known as two phase dynamic.^[7] Essentially, each counter is a modified shift register, a single bit of which is shown in Fig. 12. The shift bit operation is based on the use of transistor gate capacitance storage as the temporary memory. Thus, clock pulse $\phi 1$ transfers the data in via T_1 onto the gate of the inverter T_2 , where the information is stored. MOST T_3 acts simply as a load for the inverter, whose output is the inverse of the data in. By a similar means, clock pulse $\phi 2$ transfers this new information via a second inversion to the final output of the shift bit, where it is equivalent to the original data in, delayed by one clock period; note that $\phi 1$ and $\phi 2$ must not overlap.

A ring counter can be realized by assembling the required length of shift register and adding a single logic gate (in this case a NOR gate, as shown in Fig. 13) which determines the pattern of logic "1" and "0" being shifted through the register. The pattern required, of

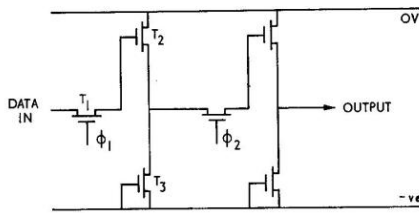


Fig. 12. Full shift bit.

course, is a single logic "1" being cycled through the register such that when a logic "1" is shifted out of the n th bit of an " n " bit register, a new logic "1" is introduced into the first bit. The pattern gate achieves this by recognizing that the first through $n-1$ bits of the register are at logic "0", thus providing a logic "1" at its output to be reintroduced into the first bit of the register.

Circuit Design Considerations

Using the characteristic equations for a MOST given below, it is a simple matter to calculate the ratio of aspect ratios of the load and inverter MOST to produce the required logic level outputs.

$$I_D = \beta^* a (V_D V_E - V_{D2}^2/2) \quad V_E \geq V_D \quad (7)$$

$$I_D = \beta^* a V_E^2/2 \quad V_E \leq V_D \quad (8)$$

where I_D is the drain current, V_D is the drain-to-source voltage, V_E is the excess gate voltage, a is the aspect ratio, and β^* is the process constant measured in $\mu\text{A}/\text{V}^2$. Clearly the drain current I_D will be equal in the load inverter MOSTs. Referring again to Fig. 12 and considering transistors T_2 and T_3 , (9) therefore represents the condition of a logic "0" from the inverter

$$I_{D_2} = I_{D_3} = \beta_2^* (V_{D_2} V_{E_2} - V_{D_2}^2/2) = \beta_3^* a_3 V_{E_3}^2/2; \quad (9)$$

thus,

$$\frac{a_2}{a_3} = \frac{V_{E_3}^2}{2V_{D_2} V_{E_2} - V_{D_2}^2}. \quad (10)$$

The values of V_{D_2} , V_{E_2} , and V_{E_3} can be determined from a knowledge of supply voltage, clock pulse amplitude, the logic "0" level required, the limits of threshold voltage (TV_{GSS}) to be expected, and how this varies with source/substrate bias. Care must be taken, however, in determining the value of V_{E_3} to be used. At first sight it would seem to be simply a matter of subtracting the respective threshold voltages of the transfer and inverter MOSTs from the height of the clock pulses and then allowing a noise margin of 1 to 2 volts. Consider, however, the effect of the gate to source capacitance of the transfer MOST which, in conjunction with the total capacitance at the gate of T_2 (i.e., gate of

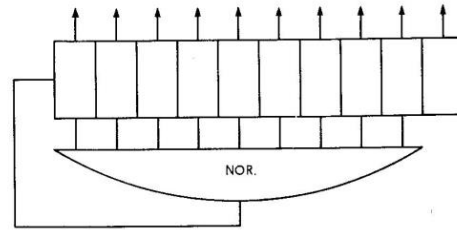


Fig. 13. 10-bit ring counter.

T_2 and sources of the transfer MOST), forms a capacitive divider for the clock pulse to earth. As determined by this divider, the trailing edge of the clock pulse will reduce the voltage to be stored on the gate of T_2 . Furthermore, during the storage period between the trailing edge of ϕ_1 , say, to the trailing edge of ϕ_2 , or vice versa, the stored voltage will be reduced in value because of the total leakage to earth at the gate of T_2 in which the source to substrate leakage of the transfer MOST will predominate. Ideally, then, for the low operating frequency necessary for the Y scan, these effects must be minimized, which points to a large inverter such that the required logical "0" is maintained with nearly zero excess gate voltage and a small transfer MOST to minimize capacitive break through of the clock pulse and leakage effects. However, a large inverter and its associated increase in gate capacitance will tend to slow down the transfer of information, as will the small size of the transfer MOST. Also, the larger the inverter the greater its handicap in achieving a compact practical layout, a requirement which might inject other significant variations from the ideal. The final design, then, must inevitably be a compromise solution derived from consideration of all the above factors.

A SIMPLE 10-BY-10 SELF-SCANNING ARRAY

Fig. 14 shows a photograph of a simple array of 100 photodiodes operating in the voltage sampling mode. The diode-to-diode spacing is 100μ in both directions, giving a sensitive area of 40 by 40 mil (1000 μ square) on a chip of 70 by 70 mil. This device was designed to evaluate both the basic concepts discussed above and devices described elsewhere.^{[8], [9]} A frame scan rate of 50 frames per second is normal, with a maximum in excess of 500 frames per second and a minimum dependent on operating conditions, but 10 frames per second can be used in most conditions. This lower limit is imposed by the dynamic scanning techniques, since stored logic levels will decay because of leakage currents associated with the clock MOSTs in the ring counter. The use of dc logic scanning would reduce scanning rates to as low as desired, but in this application the dynamic technique is considered adequate. The device shown is driven by an 11-bit and 10-bit ring counter; thus, pulses are automatically introduced for frame and line synchronization. Additional facilities on the chip allow

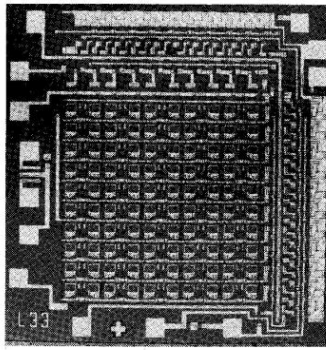


Fig. 14. 10-by-10 self-scanning array.

for external synchronization; therefore, many devices may be run synchronously if desired. In order to operate, a single device needs only 30 volts dc, two nonoverlapping—24 volt clock pulses, an array voltage supply, and an output load. These arrays can then be operated with only 6 leads, compared to 22 if external scanning were used. This advantage when using 100 by 100 and larger arrays is readily appreciated. Extension of this principle to larger arrays would inevitably lead to yield problems unless some redundancy were used. The 100 by 100 arrays presently being considered will be driven by four 10-bit counters multiplexed to give a 100 by 100 drive. In order to introduced synchronization, either arrays of 99 by 100 will be built or the first ring counter extended to 11 bits. Hence, only 41 bits of counter will be used with suitable selection switches. As a 100 by 100 array will be about 1 cm square, a chip of 1.2 cm square will be used with several ring counters. These counters will then be connected to the array by majority logic techniques or a simple form of discretionary wiring, as is becoming popular on so-called LSI. Hence, the next stage of development is a self-scanning 100 by 100 array, which should have good picture quality and operate in reasonably low light conditions.

OTHER DEVICES

During the course of this work, several other devices based on the same technique were developed. Fig. 15 shows a 4 by 18 matrix used as a card reader. The chip is 100 by 100 mil and is accessed by external circuitry by means of 5 parallel inputs to the 18 lines by a large MOSAIC encode gate. The selected line reads these 4 bits and transfers the information to 4 binary stores on the chip, which then communicate with external circuitry. The device reads at a designed rate of 10 lines per second at a very low light level, but can be read up to several tens of kilohertz if the illumination is increased. Fig. 16 shows the four outputs read sequentially. The card was a simple binary pattern. Other devices under development include position sensitive chips that can be read to 0.1 mil (2μ).

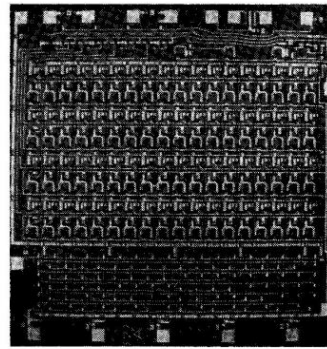


Fig. 15. Card reading chip.

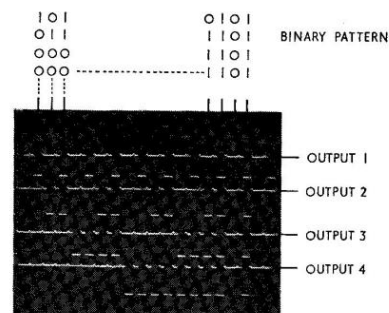


Fig. 16. Binary code read-by-card reader.

THE FUTURE

The rapid development of this field in all areas—from card reading to large self-scanning image detectors—will lead to exploitation of the basic techniques in presently unthought of areas. Atalla's recently expressed sentiments^[10] are entirely right in that we now have a new technique available which we must all use our imagination to exploit. To consider these techniques as mere replacements would be far too constricting. In the area of possible future developments, the combination of photodiodes with logic in a self-adapting manner for pattern recognition purposes is just one possibility.

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REFERENCES

- [1] P. K. Weimar *et al.*, "A self-scanned solid-state image sensor," *Proc. IEEE*, vol. 55, pp. 1591-1602, September 1967.
- [2] A. MacSwan, "The colour of thin oxide films on metals," *Proc. Phys. Soc.*, vol. 72, p. 472, November 1958.
- [3] K. J. S. Cave *et al.*, "Novel photodiode structures," presented at the Internat'l Electron Devices Meeting, Washington, D. C., October 1966.
- [4] G. P. Weckler, "Storage mode operation of a phototransistor and its adaptation to integrated arrays for image detection," presented at the Internat'l Electron Devices Meeting, Washington, D. C., October 1966; also *Electronics*, vol. 40, p. 75, May 1, 1967.
- [5] M. A. Schuster *et al.*, "Fabrication considerations for high order monolithic solid state mosaics of opto-electronic elements," presented at the AIME Conf. on Material Science and Technology in Integrated Electronics, San Francisco, Calif., September 1965.
- [6] M. H. Crowell, "An image sensing diode array with electron beam accessing," presented at the Solid State Devices Conf., Manchester, England, September 5-7, 1967.
- [7] P. E. Krebs *et al.*, "M.O.S. integrated circuits using gate capacitance storage," presented at the IEE Conf. on Integrated Circuits, Eastbourne, England, May 1967; also IEE Conf. Publication 30, p. 137.
- [8] P. J. W. Noble, "Light sensitive arrays based on photodiodes combined with M.O.S. devices," presented at the IEE Conf. on Integrated Circuits, Eastbourne, England, May 1967; also IEE Conf. Publication 30, p. 251.
- [9] P. J. W. Noble, "Solid state image detectors," presented at the SIRA Conf., Eastbourne, England, April 10-12, 1967.
- [10] M. M. Atalla, "Injection electro-luminescence and display devices," presented at the Solid State Devices Conf., Manchester, England, September 5-7, 1967.

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