CMOS Image Sensors :
State-Of-The-Art and Future Perspectives

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***Abstract*—Over the last decade, CMOS image sensor technology made huge progress. Not only the performance of the imagers was drastically improved, but also their commercial success boomed after the introduction of mobile phones with an on-board camera. Many scientists and marketing specialists predicted 15 years ago that CMOS image sensors were going to completely take over from CCD imagers, in the same way as CCD imagers did mid eighties when they took over the imaging business from tubes [1]. Although CMOS has a strong position in imaging today, it did not rule out the business of CCDs. On the other hand, the CMOS-push drastically increased the overall imaging market due to the fact that CMOS image sensors created new application areas and they boosted the performance of CCD imagers as well. This paper describes the state-of-the-art of CMOS image sensors as well as the future perspectives.**

I. IMPACT OF CMOS SCALING ON IMAGE SENSORS

It is common knowledge that the scaling effects in CMOS technology allow the semiconductor industry to make smaller devices. This rule holds for CMOS imaging applications as well.

Figure 1 gives an overview of CMOS imager data published at IEDM and ISSCC of the last 15 years [2]. The bottom curve illustrates the CMOS scaling effects over the years, as described by the ITRS roadmap [3]. The second curve shows the technology node used to fabricate the reported CMOS image sensors, and the third curve illustrates the pixel size of the same devices.

It should be clear that :

- CMOS image sensors use a technology node that is lagging behind the technology nodes of the ITRS. The reason for this is quite simple : very advanced CMOS processes used to fabricate digital circuits, are not imaging friendly (issues with large leakage current, low light sensitivity, noise performance, optical issues, …). Compared to the ITRS roadmap, the difference in technology used for image sensors and advanced logic processes is about 3 technology generations,
- CMOS image sensor technology scales almost at the same pace as standard digital CMOS processes do,
- Pixel dimension scales with the technology node used, and the ratio is about a factor of 20.

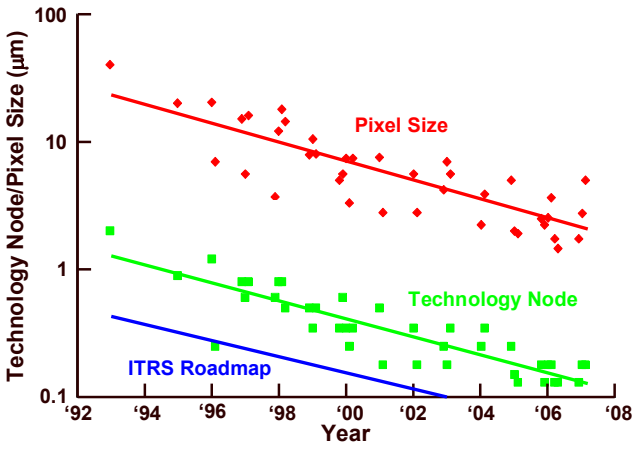

Figure 1. Evolution of pixel size, CMOS technology node used to fabricate the devices and the minimum feature size of the most advanced CMOS logic process.

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Shrinking the pixel size for CMOS image sensors is a very important driver for the overall imaging business. It has a very large impact on various parameters of the complete camera system. For instance, if the pixel size of a CMOS image sensor is equal to p, the scaling factor for various parameters are (keeping the total pixel count unchanged) :

- pixel pitch $\sim p$,
- pixel size $\sim p^2$,
- chip size $\sim p^2$,
- chip cost $\sim p^2$,
- energy to read the sensor $\sim p^2$,
- lens volume $\sim p^3$,
- camera volume $\sim p^3$,
- camera weight $\sim p^3$.

From this list it will be clear that there is a very strong driving force to shrink the pixel size as much as possible. Unfortunately smaller pixels have a negative effect on their optical and electrical performance. For instance, the proportionality of the pixel performance are :

- signal-to-noise $\sim p^{-1}$,
- depth of field $\sim p^{-1}$,
- depth of focus $\sim p^{-1}$,
- dynamic range $\sim p^{-2}$.

The market for consumer applications is asking for smaller pixel sizes at the same time that progress in CMOS technology is also offering the means to fabricate them. But as can be concluded from the table above, smaller pixels result in a weaker performance. It is a real challenge to improve the pixel design as well as the processing technology, at a pace that can counteract the loss of performance as the pixels shrink. Nevertheless new techniques to improve the light sensitivity of imagers are :

- dedicated processes with a limited amount of metal layers,
- thin interconnect layers and thin dielectrics,
- micro-lenses composed out of more than on component,
- light guide-waves on top of the pixels,
- back-side illumination.

Future devices are going to be masterpieces of vertical integration !

II. CMOS PIXEL STRUCTURES

In principle a CMOS image sensor has a very similar architecture as a digital memory, see Figure 2.

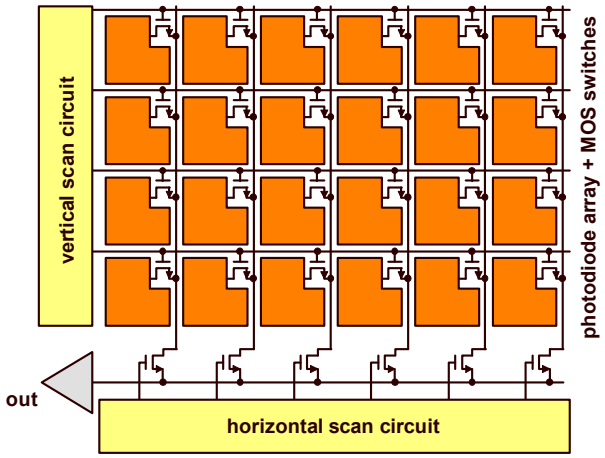

Figure 2. Architecture of a 2-dimensional CMOS image sensor.

It is composed of :

- an array of identical pixels, each having at least a photodiode and an addressing transistor, the number of pixels ranging from 330,000 for VGA-size imagers, to 17 M (or even more) for professional applications,
- a Y-addressing or scan register to address the sensor line-by-line, by activating the in-pixel addressing transistor,
- a X-addressing or scan register to address the pixels on one line, one after another,
- an output amplifier.

The structure of the pixels can be very simple : a combination of a photodiode and an addressing transistor that acts as a switch, see Figure 3.

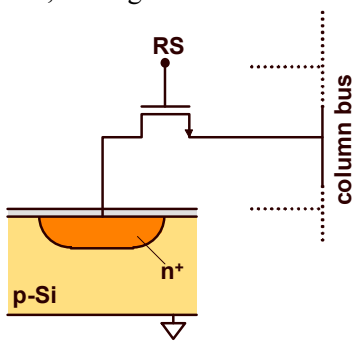

Figure 3. Passive CMOS pixel based on a single in-pixel transistor.

The working principle can be understood as follows [4] :

- at the beginning of an exposure the photodiode is reverse biased to a high voltage (e.g. 3.3 V),
- during the exposure time, impinging photons decrease the reverse voltage across the photodiode,
- at the end of the exposure time the remaining voltage across the diode is measured, and its

drop from the original value is a measure for the amount of photons falling on the photodiode during the exposure time,
- to allow a new exposure cycle, the photodiode is reset again.

This so-called passive pixel is characterized by a large fill factor (ratio of diode area and total pixel area), but unfortunately, the pixel is suffering from a large noise level as well. The reason for this is the mismatch between the small pixel capacitance and the large vertical bus capacitance.
A major improvement in the noise performance of the pixels was obtained by the introduction of the active pixel concept [5] : every pixel gets its own in-pixel amplifier, being a source-follower, see Figure 4. The pixel is composed out of the photodiode, the reset transistor, the driver of the source-follower and the addressing transistor. The current source of the source-follower is placed at the end of the column bus.

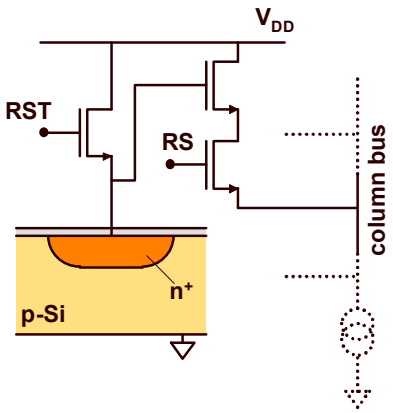

Figure 4. Active CMOS pixel based on an in-pixel amplifier.

The working principle of the active pixel sensor is basically the same as for the passive pixel sensor :
- the photodiode is reverse biased or reset,
- impinging photons decrease the reverse voltage across the photodiode,
- at the end of the exposure time the pixel is addressed and the voltage across the diode is brought outside the pixel by means the source follower,
- the photodiode is reset again.

This concept of active pixel sensor became very popular in the mid-nineties, it solved a lot of noise issues. Unfortunately the kTC noise component, introduced by resetting the photodiode, still remained.

To solve the latter issue of thermal FET noise in the presence of a filtering capacitor, the so-called pinned photodiode pixel, also popular in CCD image sensors, was introduced, see Figure 5 [6]. At the right side of this figure, one can recognize exactly the same structure as in the active pixel sensor. Additionally to this pixel, an extra (pinned) photodiode is added which is connected to the readout circuit by means of an extra transfer gate, TX. With this pixel the photodiode is separated from the readout node.

The pinned photodiode pixel operates as follows :
- conversion of the incoming photons is done in the (pinned) photodiode,
- at the end of the exposure, the readout node is reset by the reset transistor,
- a first measurement is done of the output voltage after reset,
- the photodiode is emptied by activating TX and transferring all charges from the photodiode to the readout node,

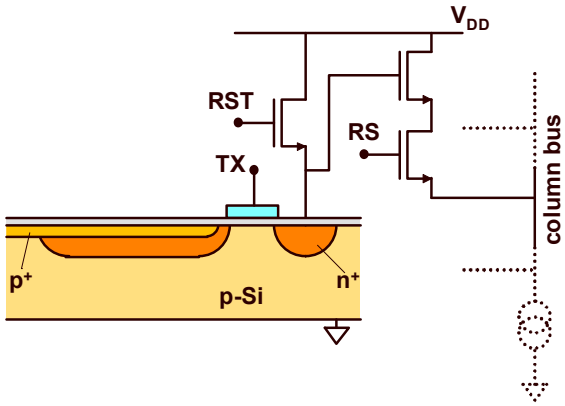

Figure 5. Active CMOS pixel based on an in-pixel amplifier in combination with a pinned-photodiode.

- a second measurement of the output voltage is done after transfer,
- the two measurements are subtracted from each other (Correlated Double Sampling, CDS) [7].

The completely depleted pinned-photodiode has several very attractive features :
- the kTC noise of the readout node can be completely cancelled by means of the CDS,
- CDS has also a positive effect on the 1/f noise of the source follower, as well as on its residual off-set,
- the kTC noise of the photodiode itself is completely absent, because in the case of full depletion, the photodiode can be made completely empty,
- the light sensitivity is higher compared to a classical photodiode, because the depletion

layer stretches almost to the Si-SiO_2 interface,
- because of the double junction (p^+n and np-substrate), the intrinsic charge storage capacitance is higher,
- the Si-SiO_2 is perfectly shielded by the p^+ layer and keeps the interface fully filled with holes, that makes the leakage or dark current extremely low.

Considering all these advantages, it will be clear that the pinned photodiode is the preferred choice for CMOS image sensor pixels. Almost all products on the market these days make use of this pixel architecture, and it is the pinned photodiode that really boosted the introduction of CMOS image sensors into commercial products. Apparently history is repeating : also the CCD business really took off after the introduction of the pinned photodiode [8].

The active CMOS pixel with a pinned photodiode is characterized by 4 transistors and 5 interconnections in each pixel, and this "complicated" architecture results in a relatively low fill factor. From the overview sketched in Figure 1, it is clear that it is very hard to make pixels smaller than 3 μm based on the PPD concept. The in-pixel periphery consumes too much space.

An answer to this issue can be found in the "shared pixel" concept : several neighboring pixels share the same output circuitry [9, 10]. The basic idea is illustrated in Figure 6 : a group of 2 by 2 pixels have in common the source follower, the reset transistor, the addressing transistor and the readout node. Next to the listed components, the cluster of pixels has 4 pinned photodiodes and 4 transfer gates. The timing of pixels becomes a bit more complicated, but the shared pixel architecture is now characterized by 8 interconnects and 7 transistors, resulting in 2 interconnects and 1.75 transistors per photodiode. The positive effect on the fill factor should be clear. The price one has to pay for the shared pixel concept is an asymmetry in pixel design, the four individual pixels of a cluster as shown in Figure 6 are no longer identical. This results in a fixed-pattern noise component that needs to be corrected during the image-processing phase.
Recently reported image sensors with pixel sizes smaller than 3 μm and even down to 1.45 μm are all based on the shared pixel concept with pinned photodiodes. Today's most popular shared-pixel structure is based on the one shown in Figure 6, but it is expected that architectures with less transistors will be developed to shrink the pixel size further.

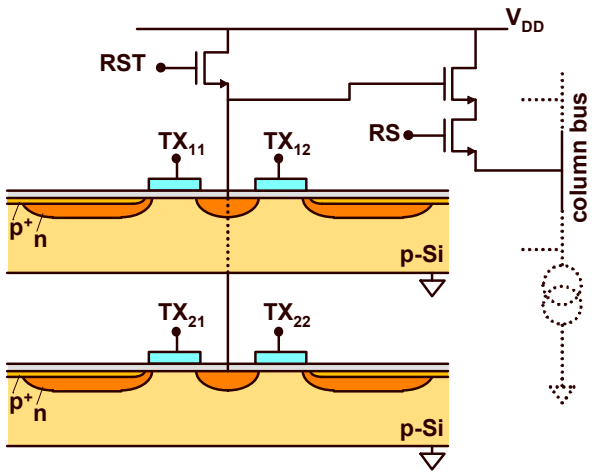

Figure 6. Shared pixel concept : a group of 2 by 2 pinned-photodiode pixels share the same reset transistor and in-pixel amplifier.

III. PHOTON SHOT NOISE

Image sensors are characterized by many different noise sources, which can be categorized in temporal noise and spatial noise sources. Examples are :
- temporal noise : kTC noise, Johnson noise, flicker noise, RTS noise, dark current shot noise, photon shot noise, power supply noise, phase noise, quantization noise, …,
- spatial noise : dark fixed pattern, light fixed pattern, column fixed pattern, row fixed pattern, defect pixels, dead and sick pixels, defects on and in the cover glass, ….

It is not the purpose of this paper to study all these noise sources, only one important noise component will be discussed : the photon shot noise. This is the noise component due to the statistical variation in the amount of photons impinging the sensor during the exposure time. The latter is a stochastical process that can be described by Poisson statistics. If a pixel receives an amount of photons, equal to μ_{ph} during the exposure time, then this value μ_{ph} is the average value, that is also characterized by a noise component σ_{ph}, being the photon shot noise. The relation between average value μ_{ph} and its associated noise σ_{ph}, is given by :

$$\sigma_{ph} = \sqrt{\mu_{ph}} \ .$$

After absorption of the incoming photons into the silicon, the flux of μ_{ph} photons results in μ_e electrons in every pixel, characterized by a noise component σ_e, connected by the same square root relation.

This ever-present photon shot noise component has a very interesting impact on the signal-to-noise behavior of an imaging system : in the case of a perfect noise-free imager in a perfect noise-free camera, the performance of the camera system is fully photon-shot-noise limited. The maximum signal-to-noise ratio $(S/N)_{MAX}$ is then given by :

$$\left(\frac{S}{N}\right)_{MAX} = \frac{\mu_e}{\sigma_e} = \frac{\mu_e}{\sqrt{\mu_e}} = \sqrt{\mu_e} \ ,$$

or, the maximum signal-to-noise ratio is equal to the square root out of the signal value ! This observation leads to an interesting rule of thumb : to make decent images for consumer applications, a minimum signal-to-noise ratio of 40 dB or more is needed, translated by means of the abovementioned formula into 10,000 electrons within every pixel. (This number tends to slowly go down due to extensive image processing and image-noise removal.)

On one hand, while the CMOS technology is shrinking further down, allowing for smaller pixels, the lower limit of the pixel size will no longer be determined by the minimum dimensions set by the CMOS technology, but it will be determined by the amount of electrons that can be stored in the pixel.

IV. ANALOG-TO-DIGITAL CONVERTERS FOR CMOS IMAGE SENSORS

It should be clear that in the era of digital imaging, most CMOS image sensors are provided with an analog-to-digital converter allowing the output signal to be accessible in the digital domain. Classical ADC architectures can be used in combination with the CMOS imager, e.g. flash converter, sigma-delta converter, successive approximation, single-slope ADC, pipelined ADC, cyclic ADC, etc. Only one particular architecture will be discussed in this paper : the single-slope ADC. This concept is very appealing in the case the CMOS imager is provided with an ADC for every column or even for every pixel. Especially column-parallel conversion has some very interesting advantages for high-speed applications. Because in this case the sensor chip has as many ADCs as it has columns, and all these ADCs work fully in parallel [11].

The basic working principle of the single-slope ADC is illustrated in Figure 7. The analog input signal V_{IN} that needs to be converted, is compared to an analog ramp signal V_{ramp}. A digital counter generates the latter. At the moment that the two voltages V_{IN} and V_{ramp} are equal to each other, the comparator changes state and latches the counter value into a memory. The data stored into the memory will be the digital value corresponding to the analog input voltage V_{IN}. In the case of column-parallel conversion, the imager has at every column a comparator and a digital memory. The digital counter is common for all pixels on a single row.

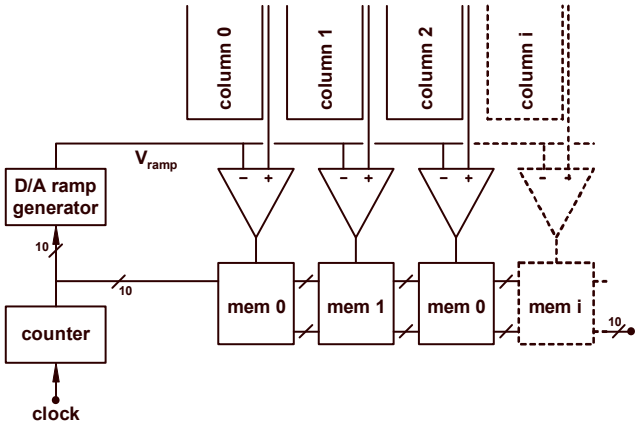

Figure 7. Basic architecture of a column-parallel, single-slope analog-to-digital converter.

After digitization, the output signal of the camera will have an extra quantization noise component σ_{ADC}, equal to :

$$\sigma_{ADC} = \frac{V_{LSB}}{\sqrt{12}} \ ,$$

with V_{LSB} being the analog voltage of the least significant bit.

In relation to the photon shot noise, an interesting observation can be made : the noise floor in the output signal of an image sensor is always (best-case) determined by the photon shot noise. The latter will be small for small output signals of the sensor, but it will be large for large output signals of the sensor. In the case of a large output signal, the quantization error of the ADC does not have to be as low as it should be for smaller output signals. This idea allows an ADC converter with an adaptive quantization step : small for small signals, large for large signals. This idea can be relatively easily implemented by means of the single-slope ADC. In that case the ramp, generated originally by the digital counter, will be no longer linear with

respect to the time, but can have a piece-wise-linear approach as shown in Figure 8 [12]. Next to the ramp itself, in Figure 8 also the photon shot noise is indicated as well as the quantization noise. It can be seen that when the quantization step is increased, the quantization noise is increased as well. But as long as it stays well below the photon-shot noise, it will not hamper the performance of the sensor. In this simple example (in which the quantization noise is kept a factor of 2 below the photon-shot noise), the ADC is changing from a single-slope to a so-called multi-slope ADC. In this way, its speed is increased by a factor of 3 without further increasing its power consumption.

Another way of increasing the speed of the single-slope ADC is changing the concept to a single-slope, multiple ramp concept. In this configuration, several ramps are running in parallel, they all have the same slope, but they differ from each other by a DC off-set [13]. Before starting the conversion, a coarse ADC action is performed, to assign every column of the image sensor to a dedicated ramp. The coarse conversion is followed by a fine conversion cycle, and at the end, both results are combined. In Figure 9, the multiple-ramp concept is illustrated : at first the coarse action is taking place and its output is memorized in a 2-bit memory cell (2 bits in this example with 4 parallel ramps).
These 2 bits not only represent the most significant bits of the digital words, but they also contain the information to which ramp the column needs to be assigned for the fine conversion. During the latter, the four parallel ramps are offered to all columns, but every column is checked against only one particular ramp. It should be clear that the increase in speed is about equal to the number of parallel ramps (neglecting the time needed to perform the coarse ADC).

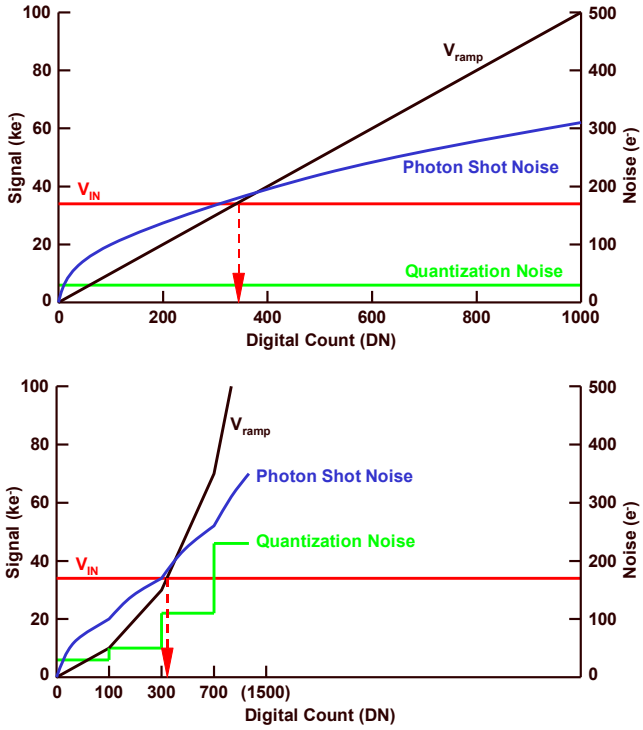

Figure 8. Ramp voltage for the single slope (top) and multi slope (bottom) analog-to-digital converter, in relation to the photon shot noise and quantization noise.

V. CONCLUSION

CMOS image sensors made a huge technological progress over the last decade. The introduction of the pinned photodiode really boosted their success. Exploring the typical characteristics, needs and requirements of the imaging application can result in very attractive circuits and devices that increase the performance of the imagers. Because of the ever-shrinking dimensions in CMOS technology, further integration on column level and even on pixel level can make the imagers even smarter than they are already.

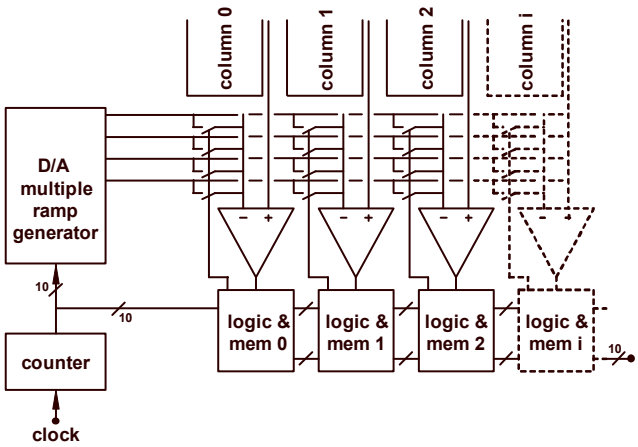

Figure 9. Basic architecture of a column-parallel, multi-slope analog-to-digital converter.

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