

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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SAMSUNG ELECTRONICS CO., LTD., AND  
SAMSUNG ELECTRONICS AMERICA, INC.,  
Petitioner,

v.

CELLECT, LLC,  
Patent Owner.

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Case IPR2020-00512  
U.S. Patent No. 9,186,052

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**DECLARATION OF DR. MICHAEL LEBBY  
IN SUPPORT OF PATENT OWNER'S RESPONSE**

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## **I. INTRODUCTION**

1. I, Michael Lebby, Ph.D., have been retained on behalf of Collect, LLC in connection with this *inter partes* review trial concerning U.S. Patent 9,186,052 (“the ’052 Patent”). The trial was initiated by Samsung Electronics Co., LTD., and Samsung Electronics America, Inc., which I will collectively refer to as “Samsung” or “Petitioner.” If called upon to testify, I can and will testify regarding the matters set forth herein.

### **A. Compensation**

2. I am being compensated for my work in this matter. My compensation does not depend on the outcome of this proceeding.

### **B. Scope of Opinions**

3. I have been asked to provide my technical opinions relating to the instituted matters at issue in this trial, *i.e.*, whether claim 2 of the ’052 Patent is valid over the obviousness challenges brought by Samsung.

4. In providing these opinions, I have also been asked to provide my technical opinions regarding the development of CMOS image sensors, including the state of the art in 1997 and through the early 2000s. Further, I have been asked to opine on the market for solid-state imagers for this time-period and how that affected the design and development of the CMOS image sensors and applications and relates to the understanding of a person or ordinary skill in the art (“POSITA”) at the time.

**C. Summary of Opinions**

5. My opinion is that the challenged claim 2 is valid as it would not have been obvious to a person having ordinary skill in the art (which I understand is sometimes abbreviated “POSITA”) over the art asserted by Petitioner as of the earliest claimed priority date, which I understand here is October 6, 1997<sup>1</sup>. Ex. 1001 at 1. Bucking the CMOS “camera on a chip” trend, the ’052 Patent discloses strategically de-integrating certain imager components would enable miniaturization theretofore unachievable:

Although the “camera on a chip” concept is one which has great merit for application in many industrial areas, a need still exists for a reduced area imaging device which can be used in even the smallest type of endoscopic instruments in order to view areas in the body that are particularly difficult to access, and to further minimize patient trauma by an even smaller diameter invasive instrument.

’052 Patent at 3:24-30. Indeed, the inventors also found unexpected benefits associated with the particular arrangement of imager components claimed in the ’052 Patent. Specifically, the inventors realized that maintaining timing and control circuitry on the same plane as the pixel array, while removing the remaining circuitry (e.g. video conversion circuitry) to a separate circuit board or box

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<sup>1</sup> The ’052 Patent, filed on May 6, 2015, as U.S. Application 14/705,334, claims priority to U.S. Patent No. 5,929,901 (Ex. 2029), filed October 6, 1997, through a series of continuation and continuation-in-part applications.

obviated the need for “shielding to avoid RFI effects,” which previously required “great efforts.” Ex. 1003 at 94-95, ¶ 21.

6. In the relevant time-period, a POSITA reading *Swift* would understand that *Swift* describes a security and surveillance camera intended for use inside a door. Further, a POSITA would understand that *Swift* describes alternate embodiments using either, (1) a CCD image sensor and off-chip architecture, or (2) an APS CMOS image sensor described by Dr. Eric Fossum with a camera-on-a-chip architecture (which *Swift* expressly cites/references). *See, e.g.*, Ex. 1005 at 12, Figure 2. This is evident from the architecture shown in *Swift*. For example, Figure 7 (CMOS embodiment) shows circuit board 201, including a section of the circuit board containing the pixel array. A POSITA would know that board 201 includes both the light collecting portion (*i.e.*, CMOS pixels) and additional space for circuitry needed for signal processing and timing and control as described in Dr. Fossum’s camera-on-a-chip design.

7. A POSITA would not have combined the APS CMOS camera-on-a-chip architecture cited in *Swift* with the off-chip CCD architecture also shown in *Swift*. These two embodiments, CCD and CMOS, in *Swift* are incompatible and combining the off-chip architecture in the CCD embodiment with CMOS architecture would have increased costs and reduced performance. For example, *Swift* cites to a 1993 Laser Focus World article which states (at p. 85) that

“Although some integrated CMOS/CCD processes have been demonstrated, undesirable compromises in the performance of CMOS or CCD technology must be made.”

8. For similar reasons, a POSITA would not have combined *Larson’s* CCD camera with CMOS image sensors in *Swift* (or *Ricquier*).

9. Additionally, a POSITA would not have combined *Swift’s* in-door security camera with the housing and imager design in *Suzuki* because it provides no technical benefits or cost savings advantages. *Swift* describes a “miniature camera” ranging in size from 100 mm to 38 mm and is approximately 6.5x to 2.5x bigger than the camera head design in *Suzuki* (e.g., 15 mm). A POSITA would not have unnecessarily reduced the size of the sensor in *Swift* to the size of the sensor used in *Suzuki*. Further a POSITA would not have had any reason to look to *Suzuki* to limit the size of the image sensor, which reduces resolution and imposes unnecessary performance constraints. Ex. 1015 at 1:28-43.

10. Further, a POSITA would not have looked to the passive CMOS image sensor in *Ricquier* for several reasons. First, a passive CMOS image sensor would not have met the design and application criteria required in *Swift’s* security camera architecture because at the relevant time period, passive CMOS image sensors were not acceptable for the application due to poor image quality, which could be measured using a variety of tests (e.g., various standards for measuring

the signal and noise, including fixed pattern noise, read noise and dark current), especially in low-light conditions. *See e.g.*, Ex. 2058 (Holst) at 92; Ex. 2036 (OIDA) at 8 (“**CCDs have historically been the dominant image sensors** and have been very successful in high speed **applications such as digital cameras, digital copiers, and flat bed scanners**. CCDs are also appropriate for surveillance and manufacturing applications where high performance is a requirement. **CCDs have traditionally had better light sensitivity** as a result of their pixel architecture, where all of the light hitting the array can potentially be converted to signal.”) (emphasis added).

11. Additionally, *Ricquier* describes a bench-test setup used for machine vision where the touted benefit is the use of X-Y addressable CMOS pixels and selectable resolution. A POSITA would understand that separating timing and control from the pixel was only done for convenience in developing the pixel array and negatively impacts performance, which is why *Ricquier* expressly states that the goal is for cointegration of the clock driving unit onto the image sensor. Ex. 1033 (*Ricquier*) at 8.

12. A POSITA would understand that the camera-on-a-chip design was important to improving performance and reducing the overall size and weight of a device. For example, in the same year as Dr. Fossum’s article was, identified in *Swift*, Dr. Fossum published numerous articles stating that the low-cost promise



and advantage of CMOS is allowed with on-chip integration. *See, e.g.*, Ex. 2004 (Fossum LFW) at 4 (“To get high transfer efficiency, CCDs are often driven with **relatively large voltages** (by microelectronics standards). They also represent high enough capacitance loads to driving electronics to make on-chip integration of clocks and drivers nearly impractical. Yet, **on-chip integration is the key to achieving future camera miniaturization.**”)

13. A POSITA would have also been aware of references in the field that camera-on-a-chip design was the major benefit of using CMOS image sensors in 1997. Ex. 2007 (Zarnowski) at 7 (“The combination of standard CMOS fabrication and **on-chip electronics** to lower external system costs yields the most economical solution.”); Ex. 2039 (Armstrong) at 2 (“One chip can **incorporate all manner of electronic controls that are usually on multiple chips**, from timing circuits to zoom and anti-jitter controls. By consolidating many functions and reading images in a more efficient way, it requires one-hundredth the power of a CCD-based system. And the chip does its own conversion from **analog to digital for output** on computer monitors or disk storage.”)

14. In summary, a POSITA would never have mixed and matched *Swift* with *Suzuki*, *Ricquier* or *Larson*.

**D. Materials Relied Upon**

15. In reaching the conclusions described in this declaration, I have relied on the documents and materials cited herein and are identified in Appendix A attached to this declaration. These materials comprise patents, related documents, and printed publications. Each of these materials is a type of document that experts in my field would have reasonably relied upon when forming their opinions and would have had access to either through the applicable patent offices and/or well-known libraries, conferences, publications, organizations and websites in the field as further discussed herein.

16. In the preparation of this declaration, I have also reviewed Exhibits filed in this case by Petitioner.

17. My opinions are also based upon my education, training, research, knowledge, and personal and professional experience.

**II. BACKGROUND AND QUALIFICATIONS**

18. All of my opinions stated in this declaration are based on my own personal knowledge and professional judgment. In forming my opinions, I have relied on my knowledge and experience in designing, developing, and researching semiconductor image based and optical/optoelectronic technology. My experience and education are detailed in my curriculum vitae, which is attached as Appendix B to this report.

19. I am currently Chief Executive Officer (CEO) and Chief Technology Officer (CTO) of Oculi, LLC. Oculi, LLC is my consulting company, where I engage in my expert witness work. I also serve as a Technical Expert/Consultant for the Photonics Unit of the European Commission. In my work at the European Commission, I review and advise on general photonics technology that includes image sensors and other light detecting mechanisms.

20. I received a Bachelor of Electrical Engineering degree in 1984, a Master of Business Administration in 1985, and a Doctorate degree in 1987, all from University of Bradford in the United Kingdom. Each of my academic degrees involved significant studies in optoelectronics, optics, sensors (including image sensors); solid-state physics; semiconductor devices; microelectronics. For example, my Ph.D. thesis involved the design and fabrication of both optoelectronic and electronic semiconductor devices, and their associated characterization, packaging, and assembly onto printed circuit technology platforms.

21. Additionally, I was awarded a Doctor of Engineering degree from University of Bradford in 2004 for my technical contributions to the field, with citation to “Technical Contributions to Optoelectronics.”

**A. Research and Professional Experience**

22. My career started in the late 1970s at the Ministry of Defense in UK where I spent time at their R&D facility in Malvern (RSRE – Royal Signals and Radar Establishment). I worked on semiconductor device design, fabrication, and characterization, and especially materials using Group IV silicon semiconductors as well as Group III-V compound semiconductors.

23. My research work in semiconductor device design then took me to ATT Bell Laboratories in 1985 where I pursued research in novel device designs using III-V semiconductor material systems that included field-effect transistors (FETs), bipolar transistors, light-emitting diodes (LEDs), laser diodes and photodetectors. The devices researched became the subject of my PhD thesis that was granted in 1987.

24. I moved to Motorola in 1989 to further develop my semiconductor engineering and development skills and became a Research and Development Manager for Motorola in the photonics division until I left the company in 1998. During my time at Motorola, I worked on many photonic technology projects that included optical interconnects, solar, displays, cameras, image sensors, LEDs and laser devices as well as the packaging and reliability of mobile product prototypes. At Motorola, my research work involved investigating various designs using both silicon CMOS technology as well as compound semiconductor technology.

25. Between 1998-1999, I worked as the Director of Technology/BD (Fiber Optics) for Tyco Electronics (previously AMP). I joined Tyco Electronics as a member of the Global Optoelectronics Division's management team. There, I was responsible for growing the optoelectronics business through external interactions that include mergers, acquisitions, strategic alliances, and technical strategic planning.

26. In 1999, I left Tyco and started employment at Intel. At Intel, I was involved heavily in photonic technology and especially those that supported silicon photonic device platforms. As a culmination of this work, I was one of Intel's founders of its silicon photonics division in the year 2000 and worked to set up a fabrication facility in South San Jose. I was also part of Intel Capital's optical investment team and participated on over 30 photonics investments into photonics and especially devices, packaging and modules. Technologies investigated included lasers, LEDs, solar cells, image sensors, cameras, and displays.

27. In 2005, I took up employment for a trade association called OIDA based in Washington DC with photonics manufacturers that included solar cells, fiber optics, display, camera sensing, defense, aerospace, LED lighting, and automotive vendors as members. As head of this trade association, I was responsible in part for industry-based technology roadmaps and implemented common industry roadmap methodologies with common features such as "Red

Brick Walls” and transferred them into optoelectronics roadmaps for the industry where technologies such as solar cells, LEDs, fiber-optics, optics, fiber, optical camera sensors, displays, and their associated packaging were featured.

28. In 2010, I became the General Manager and CTO of Translucent, Inc., a high-tech start-up company which developed and manufactured silicon and rare earth oxide based epitaxial semiconductor wafers. One of the key drivers at Translucent was to develop a new and novel platform for the growth of high performance solar cells and advanced CMOS device designs (which were patented).

29. As discussed in more detail in my *curriculum vitae* (Appendix B) to this declaration), I have continued to work in the semiconductor, electronics, optoelectronics, and photonics detection field throughout my career.

## **B. Professional Associations**

30. Throughout my career I have also had an active role in a number of technical, professional organizations, including, among others, IEEE Components, Packaging, and Manufacturing Technology (CPMT), IEEE Electronic Components and Technology Conferences (ECTC); IEEE TC-10 (Technical Committee on Optoelectronics), and IEEE Optoelectronics Industry Development Association (OIDA). Through these organizations, I have consistently been a part of

committees, events, and workshops relating to semiconductor, electronics, and camera sensor technology.

**C. Patents & Publications**

31. My work has also led to 230 USPTO utility patents and 80 published patent applications in semiconductors, electronics, and optoelectronics. I also hold over 450 patents internationally. Additionally, I am the author of more than 60 publications.

**D. Other Awards**

32. My work has been recognized through several awards over the years. These awards include Photonic Integrated Circuits Conference Entrepreneur and Business Leader of the Year (2018), Fellow of the Institute of Electrical and Electronics Engineers Fellowship (2005), and Fellow of the Optical Society (2007). Given my IP and Inventorship contributions, the USPTO cited me to be in the most prolific 75 inventors in the country from 1988-1997.

**III. LEGAL PRINCIPLES**

33. I am not a lawyer, and I have not been asked to offer opinions on the law. As a technical expert trying to assist the Patent Office, I understand that my technical analysis necessarily involves applying certain legal principles. In particular, counsel asked me to apply the following legal principles in my analysis, and I believe that I have.

**A. Person Having Ordinary Skill in the Art**

34. A patent's claim terms are to be interpreted according to the understanding of the person of ordinary skilled in the art at the time of the invention. (Counsel has asked me to assume for this a date of October 6, 1997.) That "person of ordinary skilled in the art" (a POSITA) is a hypothetical construct.

35. I understand that the factors to be considered in determining the level of ordinary skill in the art to be: (1) the educational level of active workers in the field, including the named inventors of the patent; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) the rapidity with which innovations are made; and (5) the sophistication of the technology in the art. As mentioned above, I understand the priority date of the '052 Patent to be October 6, 1997.

36. Based on my review of the '052 Patent and my consideration of the above-mentioned factors, it is my opinion that a person of ordinary skill in the art (POSITA) at the time of the invention of the '052 Patent would be someone with a bachelor's degree in Electrical Engineering, Physics, or related field of study and at least 3 years of experience in the field of solid-state image sensors. Additional graduate education could substitute for some professional experience, but solid-state image sensors were rapidly developing and at least 1-2 years of experience in the field of solid-state image sensors would be necessary.



37. Additionally, the POSITA is deemed to have been aware of all of the art that existed as of the time of the invention, and to know what those actually working in the field at the time knew.

**B. Nonobviousness**

38. I have been informed that even if a single reference does not contain every limitation of a patent claim, it can still invalidate that claim if it renders the claimed invention obvious when considered in light of other prior art references or devices. If the differences between the claimed invention and the prior art are such that the claimed invention, as a whole, would have been obvious to a person having ordinary skill in the art at the time the invention was made without the benefit of hindsight, then the claim is invalid.

39. I have been informed that the analysis of obviousness involves several factual inquiries including the scope and content of the prior art, the differences between the prior art and the claim, and the level of ordinary skill in the art at the time of the invention.

40. I have been informed that a reference qualifies as prior art for obviousness purposes when it is analogous to the claimed invention. The test for determining what art is analogous is: (1) whether the art is from the same field of endeavor, regardless of the problem addressed, and (2) if the reference is not

within the field of the inventor's endeavor, whether the reference still is reasonably pertinent to the particular problem with which the inventor is involved.

41. I have been informed that to determine whether a combination of known elements would have been obvious to a person of ordinary skill in the art at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

42. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Additionally, I understand that a patent is likely to be invalid for obviousness if a person of ordinary skill in the art can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an obvious solution encompassed by the patent's claims. A combination is not obvious, however, where the combination cannot be implemented without undue experimentation or when the motivation to create the combination comes from hindsight.

43. I have been informed that when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill in the art has good reason to pursue the known options within his or her technical grasp. I understand that, if this leads to

anticipated success, it is likely the product not of innovation, but rather of ordinary skill and common sense. I have been informed that the fact that a combination was obvious to try might show that the patent claim was obvious.

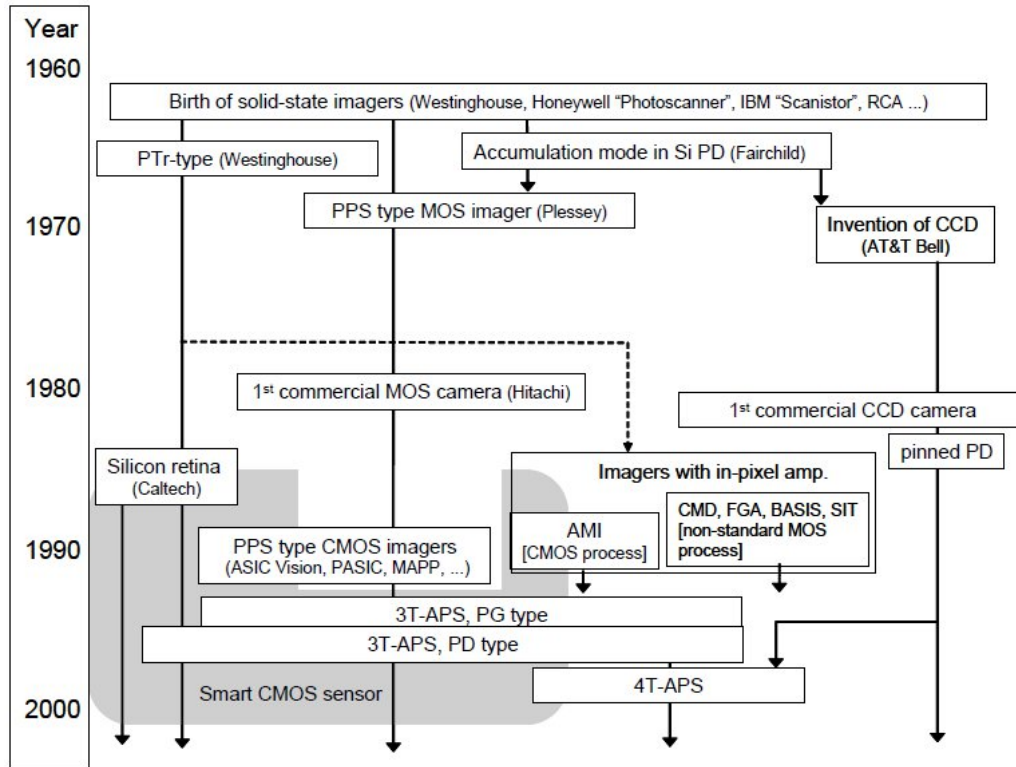
44. I have been informed that, even when all claim limitations can be found in a combination of prior art references, the fact-finder must consider as part of the obviousness determination not only what the prior art teaches, but whether the prior art teaches away from the claimed invention and whether there is a motivation to combine teachings from separate references in the manner claimed.

#### **IV. STATE OF THE ART**

##### **A. The Development of Image Sensors**

45. In 1997, and throughout the early 2000s, CCD imagers dominated the image sensor market for industrial applications, including satellite and mobile wireless systems, military, and medical devices.

46. The timeline below (copied from Ex. 2069 (Ohta) at p. 3) provides a brief overview of the major milestones in the development of image sensors, including, CCD, MOS and CMOS image sensors. *Id.* (excerpts from Jun Ohta, *Smart CMOS Image Sensors and Applications* (Brian J. Thompson ed., CRC Press 2008).



**FIGURE 1.1**  
Evolution of MOS image sensors and related matters.

47. As reflected above, the birth of solid-state imagers<sup>2</sup> first began with the development of metal-oxide-semiconductor field-effect transistor (MOSFET or

<sup>2</sup> Although the term “solid-state imagers” refers to devices using solid semiconductors, in contrast to vacuum tubes (*e.g.*, vidicon tube cameras), solid-state imagers cover different technologies that may not use compatible/interchangeable semiconductors such as CCD (only PMOS or only NMOS) and CMOS (both PMOS & NMOS), even though they may both fall under the general use of term of solid-state imager. The term existed even before the first CMOS image sensor was invented, and use of the term “solid-state” image sensor does not necessarily mean or imply a CMOS image sensor. For example, Van Nostrand Reinhold Dictionary of Information Technology (3d ed. 1989) defines “solid-state camera” to mean “In television, a television camera in which optical image is projected onto a large-scale integrated circuit device, typically a charge-coupled device, which detects the light image and develops the television signal. *See* charge-coupled device”). Ex. 2091.

MOS transistor) which were invented in 1959 at Bell Labs. The term MOS (or “metal–oxide–semiconductor”) is a reference to the physical structure of MOS field-effect transistors, having a metal gate electrode placed on top of an oxide insulator, which in turn is on top of a semiconductor material.

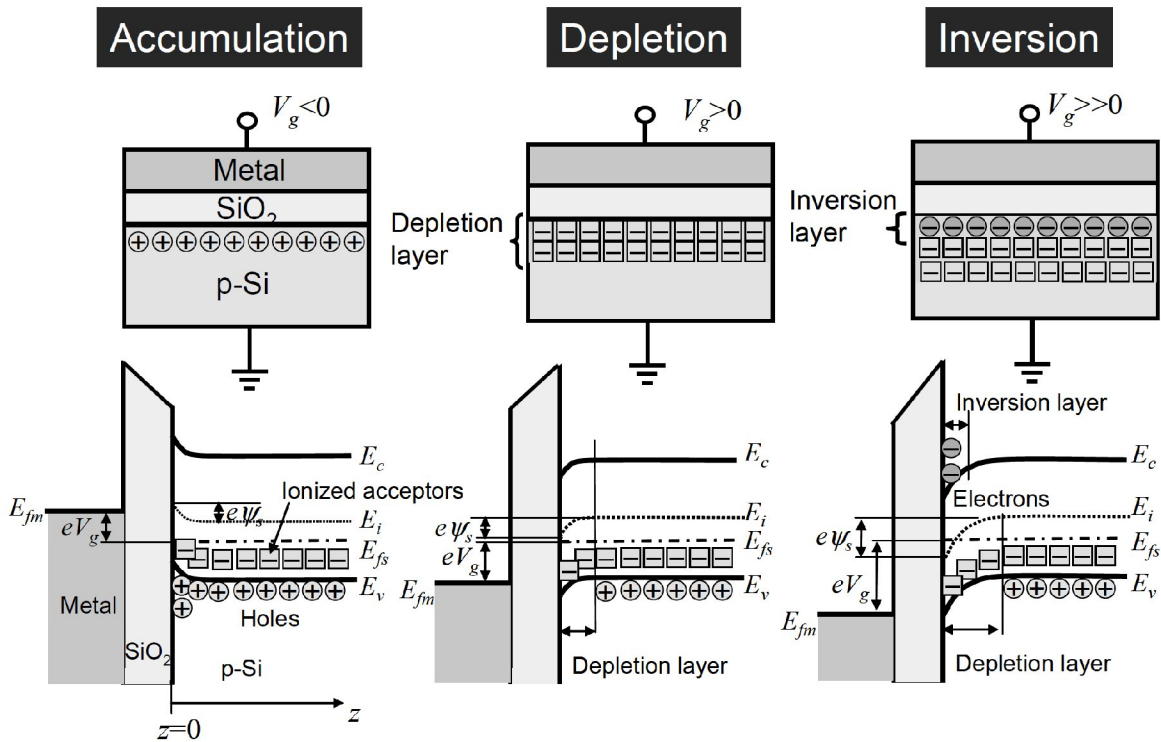
48. There were originally two types of MOSFET fabrication processes, PMOS (p-type MOS) and NMOS (n-type MOS). For example, a PMOS transistor is fabricated using p-doped metal–oxide–semiconductor capacitors. Although aluminum was once used, polysilicon replaced aluminum and is used in traditional fabrication of MOS. Other metal gates have also made a comeback with the advent of high- $\kappa$  dielectric materials.

49. In working with MOS capacitors, it was learned that photons could be converted and into an electric charge that could then be stored on a MOS capacitor. These MOS capacitors became the basic building blocks of an image sensor invented around 1968 (passive pixel sensor (PPS) in 1968 and charge-couple device (CCD) in 1969). *See* Ex. 2078 ([https://en.wikipedia.org/wiki/Charge-coupled\\_device](https://en.wikipedia.org/wiki/Charge-coupled_device)) at 1-2.

50. Solid-state imagers generally leverage and utilize MOS capacitors, a two-terminal device, and/or metal-oxide semiconductor field-effect transistors (MOSFETs), a four-terminal device—wherein both serve as the bases for modern image sensors. Ex. 2069 (Ohta) at 208-11. “A MOS capacitor is composed of a

metallic electrode (usually heavily doped polysilicon is used) and a semiconductor with an insulator (usually SiO<sub>2</sub>) in between.” *Id.* at 208. A MOS capacitor may be represented by a series sum of two capacitors, a gate oxide capacitor  $C_{ox}$  and a depletion region capacitor  $C_D$ . *Id.* In turn, the structure of a MOSFET, such as one implemented in standard CMOS technology, leverages the features of a MOS capacitor “by connecting the source and drain of a MOSFET” such that “the gate and body of the MOSFET act as the electrodes of a capacitor.” *Id.*

51. MOS capacitors have three modes: accumulation, depletion, and inversion, wherein each mode is “characterized by surface potential  $\psi_s$ ” relative to  $\psi_B$ , the surface potential  $e\psi_s$  is defined as “the difference of the mid-gap energy between the surface ( $z = 0$ ) and the bulk region ( $z = \infty$ ),” and the  $e\psi_B$  is defined as “the difference between the mid-gap energy at the bulk region  $E_i(\infty)$  and the Fermi energy  $E_{fs}$ .” *Id.* In accumulation mode, the surface potential  $\psi_s$  of the MOS capacitor is less than zero, the gate bias voltage is less than zero,  $V_g < 0$ , and holes accumulate near the surface. *Id.* In depletion mode, the surface potential  $\psi_s$  is “positive but smaller than  $\psi_B$ ” when “a positive gate bias  $V_g > 0$  is applied and causes free carriers to be depleted near the surface region.” *Id.* “Space charges of ionized acceptors are located in the depletion region and compensate the induced charges by the gate voltage  $V_g$ ,” as shown in the figure below. *Id.* at 208-09.



**FIGURE D.1**

Conceptual illustration of the three modes of MOS capacitor operation, accumulation, depletion, and inversion.  $E_c$ ,  $E_v$ ,  $E_{fs}$ , and  $E_i$  are the conduction band edge, valence band edge, Fermi energy of the semiconductor, and mid-gap energy, respectively.  $E_{fm}$  is the Fermi energy of the metal.  $V_g$  is the gate bias voltage.

Ex. 2069 (Ohta) at 209, Fig. D.1.

52. Inversion mode is a mode “used in a MOSFET when it turns on and in CMOS image sensors to accumulate photo-generated charges” shown above, when  $\psi_s$  is greater than  $\psi_B$  and gate bias voltage  $V_g$  is much greater than 0,  $V_g \gg 0$ , or once  $E_i$  at  $z = 0$  intersects  $E_{fs}$  such that  $\psi_s = \psi_B$ , an inversion layer appears such that “the non-equilibrium state can act as a reservoir for electrons when they are generated, for example by incident light,” also known as “a potential well for

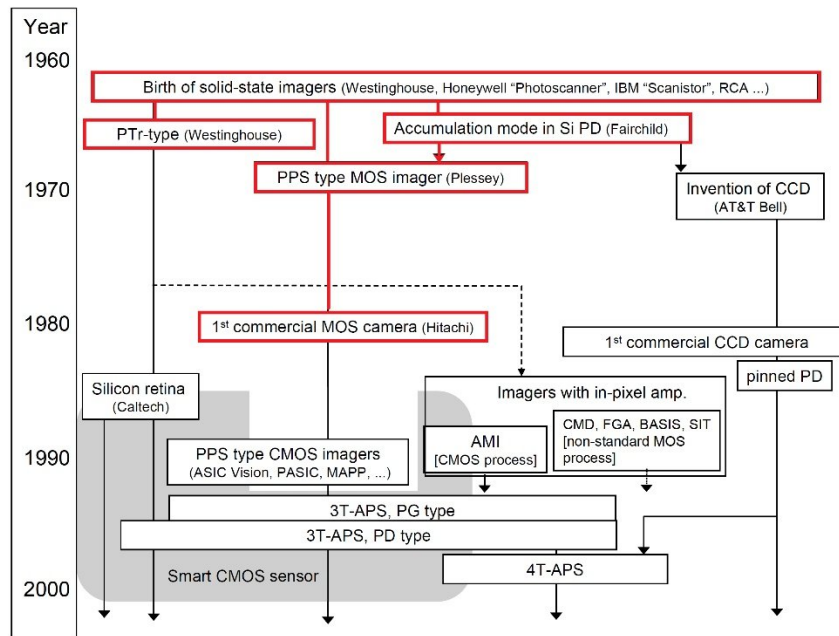
photo-generated carriers.” Ex. 2069 (Ohta) at 208-09. In the case of a MOSFET, electrons are supplied to the inversion layer “from the source and drain regions, so that an inversion layer filled with electrons is established in a very short time.” *Id.* at 209.

## **B. Types of Solid-State Imagers**

### **1. Metal-Oxide Semiconductor (MOS) Imagers**

53. The pedigree of present-day CMOS imagers can be traced to the first MOS imagers using nMOS transistors. For instance, the “scanning function in X-Y addressed silicon-junction photosensing devices [was] proposed in the early 1960s by S.R. Morrison at Honeywell as the ‘photoscanner’ and by J.W. Horton et al. at IBM as the ‘scanistor,’” while Schuster and Strull at NASA developed “phototransistors (PTrs), as photodetectors, as well as switching devices to realize X-Y addressing.” Ex. 2069 (Ohta) at 21. As another example, the accumulation mode in a photodiode was first proposed by G.P. Weckler at Fairchild Semiconductor, which uses the floating source of a MOSFET as a photodiode. *Id.* These achievements regarding properties inherent in MOS imagers are represented in the annotated chart below in red.





**FIGURE 1.1**  
Evolution of MOS image sensors and related matters.

Ex. 2069 (Ohta) at 21, Fig. 1.1 (annotated).

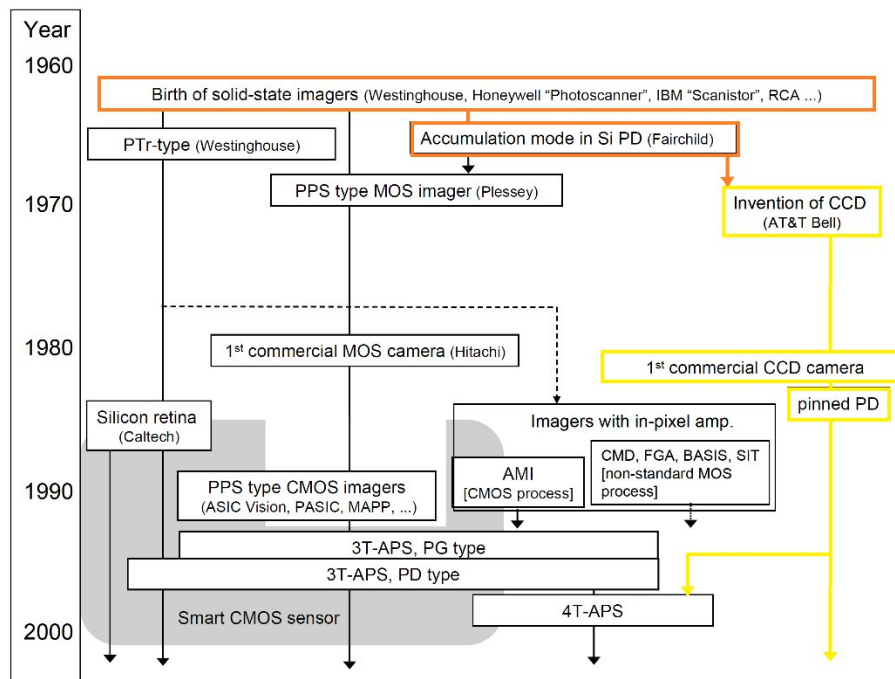
54. By 1968, Peter Noble at Plessey was credited for developing one of the first MOS image sensors or passive pixel sensor (PPS), which consisted of “a photodiode and a switching MOS transistor in a pixel with X- and Y-scanners and a charge amplifier.” *Id.* at 20. Indeed, in Noble’s IEEE article in 1968, he hinted “in the area of possible future developments” the possibility of “the combination of photodiodes with logic in a self-adapting manner for pattern recognition purposes,” which later came to fruition in CMOS imagers. Ex. 2068 (Noble) at 8.

55. Historically, passive pixel sensors (PPS), which included only one transistor per pixel, were developed first, then active pixel sensors (APS) were

developed to improve image quality, which included three transistors per pixel. *Id.* at 55.

## 2. Charge-Coupled Device (CCD) Imagers

56. Shortly after Noble's invention of a passive-pixel-sensor-type MOS imager, W. Boyle and G.E. Smith of AT&T Bell Labs invented the first CCD imager in 1969. Ex. 2069 (Ohta) at 22. These advancements regarding CCD imagers are represented in the annotated chart below in yellow.



**FIGURE 1.1**  
Evolution of MOS image sensors and related matters.

Ex. 2069 (Ohta) at 21, Fig. 1.1 (annotated).

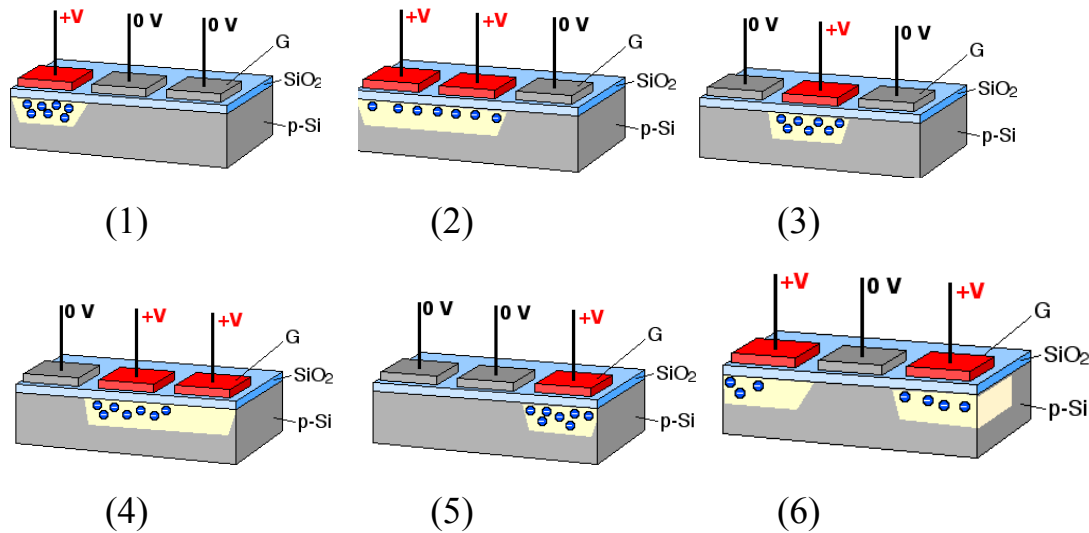
57. CCD image sensors are fabricated using either NMOS or PMOS technology. *Id.*; see also Ex. 2078 (<https://en.wikipedia.org/wiki/Charge->

[coupled\\_device](#)) at 1-2]. Initially developed as semiconductor bubble memory, CCDs resembled “a shift register type structure in which the presence or absence of a magnetic dipole representing 0s and 1s which were moved along by a rotating external magnetic field.” Ex. 2072 (Smith) at 1.

58. Combining a shift-register-type structure with a silicon diode array camera tube and working knowledge of the MOS capacitor, Boyle and Smith addressed two problems. First, Boyle and Smith addressed the problem of storing a packet of charge “in a confined region” by leveraging MOS capacitors in depletion mode. *Id.* at 1-2. In so doing, “[c]harge can than [sic] be introduced into this depletion region with the amount of charge stored being the magnitude of the signal.” *Id.* at 2. Second, Boyle and Smith tackled the problem of “shifting the charge from one site to another, thereby allowing manipulation of the information.” *Id.* Boyle and Smith solved this by “simply placing the MOS capacitors very close together in order to pass the charge easily from one to the next by applying a more attractive voltage to the receiver.” *Id.* at 2, Fig. 4.

59. In operation, the CCD “relies on the transfer of charge . . . from under one MOS electrode to the next through sequencing of voltages on the electrodes.” Ex. 2053 (Fossum, Dinosaurs) at 2. The PMOS or NMOS capacitors are biased above the threshold for inversion when image acquisition begins, allowing the conversion of incoming photons into electron charges at the semiconductor-oxide

interface. *Id.* at 2-4. The electrical charges (representing the photons of light that were absorbed) in the CCD image sensor are then read out by transferring the stored charges. *Id.* The figures below reflect the process of capturing and releasing these charges:

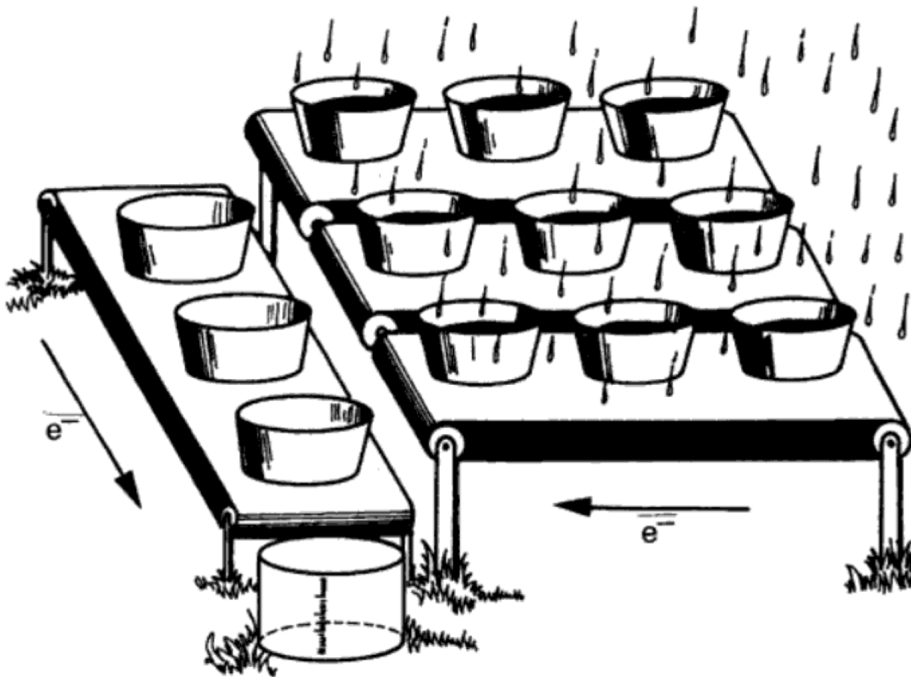


60. Referring to the figure above, once the array has been exposed to the image, a control circuit causes each capacitor to transfer its contents to its neighbor (operating as a shift register). *Id.* The last capacitor in the array dumps its charge into a charge amplifier, which converts the charge into a voltage. *Id.* By repeating this process, the controlling circuit converts the entire contents of the array in the semiconductor to a sequence of voltages and a single line is scanned out and is equivalent to a raster scan. *Id.*

61. In a digital device, these voltages are then sampled, digitized, and usually stored in memory; in an analog device (such as an analog video camera), they are processed into a continuous analog signal (*e.g.*, by feeding the output of

the charge amplifier into a low-pass filter), which is then processed and fed out to other circuits for transmission, recording, or other processing. *Id.*

62. Because the drive power requirement for CCDs increases as the CCD array size increases, and CCDs “are capacitive in nature,” “the entire CCD array must be driven to achieve the output of a single pixel.” Ex. 2053 (Fossum, Dinosaurs) at 3. The process of releasing and transferring the stored charge requires significant power. *Id.* This process has sometime been referred to as the bucket brigade to represent the flow of charge, which is inherently slow and has increased power requirements as illustrated below:



**Figure 1.7(a)** Bucket analogy used to describe CCD operation.

Ex. 2059 (Janesick) at 7, Fig. 1.7(a).

63. Due to its relative higher image quality over those of MOS and nascent CMOS imagers, over the span of intervening years, the CCD became the dominant technology. *Id.* at 2. Leading up to the relevant time and frame and for years after, “CCDs have been widely manufactured and used [is] due to the fact that they have offered superior image quality than MOS imagers,” and despite high cost level. Ex. 2068 (Noble) at 22.

### **3. Charge-Injection Device (CID) Imagers**

64. The first charge-injection device (CID) was invented a few years after the invention of the first CCD. Ex. 2053 (Fossum, Dinosaur) at 5. Compared to CCDs, however, CIDs require “only a single, intra-pixel charge transfer” and thus “are immune to the deleterious effects of imperfect charge transfer” of CCDs. *Id.* Since the charge transfer is localized within the pixel “under a floating sense gate,” the “induced voltage change is the output signal.” *Id.* Other advantages CIDs have over other solid-state imagers include: multiple, non-destructive readout capability, random accessibility of the pixels, high fill-factor, and good blue/UV response. *Id.*

65. CIDs also have its drawbacks. For example, “like the photodiode and MOS imager,” the CID suffers “from high bus capacitance since the sense gates of all pixels on a given row are tied in parallel.” *Id.* Furthermore, two drawbacks regarding CID’s capability for multiple, non-destructive readouts include “increases in readout time and a need to reduce dark current.” *Id.*

**4. Complementary-Metal-Oxide-Semiconductor (CMOS) Imagers**

66. In contrast to the CCD image sensor which use *PMOS* or *NMOS* capacitors, CMOS image sensors are fundamentally different and are fabricated using Complementary Metal-Oxide-Semiconductor (CMOS) transistors, developed in 1963. This technology uses complementary and symmetrical pairs of p-doped and n-dopes MOSFETs. In other words, it is a combination of *NMOS* and *PMOS*. Due to these underlying differences, CMOS and CCD are incompatible, requiring different underlying semiconductors, and even different voltage supply levels (*e.g.*, CCDs traditionally have higher voltage supplies to suppress noise levels which degrade signal quality). To be clear, compared to a MOS capacitor, a MOSFET includes two additional terminals—a source and a drain—each connected to individual, highly-doped regions that are separated by the bulk. Ex. 2069 (Ohta) at 208. MOSFETs come in two types: enhancement and depletion types, with CMOS imagers typically using enhancement types. *Id.* at 210. Further, MOSFETs operate in two regions: above and below threshold, and within each region, “three sub-regions exist: cutoff, linear (triode), and saturation,” wherein no drain current flows in the cutoff sub-region. *Id.* For example, in enhancement types, “the threshold of an nMOSFET is positive,” and thus, “[i]n a pixel circuit, the threshold voltage is critical for operation” of a CMOS imager. *Id.*

67. The modern integrated circuit (IC) is built using CMOS technology and complex electronics are built right into the CMOS image sensor (unlike a CCD image sensor), including timing and control and signal processing circuitry. This can be a major cost and space savings, especially for a miniaturized cell phone camera. Despite these technical advantages, CCD imagers were the dominant technology through the early 2000s because the quality (*e.g.*, signal to noise (S/N)) of the image produced by CCD, assisted by higher voltage supply levels, was far superior to CMOS. Development of the CMOS image sensor lagged behind CCDs and it was not until the work of Dr. Eric Fossum on behalf NASA's Jet Propulsion Lab (JPL), that CMOS image sensor began to garner greater attention.

68. As discussed in *Smart CMOS Image Sensors and Applications*, the APS CMOS sensor developed by Dr. Eric Fossum at NASA's JPL used a photogate (PG) as the photodetector. *See* Ex. 2053 (Fossum, Dinosaur) at 8; Ex. 2069 (Ohta) at 22.

69. The APS PG detectors, could not, in terms of image quality, compete with CCD image sensors:

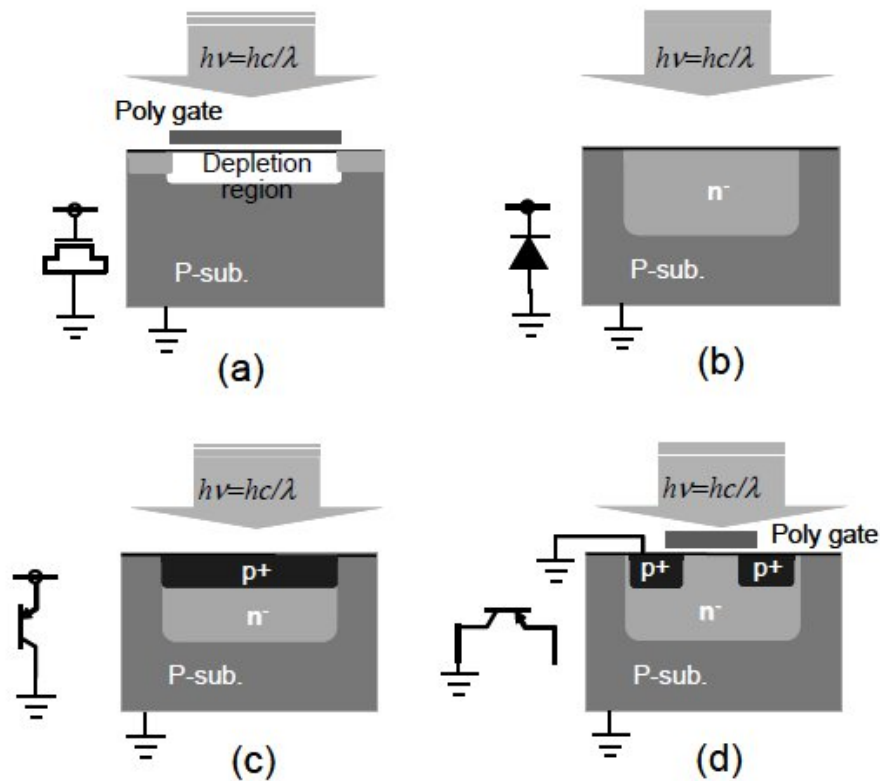
APS was first realized by using a photogate (PG) as a photodetector by E. Fossum et al. at JPL\* and then by using a photodiode (PD) [38, 39]. A PG was used mainly due to ease of signal charge handling. ***The sensitivity of a PG is not as good since polysilicon as a gate material is opaque at the visible wavelength region.*** APSs using a PD are called



3T-APSs (three transistor APSs) and are now widely used in CMOS image sensors. *In the first stage of 3T-APS development, the image quality could not compete with that of CCDs, both with respect to fixed pattern noise (FPN) and random noise.* Introducing noise canceling circuits reduces FPN but not random noise.

Ex. 2069 (Ohta) at p. 4 (emphasis added).

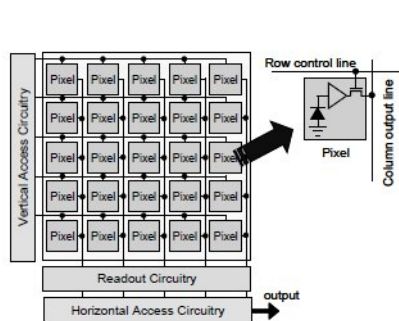
70. The differences between PD and PG CMOS image sensors (as well as phototransistors (PTs), and avalanche photodiodes (APDs)) are illustrated below:



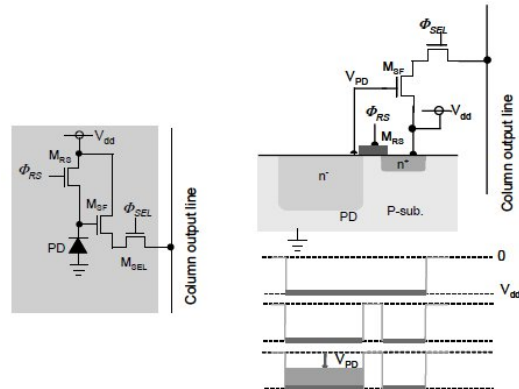
**FIGURE 2.7**  
Symbols and structures of (a) photodiode, (b) photogate, (c) vertical type phototransistor, and (d) lateral type phototransistor.

Ex. 2069 (Ohta) at 17.

71. CMOS image sensors also use a very different process to release and transfer the image (compared to CCD). Shown below on the left is a general diagram of a CMOS pixel array and shown below on the right is a basic pixel circuit for a 3T-APS image sensor:



**FIGURE 2.1**  
Architecture of a CMOS image sensor. A two-dimensional array of pixels, vertical and horizontal access circuitry, and readout circuitry are generally implemented. A pixel consists of a photodetector and transistors.



**FIGURE 2.22**  
Basic pixel circuits of a 3T-APS.

*Id.* at 11, 39.

72. The release of the image from the 3T-APS sensor involves several steps as described in *Smart CMOS Image Sensors and Applications* and operated very differently from CCD described above:

The operation of an APS is as follows. First, the reset transistor MRS is turned on. Then the PD is reset to the value  $V_{dd} - V_{th}$ , where  $V_{th}$  is the threshold voltage of transistor MRS (see Fig. 2.22(c)). Next, MRS is turned off and the PD is electrically floated (Fig. 2.22(d)). When light is incident, the photo-generated carriers accumulate in the PD junction capacitance  $CPD$  (Fig. 2.22). The accumulated charge changes the potential in the PD; the voltage of the PD  $V_{PD}$  decreases according to the input light intensity, as described in Sec. 2.4.1. After an

accumulation time, for example, 33 msec at video rate, the select transistor MSEL is turned on and the output signal in the pixel is read out in the vertical output line. When the read-out process is finished, MSEL is turned off and MRS is again turned on to repeat the above process.

It is noted that the accumulated signal charge is not destroyed, which make it possible to read the signal multiple times. This is a useful characteristic for smart CMOS image sensors.

*Id.* at 39.

73. Despite poorer image quality, CMOS image sensors had unique advantages over CCD, including (1) integration of CMOS pixels with circuitry on chip (*e.g.*, camera-on-a-chip) such as timing and control, A/D conversion, and signal processing, lowering total manufacturing costs; (2) lower power requirements; (3) increased resistance to radio frequency interference (RFI) and electromagnetic interference (EMI); and (4) flexible readout of the signal charge without destroying the accumulated charge providing key advantages for post-signal processing. *See* Ex. 2007 (Zarnowski) at 7 (“Although more radiation-tolerant than CCDs, CMOS imagers will never be as robust as the p-channel MOS CID, which will continue to control that market sector.”); Ex. 2065 (Nakamura) at 1 (“[CMOS] x-y addressing scheme provides flexible readout modes, including random access, windowing and electronic shuttering.”).

74. Notably, CMOS image sensor cameras could also be manufactured at higher volumes than CCD cameras because, unlike CCD's, MOS or CID technology, modern electronic circuitry could be integrated with the CMOS image sensor as a camera-on-a-chip, and CMOS fabrication techniques, and similar silicon semiconductor processes, were already mature by the mid-1990s. Ex. 2036 (OIDA) at 6 ("CMOS has evolved into the high volume imaging sensor solution, using common silicon manufacturing processes. **CMOS's integrated components**, including analog-to-digital (A/D) converter and clock, combined with a small footprint and low power consumption, **make CMOS the ideal solution for small handheld devices** (Figure 7.6). CMOS imaging is also capable of tracking, necessary for video images; for CCDs, this requires even more circuitry."), Fig. 7.6.

### C. Image Sensor Packaging history

75. The methods and techniques for packaging (*e.g.*, design and assembly) of image sensing technology evolved significantly since the successful commercialization of CCD image sensors into consumer products in the 1980s. A table for the packaging technologies in this time frame is shown below.<sup>3</sup> For example, Table 15-1 (at p. 1022) shows the packaging technologies used in various products, from consumer products to intermediate systems.

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<sup>3</sup> Ex. 2093.

**Table 15-1. Packaging Technologies in Consumer Products to Intermediate Systems.**

	<u>Chip Conn.</u>	<u>1st-Level Package</u>	<u>1st- to 2nd-Level Conn.</u>	<u>2nd Level Package</u>	<u>2nd- to 3rd-Level Conn.</u>	<u>3rd-Level Package</u>	<u>Chip Cooling</u>	<u>Maj. Chips/ System</u>
<b>Consumer Products</b>								
Sony CD	WB	PSCM	SMT/PTH	Card	—	—	—	4
TF-TV	WB/ TAB	PSCM	SMT/PTH	Card	—	—	—	4
Watch	WB	—	—	Card				4
<b>Low End Systems</b>								
Sharp	WB	PSCM	SMT/PTH	Card/Flex	—	—	—	8
IBM Printers	WB	PSCM	SMT/PTH	Card	Cable	—	—	
IBM PS2	WB	PSCM	SMT/PTH	Card	Conn.	Board	Air	≈10
Apple PC	WB	PSCM	SMT/PTH	Card	Conn.	Board	Air	
IBM Storage	WB	PSCM	SMT/PTH	Card/ Flex	—	—	—	
<b>Intermediate Systems</b>								
DEC 8600	WB	C-PGA	PTH	Card	Conn.	Board	Air	≈100
Fujitsu 730	WB	C-PGA	SMT	Card	Conn.	Board	Air (w/Fin)	
Hitachi 630	WB	C-PGA	PTH	Card	Conn.	Board	Air	
IBM 9370	C4	C-TCM	PTH	Board	Conn.	Cable	Air	
	WB	C-PGA	PTH	Card	Conn.	Board	Air	

Key:

C-4: Controlled Collapse Chip Connection  
CD: Compact Audio Disc  
C-PGA: Ceramic Pin-Grid Array  
C-TCM: Ceramic Thermal Conduction Module  
PSCM: Plastic Single Chip Module

PTH: Plated-Through-Hole  
SMT: Surface Mount Technology  
TAB: Tape Automated Bonding  
TF-TV: Thin Film TV  
WB: Wire Bond

Ex. 2093 at Table 15-1, p. 1022.

76. Table 15-1 above details that for consumer-based products in the 1980s, was generally wire-bonding (WB) of the chip, and surface mount (SMT) and/or plated through hole (PTH) of the package to a printed circuit board (“PCB”) or card. Tape automated bonding was not popular, and nor was C4 (which is an IBM abbreviation for controlled collapse chip connection, which in today’s environment is called flip-chip bump bonding). These choices of technology

packaging solutions matched the level of interconnects necessary for electrical connections between chip, chip and package, and package and printed circuit board.

77. By the end of the 1990s, these packaging technologies had evolved to deal with increased electrical interconnect connections, higher functionality chips such as CMOS image sensors that had become cameras-on-chip, higher pixel counts, and more system-on-chip solutions for miniaturization in consumer products. See Ex. 2093 at Chapter 15, p. 1029.

78. The packaging technologies for consumer products moved quickly to TAB (tape automated bonding) which as a flexible organic substrate, had found widespread use in camera technologies as can be seen from exploded camera parts on pages 1036-7. *Id.* at 1036-1037. This move to TAB packaging technologies was driven by the desire for packaging solutions with increased electrical interconnections that could fit in very small volumes. While initial TAB solutions utilized wire bonding, the technology quickly utilized the popularity of cost reduction, or otherwise known as flip-chip (FC) ball or bump packaging by the late 1990s.

79. One of the reasons why C4 or FC was only limited to intermediate systems (as reflected the Table 15-1 above) is that C4 or FC was expensive, and not fully qualified for high volume manufacturing in consumer products. Yield and

reliability was low, and the technology took the 1980s and the 1990s to fully become an accepted low cost high density, high interconnect packaging platform for consumer based technologies such as cameras, image sensors, televisions, compact disk players etc. *See id.* at p. 1032.

80. Today, flip-chip bumping is the package technology of choice of high-density image sensor technologies that are capable of CMOS image sensors that function as a system on a chip<sup>4</sup>. *Id.* at p. 2; pgs. 82-85 (showing the perspective for wafer-level chip scale packaging technology that is FC bumping for CMOS image sensors). For a POSITA in the late 1990s considering at packaging a CCD image sensor, the most optimal packaging technology at the time would have not been C4 or FC as it was very expensive to implement due to low yielding manufacturing processes. They would have chosen wire bonding to TAB or wire bonding to plated through hole or surface mount techniques, as the interconnect requirements would be significantly lower than those required by a fully functional and integrated CMOS system on chip camera.

#### **D. Image Sensor Market for CCD and CMOS in 1997**

81. In the mid-1990s, many engineers and their corporations working in both optoelectronic, photonic and electronic industries not only read technical

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<sup>4</sup> Text Book: 'Wafer-Level Chip-Scale Packaging: Analog and Power Semiconductor Applications' Authors Qu and Liu, Published by Springer, 2015

journals, but were members of industry trade associations, and especially those who produced technical and technology roadmaps. For example, the silicon industry prided itself on the classic ITRS semiconductor roadmap<sup>5</sup> that outlined, amongst other things, the decreasing linewidths of MOSFET transistors,<sup>6</sup> down towards ‘red brick walls,’<sup>7</sup> POSITAs working in the field of silicon semiconductors would calibrate their work using these technology roadmaps. This also was the case in the optoelectronics and photonics industry in the 1990s that leveraged electronic technology for optoelectronic and photonic functionality such as image sensors, photodetectors, LEDs, lasers, etc.

82. In the optoelectronics industry, engineers looked to the Optoelectronics Industry Development Association (OIDA) for the optoelectronic roadmaps. A POSA would have also considered more general publications reflecting technical developments and market trends. *See, e.g.*, Ex. 2036 (OIDA); Ex 2039 (Armstrong); Ex 2007 (Zarnowski); Ex. 2004 (Fossum LFW).

83. Any POSITA working in the field would be cognizant of these roadmaps showing both market and technology trends, challenges and

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<sup>5</sup> Ex. 2079 (<https://www.semiconductors.org/wp-content/uploads/2018/08/2001-Executive-Summary.pdf>).

<sup>6</sup> Ex. 2080

([https://en.wikipedia.org/wiki/International\\_Technology\\_Roadmap\\_for\\_Semiconductors](https://en.wikipedia.org/wiki/International_Technology_Roadmap_for_Semiconductors)).

<sup>7</sup> Ex. 2081 ([https://www.semiconductors.org/wp-content/uploads/2018/09/1\\_Executive-Summary.pdf](https://www.semiconductors.org/wp-content/uploads/2018/09/1_Executive-Summary.pdf)).



opportunities in the field. OIDA produced an annual market review of optoelectronic technologies that included image sensors, and in this review, technology trends were discussed.<sup>8</sup> Members of OIDA included both industrial as well as governmental entities, and their technology roadmap workshops (which led to subsequent OIDA technology roadmap reports) in the 1990s (as well as the 2000s) were heavily sponsored by governmental agencies such as ARPA (DARPA), NSF, DOE, NIST. *See* Ex. 2050 (Ackland IEEE); Ex. 2036 (OIDA); Ex 2039 (Armstrong); Ex 2007 (Zarnowski); Ex. 2004 (Fossum LFW).

84. In the 1990s, OIDA serviced the image sensing community with technology roadmaps, workshops, conferences, as well as market reports with trends. One of the findings that was generally understood by both the industry-at-large, as well as myself, during the mid-1990s was that the image quality of CMOS image sensors was not comparable to CCDs. At the time (and throughout the early 2000s) CCDs dominated the market for industrial image sensor applications where high resolutions, that commanded high ASP (Average Selling Prices), were commonplace.

85. During the mid-1990s, wireless, mobile consumers drove the need for a low resolution, increased functionality of a camera on a chip for wireless mobile applications. Despite poorer image quality, CMOS image sensors had certain

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<sup>8</sup> Ex. 11 (2007 OIDA Market Report and Forecast).

advantages over CCD, primarily in lower power consumption, more flexible readout circuitry, and increased resistance to electromagnetic interference (EMI) and radio frequency interference (RFI). For these reasons, NASA sought to develop CMOS image sensors for use in satellite and mobile/wireless applications. Led by Dr. Fossum, NASA's JPL pushed the development of CMOS to increase image quality and further reduce signal noise for use in wireless industrial applications, primarily satellite systems and the Mars Rover in early development. Ex. 2086 ([https://spinoff.nasa.gov/Spinoff2010/cg\\_3.html](https://spinoff.nasa.gov/Spinoff2010/cg_3.html)); Ex. 2087 (<https://www.nasa.gov/feature/jpl/nasa-technology-is-all-around-you>). As such, it was well understood by those skilled in the art in 1997 that development and use of CMOS sensors was associated wireless/mobile applications since NASA systems were intended for deployment in space and for wireless communications.

86. Further, in 1997 a person skilled in the art would have known that CCD image sensors were a mature technology that was (at the time) superior in performance to CMOS image sensors. Any suggestion regarding the use of CMOS image sensors in the design for industrial applications would have been driven by the unique advantages of CMOS, namely lower power (for battery operated device) and use in wireless environments (where EMI and RFI were present). Otherwise, a CCD image sensor would have been the more logical choice for industrial applications where image quality was important and less sensitive to the

higher costs associated with CCD image sensors and space was not an issue and miniaturization was less important (compared to less expensive CMOS image sensors using the camera-on-a-chip design).

87. The use of higher quality CCD image sensors in industrial fields in the 1997 time frame was well recognized and continued to dominate the industrial fields for many years, as reflected below:

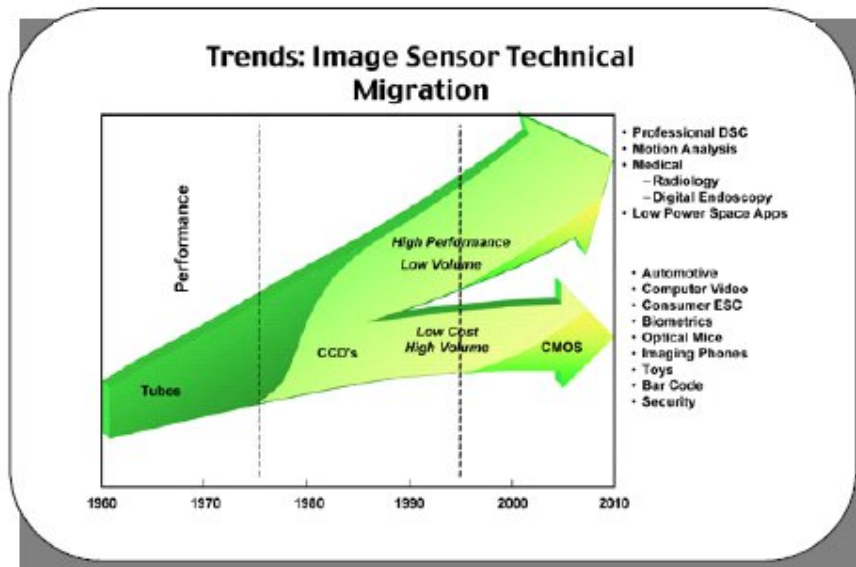


Figure 7.5: Image Sensor Migration and Materials

Source: Kodak

Image sensor products are differentiated not just by technology (CMOS vs. CCD) or pixel count, but by a variety of metrics and features. These include uniformity reduction, noise reduction, dark current, dynamic range, resistance to blooming, spectral range, ability to stitch lithographic fields into large arrays, and quality of associated integrated circuits (IC) including analog-digital conversion, color processing, and image processing.

CCDs will continue to be used for applications requiring very high quality imaging, such as medical imaging and professional cameras (Figure 7.5). CMOS has evolved into the high volume imaging sensor solution, using common silicon manufacturing processes. CMOS's integrated components, including analog-to-digital (A/D) converter and clock, combined with a small footprint and low power consumption, make CMOS the ideal solution for small handheld devices (Figure 7.6). CMOS imaging is also capable of tracking, necessary for video images; for CCDs, this requires even more circuitry.

Ex. 2036 (2007 OIDA Market Report and Forecast) at 222.

88. Further support for the dominance of CCD pixel arrays over CMOS pixel arrays for industrial applications in 1997 is evidenced by the fact that the market for CMOS image sensors was driven by mobile wireless applications, as reflected in significant growth of CMOS sensors in camera phones from 1997 to 2006. In fact, the old adage (circa 2009) by professional photographers that the best photograph is the one when the camera is with you – is something that helped the mobile wireless camera market accelerate in popularity.<sup>9, 10</sup>

89. A camera on your wireless phone, even with low pixel resolution, caught the imagination of not only engineers and POSITAs in the field, but with consumers in general. Low resolution cameras on mobile cell phones, as an ancillary add-on feature, began to take off in the late 1990s and early 2000s, and everyone who wanted the functionality of taking photographs quickly and efficiently without carrying an individual camera saw the benefits of a multi-functional wireless CMOS imager system that was enabled by a miniature form-factor, CMOS technology for low power battery operation, and on a single chip as a complete system.

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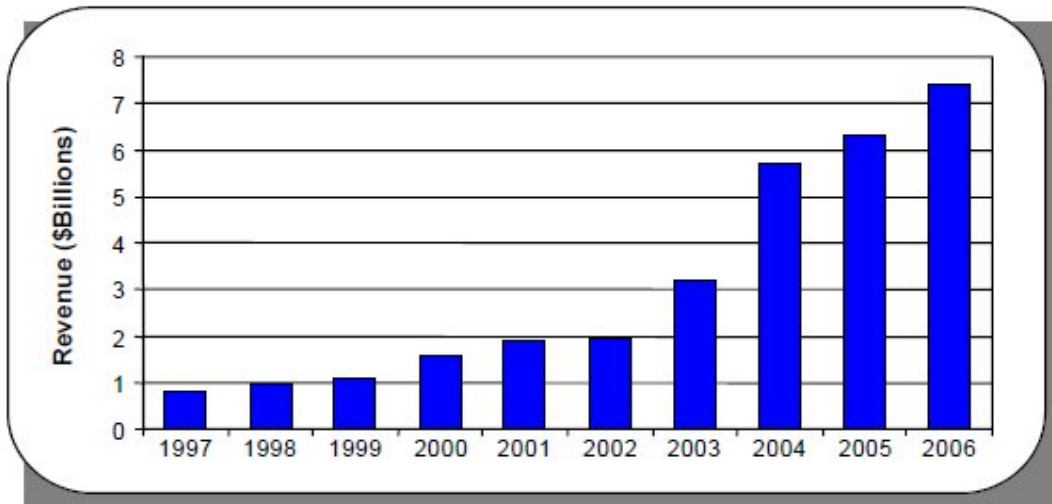
<sup>9</sup> Ex. 12 ([https://www.azquotes.com/author/31449-Chase\\_Jarvis](https://www.azquotes.com/author/31449-Chase_Jarvis))

<sup>10</sup> Ex. 13 (<https://www.amazon.com/Best-Camera-One-Thats-You/dp/0321684788>)

90. As can be seen from OIDA's market overview of worldwide image sensors from 1997 to 2006, the growth of CMOS image sensors was driven by its use as an add-on feature to wireless camera phones, despite its poor image quality (S/N):

### 7.1 Market Overview

Worldwide image sensor sales continued to grow rapidly in 2006, reaching \$7.4 billion in revenue (Figure 7.1), due primarily to the continued growth of camera phones. Complementary metal-oxide semiconductor (CMOS) image sensors led revenue with small, low cost sensors ideal for the mobile phone market. Although CMOS imagers have in previous years been less expensive and consumed less power than charge-coupled devices (CCD), they were plagued by high signal-to-noise ratios. In 2005, CMOS imagers achieved an improved signal-to-noise ratio (SNR) as a result of research investment to address the emerging high-volume integrated mobile phone/camera market.



**Figure 7.1: Worldwide Image Sensor Revenue, 1997-2006**

Sources: Strategies Unlimited, Micron, IC Insights, NE Asia, OIDA

Ex. 2036 (2007 OIDA Market Report and Forecast) at 219.

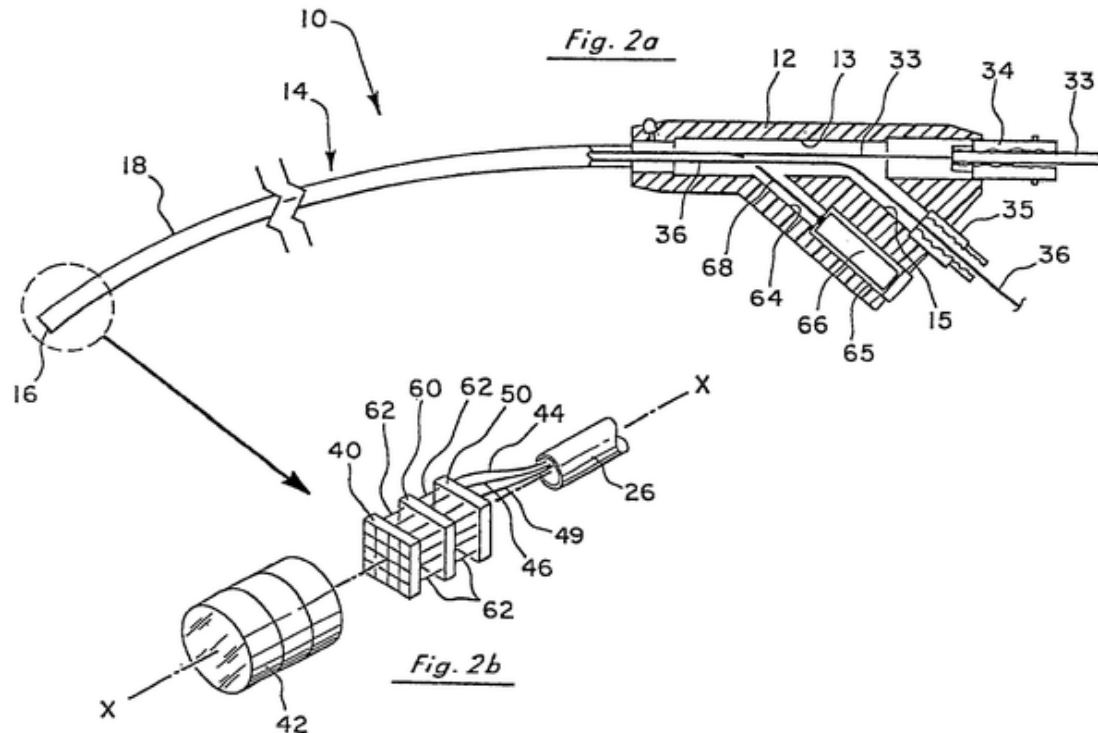
91. A POSITA would consider reference available at the time (1997) to understand the image device market. For example, a 1997 Photobit article titled

CMOS Active Pixel Sensor (APS) Technology for Multimedia Image Capture, 1997 Multimedia Technology & Applications Conference MTAC97 March 23-25, 1997 Univ. of Cal., Irvine. Ex. 2082. This is an article by Dr. Fossum regarding the history and development of CMOS image sensors at NASA's JPL. *Id.* Dr. Fossum discusses how CMOS imager technology was developed at JPL and transferred from JPL to U.S. Industry (*e.g.*, AT&T). *Id.* Further, Dr. Fossum's own company, Photobit, was developing CMOS for portable applications such as laptops and personal digital assistants (PDAs). *See, e.g.*, Ex. 2082.

## **V. The '052 Patent**

### **A. Overview**

92. The '052 Patent generally discloses a reduced area imaging device in various configurations, and connections (either wired or wireless) between the imaging device elements and a video display. *Id.*, Abstract. The '052 Patent discloses and specifically claims inventive concepts that represent significant improvements over conventional single-chip imaging devices with the image sensor and image processing on the same plane. An example of the reduced area imaging device is seen in Figure 2b which is reproduced below:



The exemplary embodiment illustrated in Figure 2b reflects one aspect of Patent Owner's inventive improvement for reduced area imaging devices that focused on minimum profile area designs by locating various aspects of the imaging device in different locations, while taking advantage of improved technology available for image sensors. For example, while CCD image devices dominated the market for many applications in the mid-90s, as well as at the time of the priority date of the '052 Patent (October 6, 1997), CMOS imagers were being developed with certain advantages over CCD technology, particularly on-chip integration of circuitry and lower power requirements and consumption. Patent Owner leveraged these developments in imager technology to develop the claimed reduced area imaging device by retaining the benefits of CMOS imagers while also separating out some

functionality from the standard on-chip integration design, thereby resulting in a reduced area imaging device that had a minimum profile. Additionally, Patent Owner described in the '052 Patent specification how the Patent Owner improved on Fossum's Camera-on-a-Chip technology to further achieve a minimum profile device.

## **B. Challenged Claim**

93. Petitioner challenges claim 2 of the '052 Patent. The Petition's grounds and asserted references are summarized below.

### **References**

<b>Asserted Reference</b>	<b>Exhibit</b>	<b>Patent/Printed Publication</b>
<i>Swift</i>	1005	U.S. Patent No. 5,835,141 to Ackland <i>et al.</i>
<i>Ricquier</i>	1033, 1038	<i>Ricquier, N., et al.</i> "CIVIS sensor: a flexible smart imager with programmable resolution," Charge-Coupled Devices and Solid State Optical Sensors IV. Vol. 2172. International Society for Optics and Photonics, 1994. (" <i>Ricquier</i> ")
<i>Suzuki</i>	1015	U.S. Patent No. 5,233,426 to <i>Suzuki et al.</i>
<i>Larson</i>	1029	U.S. Patent No. 5,541,640 to <i>Larson</i>

### **Grounds**

<b>Ground</b>	<b>Challenged Claim</b>	<b>Basis</b>
1	2	<b>35 U.S.C. § 103</b> over <i>Swift</i> in view of <i>Ricquier</i> and <i>Suzuki</i>
2	2	<b>35 U.S.C. § 103</b> over <i>Larson</i> in view of <i>Swift</i> , <i>Ricquier</i> and <i>Suzuki</i>



94. The Challenged Claim is copied below:

**Claim 2.** An imaging device comprising:

a housing;

an image sensor mounted in said housing, said image sensor including a first circuit board having a length and a width thereto, wherein said length and width of said first circuit board define a first plane, said first circuit board including an array of CMOS pixels thereon, wherein a plurality of CMOS pixels within said array of CMOS pixels each include an amplifier, said first circuit board further including timing and control circuitry thereon, said timing and control circuitry being coupled to said array of CMOS pixels, said image sensor producing a pre-video signal;

a second circuit board mounted in said housing, said second circuit board being electrically coupled to said first circuit board, said second circuit board having a length and a width thereto, wherein said length and width of said second circuit board define a second plane, said second circuit board including circuitry thereon to convert said pre-video signal to a post-video signal, said second circuit board being positioned in a stacked arrangement with respect to said first circuit board, said second plane of said second circuit board being substantially parallel to said first plane of said first circuit board;

a lens mounted in said housing, said lens being integral with said imaging device, said lens focusing images on said array of CMOS pixels of said image sensor;

a video screen, said video screen being electrically coupled to said second circuit board, said video screen receiving said post-video signal and displaying images from said post-video signal; and

a power supply mounted in said housing, said power supply being electrically coupled to said first circuit board to provide power to said array of CMOS pixels and said timing and control circuitry, said power supply also being electrically coupled to said second circuit board to provide power thereto;

wherein a largest dimension of said image sensor along said first plane is between 2 and 12 millimeters.

## VI. Claim Construction

95. Because the Petition was filed after November 13, 2018, for this *inter partes* review proceeding, the Board applies the same claim construction standard as that applied in federal courts. *See Changes to the Claim Construction Standard for Interpreting Claims in Trial Proceedings Before the Patent Trial and Appeal Board*, 83 Fed. Reg. 51340, 51343 (Oct. 11, 2018). That is, claim terms “are generally given their ordinary and customary meaning” as understood by a person of ordinary skill in the art in question at the time of the invention.

96. I understand Petitioner and Patent Owner have proposed constructions in District Court litigation. In its Institution Decision, the Board stated that the plain and ordinary meaning would be applied. For purposes of my analysis, I have applied the plain and ordinary meaning.

## VII. Alleged Prior Art

### A. Swift

97. The *Swift* reference describes a security camera intended for use inside a door. A POSITA would have known that at the relevant time, a CCD image sensor was the dominant technology for security and surveillance camera systems, and through the early 2000s. *See, e.g.*, Ex. 1005 at 12, Figure 2, Figure 4; Ex. 2036 at 226 (CCD was dominant technology for security and surveillance camera systems in 2007); Ex. 2036 (OIDA) at 8 (“**CCDs have historically been the dominant image sensors** and have been very successful in high speed

**applications such as digital cameras, digital copiers, and flat bed scanners.**

CCDs are also appropriate for surveillance and manufacturing applications where high performance is a requirement. **CCDs have traditionally had better light sensitivity** as a result of their pixel architecture, where all of the light hitting the array can potentially be converted to signal.”) (emphasis added).

98. *Swift* describes alternate embodiments: (1) with CCD image sensor and off-chip architecture, and (2) an APS CMOS image sensor described by Dr. Eric Fossum with a camera-on-a-chip architecture (citing a June 1993 *Laser Focus World* article by Dr. Eric Fossum). For example, *Swift* expressly states that the example show in in Figure 7 is an APS CMOS image sensor. *Id.* at 18:13. Further, a POSITA would have understood that other embodiment such as the one shown in Figure 6, using 12 volt power supply (typical of CCD rather than 5 volt for CMOS) and off-chip circuitry, describe a camera that uses a CCD sensor. *Id.* at 15:4-31.

#### **B. Ricquier**

99. *Ricquier* describes a bench-test setup that is being used to develop a passive CMOS pixel array intended to be used in machine vision application – not a consumer camera where the image quality is very important. The end goal of *Ricquier* is a CMOS-camera-on-a-chip that “offers the selective addressability together with the possibility of further *cointegration of processing electronics on the same chip.*” Ex. 1033 (*Ricquier*) at 8 (emphasis added). *Ricquier*’s work is

closely related to this research of “processing circuitry [being] integrated at the edges of the photodiode array exploiting the possibility to access a whole row of data at once”—*i.e.*, “the development of a multi-purpose flexible sensor architecture that can be used as a module in further *sensor systems on a single chip.*” *Id.* at 9 (emphasis added).

100. Additionally, *Ricquier* describes a pixel array with portions of the timing and control circuitry on the same plane as the pixel array (shown in Figure 1).

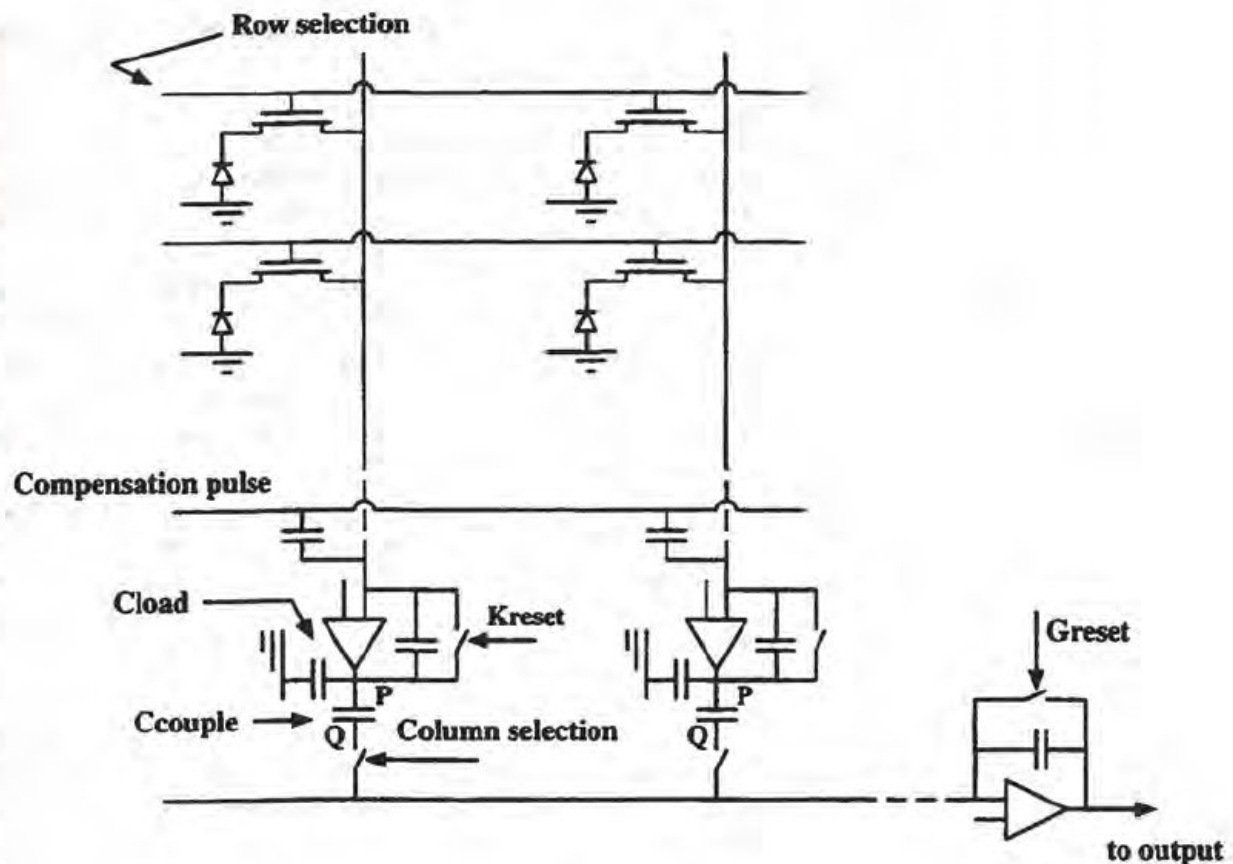


Figure 1: Schematic representation of the sensor architecture

Ex. 1033 at 11.

101. Further, *Ricquier* describes control pulses generated by an external driving unit and states the “signals” can be seen in Figure 1 above. Ex. 1033 at 11. *Ricquier* explains that the “off-chip driving unit” is the timing controller for generating the pulse signals trigger the  $K_{\text{reset}}$  switch and  $G_{\text{rest}}$  switch which control the release charge and image signal. *Id.* at 12. *Ricquier* explains that important components of the pixel array include couple capacitors  $C_{\text{couple}}$  and  $C_{\text{load}}$  also shown in Figure 1, confirming that the  $K_{\text{reset}}$  switch and  $G_{\text{rest}}$  switch are included in the pixel array:

***The pixel array consists of 256 by 256 square pixels arranged on a pixel pitch of 19  $\mu\text{m}$  and realised in a 1.5  $\mu\text{m}$  n-well CMOS technology.... The technology used offers two metal layers and two poly layers. The second poly layer was exclusively used for the realisation of compact, linear capacitors (0.5 fF /  $\mu\text{m}^2$ ) : the integration capacitors at the output amplifier, the couple capacitors  $C_{\text{couple}}$  and the load capacitors  $C_{\text{load}}$  (see figure 1). .***

Ex. 1033 at 13.

102. *Ricquier* states that the driving unit and clock signals used for timing and control are placed off chip. *Id.* at 11. Such off-chip timing control causes well-known problems that limit the “read-out frame rate.” See Ex. 1033 at 10 (disclosing a single output amplifier); Ex. 2034 at 1:44–62 (discussing the negative impact of using a single output amplifier on an imager’s frame rate). The latches,

decoders and switches, however, are shown in the same plane as the pixel array and are critical for releasing the image signal. *Id.* at 13, Figure 1.

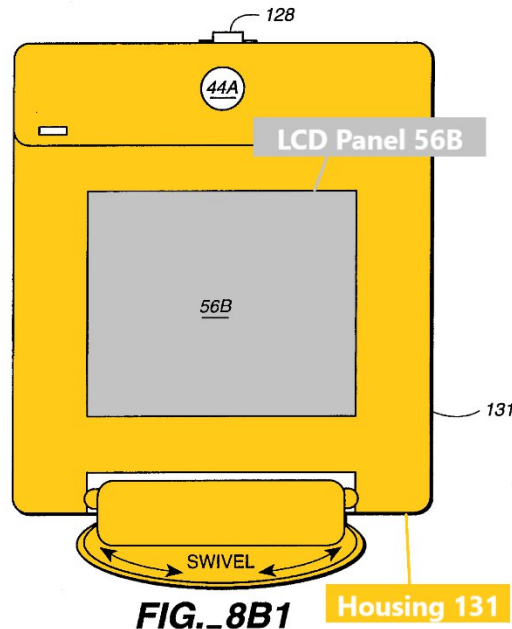
103. *Ricquier* states that the driving unit and clock signals are placed off-chip to limit the complexity of the timing controller and only some very common patterns are provided for development purposes. *Id.*

### C. Suzuki

104. *Suzuki* is an issued U.S. patent for a “reduced diameter camera head for solid-state image pickup device and method of producing same.” Ex. 1015 at Title. *Suzuki* describes a camera head for a solid-state image pickup device in housing “formed by sealing a solid-state image pickup chip (solid-state image pickup semiconductor device) between an optical glass plate and a ceramics package.” Ex. 1015 at 19-21. Based on the structure described in *Suzuki*, a POSITA would understand that a conventional CCD image sensor is described, using various off-chip circuitry, especially in the 1991 time-frame when *Suzuki* was filed. *See* Ex. 1015 at 2:38-63, Figs. 1, 2. For example, *Suzuki*’s description of “a circuit for **driving** the solid-state image pickup chip 221 and a circuit for **amplifying** the video signal from the solid-state image pickup chip 221” would have been understood by a POSITA to refer to language used to describe a CCD image sensor.

**D. Larson**

105. *Larson* teaches CCD camera in a “**housing 131** for the CCD camera lens 44A and the **LCD panel 56B**,” including an integrated display and capable of swiveling, as shown in Figure 8B1 (copied below) Ex. 1029 at 26:43-54.

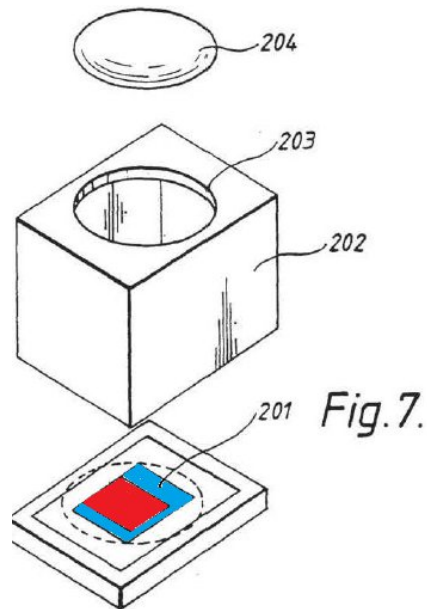


Ex. 1029 at Fig. 8B1.

**VIII. *Swift* in View of *Ricquier* and *Suzuki* Does Not Render the Challenged Claims Obvious Under 35 U.S.C. § 103(a)**

106. The *Swift* reference describes a security camera (for use inside a door) with two possible configurations, (i) an APS CMOS image sensor or (ii) CCD image sensor. While *Swift* provide few implementation details, POSITA would understand that a CCD image sensor would be used in configurations using off-chip circuitry, including off-chip signal processing and higher operating voltages (e.g., 12 V for CCD rather than 5 V for CMOS). Ex. 1005 at 15:25-31 (using 12

volt power supply for embodiment shown in Figs. 1 and 2). Further, a POSITA would have understood that the camera-on-a-chip APS CMOS image sensor described in the 1993 Laser Focus World (and cited in *Swift*) for the alternate embodiment. For example, *Swift* states that “Figure 7 shows an image sensor 201 (e.g. of APS type).” *Id.* at 18:13. As shown in Figure 7 the CMOS image sensor includes a section for the CMOS pixels (red) and a portion for other circuitry, including timing and control and signal processing circuitry (blue):



Ex. 1005 at Fig. 7 (highlighting added).

107. Consistent with packaging technology in the relevant time, a POSITA would not have separated the timing and control from the pixel array because the it would have required significant numbers of connection using C4, FC or bump packaging, and would have resulted in a significantly more complex design with



increased costs and lower yields, rather than a lower-cost option proposed by *Swift*.

Because *Swift* provides no suggestion or motivation to use such packaging technology, in 1997 a POSITA would have used a CMOS image sensor with on-chip circuitry for timing and control and signal processing (as also described Laser Focus World cited in *Swift*).

108. A POSITA would not have redesigned Dr. Fossum's APS CMOS camera-on-a-chip image sensor as proposed by Petitioner by separating processing from the pixel array because such an approach would not have had any technical benefits for security cameras, resulting in a significant loss in image quality, and little to no cost savings. Petition at 15-20. In effect, the proposed re-design of Dr. Fossum's camera-on-a-chip would negate many of the benefits of CMOS (*e.g.*, multiple off-chip circuitry with higher costs, larger footprint, increased signal noise and poorer performance). *See* Ex. 2004 (Fossum LFW) at 4 ("Although some integrated CMOS/CCD processes have been demonstrated, undesirable compromises in the performance of CMOS or CCD technology must be made."); Ex. 2054 (Fossum IEEE 1995) at 2 ("CMOS-based image sensors offer the potential opportunity to integrate a significant amount of VLSI electronics and reduce component and packaging costs. CCD technology, on the other hand, has become quite specialized and, in general, is not well-suited to CMOS integration due to voltage, capacitance and process constraints.").

109. The main advantage of Dr. Fossum's CMOS image sensor is achieved when chips are fully integrated, and the camera-on-a-chip approach not only improves the CMOS image sensor performance, it also permits significantly lower power consumption than CCDs, and can be operated in a small volume or space. Separating the on-chip functionality in Dr. Fossum's CMOS image sensor would diminish the benefits, increasing the overall size, reducing performance (more power and slower speeds), and reduce cost-savings achieved from on-chip integration. Ex. 2004 (Fossum LFW) at 4 ("To get high transfer efficiency, CCDs are often driven with relatively large voltages (by microelectronics standards), and also represent high enough capacitance loads to driving electronics to make on-chip integration of clocks and drivers nearly impractical. Yet, on-chip integration is the key to achieving future camera miniaturization."); Ex. 2039 (Armstrong) at 2 ("One chip can incorporate all manner of electronic controls that are usually on multiple chips, from timing circuits to zoom and anti-jitter controls. By consolidating many functions and reading images in a more efficient way, it requires one-hundredth the power of a CCD-based system. And the chip does its own conversion from analog to digital for output on computer monitors or disk storage."); Ex. 2054 (Fossum IEEE 1995) at 1 ("On-chip analog to digital converters and on-chip timing and control circuits permit realization of an electronic camera-on-a-chip."); Ex. 2007 (Zarnowski) at 7 ("The piece-cost-

versus-performance winner will in every instance be the CMOS imager. The combination of standard CMOS fabrication and on-chip electronics to lower external system costs yields the most economical solution.”); Ex. 2060 (Nixon) at 1, 2, Fig. 2; Ex. 2050 (Ackland IEEE) at 1; Ex. 2058 (Holst) at 117.

110. As such, absent the disclosure in the '052 Patent, a POSITA in 1997 would not deconstruct and separate the on-chip circuitry specially adapted for Dr. Fossum's CMOS image sensor. Following the path of the '052 Patent yielded smaller cameras than a POSITA would have expected given the accepted wisdom that “on-chip integration is key to achieving future camera miniaturization.” Ex. 1048 at 8. I also note that the system design claimed in the '052 Patent yielded unexpected benefits, including “that remoting processing circuitry from the CMOS imager and timing and control circuits eliminated the need for shielding.” Ex. 1003 at 85–86; *see also id.* at 94-95.

111. Additionally, there would be little to no cost savings from redesigning Dr. Fossum's CMOS image sensor by removing the pre-video to post-video signal processing because the most significant costs saving from APS CMOS pixels is derived from full on-chip integration. Ex. 2060 (Johannes) at 3 (“CMOS sensors cost an average of less than \$14, about 15% to 20% cheaper than CCDs. . . . If additional image-processing functions are crammed onto the chip, the savings can reach 50%. The chip Nintendo used, Mitsubishi Electric Corp.'s new ‘artificial

retina,' incorporates both light-sensing and image-processing functions. It costs only \$10, or half what traditional CCD technology would have cost.”). For example, a 1995 Business Week article citing Dr. Fossum, also quotes Dr. Ackland (relied upon by Petitioner on related IPRs) as saying that the true cost-saving benefits of using APS CMOS pixels is achieved with full integration.

cost much less than CCDs. One chip can incorporate all manner of electronic controls that are usually on multiple chips, from timing circuits to zoom and anti-jitter controls. By consolidating many functions and reading images in a more efficient way, it requires one-hundredth the power of a CCD-based system. And the chip does its own conversion from analog to digital for output on computer monitors or disk storage. About all it needs is a power source and a lens to focus light on it.

Fossum says several U.S. companies are negotiating with JPL on licensing the technology, but he isn't naming names. The chip offers fresh opportunities in imaging to companies that have been stymied by the high barriers to entering CCD production. "American industry is definitely interested," says Carl A. Kukkonen, director of the Cen-

ter for Space Microelectronics Technology at JPL. "For them, it's a chance to leapfrog the Japanese."

AT&T, for one, would like to take the first jump. Long interested in low-cost cameras for video telephones, it has already collaborated with JPL to build two prototype arrays. A CCD costs a modest \$20, but other components bring the system cost to \$140, says Bryan D. Ackland, head of the VLSI Systems Research Dept. at AT&T Bell Laboratories in Holmdel, N.J. By putting everything on one chip, says Ackland, "what we're trying to do is build the entire camera subsystem for \$20." At that price, every personal computer could come with a built-in videoconference feature, just as many multimedia PCs come outfitted with speakerphones today.

Bell Labs' interest in active pixel sensors is especially impressive because

Ex. 2039 at 2 (highlighting added); *see also*, Ex. 2060 (Johannes) at 3.

112. The highlighted excerpts above quote Dr. Ackland as stating that a CCD image sensor "costs a modest \$20" but the "other components" (*i.e.*, the off-chip circuitry) brings the system cost to \$140. In other words, the bulk of the costs are for the off-chip components and are not eliminated if Dr. Fossum's camera-on-

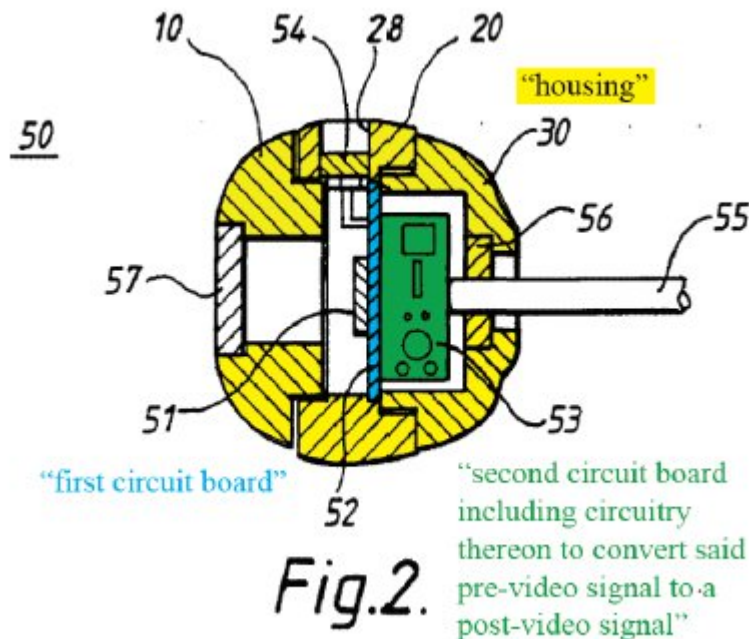
a-chip design, including timing and control and processing, is deconstructed into separate components. *Id.*

**A. *Swift* in View of *Ricquier* and *Suzuki* Fails to Disclose an Imaging Device With the Requisite Dimensions**

113. Claim 2 of the '052 Patent requires that the “largest dimension of said image sensor along said first plane is between 2 and 12 millimeters.” *Id.* Although Suzuki discloses an imaging device having a diameter within that range, its imager is not arranged in the claimed manner. In particular, Suzuki does not disclose a first circuit board that includes a CMOS pixel array and timing and control circuitry, so Petitioner’s reference to the size of Suzuki’s imager to the claimed imaging device is an apples and oranges comparison. *See Suzuki* at 2:51–54 (disclosing different circuit boards for the solid-state pickup chip and the circuit that drives it).

114. *Swift* discloses a camera having far larger dimensions than either the imaging device recited in the '052 Patent or *Suzuki*. Ex. 1005 at 5 (contemplating a maximum dimension of 100, 80, or 50 mm); *id.* 9 (contemplating a 38x38 mm housing); Ex. 1001 at 6:58–61 (“Image sensor 40 can be as small as 1 mm in its largest dimension. However, a more preferable size for most endoscopic procedures would dictate that the image sensor 40 be between 4 mm to 8 mm in its largest dimension.”).

115. Further, I note that if even if Swift was modified such that “circuit board 53 is oriented parallel to circuit board 52,” that modification would not result in an imaging device with the requisite dimensions because the dimensions of *Swift*’s camera along the plane of the image sensor **would not change** regardless of how circuit board 53 was oriented in relation to circuit board 52:



Petition at 4.

116. I also disagree that it would have been obvious to modify *Swift* and *Ricquier* with *Suzuki*. *Suzuki* claims priority to an application filed in 1990, prior to the introduction of CMOS imagers:



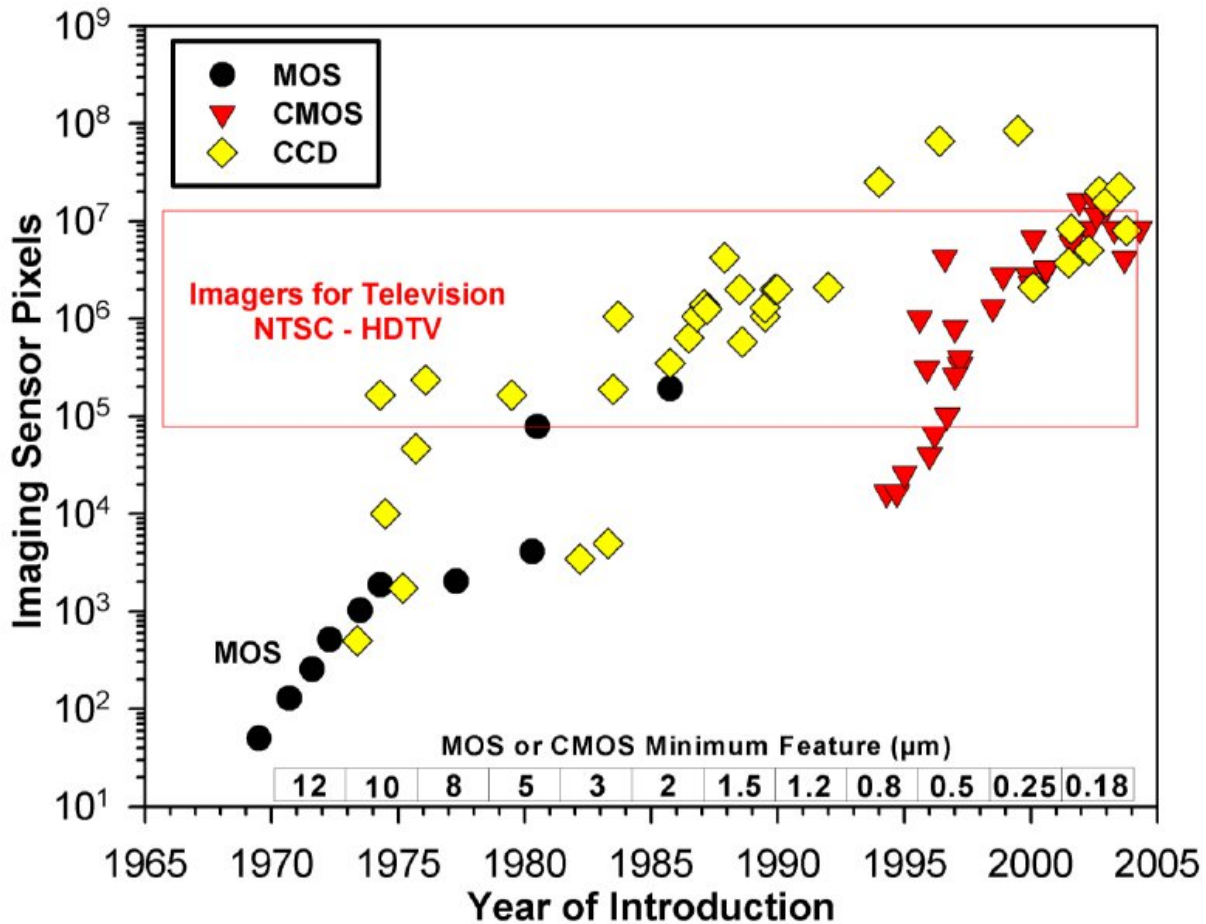


Figure 1. Chronology of visible imager development for CCD, MOS, and CMOS.

Ex. 2092 at 8. This is further evidence that a POSITA would recognize that *Suzuki's* “solid-state image pickup device” uses CCD technology, not CMOS. At the time of the invention the industry was committed to the fully integrated CMOS “camera on a chip,” so a POSITA would not have consulted a CCD reference to determine an appropriate system architecture for a CMOS imager. *See, e.g.*, Ex. 2007 (Zarnowski) at 7 (“The combination of standard CMOS fabrication and on-chip electronics to lower external system costs yields the most economical solution.”); Ex. 2039 (Armstrong) at 2 (“One chip can incorporate all manner of

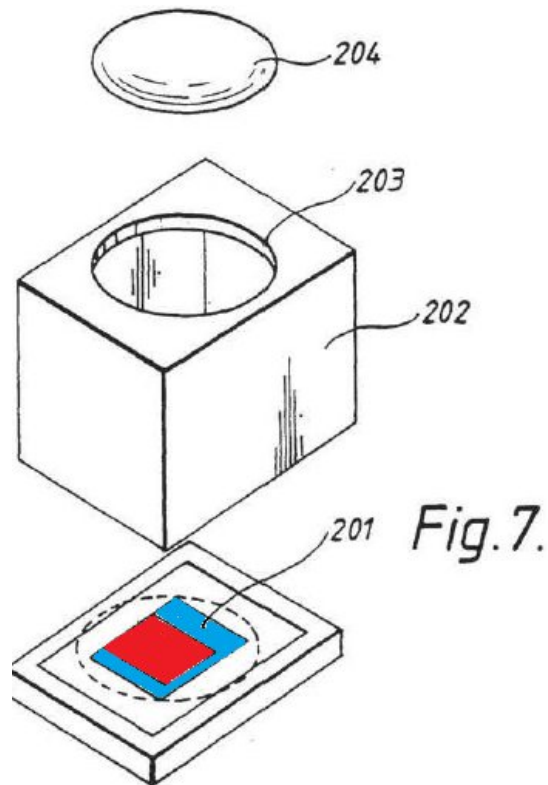
electronic controls that are usually on multiple chips, from timing circuits to zoom and anti-jitter controls. By consolidating many functions and reading images in a more efficient way, it requires one-hundredth the power of a CCD-based system. And the chip does its own conversion from analog to digital for output on computer monitors or disk storage.”). Additionally, a POSITA would not have modified *Swift* in view of *Suzuki*, which uses an 8.5 mm CCD image sensor. In particular, a POSITA would not have unnecessarily reduced the size of the sensor in *Swift* to the size of the sensor used in *Suzuki* because such a modification would have reduced image resolution and imposed unnecessary performance constraints.

Ex. 1015 at 1:28-43

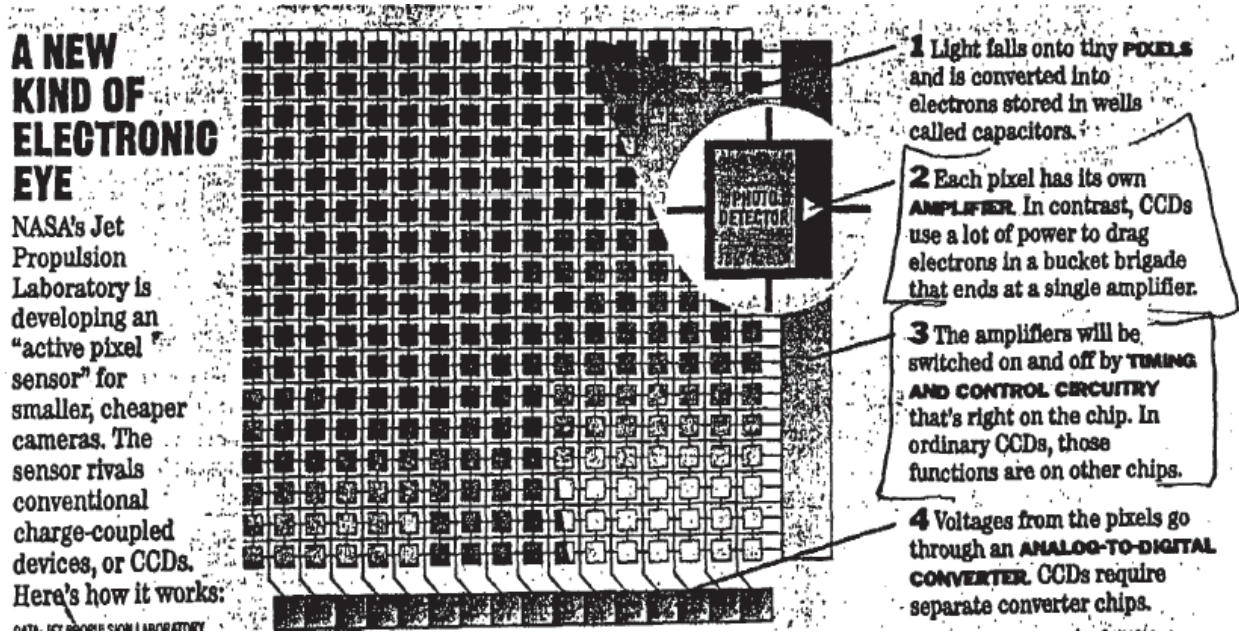
**B. A POSITA Would Not Have Combined Swift, Ricquier, and Suzuki to Arrive at the Claimed Invention**

117. One of the “electronic controls” found on Dr. Fossum’s APS-type sensor, used in *Swift*, is the claimed “timing and control circuitry.” *See* Ex. 1048 at 8 (comparing a CMOS sensor with “on-chip integration of clocks and drivers” with CCD imagers); Ex. 1060 at 2 (“The amplifiers will be switched on and off by TIMING AND CONTROL CIRCUITRY that’s right on the chip. In ordinary CCDs, those functions are on other chips.”)). Figure 7 of *Swift* shows a schematic view of *Swift*’s CMOS image sensor, which includes a section for the CMOS pixels (red) and a portion for other circuit components, including timing and control and signal processing circuitry (blue):





Ex. 1005 at Fig. 7 (highlighting added)). This CMOS imager, with an asymmetrically positioned “light-sensitive area,” is directly analogous to Dr. Fossum’s CMOS camera on a chip, which has integrated timing and control circuitry and an analog-to-digital converter and an asymmetrically located pixel array:



Ex. 1060 at 2. I address Petitioner's arguments below.

118. Petitioner argues that "**Ricquier** is also reasonably pertinent to the alleged problem(s) identified in the '052 of arranging the circuitry of a CMOS image sensor, including to minimize the device's size or profile area." Petition at 22. However, my review of *Ricquier* did not uncover any discussion of camera size or any techniques for reducing the camera's size, including moving timing and control circuitry off-chip. Indeed, the separation of the clock drivers in *Ricquier*, was incidental (and detrimental), to the development of the pixel array, and a POSITA would not have relied on this as a design feature. To the contrary, a POSITA at the time would have believed that the best way to reduce the size of a CMOS imager would have been to move toward a "camera-on-a-chip." Ex. 1048 at 8 ("Yet, on-chip integration is the key to achieving future camera

miniaturization.”); Ex. 1060 at 1 (describing the switch from “bulky” CCD imagers to “tiny” CMOS imagers “[w]ith all the smarts on one chip instead of several”). In fact, far from identifying any advantages of moving the driving unit off-chip, *Ricquier* states that the authors chose CMOS technology precisely because circuitry such as its driving unit could be realized on-chip. *Ricquier* at 1 (“A CMOS technology was chosen because it offers the selective addressability ***together with the possibility of further cointegration of processing electronics on the same chip.***”).

119. Petitioner also that *Ricquier* is also relevant to the problem of “reduc[ing] image noise in a CMOS sensor.” Petition at 22. This is not true. My review of *Ricquier* did not uncover any discussion of noise reduction or techniques for achieving a reduction in image noise. And contrary to Petitioner’s argument, a POSITA seeking low image noise would have “placed the timing and control circuits on the same planar structure with the pixel array.” ’052 Patent at 9:45–47 (emphasis added). Petitioner’s proposed combination of *Swift* and *Ricquier*, which involves placing *Ricquier*’s off-chip timing unit on the opposite side of the circuit board supporting the pixel array, would therefore be ***counterproductive*** to the goal of noise reduction. Petition at 23. Accordingly, in order to reduce noise a POSITA would maintain *Swift*’s timing and control circuitry on-chip rather than placing it on the opposite side of the circuit board, as asserted in the Petition.

120. Third, Petitioner’s argument that *Ricquier* teaches “express advantages” in the form of “‘selective addressability’ and ‘multiple resolutions...[and] data rates up to 10 MHz,’” is unrelated to the placement of *Ricquier*’s timing controller. Petition at 24. The authors of *Ricquier* chose to use CMOS technology “because “it offers the selective addressability” and the ability to program “multiple resolutions” required to meet the design goals. *Id.*; *see also id.* at 11 (“To realise the acquisition of image data only in specific regions of interest, an X-Y addressable architecture was selected.”). But this X-Y addressability and multiple resolution capability disclosed in *Ricquier* is a feature of **all** CMOS imagers and is the reason CMOS was chosen over CCD in the first instance. *See* Ex. 1060 at 2 (“They put an amplifier in each [pixel], along with circuits that allowed each pixel to be read out individually for features such as panning and zooming.”). Because Swift discloses a camera based on Dr. Fossum’s CMOS imager, its pixel array **already enjoys** that advantage.

121. Petitioner’s citation of *Ricquier*’s disclosure of “data rates up to 10 MHz” also does not provide motivation for Petitioner’s proposed combination as this performance characteristic does not result from implementing the timing controller “off chip.” Petition at 24. In fact, a POSITA understands that *Ricquier*’s off-chip driver placement **limits** the imager’s data rate because, like a traditional

CCD imager, such an architecture requires that “signals are coupled to a single output amplifier” (*Ricquier* at 10):

Typically, each column of CCD pixels is transferred to a corresponding cell of a serial output register, **whose output is amplified by a single on-chip amplifier** (e.g., a source follower transistor) before being processed in off-chip signal processing electronics. **As a result, the read-out frame rate is limited by the rate at which the on-chip amplifier can handle charge packets** divided by the number of pixels in the imager.

Ex. 2034 at 1:45–52 (emphasis added).

**C. Swift in view of Ricquier and Suzuki Does Not Disclose a Circuitry on a Second Circuit Board to Convert Pre-video Signal to a Post-Video Signal**

122. In my view, a POSITA would not have looked to *Suzuki* for ideas of how to implement the system architecture for a CMOS imager. *See* ¶¶ 116–117, *supra*.

123. Nor would a POSITA have modified *Swift* to place its pre-video to post-video conversion circuitry off-chip:

By consolidating many functions and reading images in a more efficient way, it requires one-hundredth the power of a CCD-based system. **And the chip does its own conversion from analog to digital for output on computer monitors or disk storage.** About all it needs is a power source and a lens to focus light on it.

Ex. 1060 at 1; *see also* Ex. 1048 (*Laser Focus World*) (disclosing that CMOS is the “preferred choice for implementation of on-chip signal processing”); *see also* ’052 Patent at 2:6-19 (discussing Fossum’s “camera on a chip”). Because Fossum’s (and therefore Swift’s) “camera on a chip” includes the “circuitry thereon to convert said pre-video signal to a post-video signal,” *Swift* does not disclose the claimed “circuitry” located on a second circuit board.

124. I understand that Petitioner asserts that the circuitry component mounted on circuit board 53 that is used to “process image signals received” from the image sensor is the claimed “circuitry... to convert said pre-video signal to a post-video signal.” Petition at 39 (citing Swift 9:7-13). But *Swift* does not disclose that circuit board 53 is responsible for this step. The evidence cited in the Petition only states that Swift’s **camera** outputs a signal that may be viewed on a monitor, not that the circuitry component mounted on circuit board 53 is responsible for converting a pre-video signal to a post-video signal. *See* Petition at 15-16 (citing Swift 8:31-9-13, 3:31-4:4); *see also id.* at 40 (citing Ex. 1005 at 15:7-8, 15:13-14, 17:34-18:3, 18:8-11).

125. In *Swift*’s CMOS sensor embodiments, a POSITA understands that the pre- to post-video conversion is done *on-chip*. Ex. 1060 at 1. Any further video processing carried out by the circuitry on circuit board 53 is performed on a signal already suitable “for output on computer monitors or disk storage.” Ex. 1060 at 1;

Ex. 1005 at 10. For example, as shown in Fig. 4b of the '052 Patent, the term video processing does not mean or even imply converting a “pre-video signal to a post-video signal.” Rather, video processing involves many other video conditioning procedures, including white balancing, for example. '052 Patent, Fig. 4b. In fact, a POSITA would understand that circuit board 53 in Figure 2 describes processing of post-video signal because a camera-on-a-chip image sensor would be a more efficient way to convert a pre-video signal to post-video signal. A separate circuit board 53 would be understood to provide *additional* post-video image signal processing, such as automatic gain control and automatic white balance, commonly found on separate image signal processing boards (and not used for converting pre-video to post-video signals).

**IX. *Larson* in View of *Swift*, *Ricquier* and *Suzuki* Does Not Render the Challenged Claims Obvious Under 35 U.S.C. § 103(a)**


126. *Larson* describes a CCD camera. To the extent a POSITA modified *Larson* in view of *Swift*, a POSITA would have used a CCD image sensor which provided superior performance and was a mature technology. A POSITA would not have replaced the CCD image sensor in *Larson* with a CMOS image sensor, especially not a passive pixel sensor (in *Ricquier*) used for machine vision applications.

127. Further, a POSITA looking at *Larson* would have been motivated to use a CCD sensor in *Swift* which provided better low-light capabilities which are

important in security and surveillance camera systems. Ex. 2036 at 226 (CCD was dominant technology for security and surveillance camera systems in 2007); Ex. 2036 (OIDA) at 8 (“CCDs have historically been the dominant image sensors and have been very successful in high speed applications such as digital cameras, digital copiers, and flat bed scanners. **CCDs are also appropriate for surveillance and manufacturing applications where high performance is a requirement. CCDs have traditionally had better light sensitivity** as a result of their pixel architecture, where all of the light hitting the array can potentially be converted to signal.”) (emphasis added).

I declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and that these statements were made with knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code.

Sworn to this 9th day of November, 2020 in San Francisco, California.

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Michael Lebby, Ph.D.



**APPENDIX A**  
**(List of Exhibits)**

<b>EXHIBIT No.</b>	<b>DESCRIPTION</b>
<b>Exhibit-2001</b>	Complaint for Patent Infringement in <i>Collect, LLC v. Samsung Electronics Co., LTD and Samsung Electronics America, Inc.</i> , 1:19-cv-00438, dated February 14, 2019.
<b>Exhibit-2002</b>	Proof of Service for Summons and Complaint, dated February 19, 2019.
<b>Exhibit-2003</b>	Scheduling Order in a Patent Case in <i>Collect, LLC v. Samsung Electronics Co., LTD and Samsung Electronics America, Inc.</i> , 1:19-cv-00438, dated June 10, 2019.
<b>Exhibit-2004</b>	E. Fossum, <i>Active-pixel sensors challenge CCD</i> , Laser Focus World, pp. 83-87, June 1993 (“Fossum”).
<b>Exhibit-2005</b>	Parties’ Joint Claim Construction Chart in <i>Collect, LLC v. Samsung Electronics Co., LTD and Samsung Electronics America, Inc.</i> , 1:19-cv-00438, dated May 8, 2020.
<b>Exhibit-2006</b>	U.S. Patent No. 5,754,313 (“Pelchy”).
<b>Exhibit-2007</b>	Zarnowski and Pace, <i>Imaging options expand with CMOS technology</i> , Laser Focus World, June 1997 (“Zarnowski”)
<b>Exhibit-2008</b>	U.S. Patent No. 4,491,865 (“Danna”).
<b>Exhibit-2009</b>	U.S. Patent No. 5,453,785 (“Lenhardt”).
<b>Exhibit-2010</b>	Hearing Transcript before Judge Hegarty, dated July 10, 2019.
<b>Exhibit-2011</b>	<i>Collect, LLC v. Samsung Electronics Co., LTD and Samsung Electronics America, Inc.</i> , 1:19-cv-00438 Docket Sheet.
<b>Exhibit-2012</b>	Declaration of Jonathan S. Caplan, dated March 17, 2020.
<b>Exhibit-2013</b>	Relationship of Challenged Patents and Related References.

<b>EXHIBIT NO.</b>	<b>DESCRIPTION</b>
<b>Exhibit-2014</b>	Patent Family Listing
<b>Exhibit-2017</b>	U.S. Patent No. 6,009,336 (“Harris”).
<b>Exhibit-2018</b>	U.S. Patent No. 6,417,882 (“Mahant-Shetti”).
<b>Exhibit-2019</b>	U.S. Patent No. 6,243,131 (“Martin”).
<b>Exhibit-2020</b>	U.S. Patent No. 5,162,913 (“Chatenever”).
<b>Exhibit-2021</b>	File History of U.S. Patent No. 6,310,642
<b>Exhibit-2022</b>	File History of U.S. Patent No. 5,986,693
<b>Exhibit-2023</b>	File History of U.S. Patent No. 5,929,901
<b>Exhibit-2024</b>	Ruyten, <i>Smear correction for frame transfer charge-coupled-device cameras</i> , Optics Letters, Vol. 24(13), pp. 878-880 (July 1, 1999)
<b>Exhibit-2025</b>	U.S. Patent No. 6,310,642 (“Adair ‘642”).
<b>Exhibit-2026</b>	U.S. Patent No. 6,073,034 (“Jacobson”).
<b>Exhibit-2027</b>	U.S. Patent No. 6,141,037 (“Upton”).
<b>Exhibit-2028</b>	U.S. Patent No. 6,147,366 (“Drottar”).
<b>Exhibit-2029</b>	U.S. Patent No. 5,929,901 (“Adair”).
<b>Exhibit-2030</b>	PCT WO 90/10361 (“Ullman”).
<b>Exhibit-2031</b>	PCT WO 95/15044
<b>Exhibit-2032</b>	U.S. Patent No. 5,896,375 (“Dent”).
<b>Exhibit-2033</b>	U.S. Patent No. 6,590,928 (“Haartsen”).
<b>Exhibit-2034</b>	U.S. Patent No. 5,471,515 (“Fossum ‘515”).
<b>Exhibit-2035</b>	U.S. Patent No. 5,986,693 (“Adair ‘693”).
<b>Exhibit-2036</b>	Image Sensors, OIDA’s Global Optoelectronics Industry Market Report and Forecast, October 2007.
<b>Exhibit-2037</b>	Samsung’s Invalidity Contentions, dated January 21, 2020.

EXHIBIT NO.	DESCRIPTION
<b>Exhibit-2039</b>	Armstrong, <i>NASA's Tiny Camera has a wide-angle future</i> , BusinessWeek, pp. 54-55, March 6, 1995. ("Armstrong").
<b>Exhibit-2040</b>	U.S. Patent No. 5,879,289 ("Yarush").
<b>Exhibit-2041</b>	U.S. Patent No. 7,369,176 ("Sonnenschein").
<b>Exhibit-2042</b>	File History of U.S. Patent No. 6,752,255
<b>Exhibit-2043</b>	U.S. Patent No. 5,986,693 ("Adair '693").
<b>Exhibit-2050</b>	Brian Ackland & Alex Dickinson, <i>Camera on a Chip</i> , 1996 IEEE INT'L SOLID-STATE CIRCUITS PROC. 22, 22-25, & 412 (1996).
<b>Exhibit-2051</b>	U.S. Patent No. 5,596,228 A, to Richard L. Anderton <i>et al.</i> ("Anderton").
<b>Exhibit-2052</b>	<i>1997 Product Timeline</i> , DIGIT. PHOTOGRAPHY REV., <a href="https://www.dpreview.com/products/timeline?year=1997&amp;brand=&amp;category">https://www.dpreview.com/products/timeline?year=1997&amp;brand=&amp;category</a> (last visited Oct. 20, 2020).
<b>Exhibit-2053</b>	Eric R. Fossum, <i>Active Pixel Sensors: Are CCD's Dinosaurs?</i> , 1900 SPIE: CHARGE-COUPLED DEVICES & SOLID-STATE OPTICAL SENSORS III 1, 1-13 (1993).
<b>Exhibit-2054</b>	Eric R. Fossum, <i>CMOS Image Sensors: Electronic Camera On A Chip</i> , 1995 IEEE INT'L ELECTRON DEVICES PROC. 17, 17-25 (1995).
<b>Exhibit-2055</b>	Eric R. Fossum <i>et al.</i> , <i>CMOS Active-Pixel Image Sensor Containing Pinned Photodiodes</i> , NASA TECH BRIEFS 40-42 (Oct. 1996).
<b>Exhibit-2056</b>	U.S. Patent No. RE42,974E, to Eric R. Fossum <i>et al.</i> ("Fossum Reissue"), a reissue of U.S. Patent No. 6,570,617, to same.

EXHIBIT NO.	DESCRIPTION
<b>Exhibit-2057</b>	KIRK J. HAVENS ET AL., <i>Thermal Imagers and System Considerations, in THERMAL IMAGING TECHNIQUES TO SURVEY AND MONITOR ANIMALS IN THE WILD</i> 101, 101-19 (2016) (“Havens”).
<b>Exhibit-2058</b>	GERALD C. HOLST, <i>CCD ARRAYS, CAMERAS, &amp; DISPLAYS</i> (2nd ed. 1998) (“Holst”).
<b>Exhibit-2059</b>	JAMES R. JANESICK, <i>History, Operation, Performance, Design, Fabrication and Theory, in SCIENTIFIC CHARGE-COUPLED DEVICES</i> 3, 22-37 (2001) (“Janesick”).
<b>Exhibit-2060</b>	Laura Johannes, <i>Advances in CMOS Chips Help Sales of Digital Cameras</i> , WALL ST. J., Aug. 21, 1998, <a href="https://www.wsj.com/articles/SB903661392760427500">https://www.wsj.com/articles/SB903661392760427500</a> .
<b>Exhibit-2061</b>	U.S. Patent No. 6,721,008 B2, to Paul P. Lee <i>et al.</i> (“Lee”).
<b>Exhibit-2062</b>	Dawn Levy, <i>News Release: Speedy Camera-On-A-Chip Unites Image Capture and Processing</i> , STANFORD NEWS SERV., Apr. 2001, <a href="https://news.stanford.edu/pr/01/digicam3425.html">https://news.stanford.edu/pr/01/digicam3425.html</a> .
<b>Exhibit-2063</b>	Elizabeth M. Lockyer, <i>Applications Hold the Key to Imager Choice</i> , PHOTONICS SPECTRA 80-90 (Mar. 1997).
<b>Exhibit-2064</b>	Sunetra Mendis <i>et al.</i> , <i>CMOS Active Pixel Image Sensor</i> , 41 IEEE TRANSACTIONS ON ELECTRON DEVICES 452, 452-53 (1994).
<b>Exhibit-2065</b>	Jun-ichi Nakamura <i>et al.</i> , <i>CMOS Active Pixel Image Sensor with Simple Floating Gate Pixels</i> , 42 IEEE TRANSACTIONS ON ELECTRON DEVICES 1693, 1693-94 (1995).

EXHIBIT NO.	DESCRIPTION
<b>Exhibit-2066</b>	Robert H. Nixon <i>et al.</i> , <i>256 x 256 CMOS Active Pixel Sensor Camera-On-A-Chip</i> , 1996 IEEE INT’L SOLID-STATE CIRCUITS PROC. 178, 178-79, 440 (1996).
<b>Exhibit-2067</b>	Robert Nixon <i>et al.</i> , <i>Active-Pixel Image Sensor Integrated with Readout Circuits</i> , NASA TECH BRIEFS 38-40 (Oct. 1996).
<b>Exhibit-2068</b>	Peter J.W. Noble, <i>Self-Scanned Silicon Image Detector</i> , ED-15 IEEE TRANSACTIONS ON ELECTRON DEVICES 202, 202-09 (1968).
<b>Exhibit-2069</b>	JUN OHTA, SMART CMOS IMAGE SENSORS & APPLICATIONS (CRC Press, Taylor & Francis Group 2008).
<b>Exhibit-2070</b>	U.S. Patent No. 8,279,313 B2, to Howard E. Rhodes (“Rhodes”).
<b>Exhibit-2071</b>	Santa Barbara Instrument Group, <i>Operating Manual for the Model ST-5C Advanced CCD Camera</i> (5th ed., May 1998), <a href="https://diffractionlimited.com/downloads/legacy/st5cman.pdf">https://diffractionlimited.com/downloads/legacy/st5cman.pdf</a> (“SBIG”).
<b>Exhibit-2072</b>	George E. Smith, <i>The Invention of the CCD</i> , 471 NUCLEAR INSTRUMENTS & METHODS PHYSICS RSCH. A 1, 1-5 (2001).
<b>Exhibit-2073</b>	U.S. Patent No. 5,262,871 A, to Joseph Wilder <i>et al.</i> (“Wilder”).
<b>Exhibit-2074</b>	<i>Licensing Our Technology to Medical Device Manufacturers</i> , Micro Imaging Solutions LLC, <a href="https://micro-imaging.us/licensing">https://micro-imaging.us/licensing</a> (last visited Oct. 20, 2020).
<b>Exhibit-2075</b>	Deposition Transcript of Dean Neikirk, Ph.D. (Oct. 8, 2020).
<b>Exhibit-2076</b>	Deposition Transcript of Dean Neikirk, Ph.D. (Sept. 30, 2020).
<b>Exhibit-2077</b>	Deposition Transcript of Dean Neikirk, Ph.D. (Oct. 1, 2020).

EXHIBIT NO.	DESCRIPTION
<b>Exhibit-2078</b>	<i>Charged-Coupled Device</i> , WIKIPEDIA, Aug. 15, 2020, <a href="https://en.wikipedia.org/w/index.php?title=Charge-coupled_device&amp;oldid=973099011">https://en.wikipedia.org/w/index.php?title=Charge-coupled_device&amp;oldid=973099011</a> .
<b>Exhibit-2079</b>	ITRS, INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS: EXECUTIVE SUMMARY (Wolfgang Arden et al. eds., 2d ed., 2001).
<b>Exhibit-2080</b>	<i>International Technology Roadmap for Semiconductors</i> , WIKIPEDIA, Jul. 11, 2020, <a href="https://en.wikipedia.org/w/index.php?title=International_Technology_roadmap_for_Semiconductors&amp;oldid=967213969">https://en.wikipedia.org/w/index.php?title=International_Technology_roadmap_for_Semiconductors&amp;oldid=967213969</a> .
<b>Exhibit-2081</b>	ITRS, INTERNATIONAL TECHNOLOGY ROADMAP FOR SEMICONDUCTORS: EXECUTIVE SUMMARY (Wolfgang Arden et al. eds., 10th ed., 2009).
<b>Exhibit-2082</b>	Eric R. Fossum, <i>CMOS Active Pixel Sensor (APS) Technology for Multimedia Image Capture</i> , 1997 MULTIMEDIA TECH. & APPLICATIONS PROC. 1, 1-5 (1997)
<b>Exhibit-2083</b>	Secretary's Office, <i>News Release: Hitachi Releases New MPEG Camera with Enhanced Presentations Features</i> , Hitachi, Ltd., Nov. 19, 1997, <a href="http://www.hitachi.com/New/cnews/E/1997/971119B.html">www.hitachi.com/New/cnews/E/1997/971119B.html</a> (last visited Oct. 20, 2020).
<b>Exhibit-2084</b>	Southwest Museum of Engineering, Communications & Computation, <i>Hitachi</i> , SMECC (2007), <a href="https://www.smecc.org/hitachi.htm">https://www.smecc.org/hitachi.htm</a> (last visited Oct. 20, 2020).

EXHIBIT NO.	DESCRIPTION
<b>Exhibit-2085</b>	Albert Theuwissen, <i>CMOS Image Sensors: State-Of-The-Art and Future Perspectives</i> , 2007 EUR. SOLID-STATE CIRCUITS PROC. 21, 21-27 (2007).
<b>Exhibit-2086</b>	Dan Lockney, NASA, <i>Image Sensors Enhance Camera Technologies</i> , NASA Spinoff, (2010) <a href="https://spinoff.nasa.gov/Spinoff2010/cg_3.html">https://spinoff.nasa.gov/Spinoff2010/cg_3.html</a> (last visited Sept. 3, 2020).
<b>Exhibit-2087</b>	Brian Dunbar, NASA, <i>NASA Technology is All Around You</i> , NASA, Dec. 12, 2016 (last updated Aug. 6, 2017), <a href="https://www.nasa.gov/specials/apollo50th/index.html">https://www.nasa.gov/specials/apollo50th/index.html</a> .
<b>Exhibit-2088</b>	Declaration of Michael Lebby, Ph.D.
<b>Exhibit-2089</b>	Marc J. Philippon, <i>A New Technology Platform for Arthroscopy</i> , U.S. ORTHOPAEDIC PROD. NEWS: FUTURETECH, Jul.-Aug. 2007, at 1-3.
<b>Exhibit-2090</b>	Robin Young, <i>The Eleven Best Sports Medicine Technologies for 2016</i> , Orthopedics This Week, Jul. 14, 2016, <a href="https://ryortho.com/2016/07/the-eleven-best-sports-medicine-technologies-for-2016/">https://ryortho.com/2016/07/the-eleven-best-sports-medicine-technologies-for-2016/</a> , (last visited Oct. 18, 2020).
<b>Exhibit 2091</b>	Van Nostrand Reinhold Dictionary of Information Technology p. 471 (3d ed. 1989)
<b>Exhibit 2092</b>	L. Kozlowski, <i>Development Status of CMOS 1920 x 1080 Imaging system-on-Chip for 60p and 72p HDTV</i> , SMPTE Motion Imaging (Oct./Nov. 2004)
<b>Exhibit 2093</b>	G. Albert Lemke, <i>Microelectronics Packaging Handbook</i> , (Rao R. Tummala et al. eds. 1989) (“Tummala”)
<b>Exhibit 2094</b>	Shichun Qu <i>et al.</i> , <i>Wafer-Level Chip-Scale Packaging</i> , (2013) (“Qu”)
<b>Exhibit 2095</b>	Deposition of Dean Neikirk, Ph.D IPR2020-00512 (Oct. 9, 2020).

<b>Exhibit-2096</b>	Authenticated version of Exhibit 2052, <i>1997 Product Timeline</i> , Digit. Photography Rev., <a href="https://www.dpreview.com/products/timeline?year=1997&amp;brand=&amp;category">https://www.dpreview.com/products/timeline?year=1997&amp;brand=&amp;category</a> (last visited Oct. 20, 2020), (“Authenticated Ex. 2052”).
<b>Exhibit-2097</b>	Authenticated version of Exhibit 2062, Dawn Levy, <i>News Release: Speedy Camera-On-A-Chip Unites Image Capture and Processing</i> , Stanford News Serv., Apr. 2001, <a href="https://news.stanford.edu/pr/01/digicam3425.html">https://news.stanford.edu/pr/01/digicam3425.html</a> , (“Authenticated Ex. 2062”).
<b>Exhibit-2098</b>	Authenticated version of Exhibit 2083, Secretary’s Office, <i>News Release: Hitachi Releases New MPEG Camera with Enhanced Presentations Features</i> , Hitachi, Ltd., Nov. 19, 1997, <a href="http://www.hitachi.com/New/cnews/E/1997/971119B.html">www.hitachi.com/New/cnews/E/1997/971119B.html</a> (last visited Oct. 20, 2020), (“Authenticated Ex. 2083”).
<b>Exhibit-2099</b>	Authenticated version of Exhibit 2084, Southwest Museum of Engineering, Communications & Computation, <i>Hitachi</i> , SMECC (2007), <a href="https://www.smecc.org/hitachi.htm">https://www.smecc.org/hitachi.htm</a> (last visited Oct. 20, 2020), (“Authenticated Ex. 2084”).
<b>Exhibit-2100</b>	Authenticated version of Exhibit 2086, Dan Lockney, NASA, <i>Image Sensors Enhance Camera Technologies</i> , NASA Spinoff, (2010) <a href="https://spinoff.nasa.gov/Spinoff2010/cg_3.html">https://spinoff.nasa.gov/Spinoff2010/cg_3.html</a> (last visited Sept. 3, 2020), (“Authenticated Ex. 2086”).
<b>Exhibit-2101</b>	Authenticated version of Exhibit 2087, Brian Dunbar, NASA, <i>NASA Technology is All Around You</i> , NASA, Dec. 12, 2016 (last updated Aug. 6, 2017), <a href="https://www.nasa.gov/specials/apollo50th/index.html">https://www.nasa.gov/specials/apollo50th/index.html</a> , (“Authenticated Ex. 2087”).
<b>Exhibit-2102</b>	Authenticated version of Exhibit 2090, Robin Young, <i>The Eleven Best Sports Medicine Technologies for 2016</i> , Orthopedics This Week, Jul. 14, 2016, <a href="https://ryortho.com/2016/07/the-eleven-best-sports-medicine-technologies-for-2016/">https://ryortho.com/2016/07/the-eleven-best-sports-medicine-technologies-for-2016/</a> , (last visited Oct. 18, 2020), (“Authenticated Ex. 2090”).



## APPENDIX B (Curriculum Vitae)

### Michael Lebby



#### **EDUCATION:**

2004, Doctor of Engineering (D. Eng.)  
University of Bradford, United Kingdom  
Citation, “*Technical Contributions to Optoelectronics*”  
(NB: This is a higher doctorate awarded on technical contribution to the field)

1987, Ph.D.  
University of Bradford, United Kingdom  
Thesis, “*Characterization and Fabrication of the HFET and BICFET*”

1985, MBA  
University of Bradford, United Kingdom  
Thesis, “*Small Business Planning for a Start-up*”

1984, Bachelors (B. Eng. – Honours)  
University of Bradford, United Kingdom  
Thesis, “*Computer Aided Testing of Semiconductor Devices*”

#### **SUMMARY OF TECHNICAL EXPERTISE:**

Dr. Lebby started work in telecommunications in 1977, and has over 40 years of experience in a number of technical disciplines and technologies. Dr. Lebby is well versed in electronics, semiconductor physics, optoelectronics, optics, materials, electrical engineering in general. Dr. Lebby has experience in commercial and industrial research of technologies such as silicon, compound semiconductors, manufacturing, fabrication, design, simulation, testing, evaluation, reliability, qualification of new ideas, concepts and products. The types of products that Dr. Lebby understands include, but are not limited to; Light Emitting Diodes (LEDs), Laser Diodes (LDs), photodetectors (PDs), optical waveguides, fiber optics, displays (LCD, LED, OLED), plastic photonics, optical polymers, sensors, LIDAR, solar cells, lighting, data communication, CMOS, and even new opportunities such as medical and life science applications for photonics. Dr. Lebby is internationally known for his work with integrated photonics, PICs (Photonic Integrated Circuits), silicon photonics, and semiconductor technologies such as InP, GaAs, III-GaN, silicon, as well as SiGe and silicon ICs (MOSFETs, FinFETs, bipolar), power FETs, RF FETs, various display technologies etc. Dr. Lebby has worked with DC current as well as AC current, high frequency design, microwave design, and multi-wavelength, visible wavelengths, in addition to 850nm/1310nm/1500nm/NIR fiber optic communications. Dr. Lebby has over 200 issued utility patents with the USPTO in subjects such as electronics, optoelectronics, photonics, packaging, transceiver modules, optical sub-assemblies, materials, epitaxial growth, device design, assembly, and various active and passive components (both electronic and optoelectronic). Dr. Lebby regularly receives invites to speak at technical conferences. Dr. Lebby has appeared in panels and interviews many times. Dr. Lebby is currently chairman of the International PIC conference based in Europe (for the past 5 years since its conception in 2015). Dr. Lebby is a Fellow of the IEE and OSA.

Dr. Lebby has participated in over 80 patent litigation cases, including over 10 trials and 30 depositions. Dr. Lebby has authored numerous (probably 100-200) expert reports and is familiar with State (District), Federal (ITC) and PTAB-IPR court processes for expert witness testimony.

#### **BIOGRAPHY:**

## Declaration of Dr. Lebby

### IPR2020-00512 (U.S. Patent No. 9,186,052)

Biography: Michael S. Lebby joined Lightwave Logic as a member of the Board of Directors in 2015. In May 2018, Dr. Lebby assumed the role of CEO, Lightwave Logic Inc (LWLG:OTCQB). Lightwave Logic is a leading technological company commercializing Electro-Optical polymers. Dr. Lebby (born 1961, London, UK) is an Anglo-American entrepreneur and intrapreneur in the fields of optoelectronics/photonics electronics and semiconductors. Dr. Lebby's career started with the British Government in 1977 in telecommunications and he did research at their research labs (RSRE Malvern) in the early 1980s. Dr. Lebby worked at AT&T's research labs: Bell Labs (1985-1989) in photonics, and subsequently drove the development (and co-authored the first patent) of the oxide VCSEL diode laser at Motorola in the 1990s (which is now used in laser mice, 3D sensing/FaceID in mobile phones, optical interconnects; where volumes of the laser are over 1B units today). From 2005-2010 he led the USA trade association in optoelectronics (OIDA) and represented the optoelectronics and photonics industry on Capitol Hill. Dr. Lebby has run technical start-ups and commercialized optoelectronic and photonics technology into volume manufacturing. Dr. Lebby has also had roles as a Venture Capitalist specializing in Optical Communications. He is currently a technical expert to the European Commission. He is a Fellow member of IEEE and OSA, and has been voted PIC (Photonic Integrated Circuit) business leader of the year by the PIC International Conference in 2018. Dr. Lebby holds over 450 issued international patents in photonics and electronics, that have been derived from over 220 issued USPTO utility patents, mostly in the field of optoelectronics, photonics and semiconductors. He has been cited by the USPTO to be in the most prolific 75 inventors in USA from 1988-1997. Dr. Lebby is passionate about photonics and has focused his efforts over the last 30years to drive new photonics manufacturing programs in USA and Europe as well as industry-based photonics technology roadmaps.

#### **WORK HISTORY:**

2003 – Present

**Oculi LLC, CEO and CTO (part-time consulting)**

Oculi provides consulting in expert witness, trial, deposition, expert reports, infringement, invalidity, and various patent and IP litigation in photonics, optoelectronics, semiconductors, and fiber optic telecommunication technology segments. Patent agencies have included: IMS Expert Services, Thomson Reuters Expert Witness Services, LitXpert Expert Witness Group, Teklicon Expert Witness Agency, Beche Expert Services Group, Forensis Group: Expert Witness Services, and Expertconnect.

2015 – Present

**Lightwave Logic (LWLG:OTCQB), CEO & Director, Board of Directors**

In 2015 Lebby became a director of Lightwave Logic to assist in the company for competitive optical modulator products and associated packaging, manufacturing, and technology roadmaps/marketing. In May 2017, Lebby became CEO of Lightwave Logic.

2014 – 2016

**University Southern California, Director CFR (Corporate & Foundation Relations)**

Lebby assisted USC Viterbi Engineering to foster tighter faculty-industry relationships in high technology, IT, social media, graphic arts, electronics, photonics (solar, display, medical) and fiber communications segments.

2013 – Present

**European Commission, Technical Expert**

In 2013 Lebby became a technical expert for the Photonics Unit of the European Commission. Lebby has participated in organizing workshops, lectures, evaluating photonics proposals, and advising the Commission on funded projects. Lebby currently is an advisor on 5 photonics pilot lines (MIRPHAB, PI-SCALE, PIX4LIFE, PIXAPP, InPULSE) and a photonics based cardiovascular disease program (CARDIS).

2013 – 2015

**OneChip Photonics Corporation, President and CEO**

Elected independent board member in focusing on technical and business operational strategy for communications based InP Photonic Integrated Circuit (PIC) and optoelectronic Integrated Circuit (OEIC) platforms for Onechip Photonics in 2008.

2013 – 2015

**Glyndŵr University, Professor, Chair of Optoelectronics**

## Declaration of Dr. Lebby

### IPR2020-00512 (U.S. Patent No. 9,186,052)

In 2013 Lebby became full Professor of Optoelectronics (part-time) to assist Glyndwr University to position itself as a leader in optoelectronics and photonics. Areas of focus include design, simulation, and testing of 100G/400G photonic integrated circuits (PICs) and optoelectronics integrated circuits (OEICs), laser diodes, optics, and solar cells.

2010 – 2013                      **Translucent, Inc., GM and CTO**

Lebby positioned Translucent on the product development and manufacture of epitaxial semiconductor wafers for the solar, power and lighting industries. Lebby led the R&D and development of MBE based rare earth oxide single crystal epitaxial layers deposited onto large silicon wafers. On top of these wafers both MBE and MOCVD Gallium Nitride epitaxial device layers were grown for devices. The use of GaN-on-Si is expected to be a strong catalyst for change in the power electronics and LED lighting industries. In a parallel program at Translucent, Lebby led the development efforts to develop and productize Germanium-Tin (GeSn) template wafers onto large format silicon wafers (Ge-on-Si) to enable cost effective, and ultra-high efficiency multi-junction solar cells for the CPV industry. Areas of advanced interconnect using new and novel material compounds were explored.

2005 – 2010                      **OIDA** (Optoelectronic Industry Development Association), *Executive Director, President, and CEO (Board Member)*

Lebby represented the optoelectronics industry and organized technical conferences/workshops/forecasts with industry roadmaps. Initiated green photonics metrics. Lebby positioned OIDA as a national resource in the field of optoelectronics, and has represented industry in many capacities ranging from talks, papers, expert witness, testimony, market and technical reports. Lebby created *new industry-based initiatives* in fiber optics broadband as well as the green photonics movement (solar technologies, LED lighting technologies) that is now occurring globally.

2003 – 2005                      **OCLARO, VP Technology and Business Development**

Telecommunication optoelectronic components, San Jose, Ca. Focus on technology strategy for components and sub-systems.

2001– 2003                      **Ignis Optics, President and CEO (Founder/Board Member)**

Venture-backed start-up, San Jose, California manufacturing 10Gbps fiber optic transceivers.

1999 – 2001                      **Intel Capital, Director Business Development/Investor (w/Board observer positions on Investment)**

Intel Capital, Santa Clara, California. In 1999, Lebby joined Intel as a corporate investor and was responsible for sourcing, negotiating, and closing private placement equity deals in the optical networking, component, and semiconductor arenas.

1998 – 1999                      **TE Connectivity, Director Technology/BD (Fiber Optics)**

Global Optoelectronics Division: Technology strategy for optical communications products.

1989 – 1998                      **Motorola, R&D Manager**

Corporate R&D Labs, Tempe, Arizona. Optoelectronics: VCSEL based product solutions (OPTOBUS); materials, devices, packaging, systems. Lebby was also the lead inventor in Motorola's history with over 150 issued utility patents. Lebby worked in the silicon and compound semiconductor fabrication plants (fabs) to become proficient in deposition/etching/alignment tooling

1985 – 1989                      **AT&T, Researcher**

# Declaration of Dr. Lebby

## IPR2020-00512 (U.S. Patent No. 9,186,052)

AT&T Bell Labs - Photonics Research Dept (Dept 11366), Holmdel, NJ. Lebby designed and fabricated new GaAs and InP optoelectronic devices that were grown both by MOCVD and MBE.

1977 – 1984

**UK Ministry of Defense, Apprenticeship/Journeyman + Electronics Engineer (REME – Royal Electrical and Mechanical Engineers, and RSRE – Royal Signals and Radar Establishment)**

Dr. Lebby started his career at the Royal Electrical and Mechanical Engineer (REME) division of the Ministry of Defence in the UK. Lebby was a telecommunications apprentice, and repaired all types of radio/RF communications equipment. Lebby qualified as a fully qualified Journeyman or Apprentice specializing in telecommunications in 1980. Dr. Lebby moved to the Royal Signal and Radar Establishment (RSRE) to study material and characterization issues of GaAs and InP devices.

### SELECTED PROFESSIONAL ACTIVITIES & AWARDS:

- Voted winner at the PIC Conference (Photonic Integrated Circuits) as PIC Entrepreneur and Business Leader of the Year (March 2018).
- Dr. Lebby is **co-inventor of the oxide VCSEL** (semiconductor laser) that is now being utilized for consumer applications (*Face ID of Apple's iPhone as an example*). US Patent #5359618 "High Efficiency VCSEL and Method of Fabrication" issued 25<sup>th</sup> October 1994.
- Dr. Lebby was recognized professionally as a **Fellow of IEEE (2005) and OSA (2007)** with his technical contributions to the field of optoelectronics.
- As an inventor Dr. Lebby has achieved **~220 issued utility patents with the USPTO**.
- As an inventor Dr. Lebby has ~70 published utility patent applications with the USPTO
- As an inventor Dr. Lebby has over 450 issued patents world-wide if international derivatives are counted.
- Dr. Lebby's novel laser-based device, packaging, modules designs led Motorola to sell their patent portfolio independently where a number of the patents have "very high licensing coefficients." Dr. Lebby was given a special award from the Chairman of Motorola for exemplary patent invention accomplishments in 1998 and **#1 prolific inventor in Motorola's history**.
- **Over 60 publications** ([www.linkedin.com/in/lebby](http://www.linkedin.com/in/lebby))
- **Over 200 public media activities** (that include: Books, Chapters, Reports, Abstracts, Videos, Lectures, Speeches, Reviews, Courses, Talks, Invited Talks, Keynote Talks, Plenary Talks, Webinars, Interviews, Articles, etc.). See at [www.linkedin.com/in/lebby](http://www.linkedin.com/in/lebby)
- Author of OIDA's **annual market optoelectronics report** and forecast (2009 version is over 600 pages), which receives international exposure and recognition. Regularly interacts with government agencies in Washington DC on photonics-based projects (DARPA, ARPA-E, NIH, NSF, DOE, NIST, DoD etc.). Typical chapters included: LEDs, laser diodes, fiber optic communications, sensors, displays, solar, green photonics, military photonics, and applications of photonics such as solid-state lighting, automotive, medical, etc.
- Is the recipient of a **2nd doctorate** (higher) from Bradford University, UK, and only the second in the universities history to receive a D.Eng from industry (rest being academia).
- **Entrepreneur** at: (i) Motorola: Co-founded Optobus division – VCSEL laser based parallel optical interconnect solution, and (ii) Intel: Co-founded the Intel optics division for silicon photonics where over \$300M was initially invested for the division.
- **Entrepreneur**: Founded (and CEO) Ignis Optics Inc., a venture backed company (>\$30M) that designed and manufactured 10Gbps fiber optic transceivers. Sold the company to Bookham (Naq: BKHM) in 2003. Restructured OneChip Photonics (as CEO) through bankruptcy, and new VC-based funding. Assisted in the raising of >\$50M VC funding as a member of BoD.
- **IEEE CPMT Board of Governors** ('98- '02); IEEE Phoenix Waves and Devices Junior Engineer of the Year (1993); CPMT Distinguished lecturer (2000), CPMT technical committee (TC-10 & ECTC) 1991 to present
- Advised at **Board of Director** level for a number of technical start-ups
- **Chartered Engineer** (C.Eng) from IEE (UK). The chartered engineering status is equivalent to the US PE (professional engineer)

### EXPERT WITNESS EXPERIENCE:

1. Active case work: 1Q2009 (March 24<sup>th</sup> 2009); *Testimony: US-China Economic and security review commission on the optoelectronics industry. US Congress, Capitol Hill*; Written statement on the status of the USA optoelectronics industry with aural cross-examination by the commission. Trial experience.
  - a. Deposition: 0 (Cumulative total: 0)
  - b. Trial/Hearing/Court appearance: 1 (Cumulative total: 1)

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- c. Technology: Optoelectronics (optical storage, fiber optic communications, sensors, high power lasers, LED lighting, etc).
2. Active case work: 3Q2010-1Q2011; *Finisar Corp. v. Optical Communication Products Inc.*, No. 10-CV-05617 and No. 11-cv-00104 (retained by plaintiff - Morgan, Lewis & Bockius LLP).
  - a. Deposition: 0 (Cumulative total: 0)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 1)
  - c. Technology: semiconductor lasers/VCSSELs, fiber optic transceiver modules
3. Active case work: 1Q2011; *Ziptonix, Inc. v. OmniVision Technologies, Inc., Taiwan Semiconductor Manufacturing Company Ltd., and TSMC North America Corp.*, No. 11-CV-5235 (retained by plaintiff – Alston Bird LLP).
  - a. Deposition: 0 (Cumulative total: 0)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 1)
  - c. Technology: CMOS image sensors; design and fabrication
4. Active case work: 3Q2011 to 3Q2012; *Certain Light-Emitting Diodes and Products Containing Same*, Inv. No. 337-TA-798 (USITC filed July 15, 2011) (retained by respondent Samsung – Covington & Burling LLP). Deposition (x2) and trial experience.
  - a. Deposition: 3 (Cumulative total: 3)
  - b. Trial/Hearing/Court appearance: 1 (Cumulative total: 2)
  - c. Technology: LEDs, device design, color gamut, packaging, optical lensing.
5. Active case work: 3Q2011 to 2Q2015; *Cheetah Omni, LLC v. Alcatel-Lucent USA Inc.*, No. 11-CV-390 (E.D. Tex. filed July 29, 2011) (retained by plaintiff – Brooks Kushman). Deposition experience (x2).
  - a. Deposition: 1 (Cumulative total: 4)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 2)
  - c. Technology: Fiber optic networks, optical switches, ROADMs and optical filters.
6. Active case work: 4Q2012 to 3Q2014; *Finisar Corp. v. Cheetah Omni, LLC*, No. 11-CV-15625 (E.D. Mich. filed Dec. 23, 2011) (retained by defendant – Brooks Kushman). Deposition experience (x1).
  - a. Deposition: 1 (Cumulative total: 5)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 2)
  - c. Technology: Wavelength optical switches, optical filters, and optical components.
7. Active case work: 4Q2012 to 3Q2013; *Certain Optoelectronic Devices for Fiber Optic Communications, Components Thereof, and Prods. Containing the Same*, Inv. No. 337-TA-860 (USITC filed Sept. 24, 2012) (retained by respondent – Mellanox, IPtronics and FCI Inc and counsel Alston & Bird LLP). Deposition (x2) and trial experience.
  - a. Deposition: 2 (Cumulative total: 7)
  - b. Trial/Hearing/Court appearance: 1 (Cumulative total: 3)
  - c. Technology: IC design, layout, and operation; especially laser driver chips for VCSSELs. High speed laboratory testing.
8. Active case work: 3Q2014 to 2Q2015; *Microscan Sys., Inc. v. Cognex Corp.*, No. 14-CV-6952 (S.D.N.Y. filed Aug. 27, 2014) (retained by plaintiff – Morrison & Foerster LLP). Deposition (x1) and trial experience.
  - a. Deposition: 1 (Cumulative total: 8)
  - b. Trial/Hearing/Court appearance: 1 (Cumulative total: 4)
  - c. Technology: Bar code scanners and associated optics such as imagers, lasers, LEDs, molded optics. Laboratory testing.
9. Active case work: 2Q2014 to 1Q2016; *Avago Techs. Fiber IP (Singapore) PTE Ltd. v. IPtronics Inc.*, No. 10-CV-2863 (N.D. Cal. filed June 29, 2010) (retained by respondent – Alston & Bird LLP).
  - a. Deposition: 0 (Cumulative total: 8)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 4)
  - c. Technology: IC design, layout, and operation; especially laser driver chips for VCSSELs. High speed laboratory testing.
10. Active case work: 1Q2015 to 3Q2015; *Regarding certain optical disc drives*, Inv. No. 337-TA-897 (USITC filed Oct. 21, 2013) (retained by respondent – O’Melveny & Myers LLP).
  - a. Deposition: 0 (Cumulative total: 8)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 4)
  - c. Technology: CD, CVD, BluRay optical disk drives, optical components, laser diodes, and optical beam patterns. Laboratory testing of visible optics.
11. Active case work: 1Q2015 to 2Q2015; *BMW of N. Am., LLC v. Innovative Display Techs., LLC*, No. IPR2015-00933, IPR2015-00934 (P.T.A.B. filed Mar. 24, 2015) (retained by plaintiff – Crowell Moring LLP).
  - a. Deposition: 0 (Cumulative total: 8)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 4)
  - c. Technology: LED backlights for vehicles; LED package and optical module/luminaire design.
12. Active case work: 1Q2015 to 2Q2015; *BMW of N. Am., LLC v. Innovative Display Techs., LLC*, No. IPR2015-00934 (P.T.A.B. filed Mar. 24, 2015) (retained by plaintiff – Crowell Moring LLP).
  - a. Deposition: 0 (Cumulative total: 8)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 4)
  - c. Technology: LED backlights for vehicles; LED package and optical module/luminaire design.
13. Active case work: 1Q2015 to 3Q2016; *OneChip Photonics Inc.*, Pre-litigation IP Case No. TBD; (retained by plaintiff – Patent Monetization Inc. (PMI)).
  - a. Deposition: 0 (Cumulative total: 8)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 4)

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- c. Technology: Photonic Integrated Circuits using InP (Indium Phosphide); lasers, detectors, waveguides, mux/demux, spot size converters.
- 14. Active case work: 2Q2016; *IDT v. Hyundai Motor Co.*, No. 14-CV-201 (E.D. Tex. filed May 4, 2015) (retained by defendant – DLA Piper LLP).
  - a. Deposition: 0 (Cumulative total: 8)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 4)
  - c. Technology: LED devices, packages and modules for vehicles.
- 15. Active case work: 1Q2015 to 3Q2015; *Cree Inc. v. Honeywell Int'l Inc.*, No. 3:14-CV-737 (W.D. Wisc. filed Oct. 28, 2014) (retained by defendant - Arnold & Porter LLP). Deposition experience (x1).
  - a. Deposition: 1 (Cumulative total: 9)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 4)
  - c. Technology: LEDs for mobile phones; LED epitaxial layers, device designs, optical lensing, packaging. Laboratory reverse engineering using TEM/SEM/EDAX etc.
- 16. Active case work: 2Q2015 to 4Q2015; *Trs. of Boston Univ. v. Everlight Elecs. Co.*, Nos. 12-CV-11935, 12-CV-12326, 12-CV-12330 (D. Mass. filed Oct. 17, 2012) (retained by plaintiff - Shore Chan DePumpo LLP). Deposition (x1) and trial experience.
  - a. Deposition: 1 (Cumulative total: 10)
  - b. Trial/Hearing/Court appearance: 1 (Cumulative total: 5)
  - c. Technology: GaN buffer layers for LEDs, and associated technical marketing, sales and import process into USA.
- 17. Active case work: 3Q2015 to 3Q2016; *LG Elecs. Inc. v. Toshiba Samsung Storage Tech. Corp.*, No. 12-CV-1063 (D. Del. filed Aug. 22, 2012) and IPR2015-01659 (PTAB filed Jul. 31<sup>st</sup> 2015) (retained by plaintiff – DLA Piper & Nixon Law). IPR deposition (*i.e.* trial) experience (x1).
  - a. Deposition: 1 (Cumulative total: 11)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 1 (Cumulative total: 1)
  - d. Technology: Optical storage using laser diodes, photodetectors and optical materials
- 18. Active case work: 3Q2015 to 3Q2016; *LG Elecs. Inc. v. Toshiba Samsung Storage Tech. Corp.*, No. 12-CV-1063 (D. Del. filed Aug. 22, 2012) and IPR2015-01642 (PTAB filed Jul. 30<sup>th</sup> 2015) (retained by plaintiff – DLA Piper & Nixon Law).
  - a. Deposition: 0 (Cumulative total: 11)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 1)
  - d. Technology: Optical storage using laser diodes, photodetectors and optical materials
- 19. Active case work: 3Q2015 to 3Q2016; *LG Elecs. Inc. v. Toshiba Samsung Storage Tech Corp.*, IPR2016-01677 (PTAB filed Aug. 24<sup>th</sup> 2016) (retained by plaintiff – DLA Piper & Nixon Law).
  - a. Deposition: 0 (Cumulative total: 11)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 1)
  - d. Technology: Optical storage using laser diodes, photodetectors and optical materials
- 20. Active case work: 3Q2015 to 3Q2016; *LG Elecs. Inc. v. Toshiba Samsung Storage Tech. Corp.*, IPR2015-01678 (PTAB filed Aug. 24<sup>th</sup> 2016) (retained by plaintiff – DLA Piper & Nixon Law).
  - a. Deposition: 0 (Cumulative total: 11)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 1)
  - d. Technology: Optical storage using laser diodes, photodetectors and optical materials
- 21. Active case work: 3Q2015 to 3Q2016; *LG Elecs. Inc. v. Toshiba Samsung Storage Tech. Corp.*, IPR2015-01644 (PTAB filed Jul. 30<sup>th</sup> 2015) (retained by plaintiff – DLA Piper & Nixon Law).
  - a. Deposition: 0 (Cumulative total: 11)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 1)
  - d. Technology: Optical storage using laser diodes, photodetectors and optical materials
- 22. Active case work: 3Q2015 to 3Q2016; *LG Elecs. Inc. v. Toshiba Samsung Storage Tech. Corp.*, IPR2015-01653 (PTAB filed Jul. 31<sup>st</sup> 2015) (retained by plaintiff – DLA Piper & Nixon Law).
  - a. Deposition: 0 (Cumulative total: 11)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 1)
  - d. Technology: Optical storage using laser diodes, photodetectors and optical materials
- 23. Active case work: 3Q2015; *Heptagon* Pre-litigation IPR petition; (retained by plaintiff – Proskauer Rose LLP).
  - a. Deposition: 0 (Cumulative total: 11)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 1)
  - d. Technology: Proximity sensors using LEDs, photodetectors and innovative semiconductor packaging.
- 24. Active case work: 1Q2016 to 2Q2017; *Dentsply v. Am. Orthodontics Inc.*, No. 15-CV-1706 (D. Pa. filed Sept. 1, 2015) and IPR2016-01652 (PTAB filed Aug. 19<sup>th</sup> 2016) (retained by defendant – Godfrey Kahn LLP). IPR deposition (x1) experience.
  - a. Deposition: 1 (Cumulative total: 12)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 1 (Cumulative total: 2)
  - d. Technology: High power lasers (YAG, CO2) to engrave and scribe dental orthodontic brackets.

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25. Active case work: 2Q2016 to 2Q2017; *Koninklijke Philips N.V. v. Elect-tech Int'l (H.K.)*, No. 14-CV-2737 (N.D. Cal. filed Aug. 12, 2015) (retained by plaintiff – Reed Smith LLP).
  - a. Deposition: 0 (Cumulative total: 12)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 2)
  - d. Technology: Trade secret MOCVD epitaxial growth techniques for high power GaN/InGaN LED technology
26. Active case work: 2Q2016 to 4Q2016; *Bluestone Innovations llc. v. E. Mishan & Co. Inc.*, Pre-litigation IP Case No. TBD; (retained by defendant - Notaro, Michalos, & Zaccaria P.C.).
  - a. Deposition: 0 (Cumulative total: 12)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 2)
  - d. Technology: GaN/InGaN LEDs on structured substrates with reverse engineering laboratory analysis.
27. Active case work: 3Q2016-1Q2017; *511 Innovations Inc. v. HTC Am., Inc.*, No. 15-CV-1524 (E.D. Tex. Filed June 30, 2016) (retained by plaintiff – The Davis Firm). Deposition (x2)
  - a. Deposition: 2 (Cumulative total: 14)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 2)
  - d. Technology: Proximity sensors for mobile phones.
28. Active case work: 3Q2016-4Q2016; *MellanoX Techs. Ltd. v. Methode Elecs. Inc.*, No. 15-CV-3730 (N.D. Cal. filed Aug. 16, 2015) (retained by plaintiff – Alston & Bird).
  - a. Deposition: 0 (Cumulative total: 14)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 2)
  - d. Technology: Fiber optic transceiver modules.
29. Active case work: 4Q2016-1Q2017; *Novanta Inc., v. Iridation Inc.*, No. 15-CV-01033 (D. Del. filed Nov. 9, 2015) (retained by defendant – Barnes and Thornburg LLP).
  - a. Deposition: 0 (Cumulative total: 14)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 2)
  - d. Technology: High power gas laser design and operation.
30. Active case work: 1Q2017-1Q2017; *Optolum Inc., v Cree Inc.*, No. 16-CV-03828; (D. Az. filed Nov. 3, 2016) (retained by defendant – Jones Day).
  - a. Deposition: 0 (Cumulative total: 14)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 2)
  - d. Technology: LED packaging for illumination.
31. Active case work: 1Q2017-4Q2017; *Polygroup Macau Ltd (BVI), v Willis Electric Co., Ltd.*, 15-CV-00552 (W.D. NC. Filed: Apr 21<sup>st</sup> 2016), (retained by plaintiff - Troutman Sanders LLP). Deposition experience (x2)
  - a. Deposition: 2 (Cumulative total: 16)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 1 (Cumulative total: 3)
  - d. Technology: Electrical connector, IC, and LED light product design.
32. Active case work: 1Q2017-4Q2017; *Polygroup Macau Ltd (BVI), v Willis Electric Co., Ltd.*, IPR2017-00309 (PTAB filed Nov. 21<sup>st</sup> 2017), (retained by plaintiff - Troutman Sanders LLP).
  - a. Deposition: 0 (Cumulative total: 16)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Electrical connector, IC, and LED light product design.
33. Active case work: 1Q2017-4Q2017; *Polygroup Macau Ltd (BVI), v Willis Electric Co., Ltd.*, IPR2017-00330 (PTAB filed Nov. 24<sup>th</sup> 2017), (retained by plaintiff - Troutman Sanders LLP).
  - a. Deposition: 0 (Cumulative total: 16)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Electrical connector, IC, and LED light product design.
34. Active case work: 1Q2017-4Q2017; *Polygroup Macau Ltd (BVI), v Willis Electric Co., Ltd.*, IPR2017-00331 (PTAB filed Nov. 24<sup>th</sup> 2017), (retained by plaintiff - Troutman Sanders LLP).
  - a. Deposition: 0 (Cumulative total: 16)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Electrical connector, IC, and LED light product design.
35. Active case work: 1Q2017-4Q2017; *Polygroup Macau Ltd (BVI), v Willis Electric Co., Ltd.*, IPR2017-00332 (PTAB filed Nov. 25<sup>th</sup> 2017), (retained by plaintiff - Troutman Sanders LLP).
  - a. Deposition: 0 (Cumulative total: 16)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Electrical connector, IC, and LED light product design.
36. Active case work: 1Q2017-4Q2017; *Polygroup Macau Ltd (BVI), v Willis Electric Co., Ltd.*, IPR2017-00334 (PTAB filed Nov. 25<sup>th</sup> 2017), (retained by plaintiff - Troutman Sanders LLP).
  - a. Deposition: 0 (Cumulative total: 16)

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- b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Electrical connector, IC, and LED light product design.
37. Active case work: 1Q2017-4Q2017; *Polygroup Macau Ltd (BVI), v Willis Electric Co., Ltd.*, IPR2017-00335 (PTAB filed Nov. 25<sup>th</sup> 2017), (retained by plaintiff - Troutman Sanders LLP).
- a. Deposition: 0 (Cumulative total: 16)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Electrical connector, IC, and LED light product design.
38. Active case work: 1Q2017-4Q2017; *Macom Technology Solutions Holdings Inc., and Nitronex, LLC., v. Infineon Technologies AG and Infineon Technologies North American Corp.*, 16-CV-02859 (C.D. Ca. filed Apr 26, 2016) (retained by plaintiff – Baker Botts LLP).
- a. Deposition: 0 (Cumulative total: 16)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: High performance GaN based RF FET device design and operation.
39. Active case work: 1Q2017-1Q2017; *Quanergy Systems, Inc. v. Velodyne LiDAR, Inc.* (16-cv-05251; N.D. Ca. filed: Sep 13<sup>th</sup> 2016 (retained by plaintiff Velodyne) - Latham & Watkins LLP
- a. Deposition: 0 (Cumulative total: 16)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Laser/photodetector based LIDAR design and operation for self-driving vehicles.
40. Active case work: 1Q2017-2Q2017; *The Chamberlain Group Inc., v. Techtronic Industries Co., Ltd, Techtronic Industries North America et al.*, Challenge to U.S Patent No. 7,862,209 (retained by plaintiff – The Chamberlain Group) – Morgan, Lewis & Brockius, LLP.
- a. Deposition: 0 (Cumulative total: 16)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 5)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: LED based luminaire design for lighting.
41. Active case work: 1Q2017-1Q2018; *Uber Technologies Inc., Ottomotto LLC., Otto Trucking LLC., v. Waymo LLC (Google)*, 17-CV-00939 (N.D. Ca filed: Mar 10<sup>th</sup>, 2017), (retained by defendant Uber Technologies Inc.) – Morrison and Foerster LLP. Deposition experience (x3) and trial experience (case settled at trial).
- a. Deposition: 3 (Cumulative total: 19)
  - b. Trial/Hearing/Court appearance: 1 (Cumulative total: 6)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Optical and electrical device, optics, and package designs for LIDAR based self-driving vehicles.
42. Active case work: 2Q2017-2Q2017; *Heptagon v. ST Mircoelectronics* IPR petition; (retained by plaintiff Heptagon) – Proskauer Rose LLP).
- a. Deposition: 0 (Cumulative total: 19)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 6)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Optoelectronic based proximity sensors using LEDs and photodetectors.
43. Active case work: 2Q2017-2Q2018; *AT&T Inc., v. Sycamore Holdings LLC.*, 16-CV-00588 (E. D. Tx filed: Jun 6<sup>th</sup> 2016); (retained by defendant AT&T Inc.) - Kirkland and Ellis LLP. Deposition experience (x1)
- a. Deposition: 1 (Cumulative total: 20)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 6)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Coding designs of optical digital signals for high performance optical networks.
44. Active case work: 2Q2017 – 4Q2017; *Clearfield Inc., v. CommScope, ADC, Tyco, and TE Connectivity*, 17-CV-00307 (D.C. Minn. filed Jan 31<sup>st</sup> 2017); (retained by defendant Clearfield, Inc.) – Pepper Hamilton LLP
- a. Deposition: 0 (Cumulative total: 20)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 6)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Fiber optic connectors, panels, and distribution switches using optoelectronic components.
45. Active case work: 2Q2017 – 4Q2017; *Clearfield Inc., v. CommScope, ADC, Tyco, and TE Connectivity*, IPR2017-02122 (PTAB filed Sep. 15<sup>th</sup> 2017); (retained by defendant Clearfield, Inc.) – Pepper Hamilton LLP
- a. Deposition: 0 (Cumulative total: 20)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 6)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Fiber optic connectors, panels, and distribution switches using optoelectronic components.
46. Active case work: 2Q2017 – 4Q2017; *Clearfield Inc., v. CommScope, ADC, Tyco, and TE Connectivity*, IPR2018-00003 (PTAB filed Oct. 6<sup>th</sup> 2017); (retained by defendant Clearfield, Inc.) – Pepper Hamilton LLP
- a. Deposition: 0 (Cumulative total: 20)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 6)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Fiber optic connectors, panels, and distribution switches using optoelectronic components.



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47. Active case work: 2Q2017–4Q2017; *Clearfield Inc., v. CommScope, ADC, Tyco, and TE Connectivity*, IPR2018-00154 (PTAB filed Nov. 7<sup>th</sup> 2017); (retained by defendant Clearfield, Inc.) – Pepper Hamilton LLP
  - a. Deposition: 0 (Cumulative total: 20)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 6)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Fiber optic connectors, panels, and distribution switches using optoelectronic components.
48. Active case work: 4Q2016-2Q2017; *Antunes Inc.*, Pre-litigation IP patent review; Case No. TBD; (retained by plaintiff – Antunes Inc. and Chapman Spingola LLP).
  - a. Deposition: 0 (Cumulative total: 20)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 6)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: High power grating surface emitter laser diodes, and associated packaging and device design for laser-based cooking ovens.
49. Active case work: 1Q2017-2Q2017; *Core Optical Technologies LLC v. Fujitsu Network Communications, Inc.*, 16-CV-00437 (C. D. Ca filed: Mar 7<sup>th</sup> 2016); (retained by defendant Fujitsu Network Communications) – Morrison & Foerster LLP.
  - a. Deposition: 0 (Cumulative total: 20)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 6)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Fiber optic based optical communications for coherent technologies
50. Active case work: 3Q2017-4Q2018; *Oyster Optics LLC v. Coriant America, et al*, 16-CV-01302 (E. D. Tx filed: Nov 24<sup>th</sup> 2016); (retained by plaintiff Oyster Optics LLC) – Russ August & Kabat LLP.
  - a. Deposition: 1 (Cumulative total: 21)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 6)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Fiber optic based optoelectronic semiconductor component design and operation.
51. Active case work: 3Q2017-4Q2018; *Oyster Optics LLC v. Infinera, Alcatel-Lucent, Fujitsu, Cisco Systems, Huawei*, 16-CV-01295, 16-CV-01297, 16-CV-01299, 16-CV-01301, 16-CV-01303 (E. D. Tx filed: Nov 24<sup>th</sup> 2016); (retained by plaintiff Oyster Optics LLC) – Russ August & Kabat LLP. Deposition experience (x1).
  - a. Deposition: 1 (Cumulative total: 22)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 6)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Fiber optic based optoelectronic semiconductor component design and operation.
52. Active case work: 3Q2017-4Q2017; *Olympus*, Pre-litigation IP and Due Diligence; Case No. TBD; (retained by plaintiff – Olympus and Fish & Richardson P.C.)
  - a. Deposition: 0 (Cumulative total: 22)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 6)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: High volume, low cost optical lens and optics technology.
53. Active case work: 3Q2017-1Q2018; *Honeywell International, Inc et al v. Code Corporation et al.*, ITC No 337-TA-1061 (filed Jun 28<sup>th</sup> 2017), “Certain barcode readers, scan engines, products containing the same, and components thereof,” (retained by respondent – Honeywell and Alston and Bird LLP)
  - a. Deposition: 1 (Cumulative total: 23)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 6)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Bar-code scanners and associated optical/optoelectronic component performance and operation.
54. Active case work: 4Q2017-1Q2019; *Godo Kaisha IP Bridge 1 v. Intel Corp.*, 17-CV-00676 (filed Sep 29<sup>th</sup> 2017), (retained by plaintiff – Godo Kaisha IP Bridge 1) - Ropes and Gray, LLP.
  - a. Deposition: 0 (Cumulative total: 23)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 6)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Fabrication, design, and reverse engineering of silicon-based FET ICs.
55. Active case work: 4Q2017-3Q2018; *Maxim Integrated Products, Inc. and Volterra Semiconductor LLC., v. Silicon Mitus Inc., and Silicon Mitus Technology Inc.*, 17-CV-03507 (N. D. Ca: filed Jun 16<sup>th</sup> 2017), (retained by defendant Silicon Mitus) – Pillsbury Winthrop Shaw Pittman, LLP. (Deposition and trial experience X1)
  - a. Deposition: 1 (Cumulative total: 24)
  - b. Trial/Hearing/Court appearance: 1 (Cumulative total: 7)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Fabrication, design, characterization, and packaging of silicon-based FET ICs for power applications
56. Active case work: 2Q2018-3Q2018; *Cree, Inc., v. Document Security Systems Inc.*, 17-CV-4263 (C.D. Ca filed: Apr 17<sup>th</sup> 2017), (retained by defendant Cree Inc.) - Jones Day, LLP
  - a. Deposition: 0 (Cumulative total: 24)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 7)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Design and packaging of high brightness GaN based LEDs

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57. Active case work: 2Q2018-2Q2018; *Weisen v., Ram Telecom International (RTI),* CGC-16-554331 (Sup. Ca. filed 3<sup>rd</sup> May 2017) (retained by plaintiff *Weisen, J*) - *Yetter Coleman, LLP*. Deposition experience (x1) and trial experience (x1).
  - a. Deposition: 1 (Cumulative total: 25)
  - b. Trial/Hearing/Court appearance: 1 (Cumulative total: 8)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Submarine and subsea fiber optic cables: technology, markets, economic impact, and history.
58. Active case work: 2Q2018-3Q2018; *Seoul Semiconductor, v. Document Security Systems Inc.,* 17-CV-00981 (C.D. Ca. filed: Apr 17<sup>th</sup> 2017), (retained by defendant *Seoul Semiconductor*) - *Latham and Watkins LLP*
  - a. Deposition: 1 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 8)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: Design and packaging of high brightness GaN based LEDs
59. Active case work: 3Q2018-4Q2018; *NEC Display Solutions Inc., and NEC Display Solutions of America, Inc., v. Ultravision, ITC Case# 337-TA-1114* (filed 24<sup>th</sup> May 2018), "Certain Modular LED Display Panels and Components Thereof," (retained by respondent *Jones Day, LLP*)
  - a. Deposition: 0 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 8)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
60. Active case work: 3Q2018-3Q2018; *IFT (Innovative Foundry Technologies)* (pre-lit), retained by plaintiff *Mintz Levin, Cohen, Ferris, Glovsky, and Popeo PC.*
  - a. Deposition: 0 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 8)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 3)
  - d. Technology: CMOS device (inc FinFETs) and IC fabrication techniques at 40, 28, 20, 16nm nodes.
61. Active case work: 4Q2018-2Q2019; *Eidolon Optical LLC, v. Haag-Streit AG.,* IPR2018-01311, (retained by patent owner *Eidolon Optical LLC*) - *McInnes & McLane LLP*
  - a. Deposition: 0 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 8)
  - c. IPR/PTAB trial/deposition: 1 (Cumulative total: 4)
  - d. Technology: High brightness InGaAlP, GaP, AlGaAs, and GaN/InGaN based LEDs for use in medical instruments
62. Active case work: 3Q2018-3Q2018; *Voxtel Inc., v. Joseph Lachapelle & Luminar Technologies Inc.,* 18-CV-27356 (D. Or. filed: Dec 18<sup>th</sup> 2017), (retained by plaintiff *Voxtel Inc.*) - *Ater Wynne LLP*
  - a. Deposition: 0 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 8)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: LIDAR optical and electronic component and system technology
63. Active case work: 3Q2018-1Q2019; *Alta Devices, v. LG Electronics Inc.,* 18-CV-00404 (N.D. Ca. filed: May 7<sup>th</sup> 2018), (retained by defendant *LG Electronics Inc.*) - *Hogan Lovells LLP*
  - a. Deposition: 0 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 8)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: Trade Secret GaAs based solar cell design, fabrication, manufacturing, and device performance
64. Active case work: 3Q2018-3Q18; *Opterna AM Inc., v. Commscope Technologies Inc.,* Pre-litigation preparation, (retained by defendant *Opterna AM Inc.*) - *Sterne Kessler LLP*
  - a. Deposition: 0 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 8)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: Fiber optic connectors, panels, and distribution switches using optoelectronic components.
65. Active case work: 4Q2018 – 1Q2019; *U.D. Electronic Corp., v. Pulse Electronics, Inc.,* Preparation for IPR filing: IPR2019-00508 (PTAB filed Dec 26<sup>th</sup> 2018); and support for 18-CV-00373 (S.D. Ca. filed: Feb 16<sup>th</sup> 2018) (retained by petitioner *U. D. Electronic Corp.*) – *Procopio, Cory, Hargreaves and Savitch LLP*
  - a. Deposition: 0 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 8)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: Electrical and fiber optic connectors, panels, and distribution switches using both electronic and optoelectronic components.
66. Active case work: 4Q2018 – 1Q2019; *U.D. Electronic Corp., v. Pulse Electronics, Inc.,* Preparation for IPR filing: IPR2019-00515 (PTAB filed Dec 31<sup>st</sup> 2018); and support for 18-CV-00373 (S.D. Ca. filed: Feb 16<sup>th</sup> 2018) (retained by petitioner *U. D. Electronic Corp.*) – *Procopio, Cory, Hargreaves and Savitch LLP*
  - a. Deposition: 0 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 8)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: Electrical and fiber optic connectors, panels, and distribution switches using both electronic and optoelectronic components.

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67. Active case work: 4Q2018 – 1Q2019; *U.D. Electronic Corp., v. Pulse Electronics, Inc.*, Preparation for IPR filing: IPR2019-00262 (PTAB filed Nov 9<sup>th</sup> 2018); and support for 18-CV-00373 (S.D. Ca. filed: Feb 16<sup>th</sup> 2018) (retained by petitioner U. D. Electronic Corp.) – Procopio, Cory, Hargreaves and Savitch LLP
  - a. Deposition: 0 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 8)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: Electrical and fiber optic connectors, panels, and distribution switches using both electronic and optoelectronic components.
68. Active case work: 4Q2018 – 1Q2019; *U.D. Electronic Corp., v. Pulse Electronics, Inc.*, Preparation for IPR filing: IPR2019-00511 (PTAB filed Dec 28<sup>th</sup> 2018); and support for 18-CV-00373 (S.D. Ca. filed: Feb 16<sup>th</sup> 2018) (retained by petitioner U. D. Electronic Corp.) – Procopio, Cory, Hargreaves and Savitch LLP
  - a. Deposition: 0 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 8)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: Electrical and fiber optic connectors, panels, and distribution switches using both electronic and optoelectronic components.
69. Active case work: 4Q2018 – 1Q2019; *Semiconductor Energy Laboratory Co. Ltd., v. Bluehouse Global Ltd.*, Preparation for IPR filing: IPR2018-01405 (PTAB filed Jul 18<sup>th</sup> 2018); (retained by patent owner SEL Co Ltd.) – Robinson Intellectual Law Office, P.C. (Counsel represented by Fish and Richardson LLP).
  - a. Deposition: 0 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 8)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: Semiconductor displays using active matrix LCD and thin film transistor technology. Design, fabrication, and circuit layout.
70. Active case work: 4Q2018 – 1Q2019; *Semiconductor Energy Laboratory Co. Ltd., v. Bluehouse Global Ltd.*, Preparation for IPR filing: IPR2018-01393 (PTAB filed Jul 13<sup>th</sup> 2018); (retained by patent owner SEL Co Ltd.) – Robinson Intellectual Law Office, P.C. (Counsel represented by Fish and Richardson LLP)
  - a. Deposition: 0 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 8)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: Semiconductor displays using active matrix LCD and thin film transistor technology. Design and fabrication technology.
71. Active case work: 4Q2018 - 1Q2019; *The Sloan Company dba SloanLED, v. Principle Lighting Group, LLC.*, 18-CV-06449 (C.D. Ca. filed: Jul 26<sup>th</sup> 2018), (retained by defendant SloanLED.) - Ferguson Case Orr Paterson LLP
  - a. Deposition: 0 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 9)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: LED lighting, LED luminaires, LED performance, electrical and mechanical design and construction.
72. Active case work: 1Q2019 - 1Q2019; *HTC Corporation, v. Lemire Illumination Technologies.*, 18-CV-00021 (E.D. Tx. filed: Jan 21<sup>st</sup> 2018), (retained by defendant HTC Corporation) - Perkins Coie LLP
  - a. Deposition: 0 (Cumulative total: 26)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 9)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: LEDs for mobile phones
73. Active case work: 1Q2019 - 2Q2019; *Frys Electronics, v. Seoul Semiconductor Co, and Seoul Viosys Co.,* 2:18-CV-00386-JRG (E. D. Tx. filed: Nov 20<sup>th</sup> 2018), (retained by defendant Frys Electronics) - Lamkin IP Defense
  - a. Deposition: 0 (Cumulative total: 26),
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 9)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: LED chips, LED packaging, LED lenses, LED luminaires, backlights, displays, and televisions/monitors
74. Active case work: 2Q2019 – 4Q2019; *Hanwha Q CELLS & Advance Materials Corporation, v. JinkoSolar, LONGi Solar, REC Solar*, ITC 337-TA-1151 (filed: Apr 4<sup>th</sup> 2019), (“Certain Photovoltaic Cells and Products Containing Same,”), retained by patent owner and plaintiff Hanwha Q CELLS) - Covington and Burling LLP
  - a. Deposition: 2 (Cumulative total: 28)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 9)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
75. Active case work: 2Q2019-3Q2019; *Hanwha Q CELLS & Advance Materials Corporation, v. JinkoSolar and affiliates*, 19-CV-00450 (D. Del. filed: Jan 21<sup>st</sup> 2018), (retained by patent owner and plaintiff Hanwha Q CELLS) - Covington and Burling LLP
  - a. Deposition: 0 (Cumulative total: 28)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 9)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: Silicon solar cells and materials analysis of passivation layers
76. Active case work: 2Q2019-2Q2019; *Oyster Optics LLC v. Infinera Inc.*, 2:18-CV-00206 (E. D. Tx filed: May 15<sup>th</sup> 2018); (retained by plaintiff Oyster Optics LLC) – Russ August & Kabat LLP.
  - a. Deposition: 0 (Cumulative total: 28)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 9)

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- c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: Fiber optic based optoelectronic semiconductor component design and operation.
- 77. Active case work: 2Q2019 – 2Q2019; *Nichia Corporation & Osram Opto Semiconductors Inc., v. Lighting Science Group Corp.*, IPR filing: IPR2019-01259 (PTAB filed Jun 28<sup>th</sup> 2019); (retained by petitioner Nichia and Osram Opto.) – Shearman and Sterling, LLP
  - a. Deposition: 0 (Cumulative total: 28)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 9)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: LED chips, LED packaging and ceramic thermal heat sinking technology.
- 78. Active case work: 2Q2019 – 3Q2019; *Nichia Corporation v. Lighting Science Group Corp.*, 2:17-CV-08849 (C. D. Ca filed Jul 12<sup>th</sup> 2017); (retained by defendant Nichia) – Shearman and Sterling, LLP
  - a. Deposition: 0 (Cumulative total: 28)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 9)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: LED chips, LED packaging and ceramic thermal heat sinking technology
- 79. Active case work: 3Q2019-3Q2019; *Applied Optoelectronics Inc v. Class Action Lawsuit*, 4:17-CV-02399 (S. D. Tx filed: Mar 6<sup>th</sup> 2018); (retained by plaintiff Class Action Lawsuit) – Levi and Korsinsky, LLP
  - a. Deposition: 0 (Cumulative total: 28)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 9)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: Fiber optic based optoelectronic semiconductor components, transceivers, and sub-systems.
- 80. Active case work: 3Q2019-3Q2019; *DNA Motor v. Kuen Hwa Traffic Industrial Co.*, 18-CV-05664 (C. D. Ca filed: Jan 15<sup>th</sup> 2019); (defendant DNA Motor) – Elizabeth Yang, Law and Mediation Office
  - a. Deposition: 0 (Cumulative total: 28)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 9)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: LED design patent, and the design of an aftermarket LED based headlight assembly for an automobile.
- 81. Active case work: 3Q2019 – 1Q2020; *Nichia Corporation, Osram Opto Semiconductors Inc., Philips Lumileds, GE Consumer Lighting, Cree, and Signify v. Lighting Science Group Corp.*, ITC 337-TA-1168 (filed: Apr 30<sup>th</sup> 2019), (“Certain Light-Emitting-Diode products, systems, and components thereof (III)”) (retained by respondents Nichia, Osram Optoelectronics, Philips Lumileds, GE Consumer Lighting, Cree Hong Kong., Signify Corp.) – Shearman and Sterling, LLP
  - a. Deposition: 1 (Cumulative total: 29)
  - b. Trial/Hearing/Court appearance: 1 (Cumulative total: 10)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: LED chips, LED packaging and ceramic thermal heat sinking technology (LTCC).
- 82. Active case work: 4Q2019 – 1Q2020; *Amazon.com Inc., Bed, Bath and Beyond, IKEA, Target, and Walmart Inc., v. Regents of the University of California*, ITC 337-TA-1172 (filed: July 30<sup>th</sup> 2019), (“Certain Filament Light-Emitting-Diodes and products containing same”) (retained by respondents Amazon.com Inc., Bed, Bath and Beyond, IKEA, Target, and Walmart Inc.) – Morrison and Foerster, LLP
  - a. Deposition: 2 (Cumulative total: 31)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 10)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: LED chips, LED packaging and light bulb filaments with transparent sub-mounts.
- 83. Active case work: 4Q2019 – 4Q2019; *U.D. Electronic Corp., v. Pulse Electronics, Inc.*, IPR2019-00511 (PTAB filed Dec 28<sup>th</sup> 2018), (retained by petitioner U. D. Electronic Corp.) – Procopio, Cory, Hargreaves and Savitch LLP
  - a. Deposition: 0 (Cumulative total: 31)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 10)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: Electrical and fiber optic connectors, panels, and distribution switches using both electronic and optoelectronic components.
- 84. Active case work: 1Q2020 – present; *IKEA, v. Regents of the University of California*, ITC 337-TA-1172 (filed: July 30<sup>th</sup> 2019), (“Certain Filament Light-Emitting-Diodes and products containing same”) (retained by respondents IKEA) – Flaster and Greenberg, LLP
  - a. Deposition: 2 (Cumulative total: 31)
  - b. Trial/Hearing/Court appearance: 0 (Cumulative total: 10)
  - c. IPR/PTAB trial/deposition: 0 (Cumulative total: 4)
  - d. Technology: LED chips, LED packaging and light bulb filaments with transparent sub-mounts.

**PUBLISHED PATENT APPLICATIONS:**

As per USPTO website patent applications that have been published in 2019 that are not covered by the list below:

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PUB. APP. NO.	Title
1	<a href="#"><u>20190353843 FABRICATION PROCESS OF POLYMER BASED PHOTONIC APPARATUS AND THE APPARTUS</u></a>
2	<a href="#"><u>20190305039 EPITAXIAL AlN/cREO STRUCTURE FOR RF FILTER APPLICATIONS</u></a>
3	<a href="#"><u>20190278036 EMBEDDED HERMETIC CAPSULE AND METHOD</u></a>

As per USPTO website patent applications that have been published:




PUB. APP. NO.	Title
1	<a href="#"><u>20190237930 HERMETIC CAPSULE AND METHOD</u></a>
2	<a href="#"><u>20190227233 RE-based Integrated Photonic and Electronic Layered Structures</u></a>
3	<a href="#"><u>20190221993 POROUS DISTRIBUTED BRAGG REFLECTORS FOR LASER APPLICATIONS</u></a>
4	<a href="#"><u>20190204506 PROTECTION LAYERS FOR POLYMER MODULATORS/WAVEGUIDES</u></a>
5	<a href="#"><u>20190172923 Integrated Epitaxial Metal Electrodes</u></a>
6	<a href="#"><u>20190148913 GUIDE TRANSITION DEVICE WITH DIGITAL GRATING DEFLECTORS AND METHOD</u></a>
7	<a href="#"><u>20190139761 Pnictide Buffer Structures and Devices for GaN Base Applications</u></a>
8	<a href="#"><u>20190122885 GROUP III SEMICONDUCTOR EPITAXY FORMED ON SILICON VIA SINGLE CRYSTAL REN AND REO BUFFER LAYERS</u></a>
9	<a href="#"><u>20190079243 GUIDE TRANSITION DEVICE AND METHOD</u></a>
10	<a href="#"><u>20190074365 Integrated Epitaxial Metal Electrodes</u></a>
11	<a href="#"><u>20190064436 POLYMER MODULATOR AND LASER INTEGRATED ON A COMMON PLATFORM AND METHOD</u></a>
12	<a href="#"><u>20190028081 LAYER STRUCTURES FOR RF FILTERS FABRICATED USING RARE EARTH OXIDES AND EPITAXIAL ALUMINUM NITRIDE</u></a>
13	<a href="#"><u>20180259798 DIRECT-DRIVE POLYMER MODULATOR METHODS OF FABRICATING AND MATERIALS THEREFOR</u></a>
14	<a href="#"><u>20180138284 Integrated Epitaxial Metal Electrodes</u></a>
15	<a href="#"><u>20180013053 Josephson Junction using Molecular Beam Epitaxy</u></a>
16	<a href="#"><u>20180012858 RARE EARTH INTERLAYS FOR MECHANICALLY LAYERING DISSIMILAR SEMICONDUCTOR WAFERS</u></a>
17	<a href="#"><u>20170353002 Rare Earth Pnictides for Strain Management</u></a>
18	<a href="#"><u>20170141750 LAYER STRUCTURES FOR RF FILTERS FABRICATED USING RARE EARTH OXIDES AND EPITAXIAL ALUMINUM NITRIDE</u></a>
19	<a href="#"><u>20160133708 STRAIN COMPENSATED REO BUFFER FOR III-N ON SILICON</u></a>
20	<a href="#"><u>20150014676 III-N MATERIAL GROWN ON REN EPITAXIAL BUFFER ON Si SUBSTRATE</u></a>
21	<a href="#"><u>20140357014 HIGH EFFICIENCY SOLAR CELL USING IIIB MATERIAL TRANSITION LAYERS</u></a>
22	<a href="#"><u>20140239307 REO GATE DIELECTRIC FOR III-N DEVICE ON Si SUBSTRATE</u></a>
23	<a href="#"><u>20140231818 AlN CAP GROWN ON GaN/REO/SILICON SUBSTRATE STRUCTURE</u></a>
24	<a href="#"><u>20140231817 III-N MATERIAL GROWN ON ALO/ALN BUFFER ON SI SUBSTRATE</u></a>
25	<a href="#"><u>20140225123 REO/ALO/AlN TEMPLATE FOR III-N MATERIAL GROWTH ON SILICON</u></a>
26	<a href="#"><u>20140167057 REO/ALO/AlN TEMPLATE FOR III-N MATERIAL GROWTH ON SILICON</u></a>
27	<a href="#"><u>20140077339 DELTA DOPING AT Si-Ge INTERFACE</u></a>
28	<a href="#"><u>20140077338 Si-Ge-Sn ON REO TEMPLATE</u></a>
29	<a href="#"><u>20140077240 IV MATERIAL PHOTONIC DEVICE ON DBR</u></a>
30	<a href="#"><u>20140076390 III-V SEMICONDUCTOR INTERFACE WITH GRADED GeSn ON SILICON</u></a>
31	<a href="#"><u>20140053894 GRADED GeSn ON SILICON</u></a>

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32	<a href="#">20140008644</a>	<a href="#">OXYGEN ENGINEERED SINGLE-CRYSTAL REO TEMPLATE</a>
33	<a href="#">20130334536</a>	<a href="#">SINGLE-CRYSTAL REO BUFFER ON AMORPHOUS SiO<sub>x</sub></a>
34	<a href="#">20130248853</a>	<a href="#">NUCLEATION OF III-N ON REO TEMPLATES</a>
35	<a href="#">20130214282</a>	<a href="#">III-N ON SILICON USING NANO STRUCTURED INTERFACE LAYER</a>
36	<a href="#">20130153918</a>	<a href="#">REO-Si TEMPLATE WITH INTEGRATED REO LAYERS FOR LIGHT EMISSION</a>
37	<a href="#">20130099357</a>	<a href="#">STRAIN COMPENSATED REO BUFFER FOR III-N ON SILICON</a>
38	<a href="#">20130071960</a>	<a href="#">INTEGRATED RARE EARTH DEVICES</a>
39	<a href="#">20130062610</a>	<a href="#">LATTICE MATCHED CRYSTALLINE REFLECTOR</a>
40	<a href="#">20130062609</a>	<a href="#">III-N FET ON SILICON USING FIELD SUPPRESSING REO</a>
41	<a href="#">20130032858</a>	<a href="#">RARE EARTH OXY-NITRIDE BUFFERED III-N ON SILICON</a>
42	<a href="#">20120280276</a>	<a href="#">Single Crystal Ge On Si</a>
43	<a href="#">20120256232</a>	<a href="#">Multilayer Rare Earth Device</a>
44	<a href="#">20120183767</a>	<a href="#">HEXAGONAL REO TEMPLATE BUFFER FOR III-N LAYERS ON SILICON</a>
45	<a href="#">20120147906</a>	<a href="#">LASER COOLING OF MODIFIED SOI WAFER</a>
46	<a href="#">20120145243</a>	<a href="#">SOLAR CELLS WITH MAGNETICALLY ENHANCED UP-CONVERSION</a>
47	<a href="#">20120104567</a>	<a href="#">III<sub>x</sub>O<sub>y</sub>N<sub>y</sub> ON REO/Si</a>
48	<a href="#">20120104443</a>	<a href="#">III<sub>x</sub>O<sub>y</sub>N<sub>y</sub> ON SINGLE CRYSTAL SOI SUBSTRATE AND III n GROWTH PLATFORM</a>
49	<a href="#">20120090672</a>	<a href="#">REO-Ge Multi-Junction Solar Cell</a>
50	<a href="#">20120085399</a>	<a href="#">REO-Ge Multi-Junction Solar Cell</a>
51	<a href="#">20120073648</a>	<a href="#">Photovoltaic conversion using rare earths plus Group IV Sensitizers</a>
52	<a href="#">20120019902</a>	<a href="#">INTERGRATED PUMP LASER AND RARE EARTH WAVEGUIDE AMPLIFIER</a>
53	<a href="#">20110290313</a>	<a href="#">SOLAR CELLS WITH ENGINEERED SPECTRAL CONVERSION</a>
54	<a href="#">20110220173</a>	<a href="#">ACTIVE SOLAR CONCENTRATOR WITH MULTI-JUNCTION DEVICES</a>
55	<a href="#">20110203666</a>	<a href="#">HIGH EFFICIENCY SOLAR CELL USING IIIB MATERIAL TRANSITION LAYERS</a>
56	<a href="#">20110188533</a>	<a href="#">INTEGRATED RARE EARTH DEVICES</a>
57	<a href="#">20110108908</a>	<a href="#">MULTILAYERED BOX IN FDSOI MOSFETS</a>
58	<a href="#">20100122720</a>	<a href="#">Passive Rare Earth Tandem Solar Cell</a>
59	<a href="#">20100116315</a>	<a href="#">Active rare earth tandem solar cell</a>
60	<a href="#">20100112736</a>	<a href="#">FULL COLOR DISPLAY</a>
61	<a href="#">20100109047</a>	<a href="#">Multijunction rare earth solar cell</a>
62	<a href="#">20100084680</a>	<a href="#">SPONTANEOUS/STIMULATED LIGHT EMITTING .mu.-CAVITY DEVICE</a>
63	<a href="#">20090291535</a>	<a href="#">STACKED TRANSISTORS AND PROCESS</a>
64	<a href="#">20080135924</a>	<a href="#">Multilayered box in FDSOI MOSFETS</a>
65	<a href="#">20080093670</a>	<a href="#">SIGNAL AND/OR GROUND PLANES WITH DOUBLE BURIED INSULATOR LAYERS AND FABRICATION PROCESS</a>
66	<a href="#">20070018203</a>	<a href="#">Strain inducing multi-layer cap</a>
67	<a href="#">20070018166</a>	<a href="#">Stacked transistors and process</a>
68	<a href="#">20060246691</a>	<a href="#">Signal and/or ground planes with double buried insulator layers and fabrication process</a>

**PATENTS ISSUED:**

As per the USPTO website the following are recent utility patents issued in 2019 that are not covered by the full list following:

PAT. NO.	Title
1 <a href="#">10.527.786</a>	 <a href="#">Polymer modulator and laser integrated on a common platform and method</a>
2 <a href="#">10.520.673</a>	 <a href="#">Protection layers for polymer modulators/waveguides</a>
3 <a href="#">10.511.146</a>	 <a href="#">Guide transition device with digital grating deflectors and method</a>

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- 4 [10,509,164](#)  [Guide transition device and method](#)  
5 [10,431,729](#)  [Josephson junction using molecular beam epitaxy](#)

As per the USPTO website the following are utility patents issued in USA:

PAT. NO.	Titl e
1	<a href="#">10,332,857</a>  <a href="#">Rare earth pnictides for strain management</a>
2	<a href="#">10,162,111</a>  <a href="#">Multi-fiber/port hermetic capsule sealed by metallization and method</a>
3	<a href="#">10,128,350</a>  <a href="#">Integrated epitaxial metal electrodes</a>
4	<a href="#">10,075,143</a>  <a href="#">Layer structures for RF filters fabricated using rare earth oxides and epitaxial aluminum nitride</a>
5	<a href="#">9,496,132</a>  <a href="#">Nucleation of III-N on REO templates</a>
6	<a href="#">9,443,939</a>  <a href="#">Strain compensated REO buffer for III-N on silicon</a>
7	<a href="#">9,236,249</a>  <a href="#">III-N material grown on REN epitaxial buffer on Si substrate</a>
8	<a href="#">9,105,471</a>  <a href="#">Rare earth oxy-nitride buffered III-N on silicon</a>
9	<a href="#">8,889,978</a>  <a href="#">III-V semiconductor interface with graded GeSn on silicon</a>
10	<a href="#">8,878,188</a>  <a href="#">REO gate dielectric for III-N device on Si substrate</a>
11	<a href="#">8,872,308</a>  <a href="#">AlN cap grown on GaN/REO/silicon substrate structure</a>
12	<a href="#">8,835,955</a>  <a href="#">III<sub>0.sub.x</sub>N<sub>1.sub.y</sub> on single crystal SOI substrate and III<sub>n</sub> growth platform</a>
13	<a href="#">8,823,055</a>  <a href="#">REO/ALO/AlN template for III-N material growth on silicon</a>
14	<a href="#">8,823,025</a>  <a href="#">III-N material grown on AlO/AlN buffer on Si substrate</a>
15	<a href="#">8,794,010</a>  <a href="#">Laser cooling of modified SOI wafer</a>
16	<a href="#">8,748,900</a>  <a href="#">Re-silicide gate electrode for III-N device on Si substrate</a>
17	<a href="#">8,680,507</a>  <a href="#">AlN inter-layers in III-N material grown on DBR/silicon substrate</a>
18	<a href="#">8,637,763</a>  <a href="#">Solar cells with engineered spectral conversion</a>
19	<a href="#">8,636,844</a>  <a href="#">Oxygen engineered single-crystal REO template</a>
20	<a href="#">8,633,569</a>  <a href="#">AlN inter-layers in III-N material grown on REO/silicon substrate</a>
21	<a href="#">8,623,747</a>  <a href="#">Silicon, aluminum oxide, aluminum nitride template for optoelectronic and power devices</a>
22	<a href="#">8,559,097</a>  <a href="#">Integrated pump laser and rare earth waveguide amplifier</a>
23	<a href="#">8,553,741</a>  <a href="#">Integrated rare earth devices</a>
24	<a href="#">8,542,437</a>  <a href="#">Earth abundant photonic structures</a>
25	<a href="#">8,501,635</a>  <a href="#">Modification of REO by subsequent III-N EPI process</a>
26	<a href="#">8,455,756</a>  <a href="#">High efficiency solar cell using IIIB material transition layers</a>
27	<a href="#">8,394,194</a>  <a href="#">Single crystal reo buffer on amorphous SiO<sub>2.sub.x</sub></a>
28	<a href="#">8,331,413</a>  <a href="#">Integrated rare earth devices</a>
29	<a href="#">8,331,410</a>  <a href="#">Spontaneous/stimulated light emitting .mu.-cavity device</a>
30	<a href="#">8,049,100</a>  <a href="#">Multijunction rare earth solar cell</a>
31	<a href="#">8,039,738</a>  <a href="#">Active rare earth tandem solar cell</a>
32	<a href="#">8,039,737</a>  <a href="#">Passive rare earth tandem solar cell</a>
33	<a href="#">7,968,384</a>  <a href="#">Stacked transistors and process</a>
34	<a href="#">7,967,653</a>  <a href="#">Full color display</a>
35	<a href="#">7,821,066</a>  <a href="#">Multilayered BOX in FDSOI MOSFETS</a>

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36	<a href="#">7.643.526</a>		<a href="#">Spontaneous/stimulated light emitting .mu.-cavity device</a>
37	<a href="#">7.605.531</a>		<a href="#">Full color display including LEDs with rare earth active areas and different radiative transistions</a>
38	<a href="#">7.579.623</a>		<a href="#">Stacked transistors and process</a>
39	<a href="#">7.538.016</a>		<a href="#">Signal and/or ground planes with double buried insulator layers and fabrication process</a>
40	<a href="#">7.388.230</a>		<a href="#">Selective colored light emitting diode</a>
41	<a href="#">7.365.357</a>		<a href="#">Strain inducing multi-layer cap</a>
42	<a href="#">7.355.269</a>		<a href="#">IC on non-semiconductor substrate</a>
43	<a href="#">7.323.396</a>		<a href="#">Signal and/or ground planes with double buried insulator layers and fabrication process</a>
44	<a href="#">6.999.644</a>		<a href="#">Discrete optoelectric package</a>
45	<a href="#">6.966.703</a>		<a href="#">Self eject latch mechanism for an optical transceiver module</a>
46	<a href="#">6.795.461</a>		<a href="#">Optoelectric module</a>
47	<a href="#">6.663.296</a>		<a href="#">Optoelectric module</a>
48	<a href="#">6.412.989</a>		<a href="#">Directable laser transmission module</a>
49	<a href="#">6.243.056</a>		<a href="#">Transceiver with miniature virtual image display</a>
50	<a href="#">6.228.440</a>		<a href="#">Perishable media information storage mechanism and method of fabrication</a>
51	<a href="#">6.161.106</a>		<a href="#">Perishable media system and method of operation</a>
52	<a href="#">6.158.884</a>		<a href="#">Integrated communicative watch</a>
53	<a href="#">6.156.582</a>		<a href="#">Method of fabricating top emitting ridge VCSEL with self-aligned contact and sidewall reflector</a>
54	<a href="#">6.131.017</a>		<a href="#">Dual system portable electronic communicator</a>
55	<a href="#">6.122.023</a>		<a href="#">Non-speckle liquid crystal projection display</a>
56	<a href="#">6.121.068</a>		<a href="#">Long wavelength light emitting vertical cavity surface emitting laser and method of fabrication</a>
57	<a href="#">6.115.618</a>		<a href="#">Portable electronic device with removable display</a>
58	<a href="#">6.111.839</a>		<a href="#">Optical pickup head including a coherent first order mode laser light source</a>
59	<a href="#">6.097.748</a>		<a href="#">Vertical cavity surface emitting laser semiconductor chip with integrated drivers and photodetectors and method of fabrication</a>
60	<a href="#">6.097.528</a>		<a href="#">Microscanner for portable laser diode displays</a>
61	<a href="#">6.096.666</a>		<a href="#">Holographic textile fiber</a>
62	<a href="#">6.091.754</a>		<a href="#">VCSEL having integrated photodetector for automatic power control</a>
63	<a href="#">6.084.697</a>		<a href="#">Integrated electro-optical package</a>
64	<a href="#">6.080.690</a>		<a href="#">Textile fabric with integrated sensing device and clothing fabricated thereof</a>
65	<a href="#">6.069.593</a>		<a href="#">Display carrier and electronic display control for multiple displays in a portable electronic device</a>
66	<a href="#">6.064.780</a>		<a href="#">Interconnect substrate with a single contact accessible in an upper and an end surface</a>
67	<a href="#">6.061.485</a>		<a href="#">Method for wavelength division multiplexing utilizing donut mode vertical cavity surface emitting lasers</a>
68	<a href="#">6.061.380</a>		<a href="#">Vertical cavity surface emitting laser with doped active region and method of fabrication</a>
69	<a href="#">6.029.073</a>		<a href="#">Display carrier with binocular viewing for a portable electronic device</a>
70	<a href="#">6.026.111</a>		<a href="#">Vertical cavity surface emitting laser device having an extended cavity</a>
71	<a href="#">6.022.760</a>		<a href="#">Integrated electro-optical package and method of fabrication</a>
72	<a href="#">6.021.147</a>		<a href="#">Vertical cavity surface emitting laser for high power single mode operation and method of fabrication</a>
73	<a href="#">6.021.146</a>		<a href="#">Vertical cavity surface emitting laser for high power single mode operation and method of fabrication</a>



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74	<a href="#">6.008.067</a>		<a href="#">Fabrication of visible wavelength vertical cavity surface emitting laser</a>
75	<a href="#">5.978.398</a>		<a href="#">Long wavelength vertical cavity surface emitting laser</a>
76	<a href="#">5.974.071</a>		<a href="#">VCSEL with integrated photodetectors for automatic power control and signal detection in data storage</a>
77	<a href="#">5.966.399</a>		<a href="#">Vertical cavity surface emitting laser with integrated diffractive lens and method of fabrication</a>
78	<a href="#">5.959.315</a>		<a href="#">Semiconductor to optical link</a>
79	<a href="#">5.956.364</a>		<a href="#">Vertical cavity surface emitting laser with shaped cavity mirror and method of fabrication</a>
80	<a href="#">5.956.363</a>		<a href="#">Long wavelength vertical cavity surface emitting laser with oxidation layers and method of fabrication</a>
81	<a href="#">5.953.355</a>		<a href="#">Semiconductor laser package with power monitoring system</a>
82	<a href="#">5.946.121</a>		<a href="#">IrDA data link with VCSEL light source</a>
83	<a href="#">5.943.359</a>		<a href="#">Long wavelength VCSEL</a>
84	<a href="#">5.943.357</a>		<a href="#">Long wavelength vertical cavity surface emitting laser with photodetector for automatic power control and method of fabrication</a>
85	<a href="#">5.939.773</a>		<a href="#">Semiconductor laser package including a lead frame and plastic resin housing</a>
86	<a href="#">5.936.929</a>		<a href="#">Optical submodule and method for making</a>
87	<a href="#">5.923.696</a>		<a href="#">Visible light emitting vertical cavity surface emitting laser with gallium phosphide contact layer and method of fabrication</a>
88	<a href="#">5.914.973</a>		<a href="#">Vertical cavity surface emitting laser for high power operation and method of fabrication</a>
89	<a href="#">5.906.004</a>		<a href="#">Textile fabric with integrated electrically conductive fibers and clothing fabricated thereof</a>
90	<a href="#">5.905.750</a>		<a href="#">Semiconductor laser package and method of fabrication</a>
91	<a href="#">5.903.586</a>		<a href="#">Long wavelength vertical cavity surface emitting laser</a>
92	<a href="#">5.898.722</a>		<a href="#">Dual wavelength monolithically integrated vertical cavity surface emitting lasers and method of fabrication</a>
93	<a href="#">5.886.972</a>		<a href="#">Recording information in a phase change optical medium with a vertical cavity surface emitting laser</a>
94	<a href="#">5.883.912</a>		<a href="#">Long wavelength VCSEL</a>
95	<a href="#">5.881.084</a>		<a href="#">Semiconductor laser for package with power monitoring system</a>
96	<a href="#">5.848.086</a>		<a href="#">Electrically confined VCSEL</a>
97	<a href="#">5.838.707</a>		<a href="#">Ultraviolet/visible light emitting vertical cavity surface emitting laser and method of fabrication</a>
98	<a href="#">5.838.703</a>		<a href="#">Semiconductor laser package with power monitoring system and optical element</a>
99	<a href="#">5.835.521</a>		<a href="#">Long wavelength light emitting vertical cavity surface emitting laser and method of fabrication</a>
100	<a href="#">5.831.960</a>		<a href="#">Integrated vertical cavity surface emitting laser pair for high density data storage and method of fabrication</a>
101	<a href="#">5.821.571</a>		<a href="#">Dual sided integrated electro-optical package</a>
102	<a href="#">5.818.404</a>		<a href="#">Integrated electro-optical package</a>
103	<a href="#">5.815.524</a>		<a href="#">VCSEL including GaTIP active region</a>
104	<a href="#">5.796.769</a>		<a href="#">Red light vertical cavity surface emitting laser</a>
105	<a href="#">5.789.733</a>		<a href="#">Smart card with contactless optical interface</a>
106	<a href="#">5.774.486</a>		<a href="#">Waveguide power monitoring system for vertical cavity surface emitting lasers</a>
107	<a href="#">5.764.671</a>		<a href="#">VCSEL with selective oxide transition regions</a>
108	<a href="#">5.757.836</a>		<a href="#">Vertical cavity surface emitting laser with laterally integrated photodetector</a>
109	<a href="#">5.757.829</a>		<a href="#">Flip chip power monitoring system for vertical cavity surface emitting lasers</a>
110	<a href="#">5.757.741</a>		<a href="#">CD ROM head with VCSEL or VCSEL array</a>
111	<a href="#">5.751.757</a>		<a href="#">VCSEL with integrated MSM photodetector</a>

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112	<a href="#"><u>5.751.471</u></a>	<a href="#"><u>Switchable lens and method of making</u></a>
113	<a href="#"><u>5.748.665</u></a>	<a href="#"><u>Visible VCSEL with hybrid mirrors</u></a>
114	<a href="#"><u>5.748.161</u></a>	<a href="#"><u>Integrated electro-optical package with independent menu bar</u></a>
115	<a href="#"><u>5.742.630</u></a>	<a href="#"><u>VCSEL with integrated pin diode</u></a>
116	<a href="#"><u>5.741.724</u></a>	<a href="#"><u>Method of growing gallium nitride on a spinel substrate</u></a>
117	<a href="#"><u>5.739.800</u></a>	<a href="#"><u>Integrated electro-optical package with LED display chip and substrate with drivers and central opening</u></a>
118	<a href="#"><u>5.732.103</u></a>	<a href="#"><u>Long wavelength VCSEL</u></a>
119	<a href="#"><u>5.719.893</u></a>	<a href="#"><u>Passivated vertical cavity surface emitting laser</u></a>
120	<a href="#"><u>5.719.892</u></a>	<a href="#"><u>Hybrid mirror structure for a visible emitting VCSEL</u></a>
121	<a href="#"><u>5.710.441</u></a>	<a href="#"><u>Microcavity LED with photon recycling</u></a>
122	<a href="#"><u>5.708.280</u></a>	<a href="#"><u>Integrated electro-optical package and method of fabrication</u></a>
123	<a href="#"><u>5.706.306</u></a>	<a href="#"><u>VCSEL with distributed Bragg reflectors for visible light</u></a>
124	<a href="#"><u>5.703.664</u></a>	<a href="#"><u>Integrated electro-optic package for reflective spatial light modulators</u></a>
125	<a href="#"><u>5.699.073</u></a>	<a href="#"><u>Integrated electro-optical package with carrier ring and method of fabrication</u></a>
126	<a href="#"><u>5.661.075</u></a>	<a href="#"><u>Method of making a VCSEL with passivation</u></a>
127	<a href="#"><u>5.654.228</u></a>	<a href="#"><u>VCSEL having a self-aligned heat sink and method of making</u></a>
128	<a href="#"><u>5.644.369</u></a>	<a href="#"><u>Switchable lens/diffuser</u></a>
129	<a href="#"><u>5.638.392</u></a>	<a href="#"><u>Short wavelength VCSEL</u></a>
130	<a href="#"><u>5.636.298</u></a>	<a href="#"><u>Coalescing optical module and method for making</u></a>
131	<a href="#"><u>5.633.886</u></a>	<a href="#"><u>Short wavelength VCSEL with Al-free active region</u></a>
132	<a href="#"><u>5.625.734</u></a>	<a href="#"><u>Optoelectronic interconnect device and method of making</u></a>
133	<a href="#"><u>5.574.744</u></a>	<a href="#"><u>Optical coupler</u></a>
134	<a href="#"><u>5.563.900</u></a>	<a href="#"><u>Broad spectrum surface-emitting led</u></a>
135	<a href="#"><u>5.557.626</u></a>	<a href="#"><u>Patterned mirror VCSEL with adjustable selective etch region</u></a>
136	<a href="#"><u>5.555.341</u></a>	<a href="#"><u>Waveguide with an electrically conductive channel</u></a>
137	<a href="#"><u>5.550.941</u></a>	<a href="#"><u>Optoelectronic interface module</u></a>
138	<a href="#"><u>5.546.413</u></a>	<a href="#"><u>Integrated light emitting device</u></a>
139	<a href="#"><u>5.545.359</u></a>	<a href="#"><u>Method of making a plastic molded optoelectronic interface</u></a>
140	<a href="#"><u>5.543.958</u></a>	<a href="#"><u>Integrated electro-optic package for reflective spatial light modulators</u></a>
141	<a href="#"><u>5.540.799</u></a>	<a href="#"><u>Method of fabricating optical waveguide from a laminate</u></a>
142	<a href="#"><u>5.539.554</u></a>	<a href="#"><u>Integrated electro-optic package for reflective spatial light</u></a>
143	<a href="#"><u>5.539.200</u></a>	<a href="#"><u>Integrated optoelectronic substrate</u></a>
144	<a href="#"><u>5.538.919</u></a>	<a href="#"><u>Method of fabricating a semiconductor device with high heat conductivity</u></a>
145	<a href="#"><u>5.534.888</u></a>	<a href="#"><u>Electronic book</u></a>
146	<a href="#"><u>5.530.715</u></a>	<a href="#"><u>Vertical cavity surface emitting laser having continuous grading</u></a>
147	<a href="#"><u>5.521.992</u></a>	<a href="#"><u>Molded optical interconnect</u></a>
148	<a href="#"><u>5.517.348</u></a>	<a href="#"><u>Voltage controlled transparent layer for a bi-directional device</u></a>
149	<a href="#"><u>5.511.138</u></a>	<a href="#"><u>Interlocking waveguide and method of making</u></a>
150	<a href="#"><u>5.498.883</u></a>	<a href="#"><u>Superluminescent edge emitting device with apparent vertical light emission and method of making</u></a>
151	<a href="#"><u>5.493.437</u></a>	<a href="#"><u>External communication link for a credit card pager</u></a>
152	<a href="#"><u>5.491.491</u></a>	<a href="#"><u>Portable electronic equipment with binocular virtual display</u></a>
153	<a href="#"><u>5.486.946</u></a>	<a href="#"><u>Integrated electro-optic package for reflective spatial light modulators</u></a>
154	<a href="#"><u>5.485.318</u></a>	<a href="#"><u>Dual image manifestation apparatus with integrated electro-optical package</u></a>
155	<a href="#"><u>5.482.891</u></a>	<a href="#"><u>VCSEL with an integrated heat sink and method of making</u></a>
156	<a href="#"><u>5.482.658</u></a>	<a href="#"><u>Method of making an optoelectronic interface module</u></a>
157	<a href="#"><u>5.478.774</u></a>	<a href="#"><u>Method of fabricating patterned-mirror VCSELs using selective growth</u></a>

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158	<a href="#"><u>5.473.716</u></a>	<a href="#"><u>Fiber bundle interconnect and method of making same</u></a>
159	<a href="#"><u>5.469.185</u></a>	<a href="#"><u>Remote sensory unit and driver</u></a>
160	<a href="#"><u>5.468.656</u></a>	<a href="#"><u>Method of making a VCSEL</u></a>
161	<a href="#"><u>5.468.582</u></a>	<a href="#"><u>Fused optical layer and method of making</u></a>
162	<a href="#"><u>5.467.215</u></a>	<a href="#"><u>Integrated electro-optic package for reflective spatial light modulators</u></a>
163	<a href="#"><u>5.466.633</u></a>	<a href="#"><u>Optical reading head and method for making same</u></a>
164	<a href="#"><u>5.452.387</u></a>	<a href="#"><u>Coaxial optoelectronic mount and method of making same</u></a>
165	<a href="#"><u>5.446.752</u></a>	<a href="#"><u>VCSEL with current blocking layer offset</u></a>
166	<a href="#"><u>5.437.092</u></a>	<a href="#"><u>Method of making contact areas on an optical waveguide</u></a>
167	<a href="#"><u>5.432.809</u></a>	<a href="#"><u>VCSEL with Al-free cavity region</u></a>
168	<a href="#"><u>5.432.630</u></a>	<a href="#"><u>Optical bus with optical transceiver modules and method of manufacture</u></a>
169	<a href="#"><u>5.428.704</u></a>	<a href="#"><u>Optoelectronic interface and method of making</u></a>
170	<a href="#"><u>5.422.901</u></a>	<a href="#"><u>Semiconductor device with high heat conductivity</u></a>
171	<a href="#"><u>5.416.870</u></a>	<a href="#"><u>Optoelectronic interface device and method with reflective surface</u></a>
172	<a href="#"><u>5.408.547</u></a>	<a href="#"><u>Optical read/write head</u></a>
173	<a href="#"><u>5.400.423</u></a>	<a href="#"><u>Molded star coupler and method of making same</u></a>
174	<a href="#"><u>5.400.352</u></a>	<a href="#"><u>Semiconductor laser and method therefor</u></a>
175	<a href="#"><u>5.390.275</u></a>	<a href="#"><u>Molded waveguide and method for making same</u></a>
176	<a href="#"><u>5.389.312</u></a>	<a href="#"><u>Method of fabricating molded optical waveguides</u></a>
177	<a href="#"><u>5.388.120</u></a>	<a href="#"><u>VCSEL with unstable resonator</u></a>
178	<a href="#"><u>5.369.529</u></a>	<a href="#"><u>Reflective optoelectronic interface device and method of making</u></a>
179	<a href="#"><u>5.369.415</u></a>	<a href="#"><u>Direct retinal scan display with planar imager</u></a>
180	<a href="#"><u>5.367.593</u></a>	<a href="#"><u>Optical/electrical connector and method of fabrication</u></a>
181	<a href="#"><u>5.361.317</u></a>	<a href="#"><u>Assembly with fixture aligning and affixing an optical fiber to an optical device</u></a>
182	<a href="#"><u>5.359.686</u></a>	<a href="#"><u>Interface for coupling optical fibers to electronic circuitry</u></a>
183	<a href="#"><u>5.359.669</u></a>	<a href="#"><u>Remote retinal scan identifier</u></a>
184	<a href="#"><u>5.359.618</u></a>	<a href="#"><u>High efficiency VCSEL and method of fabrication</u></a>
185	<a href="#"><u>5.358.880</u></a>	<a href="#"><u>Method of manufacturing closed cavity LED</u></a>
186	<a href="#"><u>5.351.331</u></a>	<a href="#"><u>Method and apparatus for splicing optical fibers with signal I/O</u></a>
187	<a href="#"><u>5.351.257</u></a>	<a href="#"><u>VCSEL with vertical offset operating region providing a lateral waveguide and current limiting and method of fabrication</u></a>
188	<a href="#"><u>5.349.210</u></a>	<a href="#"><u>Optical reading head with angled array</u></a>
189	<a href="#"><u>5.348.616</u></a>	<a href="#"><u>Method for patterning a mold</u></a>
190	<a href="#"><u>5.345.530</u></a>	<a href="#"><u>Molded waveguide and method for making same</u></a>
191	<a href="#"><u>5.345.527</u></a>	<a href="#"><u>Intelligent opto-bus with display</u></a>
192	<a href="#"><u>5.345.524</u></a>	<a href="#"><u>Optoelectronic transceiver sub-module and method for making</u></a>
193	<a href="#"><u>5.337.397</u></a>	<a href="#"><u>Optical coupling device and method for making</u></a>
194	<a href="#"><u>5.337.391</u></a>	<a href="#"><u>Optoelectronic sub-module and method of making same</u></a>
195	<a href="#"><u>5.335.300</u></a>	<a href="#"><u>Method of manufacturing I/O node in an optical channel waveguide and apparatus for utilizing</u></a>
196	<a href="#"><u>5.325.451</u></a>	<a href="#"><u>Modular optical waveguide and method for making</u></a>
197	<a href="#"><u>5.324.964</u></a>	<a href="#"><u>Superluminescent surface light emitting device</u></a>
198	<a href="#"><u>5.323.477</u></a>	<a href="#"><u>Contact array imager with integral waveguide and electronics</u></a>
199	<a href="#"><u>5.313.545</u></a>	<a href="#"><u>Molded waveguide with a unitary cladding region and method of making</u></a>
200	<a href="#"><u>5.309.537</u></a>	<a href="#"><u>Optoelectronic coupling device and method of making</u></a>
201	<a href="#"><u>5.286.982</u></a>	<a href="#"><u>High contrast ratio optical modulator</u></a>
202	<a href="#"><u>5.282.071</u></a>	<a href="#"><u>Contact areas on an optical waveguide and method of making</u></a>
203	<a href="#"><u>5.276.762</u></a>	<a href="#"><u>Magnetic holding methods for optical fiber I/O assembly</u></a>

204	<a href="#">5.276.754</a>	<a href="#">Optoelectronic mount and method for making</a>
205	<a href="#">5.271.083</a>	<a href="#">Molded optical waveguide with contacts utilizing leadframes and method of making same</a>
206	<a href="#">5.265.184</a>	<a href="#">Molded waveguide and method for making same</a>
207	<a href="#">5.249.245</a>	<a href="#">Optoelectronic mount including flexible substrate and method for making same</a>
208	<a href="#">5.230.030</a>	<a href="#">Interface coupling electronic circuitry</a>
209	<a href="#">5.228.101</a>	<a href="#">Electrical to optical links using metalization</a>
210	<a href="#">5.225.816</a>	<a href="#">Electrical connector with display</a>
211	<a href="#">5.218.465</a>	<a href="#">Intelligent interconnects for broadband optical networking</a>
212	<a href="#">5.172.384</a>	<a href="#">Low threshold current laser</a>
213	<a href="#">5.170.448</a>	<a href="#">Optical waveguide apparatus and method for partially collecting light</a>
214	<a href="#">5.125.054</a>	<a href="#">Laminated polymer optical waveguide interface and method of making same</a>
215	<a href="#">5.116.461</a>	<a href="#">Method for fabricating an angled diffraction grating</a>
216	<a href="#">5.068.007</a>	<a href="#">Etching of materials in a noncorrosive environment</a>
217	<a href="#">5.067.829</a>	<a href="#">Dynamic optical beam steering</a>
218	<a href="#">5.045.908</a>	<a href="#">Vertically and laterally illuminated p-i-n photodiode</a>
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- 1) Reviewer: European Commission ICT-29-2016: Photonics KET 2016 (section a(ii) Breakthrough in miniaturization of SSL light engines and systems)
  - a. 11/5/2016
  - b. <http://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020/topics/5094-ict-29-2016.html>
- 2) Keynote speech: Next decade in fiber optic communications
  - a. 30/4/2001
  - b. Electronicast: 13th Annual Fiber Optics for the Next Decade Conference
  - c. <http://www.photonics.com/Article.aspx?AID=8916>
- 3) Keynote speech: "Business and Technical Perspectives for Optical Networking"
  - a. 14/7/2002
  - b. PhoPack 2002 Stanford University
  - c. [http://www.accessmylibrary.com/coms2/summary\\_0286-25792277\\_ITM](http://www.accessmylibrary.com/coms2/summary_0286-25792277_ITM)
- 4) Talk and abstract: RIE and MIE comparison for optoelectronic integrated circuit processing
  - a. 11/1988
  - b. IEEE LEOS Conference, Santa Clara, California
  - c. [http://books.google.com/books/about/LEOS\\_88.html?id=LUS0cQAACAAJ](http://books.google.com/books/about/LEOS_88.html?id=LUS0cQAACAAJ)
- 5) Reviewer: European Commission ICT-29-2016: Photonics KET 2016 (a(iii) Pervasive high-specificity and high-sensitivity sensing for a safer environment)
  - a. 12/5/2016
  - b. European Commission
  - c. <http://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020/topics/5094-ict-29-2016.html>
- 6) Paper: Study of the Structural and Thermal Properties of Single Crystalline Epitaxial Rare-Earth-Metal Oxide Layers Grown on Si(111)
  - a. 2011
  - b. ECS Transactions 16, 161 (2011)
  - c. <http://ecst.ecsdl.org/content/41/3/161>
- 7) Invited talk and abstract: Use of VCSELs for the MONSOON parallel digital computer

- a. 01/1991
  - b. International workshop on architectures for free-space digital computing, Colorado.
- 8) Invited talk and abstract: VCSEL Technology and Progress
  - a. 1993
  - b. IEEE Waves and Devices, Phoenix Section, Tempe, Arizona, Arizona State University
- 9) Paper: An inversion channel technology for opto-electronic integration
  - a. 09/1988
  - b. "Optical Communication, 1988. (ECOC 88). Fourteenth European Conference on (Conf. Publ. No.292), Publication Year: 1988, Page(s): 211 - 214 vol.1"
  - c. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=93560>
- 10) Invited Talk/Panel session: EPIC technology workshop on Photonic Integrated Circuits (PIC) packaging standardization
  - a. 18/6/2014
  - b. EPIC
  - c. <http://epic-assoc.com/contact-us/?at=94>
- 11) Invited talk and abstract: Packaging VCSELs with GUIDECAS(TM) an overmolded waveguide packaging platform
  - a. 08/1994
  - b. IEEE Tropical workshop on optoelectronic packaging, Breckenridge, Colorado
- 12) Invited talk/keynote lecture: Compound semiconductors driving photonics technologies to become the future for high-speed communications through integration, performance, and sustainability
  - a. 12/6/2014
  - b. Glyndwr University, Wales, UK
  - c. <http://www.glyndwr.ac.uk/en/AboutGlyndwrUniversity/Newsandmediacentre/Newsarchive/PressReleases2014/UniWeek/>
- 13) Invited talk and abstract: Ridge waveguide VCSELs: improvement over planar VCSELs
  - a. 05/1994
  - b. USA Laser workshop, CLEO, Baltimore, MD
- 14) Special invited talk: "10 Grand Challenges in Photonics"
  - a. 31/10/2007
  - b. Sixth annual symposium UNCC Optoelectronics Center
  - c. <http://opticscenter.uncc.edu/node/265>
- 15) Keynote talk: Entitled "The rise of PIC based technologies over the next decade and how datacenters and telecom may enable other exciting applications"
  - a. 1/5/2017
  - b. Xilinx as part of their; "Xilinx silicon technology series seminars"
  - c. <http://www.xilinx.com>
- 16) Invited talk: Worldwide Optoelectronic Trends and Economic Opportunities.
  - a. 18/11/2005
  - b. UNCC 4th Annual symposium: UNC Charlotte Center for Optoelectronics and Optical Communications
  - c. <http://opticscenter.uncc.edu/node/275>

- 17) Reviewer: European Commission ICT-29-2016: Photonics KET 2016 (section a(i) Biophotonics: advanced imaging for in-depth disease diagnosis)
  - a. 10/5/2016
  - b. European Commission
  - c. <http://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020/topics/5094-ict-29-2016.html>
- 18) Invited talk: Global optoelectronics technology roadmaps and trends
  - a. 27/10/2006
  - b. UNCC 5th Annual Symposium: UNC Charlotte Center for Optoelectronics and Optical Communications
  - c. <http://opticscenter.uncc.edu/node/268>
- 19) Keynote talk: Global optoelectronics and green photonics trends
  - a. 28/10/2009
  - b. UNCC 8th Annual Symposium: Optoelectronics Center
  - c. <http://opticscenter.uncc.edu/node/255>
- 20) Invited talk and abstract: Optoelectronic Devices and Applications
  - a. 1993
  - b. IEEE workshop on optical interconnects
- 21) Reviewer: European Commission ICT-29-2016 Photonics KET (b) Innovation Actions (ii) Pilot line for assembly and packaging
  - a. 15/5/2016
  - b. European Commission
  - c. <http://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020/topics/5094-ict-29-2016.html>
- 22) Keynote talk and abstract: Is this the rise of green photonics?
  - a. 12/2009
  - b. ICFO (Institut de Ciencies Fotoniques) Barcelona, Spain
  - c. <http://www.icfo.es/images/news/ICFO%20CLP%20DAY%20Program.pdf>
- 23) Paper: Low-cost high-performance optical interconnect
  - a. 1996
  - b. Proceedings, Conference on Lasers and Electro-Optics, (CLEO), vol 9, 1996
  - c. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=864750>
- 24) Technical Advisor/Expert: 2nd review of MIRPHAB pilot line consortium funded by H2020 at European Commission
  - a. 20/2/2017
  - b. 2nd review for MIRPHAB consortium at the European Commission, Brussels
  - c. European Commission, Brussels
  - d. <https://www.iaf.fraunhofer.de/en/research/research-areas/semiconductor-lasers/mirphab.html>
- 25) Paper: Performance and advantages of BICFETs versus HBTs
  - a. 09/1988
  - b. "Bipolar Circuits and Technology Meeting, 1988., Proceedings of the 1988 Digital Object Identifier: 10.1109/BIPOL.1988.51041 Publication Year: 1988 , Page(s): 41- 45"
  - c. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=51041>
- 26) Talk and abstract: Magnetron Ion Etching of self aligned HFETs

- a. 05/1987
  - b. Electrochemical Society (ECS) Conference proceedings SOTAPOCS VI, Compound Semiconductors, Philadelphia
  - c. [http://www.electrochem.org/meetings/biannual/past\\_meetings\\_list.htm](http://www.electrochem.org/meetings/biannual/past_meetings_list.htm)
- 27) Project advisor: European Commission ICT-28-2015 Cross-Cutting ICT KETs: Innovation Action (b) Pilot line for PIC fabrication on III-V and/or dielectric based platforms for PICs (Photonic Integrated Circuits)
- a. 24/9/2015
  - b. European Commission
  - c. <http://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020/topics/916-ict-28-2015.html>
- 28) Paper: Integrated high reflectivity silicon substrates for GaN LEDs
- a. 13/1/2012
  - b. Volume 9, Issue 3-4, pages 814-817, March 2012, physica status solidi (c)
  - c. <http://onlinelibrary.wiley.com/doi/10.1002/pssc.201100393/abstract>
- 29) Paper: Silicon light emitting device based on rare earth oxide superlattice
- a. 09/2010
  - b. 7th IEEE International conference on Group IV photonics, Beijing China
  - c. <http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=5643407&url=http%3A%2F%2Fieeexplore.ieee.org%2Fiel5%2F5623516%2F5643317%2F05643407.pdf%3Farnumber%3D5643407>
- 30) Paper: Integrated high reflectivity silicon substrates for GaN LEDs
- a. 13/1/2012
  - b. "Conference Publication: ICNS-9 "Contributed Article Integrated high reflectivity silicon substrates for GaN LEDs
  - c. F. Erdem Arkun\*, Rytis Dargis, Robin Smith, David Williams, Andrew Clark, Michael Lebby
  - d. Article first published online: 13 JAN 2012" ICNS-9 "Contributed Article Integrated high reflectivity silicon substrates for GaN LEDs
  - e. <http://onlinelibrary.wiley.com/doi/10.1002/pssc.201100393/abstract>
- 31) Cover story/Interview: Does a foundry model add up for InP optoelectronics
- a. 07/2005
  - b. Interview with Michael Hatcher from Compound Semiconductor magazine. Volume 11, Number 7, August 2005 pp 17-19
  - c. Compound Semiconductor: Three-fives and silicon heterostructures
  - d. <http://www.compoundsemiconductor.net>
- 32) Paper: A low-cost high-performance optical interconnect
- a. 1996
  - b. "Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on Volume: 19, Issue: 3 Digital Object Identifier: 10.1109/96.533892 Publication Year: 1996, Page(s): 532- 539"
  - c. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=533892>
- 33) Co-Chairman Optoelectronics session, 48th ECTC Conference
- a. 25/5/1998
  - b. Co-chairman Optoelectronics session, 48th ECTC Conference Seattle, Washington

- c. ECTC, IEEE-CPMT, EIA/ECA
- d. <http://www.ectc.net>
- 34) Paper: GaAs/AlGaAs inversion channel devices for an integrated opto-electronic technology
  - a. 06/1988
  - b. "Electron Devices, IEEE Transactions on Volume: 35, Issue: 12 Digital Object Identifier: 10.1109/16.8871 Publication Year: 1988"
  - c. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=8871>
- 35) Paper & Poster: 100Gb/s Multi-guide vertical integration transmitter PIC in InP for fiber-optics interconnects
  - a. 24/9/2013
  - b. Sasa Ristic and Michael Lebby, Valery Tolstikhin, and Kirill Pimenov,
  - c. ECOC 2013
  - d. <http://www.ecoc2013.org/sc2.html>
- 36) Paper: Photonic Intgeration: what is the Holy Grail?
  - a. 14/10/2009
  - b. Compound Semiconductor
  - c. <http://compoundsemiconductor.net/csc/features-details.php?id=40435>
- 37) Paper: Optical components and their role in optical networks
  - a. 2001
  - b. Electronic Components and Technology Conference, 2001. Proceedings., 51<sup>st</sup>
  - c. [http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=927765&url=http%3A%2F%2Fieeexplore.ieee.org%2Fxppls%2Fabs\\_all.jsp%3Farnumber%3D927765](http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=927765&url=http%3A%2F%2Fieeexplore.ieee.org%2Fxppls%2Fabs_all.jsp%3Farnumber%3D927765)
- 38) Paper: Green photonics technology and markets
  - a. 09/2009
  - b. Green photonics technology will open up opportunities over the next decade for new and creative products to be designed as the interest in a green, clean and energy efficient lifestyle continues to grow. This overview forecasts the optoelectronics expectations for green photonics technology and associated markets over the next decade and explores just a few of the exciting opportunities from green photonics technology.
  - c. Electronics Letters, Vol 45, issue 20
  - d. <http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=5270369&url=http%3A%2F%2Fieeexplore.ieee.org%2Fiel5%2F2220%2F5270368%2F05270369.pdf%3Farnumber%3D5270369>
- 39) Paper: OEICs: commercialization at last
  - a. 07/2001
  - b. Compound Semiconductor, vol. 7. no. 6, pp. 81-2, 85, July 2001
  - c. <http://www.compoundsemiconductor.net/csc/features-details.php?cat=features&id=11719>
- 40) Report: Photonics industry-university collaborations (PICs)
  - a. 1/6/2009
  - b. OIDA Final Technical Report
  - c. <http://oai.dtic.mil/oai/oai?verb=getRecord&metadataPrefix=html&identifier=ADA502737>

- 41) Invited Paper and Presentation: Approaching the problem of high density interconnects in the 'Monsoon' data-flow parallel processor with optics"
- a. 28/1/1991
  - b. AFOSR, ONR, DARPA: A compendium of position papers from the workshop on architectures for free space digital optical computing
  - c. [http://www.researchgate.net/publication/235184814\\_A\\_Compendium\\_of\\_Position\\_Papers\\_from\\_the\\_Workshop\\_on\\_Architectures\\_for\\_Free\\_Space\\_Digital\\_Optical\\_Computing\\_Held\\_in\\_Vail\\_Colorado\\_on\\_28-30\\_January\\_1991](http://www.researchgate.net/publication/235184814_A_Compendium_of_Position_Papers_from_the_Workshop_on_Architectures_for_Free_Space_Digital_Optical_Computing_Held_in_Vail_Colorado_on_28-30_January_1991)
- 42) Session organizer/Committee member: Market Focus at ECOC exhibit 2015
- a. 28/9/2015
  - b. Session organizer/Committee member: Market Focus at ECOC exhibit 2015 with sessions in broadband access, datacentres, service provider optical transmission, network agility/SDN, photonics integration and packet optical transport. Nexus Business Media Ltd
  - c. <http://webcache.googleusercontent.com/search?q=cache:Qb68vjzhV5IJ:www.ecocexhibition.com/visitorhome/marketfocus2015/cfs+&cd=1&hl=en&ct=clnk&gl=us&client=safari>
- 43) Invited Presentation and Abstract: VCSEL Technology - VCSEL technology is discussed with the work between AMP and MODE (division of EMCORE) fiber optics.
- a. ECOC European Laser Workshop (in association with ECOC 1998, Madrid, Spain
  - b. [https://openlibrary.org/books/OL22322573M/ECOC\\_'98\\_24th\\_European\\_Conference\\_on\\_Optical\\_Communication](https://openlibrary.org/books/OL22322573M/ECOC_'98_24th_European_Conference_on_Optical_Communication)
- 44) Paper and Invited talk: VCSEL Devices and Packaging for Fiber Optic Transceivers
- a. 30/3/1998
  - b. OSA Technical Digest: Integrated Photonics Research (IPR) 1998 paper: IWD1
  - c. <http://www.opticsinfobase.org/abstract.cfm?URI=IPR-1998-IWD1>
- 45) Invited Paper: Elegant cost effective optical subsystems for next generation optical networks
- a. 13/11/2002
  - b. Electronicast: 4th Annual OADM and advanced photonics communication networks conference - market and technology trends, San Mateo, California
  - c. <http://www.electronicastconsultants.com/>
- 46) Paper: Key challenges and results of VCSELs in data links
- a. 1996
  - b. "Lasers and Electro-Optics Society Annual Meeting, 1996. LEOS 96., IEEE Volume: 2 Digital Object Identifier: 10.1109/LEOS.1996.571604 Publication Year: 1996 , Page(s): 167 - 168 vol.2"
  - c. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=571604>
- 47) Paper: A p-channel BICFET in the InGaAs/InAlAs material system
- a. 06/1988
  - b. "Electron Device Letters, IEEE Volume: 9, Issue: 6 Digital Object Identifier: 10.1109/55.716 Publication Year: 1988 , Page(s): 278 - 280"
  - c. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=716&tag=1>
- 48) Interview Optcon (Japan), "Ignis Optics: Small is beautiful"
- a. 15/8/2002



- b. Overview of Ignis Optics strategy for fiber optic transceivers with innovative optoelectronic devices and packaging (in Japanese).
  - c. Optcon volume 8, no 161, pp50-51
  - d. <http://magissuelist.nichigai.co.jp/detail?id=000000098732>
- 49) Book: Research in optoelectronic devices volume II
- a. 1996
  - b. Annual collection of optoelectronic device and reliability department papers at the photonics technology center, Motorola, Tempe, USA. Key focus was the commercialization of VCSEL technology, especially at 850nm for the optobus parallel array product and other associated VCSEL prototypes. Demonstration of 660nm VCSELs discussed.
  - c. Motorola
- 50) Keynote invited speech: Green Photonics and GaN-on-Si for LEDs and Ge-on-Si for high Efficiency Multi-junction for PVs
- a. 12/2011
  - b. Conference proceedings: High Capacity Optical Networks and Enabling Technologies (HONET), 2011
  - c. <http://honet.uncc.edu/archive/honet11/speakers.htm>
- 51) Invited Presentation: "Starting a company and hitting the ground running"
- a. 7/2/2001
  - b. Storm Ventures limited partner meeting
  - c. <http://www.stormventures.com>
- 52) Book: Research in VCSEL devices - Annual technical review 1995
- a. 1995
  - b. Annual collection of optoelectronic device and reliability department papers at the photonics technology center, Motorola, Tempe, USA.
  - c. Key focus was the commercialization of VCSEL technology, especially at 850nm for the Optobus™ parallel array product and other associated VCSEL prototypes.  
Motorola
- 53) Paper: Optical bistability in vertical cavity surface emitting lasers with a simple intra-cavity epitaxial absorber layer
- a. 4/10/1998
  - b. Conference Digest: Semiconductor Laser Conference, 1998. ISLC 1998 NARA. 1998 IEEE 16th International
- 54) Invited Paper (extended abstract) and Presentation: Automated commercial fabrication of wideband tunable lasers using ultra-high resolution e-beam lithography
- a. 27/10/2004
  - b. IoP/CS-MAX extended abstract at the Compound Semiconductor Manufacturing Expo, Monterey, California, pp92-94 in the technical digest.
  - c. <http://www.compoundsemiconductor.net>
- 55) Trial & Cross: Testimony before the US-China economic and security review commission on the optoelectronics industry
- a. 24/3/2009
  - b. "Expert witness and testimony on Capitol Hill
  - c. Final oral comments: In preparing this testimony, many people I contacted stressed the importance of decisive action by the U.S. government and industry

now. Optoelectronics sits at the intersection of multiple technical disciplines. U.S. universities and industry are particularly adept at bringing diverse people together to work on complex problems. We have, by the nature of our inherent diversity, an advantage. What for many presents a challenge, for us comes naturally. Thank you for this opportunity to present our industry's perspective. "

- d. United States China Commission
  - e. [http://www.uscc.gov/hearings/2009hearings/written\\_testimonies/09\\_03\\_24\\_wrts/09\\_03\\_24\\_lebby\\_statement.pdf](http://www.uscc.gov/hearings/2009hearings/written_testimonies/09_03_24_wrts/09_03_24_lebby_statement.pdf)
- 56) Paper: Growing at light speed
- a. The article discusses the significance of optoelectronics in high technology manufacturing industries. Optoelectronics components are being used in the manufacturing cameras of mobile phones, plasma display panel TVs and LCD TVs, among others. Since its application allows product differentiation and innovation, it has spurred growth in segments such as the consumer/entertainment, computer and communications industries. The article also discusses the differences in the material and processing equipment such as silicon photonics.
  - b. 09/2007
  - c. IEEE Circuits Assembly; Sep 2007, Vol. 18 Issue 9, p44
  - d. <http://www.thefreelibrary.com/Growing+at+light+speed%3a+after+a+false+start%2c+OE+is+fast+becoming+a...-a0168812805>
- 57) Paper: Fiber optic sensing technology: emerging markets and trends
- a. 2007
  - b. Third European Workshop on Optical Fibre Sensors.
  - c. Edited by Cutolo, Antonello; Culshaw, Brian; Lopez-Higuera, Joshua Miguel.
  - d. Proceedings of the SPIE, Volume 6619, pp. 661902 (2007). (SPIE Homepage)
  - e. <http://adsabs.harvard.edu/abs/2007SPIE.6619E...2H>
- 58) Paper: O/e-MCM packaging with new, patternable dielectric and optical materials
- a. 05/1998
  - b. Electronic Components & Technology Conference, 1998. 48th IEEE
  - c. <http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=678929&url=http%3A%2F%2Fieeexplore.ieee.org%2Fiel4%2F5582%2F14953%2F00678929.pdf%3Farnumber%3D678929>
- 59) Video Interview: ECOC Market Focus on Datacenters and emerging new PIC technologies that include silicon and polymer photonics
- a. 3/10/2016
  - b. Video taped interview by ECOC Exhibition Market Focus on Datacenters and emerging new PIC technologies that include polymer photonics.
  - c. ECOC Exhibition
  - d. <http://www.ecocexhibition.com/interviews2016>
- 60) Paper: Characteristics of VCSELs and VCSEL arrays for Optical Data Links
- a. 10/12/1996
  - b. Motorola: Technical Enrichment Matrix Conference, Motorola SPS- SABA, Hilton Pavilion, Mesa, Az
- 61) Paper: Very high-transconductance heterojunction field-effect transistor (HFET)
- a. 01/1987



- b. "A new form of FET has been demonstrated in the GaAs/AlGaAs material system. Designated the HFET, it has shown a transconductance of 500mS/mm at 300 K for a nominal  $L_g = 2/\mu m$  and a drain current of 430mA/mm. The conduction occurs in an inversion channel at the heterointerface"
  - c. "Electronics Letters Volume: 23, Issue: 2 Digital Object Identifier: 10.1049/el:19870056 Publication Year: 1987 , Page(s): 77 - 79"
  - d. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=4257306>
- 62) Keynote Talk: Industry 'Optomism'
- a. 30/4/2001
  - b. Electronicast; Fiber Optics for the next decade conference; 13th Annual Monterey conference <http://www.electronicastconsultants.com>
- 63) Invited talk and moderator: Integrated photonics pilot lines
- a. 14/11/2014
  - b. "Photonics Pilot Line Workshop 14 November 2014 - Brussels, Belgium
  - c. European Commission and Photonics21
  - d. <http://www.photonics21.org/download/Events/DraftagendaPhotonicsPilotLineworkshop-Website.pdf>
- 64) Invited Talk and Abstract: VCSEL/detector technology for parallel optical interconnects
- a. 17/6/1997
  - b. International Workshop for new technologies, interconnects, and communications in distributed and parallel systems by IRIT, ONERA, CERT, CNRS, and LAAS (France)
- 65) Invited Talk: OIDA optoelectronics markets, technology and opportunities for optofluidics
- a. 20/10/2006
  - b. Organized by the DARPA center for optofluidics: translational research and commercialization workshop.
  - c. DARPA Optofluidics industry forum, UCSD San Diego, CA
  - d. <http://www.biophot.caltech.edu/optofluidics/>
- 66) Article: "Optoelectronics Technology: New and Exciting Markets in Consumer and Entertainment"
- a. 10/1/2007
  - b. "The total optoelectronics components and enabled products grew 20% in 2005 to \$364 billion, from \$304 billion in 2004. Components grew 17% in 2005 to \$104 billion, from \$89 billion in 2004. When flat panel displays are excluded as components, components grew 10% in 2005 to \$30 billion, from \$27 billion in the previous year. Enabled products grew 21% to \$260 billion in 2005, from \$215 billion in 2004.
  - c. IEEE CPMT Santa Clara
  - d. <http://www.cpmt.org/scv/meetings/cpmt0701.html>
- 67) Paper: Characteristics of VCSEL arrays for parallel optical interconnects
- a. 1996
  - b. "Electronic Components and Technology Conference, 1996. Proceedings., 46th Digital Object Identifier: 10.1109/ECTC.1996.517404 Publication Year: 1996 , Page(s): 279 - 291"
  - c. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=517404>

- 68) Paper: Demonstration of a p-channel GaAs/AlGaAs BICFET
- a. 02/1988
  - b. "Electron Device Letters, IEEE Volume: 9, Issue: 2 Digital Object Identifier: 10.1109/55.2048 Publication Year: 1988 , Page(s): 84 - 86"
  - c. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=2048>
- 69) Reviewer: European Commission ICT-29-2016 Photonics KET (b) Innovation Actions (i) Application driven core photonic devices integrated in systems.
- a. 14/5/2016
  - b. European Commission
  - c. <http://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020/topics/5094-ict-29-2016.html>
- 70) Paper: Optoelectronics Roadmap OIDA-iNEMI
- a. 05/2007
  - b. IEEE Packaging and Assembly
- 71) Article: A New Model for the Optoelectronic Indium-based Semiconductor Industry
- a. 05/2006
  - b. OSA: Optics and Photonics News
  - c. <http://www.osa-opn.org/Content/ViewFile.aspx?id=10456>
- 72) Book: Optoelectronic Markets 2005
- a. 06/2005
  - b. Comprehensive market report and forecast of current optoelectronics markets, needs, technologies, and applications. This report forecasts the current state and direction of the optoelectronics industry.
  - c. OIDA
  - d. <http://www.oida.org/home/publications/oida-publication-report-library/>
- 73) Book: Worldwide Optoelectronics Markets and Trends 2006
- a. 06/2006
  - b. Comprehensive market report and forecast of current optoelectronics markets, needs, technologies, and applications. This report forecasts the current state and direction of the optoelectronics industry.
  - c. OIDA, 431 pages
  - d. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/2006\\_global\\_optoelectronics\\_industry\\_market\\_report/](http://www.oida.org/home/publications/oida_publication_report_library/2006_global_optoelectronics_industry_market_report/)
- 74) Project advisor: European Commission ICT-28-2015 Cross-Cutting ICT KETs: Innovation Action (b) Pilot line for analytical mid-infrared (MIR) micro-sensors
- a. 22/9/2015
  - b. European Commission
  - c. <http://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020/topics/916-ict-28-2015.html>
- 75) Video: The importance of photonics roadmapping
- a. 30/1/2017
  - b. Video on the importance of roadmapping photonics technologies at Photonics West San Francisco, 30th Jan 2017. Interview by Photon Delta.
  - c. <http://www.photondelta.eu>
- 76) Invited Presentation and Abstract: An investor's perspective on optical interconnects
- a. 24/5/2000

- b. The talk discusses the investor's perspective on optical interconnects from Intel Capital.
  - c. IEEE: Workshop on interconnections within high-speed digital systems
  - d. <http://www.oj-ieee.org/>
- 77) Paper: A new heterostructure FET
- a. 12/1986
  - b. "Electron Devices Meeting, 1986 International Volume: 32 Digital Object Identifier: 10.1109/IEDM.1986.191323 Publication Year: 1986, Page(s): 817 - 821"
  - c. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=1486581>
- 78) Panel Session: Semiconductors to Optics
- a. 6/11/2000
  - b. Representing Intel at the conference, the panel explored the reasons why Intel was investing into photonics, optics, and fiber optic communications. Panel moderator was Drew Lanza, VC Morgenthaler.
  - c. JP Morgan communications components conference: the convergence of optical components and communications ICs
  - d. <http://www.thefreelibrary.com/Endwave+Founder+and+EVP+To+Speak+at+JP+Morgan+Communications...-a067529552>
- 79) Growth of GaN by MOCVD on rare earth oxide on Si(111)
- a. 31/10/2013
  - b. ECS Transactions, 58, 455 (2013)
  - c. <http://ecst.ecsdl.org/content/58/4/455.short>
- 80) Article: OPTICAL MATERIALS: 'On-silicon' engineered substrates speed photonic device development
- a. 1/4/2013
  - b. Laser Focus World
  - c. <http://www.laserfocusworld.com/articles/print/volume-49/issue-04/features/optical-materials---on-silicon--engineered-substrates-speed-phot.html>
- 81) Panel Session: An adventure into venture capital - lessons from silicon valley
- a. 12/9/2002
  - b. Evening forum discussion chaired by Professor Richard Harrison, Chair, with panel members Pitch Johnson (VC), Brendan Hyland (Nutrion Ventures), Jane Karwoski (All-hotels Ltd), and Colin Rutherford (Intelli Partners). Sponsored by Scottish Development International, University of Edinburgh, British Council
- 82) Paper: Vertical cavity surface emitting laser packaging with auto power control
- a. 18/5/1997
  - b. Electronic Components and Technology Conference, 1997. Proceedings., 47<sup>th</sup>
  - c. [http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=606195&contentType=Conference+Publications&sortType%3Dasc\\_p\\_Sequence%26filter%3DAND\(p\\_IS\\_Number%3A13278\)](http://ieeexplore.ieee.org/xpl/articleDetails.jsp?tp=&arnumber=606195&contentType=Conference+Publications&sortType%3Dasc_p_Sequence%26filter%3DAND(p_IS_Number%3A13278))
- 83) Webinar and presentation
- a. 29/3/2011
  - b. "The future of photonics webinar and presentation: The Future of Photonics: Three Perspectives brings together three expert viewpoints on the future of the photonics industry (Michael Lebby will be the expert on market trends and

photonic integrated circuits (PICs)). You will learn: global optoelectronics market outlook through 2021 trends in photonic integrated circuits over the next two decades."

- c. Photonics Media
  - d. <http://www.photonics.com/Webinar.aspx?WebinarID=7>
- 84) Book: 2007 Global Optoelectronics Industry Market Report and Forecast
- a. 06/2007
  - b. Comprehensive market report and forecast of current optoelectronics markets, needs, technologies, and applications. This report forecasts the current state and direction of the optoelectronics industry.
  - c. OIDA, 517 pages
  - d. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/2007\\_global\\_optoelectronics\\_industry\\_market\\_report/](http://www.oida.org/home/publications/oida_publication_report_library/2007_global_optoelectronics_industry_market_report/)
- 85) Paper: Use of VCSEL arrays for parallel optical interconnects
- a. 10/4/1996
  - b. Proc. SPIE 2683, Fabrication, Testing, and Reliability of Semiconductor Lasers, 81 (April 10, 1996); doi:10.1117/12.237679
  - c. <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=1015866>
- 86) Book: 2009 Global Optoelectronics Industry Market Report and Forecast
- a. 12/2009
  - b. Comprehensive market report and forecast of current optoelectronics markets, needs, technologies, and applications. This report forecasts the current state and direction of the optoelectronics industry.
  - c. OIDA, 545 pages
  - d. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/2009\\_global\\_optoelectronics\\_industry\\_market\\_report/](http://www.oida.org/home/publications/oida_publication_report_library/2009_global_optoelectronics_industry_market_report/)
- 87) Workshop: The Challenge for Indium Phosphide Photonic Development and the Optical Foundry
- a. 2006
  - b. "Workshop chairman and editor of the report.
  - c. Abstract: Indium Phosphide, InP, is a semiconductor material with properties that make it particularly suitable for optoelectronic devices. Optical communications requirements drove its initial development. Recently, the applications for InP semiconductor devices have broadened to include high-speed electronics and optical sensors. This report examines the current state of the InP device market and its future direction. Addresses challenges for a pure foundry play and the role for InP devices. Seeks to find the best ways to address the needs for InP device development in the U.S."
  - d. OIDA
  - e. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/the\\_challenge\\_for\\_indium\\_phosphide\\_photonic\\_develo/](http://www.oida.org/home/publications/oida_publication_report_library/the_challenge_for_indium_phosphide_photonic_develo/)
- 88) Workshop: Nitride LED and Laser Technology and Its Impact on the Display, Medical, and Storage Industries
- a. 2006
  - b. Workshop chairman and editor of the report:

- c. Abstract: Since the development of p-type material in 1989, research in nitride emitter technology has developed rapidly over the last 15 years. This material system provided a new range of color applications that could be better utilized and with far better reliability than the II-VI material system. This report examines material systems and developments for short wavelength (green-ultraviolet) lasers and LEDs.
  - d. OIDA
  - e. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/nitride\\_led\\_and\\_laser\\_technology\\_and\\_its\\_impact\\_on/](http://www.oida.org/home/publications/oida_publication_report_library/nitride_led_and_laser_technology_and_its_impact_on/)
- 89) Workshop: High Power Diode Laser Sources and Their Impact on Industrial, Medical, and Military Laser Industries
- a. 1/7/2006
  - b. Workshop chairman and editor of the report:
  - c. Abstract: High power semiconductor laser diodes are used in several different market segments today. The technology continues to advance and improvements in efficiency and power are reported each year. Semiconductor laser diodes are used either directly or indirectly to enable new applications or as a replacement for older technology approaches. This report examines practical implementations and limitations for lasers in the 100 W to 100 kW range and roadmaps and developments anticipated over the next five years.
  - d. OIDA
  - e. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/high\\_power\\_diode\\_laser\\_sources\\_and\\_their\\_impact\\_on/](http://www.oida.org/home/publications/oida_publication_report_library/high_power_diode_laser_sources_and_their_impact_on/)
- 90) Keynote talk and invited abstract: "Integrated photonics as a vehicle for the next generation IC"
- a. 9/9/2015
  - b. Internet Technology Applications (ITA) ITA-15 conference Wrexham, Wales, UK 8-11th Sept 2015
  - c. <http://www.ita15.net/keynote-speaker/>
- 91) Talk and panel session: Approaches for combining 3-5 and silicon, add functionality to Si photonics, heterogeneous versus hybrid integration, introduction of photonic platforms
- a. 5/12/2013
  - b. Short presentation on PICs, OEICs, Si photonics, and combinations of these technologies from a revenue, investment, application and technology standpoint.
  - c. EPIC workshop: Meet or eat? collaboration and/or competition in photonic integrated circuits (PICs)
  - d. <http://epic-assoc.com/contact-us/?at=94>
- 92) Invited talk: Feedback USA/International related events
- a. 5/12/2013
  - b. Feedback on the subject of InP PICs, OEICs, and silicon photonics from workshops and related international events from around the globe.
  - c. EPIC workshop: Meet or eat? Collaboration and/or competition in Photonic Integrated Circuits (PICs)?
  - d. <http://epic-assoc.com/contact-us/?at=94>
- 93) Course: Optoelectronics Components and Modules for Datacom and Telecom
- a. 05/2000

- b. Optoelectronics components and modules for the Telecommunication industry and Datacom Networks are rapidly advancing in terms of speed, lower cost and design. The main objectives of this course are to review the current and future trends for active devices and packaging technology for discrete components and data network modules. The course will cover in detail the fundamental active III-V devices and components used today and review current trends in both III-V device technology and packaging for telecom and datacom applications.
  - c. Proceedings 50th Electronics Components and Technology Conference May 2000
  - d. <http://www.thierry-lequeu.fr/data/Ectc/ECTC2000/ECTC2000.pdf>
- 94) Thesis: Fabrication and characterization of the heterojunction field effect transistor and the bipolar inversion channel field effect transistor
- a. 1987
  - b. Characterization of HFETs and BICFETs fabricated from GaAs/AlGaAs with magnetron ion etching, sputtered tungsten gates, ion implanted source/drain contacts and rapid thermal anneals.
  - c. University of Bradford, UK 1987
  - d. <http://www.edt.brad.ac.uk/home/>
- 95) Technical Advisor/Expert: 2nd review of PIX4LIFE pilot line consortium funded by H2020 at European Commission
- a. 14/3/2017
  - b. 2nd review of PIX4LIFE pilot line consortium at the European Commission, Brussels.
  - c. European Commission, Brussels, Belgium
  - d. <http://www.pix4life.eu>
- 96) Invited Presentation: Optoelectronic Integration for Metro DWDM: Intel's perspective...
- a. 3/9/2000
  - b. As part of the ECOC conference in Munich Germany, this workshop invited 9 speakers to discuss the future of optical networking in metropolitan environments.
  - c. Electronicast Europe
  - d. <http://www.electronicastconsultants.com>
- 97) Workshop: Biophotonic Sensors and Smart Fiber Optic Sensor Networks
- a. 1/8/2006
  - b. Workshop chairman and editor of the report:
  - c. Abstract: This roadmap report examines biophotonic sensor opportunities from many perspectives including; government, industrial, university and venture capital. The markets, technologies, commercialization, and roadmap trends are presented in addition to promising areas for R & D.
  - d. OIDA
  - e. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/biophotonic\\_sensors\\_and\\_smart\\_fiber\\_optic\\_sensor\\_n/](http://www.oida.org/home/publications/oida_publication_report_library/biophotonic_sensors_and_smart_fiber_optic_sensor_n/)
- 98) Paper: Parallel optical interconnects using VCSELs
- a. 1995
  - b. "High Speed Semiconductor Devices and Circuits, 1995. Proceedings., IEEE/Cornell Conference on Advanced Concepts in Digital Object Identifier: 10.1109/CORNEL.1995.482526 Publication Year: 1995 , Page(s): 348 - 356"



- c. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=482526>
- 99) Poster paper: A versatile InP OEIC (PIC) platform enabling 100G+ coherent receiver and client-side transceiver engines
  - a. 12/11/2013
  - b. Poster paper describing OneChip's latest results in coherent receivers, LR4 optical engines, and PSM4 optical engines.
  - c. Silicon Photonics Workshop, Southampton University, UK
  - d. [http://www.orc.soton.ac.uk/UKSP\\_presents.html](http://www.orc.soton.ac.uk/UKSP_presents.html)
- 100) Keynote Presentation: Optoelectronics Integration for Metro DWDM, Intel's Perspective
  - a. 9/10/2000
  - b. Electronicast Corporations: Optical communications start-up and emerging companies conference
  - c. <http://www.electronicastconsultants.com>
- 101) Workshop: Wide Area Surveillance
  - a. 1/10/2006
  - b. Workshop chairman and editor of the report:
  - c. Abstract: This report examines wide area surveillance of pipelines and other strategic infrastructure as it is rapidly becoming an important issue on a worldwide basis. The increasing need for surveillance for both homeland security as well as defense applications should make this commercially attractive to both the defense as well as to commercial industry. (Report is 62 pages followed by hard copies of presentations from the forum.)
  - d. OIDA
  - e. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/wide\\_area\\_surveillance/](http://www.oida.org/home/publications/oida_publication_report_library/wide_area_surveillance/)
- 102) Invited Panel Session: Opto Electronic Integrated Circuits - More IC than OE?
  - a. 5/3/2000
  - b. "The panel session focused on optical integration for communications. Other panel members included Brendan Hyland CEO of Kymata amongst others.
  - c. OSA Executive Forum: Photonics and Telecommunications: the tidal wave of the new millennium
  - d. <http://www.laserfocusworld.com/articles/2000/02/osa-executive-forum-at-ofc-2000.html>
- 103) Keynote talk and abstract: "PIC the next generation IC..."
  - a. 23/9/2015
  - b. Photonic Integration Conference, organized by Jakajima, Netherlands
  - c. <http://www.phiconference.com/program/>
- 104) Workshop: 100 Gb Ethernet: The Next Challenge for Communications Systems
  - a. 1/10/2006
  - b. Workshop chairman and editor of the report: Abstract: The communications market is continuously evolving to provide better and cheaper services. These changes have led to the movement away from the traditional voice-switched networks to more data-centric packet networks. This report seeks to examine the next generation of Ethernet devices as we strain the technology limits at 100 Gb/s? How will datacom and telecom networks differ in their approaches? OIDA

- [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/100\\_gb\\_ethernet\\_the\\_next\\_challenge\\_for\\_communi\\_\(1\)/](http://www.oida.org/home/publications/oida_publication_report_library/100_gb_ethernet_the_next_challenge_for_communi_(1)/)
- 105) Paper: Vertical cavity surface emitting laser-based parallel optical data link
- a. 12/1998
  - b. Optical Engineering, vol 37, no. 12, pp.3113-18, Dec. 1998.
  - c. [http://spie.org/x648.html?product\\_id=318648](http://spie.org/x648.html?product_id=318648)
- 106) Workshop: Artificial vision systems
- a. 1/12/2006
  - b. Workshop chairman and editor of the report:
  - c. Abstract: The ability to identify objects of interest and emerging threats around a vehicle in real time or by a warfighter looking for threats in a large field of view is currently severely hampered by the limitations of current algorithms and processing platforms. There have been recent advances in several technology areas, which if combined intelligently could solve this hard problem in enhancing situational awareness cost effectively. This report looks at the issues surrounding automated surveillance systems specifically looking at enhanced binoculars and convoy vehicle automated protection systems.
  - d. OIDA
  - e. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/artificial\\_vision\\_systems/](http://www.oida.org/home/publications/oida_publication_report_library/artificial_vision_systems/)
- 107) Workshop: Silicon Photonics: Challenges and Future, 2007
- a. 2007
  - b. Workshop chairman and editor of the report:
  - c. Abstract: Copper interconnects are currently used extensively within the data center environment. Fiber optic technology is used as a connectivity solution when higher performance is required and the cost differential compared to a copper solution is affordable. Fiber optic technology offers several key advantages over copper solutions for data transmission. This report looks at silicon photonics as a potential optical interconnect solution and addresses the issues and technology paths being pursued.
  - d. OIDA
  - e. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/silicon\\_photonics\\_challenges\\_and\\_future\\_2007/](http://www.oida.org/home/publications/oida_publication_report_library/silicon_photonics_challenges_and_future_2007/)
- 108) Invited talk/plenary: High-Performance Datacenter Platform: Using InP for Silicon Photonics
- a. 8/1/2014
  - b. IEEE-CPMT/Photonics Society local chapter meeting, Santa Clara, California
  - c. <http://www.cpmpt.org/scv/meetings/cpmpt1401.html>
- 109) Paper: ORMOCERs - new photo-patternable dielectric and optical materials for MCM-packaging
- a. 01/1998
  - b. Hybrid inorganic-organic polymers (ORMOCERs\*) have been developed and tested in an ongoing EU-program (BE 7250 DONDOMCM) for evaluation in MCM applications. The photopatternable materials with negative resist behavior are composed of inorganic oxidic structures cross-linked or substituted by organic groups. They are prepared from organosilane precursors by sol-gel-



processing in combination with organic crosslinking of polymerizable organic functions. As a result of these functionalities the properties of the ORMOCERs can be adjusted to particular applications. Systematic variation of composition combined with adaptation to micro system technology allows great flexibility in processing. Some features of these materials are: Postbaking at moderate temperatures (120 °C - 180 °C) enables processing on substrates such as FR-4 and BT. Combined use as dielectric and passivation layers in electrical systems and devices as well as core and cladding for optical applications enables e/o applications with high integration levels. Easily adaptable to thin film technology: spin-on with planarization >90% and via diameters down to 20 µm have been achieved

- c. Proceedings of the 1998 48th Electronic Components and Technology Conference
  - d. <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?reload=true&arnumber=678838&contentType=Conference+Publications>
- 110) Technical Advisor/Expert: 2nd review of PI-SCALE project pilot line funded by H2020, European Commission
- a. 21/2/2017
  - b. 2nd review of PI-SCALE consortium pilot line at European Commission, Brussels
  - c. European Commission, Brussels, Belgium
  - d. <http://pi-scale.eu>
- 111) Short Article: President's Letter to OIDA Membership
- a. 11/2005
  - b. OIDA Newsletter, quarterly from 2005-2009
  - c. [http://www.wsr-ods.com/files/oidanews\\_0408.pdf](http://www.wsr-ods.com/files/oidanews_0408.pdf)
- 112) Workshop: Photonic Sensors Roadmapping Report, 2007
- a. 2007
  - b. Workshop chairman and editor of the report:
  - c. Abstract: This OIDA workshop report examines application specific sensor needs for both the government and the private sector with an emphasis on the oil and gas market, sensing function integration, cost reduction opportunities, and barriers and competing technologies.
  - d. OIDA
  - e. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/photonic\\_sensors\\_roadmapping\\_report\\_2007/](http://www.oida.org/home/publications/oida_publication_report_library/photonic_sensors_roadmapping_report_2007/)
- 113) Paper: A low-cost high-performance optical interconnect
- a. 08/1996
  - b. The Optobus™ link is a ten channel parallel bidirectional data link based on multimode fiber ribbons. The guiding principal of the Optobus™ design was to produce an optical interconnect capable of competing with copper on price, not just performance. Recognizing that packaging dominates the cost of optical interconnects, the design focused on minimizing the complexity of the optical subassembly. A key component of this strategy is the use of AlGaAs/GaAs vertical cavity surface emitting lasers (VCSELs). Another is designing the silicon receiver and transmitter arrays around the module level packaging parasitics. The

- resulting parallel transceiver modules achieve a minimum throughput of 1.5 Gb/s in each direction with a power dissipation of 1.6 W
- c. Components, Packaging, and Manufacturing Technology, Part B: Advanced Packaging, IEEE Transactions on Volume: 19 , Issue: 3 Page(s): 532- 539
  - d. <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=533892>
- 114) Workshop: Micropackaging for the Next Generation of Optical and Electrical Components
- a. 2007
  - b. Workshop chairman and editor of the report:
  - c. Abstract: Optical components are ubiquitous. Applications that use them include DVD players, audio devices, cell phones, re-writable drives, projection displays, and communication devices. This report concentrates on the role of micropackaging for the for next generation fiber optic components with an eye towards lower cost and higher volume.
  - d. OIDA
  - e. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/micropackaging\\_for\\_the\\_next\\_generation\\_of\\_optical/](http://www.oida.org/home/publications/oida_publication_report_library/micropackaging_for_the_next_generation_of_optical/)
- 115) Paper: ORMOCERs(TM)-new photo-patternable dielectric and optical materials for MCM-packaging
- a. 05/1998
  - b. Hybrid inorganic-organic polymers (ORMOCERs\*) have been developed and tested in an ongoing EU-program (BE 7250 DONDOMCM) for evaluation in MCM applications. The photo-pattemable materials with negative resist behavior are composed of inorganic oxidic structures cross-linked or substituted by organic groups. They are prepared from organosilane precursors by sol-gel-processing in combination with organic crosslinking of polymerizable organic functions. As a result of these functionalities the properties of the ORMOCERs can be adjusted to particular applications. Systematic variation of composition combined with adaptation to micro system technology allows great flexibility in processing. Some features of these materials are: Post baking at moderate temperatures (120 °C - 180 °C) enables processing on substrates such as FR-4 and BT. Combined use as dielectric and passivation layers in electrical systems and devices as well as core and cladding for optical applications enables e/o applications with high integration levels. Easily adaptable to thin film technology: spin-on with planarization >90% and via diameters down to 20 µm have been achieved
  - c. 1998 Proceedings. 48th Electronic Components and Technology Conference
  - d. <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?reload=true&arnumber=678838&contentType=Conference+Publications>
- 116) Invited talk/plenary: Next generation ICs using photonics integration
- a. 10/12/2013
  - b. Talk that reviews OneChip Photonics technology and in general PICs, OEICs, Silicon photonics, and how these technologies play into datacenters (data centers) for client side high speed 100G fiber (fibre) optic transceiver interconnects and cabling.
  - c. IQE Capital markets day, Sky Pavillion, Rothschild Building, London, UK

- d. <http://www.euroinvestor.com/news/2013/12/10/iqe-plc-capital-markets-day/12617916>
- 117) Workshop: 100 Gbit Interconnects and Above: The Need for Speed
  - a. 1/5/2007
  - b. Workshop chairman and editor of the report:
  - c. Abstract: The electronic society we live in today is seeing increased demand for data transfer, internet downloads, online applications, video sharing and storage. The electronic world of banks, companies, universities and governments require large secure datacenters connected to secure networks. This continuously drives for the development of more powerful servers and computer systems. This report examines needs and motivations for optical interconnect implementation. Looks at the applications, history, market drivers, and future issues that affect this crossover.
  - d. OIDA
  - e. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/100\\_gb\\_ethernet\\_the\\_next\\_challenge\\_for\\_communicati/](http://www.oida.org/home/publications/oida_publication_report_library/100_gb_ethernet_the_next_challenge_for_communicati/)
- 118) Paper: VCSEL devices and packaging
  - a. 12/1998
  - b. Proceedings of SPIE, ISSN 0277-786X, 05/2003, Volume 3289, Issue 1
  - c. <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=935769>
- 119) Workshop: Perspectives on the Optoelectronics Industry: Manufacturing in the 21st Century, 2008
  - a. 2008
  - b. Workshop chairman and editor of the report:
  - c. Abstract: This report provides insight and perspectives by senior-level representatives from industry on global trade and manufacturing practices in the field of optoelectronics. Three areas examined are: 1) Can automation or optical integration relieve the momentum to outsource and off-shore manufacturing from North America? 2) The supply chain and the economics of manufacturing in the U.S., Europe, and Asia, and 3) The implications of offshore manufacturing on both the U.S. defense and commercial market sectors within the different fields of optoelectronics.
  - d. OIDA
  - e. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/perspectives\\_on\\_the\\_optoelectronics\\_industry\\_manuf/](http://www.oida.org/home/publications/oida_publication_report_library/perspectives_on_the_optoelectronics_industry_manuf/)
- 120) Workshop: Perspectives on the Optoelectronics Industry: Innovation, 2008
  - a. 2008
  - b. Workshop chairman and editor of the report: Abstract: This report documents some of the issues raised at the Optoelectronics Industry Development Association (OIDA) forum and provides a review on the critical issue of innovation in the U.S. and the impact it has on future American competitiveness and technology leadership. This report looks at innovation and R&D from many perspectives: global, business, university, government funding agencies.
  - c. OIDA
  - d. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/perspectives\\_on\\_the\\_optoelectronics\\_industry\\_innov/](http://www.oida.org/home/publications/oida_publication_report_library/perspectives_on_the_optoelectronics_industry_innov/)

- 121) Technical Advisor/Expert: 1st review of PIXAPP pilot line consortium funded by H2020 at European Commission
  - a. 21/2/2017
  - b. 1st Review of Pixapp project at EU Commission as part of the pilot line project.
  - c. European Commission, Brussels
  - d. <http://www.fabiodisconzi.com/open-h2020/projects/206352/index.html>
- 122) Invited talk and Chair panel session: EPIC workshop on photonic integrated circuits; "Global integrated photonics update and roadmaps"
  - a. 9/6/2015
  - b. "Invited talk: Global integrated photonics update and roadmaps
  - c. Panel Session: Integrated photonics foundry status
  - d. EPIC trade association, Europe
  - e. <http://www.epic-assoc.com/epic-workshop-on-photonic-integrated-circuits/>
- 123) Paper: Epitaxial Si and Gd<sub>2</sub>O<sub>3</sub> Heterostructures - Distributed Bragg Reflectors with Stress Management Function for GaN on Si Light Emitting Devices
  - a. 1/10/2012
  - b. ECS J. Solid State Sci. Technol. 1, 246 (2012)
  - c. <http://jss.ecsdl.org/content/1/5/P246.full>
- 124) Invited Talk: Lightwave Logic Inc Annual Shareholder Meeting "High Performance Polymer Photonics for Next Generation PICs"
  - a. 18/5/2017
  - b. Presentation of corporate technology and strategy for Lightwave Logic Inc and polymer PIC platforms.
  - c. Lightwave Logic Inc (OTCQB:LWLG)
  - d. <http://www.lightwavelogic.com/presentations>
- 125) Course and Tutorial: Optoelectronic Devices and Packaging: VCSEL Technology
  - a. 01/1998
  - b. "Optoelectronic devices and packaging have found increasing use in many new products over the last 20 Yrs. This tutorial primarily will focus on semiconductor laser based technology with particular emphasis on emerging new technologies such as the Vertical Cavity Surface Emitting Laser (VCSEL) and how to take advantage of its uniqueness in packaging. The tutorial will look at the driving factors required for low cost high volume VCSEL based packages and what impact they will have in tomorrow's products. As there are many packaging solutions for VCSEL based technology proposed, the course will show the relative merits of popular new technologies with respect to high volume and low cost manufacturing.
  - c. 4th IEEE Workshop on AST Phoenix Research Center
  - d. <http://www.ewh.ieee.org/soc/cpmt/ast98/lebby-01.ppt>
- 126) Invited talk/Panel session: InP based photonics integration platform for datacenter and coherent communications
  - a. 4/2/2014
  - b. Invited talk/panel session on the future of integrated photonics. Discussion was on both InP and silicon photonics technologies over the next decade.

- c. Workshop on the future of Integrated Photonics organized by the Netherlands Office for Science & Technology is pleased to invite you to a workshop, occurring In conjunction with the upcoming Photonics West conference
- d. <http://www.hollandinthevalley.com/panel-discussion-on-the-future-of-integrated-photonics/>
- 127) Paper: An n-channel BICFET in the InGaAs/InAlGaAs/InAlAs material system
  - a. 1989
  - b. "Electron Device Letters, IEEE Volume: 10 , Issue: 7 Digital Object Identifier: 10.1109/55.29660 Publication Year: 1989 , Page(s): 304 - 306"
  - c. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=29660&tag=1>
- 128) Workshop: Perspectives on the Optoelectronics Industry, 2008
  - a. 2008
  - b. Workshop chairman and editor of the report:
  - c. Abstract: The United States is falling behind in the manufacturing, packaging, and assembling of optoelectronics products. Innovating technology may also be imperiled. This report is the result of the first of three optoelectronic forums sponsored by the Defense Advanced Research Projects Agency (DARPA), This report details the trends, findings, and directions for optoelectronics in each of these market applications. Included in the first chapter of this report is the global optoelectronics summary that was compiled by OIDA in 2007.
  - d. OIDA
  - e. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/perspectives\\_on\\_the\\_optoelectronics\\_industry\\_2008/](http://www.oida.org/home/publications/oida_publication_report_library/perspectives_on_the_optoelectronics_industry_2008/)
- 129) Workshop: Future Optical Communication Systems, 2008
  - a. 2008
  - b. Workshop chairman and editor of the report:
  - c. Abstract: This report examines future optical communication needs and technologies. Topics include: Networks, Core, Metro, and Access Technology, photonic integration, and markets.
  - d. OIDA
  - e. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/future\\_optical\\_communication\\_systems\\_2008/](http://www.oida.org/home/publications/oida_publication_report_library/future_optical_communication_systems_2008/)
- 130) Workshop: Green Photonics: The Role of Optoelectronics in a Sustainable Future, 2009
  - a. 2009
  - b. Workshop chairman and editor of the report:
  - c. Abstract: This report explores the optoelectronics expectations for green photonics technology, and forecasts the associated markets through 2020. The cultural impact for a green, clean, and energy efficient lifestyle is just beginning. Over the next decade, many innovative new products will emerge in a variety of industries that will better define and demonstrate green photonics technology. It is clear to many that a broad range of products and services that the economy will utilize over the next decade will contain optoelectronics (interchangeable with the term photonics), either as key components or as components that enable better and more efficient systems.
  - d. OIDA

- e. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/green\\_photonics\\_the\\_role\\_of\\_optoelectronics\\_in\\_a\\_s/](http://www.oida.org/home/publications/oida_publication_report_library/green_photonics_the_role_of_optoelectronics_in_a_s/)
- 131) Paper: Automatic power control of a VCSEL using an angled lid TO56 package
  - a. 05/1998
  - b. 1998 Proceedings. 48th Electronic Components and Technology Conference
  - c. <http://ieeexplore.ieee.org/xpl/login.jsp?tp=&arnumber=678694&url=http%3A%2F%2Fieeexplore.ieee.org%2Fiel4%2F5582%2F14953%2F00678694.pdf%3Farnumber%3D678694>
- 132) Workshop: Fabrication Challenges and Opportunities in Photonics, 2010
  - a. 2010
  - b. Workshop chairman and editor of the report: Abstract: This report examines different operational models employed by industry (fabless, fab-lite, pure play foundry and vertically integrated companies), and the role of governments in stimulating the growth of the photonics industry.
  - c. OIDA
  - d. [http://www.oida.org/home/publications/oida\\_publication\\_report\\_library/fabrication\\_challenges\\_and\\_opportunities\\_in\\_photonics/](http://www.oida.org/home/publications/oida_publication_report_library/fabrication_challenges_and_opportunities_in_photonics/)
- 133) Conference: Optimism: "Powering the green revolution through photonics"
  - a. 1/4/2009
  - b. "Co-chairman of Optimism conference with Pennwell.
  - c. OIDA and Pennwell (Laser Focus World)
  - d. <http://www.laserfocusworld.com/articles/print/volume-45/issue-4/world-news/conference-preview-optimism-to-emphasize-lsquoogreenrsquo-growth.html>
- 134) Paper: Characteristics of VCSELs and VCSEL arrays for optical data links
  - a. 02/1997
  - b. Proc. SPIE 3004, Fabrication, Testing, and Reliability of Semiconductor Lasers II, 122 (May 1, 1997); doi:10.1117/12.273825
  - c. <http://proceedings.spiedigitallibrary.org/proceeding.aspx?articleid=918720>
- 135) Paper: Epitaxial Si, SiGe and Ge on binary and ternary rare earth oxide buffers
  - a. 2012
  - b. Phys. Status Solidi C 9, 2031 (2012)
  - c. <http://onlinelibrary.wiley.com/doi/10.1002/pssc.201200255/abstract>
- 136) Paper: Epitaxial Si and Gd2O3 Heterostructures - Distributed Bragg Reflectors with Stress Management Function for GaN on Si Light Emitting Devices
  - a. 2013
  - b. ECS Trans 2013 volume 50, issue 4, 47-52
  - c. <http://ecst.ecsdl.org/content/50/4/47.short>
- 137) Keynote talk: Photonic integration in InP: A regrowth-free platform for fabless manufacturing model
  - a. 19/3/2014
  - b. CS International Conference Frankfurt, March 17th-20th 2014
  - c. <http://cs-international.net/agenda.php>
- 138) Paper: An Inversion Channel Technology For Opto-Electronic Integration
  - a. 8/2/1989
  - b. A new approach to optoelectronic integration is reported which combines electronic and optical devices fabricated with a common sequence and a single



- MBE wafer growth. The devices have in common, an inversion layer structure produced by charge sheet doping.
- c. Proceedings Vol. 0994 Optoelectronic Materials, Devices, Packaging, and Interconnects II, Glen M. McWright; Henry J. Wojtunik, Editors, pp.251-510  
Date: 9 February 1989 ISBN: 9780819400291
  - d. [http://spie.org/x648.html?product\\_id=960136](http://spie.org/x648.html?product_id=960136)
- 139) Invited talk/Panel session "Optical interconnect in datacenters"
- a. 18/3/2014
  - b. "The 1st Optical Interconnect in Data Centers Symposium takes place on the 18th and 19th of March 2014 in Berlin/ Germany.
  - c. It is focused on high-performance, low-energy and low-cost and small-size optical interconnects across the different hierarchy levels in data center and high-performance computing systems: on-board, board-to-board and rack-to-rack.
  - d. EPIC: Symposium on optical interconnect in datacenters
  - e. <http://www.phoxtrot.eu/1st-optical-interconnect-in-data-centers-symposium/>
- 140) Conference and workshop: 3rd Annual Green Photonics Forum (OIDA Green 2010)
- a. 10/6/2010
  - b. Conference chairman: OIDA's innovative green photonics forums have become a focal point for photonics and optics in the area of sustainable energy. The annual forum on green photonics, brings together key players involved in developing the technical and business roles of photonics in building a more sustainable and renewable future. Efficiency, monitoring, and energy generation are areas where photonics technology will play a key role and the photonics industry will deliver solutions.
  - c. OIDA
  - d. <http://www.clocate.com/conference/3rd-Annual-Green-Photonics-Forum-OIDA-Green-2010/4045/>
- 141) Invited talk, short abstract, and session chairman: Energy Efficient Photonics
- a. 19/3/2009
  - b. Summary: Green photonics initiatives: The role of optoelectronics in a sustainable future...
  - c. European Commission: High Level Event on ICT for Energy Efficiency
  - d. [http://ec.europa.eu/information\\_society/events/cf/ee09/item-display.cfm?id=2174](http://ec.europa.eu/information_society/events/cf/ee09/item-display.cfm?id=2174)
- 142) Paper: Vertical cavity surface emitting laser packaging with auto power control
- a. 05/1997
  - b. Proceedings, 47th Electronic Components and Technology Conference, pp. 368-370, May 1007
  - c. [http://www.researchgate.net/publication/3700010\\_Vertical\\_cavity\\_surface\\_emitting\\_laser\\_packaging\\_with\\_auto\\_powercontrol](http://www.researchgate.net/publication/3700010_Vertical_cavity_surface_emitting_laser_packaging_with_auto_powercontrol)
- 143) Invited presentation for Day of Photonics at Glyndwr University: Photonics - markets, applications, integrated, next generation IC
- a. 21/10/2014
  - b. Invited presentation/lecture on photonics at the Glyndwr University.
  - c. Welsh Optoelectronic Forum (WOF)
  - d. [http://www.wof.org.uk/home.php?page\\_id=4&event\\_id=317](http://www.wof.org.uk/home.php?page_id=4&event_id=317)

Declaration of Dr. Lebby  
IPR2020-00512 (U.S. Patent No. 9,186,052)

- 144) Paper: Reactive ion etching (RIE) and magnetron ion etching (MIE) combinations for opto-electronic integrated circuit (OEIC) processing
  - a. 11/1988
  - b. Proc. SPIE Vol. 1037, p. 88, Monitoring and Control of Plasma-Enhanced Processing of Semiconductors, James E. Griffiths; Ed.
  - c. [http://spie.org/x648.html?product\\_id=951018](http://spie.org/x648.html?product_id=951018)
- 145) Paper: Scalable GaN-on-Silicon using rare earth oxide buffer layers
  - a. 9/10/2012
  - b. ECS Trans 2013 volume 50, issue 9, 1065-1071
  - c. <http://ma.ecsdl.org/content/MA2012-02/30/2538.short>
- 146) Video and presentation: Green Photonics: Will it Change our Lives over the Next Decade?
  - a. 04/2010
  - b. Photonics is growing to enable new green technologies and products. Photonics already has a large presence in various modules and components with opportunities to expand to home displays, solar cells, lighting, and various consumer applications. The global optoelectronics industry has a strong outlook for growth in the near future, with even faster growth in green photonics. Green photonics can help reduce greenhouse gas emissions, generate or conserve energy, reduce pollution, and improve human health.
  - c. University of California, Santa Barbara: Institute of Energy Efficiency
  - d. <http://iee.ucsb.edu/node/1024>
- 147) Invited Talk and Panelist: Emerging Technologies Summit; Integrated Photonics session, Stanford University, as part of the Kingdom of the Netherlands trade mission to Silicon Valley
  - a. 10/1/2017
  - b. "Discussion with HRH Prince Constantijn and DG Bertolt Loeffink about photonics ecosystem and startups. Photonics highlights (Michael Lebby)
  - c. Consulate General San Francisco, The Kingdom of Netherlands
  - d. <https://ez.atavist.com/emerging-technologies-summit>
- 148) Invited talk and abstract: Coherent Receiver Chip for 100G DP-QPSK
  - a. 30/4/2014
  - b. SIOE (Semiconductor and integrated optoelectronics) Conference, Cardiff, Wales, UK 29th April-1st May 2014, Institute of Physics
  - c. <http://www.astro.cardiff.ac.uk/research/cmp/events/resources/Sioeprogramme14final.pdf>
- 149) Invited Talk: Annual Shareholder Meeting 2016 - Market Perspective LWLG Polymer Photonics vs Legacy Devices
  - a. 20/5/2016
  - b. Presentation to investor group at Lightwave Logic's Annual Shareholder Meeting  
Lightwave Logic
  - c. <http://lightwavelogic.com/company-updates/>
- 150) Project advisor: European Commission ICT-28-2015 Cross-Cutting ICT KETs: Innovation Action (b) Pilot line for OLEDs on flexible substrates
  - a. 20/9/2015
  - b. European Commission



- c. <http://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020/topics/916-ict-28-2015.html>
- 151) Invited talk: Compound Semiconductors (CS) driving photonics
  - a. 11/6/2014
  - b. Invited presentation for Welsh Gvt and commercial industry in epitaxial growth. The talk covered photonics: global markets, green photonics, photonics technology sectors (lighting, solar, displays, sensors, communications), integrated photonics and silicon photonics. Commercial industry invite by International Quantum Epitaxy (IQE)
  - c. Growth and application of epitaxial heterostructures with polymorphous rare earth oxides
  - d. Journal of Crystal Growth
  - e. <http://www.sciencedirect.com/science/article/pii/S0022024812009487>
- 152) Engineering of the Interface Between Silicon and Rare-Earth Oxide Buffer for GaN growth
  - a. 09/2012
  - b. ECS Meeting Oct 2013, San Francisco, USA
  - c. [http://scholar.googleusercontent.com/scholar?q=cache:l3-oHWxNDzwJ:scholar.google.com/+%22michael+lebby%22&hl=en&as\\_sdt=1,5&as\\_ylo=2013&as\\_vis=1](http://scholar.googleusercontent.com/scholar?q=cache:l3-oHWxNDzwJ:scholar.google.com/+%22michael+lebby%22&hl=en&as_sdt=1,5&as_ylo=2013&as_vis=1)
- 153) Paper: Parallel interconnect for a novel system approach to short distance high information transfer data links
  - a. 04/1997
  - b. Proceedings of SPIE, ISSN 0277-786X, 04/1997, Volume 3038, Issue 1
  - c. <http://www.deepdyve.com/lp/spie/parallel-interconnect-for-a-novel-system-approach-to-short-distance-RFreDaEJjb>
- 154) Abstract and conference invited talk: The case for a photonics foundry in USA
  - a. 27/4/2007
  - b. European Conference on Integrated Optics (2007): Towards foundries for photonic ICs
  - c. <http://www.epixnet.org/index.php?id=393>
- 155) Scalable virtual Ge templates for III-V integration on Si wafers
  - a. 18/4/2012
  - b. AIP Conference Proceedings / Volume 1477 / CONCENTRATOR SOLAR CELLS, CELL ASSEMBLIES AND RELATED MATERIALS
  - c. [http://proceedings.aip.org/resource/2/apcpcs/1477/1/36\\_1?bypassSSO=1](http://proceedings.aip.org/resource/2/apcpcs/1477/1/36_1?bypassSSO=1)
- 156) Video presentation: Living at the speed of light
  - a. 10/12/2009
  - b. Living at the speed of light, hosted by renown physicist Michael Lebby, takes us on a fast paced fly through of the many facets of photonics and how the use of light touches the many aspects of our lives
  - c. National Research Council: Canadian Photonics Fabrication Centre
  - d. <http://www.youtube.com/watch?v=t8EB-1-lirY>
- 157) Keynote address: Global perspectives in optoelectronics and photonics
  - a. 6/12/2006
  - b. Photonics 21: European Union's 7th Framework Program Key Photonics Platform

- b. Integrated Photonics Institute for Manufacturing Innovation (IP-IMI) site visit technical review:
- c. The University of Southern California's (USC) Information Sciences Institute (ISI) is leading an effort with partner universities at the University of California-Los Angeles (UCLA), the University of California-Berkeley (UCB), the University of California-San Diego (UCSD), Arizona State University, the University of New Mexico, and the Ohio State University, as well as numerous industry partners, to develop the only California-based and led proposal to compete for the IP-IMI award. If successful, the proposal will receive a federal award of up to \$110 million over five years. A successful proposal requires 100

- percent or more in matching funds (cash or in-kind) from state and local governments and from industry partners.
- d. IPI-CDMS (Integrated Photonics Institute and Center for Design and Manufacturing Services)
  - e. <http://www.isi.edu/news/story/531784>
- 161) Video interview: World Photonic Mapping Forum; s'Hertogenbosch, Netherlands
- a. 15/6/2017
  - b. Interview on photonics roadmaps.
  - c. PhotonDelta (via Videographer Jonathan Marks)
  - d. <https://worldtechnologymappingforum.org/the-programme>
- 162) Paper: Relative intensity noise of 780nm vertical cavity surface emitting lasers
- a. 01/1997
  - b. Proceedings of the 1997 Pacific Rim Conference on Lasers and Electro-Optics, CLEO/Pacific Rim, No 46984, Jan 1997
  - c. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=610586>
- 163) Invited Presentation and abstract: "High-Performance Polymer Photonics for Next-Generation Photonic Integrated Circuits"
- a. 3/10/2016
  - b. ECOC Market Focus by ECOC Exhibition
  - c. <http://www.ecocexhibition.com/marketfocus>
- 164) Paper: Effect of proton implantation on the degradation of GaAs/AlGaAs vertical cavity surface emitting lasers
- a. 1997
  - b. Electronics Letters, ISSN 0013-5194, 1997, Volume 33, Issue 2, p. 137
  - c. <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?arnumber=579434>
- 165) Invited Talk: Photonics Integration Circuits - Global Market Analysis 2017
- a. 13/3/2017
  - b. Invite by The Netherlands Department of Economics to review PIC technology and markets for potential investment.
  - c. The Dutch Government - Dept of Economics, The Hague together with Photon Delta, The Netherlands
  - d. <http://www.photondelta.eu>
- 166) Invited Talk: Belgium LWLG Investor Group at the Royal Antwerp Golf Club
- a. 6/3/2017
  - b. Invited talk entitled "High performance polymer photonics for next generation PICs"
  - c. Belgium LWLG Investor Group
  - d. <http://www.lightwavelogic.com>
- 167) Paper: Optical bistability in vertical cavity surface emitting lasers with a simple intra-cavity epitaxial absorber layer
- a. 4/10/1998
  - b. Conference Digest: Semiconductor Laser Conference, 1998. ISLC 1998 NARA. 1998 IEEE 16th International
- 168) Course (peer reviewed): "Optoelectronic devices and packaging"
- a. 05/1997
  - b. IEEE ECTC

- c. <http://www.ectc.net>
- 169) Course (peer reviewed): "Optoelectronic devices and packaging: VCSEL technology"
  - a. 05/1998
  - b. IEEE ECTC
  - c. <http://www.ectc.net>
  - d.
- 170) Course (peer reviewed): "Optoelectronic devices and packaging: VCSEL and edge emitter technology"
  - a. 05/1999
  - b. IEEE Electronics and components technology conference; San Diego, California
  - c. <http://www.ectc.net>
- 171) Plenary Talk: Global Market Research at the World Technology Mapping Forum, s'Hertogenbosch, Netherlands
  - a. 14/6/2017
  - b. "PhotonDelta and the AIM Photonics Academy are organising the first meeting of the World Technology Mapping Forum. The goal of the forum is to produce the first International Photonic Systems Roadmap, looking ahead to global technology needs in 2030 and beyond.
  - c. PhotonDelta, Netherlands as part of the International Photonics System Roadmap (IPSR) conference
  - d. <https://worldtechnologymappingforum.org/the-programme>
- 172) Paper: Rare-earth-metal oxide buffer for epitaxial growth of single crystal GeSi and Ge on Si(111)
  - a. 1/3/2012
  - b. Conference and journal publication."Rare-earth-metal oxide buffer for epitaxial growth of single crystal GeSi and Ge on Si(111)"
  - c. With publication details: 28th North American Molecular Beam Epitaxy Conference, Published by AVS through the American Institute of Physics, 2012 ISBN 978-0-9836933-0-7 ISSN: 2166-27646 J.Vac.Sci.Technol B 30(2), Mar/Apr 2012 pp02B110-1 to pp-3B110-6
  - d. <http://ieeexplore.ieee.org/xpl/articleDetails.jsp?reload=true&arnumber=6118290&contentType=Journals+%26+Magazines>
- 173) Invited talk and abstract: Vertical cavity surface emitting lasers and applications
  - a. 09/1997
  - b. European Laser Workshop, Glasgow, Scotland
- 174) Invited talk and abstract: VCSEL Transceiver technology
  - a. 09/1998
  - b. European Laser Workshop, Madrid, Spain
- 175) Press interview: "Building Big Business with the Next Generation Integrated Circuits!"
  - a. 15/9/2015
  - b. "Insights from Michael Lebby, CEO OneChip Photonics Corporation, the keynote speaker at the Photonics Integration Conference
  - c. Photonics Integration Conference, organized by Jakajima, Netherlands

- d. <http://www.phiconference.com/photronics/building-big-business-with-the-next-generation-integrated-circuits/>
- 176) Chairman: PIC (Photonic Integrated Circuits) International Conference, Brussels, Belgium
  - a. 7/3/2017
  - b. "Photonic Integrated Circuits International
  - c. CS International
  - d. <http://www.picinternational.net>
- 177) Paper (invited): Laser safety issues with VCSEL arrays in OPTOBUS(tm)
  - a. 1997
  - b. Optical Society of America (OSA); Annual Meeting, Micro-optics session
- 178) Paper and Interviewed Article: Commercial VCSEL Manufacturing
  - a. 04/1999
  - b. Compound Semiconductor
- 179) Invited talk and abstract: Vertical cavity surface emitting lasers for communication applications
  - a. 10/1996
  - b. Optical Society of America (OSA) Annual meetings, proceedings, paper WR1, Rochester, NY
- 180) Paper: Structural and Thermal Properties of Single Crystalline Epitaxial Gd<sub>2</sub>O<sub>3</sub> and Er<sub>2</sub>O<sub>3</sub> Grown on Si(111)
  - a. 2012
  - b. ECS Journal of Solid State Science and Technology 1, N24 (2012)
  - c. <http://jss.ecsdl.org/content/1/2/N24.full.pdf+html>
- 181) Invited talk and abstract: VCSEL Arrays and GUIDECAST(tm) packaging technology as used in OPTOBUS(tm)
  - a. 09/1995
  - b. European Laser Workshop, Eindhoven, Netherlands
- 182) Invited talk and abstract: Ridge Waveguide and Planar VCSEL Device Reliability
  - a. 09/1996
  - b. European Laser Workshop, Oslo, Norway
- 183) Paper: An n-channel BICFET in the GaAs/AlGaAs material system
  - a. 02/1989
  - b. "Electron Device Letters, IEEE Volume: 10, Issue: 2 Digital Object Identifier: 10.1109/55.32438 Publication Year: 1989 , Page(s): 88 - 90"
  - c. <http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&arnumber=32438&tag=1>
- 184) Book chapter: "Optical sources: Light-emitting diodes and laser technology"
  - a. 02/2002
  - b. "The Handbook includes chapters on all the major industry standards, quick reference tables, helpful appendices, plus a new glossary and list of acronyms. This practical handbook can stand alone or as a companion volume to DeCusatis: Fiber Optic Data Communication: Technological Advances and Trends (February 2002, ISBN: 0-12-207892-6), which was developed in tandem with this book.
  - c. Academic Press (1998, 2002); ISBN: 0-12-207892-6; Handbook of Fiber Optic Data Communication By Casimer DeCusatis

- d. [http://books.google.com/books?id=Rlb61KknI8IC&printsec=frontcover&source=gbs\\_ge\\_summary\\_r&cad=0#v=onepage&q&f=false](http://books.google.com/books?id=Rlb61KknI8IC&printsec=frontcover&source=gbs_ge_summary_r&cad=0#v=onepage&q&f=false)
- 185) Book chapter: "Semiconductor laser and light emitting diode fabrication"
  - a. 2002
  - b. "The Handbook includes chapters on all the major industry standards, quick reference tables, helpful appendices, plus a new glossary and list of acronyms. This practical handbook can stand alone or as a companion volume to DeCusatis: Fiber Optic Data Communication: Technological Advances and Trends (February 2002, ISBN: 0-12-207892-6), which was developed in tandem with this book.
  - c. Academic Press: Editor DeCusatis: Fiber Optic Data Communication: Technological Advances and Trends (February 2002, ISBN: 0-12-207892-6)
  - d. <http://books.google.com/books?id=Rlb61KknI8IC&lpg=PP1&pg=PP1#v=onepage&q&f=false>
- 186) Invited talk and abstract: Ridge waveguide VCSEL device performance
  - a. 05/1995
  - b. USA Laser workshop, CLEO, Anaheim, California
- 187) Keynote speech: Next decade in fiber optic communications
  - a. 30/4/2001
  - b. Electrocast: 13th Annual Fiber Optics for the Next Decade Conference
  - c. <http://www.photonics.com/Article.aspx?AID=8916>
- 188) Reviewer: European Commission ICT-29-2016: Photonics KET 2016 (section a(ii) Breakthrough in miniaturization of SSL light engines and systems)
  - a. 11/5/2016
  - b. European Commission: Reviewing submitted technical photonics proposals for Horizon 2020, and rate proposals to EU guidelines.
  - c. <http://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020/topics/5094-ict-29-2016.html>
- 189) Invited talk and abstract: Polymer based PICs
  - a. 9/14/2017
  - b. ECOC, Datacenter technologies. Sweden
- 190) Video: Polymer based PICs
  - a. 9/15/2017 ECOC, Sweden as part of Market Focus at the ECOC Exhibit. (youtube: Michael Lebby ECOC 2017)
- 191) Keynote invited talk and abstract: PIC based technologies
  - a. 9/22/2017
  - b. PIC Conference, The Netherlands
- 192) Invited talk and abstract: Polymer PIC technology as part of the Photonics Integrated Circuits (PIC) conference in Eindhoven, Netherlands.
  - a. 10/5/2017
  - b. PIC technologies and polymer photonics
- 193) Invited talk: PIC Training conference/workshop in Sunnyvale, Silicon Valley
  - a. PIC training session/workshop
- 194) Invited talk: Photonics Pilot Lines
  - a. 12/8/2017
  - b. European Commission, Photonics Proposers Meeting, Brussels
- 195) International Roadmap meeting at Berenshot, Utrecht, Netherlands

- a. 1/20 2018
- b. Invited talk: International Roadmap meeting: Datacom/Telecom ICT markets, AOC, and Polymer PIC technology platforms
- 196) Co-Chairman: PIC (Photonic Integrated Circuits), International Conference, Brussels, Belgium
  - a. 10/4/2018
  - b. Photonic Integrated Circuits International
  - c. CS International
  - d. <http://www.picinternational.net>
- 197) Session chair and moderator: High volume, high performance PICs (Photonic Integrated Circuits) at the International Conference, Brussels, Belgium
  - a. 10/4/2018
  - b. Photonic Integrated Circuits International
  - c. CS International
  - d. <http://www.picinternational.net>
- 198) Session chair and moderator: Silicon Photonics (SiP) PICs (Photonic Integrated Circuits) at the International Conference, Brussels, Belgium
  - a. 11/4/2018
  - b. Photonic Integrated Circuits International
  - c. CS International
  - d. <http://www.picinternational.net>
- 199) Invited Talk: Scalable PIC platforms: “The impact of using polymer PICs for 100 and 400Gbps datacom applications,” PICs (Photonic Integrated Circuits) at the International Conference, Brussels, Belgium
  - a. 10/4/2018
  - b. Photonic Integrated Circuits International
  - c. CS International
  - d. <http://www.picinternational.net>
- 200) Workgroup chair and moderator: Telecom, Datacom, and ICT roadmap committee at the International world mapping conference, Enschede, Netherlands
  - a. 20<sup>th</sup> June 2018
  - b. Photondelta Conference: chairing technical workgroup meetings to address photonics roadmap trends and challenges.
  - c. Photondelta in coordination with iNEMI, and AIM photonics.
  - d. <https://www.photondelta.eu>
- 201) Workgroup chair and moderator: Telecom long haul roadmap committee at the International world mapping conference, Enschede, Netherlands
  - a. 20<sup>th</sup> June 2018
  - b. Photondelta Conference: chairing technical workgroup meetings to address photonics roadmap trends and challenges.
  - c. Photondelta in coordination with iNEMI, and AIM photonics.
  - d. <https://www.photondelta.eu>
- 202) Reviewer: European Commission ICT-03-2018: Photonics Pilot lines (InP and silicon photonics PICs)
  - a. 11<sup>th</sup> June 2018



- b. European Commission: Reviewing submitted technical photonics proposals for Horizon 2020, and rate proposals to EU guidelines.
- c. <http://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020>
- 203) Reviewer: European Commission ICT-04-2018: Tbps optical fiber optic transceivers
  - a. 11<sup>th</sup> June 2018
  - b. European Commission: Reviewing submitted technical photonics proposals for Horizon 2020, and rate proposals to EU guidelines.
  - c. <http://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020>
- 204) Reviewer: European Commission ICT-04-2018: Connected lighting
  - a. 11<sup>th</sup> June 2018
  - b. European Commission: Reviewing submitted technical photonics proposals for Horizon 2020, and rate proposals to EU guidelines.
  - c. <http://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020>
- 205) Invited talk and abstract: Pushing the performance of 50Gbps NRZ polymer modulators towards 100Gbps NRZ in a PIC platform to access 400 and 800Gbps data-rates
  - a. 25<sup>th</sup> Sept 2018
  - b. ECOC, Datacenter technologies. Sweden
- 206) Video: Pushing the performance of 50Gbps NRZ polymer modulators towards 100Gbps NRZ in a PIC platform to access 400 and 800 Gbps datarates.
  - a. 25<sup>th</sup> Sept 2018
  - b. ECOC, Market Focus at the ECOC Exhibit, (Youtube: Michael Lebby ECOC 2018)
- 207) Invited talk and abstract: ECOC [International Symposium on Hybrid PICs](#) entitled "Polymer PICs: technology and prospects"
  - a. 26<sup>th</sup> Sept 2018
  - b. International Symposium on Hybrid PICs co-located at the ECOC conference, Rome, Italy.
- 208) Reviewer (European Commission) for pilot line PISCALE
  - a. 18<sup>th</sup> Sept 2018
  - b. European Commission, Brussels
  - c. PISCALE is a pilot line that is focused on bringing to commercial market flexible organic display technologies in both panel and reel to reel formats.
- 209) Reviewer (European Commission) for pilot line MIPHAB
  - a. 19<sup>th</sup> Sept 2018
  - b. European Commission, Brussels
  - c. MIPHAB is a pilot line that is focused on bringing to commercial market near infra-red devices and packaging for industrial, defense, military and high volume applications.
- 210) Reviewer (European Commission) for pilot line PIXAPP
  - a. 2<sup>nd</sup> Oct 2018
  - b. European Commission, Brussels
  - c. PIXAPP is a pilot line that is focused on bringing to commercial market PIC (photonic integrated circuit) packaging solutions for InP and silicon photonics based technologies.



- 211) Reviewer (European Commission) for pilot line PIX4LIFE
  - a. 3<sup>rd</sup> Oct 2018
  - b. European Commission, Brussels
  - c. PIX4LIFE is a pilot line that is focused on bringing to commercial market PIC dielectric solutions for applications in the visible wavelength range in the medical applications market.
- 212) Reviewer (European Commission) for pilot line MIPHAB
  - a. 16<sup>th</sup> Feb 2019
  - b. European Commission, Brussels
  - c. MIPHAB is a pilot line that is focused on bringing to commercial market near infra-red devices and packaging for industrial, defense, military and high volume applications.
- 213) Reviewer (European Commission) for pilot line PIX4LIFE
  - a. 25<sup>th</sup> Mar 2019
  - b. European Commission, Brussels
  - c. PIX4LIFE is a pilot line that is focused on bringing to commercial market PIC dielectric solutions for applications in the visible wavelength range in the medical applications market.
- 214) Reviewer (European Commission) for project CARDIS
  - a. 18<sup>th</sup> Apr 2019
  - b. European Commission, Brussels
  - c. CARDIS is an EU project for PIC based technology to monitor blood flow and artery stiffness in the human body using long wavelength lasers and silicon photonics.
- 215) Reviewer: European Commission ICT-03-2019: Fiber optic communications and bio-photonics for medical applications
  - a. 6<sup>th</sup> June 2019
  - b. European Commission: Reviewing submitted technical photonics proposals for Horizon 2020, and rate proposals to EU guidelines.
  - c. <http://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020>
- 216) Reviewer: European Commission ICT-05-2019: Pilot lines (free form optics and integrated photonics for bio-medical applications)
  - a. 16<sup>th</sup> June 2019
  - b. European Commission: Reviewing submitted technical photonics proposals for Horizon 2020, and rate proposals to EU guidelines.
  - c. <http://ec.europa.eu/research/participants/portal/desktop/en/opportunities/h2020>
- 217) Reviewer (European Commission) for pilot line PISCALE
  - a. 11<sup>th</sup> Sept 2019
  - b. European Commission, Brussels
  - c. PISCALE is a pilot line that is focused on bringing to commercial market flexible organic display technologies in both panel and reel to reel formats.
- 218) Invited talk: Polymer modulators and polymer PIC technologies: PIC Training conference/workshop in Sunnyvale, Silicon Valley
  - a. 28<sup>th</sup> Jan 2019
  - b. PIC training session/workshop at Keysight facility

- 219) Co-Chairman: PIC (Photonic Integrated Circuits), International Conference, Brussels, Belgium
  - a. 26-27<sup>th</sup> Mar 2019
  - b. Photonic Integrated Circuits International
  - c. CS International
  - d. <http://www.picinternational.net>
- 220) Session chair and moderator: High volume, high performance PICs (Photonic Integrated Circuits) for Foundries at the International Conference, Brussels, Belgium
  - a. 26<sup>th</sup> Mar 2019
  - b. Photonic Integrated Circuits International
  - c. CS International
  - d. <http://www.picinternational.net>
- 221) Session chair and moderator: High volume PICs (Photonic Integrated Circuits) at the International Conference, Brussels, Belgium
  - a. 27<sup>th</sup> Mar 2019
  - b. Photonic Integrated Circuits International
  - c. CS International
  - d. <http://www.picinternational.net>
- 222) Invited Talk: Polymer PICs for 400Gbps+ datacom applications,” PICs (Photonic Integrated Circuits) at the International Conference, Brussels, Belgium
  - a. 27<sup>th</sup> Mar 2019
  - b. Photonic Integrated Circuits International
  - c. CS International
  - d. <http://www.picinternational.net>
- 223) Workgroup chair and moderator: Datacom roadmap committee at the International world mapping conference, Berlin, Germany
  - a. 12<sup>th</sup> June 2019
  - b. Photondelta Conference: chairing technical workgroup meetings to address photonics roadmap trends and challenges.
  - c. Photondelta in coordination with iNEMI, and AIM photonics.
  - d. <https://www.photondelta.eu>
- 224) Keynote speaker: ‘Global markets for PIC technologies’ at the 3<sup>rd</sup> International world mapping conference, at the Fraunhofer HHI, Berlin, Germany
  - a. 15<sup>th</sup> June 2019
  - b. Photondelta Conference: chairing technical workgroup meetings to address photonics roadmap trends and challenges.
  - c. Photondelta in coordination with iNEMI, and AIM photonics.
  - d. <https://www.photondelta.eu>
- 225) Invited speaker: ‘Lightwave Logic polymer modulator platform’ at the Spring Investor Conference, NYC, NY
  - a. 2<sup>nd</sup> April 2019
  - b. Spring Investor Summit (Microcap Conference) ([www.springinvestorsummit.com](http://www.springinvestorsummit.com))
- 226) Invited video ‘Lightwave Logic polymer modulator platform’ at the Spring Investor Conference, NYC, NY
  - a. 2<sup>nd</sup> April 2019
  - b. Spring Investor Summit (Microcap Conference)

- c. <https://www.youtube.com/watch?v=Mn4oICQpVTQ>
- 227) Invited video Interview by EPIC CTO Jose Pozo in EPIC's Photonics Industry Luminary video series.
  - a. 28<sup>th</sup> Jan 2019 (at Photonics West conference in San Francisco)
  - b. EPIC Trade Association, Europe
  - c. [https://www.youtube.com/watch?v=e\\_V4TeTSwaM](https://www.youtube.com/watch?v=e_V4TeTSwaM)
- 228) Invited video 'Global Markets and Trends' at the 3<sup>rd</sup> International Roadmap conference, Faunhofer HHI, Berlin Germany
  - a. 16<sup>th</sup> June 2019
  - b. PhotonDelta video PR team
  - c. <https://vimeo.com/341952732>
- 229) Invited video 'Lightwave Logic roadmaps for polymer photonics at the 3<sup>rd</sup> International Roadmap conference, Eindhoven, Netherlands
  - a. 16<sup>th</sup> June 2017
  - b. PhotonDelta video PR team
  - c. <https://vimeo.com/317216466>
- 230) Invited video 'Welcome to WTMF 18' at the 2<sup>nd</sup> International Roadmap conference, Eindhoven, Netherlands
  - a. 12<sup>th</sup> June 2018
  - b. PhotonDelta video PR team
  - c. <https://vimeo.com/275376937>
- 231) Reviewer (European Commission) for pilot line PISCALÉ
  - a. 11<sup>th</sup> Sept 2019
  - b. European Commission, Brussels
  - c. PISCALÉ is a pilot line that is focused on bringing to commercial market flexible organic display technologies in both panel and reel to reel formats.
- 232) Invited talk and abstract: "Polymer modulators with >50GHz performance for power consumption reduction at 400, 800, and 1600 Gbaud aggregated data-rates"
  - a. 24<sup>th</sup> Sept 2019
  - b. Market Focus Session, Photonics Integration and Digital Silicon Photonics,
  - c. ECOC 2019, Dublin, Ireland
  - d. <https://www.ecocexhibition.com/visit/market-focus/market-focus-2019-timetable/>
- 233) Video: Polymer modulators with >50GHz performance for power consumption reduction at 400, 800, and 1600 Gbaud aggregated datarates"
  - a. 24<sup>th</sup> Sept 2019
  - b. ECOC, Market Focus at the ECOC Exhibit, (Youtube: Michael Lebby ECOC 2019)
  - c. ECOC 2019, Dublin, Ireland
- 234) Invited talk and abstract: ECOC International Symposium on Hybrid PICs entitled "Polymer modulators enable the next generation of speeds and low power in optical networks"
  - a. 22<sup>nd</sup> Sept 2019
  - b. International Symposium and workshop (WO5) on Hybrid PICs,
  - c. ECOC conference 2019, Dublin, Ireland
  - d. <https://www.ecoc2019.org/workshop.html>

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- 235) Chairman and moderator, Market Focus ECOC 2019 session: Service and Content Provider Optical Transmission
  - a. 24<sup>th</sup> Sept 2019
  - b. Market Focus Session #5, ECOC 2019, Dublin, Ireland
  - c. <https://www.ecocexhibition.com/visit/market-focus/market-focus-2019-timetable/>
- 236) Chairman and moderator, Market Focus ECOC 2019 session: Optical Network Agility/Software Defined Networks
  - a. 24<sup>th</sup> Sept 2019
  - b. Market Focus Session #7, ECOC 2019, Dublin, Ireland
  - c. <https://www.ecocexhibition.com/visit/market-focus/market-focus-2019-timetable/>
- 237) Reviewer (European Commission) for pilot line MIPHAB
  - a. 10<sup>th</sup> Dec 2019
  - b. European Commission, Brussels
  - c. MIPHAB is a pilot line that is focused on bringing to commercial market near infra-red devices and packaging for industrial, defense, military and high-volume applications.
- 238) Webinar: Wall Street resource
  - a. 9<sup>th</sup> Jan 2020
  - b. Lightwave Logic HQ facilities in Denver, Colorado
  - c. A 30min recorded webinar answering questions on Lightwave Logic and its business plans, technology and plans for the future.
- 239) Invited video Interview by EPIC in EPIC's Photonics Industry video series on European funded pilot lines.
  - a. 5<sup>th</sup> Feb 2020 (at Photonics West conference in San Francisco)
  - b. EPIC Trade Association, Europe