Cellect

PTAB Consolidated Oral Arguments

May 26, 2021

SAMSUNG ELECTRONICS CO., LTD.,
SAMSUNG ELECTRONICS AMERICA
PETITIONERS

v.

CELLECT, LLC
PATENT OWNER

CASE NOS.: IPR2020-00475
IPR2020-00512

PATENT NO.: 9,186,052

DEMONSTRATIVE EXHIBIT – NOT EVIDENCE

IPR2020-00475 - Instituted Grounds

Claims Challenged	35 U.S.C. §	References
1	103	Wakabayashi, Ackland
1	103	Wakabayashi, Ackland, Suzuki
3, 7	103	Wakabayashi, Ricquier, Dierickx

IPR2020-00512 – Instituted Grounds

Claims Challenged	35 U.S.C. §	References
2	103	Swift, Ricquier, Suzuki
2	103	Larson, Swift, Ricquier, Suzuki

Technology Background / State of the Art

CCD and CMOS Image Sensor Development

- MOS Development
  - 1968 - Passive Pixel Sensor MOS
  - 1985 - Active Pixel Sensor MOS
- CCD Development
  - 1969
- CMOS Development
  - 1963 - PPS CMOS
  - 1993 - Camera-on-Chip APS CMOS (Dr. Fossum)

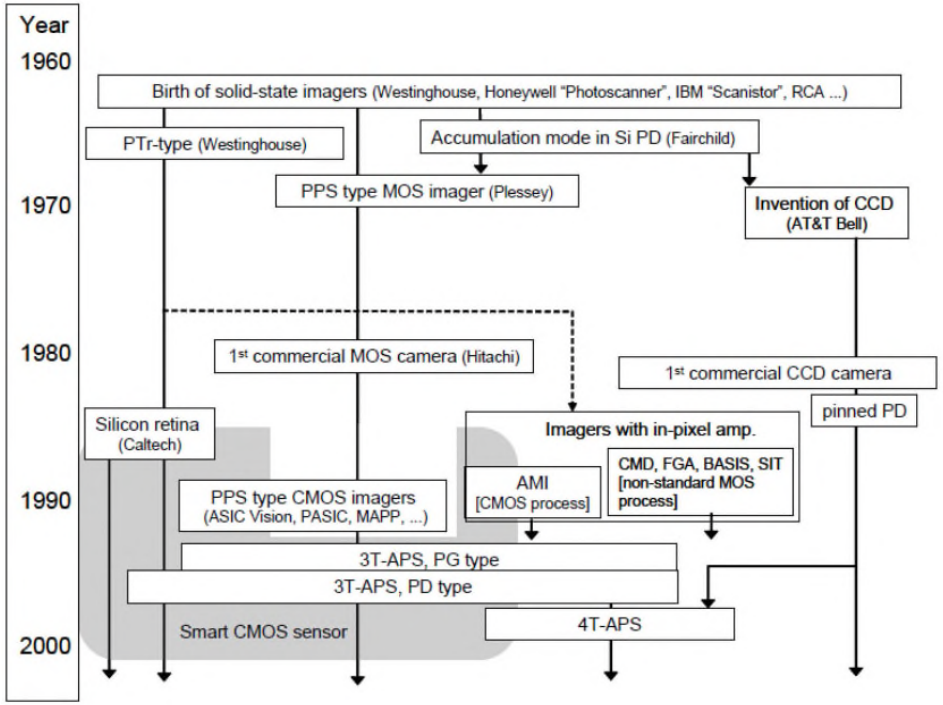


FIGURE 1.1
Evolution of MOS image sensors and related matters.
Ex. 2069 at 22.

POR at 8-10, 10-18

CCD Image Sensor Characteristics

- Pixel design provided superior performance in signal to noise
- Destructive one-way readout design (not addressable)
- Off-chip architecture
- CCD dominated market

POR at 11-14; Ex. 1003 at 83–89 (Adair Decl.), 90–95 (Baird Decl.); *see also* Ex. 2004 (Laser Focus World); Ex. 2039 (Business Week); Ex. 2053 (Fossum); Ex. 2058 (Holst); Ex. 2059 (Janesick); Ex. 2072 (Smith).

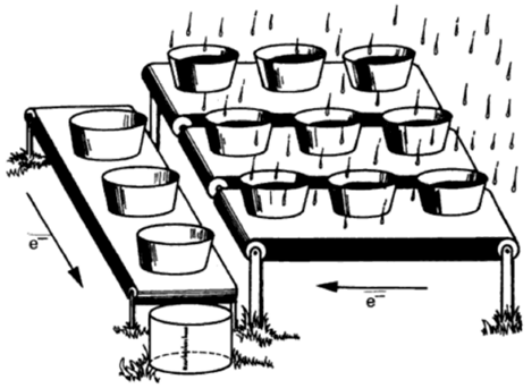


Figure 1.7(a) Bucket analogy used to describe CCD operation.

Ex. 2059 at 7.

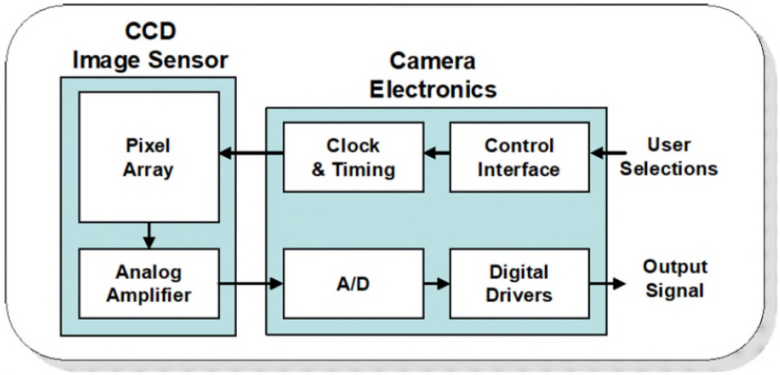


Figure 7.9: CCD Image Sensor with Off-Chip Supporting Components

Source: OIDA

Ex. 2036 at 8.

CMOS Image Sensor Characteristics

- Pixel design lacked performance (signal-to-noise) of CCD with the exception of EMI/RFI
- Non-destructive read-out design and was X-Y addressable allowing for images to be read out in different directions
- CMOS cost savings from camera-on-chip design
- CMOS imager sensors had very low image quality and had some application in low-end market

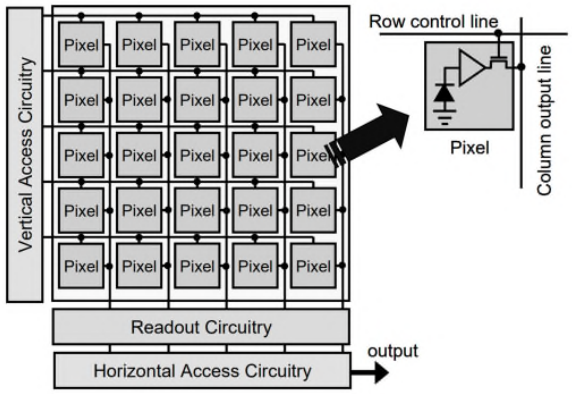


FIGURE 2.1
Architecture of a CMOS image sensor. A two-dimensional array of pixels, vertical and horizontal access circuitry, and readout circuitry are generally implemented. A pixel consists of a photodetector and transistors.

Ex. 2069 at 30.

POR at 9-16; Ex. 1003 at 83–89 (Adair Decl.), 90–95 (Baird Decl.); *see also* Ex. 2007 (Zarnowski); Ex. 2039 (Business Week); Ex. 2050 (Ackland's *Camera on a Chip*); Ex. 2053 (Fossum's *Are CCD's Dinosaurs* SPIE article); Ex. 2054 (Fossum's IEEE article); Ex. 2055 (Fossum's NASA tech brief); Ex. 2064 (Mendis); Ex. 2065 (Nakamura); Ex. 2066 (Nixon's *256x256 CMOS Active Pixel Sensor Camera-On-A-Chip* IEEE article); Ex. 2067 (Nixon's NASA tech brief); Ex. 2069 (Ohta).

Comparison of CCD and CMOS Image Quality

- CCD provided superior performance and image quality due to lower Fixed Pattern Noise (FPN) and Random Noise. Lebby Decl. at ¶ 79
- CCD required additional electromagnetic shielding to prevent noise from EMI/RFI, whereas CMOS is more resistant to EMI/RFI noise. Lebby Decl. at ¶¶ 89-90

- "**CCDs have historically been the dominant image sensors** and have been very successful in high speed **applications such as digital cameras, digital copiers, and flat bed scanners.** CCDs are also appropriate for surveillance and manufacturing applications where high performance is a requirement. **CCDs have traditionally had better light sensitivity** as a result of their pixel architecture, where all of the light hitting the array can potentially be converted to signal." Ex. 2036 (OIDA) at 8 (emphasis added).

CCDs Dominated the Market in 1997 and into the 2000s

- CCD architecture was well known and widely adopted because it offered the best performance and price
- CMOS did not even begin to be commercially feasible until late 1990s – early 2000s and only in very low-end product designs

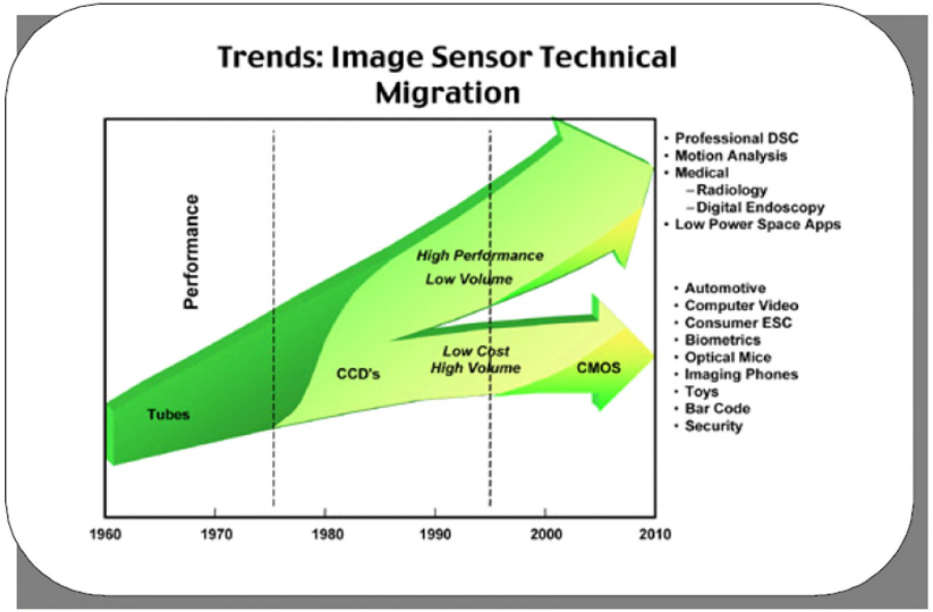


Figure 7.5: Image Sensor Migration and Materials

Source: Kodak

Ex. 2036 at 6.

POR at 11-16

The ’052 Patent

The '052 Patent's Innovation Over Conventional Camera-on-Chip

- Image sensor market in 1997 – the context for a POSITA
- State of the Art
  - CCD
    - Dominant imager at the time
    - High image quality, mature technology
  - APS CMOS Camera-on-a-Chip latest innovation by Dr. Fossum in 1993 over CMOS


1994's GANGBUSTER PROFITS FIRST FULL-YEAR RESULTS FOR 900 COMPANIES

BusinessWeek

Science & Technology

INVENTIONS

NASA'S TINY CAMERA HAS A WIDE-ANGLE FUTURE

It may still be in the lab, but the latest advance in capturing images has very bright prospects, indeed

Cellular phones giveawa Softwar comes f Laptops have th power o mainfra

Patent Owner Cellect, LLC Ex. 2039, p. 2

Get ready for the camera-on-a-chip. Since the 1970s, camera makers have dreamed of a one-chip camera containing all the components necessary to take a snapshot or make a movie.

Such devices are impractical with today's standard electronic image sensor. It's called a CCD, for charge-coupled device, and it's at the heart of every fax machine and camcorder. Japanese powerhouses such as Sony, Matsushita, and NEC churn out millions a year. CCDs offer good image quality. But they are costly, power-hungry, and—with the accessory chips they require—bulky.

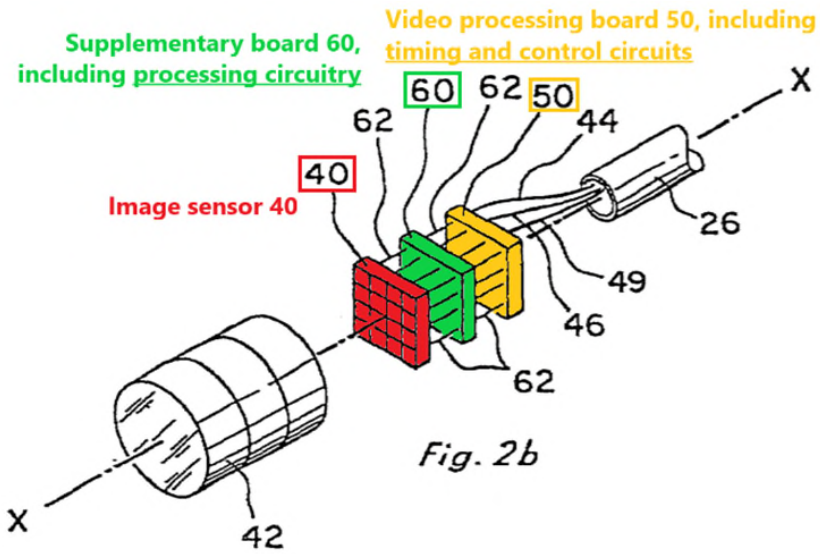
TEAMWORK. Now, the one-chip dream appears on the verge of being fulfilled, thanks to three inventors from NASA's Jet Propulsion Laboratory at California Institute of Technology in Pasadena. The leader is Eric R. Fossum, 37, who

AT&T, for one, would like to take the first jump. Long interested in low-cost cameras for video telephones, it has already collaborated with JPL to build two prototype arrays. A CCD costs a modest $20, but other components bring the system cost to $140, says Bryan D. Ackland, head of the VLSI Systems Research Dept. at AT&T Bell Laboratories in Holmdel, N.J. By putting everything on one chip, says Ackland, "what we're trying to do is build the entire camera subsystem for $20." At that price, every personal computer could come with a built-in videoconference feature, just as many multimedia PCs come outfitted with speakerphones today.

Ex. 2039 at 2.

'052 Patent's Innovation Over Conventional Camera-on-Chip

- Reduced Area Imaging Device
- Environments with high EMI/RFI
- Remoting image processing circuitry
- Further modified Fossum's CMOS APS Camera-on-a-Chip
- Deconstructing an aspect of APS CMOS Camera-on-a-Chip despite higher costs and degrading performance.



'052 Patent at Fig. 2b (annotated).

POR 2-6

'052 Patent Bucked Conventional Wisdom

- '052 Patent's inventors departed from conventional wisdom of emerging CMOS imagers, camera-on-a-chip design

  POR at 66, Sur-Reply at 1

- At the time, industry efforts focused on **MORE** component integration onto a single silicon die
- Starting from the CMOS camera-on-a-chip, the inventors recognized that strategically de-integrating certain imager components would enable miniaturization theretofore had been unachievable:

  POR-512 at 19-20

> The above-mentioned developments in solid state imaging technology have shown that "camera on a chip" devices will continue to be enhanced not only in terms of the quality of imaging which may be achieved, but also in the specific construction of the devices which may be manufactured by new breakthrough processes.
>
> Although the "camera on a chip" concept is one which has great merit for application in many industrial areas, a need still exists for a reduced area imaging device which can be used in even the smallest type of endoscopic instruments in order to view areas in the body that are particularly difficult to access, and to further minimize patient trauma by an even smaller diameter invasive instrument.

´052 Patent at 3:24-30

Claim 1 of the '052 Patent

1. An imaging device comprising:
   - a housing;
   - **an image sensor** mounted in said housing,
     - said **image sensor including a first circuit board** having a length and a width thereto, wherein said length and width of said first circuit board define **a first plane**,
     - **said first circuit board including an array of CMOS pixels thereon**, wherein a plurality of CMOS pixels within **said array of CMOS pixels each include an amplifier**,
     - said first circuit board further including **timing and control circuitry thereon**, said timing and control circuitry being coupled to said array of CMOS pixels,
     - **said image sensor producing a pre-video signal**;
   - **a second circuit board** mounted in said housing,
     - said second circuit board being electrically coupled to said first circuit board,
     - said second circuit board having a length and a width thereto, wherein said length and width of said second circuit board **define a second plane**,
     - said **second circuit board including circuitry thereon to convert said pre-video signal to a post-video signal**,
     - said second circuit board **being offset** from said first circuit board,
     - said second plane of said second circuit board being **substantially parallel** to said first plane of said first circuit board; **...**

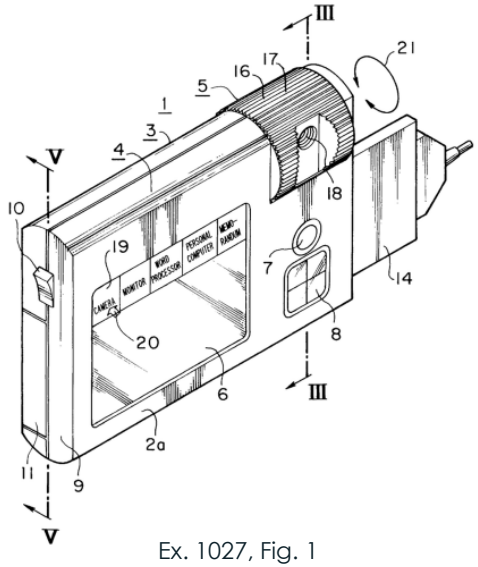
Claim 1 of the ’052 Patent (cont.)

…

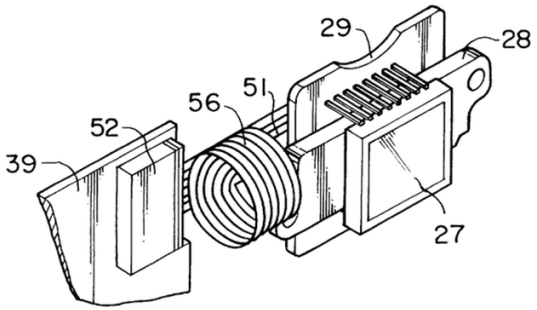
- a lens mounted in said housing, said lens being integral with said imaging device, said lens focusing images on said array of CMOS pixels of said image sensor;
- a video screen, said video screen being electrically coupled to said second circuit board, said video screen receiving said post-video signal and displaying images from said post-video signal; and
- a power supply mounted in said housing, said power supply being electrically coupled to said first circuit board to provide power to said array of CMOS pixels and said timing and control circuitry, said power supply also being electrically coupled to said second circuit board to provide power thereto;
- wherein said image sensor has a generally square shape along said first plane;
- and wherein a largest dimension of said image sensor along said first plane is between 2 and 12 millimeters.

IPR2020-00475:
Claims 1, 3, 7 of the ’052 Patent

Wakabayashi (U.S. 5,903,706, Ex. 1027)



Ex. 1027, Fig. 1



Ex. 1027, Fig. 7

- Digital camera with rotatable camera head
  - Key feature: image arrangement convertor circuit that flips image upright when camera head rotated

Ex. 1027 at 10:18-11:34, Lebby Decl., ¶ 132-134

- **No** disclosure of CMOS image sensor, let alone de-integrated CMOS camera-on-chip design

POR at 19-20, Lebby Decl., ¶ 101-102

POSITA Would Not Have Been Motivated to Modify Wakabayashi

POSITA would understand is a CCD-based digital camera

POR at 19, Lebby Decl., ¶ 101-102

Expressly discloses an off-chip circuit design for its processing circuitry

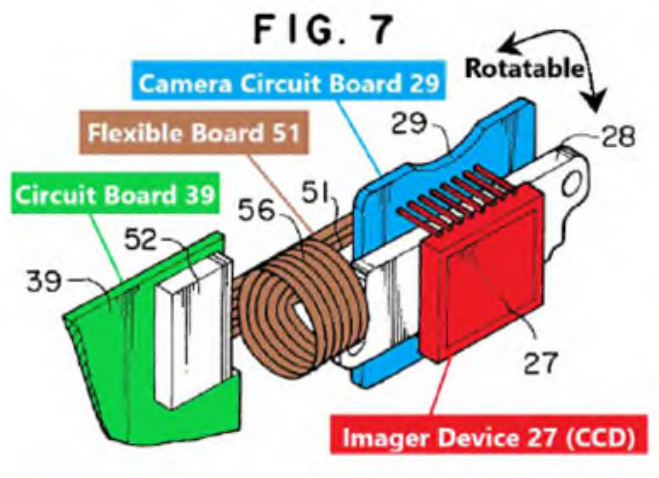
POR at 20-21, Ex. 1027 at 5:48-58, 6:5-10

OR

- No motivation to combine with Ackland/Suzuki (Grounds 1-2) or Ricquier/Dierickx (Ground 3) POR 25-47, 52, 55; Sur-Reply at 3-20; *Lebby Decl. at* ¶ 124-130, 136-138.
  - Record evidence demonstrates technical obstacles POR 29-30, 41-42
  - Requires complete redesign POR at 28-31, 41-42, Sur-Reply at 15-18
  - Changes principle of operation POR at 31-34, Sur-Reply at 16-18
  - Contrary to intended purpose POR at 34-37, Sur-reply at 13-15

POSITA Understands Wakabayashi is a CCD-based Camera

- Wakabayashi's pixel array with off-chip circuit board design understood to be CCD
  - CCD pixels not integrated with CMOS circuit boards, requiring off-chip design. *See* Ex. 2088 ("Lebby Decl.") ¶¶ 7, 10, 101–02, 107–10, 114, 116–17, 122–24.
  - CCD generates significant heat—metal bracket 28 provided heat sink (interposed between pixels and board 29). *See* Lebby Decl. ¶¶ 7, 118, 125, 136.
  - Driving circuits associated with CCD. *See* Lebby Decl. ¶¶ 101–02, 110, 117–18, 128–29, 137.
- Camera design included numerous high-end features (built-in video screen, external storage, etc.), demanding a high performance image sensor – CCD

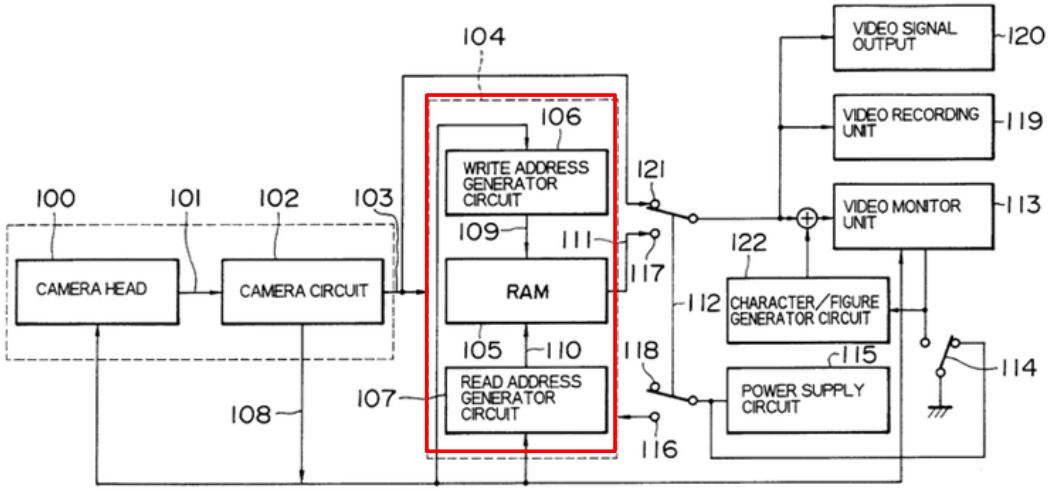


POSITA Understands Wakabayashi is a CCD-based camera (cont.)

- Wakabayashi's key feature, "image arrangement convert circuit" demonstrates it is directed to a CCD camera
    - CCD image sensors, unlike CMOS image sensors, cannot readout image in reverse order (i.e., "addressability").

[57] **ABSTRACT**

An upside-down image, generated when a video camera is rotated about a horizontal axis to face to substantially the same direction as a display unit does, is electrically corrected to be an upright image. A video camera unit made compact to realize a reduction in weight of a video camera rotating mechanism. An image arrangement convertor circuit is provided between the video camera unit and a liquid crystal display serving as a display unit or a recording unit.



POR at 28-29; Lebby Decl. at ¶132-134, 136; Sur-Reply 14-15 (responding to Petitioner's Reply at 3-4, Neikirk Reply at ¶ 13-20)

Ackland Patent (U.S. 5,835,141 , Ex. 1006)

- **Ackland's CMOS APS Pixel Array**
  - Single polysilicone layer

    See Ackland Patent at Title, Abstract.
  - Timing and Control on-chip

    Lebby Decl. ¶¶ 103–05, 122–25, 128, 138; Ex. 2054 at 1.
  - Location of image processing circuitry expressly described as "not shown"

    Lebby Decl. ¶¶ 103–05.

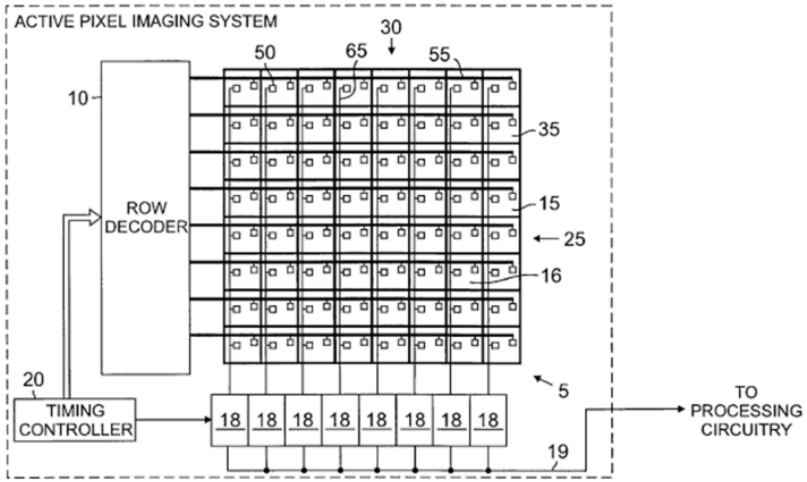


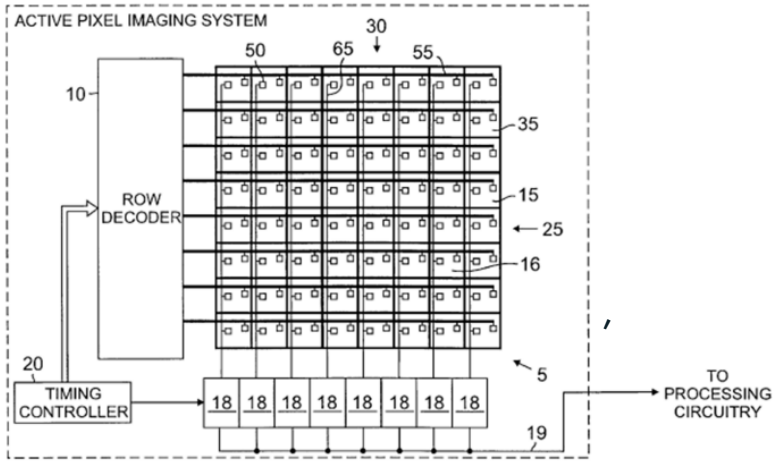
FIG. 6

  - Ackland's *Camera on a Chip* Article tells us what Ackland developed:

    (Ex. 2050, "Ackland Article")
    - **Camera on a chip**

Ackland Patent's Processing Circuitry is Simply "Not Shown"

Petitioner asserts Ackland Patent discloses its processing circuitry is "off-chip"



Ex. 1006 at 5, Fig. 6. **FIG. 6**

This is incorrect.

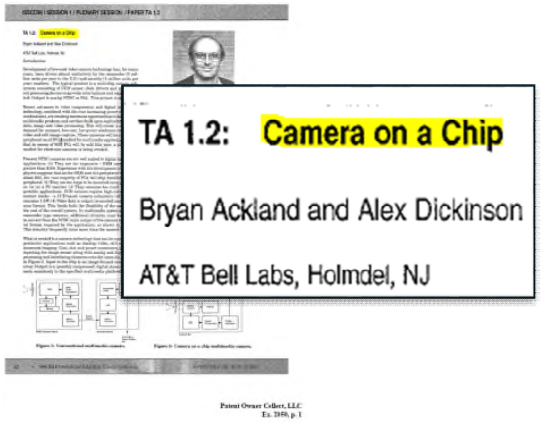
It is simply "not shown"

POR at 22, Sur-Reply at 5-6, Lebby Decl., ¶ 103-105

pixel **35**. If an image focused on the array **5** by, for example, a conventional camera lens, then each pixel **35** generates an output voltage signal corresponding to the light intensity for a portion of the image focused on that pixel **35**. The output voltage signals generated by the activated row **35** are simultaneously provided to the corresponding amplifiers **18** via the column output line **65**. Output signals from the amplifiers **18** are provided to the common output line **19** in serial fashion based on timing control signals from the timing control **20**. The output signals are routed to suitable processing circuitry, not shown.

Ex. 1006 at 9 (annotating 8:42–52).

What Dr. Ackland Was Working on at the Time: Camera on a Chip



TA 1.2: Camera on a Chip

Bryan Ackland and Alex Dickinson

AT&T Bell Labs, Holmdel, NJ

Arguably the most important advantage of the CMOS APS approach, however, is the ability to integrate much of the camera timing, control and signal processing circuitry onto the same silicon die. A CIF (352x288) sensor array can be built in 0.5µm CMOS in under 11mm² active area. Even assuming a 30mm² die, this leaves area for these system functions, plus extra circuitry to customize the camera for a particular application.

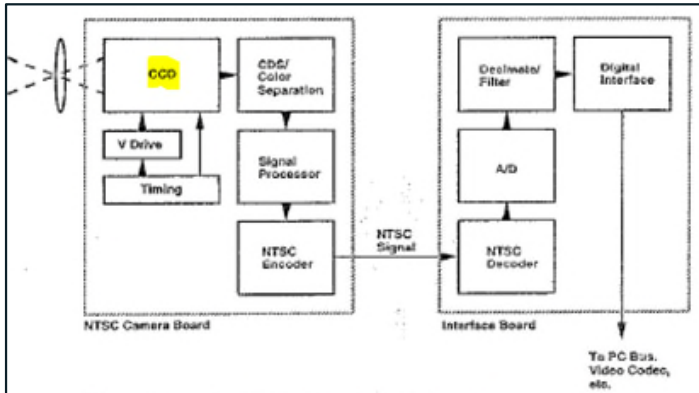


Figure 1: Conventional multimedia camera.

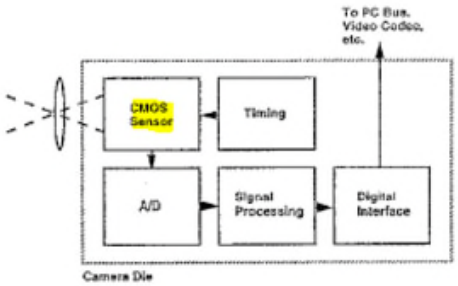


Figure 2: Camera on a chip multimedia camera.

Ex. 2050 at 1,3 (annotated).

Ricquier (Ex. 1033/1038)

- Describes **passive** CMOS image sensor image sensor "specifically designed for use in industrial machine vision applications" Ex. 1038 at 8; POR at 23–24, 52–55; Sur-Reply at 13,15.

- Describes "sensor architecture that can be used as a module in further sensor systems on a **single chip**."
  Ex. 1038 at 9; POR at 24, 34-35.

- POSITA understands that Ricquier does not teach off-chip processing circuitry for CMOS sensor.

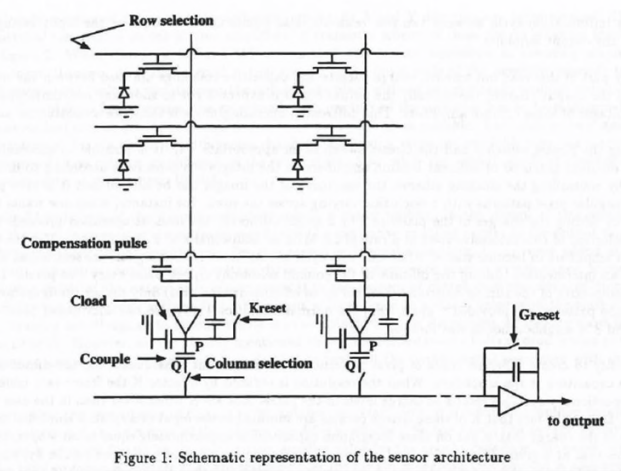


Figure 1: Schematic representation of the sensor architecture

Ex. 1038 at 9.

the image acquisition rate is increased in inspection tasks or when tracking can be performed faster in assembly tasks, the production volume can be increased accordingly. A CMOS technology was chosen because it offers the selective addressability together with the possibility of further cointegration of processing electronics on the same chip.

Ex. 1038 at 8; POR at 23–24; Sur-Reply at 15-17.

- Petitioner fails to demonstrate a rational motivation ("selective addressability", "multiple resolutions") for combining Wakabayashi and Ricquier. POR at 52–55; Sur-Reply at 15–17, 22–24.

Dierickx (Ex. 1041)

- Describes a CMOS-based imaging device
- Cited for teaching active pixels, size, and dimensions of image sensors.

POR at 24-26

- **BUT** no motivation to combine with Wakabayashi and Ricquier
  - Dierickx acknowledges "CCD-based camera systems are nowadays **preferred** in applications wherein a high image quality is required such as video or still camera applications."

POR at 55-57, Ex. 1041 at ¶5, Sur-Reply 22-24

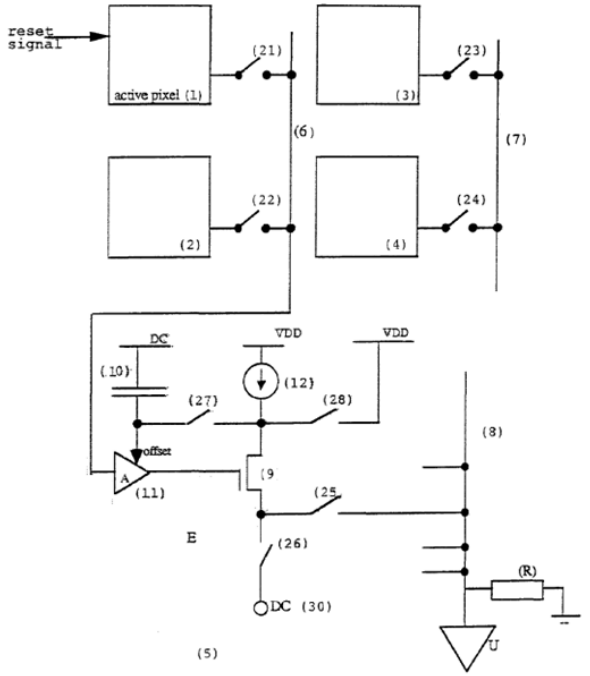


Fig. 2

It Was Not Known to De-integrate CMOS Imagers

- Petitioner argues: "it was a well-known engineering consideration to move the circuitry from a circuit board directly attached to the image sensor chip to one that is remote to the image sensor chip." Petition at 24.
  - **Incorrect.** **Ackland** does not demonstrate off-chip circuitry. The processing circuitry is simply "not shown" POR at 22; Lebby Decl. at ¶¶ 103–05.

- Petitioner does not specifically argue "CMOS with off-chip circuitry were well-known at the time" until its Reply. *Compare* Pet. Reply at 3-4 *with* Petition at 24-25.
  - **AND** Patent Owner addressed this allegation regarding **Swift** and **Monroe** in its Sur-Reply. Sur-Reply at 7; *see also* POR at 22, 50

Petitioner Fails to Demonstrate Any Motivation to Combine Wakabayashi and Ackland/Suzuki or Ricquier/Dierickx

Petitioner's Positions – Inconsistent

Feature	Wakabayashi	Ackland Patent
Pixel array	**Not shown** (can be anything)	APS CMOS
Timing & Control	**Not shown** (can be anything)	On-Chip
Image Processing	Camera Circuit Board off chip	**Not shown** (means off-chip)

Design Choice Not Enough

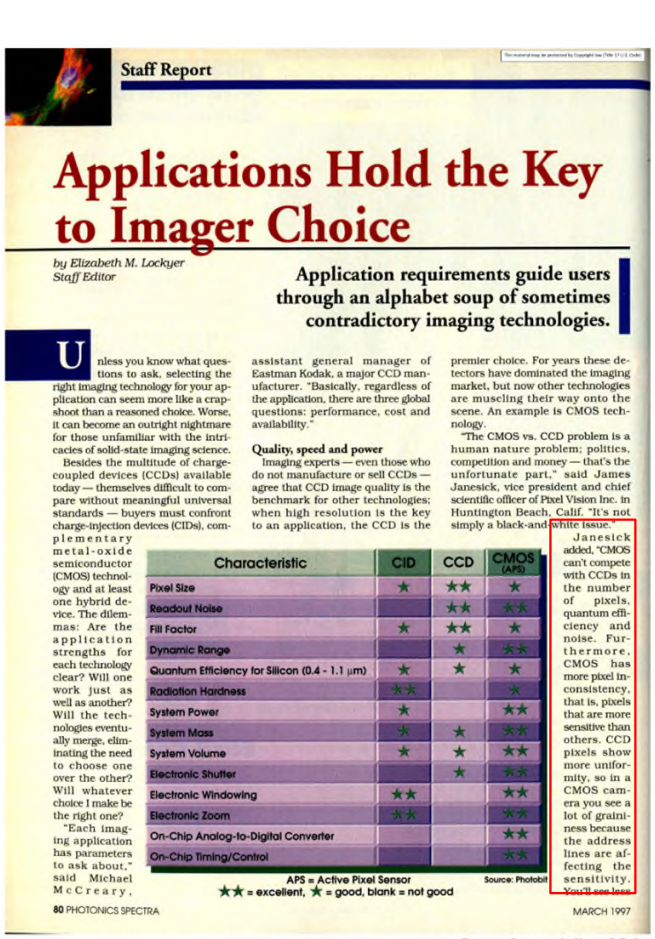
- Petitioner and its expert rely on design choice. Petition at 32; POR at 41-42; Sur-Reply at 9-10; Ex. 2091 at 165:12–166:3, 166:14–167:6.
- Could Have vs Would Have POR at 37-42; Sur-Reply at 8–9.
  - *Personal Web Technologies, LLC v. Apple, Inc.*,
    - That two references *could be* combined is "not enough" to "imply a motivation to pick out those two references and combine them to arrive at the claimed invention"
  - *Belden Inc. v. Berk-Tek LLC*
    - "[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated* to make the combinations or modifications of prior art to arrive at the claimed invention."

Record Evidence Demonstrates No Motivation to Combine Wakabayashi and Ackland

- No reasonable expectation of success POR at 42-45; Sur-Reply at 10; Lebby Decl. at ¶¶10-15, 125-131
  - Proposed Wakabayashi and Ackland combination results in **poor performance** and **higher costs** compared to CCD or Camera-on-Chip APS CMOS
  - Worst aspects from CCD and APS CMOS
  - Significant Re-Design of Wakabayashi and Ackland POR at 28-31, 41-42, Sur-Reply at 15-18

Lockyer Photonics Spectra Article (Ex. 2063)

1997 Evidence: CMOS could not compete with CCD image quality



Staff Report

Applications Hold the Key to Imager Choice

by Elizabeth M. Lockyer
Staff Editor

Application requirements guide users through an alphabet soup of sometimes contradictory imaging technologies.

Unless you know what questions to ask, selecting the right imaging technology for your application can seem more like a crapshoot than a reasoned choice. Worse, it can become an outright nightmare for those unfamiliar with the intricacies of solid-state imaging science.

Besides the multitude of charge-coupled devices (CCDs) available today — themselves difficult to compare without meaningful universal standards — buyers must confront charge-injection devices (CIDs), complementary metal-oxide semiconductor (CMOS) technology and at least one hybrid device. The dilemmas: Are the application strengths for each technology clear? Will one work just as well as another? Will the technologies eventually merge, eliminating the need to choose one over the other? Will whatever choice I make be the right one?

"Each imaging application has parameters to ask about," said Michael McCreary, assistant general manager of Eastman Kodak, a major CCD manufacturer. "Basically, regardless of the application, there are three global questions: performance, cost and availability."

Quality, speed and power

Imaging experts — even those who do not manufacture or sell CCDs — agree that CCD image quality is the benchmark for other technologies; when high resolution is the key to an application, the CCD is the premier choice. For years these detectors have dominated the imaging market, but now other technologies are muscling their way onto the scene. An example is CMOS technology.

"The CMOS vs. CCD problem is a human nature problem; politics, competition and money — that's the unfortunate part," said James Janesick, vice president and chief scientific officer of Pixel Vision Inc. in Huntington Beach, Calif. "It's not simply a black-and-white issue."

Janesick added, "CMOS can't compete with CCDs in the number of pixels, quantum efficiency and noise. Furthermore, CMOS has more pixel inconsistency, that is, pixels that are more sensitive than others. CCD pixels show more uniformity, so in a CMOS camera you see a lot of graininess because the address lines are affecting the sensitivity. You'll see less

Characteristic	CID	CCD	CMOS (APS)
Pixel Size	★	★★	★
Readout Noise		★★	★★
Fill Factor	★	★★	★
Dynamic Range		★	★★
Quantum Efficiency for Silicon (0.4 - 1.1 μm)	★	★	★
Radiation Hardness	★★		★
System Power	★		★★
System Mass	★	★	★★
System Volume	★	★	★★
Electronic Shutter		★	★★
Electronic Windowing	★★		★★
Electronic Zoom	★★		★★
On-Chip Analog-to-Digital Converter			★★
On-Chip Timing/Control			★★

APS = Active Pixel Sensor
★★ = excellent, ★ = good, blank = not good
Source: Photobit

80 PHOTONICS SPECTRA MARCH 1997

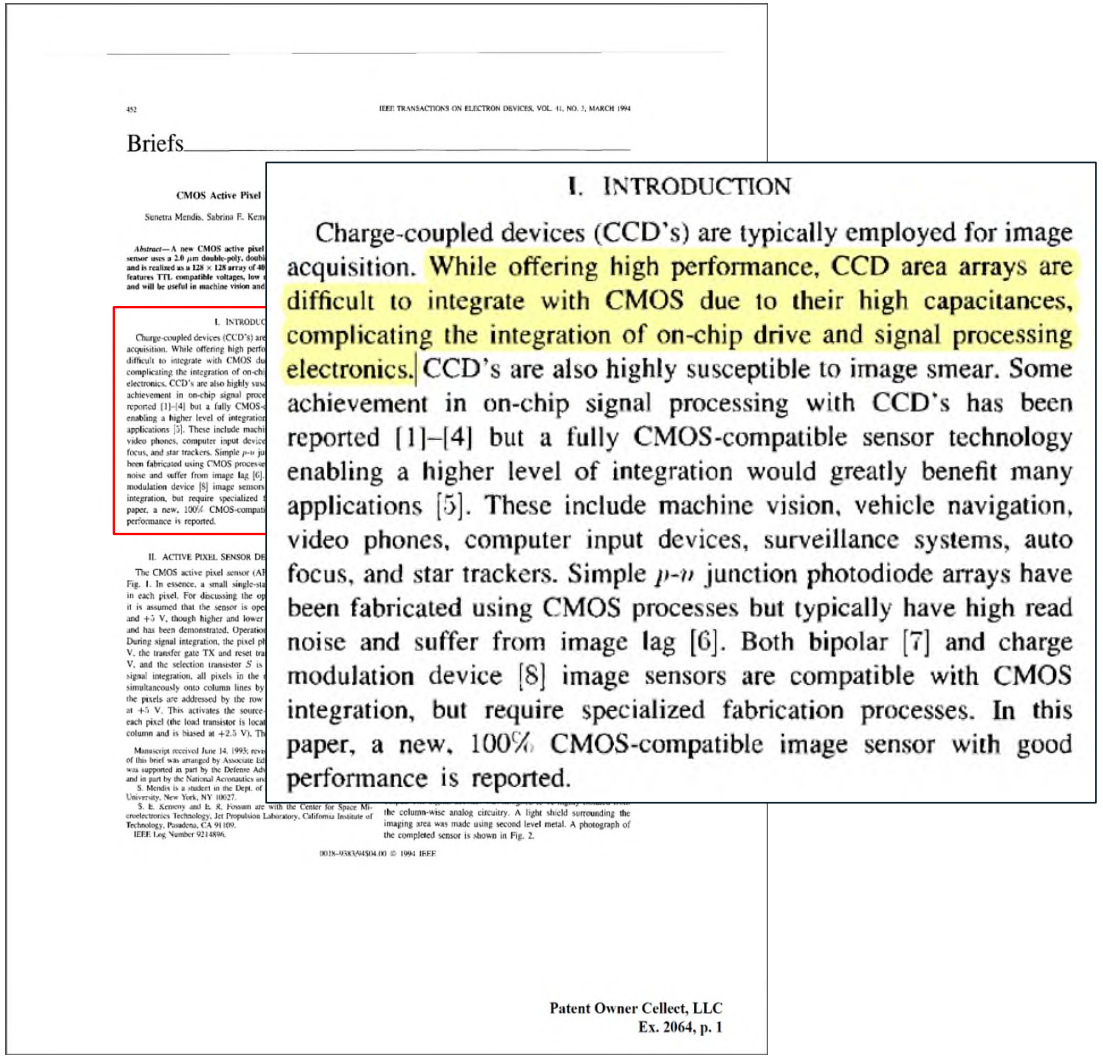
Patent Owner Cellect, LLC
Ex. 2063, p. 1

"CMOS can't compete with CCDs in the number of pixels, quantum efficiency and noise. Furthermore, CMOS has more pixel inconsistency, that is, pixels that are more sensitive than others. CCD pixels show more uniformity, so in a CMOS camera you can see a lot of graininess because the address lines are affecting the sensitivity. You'll see less graininess on the CCD image."

POR at 33, 43-44; Ex. 2063 at 1–2 (annotated).

Mendis' IEEE Article (Ex. 2064)

1993 Evidence: CCD and CMOS cannot simply be combined or switched and use different fabrication processes



452 IEEE TRANSACTIONS ON ELECTRON DEVICES, VOL. 41, NO. 3, MARCH 1994

Briefs

CMOS Active Pixel

Sunetra Mendis, Sabrina E. Kem

I. INTRODUCTION

Charge-coupled devices (CCD's) are typically employed for image acquisition. While offering high performance, CCD area arrays are difficult to integrate with CMOS due to their high capacitances, complicating the integration of on-chip drive and signal processing electronics. CCD's are also highly susceptible to image smear. Some achievement in on-chip signal processing with CCD's has been reported [1]–[4] but a fully CMOS-compatible sensor technology enabling a higher level of integration would greatly benefit many applications [5]. These include machine vision, vehicle navigation, video phones, computer input devices, surveillance systems, auto focus, and star trackers. Simple p-n junction photodiode arrays have been fabricated using CMOS processes but typically have high read noise and suffer from image lag [6]. Both bipolar [7] and charge modulation device [8] image sensors are compatible with CMOS integration, but require specialized fabrication processes. In this paper, a new, 100% CMOS-compatible image sensor with good performance is reported.

II. ACTIVE PIXEL SENSOR DE

Manuscript received June 14, 1993; revi

S. Mendis is a student in the Dept. of University, New York, NY 10027.

S. E. Kemeny and E. R. Fossum are with the Center for Space Microelectronics Technology, Jet Propulsion Laboratory, California Institute of Technology, Pasadena, CA 91109.

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0018–9383/94$04.00 © 1994 IEEE

the column-wise analog circuitry. A light shield surrounding the imaging area was made using second level metal. A photograph of the completed sensor is shown in Fig. 2.

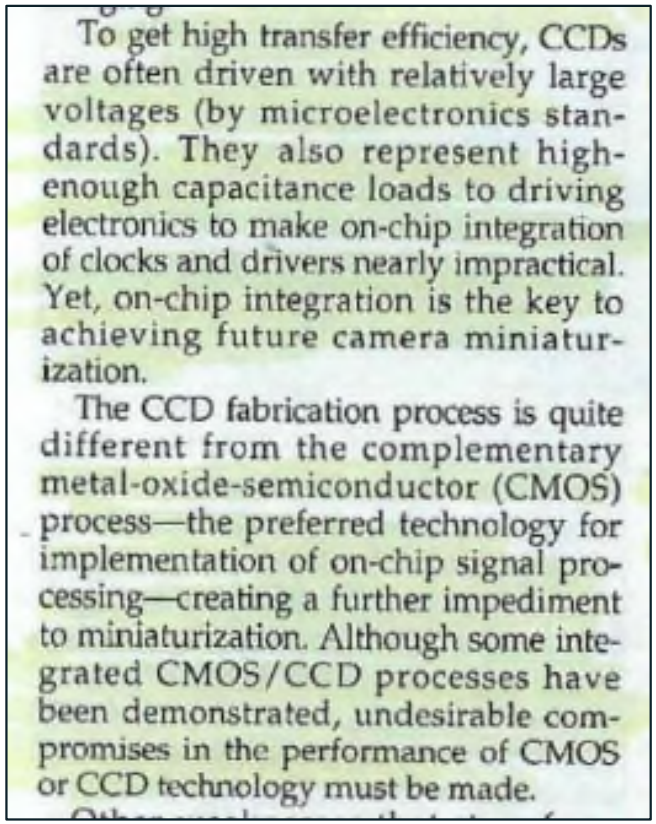
Patent Owner Cellect, LLC
Ex. 2064, p. 1

POR at 29; Lebby Decl. at ¶ 10, Ex. 2064 at 1 (annotated).

Fossum's Laser Focus World Article (Ex. 2004)

1993 Evidence: benefit of APS CMOS achieved through camera-on-a-chip integration to achieve further miniaturization.

"…on-chip integration is key to achieving future camera miniaturization."



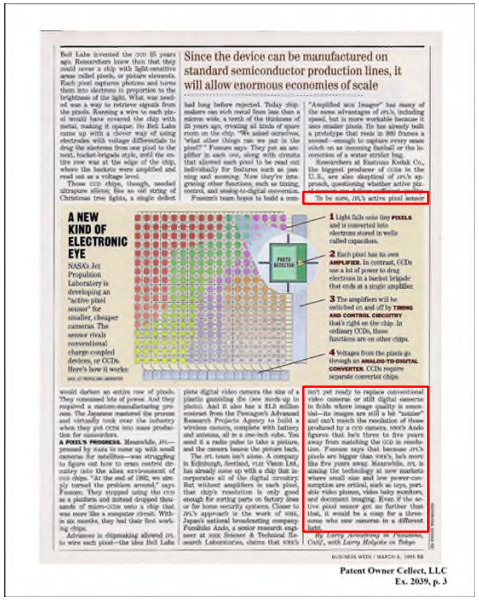
To get high transfer efficiency, CCDs are often driven with relatively large voltages (by microelectronics standards). They also represent high-enough capacitance loads to driving electronics to make on-chip integration of clocks and drivers nearly impractical. Yet, on-chip integration is the key to achieving future camera miniaturization.

The CCD fabrication process is quite different from the complementary metal-oxide-semiconductor (CMOS) process—the preferred technology for implementation of on-chip signal processing—creating a further impediment to miniaturization. Although some integrated CMOS/CCD processes have been demonstrated, undesirable compromises in the performance of CMOS or CCD technology must be made.

Ex. 2004 at 9 (annotated), Lebby. Decl at ¶ 128, POR at 35-36, 44

Armstrong's BusinessWeek Article (Ex. 2039)

1995 Evidence: Conventional CCD provided superior image quality over APS CMOS



Since the device can be manufactured on standard semiconductor production lines, it will allow enormous economies of scale

A NEW KIND OF ELECTRONIC EYE

To be sure, JPL's active pixel sensor isn't yet ready to replace conventional video cameras or still digital cameras in fields where image quality is essential—its images are still a bit "noisier" and can't match the resolution of those produced by a CCD camera. NHK's Ando figures that he's three to five years away from matching the CCD in resolution. Fossum says that because JPL's pixels are bigger than NHK's, he's more like five years away. Meanwhile, JPL is aiming the technology at new markets where small size and low power-consumption are critical, such as toys, portable video phones, video baby monitors, and document imaging. Even if the active pixel sensor got no further than that, it would be a coup for a threesome who saw cameras in a different light.

Patent Owner Cellect, LLC Ex. 2039, p. 3

POR at 33, Ex. 1060 at 55

Armstrong's BusinessWeek Article (cont.)


Science & Technology

INVENTIONS

NASA'S TINY CAMERA HAS A WIDE-ANGLE FUTURE

1995 Evidence: Cost saving benefit of APS CMOS achieved by using Camera-on-Chip design

Get ready for the camera-on-a-chip. Since the 1970s, camera makers have dreamed of a one-chip camera containing all the components necessary to take a snapshot or make a movie. With all the smarts on one chip instead of several, designers figure they could make a camera small and cheap enough to open vast new markets for everything from dolls that "see" to rear-bumper cameras that would help drivers back up.

AT&T, for one, would like to take the first jump. Long interested in low-cost cameras for video telephones, it has already collaborated with JPL to build two prototype arrays. A CCD costs a modest $20, but other components bring the system cost to $140, says Bryan D. Ackland, head of the VLSI Systems Research Dept. at AT&T Bell Laboratories in Holmdel, N.J. By putting everything on one chip, says Ackland, "what we're trying to do is build the entire camera subsystem for $20." At that price, every personal computer could come with a built-in videoconference feature, just as many multimedia PCs come outfitted with speakerphones today.

POR at 40, Ex. 1060 at 54 (annotated), Ex. 2039 at 2

Johannes' Wall Street Journal Article (Ex. 2060)

1998 Evidence: 50% cost saving benefit of APS CMOS achieved by using Camera-on-Chip design

Nintendo's Game Boy uses CMOS sensor chips.

CMOS sensors cost an average of less than $14, about 15% to 20% cheaper than CCDs, says Mark Kirstein, of Cahners In-Stat Group, a market researcher in Newton, Mass. If additional image-processing functions are crammed onto the chip, the savings can reach 50%, he says. The chip Nintendo used, Mitsubishi Electric Corp.'s new "artificial retina," incorporates both light-sensing and image-processing functions. It costs only $10, or half what traditional CCD technology would have cost, Mitsubishi says.

1998 Evidence: APS CMOS still lag in image quality compared to CCD

First, CMOS designers must work out the kinks, including "noise," the industry's term for annoying little dots or scratches on photos. "These chips have to work in low light and deliver the same vivid colors your eye sees. They have to do that running off a watch battery, for a price that everybody can afford," says Don Lake, general manager of Vision's U.S. unit. "There are a lot of smart people in the world, but no one's completely figured it out yet."

POR at 40, Ex. 2060 at 1.

Fossum's IEEE Article (Ex. 2054)

1995 Evidence: Benefit of APS CMOS achieved by using Camera-on-Chip design

Abstract

Recent advancements in CMOS image sensor technology are reviewed, including both passive pixel sensors and active pixel sensors. On-chip analog to digital converters and on-chip timing and control circuits permit realization of an electronic camera-on-a-chip.

1995 Evidence: CCD technology was "not well-suited to CMOS integration"

3. Modern CMOS image sensors

The 1990's have seen a resurgent interest in CMOS image sensors. The major reason for the interest is related to miniaturized and cost effective imaging systems. CMOS-based image sensors offer the potential opportunity to integrate a significant amount of VLSI electronics on-chip and reduce component and packaging costs. CCD technology, on the other hand, has become quite specialized and, in general, is not well-suited to CMOS integration due to voltage, capacitance and process constraints.

POR at 29, Lebby Decl. ¶ 9, 124, 154, Ex. 2054 at 1–2 (annotated).

OIDA Market Report (Ex. 2036)

- **Evidence**: Analysis of market shows that in 1997, CCD image sensors dominated the market until the mid 2000's.

> CCDs will continue to be used for applications requiring very high quality imaging, such as medical imaging and professional cameras (Figure 7.5). CMOS has evolved into the high volume imaging sensor solution, using common silicon manufacturing processes. CMOS's integrated components, including analog-to-digital (A/D) converter and clock, combined with a small footprint and low power consumption, make CMOS the ideal solution for small handheld devices (Figure 7.6). CMOS imaging is also capable of tracking, necessary for video images; for CCDs, this requires even more circuitry.

Ex. 2036 at 6

- In the late-1990's and mid-2000s, APS CMOS was relegated to high-volume, low-quality applications, like security applications in *Swift*

> CCDs have historically been the dominant image sensors and have been very successful in high speed applications such as digital cameras, digital copiers, and flat bed scanners. CCDs are also appropriate for surveillance and manufacturing applications where high performance is a requirement. CCDs have traditionally had better light sensitivity as a result of their pixel architecture, where all of the light hitting the array can potentially be converted to signal.

Ex. 2036 at 8

POR at 12-13, 31; Lebby Decl. ¶ 10-11, 84, 86-87, 91, 115-116, 123.

OIDA Market Report (cont.)

- **Evidence**: CCDs require much higher voltages than CMOS imagers
  - i.e., high technical obstacles facing any combination of CMOS and CCD technologies

> Although CCDs offer high imaging performance, they are expensive to produce. Unlike CMOS, CCDs require a special manufacturing process in order to create components capable of transporting the charge across the chip without distortion (Figure 7.9). CCDs also require additional supporting components, increasing the footprint of the total solution. Power consumption is significantly higher with CCDs compared to CMOS imagers. Voltage requirements also run higher, typically over 10 volts; in some instances two different voltages are required. Lastly, current CCDs require additional components in order to support both still images as well as video.

POR at 29-31; Lebby Decl. ¶ 122, 137; Ex. 2036 at 9 (annotated).

IPR2020-00512:
Claim 2 of the ‘052 Patent

Grounds (IPR2020-00512 – '052 Patent)*

Ground 1: Claim 2 is not obvious over Swift in view of Ricquier and Suzuki.

- POSITA would not have combined Swift, Ricquier, and Suzuki. POR at 25-35, Sur-Reply at 18
- Swift in view of Ricquier/Suzuki does not disclose circuitry on a second circuit board to convert pre-video signal to post-video signal. POR at 35-38, Sur-Reply at 20-21
- Swift, Ricquier, Suzuki fail to disclose an imaging device with the requisite dimensions. POR at 21-25, Sur-Reply at 14-21

Grounds (IPR2020-00512 – '052 Patent)*

Ground 2: Claim 2 is not obvious over Larson in view of Swift, Ricquier, and Suzuki.

- Erroneously mixes and matches different technologies
- POSITA would not have combined Larson, Swift, Ricquier, and Suzuki.

POR at 38-39, Sur-Reply at 21-23

Claim 2 of the ´052 Patent

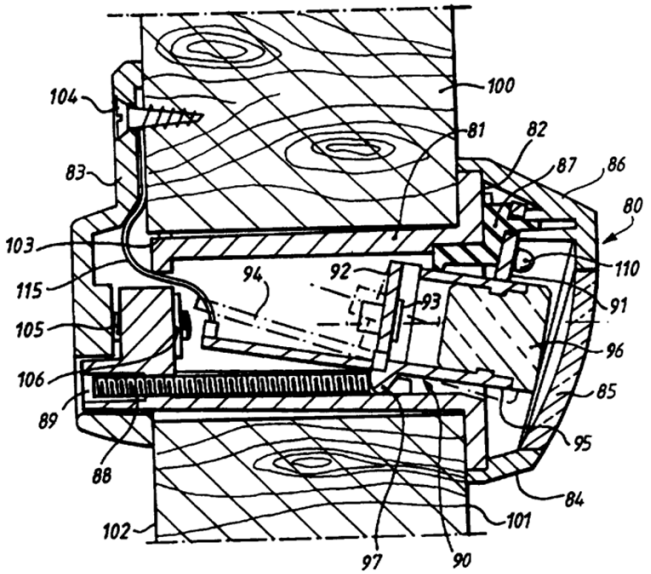
- 2. An imaging device comprising:
  - a housing;
  - **an image sensor** mounted in said housing,
    - said **image sensor including a first circuit board** having a length and a width thereto, wherein said length and width of said **first circuit board define a first plane**,
    - said first circuit board including **an array of CMOS pixels thereon**, wherein a plurality of CMOS pixels within **said array of CMOS pixels each include an amplifier**,
    - said **first circuit board further including timing and control circuitry thereon**, said timing and control circuitry being coupled to said array of CMOS pixels, said image sensor producing a pre-video signal;
  - **a second circuit board** mounted in said housing,
    - said second circuit board being electrically coupled to said first circuit board,
    - said second circuit board having a length and a width thereto, wherein said length and width of said second circuit board **define a second plane**,
    - said **second circuit board including circuitry thereon to convert said pre-video signal to a post-video signal**,
    - said second circuit board being **positioned in a stacked arrangement** with respect to said first circuit board,
    - said second plane of said second circuit board being **substantially parallel** to said first plane of said first circuit board;

Claim 2 of the ´052 Patent (cont.)

- …
- a lens mounted in said housing, said lens being integral with said imaging device, said lens focusing images on said array of CMOS pixels of said image sensor;
- a video screen, said video screen being electrically coupled to said second circuit board, said video screen receiving said post-video signal and displaying images from said post-video signal; and
- a power supply mounted in said housing, said power supply being electrically coupled to said first circuit board to provide power to said array of CMOS pixels and said timing and control circuitry, said power supply also being electrically coupled to said second circuit board to provide power thereto;
- wherein **a largest dimension of said image sensor along said first plane is between 2 and 12 millimeters**.

Swift (Ex. 1005)

- Describes APS CMOS Camera-on-a-Chip Design
  POR at 14-16, Sur-reply at 3-8
  - Same APS-type sensor disclosed in *Laser Focus World* article (Ex. 1048)
  - Also same Fossum camera-on-a-chip disclosed in Background section and *BusinessWeek* article (Ex. 1060)
    POR at 35-38
- Also describes CCD embodiments
  POR at 14-16, Sur-reply at 8-11
- **BUT** does not show off-chip pre- to post-image processing for an APS CMOS sensor
  POR at 14-16, 35-38, Sur-Reply at 11-13



Swift, Fig. 4

jitter controls. By consolidating many functions and reading images in a more efficient way, it requires one-hundredth the power of a CCD-based system. And the chip does its own conversion from analog to digital for output on computer monitors or disk storage. About all it needs is a power source and a lens to focus light on it.

Ex., 2039 at 2, Ex. 1060 at 54 (highlighted)

Swift Does Not Show CMOS Sensor with Off-Chip Pre- to Post-Image Processing

- POSITA understands that *Swift's* multi-circuit-board system architecture is consistent with CCD imager architecture, not CMOS imagers.

POR at 14-16, 25-27; Sur-Reply at 11; Lebby Decl. at ¶¶ 97-98.

- Petitioner fails to show Swift's processing circuitry converts a pre-video signal to a post-video signal, as required by claim 2

POR at 35-38; Sur-Reply at 12; Lebby Decl. at ¶¶ 106-112.

  - Swift's vague description of "various circuitry":

of the intermediate bore 23. A further printed circuit board 53 is mounted on the first printed circuit board 52, substantially at right angles thereto. Various circuitry components are mounted on the circuit board 53, to provide power to the image sensor 51, process image signals received therefrom, and also to process audio signals from a miniature microphone 54 which is mounted within the radially extending passage 28 and connected to the printed circuit board 52 and/or 53. A cable 55 is connected to

Swift at 9:7-14.

Ricquier (Ex. 1033/1038)

- Describes **passive** CMOS image sensor image sensor "specifically designed for use in industrial machine vision applications"

  Ex. 1038 at 8; Sur-Reply at 13,15

- Describes "sensor architecture that can be used as a module in further sensor systems on a **single chip**."

  Ex. 1038 at 9; POR at 17, 34-35

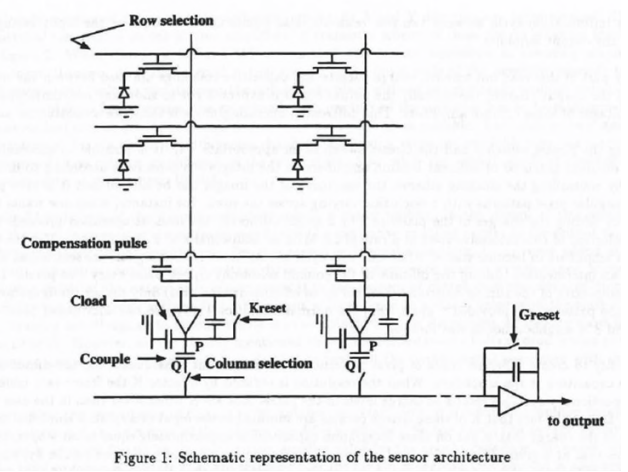


Figure 1: Schematic representation of the sensor architecture

Ex. 1038 at 9.

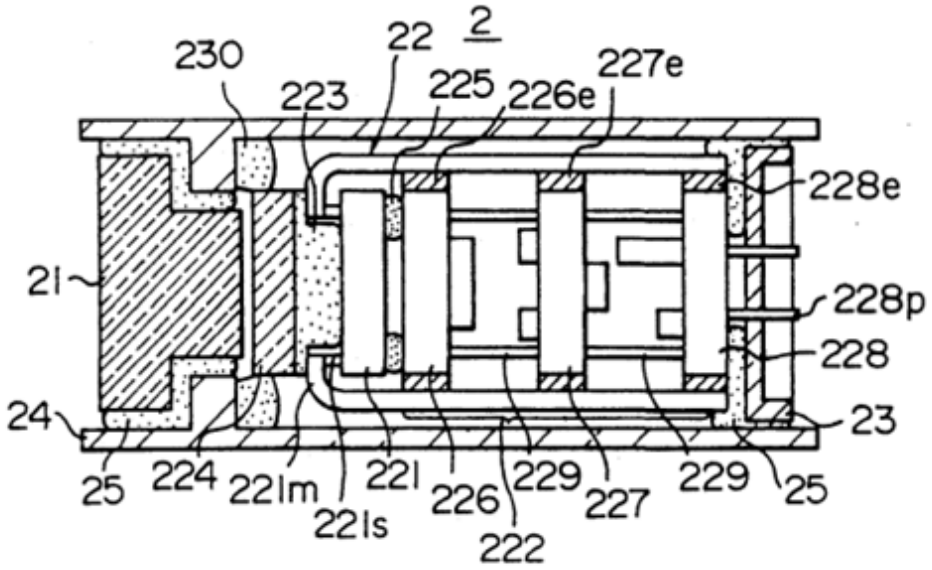
- Ricquier demonstrates that a POSITA **would not** have been motivated to combine with Swift:

the image acquisition rate is increased in inspection tasks or when tracking can be performed faster in assembly tasks, the production volume can be increased accordingly. A CMOS technology was chosen because it offers the selective addressability together with the possibility of further cointegration of processing electronics on the same chip.

Ex. 1038 at 8;
POR at 16-17, 28-30, 34-35;
Sur-Reply at 15-17.

Suzuki (Ex. 1015)

FIG. 2



Ex. 1015, Fig. 2.

- Conventional **CCD** device — POR at 17-18; Sur-Reply at 14; Lebby Decl. ¶¶104-116.
- Cited for stacked arrangement of circuit boards
- **BUT** this arrangement of circuit board incompatible with Swift's CMOS sensor embodiment — POR at 17-18, 35-36; Sur-Reply at 14.
- **BUT** POSITA would not have combined Suzuki with Swift and Ricquier — POR at 21-25; Sur-Reply 14-21.

Larson (Ex. 1029)

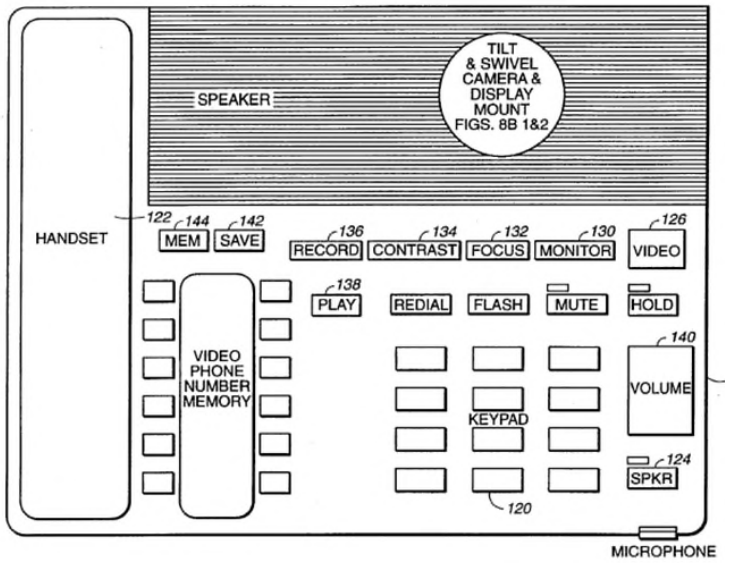
- Video phone with **CCD** camera

POR at 18-19,
Lebby Decl. ¶105

- Cited to address deficiencies in other cited references as to disclosure of a physical camera within same housing as the video monitor

- **BUT** POSITA would have used Larson's CCD image sensor, not Swift's CMOS, at the time
  - Record evidence demonstrates CCD sensor had superior performance; was mature technology at the time.

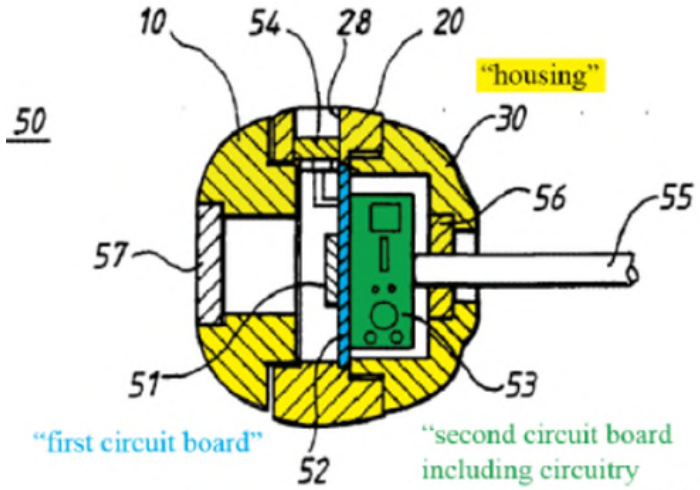
POR at 38-39, Sur-Reply at 21-23,
Lebby Decl. ¶127



Ex. 1029, Fig. 8A

References Fail to Disclose Imaging Device with Requisite Dimensions

- Suzuki's imager is not arranged in the claimed manner
- Petitioner fails to explain what modifications to Swift would result in imager with Suzuki's dimensions
- Dimensions of Swift's camera along the plane of the image sensor would not change regardless of how the circuit board 53 was oriented relative to board 52:

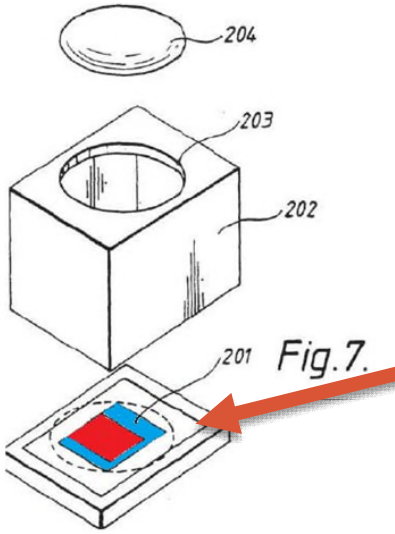


Petition at 4

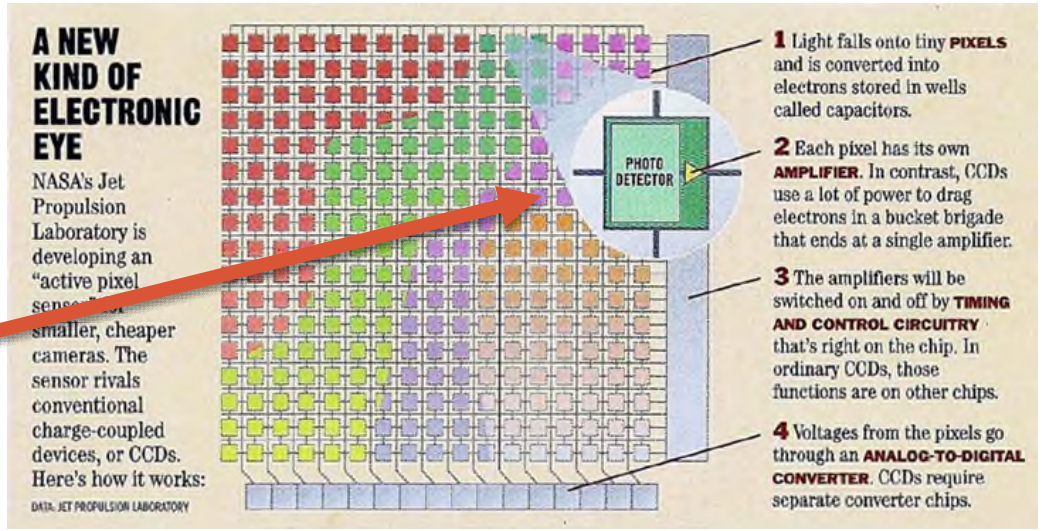
POR at 22-23, Lebby ¶ 115,
Sur-Reply at 16-20

POSITA Would Not Have Combined References to Arrive at Claim 2

- Swift's sensor **directly cites** to Fossum's camera on a chip.
  - Has integrated timing and control circuitry and analog-to-digital circuitry and an asymmetrically located pixel array.



Lebby ¶ 117 (annotating Fig. 7 of Ex. 1005)



Ex., 2039 at 3, Ex. 1060 at 55

- **BUT** no evidence in the record that a POSITA would have been motivated to de-integrate these features of the Swift/Fossum camera on a chip or to arrange them as required in claim 2

POR at 25-27, Lebby Decl. ¶ 117

Petitioner Fails to Demonstrate It Would Have Been Obvious to Combine the Asserted References to Yield Claim 2

Petitioner asserts:

- References are in the "same field of art"

  Petition at 22

- Ricquier is reasonably pertinent to the problem of arranging circuitry to "minimize the device's size or profile area"

  Petition at 22

- Ricquier adds flexibility in selecting from the several design choices for placing circuitry

  Petition at 23

- **BUT** references that are analogous art does not automatically mean a POSITA would be motivated to combine them

  POR at 27-28

- **NOT TRUE.** Ricquier is silent on "minimizing the device's size or profile area"

  POR at 28-29, Sur-Reply at 15-17

- **BUT** this analysis is tainted by hindsight bias

  POR at 30-35, Sur-Reply at 15-17

- **CANNOT** be a "design choice" because claimed arrangement solved a particular problem and gave rise to unexpected results

  POR at 31, Lebby ¶110, Sur-Reply at 16

Secondary Considerations Demonstrate Non-Obviousness of the Challenged Claims

Industry Skepticism

- Jeffrey Adair declaration (Ex. 1003 at 84-85) in prosecution history of patent family member
- Demonstrates "great skepticism" within the medical industry about using CMOS technology in medical imaging applications.
- Mr. Adair adds that CMOS imagers have a reputation of producing poor quality imaging that is not suitable for medical imaging applications, and that reputation was well known in the industry.

8. There has been great skepticism in the industry as to the capability to use CMOS technology in medical imaging applications. CMOS imagers have been characterized as not being capable of producing high quality images. Despite this skepticism, we were able to locate companies developing CMOS technology that might be usable within an imaging device configured as described in Paragraph 7 above.

Ex. 1003 at 84–85.

POR at 63

Unexpected Results

- Adair Declaration (Ex. 1003 at 84-85) demonstrates unexpected results:
- Improved RFI performance from using remote CMOS image processing circuitry.
- Unexpected result is **not merely** that the processing circuitry can be placed in a remote control box.
- Rather, the unexpected result is that the processing circuitry can be ***so close*** that it is "**adjacent to the pixel array**" without any RFI or shielding.

10. During our testing of the devices claimed in this invention, we discovered an unknown, but very important advantage that our device has over CCD imagers. This advantage is the capability of our device to reject radio frequency interference (RFI) which is emitted by electrosurgical generators used during surgery. In many surgical procedures, an endoscope is used in order to view the surgical area while another device, such as an electrosurgical generator, is used to actually manipulate (*i.e.*, cut or cauterize) the tissue.

11. CCD devices cannot be used near an electrical surgical generator without requiring significant shielding for the CCD device. Such shielding requires intense grounding techniques for the CCD camera cables/conductors which trail the CCD imager, and also grounding for the actual CCD pixel array. These shielding techniques not only add significantly to the size of the CCD device, but also to the overall cost of the CCD camera system. Even when such shielding is incorporated, RFI levels are only brought to a reasonable level which may still result in an obstructed view of the surgical area.

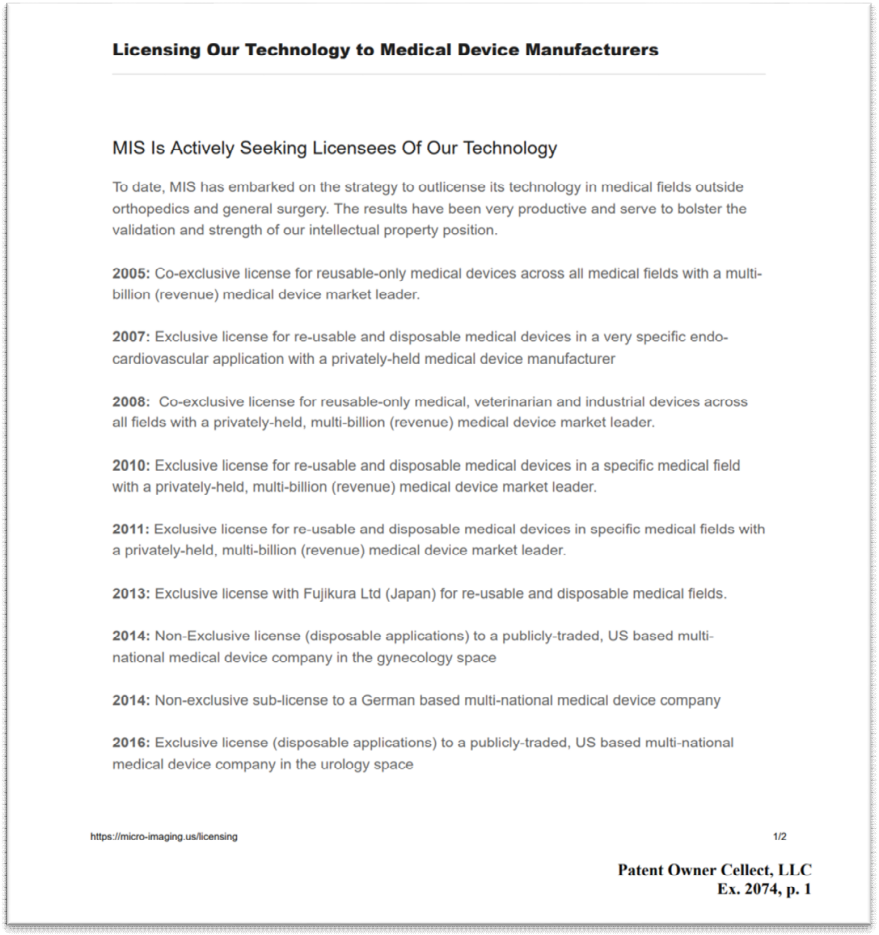
12. After testing several types of CMOS configurations, we concluded that remoting the processing circuitry from the CMOS imager and timing and control circuits eliminated the need for shielding. In other words, we found that this configuration was not susceptible to RFI. Such an unexpected result allowed

16. In addition to the configuration in which the pixel array and the timing and control circuit is placed on a single plane, we also observed the same advantageous results with respect to RFI rejection when we placed the CMOS pixel array by itself on one plane, and connected the timing and control circuitry to the pixel array on a second plane spaced from the pixel array. In this configuration, the processing circuitry was also remoted in either a remote control box or on circuit boards separated from, but adjacent to the pixel array. This particular feature is specifically claimed in Claim 30.

Ex. 1003 at 85–86 (excerpt)

POR at 64

Commercial Success and Licensing of the Patent Family



Licensing Our Technology to Medical Device Manufacturers

MIS Is Actively Seeking Licensees Of Our Technology

To date, MIS has embarked on the strategy to outlicense its technology in medical fields outside orthopedics and general surgery. The results have been very productive and serve to bolster the validation and strength of our intellectual property position.

2005: Co-exclusive license for reusable-only medical devices across all medical fields with a multi-billion (revenue) medical device market leader.

2007: Exclusive license for re-usable and disposable medical devices in a very specific endo-cardiovascular application with a privately-held medical device manufacturer

2008: Co-exclusive license for reusable-only medical, veterinarian and industrial devices across all fields with a privately-held, multi-billion (revenue) medical device market leader.

2010: Exclusive license for re-usable and disposable medical devices in a specific medical field with a privately-held, multi-billion (revenue) medical device market leader.

2011: Exclusive license for re-usable and disposable medical devices in specific medical fields with a privately-held, multi-billion (revenue) medical device market leader.

2013: Exclusive license with Fujikura Ltd (Japan) for re-usable and disposable medical fields.

2014: Non-Exclusive license (disposable applications) to a publicly-traded, US based multi-national medical device company in the gynecology space

2014: Non-exclusive sub-license to a German based multi-national medical device company

2016: Exclusive license (disposable applications) to a publicly-traded, US based multi-national medical device company in the urology space

https://micro-imaging.us/licensing 1/2

Patent Owner Cellect, LLC
Ex. 2074, p. 1

Ex. 2074 at 1.

POR at 60-61

Additional Slides

Claim 3 and 7 of the '052 Patent

- 3. An imaging device comprising:
  - a housing;
  - **an image sensor** mounted in said housing, said image sensor including **a planar substrate** having a length and a width thereto, wherein said length and width of **said planar substrate define a first plane**, said planar substrate including **an array of CMOS pixels thereon**, wherein a plurality of CMOS pixels within said array of CMOS pixels each include an amplifier, said image sensor further including **a first circuit board** having a length and a width thereto, wherein said length and width of said first circuit board **define a second plane**, **said first circuit board including timing and control circuitry thereon**, said timing and control circuitry being coupled to said array of CMOS pixels, said first circuit board being positioned in **a stacked arrangement** with respect to said planar substrate, said second plane of said first circuit board being **substantially parallel** to said first plane of said planar substrate, said image sensor producing a pre-video signal;
  - **a second circuit board** mounted in said housing, said second circuit board being electrically coupled to said planar substrate and to said first circuit board, said second circuit board having a length and a width thereto, wherein said length and width of said **second circuit board define a third plane**, **said second circuit board including circuitry thereon to convert said pre-video signal to a post-video signal**, said second circuit board **being offset** from said first circuit board and from said planar substrate, said third plane of said second circuit board being **substantially parallel** to said second plane of said first circuit board and to said first plane of said planar substrate;
  - a lens mounted in said housing, said lens being integral with said imaging device, said lens focusing images on said array of CMOS pixels of said image sensor;
  - a video screen, said video screen being electrically coupled to said second circuit board, said video screen receiving said post-video signal and displaying images from said post-video signal; and
  - a power supply mounted said housing, said power supply being electrically coupled to said planar substrate to provide power to said array of CMOS pixels, said power supply also being electrically coupled to said first circuit board to provide power to said timing and control circuitry, said power supply also being electrically coupled to said second circuit board to provide power thereto;
  - wherein a largest dimension of said image sensor along said first plane is between 2 and 12 millimeters.
- 7. The imaging device of claim 3, wherein:
  - said image sensor has a generally square shape along said first plane.

Hybrid CCD/CMOS Image Sensors Use CCD Pixels

- Patent describes Hybrid CCD/CMOS ('052 Patent at 2:35-56)
- Based on new development and not modifying an existing CCD device with a CMOS pixel array
- CCD/CMOS hybrid features a CCD pixel array
- Challenged Claims recite a CMOS active pixel arrangement
  - Law is clear that inventors' path is not a basis for obviousness
    - *Otsuka Pharmaceutical Co., Ltd. v. Sandoz, Inc.*, 678 F. 3d 1280, 1296 (Fed. Cir. 2012);
    - *Ortho-McNeil Pharmaceutical v. Mylan Labs.*, 520 F. 3d 1358, 1364 (Fed. Cir. 2008).