UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SAMSUNG ELECTRONICS CO., LTD., AND
SAMSUNG ELECTRONICS AMERICA, INC.,
Petitioners,

v.

CELLECT, LLC,
Patent Owner.

Case IPR2020-00512
U.S. Patent No. 9,198,052

PATENT OWNER CELLECT, LLC SUR-REPLY

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I. Introduction

Since the Board's Institution Decision (Paper 14, "DI"), Patent Owner has introduced expert testimony and contemporaneous articles into the record that fully rebut Petitioner's contention that the cited references, *Swift*, *Ricquier*, *Suzuki and Larson* render obvious Claim 2 ("the Challenged Claim") of U.S. Patent No. 9,186,052 (Ex. 1001, "the '052 Patent").

Petitioner's reasons for combining the asserted references are rely improperly on hindsight and lack a rational underpinning. Contrary to Petitioner's assertions, a POSITA at the time of the invention would not have de-integrated components of the newly arrived CMOS camera-on-a-chip, including pre- to post-image processing circuitry, and place it onto separate circuit boards because such an arrangement would have increased the overall system size, add costs, and reduce performance. Indeed, Petitioner's expert could not dispute these fundamental fact sand concedes that he did no analysis or comparison regarding the performance characteristics and image quality from different sensor types (CCD, passive CMOS, APS CMOS, CID etc.), configurations, and sizes, and was not aware of design trends that would have guided a POSITA at the time of the invention. *See, e.g.*, Neikirk 3/2/21 Tr. (Ex. 2103) at 121:18-24; 162:21-163:17. Only by using the Challenged Claim as a roadmap would a POSITA have been led to de-integrate the pre- to post- image processing of the Fossum CMOS camera-

on-a-chip design cited and used in *Swift*.

Petitioner also fails to explain why a POSITA would have looked to *Suzuki* and *Ricquier* (for all grounds) for the purpose of making the miniature camera in *Swift* even smaller. In particular, Petitioner's reliance on *Suzuki* and its description of a CCD image sensor having a length between 8.5 mm and 10 mm, is meaningless because *Suzuki* achieved those dimensions using an entirely different design than claimed or even envisioned in Petitioner's cobbling together of *Swift*, *Suzuki*, and *Ricquier*. Accordingly, Patent Owner respectfully submits Claim 2 is patentable.

II. Petitioner's Obviousness Analysis Ignored Inconvenient Facts and Misapplied the Law

Petitioner's Reply confirms that its obviousness analysis was inconsistent with how a POSITA would have understood the cited references at the time of the invention. For example, Petitioner consistently relies on vague disclosures to argue that a POSITA would have understood those disclosures to encompass the world while selectively ignoring portions of the references relied upon which teach away from the very modifications and proposed combination.

Nor does Petitioner make any attempt to explain the technical details of the proposed combination or how they modifications would have been obvious to a POSITA. Instead, Petitioner merely argues that because a POSITA could have constructed the Challenged Claim without explaining why a POSITA would have

done so at the time of the invention. *See Personal Web Technologies, LLC v. Apple, Inc.*, 848 F. 3d 987, 993-994 (Fed. Cir. 2017) (that two references *could be* combined is "not enough" to "imply a motivation to pick out those two references and combine them to arrive at the claimed invention"); *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated* to make the combinations or modifications of prior art to arrive at the claimed invention.") (emphasis original).

A. *Swift*

1. A POSITA Understands that *Swift* Describes an APS CMOS Camera-on-a-Chip Design

In the POR, Patent Owner submitted numerous articles and expert testimony demonstrating that a POSITA would have understood *Swift* do disclose a security camera with a CMOS APS camera-on-a-chip image sensor. *See, e.g.*, POR at 16; Lebby Decl. ¶¶ 106-12.

In Reply, Petitioner incorrectly argues that *Swift* only describes a "***generic*** disclosure of 'CMOS/APS (Active Pixel Sensor) type'" with off-chip processing circuitry (*e.g.*, board 53). Reply at 4 (emphasis added). That is not correct. *Swift* expressly states that the design utilizes Dr. Fossum's CMOS/APS article for camera-on-a-chip APS CMOS image sensor. *Swift* at 10:4-6 (citing Dr. Fossum's article in Laser Focus World). A POSITA would therefore understand *Swift* to use

camera-on-a-chip APS CMOS design—which was universal at the time of the invention. Ex. 2053-55. Even if one were to ignore the explicit citation to Dr. Fossum's article, however, a POSITA would still understand that a "***generic***" APS CMOS image sensor at the time was a camera-on-a-chip, based on industry guidance and trends, which Petitioner's expert concedes he did not analyze. POR at 21; Lebby Decl., ¶¶ 100-103, 107, 108, 118-119.

Petitioner's theory that ambiguity in *Swift* is an invitation to ignore how a POSITA would understand *Swift* is flawed. *Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("[O]bviousness concerns whether a skilled artisan not only *could have made* but *would have been motivated* to make the combinations or modifications of prior art to arrive at the claimed invention.") (emphasis original). For example, Petitioner provides a list of possibilities for how *Swift* might be construed using hindsight gleaned from the '052, ignoring what it actually discloses to a POSITA. Reply at 6-7. In contrast to Petitioner's strained reading of *Swift*, Dr. Lebby provides several reasons as to why Dr. Fossum's APS CMOS imager represents the universal camera-on-a-chip design for CMOS imagers when *Swift* was filed:

- Industry broadly equated APS CMOS imagers with camera-on-a-chip design; Ex. 2050; 2060; Ex. 2054.

- Dr. Fossum, specifically cited in *Swift*, touted the benefits of camera-on-a-chip design, due to its overall reduced size, lower cost, and better performance; Ex. 2053-55.
- Numerous articles touted the lower cost benefits of the camera-on-chip design providing for integration of image processing as well as additional circuitry; Ex. 2060; Ex. 2054.

Additionally, Figure 7 in *Swift* (shown below with highlighting added) depicts an imaging chip having an off-axis pixel array (in red), consistent with typical camera-on-a-chip designs where additional space on the chip (in blue) is allocated for other integrated circuit components, including timing and control and pre- to post- image processing circuitry. Petitioner's contention (Reply at 5-6) that *Swift* does not specifically annotate the red and blue regions is of no moment as a POSITA would readily recognize and appreciate that an APS CMOS image sensor would not be fabricated with empty space to simply add costs and reduce yields. Lebby Decl. ¶ 106.

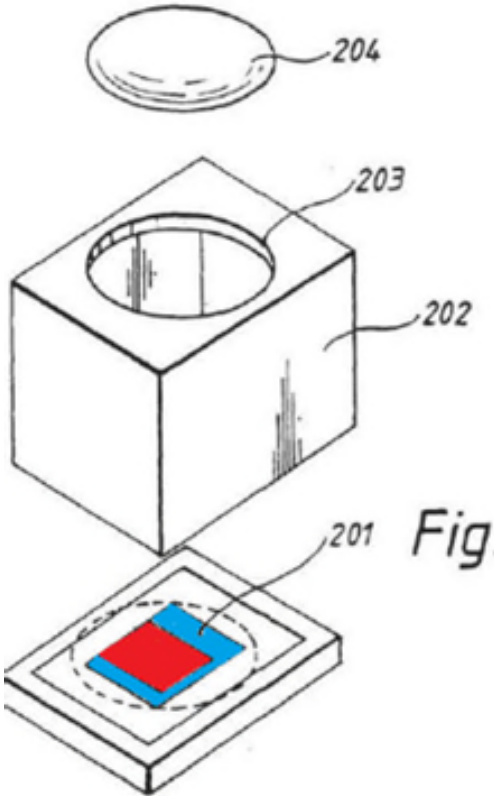

Fig.7.

Petitioner also misrepresents the record, arguing that PO conceded that conventional CMOS APS image sensors at the time of the invention did not have on-chip timing and control and pre- to post- image processing. Reply at 4. The record evidence plainly demonstrates the contrary, as explained by Dr. Lebby based on his experience as well as multiple industry articles. *See, e.g.*, Lebby Decl. ¶¶ 81-91; Ex. 2050; 2054; 2056. Notably, Petitioner references an article titled "Camera on Chip," touting the benefits of camera-on-a-chip design, yet maintains that CMOS APS imagers did not utilize the camera-on-a-chip design. The record evidence fully supports and confirms Patent Owner's position - Petitioner's suggestion that the words "ability" or "possible" refers to some future

development needed to integrate image processing mischaracterizes the references and negates the teaching of multiple articles – that Petitioner never challenged – rings hollow.

As explained by Patent Owner and Dr. Lebby, in 1997, CCD image sensors dominated the market because of their superior image quality, and camera-on-chip APS CMOS sensors needed further development to improve image quality, including line widths, resolution and fixed pattern noise—not because the CMOS camera-on-chip needed further work. Ex. 2050 at 4 ("As the CMOS sensor array technology evolves, and process line widths continue to decrease, we expect to see: (1) CMOS image sensor arrays will become standard cells much like any other chip layout component."). Furthermore, Petitioner's reliance on references that focus on development and improvement of the pixel array in isolation and *passive* CMOS sensors are, therefore, inapposite. Reply at 5. For example, Petitioner refers to Ex. *Stam* (Ex. 1043) as an example of a CMOS sensor that is not a camera-on-a-chip, but *Stam* actually cites to (at 4:66-5:2) the use of APS CMOS sensor from Photobit LLC, a company founded by Dr. Fossum and which manufactured APS CMOS camera-on-a-chip sensors. Petitioner also refers to *Zarnowsky* (Ex. 2007) which describes partial integration of electronics and when read in its context confirms that it includes pre- to-post- image processing, and describes potential integration significantly more electronics such as memory,

compression logic, smart sensors, and ASIC subcells, among other components, *Id.* at 138-139.

2. A POSITA Understands that *Swift* Also Describes CCD Embodiments

A POSITA understands that *Swift* also describes embodiments using a CCD image sensor based on figures showing circuitry on separate circuit board, a hallmark of CCD image sensors, and based on Swift's description of 12 volt camera modules. More specifically, a POSITA would understand that *Swift*'s description regarding the use of 12 volts to power the camera module, and *Swift's* characterization of this voltage as "low", would mean that the embodiment describes a CCD camera module. Lebby Decl. ¶¶ 98, 106.

In a half-hearted effort to avoid the necessary implications that *Swift* describes embodiments directed to CCD image sensor, Petitioner contends (Reply at 6-7) that *Swift* cannot be a CCD image sensor because it does not mention CCD and states that an APS CMOS sensor is "preferable." This argument, however, is inconsistent with Petitioner's argument that *Swift* is not limited to Dr. Fossum's camera-on-a-ship design because *Swift* only provide a generic reference to "image sensor" and broad teachings that are not limited to a specific embodiment. Reply at 3-4. Under Petitioner's interpretation, Swift's purported teaching of a generic image sensor exactly supports Patent Owner's explanation that Swift's multi-circuit board embodiments reflect the industry-dominant CCD imager design,

whereas other embodiments—such as where only a single circuit board is used—are consistent with the Fossum's camera-on-a-chip, which *Swift* uses. *See Swift* at 9:20-21 ("A single circuit board (e.g. circular) may be provided, instead of the two circuit boards 52 and 53."). A POSITA would understand Swift to disclose a security camera using either the Fossum camera-on-a-chip design or the dominant CCD design, but not as a deconstructed Fossum CMOS imager, as Petitioner suggests. Lebby Decl. ¶¶ 97-98.

Further, Petitioner ignores how a POSITA understands how the term "image sensor" was understood in 1995 (when *Swift* was filed) and at the time of the invention. Petitioner does not dispute that the CCD imager was the most common solid-state imaging device for consumer imaging devices, such as video cameras and point and shoot cameras, as well as for security and surveillance applications, at the time of the invention. Ex. 2061 (Lee) at 1:12-14; Ex. 2036 at 6, Fig. 7.5; *see also* Ex. 2053 at 2.

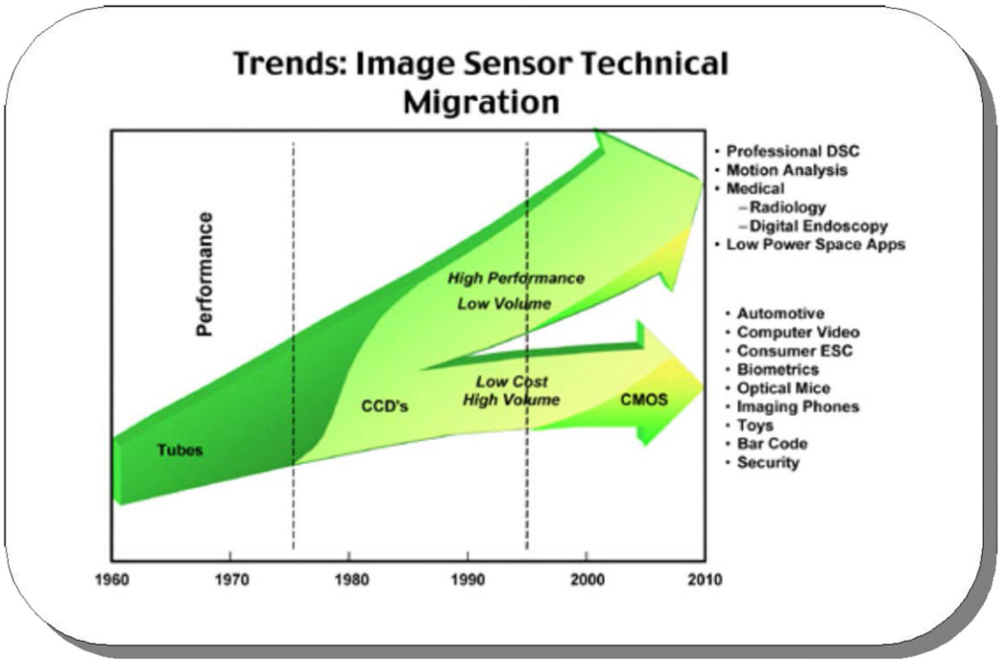

Figure 7.5: Image Sensor Migration and Materials
Source: Kodak

Ex. 2036 at 6, Fig. 7.5 (depicting market shares of imaging tubes (forest green) against CMOS imagers (neon green) and CCD imagers (green-yellow)). CMOS imagers only started to gain market share in the late 1990s, with limited availability. Lebby Decl. ¶¶ 87-88.

Additionally, Petitioner's contention that *Swift*'s discussion of 12 volts refers to the power supply for the entire camera module is irrelevant. Even if the 12 volt supplies power to the entire camera module, *Swift* does not state that another voltage is supplied to the image sensor, and a POSITA would know that 12 volts is exceedingly ***high*** for an APS CMOS camera module. Lebby Decl. ¶ 106. In contrast, 12 volts would only be considered ***low*** for a CCD camera module. Ex. 1001 at 2:48-51; Lebby Decl. ¶¶ 98; 106. Thus, for this reason as well, a POSITA

understands that *Swift* describes a CCD camera module.

Accordingly, a POSITA would understand *Swift* describes CCD embodiments which use off-chip circuitry, including processing circuitry.

3. *Swift* Does Not Show Off-Chip Pre- to Post- Image Processing for an APS CMOS Sensor

The Reply maintains that *Swift*'s generic disclosure shows pre- to post-video processing of an APS CMOS sensor on a separate circuit boards. Reply at 3-4. *Swift* does not provide any such express description for several reasons.

First, a POSITA would understand that *Swift* describes CCD embodiments based on the figures showing separate circuit boards and use of 12 volts on these boards (as described above). A POSITA therefore would have understood that the embodiment showing separate circuit boards would have used CCD image sensors. Petitioner's argument (Reply at 4, 6) that *Swift*'s description of Figure 2 and separate circuits boards cannot refer to CCD image sensors is wholly inconsistent with its argument "*Swift* is not limited to any specific embodiment" (Reply at 4 (citing *Swift* 19:8-21)) and not consistent with the understanding of a POSITA. Lebby Decl. ¶¶ 97-98. As explained above, a POSITA would understand that *Swift* describes embodiments with CCD image sensors and figures depicting image sensors with separate circuit boards would be understood to be CCD camera modules which were standard in miniature cameras and surveillance systems. Lebby Decl. ¶¶ 97-98.

Second, even assuming a CMOS image sensor is used with separate circuit boards with additional image signal processing, Petitioner has not shown that the processing circuitry on *Swift*'s circuit board 53 converts a pre-video signal to a post-video signal. There are a number of different types of image processing circuitry (including conditioning or pre-video, further post-video processing), and *Swift* does not disclose the claimed processing circuitry of circuit board 53. Lebby Decl. ¶¶ 106-12. In particular an APS CMOS camera on a chip design (which converts pre-video to post-video) would still include separate post-video image signal processing. As explained above, a POSITA would understand that Figure 7 depicts a camera-on-chip design architecture:

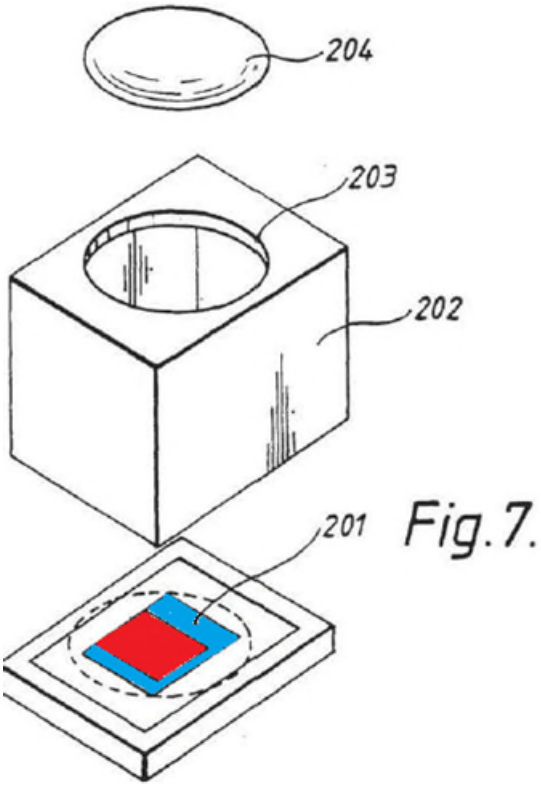

Fig. 7.

Petitioner's argument that purported ambiguities in *Swift* does not permit a POSITA to ignore the express teaching of APS CMOS camera-on-a-chip in *Swift* and combine *Swift* with any known references. *Metalcraft of Mayville, Inc. v. Toro Co.*, 848 F.3d 1358 (Fed. Cir. 2017) ("not enough [] to merely demonstrate that elements of the claimed invention were independently known in the prior art. Often, every element of a claimed invention can be found in the prior art… Knowledge of a problem and motivation to solve it are entirely different from motivation to combine particular references.")

B. *Ricquier*

Ricquier only discusses a ***passive*** CMOS image sensors intended to be used in machine vision applications and not miniature cameras or surveillance systems. Neikirk Tr. (Ex. 2104) at 82:11-17; 91:5-92:7. Although Petitioner relies on *Ricquier* as the motivation to place timing and control onto a separate circuit board from the CMOS pixel array for flexibility in designing a "a more compact camera," *Ricquier* is completely silent with respect to minimizing a device's size or profile area. Reply at 8-9; *Lebby*, ¶ 118. Indeed, Petitioner's expert concedes that *Ricquier* does not describe any details regarding the physical arrangement of the components in *Ricquier* or if the overall size would even be reduced. Neikirk Tr. (Ex. 2104) at 104:5-106:16. In fact, in order to minimize device size for a CMOS imager, the well-known solution at the time was to move toward a

"camera-on-a-chip." Lebby, ¶ 118 (citing Ex. 1048 at 8 ("Yet, on-chip integration is the key to achieving future camera miniaturization."); Ex. 1060 at 1 (describing the switch from "bulky" CCD imagers to "tiny" CMOS imagers "[w]ith all the smarts on one chip instead of several")).

Additionally, Petitioner selectively ignores that express statements in *Ricquier* regarding its goal to design a fully integrated system (*i.e.*, integration of all circuitry) for machine vision application to adopt the APS CMOS camera-on-a-chip design.

C. Suzuki

A POSITA would understand that Suzuki describes a CCD architecture, consistent with state of art in 1991 (prior to introduction of CMOS image sensors). Petitioner's argument (Reply at 118) that CMOS sensors were invented prior to 1991 misses the point. A POSITA knew that based on the state of the art in 1994, including standard CCD and CMOS architecture, image quality of CCD and CMOS, and intended application, a POSITA would understand that Suzuki is not a CMOS image sensor and would have been a CCD image sensor. *See, e.g.*, Neikirk Tr. (Ex. 2103 at 177:4-23); Lebby Decl. ¶¶ 104-116.

III. Ground 1: *Swift* in View of *Ricquier* and *Suzuki* Fails to Disclose an Imaging Device With the Requisite Dimensions

Notwithstanding the fact that Petitioner argues *Ricquier* motivates a POSITA to place timing and control on a separate board from the CMOS pixels

(contrary to Claim 2), Petitioner's proposed obviousness combination ignores the negative technical effects associated with the proposed combination, which undermines the purported motivations (*e.g.*, size, stability, flexibility, cost) for combining the references in the first place.

First, a POSITA would not have looked to or combined *Ricquier's* ***passive*** CMOS pixels with *Swift*. As discussed in detail above, based on *Swift* explicit reference to Dr. Fossum's ***active*** pixel sensor ("APS") CMOS imager. Petitioner does not explain why a POSITA reading *Swift* would have looked to *Ricquier's* ***passive*** CMOS image sensor. Petitioner does not dispute that *Ricquier's* ***passive*** CMOS do not provide the same image quality as APS CMOS, especially using *Ricquier's* test bench setup. Lebby Decl. ¶ 99. Indeed, Petitioner has not identified any credible motivation for doing so or how passive and active pixels could be combined.

Although Petitioner argues a POSITA would look to Ricquier because it purportedly provides the benefit of "flexibility to optimize circuitry placement for a more compact device and, because of Ricquier's express advantages of 'selective addressability' and 'multiple resolutions…[and] data rates up to 10 MHz'" these stated goals are illusory. Selective addressability and multiple resolutions are all basic to all APS CMOS camera-on-chip designs, including Dr. Fossum's camera-on-a-chip design cited in *Swift*. Ex. 2050; 2053-55. Looking to *Ricquier* passive

pixels adds nothing and only serves to offer poorer performance compared Fossum's APS CMOS camera-on-chip. Lebby Decl. ¶ 10.

Additionally, *Ricquier's* purported benefit of providing smaller size is also a red herring. Indeed, Petitioner's expert concedes that *Ricquier* makes no mention of reducing size. Neikirk Tr. (Ex. 2104) at 105:5-108:18. Further, separating and adding additional circuit boards runs counter to well-known principles that reducing size would be reduced by camera on chip. Lebby Decl. ¶ 118.

Petitioner's contention that *Ricquier* is also reasonably pertinent regarding flexibility in choosing where to locate components like timing and control circuitry is also flawed. The location and integration of these components are not a matter of "design choice" as a matter of law because the claimed arrangement solved a particular problem and gave rise to unexpected results. *See In re Chu*, 66 F.3d 292, 298–99 (Fed. Cir. 1995) (holding that a specific arrangement is not a matter of "design choice" where it solves a stated problem or provides unexpected results (citing *In re Rice*, 341 F.2d 309 (CCPA 1965); *In re Kuhle*, 526 F.2d 553, 555 (CCPA 1975)).

The claimed imaging device of the '052 Patent both solves the particular problem of further miniaturizing the CMOS "camera on a chip" and impacts the technical operation of the device. Lebby Decl. ¶¶ 5, 92. Petitioner's arguments that de-integrating the APS CMOS camera-on-a-chip design based on *Ricquier*

would have no effect because Ricquier provides sufficient data rates up to 10 MHz is also flawed. Reply at 7-15. *Ricquier* makes no comparison of the technical impact of separating components, and Petitioner has not shown how the ability to achieve data rates of 10 MHz for passive CMOS pixels applies to APS CMOS image sensors or is related in any way to the timing and control circuitry being realized off-chip.

Second, Petitioner fails to provide any basis on why a POSITA would rely on Suzuki to modify *Swift* to construct a CMOS image sensor having a maximum dimension between 2 and 12 mm. Instead, Petitioner simply argues that *Swift* would motivate a POSITA to make the image sensor "miniature." Reply at 1-12, 16. The desire for a small device, however, provides no guidance as to how a POSITA could have reduced *Swift's* large device (with a maximum dimension no smaller than 38 mm) down to between 2 and 12 mm given that Suzuki does not disclose the claimed arrangement of circuit boards and imager components or the arrangement associated with Petitioner's proposed combination. Lebby Decl. ¶ 113.

Petitioner's contention (Reply at 8) that a POSITA would have been motivated to apply the teachings of *Suzuki* to stack separate circuit boards is also contrary to the understanding of a POSITA. It was widely accepted at the time that the best way to reduce system size and cost was to integrate as much of the system

circuitry onto a single integrated circuit ("IC"). Lebby Decl. ¶¶ 110-12. Petitioner neither rebuts the record evidence showing that the overall size and space is reduced by using a camera-on-a-chip design, which allows for a more compact design and better performance (eliminating excessive connections and capacitance). Lebby Decl. ¶ 109.

Third, as explained above, Suzuki would be understood to be a CCD architecture and would not be combined with an APS CMOS camera-on-a-chip design. Moreover, even if Suzuki does not expressly state it is limited to a CCD device, a POSITA would not have looked to Suzuki's much older design to modify a later developed CMOS camera-on-a-chip design. The fact that a lot of different design factors exist in the abstract and could be applied to any device (Ex. 1045) does not make it obvious to select certain design features from certain references other than the Challenged Claim recites that combination of features. *Belden, Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1075 (Fed. Cir. 2015). Further, stacking components does not reduce the overall size as discussed above and it is undisputed that a camera-on-a-chip design provides a more compact overall size.

Additionally, Petitioner provides no basis why a POSITA would use an APS CMOS image sensor between 2 and 12 mm. There is nothing in *Swift* (or *Larson* discussed below) that suggests using an image sensor between 2 and 12 mm. Petitioner's expert concedes he did no analysis to determine the performance

characteristics and image quality of different sized image sensors (or differences between CCD and CMOS). Neikirk Tr. (Ex. 2103) at 121:18-123:24; 162:21-163:17. Rather, Petitioner argues that that *Swift* mentions "miniature" cameras and as a motivation to reduce size and using hindsight arrives at 2 to 12 mm. Reply at 1-12, 16. *Swift* only states that a maximum size of 38 mm is preferable. There is a large range of image sensor sizes below 38 mm,

Even assuming a POSITA would be motivated to simply make a sensor "small," Petitioner points to no reason why an image sensor smaller than 2 mm would not be used. *Ricquier* itself suggests that a much smaller size could be used. For example, Petitioner relies on *Ricquier's* ability to provide "multiple resolutions…[and] data rates up to 10 MHz" which *Ricquier* explains as "a maximal data rate of 10 MHz in the [1 pixel x 1 pixel] resolution" and further explains that "pixels arranged on a pixel pitch of 19 μm and realised in a 1.5 μm n-well CMOS technology," meaning that the image sensor could be an order of magnitude smaller than 2 mm.

Petitioner's argument that the 2-12 mm limitation is not entitled to patentable weight because it is a non-critical limitation is flawed. Reply at 20. The Specification of the '052 Patents states that image sensors as small as 1 mm could be used and for certain application like endoscopes, a more preferable range could be between 4 mm and 8mm:

> Image sensor **40** can be as small as 1 mm in its largest dimension. However, a more preferable size for most endoscopic procedures would dictate that the image sensor **40** be between 4 mm to 8 mm in its largest dimension.

Ex. 1001 at 9:23-26.

In other words, the size limitations are important depending on the particular application. Further, during prosecution the 2-12 mm limitation was added to distinguish prior art which lacked this important size limitation and which provides optimal size and performance characteristics (as described in the ’052 Specification), especially for certain devices such as endoscopes.

In contrast to the ’052’s explanation regarding the selection of image sensor size, Petitioner’s argument that it would be obvious to use a CMOS sensor between 2 and 12 mm is pure hindsight.

Fourth, nothing in Petitioner’s Reply resolves the deficiency in Petitioner’s case that a POSITA would not have modified *Swift*’s CMOS camera-on-a-chip to place its pre- to post- video processing circuitry off-chip. *See Belden Inc.,* 805 F.3d at 1073 (could-have-made rationale not sufficient for obviousness); *Personal Web Technologies, LLC,* 848 F.3d at 993-994 (same). As described above (*supra* II.A.3), Petitioner argues circuit board 53 converts pre- to –post- image processing, but *Swift* does not state that. To contrary, there are no details in *Swift* that explain what type of image processing is performed on circuit board 53.

As an initial matter, however, based on the architecture in Figure 2 and Specification in *Swift*, a POSITA would understand that particular embodiment to be a CCD image sensor powered by 12 volts (which would be too high for CMOS). Lebby Decl. ¶¶ 98, 106. Even if an APS CMOS image sensor were implemented in Figure 2, a POSITA, however, would understand that circuit board 53 refers to processing of a post-video image signal. For example, it was well-known that an APS CMOS camera-on-a-chip design with post-video output, referenced in *Swift*, provides better performance and lower cost than if it were de-integrated. Ex. 2060. Petitioner ignores this understanding of a POSITA based on these technical effects and simply assumes (with no detail) that *Swift*'s circuit board 53 performs pre- to post- image processing. This wrong as a matter of law. *See Belden Inc.*, 805 F.3d at 1073 (could-have-made rationale not sufficient for obviousness); *Personal Web Technologies, LLC*, 848 F.3d at 993-994 (same)

IV. Ground 2: *Larson* in View of *Swift, Ricquier*, and *Suzuki* Does Not Render Claim 2 Obvious Under 35 U.S.C. § 103

A. Petitioner Cannot Dispute its Combinations Result in Poorer Performance and Increased Costs

A POSITA would have not modified *Swift, Ricquier*, and *Suzuki* with *Larson*. *Larson* discloses a CCD camera, which at the time of the invention provided much better image quality and was the dominant image sensor technology at the time. Lebby Decl. ¶¶ 105, 126. Thus, to the extent a POSITA

modified *Larson* in view of *Swift*, a POSITA would have used *Larson's* CCD image sensor, which provided superior performance and was a mature technology especially for security and surveillance applications such as in *Swift*. Lebby Decl. ¶ 127.

Petitioner's argument (Reply at 23) that a POSITA would apply *Swift*'s miniature camera in Larson's CCD video telephone device, despite having no disclosure regarding the details of Swift's image sensors, is not credible. Indeed, *Swift* describes a camera that is 100, 80, 50 or potentially 38 mm in diameter provides no benefit or motivation to combine Larson with Swift [?]. Further, using the passive CMOS pixels in *Ricquier* would not provide sufficient image quality and Petitioner simply picks and chooses portions of *Larson, Swift, Ricquier and Suzuki* with no rationale basis for the reasons discussed above.

With respect to Larson, there is no reason to use a sensor between 2 and 12 mm based on Suzuki given it intended purpose of a desktop video telephone shown in Figure 8A (copied below). Indeed a larger CCD image sensor would provide far superior image quality in every respect and there are relatively no size constraints that would merit using a sensor between 2-12 mm (but for hindsight):

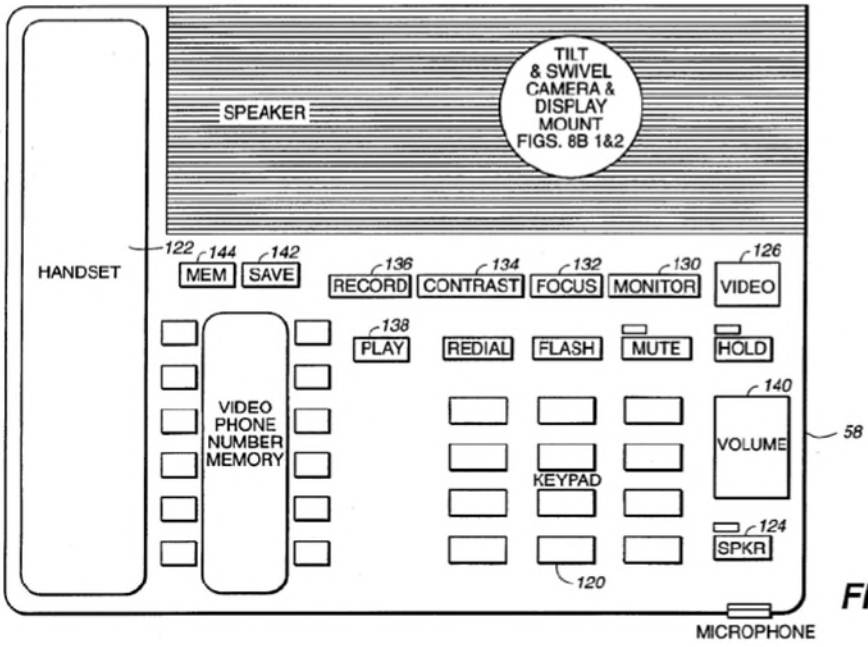

FIG._8A

Additionally, Petitioner's argument (Reply at 22) that APS CMOS sensors (not described in *Ricquier*) as providing lower noise than CCD is contradicted by record evidence. The one exception where APS CMOS has lower noise is with respect to EMI/RFI, but otherwise cannot match the performance of CCD imagers Ex. 1003 ¶¶ 10, 11 (pg. 85). Therefore, there is no basis to replace a CCD image sensor in Larson with a CMOS sensor.

V. Secondary Considerations Demonstrate Non-Obviousness of the Challenged Claim

Petitioner erroneously asserts that Patent Owner failed to provide the requisite nexus for the multiple examples of secondary considerations. Reply at 27. In fact, Patent Owner provided several express illustrations of the requisite nexus. *See, e.g.*, POR at 61 ("Current cameras and endoscopes (all types) have

remained unchanged for decades and degrade from 'Day 1'"); POR at 60 ("CCD devices cannot be used near an electrical surgical generator without requiring shielding for the CCD device [due to electromagnetic/radio frequency noise common in medical settings]. . . . After testing several type of CMOS configurations, we concluded that remoting processing circuitry from the CMOS imager and timing and control circuits eliminated the need for shielding…. This [claimed technology allows for flexible or rigid applications as a reusable or disposable with significant value.""").[1]

Petitioner attempts to suggest that the secondary considerations highlight other features not claimed in the Challenged Claims. Reply at 28-19. However, although secondary considerations may contain other features not found in the asserted claims, nexus still exists because the secondary considerations are due in part to the claimed invention—rearrangement of circuitry of a CMOS camera-on-a

[1] In 1997, CCD imagers provided vastly superior image quality (*e.g.*, better signal to noise) compared to CMOS sensors. In environments with significant EMI/RFI interference, such as in electrosurgical equipment and wireless devices, however, CCD needed significant shielding. CMOS was unexpectedly more resistant to EMI/RFI and generated lower ***EMI/RFI noise*** in these environments. Ex. 1003 ¶ 10, 11 (pg. 85); Ex. 2088 ¶ 17.

chip to create a small profile camera. *See In Ex parte Whirlpool Corp.*, IPR2013-008232 at 15-16 (P.T.A.B. Oct. 30, 2013) (informative) ("An invention may be praised or commercially successful for reasons other than the claimed invention but a nexus may still exist as long as it can be shown that such praise or success is also due in part to the claimed invention.").

Petitioner attempts to discredit the Adair Declaration but does not dispute the accuracy or veracity of the declaration. The Adair Declaration was contemporaneous with the prosecution of related earlier-issued patents, was accepted by the Patent Office, and expressly connects the evidence of nonobviousness with the claimed features, such as separation of circuitry from a CMOS camera-on-a-chip. Such a showing meets and exceeds the nexus requirements for secondary considerations. Moreover, the cases that Petitioner cites to support their "self-serving declaration assertion" are inapposite as they are not analogous. *See, e.g.*, *In re Cree, Inc.*, 818 F.3d 694, 702 (Fed. Cir. 2016) (rejecting a third-party's press release because it was not directed to the work of the inventors of the patent at issue); *Stride Rite Children's Grp. v. Shoes by Firebug*, IPR2017-01810, Paper 66, 51-52 (affording little weight to an expert testimony from the proceeding which "character[s] the reaction of others as reported to him by a non-declarant").

VI. Conclusion

Petitioner has failed to prove by a preponderance of evidence that Claim 2 of the ’052 Patent are unpatentable.

Respectfully submitted,

Dated: March 15, 2021

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CERTIFICATE OF COMPLIANCE WITH 37 C.F.R. § 42.24

This paper complies with the type-volume limitation of 37 C.F.R. § 42.24. The paper includes 5,121 words, excluding the parts of the paper exempted by § 42.24(a).

This paper also complies with the typeface requirements of 37 C.F.R. § 42.6(a)(ii) and the type style requirements of § 42.6(a)(iii)&(iv).

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CERTIFICATE OF SERVICE

The undersigned certifies, in accordance with 37 C.F.R. § 42.6(e), that service was made on the Petitioner as detailed below.

Date of service	March 15, 2021
Manner of service	Electronic Mail (scott.mckeown@ropesgray.com; james.l.davis@ropesgray.com, carolyn.redding@ropesgray.com, Samsung-Cellect-IPR@ropesgray.com)
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