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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/653,639	10/17/2012	Martin VORBACH	2885/162	6103

73481 7590 04/01/2015
Alliacense Limited LLC
4880 Stevens Creek Boulevard
Suite 103
San Jose, CA 95129

EXAMINER

ELAMIN, ABDELMONIEM I

ART UNIT	PAPER NUMBER
----------	--------------

2116

DATE MAILED: 04/01/2015

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 13/653,639	Applicant(s) VORBACH ET AL.	
	Examiner ABDELMONIEM ELAMIN	Art Unit 2116	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to Amendment filed on 10/30/2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 1 and 47-51. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☒ All b) ☐ Some *c) ☐ None of the:
1. ☒ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.
Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| 1. ☐ Notice of References Cited (PTO-892) | 5. ☒ Examiner's Amendment/Comment |
| 2. ☐ Information Disclosure Statements (PTO/SB/08),
Paper No./Mail Date _____ | 6. ☐ Examiner's Statement of Reasons for Allowance |
| 3. ☐ Examiner's Comment Regarding Requirement for Deposit
of Biological Material | 7. ☐ Other _____. |
| 4. ☐ Interview Summary (PTO-413),
Paper No./Mail Date _____. | |

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EXAMINER'S AMENDMENT

1. The present application is being examined under the pre-AIA first to invent provisions.
2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

IN THE SPECIFICATION:

Please amend the specification as follows:

On page 1, before "FIELD OF THE INVENTION," insert the following section:

--CROSS-REFERENCE TO RELATED APPLICATIONS

This application is a continuation of U.S. Pat. App. Ser. No. 12/570,984, filed on September 30, 2009, now US. Patent No. 8,312,301, which is a continuation of U.S. Pat. App. Ser. No. 12/257,075, filed on October 23, 2008, now US. Patent No. 8,099,618, which is a divisional of U.S. Pat. App. Ser. No. 10/469,909, filed on September 21, 2004, now US. Patent No. 7,444,531, which is a national phase of int. Pat. App. No. PCT/EP02/02402, filed on March 5, 2002, which claims priority to German Patent Application Serial No. DE 101 10 530.4, filed on March 5, 2001, the entire contents of each of which are expressly incorporated herein by reference thereto.--

3. Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for

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Allowance."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDELMONIEM ELAMIN whose telephone number is (571)272-3674. The examiner can normally be reached on MON - THUR 10:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ABDELMONIEM ELAMIN/
Primary Examiner, Art Unit 2116

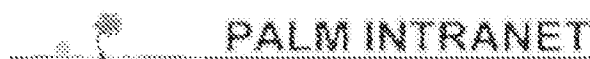
March 12, 2015

WEST Search History

DATE: Tuesday, March 10, 2015

Hide?	<u>Set</u> <u>Name</u>	<u>Query</u>	<u>Hit</u> <u>Count</u>
<i>Prior Art</i>			
	<i>DB=PGPB,USPT; PLUR=YES; OP=ADJ</i>		
☐	L13	(12 or 19) and (minimum near3 (clock or frequency))	34
☐	L12	L10 and ((clock or frequency))	0
☐	L11	L10 and (minimum near3 (clock or frequency))	0
☐	L10	12 and 19	0
	<i>DB=USPT; PLUR=YES; OP=ADJ</i>		
☐	L9	(5319772 5561792 5301306 5488715 5451892 5455931 5428746 5416434 5142684 5506981 5450574 4677433 5537581 5535377 5563928 5491814 5546568 5469561 5392435 5287292 5381543 5163146 5442774 5586270 5319771 5490059 5408639 5325516 5420865 5487092 5291529 5579353)![PN]	32
☐	L8	("5774704")[PN]	1
	<i>DB=PGPB,USPT; PLUR=YES; OP=ADJ</i>		
☐	L7	(minimum near5 (clock or frequency)) with multi\$1process\$4	20
☐	L6	L5 with (clock or frequency)	1
☐	L5	(pend\$7) with multi\$1process\$4	447
☐	L4	(minimum) with (pend\$7) with multi\$1process\$4	0
☐	L3	(minimum near5 (clock or frequency)) with (pend\$7) with multi\$1process\$4	0
	<i>DB=USPT; PLUR=YES; OP=ADJ</i>		
☐	L2	5774704[urpn]	121
	<i>DB=PGPB,USPT; PLUR=YES; OP=ADJ</i>		
☐	L1	5,774,704.pn.	1

END OF SEARCH HISTORY



Day : Thursday
Date: 3/12/2015
Time: 14:32:56

Inventor Name Search Result

Your Search was:

Last Name = BAUMGARTE

First Name = VOLKER

Application#	Patent#	PG Pub#	Status	Date Filed	Title	Examiner Name	Inventor Name
10297959	7003660	20040025005	150	06/19/2003	PIPELINE CONFIGURATION UNIT PROTOCOLS AND COMMUNICATION	ELAMIN,ABDELMONIEM	BAUMGARTE, VOLKER
10398546	7595659	20040128474	150	01/20/2004	LOGIC CELL ARRAY AND BUS SYSTEM	TAN,VIBOL	BAUMGARTE, VOLKER
10469909	7444531	20050066213	150	09/21/2004	METHODS AND DEVICES FOR TREATING AND PROCESSING DATA	ELAMIN,ABDELMONIEM	BAUMGARTE, VOLKER
10469910	Not Issued	20070299993	161	02/17/2005	Method and Device for Treating and Processing Data	MAMO,ELIAS	BAUMGARTE, VOLKER
10501845	8281108	20060090062	150	08/26/2005	RECONFIGURABLE GENERAL PURPOSE PROCESSOR HAVING TIME RESTRICTED CONFIGURATIONS	VICARY,KEITH	BAUMGARTE, VOLKER
10504684	8127061	20070150637	150	07/14/2006	BUS SYSTEMS AND RECONFIGURATION METHODS	CLEARY,THOMAS	BAUMGARTE, VOLKER
10523764	8156284	20070050603	150	08/02/2005	DATA PROCESSING METHOD AND DEVICE	THAI,TUAN	BAUMGARTE, VOLKER
11122500	8301872	20050223212	150	05/04/2005	PIPELINE CONFIGURATION PROTOCOL AND CONFIGURATION UNIT COMMUNICATION	ELAMIN,ABDELMONIEM	BAUMGARTE, VOLKER
12257075	8099618	20090100286	150	10/23/2008	METHODS AND DEVICES FOR TREATING AND PROCESSING DATA	ELAMIN,ABDELMONIEM	BAUMGARTE, VOLKER
12371040	8058899	20090146691	150	02/13/2009	LOGIC CELL ARRAY AND BUS SYSTEM	TAN,VIBOL	BAUMGARTE, VOLKER
12389116	Not Issued	20090210653	30	02/19/2009	METHOD AND DEVICE FOR TREATING AND PROCESSING DATA	VICARY,KEITH	BAUMGARTE, VOLKER

12570943	8914590	20100153654	150	09/30/2009	DATA PROCESSING METHOD AND DEVICE	THAI,TUAN	BAUMGARTE, VOLKER
12570984	8312301	20100023796	150	09/30/2009	METHODS AND DEVICES FOR TREATING AND PROCESSING DATA	ELAMIN,ABDELMONIEM	BAUMGARTE, VOLKER
12743356	Not Issued	20100281235	30	06/29/2010	RECONFIGURABLE FLOATING-POINT AND BIT-LEVEL DATA PROCESSING UNIT	PETRANEK,JACOB	BAUMGARTE, VOLKER
13289296	8471593	20120072699	150	11/04/2011	LOGIC CELL ARRAY AND BUS SYSTEM	TAN,VIBOL	BAUMGARTE, VOLKER
13324048	Not Issued	20120151113	161	12/13/2011	BUS SYSTEMS AND METHODS FOR CONTROLLING DATA FLOW IN A FIELD OF PROCESSING ELEMENTS	CLEARY,THOMAS	BAUMGARTE, VOLKER
13491894	8468329	20120311301	150	06/08/2012	PIPELINE CONFIGURATION PROTOCOL AND CONFIGURATION UNIT COMMUNICATION	ELAMIN,ABDELMONIEM	BAUMGARTE, VOLKER
13653639	Not Issued	20130042137	71	10/17/2012	METHODS AND DEVICES FOR TREATING AND PROCESSING DATA	ELAMIN,ABDELMONIEM	BAUMGARTE, VOLKER
13872779	Not Issued	20140325175	30	04/29/2013	PIPELINE CONFIGURATION PROTOCOL AND CONFIGURATION UNIT COMMUNICATION	ROSSITER,SEAN	BAUMGARTE, VOLKER
13903470	Not Issued	20140359254	93	05/28/2013	LOGICAL CELL ARRAY AND BUS SYSTEM	TAN,VIBOL	BAUMGARTE, VOLKER
14219945	Not Issued	20140208143	30	03/19/2014	Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply	ELAMIN,ABDELMONIEM	BAUMGARTE, VOLKER
14318211	Not Issued	20140310466	41	06/27/2014	Multi-processor bus and cache interconnection system	MISIURA,BRIAN	BAUMGARTE, VOLKER
14465157	Not Issued	20150033000	41	08/21/2014	Parallel Processing Array of Arithmetic Unit having a Barrier Instruction	MEHTA,JYOTI	BAUMGARTE, VOLKER
14500618	Not Issued	20150026431	41	09/29/2014	Method of Processing Data with an Array of Data Processors According to	NGUYEN,THAN	BAUMGARTE, VOLKER

					Application ID		
14572643	Not Issued	0	41	12/16/2014	Data Processing System Having Integrated Pipelined Array Data Processor	THAI,TUAN	BAUMGARTE, VOLKER
60238855	Not Issued		159	10/06/2000	Dataprocessor and applications	,	BAUMGARTE, VOLKER

Inventor Search Completed: No Records to Display.

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WEST Search History

DATE: Thursday, March 12, 2015

Hide?	<u>Set</u> <u>Name</u>	<u>Query</u>	<u>Hit</u> <u>Count</u>
<i>Prior Art</i>			
<i>DB=USOC,EPAB,JPAB,DWPI,TDBD,FPRS; PLUR=YES; OP=ADJ</i>			
☐	L76	(L75 or l74 or l73 or l72) and ((overheat\$4 or thermal\$6 or temperature) with (threshold or limit or level or predetermined or prespecified))	1
☐	L75	((clock or frequency) same (minimum\$4 or maximum\$4 or lower\$4 or reduc\$7 or increas\$4 or adjust\$4) same (queue\$4) same ((plural7 or multiple) adj process\$4 or multi\$1process\$4))	25
☐	L74	((clock or frequency) same (minimum\$4 or maximum\$4 or lower\$4 or reduc\$7 or increas\$4 or adjust\$4) same (utilize\$4 or usage) same ((plural7 or multiple) adj process\$4 or multi\$1process\$4))	52
☐	L73	((clock or frequency) same (minimum\$4 or maximum\$4 or lower\$4 or reduc\$7 or increas\$4 or adjust\$4) same load same ((plural7 or multiple) adj process\$4 or multi\$1process\$4))	44
☐	L72	((clock or frequency) with (minimum\$4 or maximum\$4 or lower\$4 or reduc\$7 or increas\$4 or adjust\$4) with load with ((plural7 or multiple) adj process\$4 or multi\$1process\$4))	17
<i>DB=PGPB,USPT; PLUR=YES; OP=ADJ</i>			
☐	L71	L70 and ((overheat\$4 or thermal\$6 or temperature) with (threshold or limit or level or predetermined or prespecified))	45
☐	L70	L60 and l5	114
☐	L69	l66 and ((overheat\$4 or thermal\$6 or temperature) with (threshold or predetermined or prespecified))	72
☐	L68	l66 and (overheat\$4 or thermal\$6 or temperature)	139
☐	L67	L60 and l11	16
☐	L66	L60 and l21	240
☐	L65	L60 and l22	55
☐	L64	L60 and l27	39
☐	L63	L62	83
☐	L62	L60 and l34	83
☐	L61	L60 and l36	44
☐	L60	L59 or l58 or l57	31162
☐	L59	(713/3\$2)! [CCLS]	20812
☐	L58	((G06F1/00).IPCR.)	9260
☐	L57	((G06F1/3203 G06F1/3237 Y02B60/1221 Y02B60/32).CPC.)	12189
☐	L56	20130042137 and operation	1

INTEL - 1004

☐	L55	20130042137 and pending	0
☐	L54	6311287.pn. and ((clock or frequency) with (max\$4 with minimum))	1
☐	L53	6311287.pn. and (busy or idle)	1
☐	L52	6311287.pn. and (process\$4 or microprocess\$4 or cpu)	1
☐	L51	6311287.pn. and (process\$4 or microprocess\$4 or cpu)	1
☐	L50	6311287.pn.	1
☐	L49	L48 not l47	15
☐	L48	l46 and ((clock or frequency) with (max\$4 with minimum))	17
☐	L47	l46 and (adjust\$4 with (clock or frequency) with (max\$4 with minimum))	2
<i>DB=USPT; PLUR=YES; OP=ADJ</i>			
☐	L46	("6311287")[URPN]	94
☐	L45	(5483102 5287292 5189314 5452401 5142684 4893271 5490059 5469561)! [PN]	8
☐	L44	("6311287")[PN]	1
<i>DB=PGPB,USPT; PLUR=YES; OP=ADJ</i>			
☐	L43	6311287.pn. and (adjust\$4 with (clock or frequency) with (max\$4 with minimum))	1
☐	L42	6311287.pn. and (performance)	1
☐	L41	6311287.pn. and (task or usage or use or utilize\$7)	1
☐	L40	6311287.pn. and operating conditions	1
☐	L39	6311287.pn. and operat\$7	1
☐	L38	6311287.pn. and load\$4	1
☐	L37	L36 same (process\$4 or microprocess\$4 or cpu) same (overheat\$4 or thermal\$6 or temperature)	27
☐	L36	adjust\$4 with (clock or frequency) with (max\$4 with minimum)	1664
☐	L35	L34 and ((clock or frequency) with max\$4 with minimum)	23
☐	L34	l33 or l29 or l27 or l26 or l25	224
<i>DB=USPT; PLUR=YES; OP=ADJ</i>			
☐	L33	(5319772 5561792 5301306 5488715 5451892 5455931 5428746 5416434 5142684 5506981 5450574 4677433 5537581 5535377 5563928 5491814 5546568 5469561 5392435 5287292 5381543 5163146 5442774 5586270 5319771 5490059 5408639 5325516 5420865 5487092 5291529 5579353)! [PN]	32
☐	L32	("5774704")[PN]	1
☐	L31	(5774704 5752011 5781768 5490059 6141762 5502838)! [PN]	6
☐	L30	("6397343")[PN]	1
☐	L29	6397343[urpn]	30
<i>DB=PGPB,USPT; PLUR=YES; OP=ADJ</i>			
☐	L28	l27 and l21	1
<i>DB=USPT; PLUR=YES; OP=ADJ</i>			

☐	L27	("5774704")[URPN]	121
☐	L26	5884233[urpn]	39
☐	L25	5610453[urpn]	6
<i>DB=PGPB,USPT; PLUR=YES; OP=ADJ</i>			
☐	L24	L23 not l18	5
☐	L23	L22.ti,ab,clm.	5
☐	L22	L21 same (temperature or overheat\$4)	214
☐	L21	load\$4 same (process\$4 or microprocess\$4 or cpu) same ((clock or frequency) near3 (max\$4 or minimum))	1743
☐	L20	L19 not (l18 or l17)	28
☐	L19	load\$4 with (temperature or overheat\$4) with ((clock or frequency) near3 minimum)	30
☐	L18	L16 same (process\$4 or microprocessor or cpu)	8
☐	L17	L16.ti,ab,clm.	2
☐	L16	load\$4 with (temperature or overheat\$4) with (clock or frequency) with max\$7 with minimum	62
☐	L15	load\$4 with (temperature or overheat\$4) with (clock or frequency) with amx\$7 with minimum	0
☐	L14	(5,774,704.pn.) and frequency	1
☐	L13	20130042137 and hysteresis	1
☐	L12	(7,620,784.pn.)	1
☐	L11	L5 same (queue\$4) same ((plur\$7 or multiple) adj process\$4 or multi\$1process\$4)	125
☐	L9	((5,774,704.pn.) and (max\$8 or min\$8))	1
☐	L8	((5,774,704.pn.) and (max\$7 or min\$7))	1
☐	L7	(5,774,704.pn.)	1
☐	L6	L5 same ((overheat\$4 or thermal\$6 or temperature) with (threshold or limit or level))	16
☐	L5	l1 or l2 or l3 or l4	562
☐	L4	((clock or frequency) same (minimum\$4 or maximum\$4 or lower\$4 or reduc\$7 or increas\$4 or adjust\$4) same (queue\$4) same ((plural7 or multiple) adj process\$4 or multi\$1process\$4))	125
☐	L3	((clock or frequency) same (minimum\$4 or maximum\$4 or lower\$4 or reduc\$7 or increas\$4 or adjust\$4) same (utilize\$4 or usage) same ((plural7 or multiple) adj process\$4 or multi\$1process\$4))	216
☐	L2	((clock or frequency) same (minimum\$4 or maximum\$4 or lower\$4 or reduc\$7 or increas\$4 or adjust\$4) same load same ((plural7 or multiple) adj process\$4 or multi\$1process\$4))	259
☐	L1	((clock or frequency) with (minimum\$4 or maximum\$4 or lower\$4 or reduc\$7 or increas\$4 or adjust\$4) with load with ((plural7 or multiple) adj process\$4 or multi\$1process\$4))	21

END OF SEARCH HISTORY

Search Notes 	Application/Control No. 13653639	Applicant(s)/Patent Under Reexamination VORBACH ET AL.
	Examiner M ELAMIN	Art Unit 2116

CPC- SEARCHED		
Symbol	Date	Examiner
G06F 1/3203	3/12/2015	AE
G06F 1/3237	3/12/2015	AE
Y02B 60/1221	3/12/2015	AE
Y02B 60/32	3/12/2015	AE

CPC COMBINATION SETS - SEARCHED		
Symbol	Date	Examiner

US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner

SEARCH NOTES		
Search Notes	Date	Examiner
WEST	12/16/2012	AE
WEST	3/12/2015	AE
INVENTOR'S NAME SEARCH	3/12/2015	AE
CLASS/SUBCLASS WITH TEXT	3/12/2015	AE

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner
G06F	1/3203, 1/3237	3/12/2015	AE
Y02B	60/1221, 60/32	3/12/2015	AE

	/ABDELMONIEM ELAMIN/ Primary Examiner, Art Unit 2116
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Issue Classification 	Application/Control No. 13653639	Applicant(s)/Patent Under Reexamination VORBACH ET AL.	
	Examiner M ELAMIN	Art Unit 2116	

CPC						
Symbol					Type	Version
G06F		1	/	3203	F	2013-01-01
G06F		1	/	3237	I	2013-01-01
Y02B		60	/	1221	A	2013-01-01
Y02B		60	/	32	A	2013-01-01
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CPC Combination Sets				
Symbol	Type	Set	Ranking	Version

NONE		Total Claims Allowed:	
		6	
(Assistant Examiner)	(Date)		
/M ELAMIN/ Primary Examiner.Art Unit 2116	03/12/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification 	Application/Control No. 13653639	Applicant(s)/Patent Under Reexamination VORBACH ET AL.
	Examiner M ELAMIN	Art Unit 2116

US ORIGINAL CLASSIFICATION						INTERNATIONAL CLASSIFICATION										
CLASS			SUBCLASS			CLAIMED					NON-CLAIMED					
						G	0	6	F	1 / 00 (2006.01.01)						
CROSS REFERENCE(S)																
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)															

NONE		Total Claims Allowed:	
		6	
(Assistant Examiner)	(Date)		
/M ELAMIN/ Primary Examiner.Art Unit 2116	03/12/2014	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	2

Issue Classification 	Application/Control No. 13653639	Applicant(s)/Patent Under Reexamination VORBACH ET AL.
	Examiner M ELAMIN	Art Unit 2116

☐ Claims renumbered in the same order as presented by applicant								☐ CPA		☐ T.D.		☐ R.1.47			
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
1	1	-	17	-	33	4	49								
-	2	-	18	-	34	5	50								
-	3	-	19	-	35	6	51								
-	4	-	20	-	36										
-	5	-	21	-	37										
-	6	-	22	-	38										
-	7	-	23	-	39										
-	8	-	24	-	40										
-	9	-	25	-	41										
-	10	-	26	-	42										
-	11	-	27	-	43										
-	12	-	28	-	44										
-	13	-	29	-	45										
-	14	-	30	-	46										
-	15	-	31	2	47										
-	16	-	32	3	48										

NONE		Total Claims Allowed:	
		6	
(Assistant Examiner)	(Date)	O.G. Print Claim(s)	O.G. Print Figure
/M ELAMIN/ Primary Examiner.Art Unit 2116	03/12/2014	1	2
(Primary Examiner)	(Date)		



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CONFIRMATION NO. 6103

SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
13/653,639	10/17/2012	713	2116	2885/162
RULE				
APPLICANTS PACT XPP TECHNOLOGIES AG, Munchen, GERMANY				
INVENTORS Martin VORBACH, Lingenfeld, GERMANY; Volker BAUMGARTE, Munchen, GERMANY;				
** CONTINUING DATA ***** This application is a CON of 12/570,984 09/30/2009 PAT 8312301 which is a CON of 12/257,075 10/23/2008 PAT 8099618 which is a DIV of 10/469,909 09/21/2004 PAT 7444531 which is a 371 of PCT/EP02/02402 03/05/2002				
** FOREIGN APPLICATIONS ***** GERMANY 101 10 530.4 03/05/2001 GERMANY 101 11 014 03/07/2001 GERMANY 101 29 237 06/20/2001 EUROPEAN PATENT OFFICE (EPO) 011 15 021 06/20/2001 GERMANY 101 35 210 07/24/2001 GERMANY 101 35 211 07/24/2001 GERMANY 101 39 170 08/16/2001 GERMANY 101 42 231 08/29/2001 GERMANY 101 42 894 09/03/2001 GERMANY 101 42 903 09/03/2001 GERMANY 101 42 904 09/13/2001 GERMANY 101 44 732 09/11/2001 GERMANY 101 44 733 11/09/2001 GERMANY 101 45 792 09/17/2001 GERMANY 101 45 795 09/17/2001 GERMANY 101 46 132 09/19/2001 GERMANY 101 54 260 11/05/2001 GERMANY 101 54 259 11/05/2001 EUROPEAN PATENT OFFICE (EPO) 011 29 923 12/14/2001 EUROPEAN PATENT OFFICE (EPO) 020 01 331 01/18/2002 GERMANY 102 02 044 01/19/2002 GERMANY 102 02 175 01/20/2002 GERMANY 102 06 653 02/15/2002 GERMANY 102 06 857 02/18/2002 GERMANY 102 06 856 02/18/2002 GERMANY 102 07 226 02/21/2002 GERMANY 102 07 224 02/21/2002 GERMANY 102 07 225 02/21/2002 GERMANY 102 08 435 02/27/2002 GERMANY 102 08 434 02/27/2002 EUROPEAN PATENT OFFICE (EPO) PCT/EP01/06703 06/13/2001 EUROPEAN PATENT OFFICE (EPO) PCT/EP01/08534 07/24/2001				



PALM INTRANET

Day : Thursday
Date: 3/12/2015
Time: 14:32:31

Inventor Name Search Result

Your Search was:

Last Name = VORBACH

First Name = MARTIN

Application#	Patent#	PG Pub#	Status	Date Filed	Title	Examiner Name	Inventor Name
08946810	6425068		150	10/08/1997	UNIT FOR PROCESSING NUMERICAL AND LOGICAL OPERATIONS FOR USE IN CENTRAL PROCESSING UNITS (CPUS), MULTIPROCESSOR SYSTEMS, DATA - FLOW PROCESSORS (DSPS), SYSTOLIC PROCESSORS AND FIELD PROGRAMMABLE GATE ARRAYS (FPGAS)	ELLIS,RICHARD	VORBACH, MARTIN
08946811	Not Issued		169	10/08/1997	INTERNAL BUS SYSTEM FOR DFPS AS WELL AS MODULES HAVING TWO OR MULTI DIMENSIONAL PROGRAMMABLE CELL STRUCTURES FOR MANAGING LARGE QUNATITIES OF DATA ENTAILING A HIGH NETWORKING COMPLEXITY		VORBACH, MARTIN
08946812	6081903		150	10/08/1997	METHOD OF THE SELF-SYNCHRONIZATION OF CONFIGURABLE ELEMENTS OF A PROGRAMMABLE UNIT	BUTLER,DENNIS	VORBACH, MARTIN
08946998	6021490		150	10/08/1997	RUN-TIME RECONFIGURATION METHOD FOR PROGRAMMABLE UNITS	HECKLER,THOMAS	VORBACH, MARTIN
08946999	6038650		150	10/08/1997	METHOD FOR THE AUTOMATIC ADDRESS GENERATION OF MODULES WITHIN	NGUYEN,THAN	VORBACH, MARTIN

INTEL - 1004

					CLUSTERS COMPRISED OF A PLURALITY OF THESE MODULES		
<u>08947002</u>	<u>6088795</u>		150	10/08/1997	PROCESS FOR AUTOMATIC DYNAMIC RELOADING OF DATA-FLOW PROCESSORS (DFPS) AND UNITS WITH TWO-OR THREE- DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES (FPGAS, DPGAS AND THE LIKE)	MAI,RIJUE	VORBACH, MARTIN
<u>08947254</u>	<u>6119181</u>		150	10/08/1997	I/O AND MEMORY BUS SYSTEM FOR DFPS AND UNITS WITH TWO- OR MULTI- DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES	RAY,GOPAL	VORBACH, MARTIN
<u>09000724</u>	Not Issued		168	12/30/1997	PROCESS FOR AUTOMATIC DYNAMIC RELOADING OF DATA FLOW PROCESSORS (DFPS) AND UNITS WITH TWO- OR THREE- DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES (FPGAS, DPGAS, AND THE LIKE)	MAI,RIJUE	VORBACH, MARTIN
<u>09145139</u>	<u>6405299</u>		150	08/28/1998	INTERNAL BUS SYSTEM FOR DFPS AND UNITS WITH TWO-OR MULTI- DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES, FOR MANAGING LARGE VOLUMES OF DATA WITH A HIGH INTERCONNECTION COMPLEXITY	VO,TIM	VORBACH, MARTIN
<u>09290342</u>	<u>6859869</u>		150	04/12/1999	DATA PROCESSING SYSTEM	WHITMORE,STACY	VORBACH, MARTIN
<u>09329132</u>	<u>6728871</u>		150	06/09/1999	RUNTIME CONFIGURABLE ARITHMETIC AND LOGIC CELL	ELLIS,RICHARD	VORBACH, MARTIN

09335974	6338106		150	06/18/1999	I/O AND MEMORY BUS SYSTEM FOR DFPS AND UNITS WITH TWO OR MULTI-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES	RAY,GOPAL	VORBACH, MARTIN
09369653	6542928		150	08/06/1999	METHOD OF SELF-SYNCHRONIZATION OF CONFIGURABLE ELEMENTS OF A PROGRAMMABLE MODULE	HECKLER,THOMAS	VORBACH, MARTIN
09494567	7174443		150	01/31/2000	RUN-TIME RECONFIGURATION METHOD FOR PROGRAMMABLE UNITS	DOLLINGER,TONIA	VORBACH, MARTIN
09537932	6526520		150	03/29/2000	METHOD OF SELF-SYNCHRONIZATION OF CONFIGURABLE ELEMENTS OF A PROGRAMMABLE UNIT	BUTLER,DENNIS	VORBACH, MARTIN
09598926	6697979		150	06/21/2000	METHOD OF REPAIRING INTEGRATED CIRCUITS	LAMARRE,GUY	VORBACH, MARTIN
09613217	6477643		150	07/10/2000	PROCESS FOR AUTOMATIC DYNAMIC RELOADING OF DATA FLOW PROCESSORS (DFPS) AND UNITS WITH TWO-OR THREE-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES (FPGAS,DPGAS, AND THE LIKE)	MAI,RIJUE	VORBACH, MARTIN
09623052	6480937		150	01/09/2001	METHOD FOR HIERARCHICAL CACHING OF CONFIGURATION DATA HAVING DATAFLOW PROCESSORS AND MODULES HAVING TWO-OR MULTIDIMENSIONAL PROGRAMMABLE CELL STRUCTURE (FPGAS, DPGS, ETC.)--	ELMORE,STEPHEN	VORBACH, MARTIN
09623113	6571381		150	01/09/2001	METHOD FOR DEADLOCK-FREE	KIK,PHALLAKA	VORBACH, MARTIN

					CONFIGURATION OF DATAFLOW PROCESSORS AND MODULES WITH A TWO-OR MULTIDIMENSIONAL PROGRAMMABLE CELL STRUCTURE (FPGAS, DPGAS, ETC.)		
09915213	6513077	20020099888	150	07/25/2001	I/O AND MEMORY BUS SYSTEM FOR DFPS AND UNITS WITH TWO- OR MULTI-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES	RAY,GOPAL	VORBACH, MARTIN
09967497	7266725	20030046607	150	09/28/2001	METHOD FOR DEBUGGING RECONFIGURABLE ARCHITECTURES	LE,DIEU MINH	VORBACH, MARTIN
09967498	Not Issued	20040015899	161	09/28/2001	Method for processing data	RAMPURIA,SATISH	VORBACH, MARTIN
09967847	7210129	20030056202	150	09/28/2001	METHOD FOR TRANSLATING PROGRAMS FOR RECONFIGURABLE ARCHITECTURES	INGBERG,TODD	VORBACH, MARTIN
10009649	8230411		150	05/29/2002	METHOD FOR INTERLEAVING A PROGRAM OVER A PLURALITY OF CELLS	DAO,THUY	VORBACH, MARTIN
10116986	7010667	20030135686	150	04/05/2002	INTERNAL BUS SYSTEM FOR DFPS AND UNITS WITH TWO- OR MULTI-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES, FOR MANAGING LARGE VOLUMES OF DATA WITH A HIGH INTERCONNECTION COMPLEXITY	VO,TIM	VORBACH, MARTIN
10156397	7237087	20030056085	150	05/28/2002	RECONFIGURABLE MULTIDIMENSIONAL ARRAY PROCESSOR ALLOWING RUNTIME RECONFIGURATION OF SELECTED INDIVIDUAL ARRAY CELLS	ELLIS,RICHARD	VORBACH, MARTIN
10191926	6687788	20030074518	150	07/09/2002	METHOD OF HIERARCHICAL CACHING OF	ELMORE,STEPHEN	VORBACH, MARTIN

					CONFIGURATION DATA HAVING DATAFLOW PROCESSORS AND MODULES HAVING TWO-OR MULTIDIMENSIONAL PROGRAMMABLE CELL STRUCTURE (FPGAS, DPGAS, ETC.)		
10265846	7028107	20030093662	150	10/07/2002	PROCESS FOR AUTOMATIC DYNAMIC RELOADING OF DATA FLOW PROCESSORS (DFPS) AND UNITS WITH TWO- OR THREE-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES (FPGAS, DPGAS, AND THE LIKE)	KNAPP,JUSTIN	VORBACH, MARTIN
10297959	7003660	20040025005	150	06/19/2003	PIPELINE CONFIGURATION UNIT PROTOCOLS AND COMMUNICATION	ELAMIN,ABDELMONIEM	VORBACH, MARTIN
10304252	6721830	20030097513	150	11/26/2002	L/O AND MEMORY BUS SYSTEM FOR DFPS AND UNITS WITH TWO- OR MULTI-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES	RAY,GOPAL	VORBACH, MARTIN
10373595	6968452	20040052130	150	02/24/2003	METHOD OF SELF-SYNCHRONIZATION OF CONFIGURABLE ELEMENTS OF A PROGRAMMABLE UNIT	BUTLER,DENNIS	VORBACH, MARTIN
10379403	7036036	20040083399	150	03/04/2003	METHOD OF SELF-SYNCHRONIZATION OF CONFIGURABLE ELEMENTS OF A PROGRAMMABLE MODULE	YANCHUS III,PAUL	VORBACH, MARTIN
10398546	7595659	20040128474	150	01/20/2004	LOGIC CELL ARRAY AND BUS SYSTEM	TAN,VIBOL	VORBACH, MARTIN
10469909	7444531	20050066213	150	09/21/2004	METHODS AND DEVICES FOR TREATING AND PROCESSING DATA	ELAMIN,ABDELMONIEM	VORBACH, MARTIN
10469910	Not Issued	20070299993	161	02/17/2005	Method and Device for Treating and Processing Data	MAMO,ELIAS	VORBACH, MARTIN

10471061	7581076	20050086462	150	10/29/2004	METHODS AND DEVICES FOR TREATING AND/OR PROCESSING DATA	NGUYEN,THAN	VORBACH, MARTIN
10480003	7657877	20040243984	150	06/18/2004	METHOD FOR PROCESSING DATA	BROPHY,MATTHEW	VORBACH, MARTIN
10486771	7996827	20050086649	150	09/20/2004	METHOD FOR THE TRANSLATION OF PROGRAMS FOR RECONFIGURABLE ARCHITECTURES	DAO,THUY	VORBACH, MARTIN
10487681	7577822	20040249880	150	08/05/2004	PARALLEL TASK OPERATION IN PROCESSOR AND RECONFIGURABLE COPROCESSOR CONFIGURED BASED ON INFORMATION IN LINK LIST INCLUDING TERMINATION INFORMATION FOR SYNCHRONIZATION	KIM,KENNETH	VORBACH, MARTIN
10487687	7480825	20050022062	150	08/25/2004	METHOD FOR DEBUGGING RECONFIGURABLE ARCHITECTURES	CONTINO,PAUL	VORBACH, MARTIN
10490079	7434121	20050053056	150	11/02/2004	ROUTER	LIN,SUN	VORBACH, MARTIN
10490081	8429385	20060245225	150	11/29/2004	DEVICE INCLUDING A FIELD HAVING FUNCTION CELLS AND INFORMATION PROVIDING CELLS CONTROLLED BY THE FUNCTION CELLS	FENNEMA,ROBERT	VORBACH, MARTIN
10501845	8281108	20060090062	150	08/26/2005	RECONFIGURABLE GENERAL PURPOSE PROCESSOR HAVING TIME RESTRICTED CONFIGURATIONS	VICARY,KEITH	VORBACH, MARTIN
10501903	Not Issued	20050132344	161	03/01/2005	Method of compilation	LOUIE,JUE	VORBACH, MARTIN
10504684	8127061	20070150637	150	07/14/2006	BUS SYSTEMS AND RECONFIGURATION METHODS	CLEARY,THOMAS	VORBACH, MARTIN
10508559	Not Issued	20060075211	161	06/20/2005	Method and device for data processing	GIROUX,GEORGE	VORBACH, MARTIN
10523763	7657861	20060248317	150	11/22/2005	METHOD AND DEVICE FOR PROCESSING DATA	DINH,PAUL	VORBACH, MARTIN
10523764	8156284	20070050603	150	08/02/2005	DATA PROCESSING METHOD AND DEVICE	THAI,TUAN	VORBACH, MARTIN
10526595	7394284	20060192586	150	01/09/2006	RECONFIGURABLE SEQUENCER STRUCTURE	LE,DON	VORBACH, MARTIN

10551891	Not Issued	20070011433	30	08/28/2006	Method and device for data processing	VICARY,KEITH	VORBACH, MARTIN
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13653639
	Filing Date		2012-10-17
	First Named Inventor	Martin Vorbach	
	Art Unit	2116	
	Examiner Name	ELAMIN, ABDELMONIEM I	
	Attorney Docket Number	PACT-025-PCT-US-D1-2C1	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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First Named Inventor	Martin Vorbach	
Art Unit	2116	
Examiner Name	ELAMIN, ABDELMONIEM I	
Attorney Docket Number	PACT-025-PCT-US-D1-2C1	

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Filing Date:	17-Oct-2012			
Title of Invention:	METHODS AND DEVICES FOR TREATING AND PROCESSING DATA			
First Named Inventor/Applicant Name:	Martin VORBACH			
Filer:	Edward Peter Heller/Emi Rhodes			
Attorney Docket Number:	PACT-025-PCT-US-D1-2C1			
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Claims:				
Miscellaneous-Filing:				
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International Application Number:	
Confirmation Number:	6103
Title of Invention:	METHODS AND DEVICES FOR TREATING AND PROCESSING DATA
First Named Inventor/Applicant Name:	Martin VORBACH
Customer Number:	73481
Filer:	Edward Peter Heller/Emi Rhodes
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Filing Date:	17-OCT-2012
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20	Non Patent Literature	1-22- ClockLock_ClockBoost_Circuitr y_for_High- Density_PLDS_ALTR00266383. pdf	3017208 b05d6d219aa8da3d954bc620c40d91df979 5d8d4	no	31
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21	Non Patent Literature	1-23- Configuring_FLEX_10K_Device s_ALTR00266494.pdf	1040795 e7cbf419138203520893e8c91cdce40a80a5 e94a	no	24
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22	Non Patent Literature	1-24-Datavave_A_Single- Chip_Multiprocessor_for_Vide o_Applications_ALTR00276651. pdf	1252057 6ee92bdecf1dd5b7aabfe08d0913605bffd f552	no	11
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23	Non Patent Literature	1-25- Embedded_Configurable_Mem ory_and_Logic_Boost_FPGA_F unctionality_ALTR00268355. pdf	677496 fa5dea40631308382584eadc0a360304302f b470	no	3
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25	Non Patent Literature	1-27- IBM_Extends_DSP_Performanc e_with_Mfast_ALTR00268641. pdf	512092 212a200d0cd537e5fd968d253b4a0f14138d6b7d	no	4
Warnings:					
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26	Non Patent Literature	1-28- IEEE_Standard_Test_Access_Po rt_and_Boundary- Scan_Architecture_ALTR00269 515.pdf	1516271 64a20f53f1e1d456ce368f1898c690e026d87f63	no	38
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27	Non Patent Literature	1-29- Implementing_State_Machines _in_LCA_Devices_ALTR002641 68.pdf	276021 1186ebb95121d643aeb26a0d338b1981bd7f9ecd	no	4
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28	Non Patent Literature	1-30- Improving_XC4000_Design_Pe rformance_ALTR00276409.pdf	1310320 7bb4cac23daf3fc605506d7661b05545974cfab0	no	15
Warnings:					
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29	Non Patent Literature	1-31- Intel_82375EB-82375SB_PCI- EISA_Bridge_PCEB_Advance_In formation_ALTR00276470.pdf	6205040 6b7899cdd2543743b7dd51c6241ef0e5496c1d6	no	132
Warnings:					
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30	Non Patent Literature	1-32- Interfacing_XC6200_to_Microp rocessors_MC68020_Example_ ALTR00274453.pdf	427434 c067270da5cf6b03e006feb983c928dde1ec6442	no	8
Warnings:					
Information:					
31	Non Patent Literature	1-33- Interfacing_XC6200_To_Micro processors_TMS320C50_Exam ple_ALTR00278492.pdf	509685 23912472e436445fe37e841dd6addda62231a410	no	9
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32	Non Patent Literature	1-34- Introducing_the_XC6200_FPG A_Architecture_XCELL_1995_A LTR00269592.pdf	6602655 1a9d8cdc152834e538741a7792d9281f3b1e85d5	no	40

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33	Non Patent Literature	1-35- JTAG_Boundary_Scan_Testing _in_Altera_Devices_ALTR00266 442.pdf	1270243 188f25e38ab05bd8d4f6c676a83a1808762f cddd	no	28
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35	Non Patent Literature	1-37- Megabit_FIFO_in_Two_Chips_ One_LCA_Device_and_One_D RAM_ALTR00276308.pdf	165056 648ea9c028d6edbf0f9a727cadafa51af7a3a 2613	no	3
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36	Non Patent Literature	1-38- Microcomputer_Buses_and_Li nks_ALTR00276432.pdf	675213 308dd5d4d46c149931638db57b3e6b31d8 b562b0	no	18
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37	Non Patent Literature	1-39- Mixed_Fixed_and_Reconfigura ble_Logic_for_Array_Processin g_ALTR00276373.pdf	691191 b46aded483206652750e6004468222a68e b5c99	no	8
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38	Non Patent Literature	1-40- PCI_Bus_Applications_in_Alter a_Devices_ALTR00271019.pdf	1300986 ec3755f09000cdf8a111366ca220416d0a59 2f53	no	32
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39	Non Patent Literature	1-41- PCI_Bus_Target_Megafunction _ALTR00271061.pdf	124150 9864b9b4151ba6c25e8259fe0cfc8795f24 9ca2	no	2
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40	Non Patent Literature	1-42- PCI_Compliance_of_Altera_De vices_ALTR00271009.pdf	469741 e0e536a2283461c71cd54db03fa916705e4 cce5e	no	10
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42	Non Patent Literature	1-44- Rambus_Architectural_Overview w_ALTR00276001.pdf	9259117 fe08b1c3faa36fd5dd00b8dab404750c7606471	no	27
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43	Non Patent Literature	1-46a- Rambus_Product_Catalog_ALT R00276077.pdf	25080691 c7379c62506241cf723d7553309c9cf649284e45	no	97
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44	Non Patent Literature	1-48- System_Design_with_New_XC 4000EX_IO_Features_ALTR002 76424.pdf	612917 919b8fe581b56f709d3f1eb10d274b6a23945230	no	8
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45	Non Patent Literature	1-49-Technical_Data_- _XC5200_Logic_Cell_Array_Fa mily_Preliminary_v-1-0_ALTR0 0278897.pdf	2357491 448e199ad9a2a1338f37086726077e5cc5f802af	no	48
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46	Non Patent Literature	1-50a- The_Programmable_Logic_Dat a_Book_1993_ALTR00271877. pdf	25726613 7f6f674233f7e6844ccde8c14a2aa8dc900ee39e	no	164
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47	Non Patent Literature	1-50b- The_Programmable_Logic_Dat a_Book_1993_ALTR00271877. pdf	20716131 b83d34c5222ec9016f6ddc3b494b294b594f2893	no	140
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48	Non Patent Literature	1-50c- The_Programmable_Logic_Dat a_Book_1993_ALTR00271877. pdf	18914362 7873bed97418ada1fdbfcd4835ef067c6d937bc2	no	141
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Warnings:					
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50	Foreign Reference	1-FRN-DE4416881_ALTR00276450.pdf	1388778 1b57823e91afaa1f4954e3abd660bbb883c4ebac	no	20
Warnings:					
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51	Foreign Reference	1-FRN-WO-1995-028671_ALTR00278501.pdf	3428175 bbabc2b2f37f337bf7ef6ba2a7ce38306e7f5925	no	60
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52	Transmittal Letter	PACT-025-PCT-US-D1-2C1_1150401_IDS_Letter.pdf	106302 129b68f7082b134bb546a3d2b22156e23afe725	no	4
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53	Information Disclosure Statement (IDS) Form (SB08)	PACT-025-PCT-US-D1-2C1_150401_PTOSB08a_1.pdf	617129 972f6235c29ec62bebedd8f6af9fa0654405c5b	no	17
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54	Fee Worksheet (SB06)	fee-info.pdf	30706 f9f590996379072bea00e15d5ba56eae6e8c2409	no	2
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①⑨ BUNDESREPUBLIK
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⑫ **Offenlegungsschrift**
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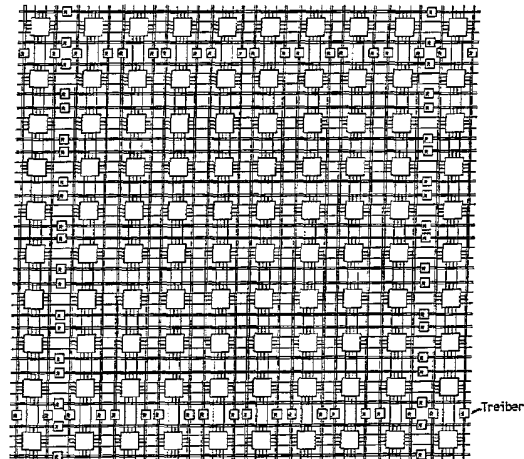
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⑦② Erfinder:
gleich Anmelder

Prüfungsantrag gem. § 44 PatG ist gestellt

⑤④ Datenverarbeitungseinrichtung

⑤⑦ In Verbindung mit einer Datenverarbeitungseinrichtung, wobei ein (im folgenden Datenflußprozessor - DFP - genannter) integrierter Schaltungskreis (Chip) mit einer Vielzahl insbesondere orthogonal zueinander angeordneter homogen strukturierter Zellen mit je einer Mehrzahl jeweils logisch gleicher und strukturell identisch angeordneter Bausteine vorgesehen ist, dessen Zellen zeilen- und spaltenweise, gegebenenfalls gruppenweise zusammengefaßt, mit Ein-/Ausgangsanschlüssen des integrierten Schaltkreises verbunden sind, ist erfindungsgemäß den Zellen eine Ladelogik zugeordnet, über die sie je für sich und gegebenenfalls gruppenweise zusammengefaßt so programmierbar (konfigurierbar) sind, daß beliebige logische Funktionen und/oder Vernetzungen untereinander verifizierbar sind, und zwar derart, daß eine Manipulation der DFP-Konfiguration während des Betriebes (oder zur Laufzeit), d. h. die Modifikation funktioneller Teile (MACROS) des DFPs erfolgen kann, ohne daß andere funktionelle Teile angehalten werden müssen oder in ihrer Funktion beeinträchtigt werden.



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Die folgenden Angaben sind den vom Anmelder eingereichten Unterlagen entnommen

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Die vorliegende Erfindung bezieht sich auf eine Datenverarbeitungseinrichtung, d. h. eine Hardwareeinheit zur logischen Manipulation (Verknüpfung) von in binärer Form vorliegenden Daten (Informationen).

Derartige Datenverarbeitungseinrichtungen sind mittlerweile lange bekannt und sie haben bereits breite Anwendung und Anerkennung gefunden. Die prinzipielle Aufbau- und Arbeitsstruktur der bekannten Datenverarbeitungseinrichtungen ist in etwa so zu definieren, daß eine arithmetisch-logische Verknüpfungseinheit vorgesehen ist, in der die zu verknüpfenden Daten einer programmtechnischen Anweisung (Software) zufolge verarbeitet werden. Die Daten werden dabei über ein Steuerwerk in mehr oder weniger komplexen Adressierungsvorgängen entsprechend abgerufen und zunächst in Arbeitsregistern bereitgestellt; nach der logischen Verknüpfung werden dann die neuen Daten in einer vorgegebenen Speicherstelle wieder abgelegt. Die arithmetisch-logische Verknüpfungseinheit besteht dabei aus logischen Verknüpfungsbausteinen (Gatter, Glieder), die jeweils so miteinander gekoppelt sind, daß die zu manipulierenden Daten der zugrunde liegenden Software entsprechend den vier Grundrechenarten gemäß logisch verarbeitet werden.

Es ist leicht nachzuvollziehen, daß auf der Basis der bekannten Strukturen relativ viel Rechenzeit dafür erforderlich ist, die zu manipulierenden Daten auszulesen, und die Arbeitsregister zu überführen, den spezifischen Logikbausteinen in der arithmetisch-logischen Verknüpfungseinheit zuzuleiten und schließlich wieder abzuschreiben. Es ist ferner einsichtig, daß die Hardware-Struktur der arithmetisch-logischen Verknüpfungseinheit insoweit nicht als optimal betrachtet werden kann, als schließlich die hardwaremäßig vorhandenen integrierten logischen Bausteine stets nur in ein und derselben Art und Weise im Gesamtsystem aktiv benutzt werden. Ebenso wird durch strikte Hardwarevorgabe ein Aneinanderreihen von Funktionen in sogenannten Pipelines sehr erschwert oder eingeschränkt, was zwangsläufig ein häufiges Registerumladen zwischen Arbeitsregistern und Rechenwerk bedeutet. Derartige Bausteine sind des weiteren nur schlecht kaskadierbar und erfordern dann sehr viel Programmierarbeit.

Ein zusätzlicher Vorteil der vorliegenden Erfindung liegt darin, daß eine über einen weiten Raum skalierbare Parallelität zur Verfügung steht. Hierbei wird eine Basis zum schnellen und flexiblen Aufbau von neuronalen Strukturen geschaffen, wie die bis dato lediglich mit erheblichem Aufwand simuliert werden können.

Die der vorliegenden Erfindung zugrunde liegende Aufgabe besteht darin, eine im folgenden Datenflußprozessor (DFP) genannte Datenverarbeitungseinrichtung anzugeben, bei der eine höhere beziehungsweise bessere Flexibilität der Gesamtstruktur und des Datenflusses sowie der Pipelining- und Kaskadierungsmöglichkeiten zu einer Erhöhung der Rechnerbeziehungsweise Verknüpfungsleistung führt.

Außer dem Einsatz als reiner Datenflußprozessor, soll der DFP folgende weitere Aufgaben erfüllen können:

- Einsatz als universeller Baustein zum Aufbau von herkömmlichen Rechnern, wobei der Aufbau einfacher und billiger werden soll.
- Einsatz in neuronalen Netzen.

Diese Aufgabe wird dadurch gelöst, daß ein integrierter Schaltkreis (Chip) mit einer Vielzahl insbesondere orthogonal zueinander angeordneter Zellen mit je einer Mehrzahl jeweils logisch gleicher und strukturell identisch angeordneter Zellen vorgesehen ist deren Anordnung, sowie die interne Busstruktur, zur Erleichterung der Programmierung äußerst homogen ist. Dennoch ist es denkbar innerhalb eines Datenflußprozessors Zellen mit verschiedenen Zelllogiken und Zellstrukturen unterzubringen, um so die Leistungsfähigkeit zu erhöhen, indem zum Beispiel für Speicheransteuerungen andere Zellen als für arithmetische Operationen existieren. Insbesondere kann für neuronale Netze eine gewisse Spezialisierung von Vorteil sein. Den Zellen ist eine Ladelogik zugeordnet, über die die Zellen je für sich und gegebenenfalls gruppenweise in sogenannte MACROs zusammengefaßt so programmierbar sind, daß einerseits beliebige logische Funktionen, andererseits aber auch die Verknüpfung der Zellen untereinander in weiten Bereichen verifizierbar sind. Dies wird erreicht indem jeder einzelnen Zelle ein gewisser Speicherplatz zur Verfügung steht, in dem die Konfigurationsdaten abgelegt sind. Anhand dieser Daten werden Multiplexer oder Transistoren in der Zelle beschaltet um die jeweilige Zellfunktion zu gewährleisten (siehe Fig. 12).

Mit anderen als im Patentanspruch 1 gebrauchten Worten besteht der Kern der vorliegenden Erfindung darin, einen Datenflußprozessor vorzuschlagen, der zellular aufgebaut ist und dessen Zellen über eine externe Ladelogik im arithmetisch-logischen Sinne quasi beliebig neu konfiguriert werden können. Dabei ist es von äußerster Notwendigkeit, daß die betreffenden Zeilen einzeln und ohne Beeinflussung der übrigen Zeilen oder gar einer Stilllegung des gesamten Bausteins umkonfiguriert werden können. Der Datenflußprozessor gemäß der vorliegenden Erfindung kann so während eines ersten Arbeitszyklus als Addierer und während eines späteren Arbeitszyklus als Multiplizierer "programmiert" werden, wobei die Anzahl der für die Addition beziehungsweise die Multiplikation erforderlichen Zellen durchaus unterschiedlich sein können. Dabei bleibt die Plazierung der bereits geladenen MACROs erhalten; der Ladelogik beziehungsweise dem Compiler obliegt es, das neu zu ladende MACRO innerhalb der freien Zellen zu partitionieren (d. h. das zu ladende MACRO so zu zerlegen, daß es sich optimal einfügen läßt). Die Ablaufsteuerung des Programms wird dabei von der Ladelogik übernommen, indem sie gemäß dem momentan ausgeführten Programmabschnitt die entsprechenden MACROs in den Baustein lädt, wobei der Ladevorgang von der später beschriebenen Synchronisationslogik mitgesteuert wird, indem sie den Zeitpunkt des Umladens festlegt. Daher entspricht der DFP nicht der bekannten von-Neumann-Architektur, da die Daten- und Programmspeicher getrennt sind. Dies bedeutet jedoch gleichzeitig eine höhere Sicherheit, da fehlerhafte Programme keinen CODE, sondern lediglich DATEN zerstören können.

Um den Datenflußprozessor eine arbeitsfähige Struktur zu geben, werden einige Zellen, und zwar unter anderem die Eingabe-/Ausgabefunktionen (I/O) und Speichermanagementfunktionen vor dem Laden der Programme geladen und bleiben für gewöhnlich während der gesamten Laufzeit konstant. Dies ist erforderlich um den Datenflußprozessor an seine Hardwareumgebung anzupassen. Die übrigen Zellen werden zu sogenannten MACROs zusammengefaßt und können während der Laufzeit nahezu beliebig und ohne Beeinflussung der

Nachbarzellen umkonfiguriert werden. Dazu sind die Zellen einzeln und direkt adressierbar.

Um die Umstrukturierung (das Umladen) der Zellen oder MACROs mit der Ladelogik zu synchronisieren, kann — wo notwendig, da nur Umgeladen werden darf, wenn die MACROs mit ihrer alten Tätigkeit fertig sind — eine Synchronisationsschaltung als MACRO auf dem Datenflußprozessor untergebracht werden, die die entsprechenden Signale an die Ladelogik absendet. Hierzu kann eventuell eine Modifikation der gewöhnlichen MACROs von Nöten sein, da diese dann der Synchronisations-Schaltung Zustandsinformationen zur Verfügung stellen müssen.

Diese Zustandsinformationen signalisieren der Synchronisationslogik für gewöhnlich, daß einzelne MACROs ihre Aufgabe erledigt haben, was aus programmertechnischer Sicht zum Beispiel die Terminierung einer Prozedur oder das Erreichen der Terminierungsbedingung einer Schleife bedeuten kann. D.h. das Programm wird an einer anderen Stelle fortgesetzt und die Zustandsinformation absendenden MACROs können umgeladen werden. Zudem kann es von Interesse sein, daß die MACROs in einer bestimmten Reihenfolge umgeladen werden. Hierzu kann eine Wertung der einzelnen Synchronisations-Signale durch einen Prioritätsdekodier erfolgen. Eine derartige — einfache — Logik ist in Fig. 13 gezeichnet. Die Logik besitzt sieben Eingangssignale durch die die sieben MACROs ihre Zustandsinformation abgeben. In diesem Fall soll 0 für "in Arbeit" und 1 für "fertig" stehen. Die Logik besitzt drei Ausgangssignale, die an die Ladelogik geführt werden, wobei der Zustand 000 als Ruhezustand gilt. Liegt ein Signal an einem der sieben Eingänge an, so findet eine Dezimal-Binär-Umsetzung statt, so wird zum Beispiel Sync6 als 110 dargestellt, was der Ladelogik anzeigt, daß das MACRO, welches Sync6 bedient, seine Aufgabe beendet hat. Liegen gleichzeitig mehrere Synchronisations-Signale am Eingang an, so gibt die Synchronisationsschaltung das Signal mit der höchsten Priorität an die Ladelogik weiter; liegen zum Beispiel Sync0, Sync4 und Sync6 an, so reicht die Synchronisations-Schaltung zunächst Sync6 an die Ladelogik weiter. Nachdem die entsprechenden MACROs umgeladen sind und somit Sync6 nicht mehr anliegt wird Sync4 weitergeleitet usw. Zur Verdeutlichung dieses Prinzips kann der Standard-TTL-Baustein 74148 in Betracht gezogen werden.

Über die Ladelogik kann der Datenflußprozessor jeweils optimal und gegebenenfalls dynamisch auf eine zu lösende Aufgabe eingestellt werden. Damit ist zum Beispiel der große Vorteil verbunden, daß neue Normen oder dergleichen einzig und allein durch eine Umprogrammierung des Datenflußprozessors umgesetzt werden können und nicht — wie bisher — einen Austausch mit entsprechendem Anfall von Elektronikschrott bedingen.

Die Datenflußprozessoren sind untereinander kaskadierbar, was zu einer beinahe beliebigen Erhöhung des Parallelisierungsgrades, der Rechenleistung, sowie der Netzgröße in neuronalen Netzen führt. Besonders wichtig ist hier eine klare homogene Verbindung der Zellen mit den Ein-/Ausgangs-Pins (IO-Pin) der Datenflußprozessoren, um möglichst keine Einschränkungen auf die Programme zu haben.

In Fig. 14 ist zum Beispiel die Kaskadierung von vier DFPs gezeigt. Sie erscheinen der Umgebung wie ein großer homogener Baustein (Fig. 15). Prinzipiell sind damit zwei Kaskadierungsmethoden denkbar:

a) Nur die lokalen Verbindungen zwischen den Zellen werden herausgeführt, was im vorliegenden Beispiel zwei IO-Pins pro Kantenzelle und vier IO-Pins pro Eckzelle bedeutet. Allerdings hat der Compiler/Programmierer zu beachten, daß die globalen Verbindungen nicht herausgeführt werden, wodurch die Kaskadierung nicht vollständig homogen ist. (Globale Verbindungen zwischen mehreren Zellen, für gewöhnlich zwischen einer kompletten Zellenreihe oder -spalte — siehe Fig. 6 —; lokale Verbindungen existieren nur zwischen zwei Zellen). Fig. 16a zeigt den Aufbau innerhalb eines DFPs, Fig. 17a zeigt die daraus resultierende Kaskadierung von mehreren DFPs (drei gezeichnet).

b) Die lokalen und globalen Verbindungen werden herausgeführt, was die Anzahl der benötigten Treiber/IO-Pins und Leitungen drastisch erhöht, in unserem Beispiel auf sechs IO-Pins pro Kantenzelle und zwölf IO-Pins pro Eckzelle. Dadurch ist eine vollständige Homogenität bei der Kaskadierung gegeben.

Da die globalen Verbindungen insbesondere bei Verwendung der Kaskadierungstechnik b) sehr lang werden können, kann der unangenehme Effekt auftreten, daß die Zahl der globalen Verbindungen nicht ausreicht, da bekanntlich jede Verbindung nur von einem Signal genutzt werden kann. Um diesen Effekt zu minimieren, kann nach einer gewissen Länge der globalen Verbindungen ein Treiber eingeschleift werden. Der Treiber hat zum einen eine Verstärkung des Signals zur Aufgabe, die bei langen Strecken und entsprechend hohen Lasten, unbedingt erforderlich ist; zum anderen kann der Treiber in Tristate gehen und damit das Signal unterbrechen. Dadurch können die Abschnitte links und rechts, beziehungsweise oberhalb und unterhalb des Treibers von verschiedenen Signalen genutzt werden, sofern der Treiber in Tristate ist, ansonsten wird ein Signal durchgeschleift. Wichtig ist hierbei, daß die Treiber der einzelnen globalen Leitungen auch einzeln angesteuert werden können, d. h. ein globales Signal kann unterbrochen sein, das Nachbarsignal ist jedoch durchgeschleift. Somit können auf einer globalen Verbindung durchaus abschnittsweise verschiedene Signale anliegen, während die globale Nachbarverbindung tatsächlich global von ein und demselben Signal verwendet wird (vergleiche Fig. 22).

Zur besseren Kommunikation zwischen den Datenflußprozessoren und der Ladelogik können sogenannte Shared-Memories eingesetzt werden. So können zum Beispiel Programme von einer Festplatte, die im IO-Bereich eines Datenflußprozessors liegt zur Ladelogik durchgereicht werden, indem die Datenflußprozessoren die Daten von der Platte in den Shared-Memory schreiben und die Ladelogik sie dort abholt. Dies ist besonders wichtig, da hier, wie bereits erwähnt, keine von-Neumann- sondern eine Harvardarchitektur vorliegt. Ebenso sind die Shared-Memories von Vorteil, wenn Konstanten, die im Programm — das im Speicherbereich der Ladelogik liegt — definiert sind, mit Daten — die im Speicherbetrieb der Datenflußprozessoren liegen — verknüpft werden sollen.

Weiterbildungen der vorstehend definierten und umschriebenen Erfindung sind Gegenstand der Unteransprüche.

Eine besondere Verwendung des erfindungsgemäßen Datenflußprozessors ist darin zu sehen, daß er in Verbindung mit geeigneten Ein-/Ausgabe-Einheiten einer-

seits und einem Speicher andererseits die Basis für einen kompletten (komplexen) Rechner bilden kann. Dabei kann ein Großteil der IO-Funktionen als MACROS auf dem Datenflußprozessor implementiert werden und es brauchen momentan lediglich Spezialbausteine (Ethernet-Treiber, VRAMS ...) extern zugefügt zu werden. Bei einer Normänderung oder Verbesserung muß dann wie bereits angedeutet nur das MACRO softwareseitig gewechselt werden; ein Eingriff in die Hardware ist nicht notwendig. Es bietet sich hier an, einen IO-(Eingabe-/Ausgabe-) Stecker festzulegen, über welchen dann die Zusatzbausteine angeschlossen werden können.

Fig. 20 zeigt den stark vereinfachten Aufbau eines heute üblichen Rechners. Durch den Einsatz eines DFP-Bausteins können erhebliche Teile eingespart werden (Fig. 21), wobei die entsprechenden herkömmlichen Baugruppen (CPU, Speicherverwaltung, SCSI-, Tastatur- und Videointerface, sowie der parallelen und seriellen Schnittstellen) als MACROS in die kaskadierten DFPs abgelegt werden. Nur die durch einen DFP nicht nachbildbaren Teile wie Speicher und Leitungstreiber mit nicht TTL-Pegeln oder für hohe Lasten müssen extern zugeschaltet werden. Durch die Verwendung des DFPs ist eine günstige Produktion gegeben, da ein und derselbe Baustein sehr häufig verwendet wird, das Layout der Platine ist durch die homogene Vernetzung entsprechend einfach. Zudem wird der Aufbau des Rechners durch die Ladelogik bestimmt, die hier für gewöhnlich nur zu Beginn der Abarbeitung (nach einem Reset) das DFP-Array lädt, wodurch eine günstige Fehlerkorrektur- und Erweiterungsmöglichkeit gegeben ist. Ein derartiger Rechner kann insbesondere mehrere verschiedene Rechnerstrukturen simulieren, indem einfach der Aufbau des zu simulierenden Rechners in das DFP-Array geladen wird. Zu bemerken ist, daß hierbei der DFP nicht in seiner Funktion als DFP arbeitet sondern lediglich ein hochkomplexes und frei programmierbares Logikarray zur Verfügung stellt, sich hierbei jedoch von herkömmlichen Bausteinen in seiner besonderen guten Kaskadierbarkeit unterscheidet.

Ein weiteres Einsatzgebiet des Bausteins ist der Aufbau großer neuronaler Netze. Sein besonderer Vorzug liegt hierbei in seiner hohen Gatterdichte, seiner ausgezeichneten Kaskadierbarkeit, sowie seiner Homogenität. Ein Lernvorgang, der eine Änderung einzelner axiomatischer Verbindungen beziehungsweise einzelner Zellfunktionen beinhaltet ist auf üblichen Bausteinen ebenso schlecht durchführbar, wie der Aufbau großer homogener und gleichzeitig flexibler Zellstrukturen. Die dynamische Umkonfigurierbarkeit ermöglicht erstmalig die optimale Simulation von Lernvorgängen.

Die vorliegende Erfindung wird im folgenden anhand der weiteren Figuren näher erläutert. Insgesamt zeigen

Fig. 1 ein Schaltsymbol für einen 8-Bit-Addierer;

Fig. 2 ein Schaltsymbol für einen aus acht 1-Bit-Addierern bestehenden 8-Bit-Addierer nach Fig. 1;

Fig. 3 eine logische Struktur eines 1-Bit-Addierers entsprechend Fig. 2;

Fig. 4 eine Zellenstruktur des 1-Bit-Addierers entsprechend Fig. 3;

Fig. 5 einen der Zellenstruktur nach Fig. 1 entsprechend aufgebauten 8-Bit-Addierer;

Fig. 6 ein aus vier Zellen bestehendes unprogrammiertes SUBMACRO X (analog einem 1-Bit-Addierer gemäß Fig. 4 beziehungsweise Fig. 5) mit den erforderlichen Leitungsanschlüssen;

Fig. 7 einen Teilausschnitt eines integrierten Schaltkreises (Chip) mit einer Vielzahl von Zellen und einem

separierten SUBMACRO X gemäß Fig. 6;

Fig. 8 einen integrierten Schaltkreis (Chip) mit einer Orthogonalstruktur einer quasi beliebigen Vielzahl von Zellen und einer extern zugeordneten Ladelogik;

Fig. 9 ein erstes Ausführungsbeispiel einer Mehrzahl miteinander zu einem Rechenwerk gekoppelter integrierter Schaltkreise (Datenflußprozessor) nach Fig. 8;

Fig. 10 ein zweites Ausführungsbeispiel einer Mehrzahl miteinander zu einem Rechenwerk gekoppelter integrierter Schaltkreise (Datenflußprozessor) nach Fig. 8;

Fig. 11 ein Ausführungsbeispiel eines MACRO zur Addition zweier Zahlenreihen;

Fig. 12 einen beispielhaften Aufbau einer Zelle mit Multiplexern zur Auswahl der jeweiligen logischen Bausteine;

Fig. 13 eine zum Beispiel mit einem Standard-TTL-Baustein 74148 ausgeführte Synchronisationslogik;

Fig. 14 die Kaskadierung von vier DFPs, wobei die Verbindung zwischen den IO-Pins nur schematisch dargestellt sind (tatsächlich bedeutet eine gezeichnete Verbindung eine Mehrzahl von Leitungen);

Fig. 15 die durch die Kaskadierung erreichte Homogenität;

Fig. 16a die Struktur der E/A-Zellen, wobei die globalen Verbindungen nicht herausgeführt werden,

Fig. 16b die Struktur der E/A-Zellen, jedoch mit herausgeführten globalen Verbindungen;

Fig. 17a die aus Fig. 16a resultierende Kaskadierung, wobei eine Eckzelle, sowie die zwei mit ihr kommunizierenden Treiberzellen der kaskadierten Bausteine (vergleiche hierzu Fig. 14) gezeichnet sind;

Fig. 17b die aus Fig. 16b resultierende Kaskadierung, wobei eine Eckzelle, sowie die zwei mit ihr kommunizierenden Treiberzellen der kaskadierten Bausteine (vergleiche hierzu Fig. 14) gezeichnet sind;

Fig. 18a eine Multiplikationsschaltung (vergleiche Fig. 11a);

Fig. 18b die interne Struktur des DFPs nach dem Laden (vergleiche Fig. 11b);

Fig. 19c die Arbeitsweise des DFPs im Speicher, sowie die Zustände der Zähler 47, 49;

Fig. 19 eine Kaskadenschaltung, wobei der Addierer aus Fig. 11 und der Multiplizierer aus Fig. 18 zur Steigerung der Rechenleistung hintereinander geschaltet sind;

Fig. 20 den stark schematisierten Aufbau eines herkömmlichen Rechners;

Fig. 21 den möglichen Aufbau desselben Rechners mit Hilfe eines Arrays aus kaskadierten DFPs;

Fig. 22 einen Ausschnitt mit eingezeichneten (Leitungs-) Treibern eines DFPs.

In Fig. 1 ist ein Schaltsymbol eines 8-Bit-Addierers dargestellt. Das Schaltsymbol besteht aus einem quadratischen Baustein 1 mit acht Eingängen A 0 ... 7 für ein erstes Datenwort A und acht Eingängen B 0 ... 7 für ein zweites (zu addierendes) Datenwort B. Die jeweils acht Eingänge A_i, B_i werden ergänzt durch einen weiteren Eingang Ü_{ein} über den dem Baustein 1 gegebenenfalls ein Übertrag zugeleitet wird. Der Baustein 1 hat funktions- und bestimmungsgemäß acht Ausgänge S 0 ... 7 für binären Summanden und einen weiteren Ausgang Ü_{aus} für den gegebenenfalls bestehenden Übertrag.

Das in Fig. 1 dargestellte Schaltsymbol ist in Fig. 2 als Anordnung sogenannter SUBMACROS dargestellt. Diese SUBMACROS 2 bestehen je aus einem 1-Bit-Addierer 3 mit je einem Eingang für die entsprechenden Bits des Datenworts und einem weiteren Eingang für ein

Übertragsbit. Die 1-Bit-Addierer 3 weisen darüberhinaus einen Ausgang für den Summanden und einen Ausgang für den Übertrag Üaus auf.

In Fig. 3 ist die binäre Logik eines 1-Bit-Addierers beziehungsweise eines SUBMACROS 2 nach Fig. 2 dargestellt. Analog zu Fig. 2 weist diese Schaltlogik je einen Eingang Ai, Bi für die konjugierten Bits der zu verknüpfenden Daten auf; ferner ist ein Eingang Üein für den Übertrag vorgesehen. Diese Bits werden den dargestellten Verbindungen beziehungsweise Verknüpfungen entsprechend in zwei ODER-Gliedern 5 und drei NAND-Gliedern 6 verknüpft, so daß am Ausgangsanschluß Si und am Ausgang für den Übertrag Üaus die einem Volladdierer entsprechenden Verknüpfungsergebnisse (Si, Üaus) anstehen.

Die Erfindung setzt da ein, wo es — wie in Fig. 4 dargestellt — darum geht, das in Fig. 3 gezeigte SUBMACRO 2 oder eine oder mehrere beliebige Funktion(en) in geeigneter Weise in einer Zellstruktur zu implementieren. Dies geschieht auf der Grundlage logisch und strukturell identischer Zellen 10, deren einzelne logische Bausteine der auszuführenden Verknüpfungsfunktion entsprechend miteinander gekoppelt werden, und zwar mittels der noch zu beschreibenden Ladelogik. Gemäß der in Fig. 4 gezeigten, von der Schaltlogik nach Fig. 3 abgeleiteten Verknüpfungslogik für einen 1-Bit-Addierer sind je zwei Zellen 10.1, 10.2 bezüglich der logischen Bausteine insoweit gleich, daß jeweils ein ODER-Glied 5 und ein NAND-Glied 6 aktiviert sind. Eine dritte Zelle 10.3 wird nur als Leitungszelle (Leiterbahnzelle) benutzt und die vierte Zelle 10.4 ist bezüglich des dritten NAND-Gliedes 6 aktiv geschaltet. Das aus den vier Zellen 10.1 ... 10.4 bestehende SUBMACRO 2 steht somit stellvertretend für einen 1-Bit-Addierer, d. h. ein 1-Bit-Addierer einer Datenverarbeitungseinrichtung gemäß der vorliegenden Erfindung wird über vier entsprechend programmierte (konfigurierte) Zellen 10.1 ... 10.4 verifiziert. (Der Vollständigkeit halber soll angemerkt werden, daß die einzelnen Zellen ein erheblich umfangreicheres Netzwerk von logischen Bausteinen, sprich Verknüpfungsgliedern, und Invertern aufweist, die jeweils dem aktuellen Befehl der Ladelogik zufolge aktiv geschaltet werden können. Neben den logischen Bausteinen ist auch ein dichtes Netz von Verbindungsleitungen zwischen den jeweils benachbarten Bausteinen und zum Aufbau von zeilen- und spaltenweisen Busstrukturen zur Datenübertragung andererseits vorgesehen, so daß über eine entsprechende Programmierung seitens der Ladelogik quasi beliebige logische Verknüpfungsstrukturen implementiert werden können).

Der Vollständigkeit halber ist in Fig. 5 der Zellenaufbau eines 8-Bit-Addierers in seiner Gesamtheit dargestellt. Die in Fig. 5 gezeigte Struktur entspricht insoweit der nach Fig. 2, wobei die in Fig. 2 symbolisch als SUBMACROS 2 dargestellten 1-Bit-Addierer jeweils durch eine vier-zellige Einheit 10.1 ... 10.4 ersetzt sind. Bezogen auf den erfindungsgemäßen Datenflußprozessor bedeutet dies, daß zweiunddreißig Zellen der zur Verfügung stehenden Gesamtheit von Zellen einer zellular mit logisch identischem Layout gefertigten Schaltungsplatine seitens der Ladelogik so angesteuert und konfiguriert beziehungsweise programmiert werden, daß diese zweiunddreißig Zellen ein 8-Bit-Addierer bilden.

In der Darstellung nach Fig. 5 ist über eine strichpunktierte Umrahmung ein SUBMACRO "X" zeichnerisch separiert, das letztlich als aus vier einem 1-Bit-Addierer entsprechend programmierten Zellen (10 gemäß

Fig. 4) bestehende Untereinheit zu betrachten ist.

Das in Fig. 5 separierte SUBMACRO "X" ist in Fig. 6 als Teil eines integrierten Schaltkreises (Chip) 20 gemeinsam mit Leitungs- und Datenanschlüssen dargestellt. Das SUBMACRO "X" besteht aus den vier Zellen 10 die entsprechend der orthogonalen Struktur je Seite vier Datenanschlüsse (also insgesamt sechzehn Datenanschlüsse je Zelle) aufweisen. Die Datenanschlüsse verbinden jeweils benachbarte Zellen, so daß ersichtlich wird, wie beispielsweise eine Dateneinheit von Zelle zu Zelle durchgeschleust wird. Die Ansteuerung der Zellen 10 erfolgt einerseits über sogenannte lokale Steuerungen, das sind lokale Leitungen, die mit allen Zellen verbunden sind, und andererseits über sogenannte globale Leitungen, d. h. Leitungen, die über den gesamten integrierten Schaltkreis (Chip) 20 geführt sind.

In Fig. 7 ist ein vergrößerter Ausschnitt eines integrierten Schaltkreises 20 dargestellt, der mit einem orthogonalen Raster von Zellen 10 belegt ist. Wie in Fig. 7 angedeutet kann so zum Beispiel eine Gruppe von vier Zellen 10 als SUBMACRO "X" ausgewählt und dem 1-Bit-Addierer entsprechend Fig. 4 gemäß programmiert beziehungsweise konfiguriert werden.

Ein vollständiger integrierter Schaltkreis (Chip) 20 ist in Fig. 8 dargestellt. Dieser integrierte Schaltkreis 20 besteht aus einer Vielzahl im orthogonalen Raster angeordneter Zellen 10 und weist an seinen Außenkanten eine entsprechende Anzahl von Leitungsanschlüssen (Pins) auf, über die Signale, insbesondere Ansteuersignale und Daten zugeführt und weitergeleitet werden können. In Fig. 8 ist wiederum das SUBMACRO "X" gemäß Fig. 5/ Fig. 6 abgegrenzt; darüberhinaus sind auch weitere SUBMACROS separiert, die spezifischen Funktionen und Vernetzungen entsprechend zu Untereinheiten zusammengefaßt sind. Dem integrierten Schaltkreis (Chip) 20 ist eine Ladelogik 30 zugeordnet beziehungsweise übergeordnet, über die der integrierte Schaltkreis 20 programmiert und konfiguriert wird. Die Ladelogik 30 teilt letztlich dem integrierten Schaltkreis 20 mit, wie er arithmetisch-logisch zu arbeiten hat. Bezugnehmend auf die Fig. 1 bis 5 ist in Fig. 8 einerseits das SUBMACRO "X" entsprechend Fig. 4 und Fig. 5 hervorgehoben; andererseits ist auch ein MACRO "Y" entsprechend Fig. 1 und Fig. 2 angezeichnet, das als Einheit einem 8-Bit-Addierer entspricht.

Anhand von Fig. 9 beziehungsweise Fig. 10 soll im folgenden eine Rechnerstruktur beschrieben werden, die auf den im vorstehenden definierten und erläuterten integrierten Schaltkreis 20 aufbaut.

Gemäß dem in Fig. 9 dargestellten ersten Ausführungsbeispiel ist — analog zur Anordnung der Zellen — im Orthogonalraster eine Mehrzahl von integrierten Schaltkreisen 20 angeordnet, deren jeweils benachbarte über lokale BUS-Leitungen 21 miteinander gekoppelt beziehungsweise vernetzt sind. Die — beispielsweise aus sechzehn integrierten Schaltkreisen 20 bestehende — Rechnerstruktur weist Ein-/Ausgangsleitungen IO auf, über die der Rechner quasi mit der Außenwelt in Verbindung steht, d. h. korrespondiert. Der Rechner gemäß Fig. 9 weist ferner einen Speicher 22 auf, der dem dargestellten Ausführungsbeispiel entsprechend aus zwei separierten Speichern, zusammengesetzt aus jeweils RAM, ROM sowie einem Dual-Ported RAM als shared memory zu der Ladelogik geschaltet, besteht, die gleichermaßen als Schreib-Lese-Speicher oder auch nur als Lese-Speicher realisiert sein können. Der soweit beschriebenen Rechnerstruktur ist die Ladelogik 30 beziehungsweise übergeordnet, mittels der die inte-

grierten Schaltkreise (Datenflußprozessor) 20 programmiert und konfiguriert und vernetzt werden.

Die Ladelogik 30 baut auf einem Transputer 31, d. h. einem Prozessor mit mikrocodiertem Befehlssatz auf, dem seinerseits ein Speicher 32 zugeordnet ist. Die Verbindung zwischen dem Transputer 31 und dem Datenflußprozessor basiert auf einer Schnittstelle 33 für die sogenannten Ladedaten, d. h. die Daten die den Datenflußprozessor aufgabenspezifisch programmieren und konfigurieren und einer Schnittstelle 34 für den bereits genannten Rechnerspeicher 22, d. h. den Shared-Memory-Speicher.

Die in Fig. 9 dargestellte Struktur stellt so einen kompletten Rechner dar, der über die Ladelogik 30 jeweils fall- beziehungsweise aufgabenspezifisch programmiert und konfiguriert werden kann. Der Vollständigkeit halber sei noch angemerkt, daß — wie in Verbindung mit der Ladelogik 30 über Pfeile angedeutet — mehrere dieser Rechner vernetzt, d. h. miteinander gekoppelt werden können.

Ein weiteres Ausführungsbeispiel einer Rechnerstruktur ist in Fig. 10 dargestellt. Im Unterschied zu Fig. 9 sind dabei neben den lokalen BUS-Leitungen zwischen den benachbarten integrierten Schaltkreisen 20 noch übergeordnete zentrale BUS-Leitungen 23 vorgesehen, um zum Beispiel spezifische Ein- beziehungsweise Ausgangsprobleme lösen zu können. Auch der Speicher 22 (Shared-Memory) ist über zentrale BUS-Leitungen 23 mit den integrierten Schaltkreisen 20 verbunden, und zwar wie dargestellt jeweils mit Gruppen dieser integrierten Schaltkreise. Die in Fig. 10 dargestellte Rechnerstruktur weist die gleiche Ladelogik 30 auf, wie sie anhand von Fig. 9 erläutert wurde.

In Verbindung mit Fig. 11a soll eine auf erfindungsgemäßen Datenflußprozessoren aufgebaute Additionsschaltung erläutert werden. Ausgegangen wird von zwei Zahlenreihen An und Bn für sämtliche n zwischen 0 und 9; die Aufgabe besteht darin, die Summe $C_i = A_i + B_i$ zu bilden, wobei der Index i die Werte $0 \leq n < 9$ annehmen kann.

Bezugnehmend auf die Darstellung nach Fig. 11a ist die Zahlenreihe An in einem ersten Speicher RAM1 abgespeichert und zwar zum Beispiel ab einer Speicheradresse 1000h; die Zahlenreihe Bn ist in einem Speicher RAM2 an einer Speicheradresse 0dfa0h abgespeichert; die Summe Cn wird in den RAM1 eingeschrieben und zwar unter der Adresse 100ah.

Es ist ein weiterer Zähler 49 zugeschaltet, der lediglich die einzelnen durch die Steuerschaltung freigegebenen Taktzyklen hochzählt. Dies soll im Weiteren zur Verdeutlichung der Umkonfigurierbarkeit einzelner MACROS ohne Beeinflussung der an der Umkonfigurierung nicht beteiligten MACROS dienen.

Fig. 11a zeigt zunächst die eigentliche Additionsschaltung 40, die aus einem ersten Register 41 zur Aufnahme der Zahlenreihe An und einem zweiten Register 42 zur Aufnahme der Zahlenreihe Bn besteht. Den beiden Registern 41/42 ist ein 8-Bit-Addierer entsprechend dem in Fig. 1 dargestellten MACRO 1 nachgeschaltet. Der Ausgang des MACRO 1 führt über eine Treiberschaltung 43 zurück zum Speicher RAM1. Die Taktbeziehungsweise Zeitsteuerung der Additionsschaltung 40 erfolgt über eine von einem Taktgenerator T angesteuerte Zeitsteuerung (STATEMACHINE) 45, die mit den Registern 41, 42 und der Treiberschaltung 43 verbunden ist.

Die Additionsschaltung 40 wird funktional durch eine Adreßschaltung 46 zur Generierung der Adreßdaten für

die abzuspeichernden Additionsergebnisse ergänzt. Die Adreßschaltung 46 besteht ihrerseits aus drei MACROS 1 (gemäß Fig. 1) zur Bildung der Adreßdaten, wobei diese MACROS 1 wie folgt geschaltet sind: Über jeweils einen Eingang werden die zu verknüpfenden Adressen für An, Bn, Cn zugeführt. Diese Adressen werden mit den Ausgangssignalen eines Zählers 47 addiert und mit der Statemachine 45 so verknüpft, daß am Ausgang die neue Zieladresse ansteht. Der Zähler 47 und der Komparator 48 haben dabei die Aufgabe sicherzustellen, daß jeweils die richtigen Summanden verknüpft werden und daß jeweils am Ende der Zahlenreihen, d. h. bei $n = 9$ abgebrochen wird. Ist die Addition vollendet, so wird in der Zeitsteuerung 45 ein STOP-Signal generiert und die Schaltung passiv geschaltet. Ebenso kann das STOP-Signal als Eingangssignal für eine Synchronisations-Schaltung verwendet werden, indem die Synchronisationslogik anhand dieses Signals erkennen kann, daß die Gesamtfunktion "Addieren" gemäß dem nachfolgend beschriebenen ML1 Programm beendet ist und die MACROS somit durch neue ersetzt werden können (zum Beispiel könnte STOP das Signal Sync5 sein).

Der Zeitablauf in der Zeitsteuerung 45 (STATEMACHINE) läßt sich dabei wie folgt darstellen, wobei noch anzumerken ist, daß in der Zeitsteuerung 45 eine Verzögerungszeit T (in Form von Taktzyklen) zwischen der Adreßgenerierung und dem Datenerhalt implementiert ist:

- Im Zyklus 1 wird jeweils der Zähler 47 um 1 erhöht und im Komparator 48 wird geprüft, ob $n > 9$ erreicht ist; synchron zu diesen Operationen werden die Adressen für A, B, C berechnet;
- im Zyklus (T + 1) werden die Summanden A, B ausgelesen und addiert;
- im Zyklus (T + 2) wird die Summe C abgespeichert.

Mit anderen Worten heißt dies, daß die Operationschleife und die eigentliche Addition gerade (T + 2) Taktzyklen erfordert. Im allgemeinen sind für T 2 ... 3 Takte erforderlich, so daß verglichen mit den herkömmlichen Prozessoren (CPU), die im allgemeinen 50 bis mehrere 100 Taktzyklen bedingen, eine ganz wesentliche Rechenzeit-Reduzierung möglich wird.

Die anhand von Fig. 11 aufgezeigte Konfiguration soll im folgenden über eine hypothetische MACRO-Sprache ML1 nochmals erläutert werden:
Es existieren die Zahlenreihen An und Bn

$$\forall n: 0 \leq n \leq 9$$

Es sollen die Summen $C_i = A_i + B_i$ mit $i \in \mathbb{N}$ gebildet werden.

```
const n = 9;
array A[n] in RAM[1] at 1000h;
array B[n] in RAM[2] at 0dfa0h;
array C[n] in RAM[1] at 100ah;
for i = 0 to n with (A[i], B[i], C[i])
```

```
Δ1;
```

```
C = Δ1 = A + B;
```

```
next;
```

```
RAM1 ist der 1. Speicherblock
```

```
RAM2 ist der 2. Speicherblock
```

```
at folgt die Basisadresse der Arrays
```

```
for ist der Schleifenbeginn
```

```
next ist das Schleifenende
```

```
with ( ) folgen die Variablen, deren Adressen durch die
```

Zählvariable i bestimmt werden

ΔT folgt die Verzögerungszeit für eine Statemachine in Taktzyklen.

Das Timing der Statemachine sieht demnach folgendermaßen aus:

Zyklus	Aktivität
1	Zähler erhöhen, Vergleich auf > 9 (ja $\Rightarrow$ Abbruch) und Adressen für A, B, C, berechnen
T + 1	A, B, holen und addieren
T + 2	Nach C speichern

Das heißt — wie bereits erwähnt — die Schleife und die Addition benötigen gerade einmal $T + 2$ Taktzyklen.

Fig. 11b zeigt den groben Aufbau der einzelnen Funktionen (MACROS) in einem DFP. Die MACROS sind in ihrer etwaigen Lage und Größe eingezeichnet und mit den anhand von Fig. 11a erläuterten entsprechenden Nummern versehen.

Fig. 11c zeigt den groben Aufbau der einzelnen Funktionen auf die RAM-Blöcke 1 und 2: Die Summanden werden nacheinander in aufsteigender Reihenfolge aus den RAM-Blöcken 1 und 2 ab Adresse 1000h beziehungsweise 0dfa0h gelesen und in RAM-Block 1 ab Adresse 100ah gespeichert. Zudem sind die Zähler 47 und 49 gegeben, beide zählen während des Ablaufs der Schaltung von 0 bis 9.

Nach Beendigung des beschriebenen Programms soll ein neues Programm geladen werden, das die Ergebnisse weiterverwertet. Die Umladung soll zur Laufzeit erfolgen. Das Programm ist im Folgenden gegeben:

Es existieren die Zahlenreihen A_n und B_n , wobei A_n durch das Ergebnis C_n des vorher ausgeführten Programms gegeben ist:

$$\forall n: 0 \leq n \leq 9$$

Es sollen die Produkte $C_i = A_i \cdot B_i$ mit $i \in N$ gebildet werden.

```
const n = 9;
array A[n] in RAM[1] at 100ah
array B[n] in RAM[2] at 0dfa0h
array C[n] in RAM[1] at 1015h
for i = 0 to n with (A[i], B[i], C[i])
  Δ1;
C = Δ1 = A * B;
next;
Die Beschreibung der einzelnen Befehle ist bereits bekannt;
* symbolisiert die Multiplikation.
```

Die MACRO-Struktur ist in Fig. 18a beschrieben, Fig. 18b gibt in bekannter Weise die Lage und Größe der einzelnen MACROS auf dem Chip an, besonders zu beachten ist die Größe des Multiplizierers 2 in Vergleich zu Addierer 1 aus Fig. 11b. In Fig. 18c ist erneut die Auswirkung der Funktion auf den Speicher aufgezeigt, Zähler 47 zählt erneut von 0 bis 9, d. h. er wird beim Nachladen der MACROS zurückgesetzt.

Besonders zu beachten ist der Zähler 49. Angenommen, das Umladen der MACROS beträgt 10 Taktzyklen. Dann läuft der Zähler 49 von 9 auf 19, da der Baustein dynamisch umgeladen wird, d. h. nur die umzuladenden Teile werden gestoppt, der Rest arbeitet weiter. Das führt nun dazu, daß der Zähler während des Programm-

ablaufs von 19 auf 29 hochläuft. (Hiermit soll das dynamische unabhängige Umladen demonstriert werden, in jedem bisher bekannten Baustein würde der Zähler erneut von 0 auf 9 laufen, da er zurückgesetzt wird).

Bei näherer Betrachtung des Problems stellt sich die Frage, warum nicht beide Operationen, die Addition und die Multiplikation in einem Zyklus durchgeführt werden, also die Operation:

Es existieren die Zahlenreihen A_n und B_n , wobei A_n durch das Ergebnis von C_n des vorher ausgeführten Programms gegeben ist:

$$\forall n: 0 \leq n \leq 9$$

Es sollen die Produkte $C_i = (A_i + B_i) \cdot B_i$ mit $i \in N$ gebildet werden.

```
path D;
const n = 9;
array A[n] in RAM[1] at 1000h
array B[n] in RAM[2] at 0dfa0h
array C[n] in RAM[1] at 100ah
for i = 0 to n with (A[i], B[i], C[i])
  Δ1;
D = Δ1 = A + B;
C = Δ1 = D * B;
next;
```

path D definiert einen internen nicht aus den DFP herausgeführten Doppelpfad. Die Operation benötigt wegen einem zusätzlichen $\Delta 1$ einen Taktzyklus mehr als vorher, ist insgesamt jedoch schneller als die beiden obigen Programme in Folge ausgeführt, da zum einen die Schleife nur einmal durchlaufen wird, zum zweiten nicht umgeladen wird.

Prinzipiell könnte das Programm auch so formuliert werden:

```
const n = 9;
array A[n] in RAM[1] at 1000h
array B[n] in RAM[2] at 0dfa0h
array C[n] in RAM[1] at 100ah
for i = 0 to n with (A[i], B[i], C[i])
  Δ - 1;
C = Δ2 = (A + B) * B;
next;
```

Sind die Gatterlaufzeiten des Addierers und des Multiplizierers zusammen kleiner als ein Taktzyklus, kann die Operation $(A + B) \cdot B$ auch in einem Taktzyklus durchgeführt werden, was zu einer weiteren erheblichen Geschwindigkeitssteigerung führt:

```
const n = 9;
array A[n] in RAM[1] at 1000h
array B[n] in RAM[2] at 0dfa0h
array C[n] in RAM[1] at 100ah
for i = 0 to n with (A[i], B[i], C[i])
  Δ1;
C = Δ1 = (A + B) * B;
next;
```

Anhand von Fig. 12 soll ein einfaches Beispiel eines Zellenaufbaus erläutert werden. Die Zelle 10 umfaßt zum Beispiel ein UND-Glied 51, ein ODER-Glied 52, ein XOR-Glied 53, einen Inverter 54 sowie eine Registerzelle 55. Die Zelle 10 weist darüberhinaus eingangsseitig zwei Multiplexer 56, 57 mit (den sechzehn Eingängen der Zelle entsprechend Fig. 6) zum Beispiel je sechzehn Eingangsanschlüssen IN1, IN2 auf. Über diesen (16:1)-Multiplexer 56/57 werden jeweils die den genannten logischen Gliedern UND, ODER, XOR 51 ... 53 zuzuführenden Daten ausgewählt. Diese logischen Glieder sind ausgangsseitig mit einem (3:1)-Multiple-

5
 10
 15
 20
 25

Der Vollständigkeit halber sei angemerkt, daß die Registerzelle 55 mit einem Reset-Eingang R und einem Takteingang gekoppelt ist.

Dem im vorstehenden erläuterten Zellenaufbau, d. h. der Zelle 10 ist nun eine Ladelogik 30 übergeordnet, die mit den Multiplexern 56, 57, 58 und 59 verbunden ist und diese den gewünschten Funktionen entsprechend ansteuert.

Sollen zum Beispiel die Signale A2 mit B5 verundet werden, so werden die Multiplexer 56, 57 den Leitungen "ZWEI" beziehungsweise "FÜNF" entsprechend aktiv geschaltet; die Summanden gelangen dann zum UND-Glied 51 und werden bei entsprechender Aktivierung der Multiplexer 58, 59 am Ausgang OUT abgegeben. Soll zum Beispiel eine NAND-Verknüpfung durchgeführt werden, so schaltet der Multiplexer 58 zum Inverter 54 und am Ausgang OUT steht dann das negierte UND-Ergebnis an.

Patentansprüche

1. Datenverarbeitungseinrichtung, wobei ein (im folgenden Datenflußprozessor — DFP — genannter) integrierter Schaltungskreis (Chip) mit einer Vielzahl insbesondere orthogonal zueinander angeordneter homogen strukturierter Zellen mit je einer Mehrzahl jeweils logisch gleicher und strukturell identisch angeordneter Bausteine vorgesehen ist, dessen Zellen zeilen- und spaltenweise, gegebenenfalls gruppenweise zusammengefaßt, mit Ein-/Ausgangsanschlüssen des integrierten Schaltkreises verbunden sind, **dadurch gekennzeichnet**, daß den Zellen eine Ladelogik zugeordnet ist, über die sie je für sich und gegebenenfalls gruppenweise zusammengefaßt so programmierbar (konfigurierbar) sind, daß beliebige logische Funktionen und/oder Vernetzungen untereinander verifizierbar sind, und zwar derart, daß eine Manipulation der DFP-Konfiguration während des Betriebes (oder zur Laufzeit), d. h. die Modifikation funktioneller Teile (MACROS) des DFPs erfolgen kann, ohne daß andere funktionelle Teile angehalten werden müssen oder in ihrer Funktion beeinträchtigt werden.
2. Datenverarbeitungseinrichtung nach Anspruch 1, dadurch gekennzeichnet, daß die Ladelogik mit Speichermitteln gekoppelt ist, über die die Konfiguration der Zellen spezifizierbar ist.
3. Datenverarbeitungseinrichtung nach einem der Ansprüche 1 bis 2, dadurch gekennzeichnet, daß die Ladelogik aus einem Prozessor besteht, der den gesamten Programmablauf auf der Grundlage von in verschiedenen Speichern abgelegten Daten und Programmen im Sinne einer Harvard-Struktur verwaltet.
4. Datenverarbeitungseinrichtung nach Anspruch 3, dadurch gekennzeichnet, daß die Ladelogik ihrerseits aus Zellen mit je einer Mehrzahl jeweils logisch gleicher und strukturell identisch angeordneter Bausteine aufgebaut ist.
5. Datenverarbeitungseinrichtung nach einem der

Ansprüche 1 oder 4, dadurch gekennzeichnet, daß die Zellen dynamisch während eines Programmablaufs umkonfigurierbar sind, ohne daß die zu bearbeitenden Daten selbst beeinflusst werden.

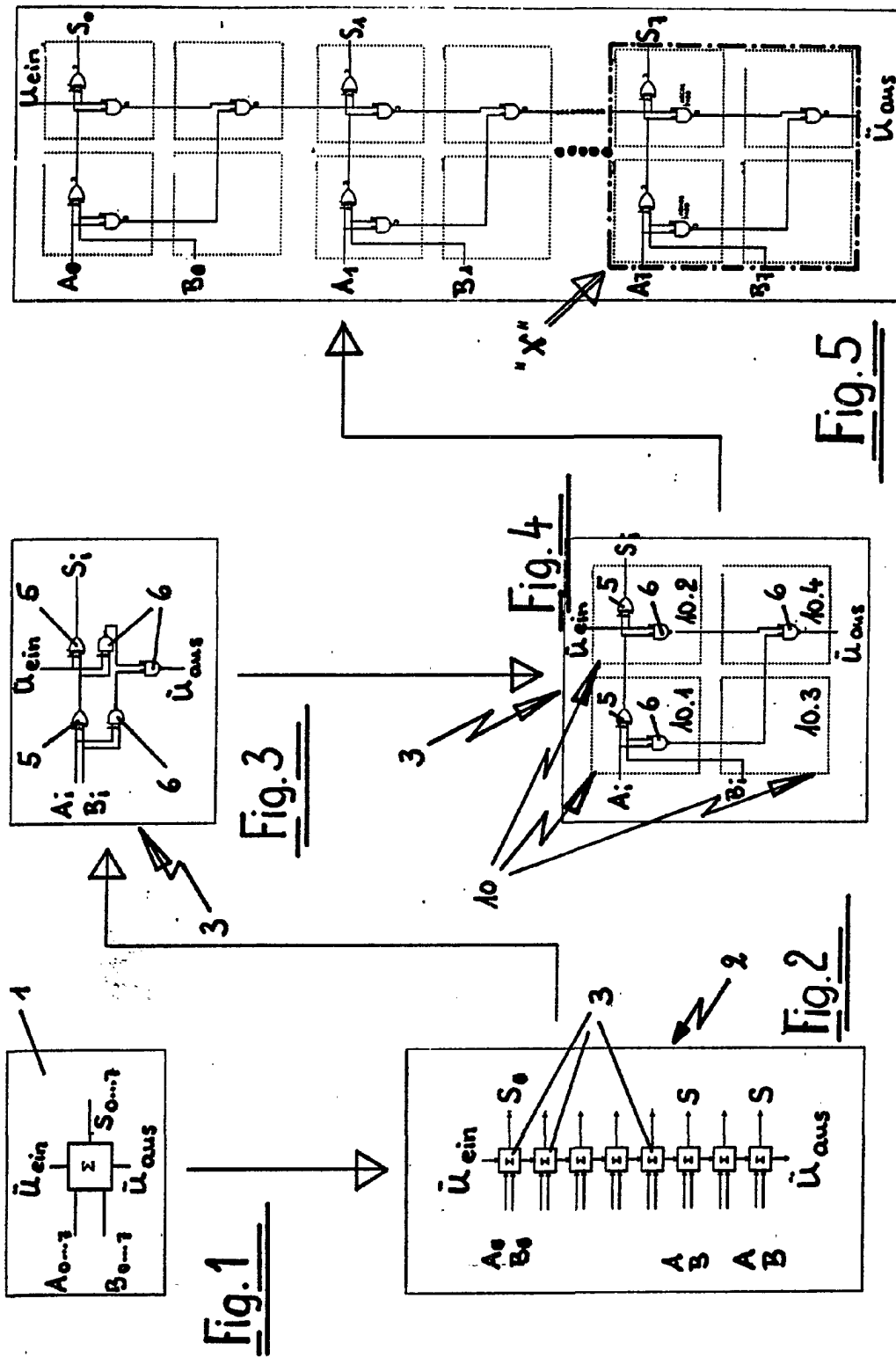
6. Datenverarbeitungseinrichtung, wobei ein (im folgenden Datenflußprozessor — DFP — genannter) integrierter Schaltungskreis (Chip) mit einer Vielzahl insbesondere orthogonal zueinander angeordneter homogen strukturierter Zellen mit je einer Mehrzahl jeweils logisch gleicher und strukturell identisch angeordneter Bausteine vorgesehen ist, dessen Zellen zeilen- und spaltenweise, gegebenenfalls gruppenweise zusammengefaßt, mit Ein-/Ausgangsanschlüssen des integrierten Schaltkreises verbunden sind, dadurch gekennzeichnet, daß eine Mehrzahl von ihnen in Kaskadenform koppelbar sind.

7. Datenverarbeitungseinrichtung nach einem der Ansprüche 1 bis 6, gekennzeichnet durch, die Zuordnung geeigneter Daten-Ein-/Ausgabe-Einheiten und mindestens eines Speichers zum Aufbau eines (komplexen, kompletten) Rechenwerks.

8. Datenverarbeitungseinrichtung nach einem der Ansprüche 1 bis 7, dadurch gekennzeichnet, daß die Funktionen der Ein-/Ausgabeeinheiten partiell im integrierten Schaltkreis (Chip) implementierbar sind.

Hierzu 11 Seite(n) Zeichnungen

- Leerseite -



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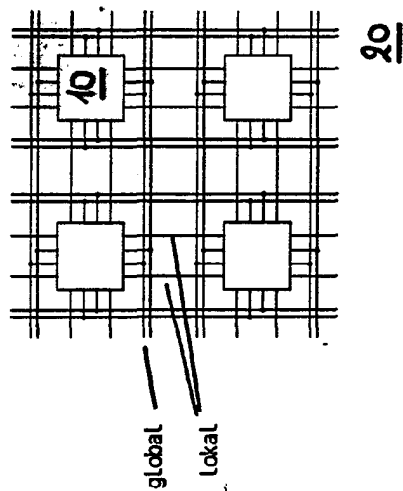


Fig. 6

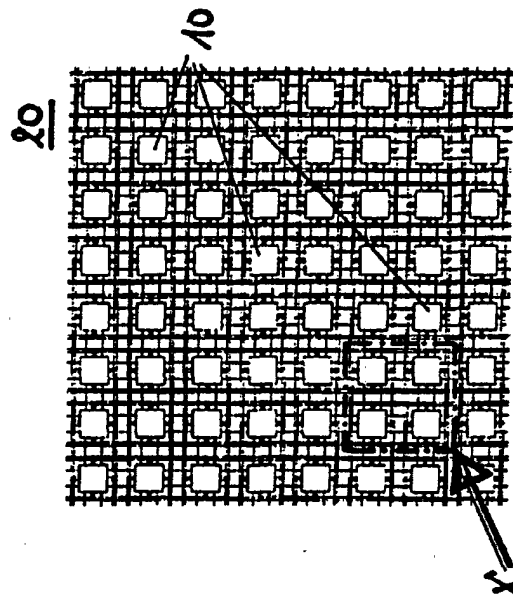


Fig. 7

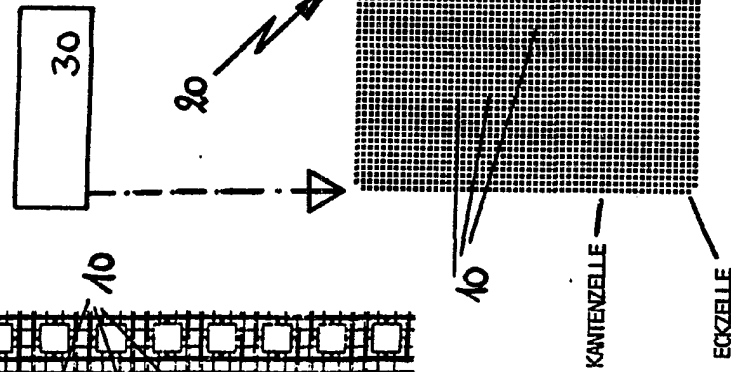
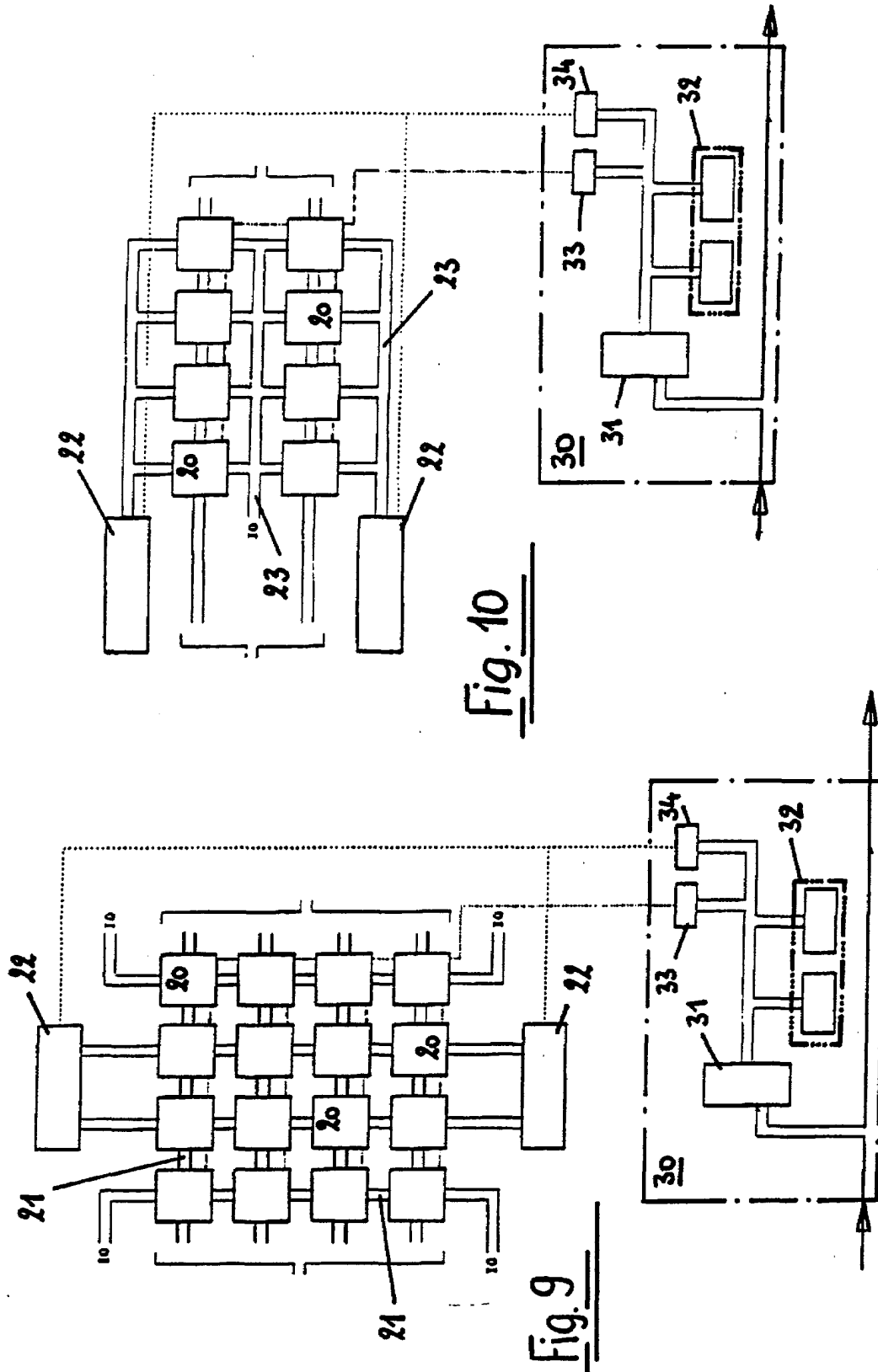


Fig. 8



408 046/623

Fig. 11 a

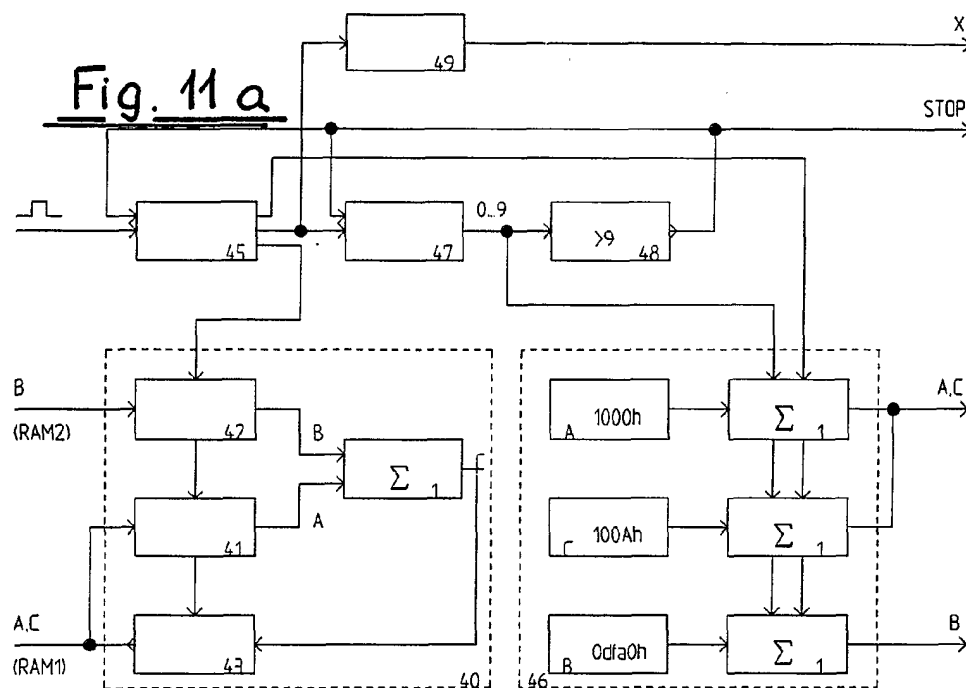
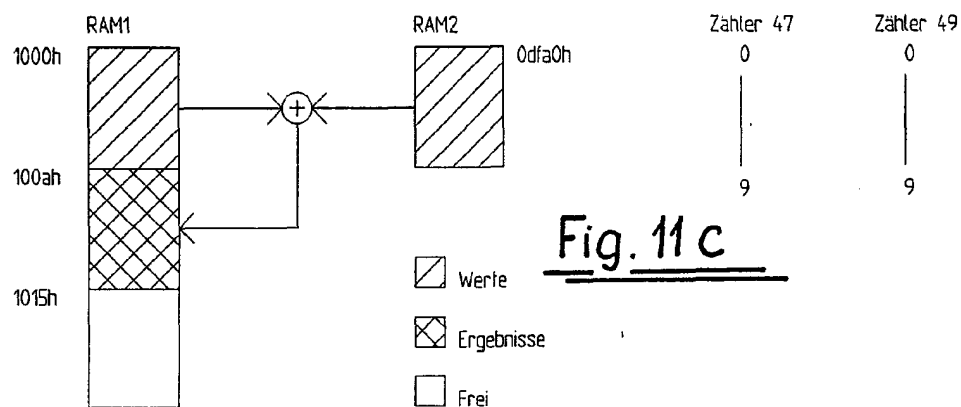
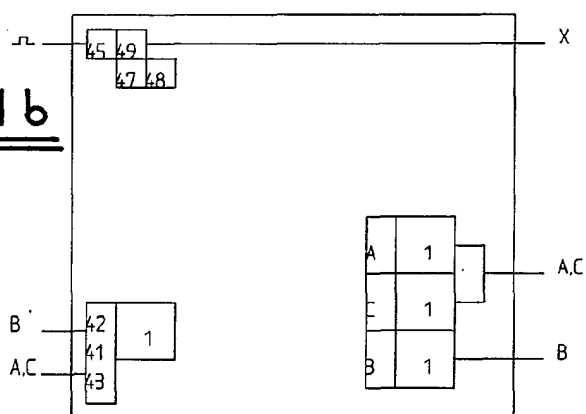


Fig. 11 b



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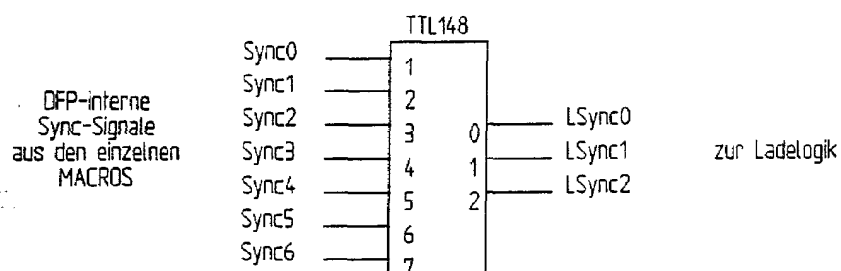
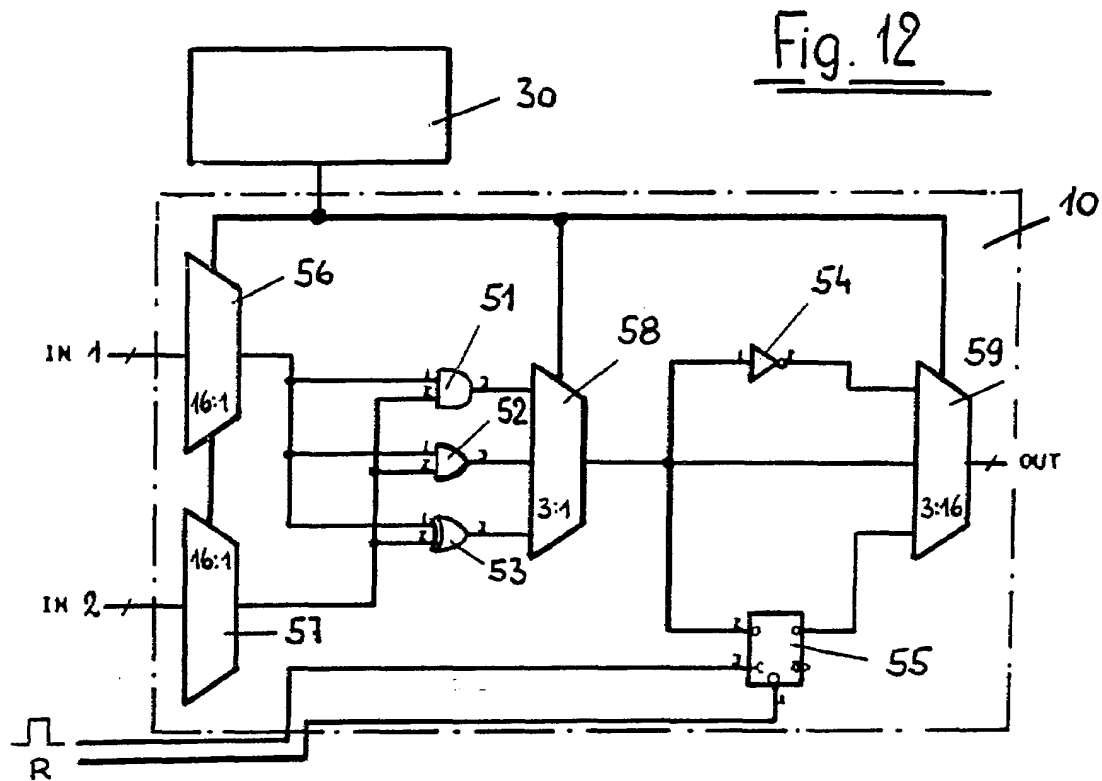


Fig. 13

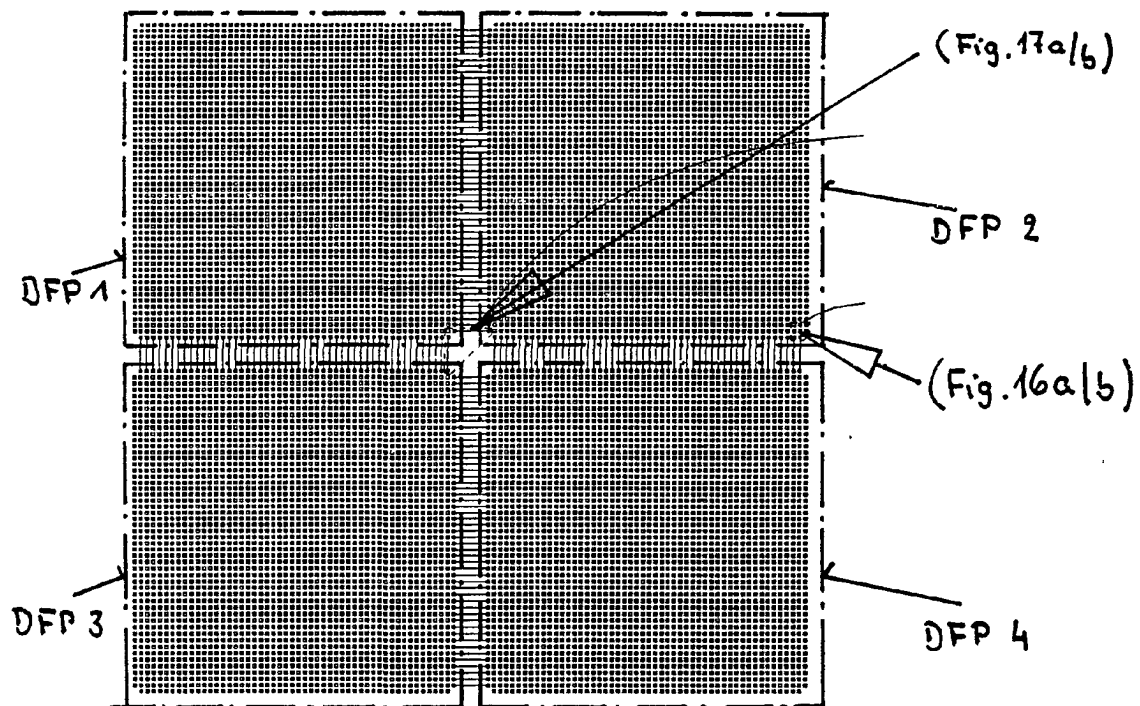


Fig. 14

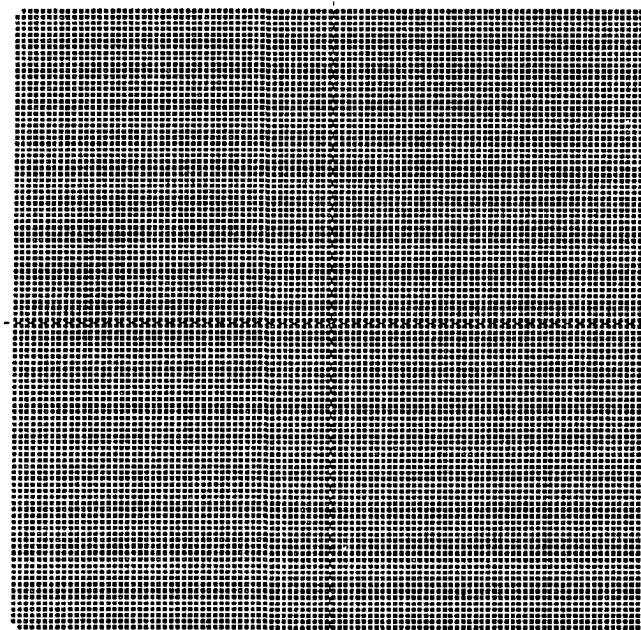


Fig. 15

408 046/623

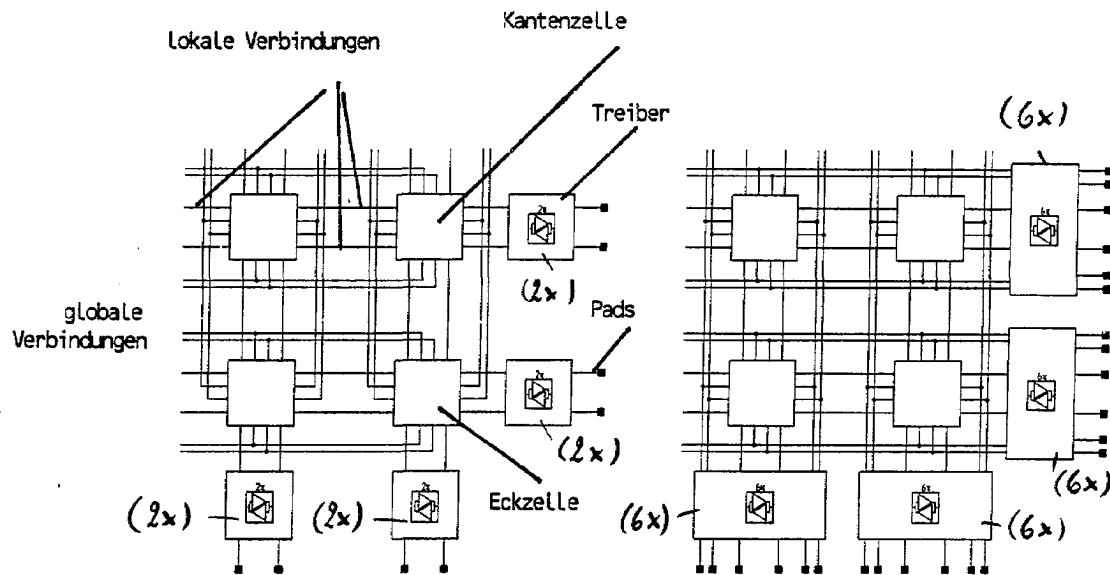


Fig. 16a

Fig. 16b

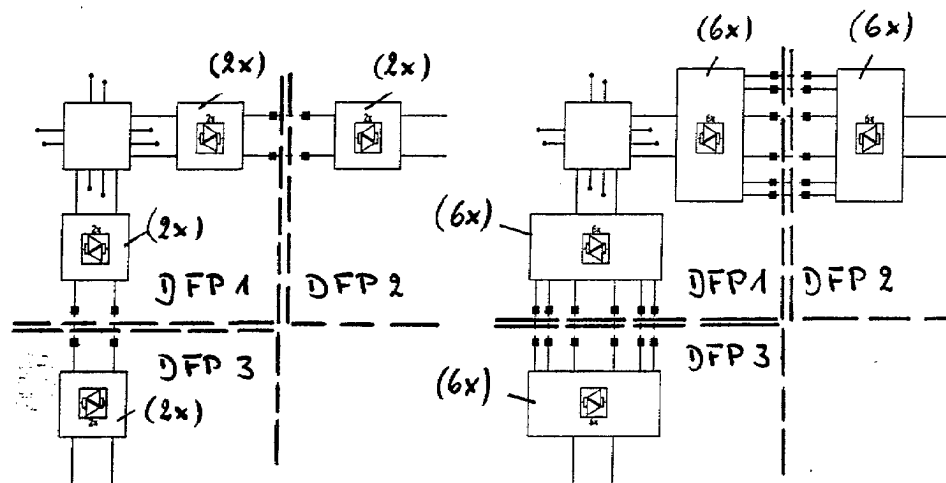


Fig. 17a

Fig. 17b

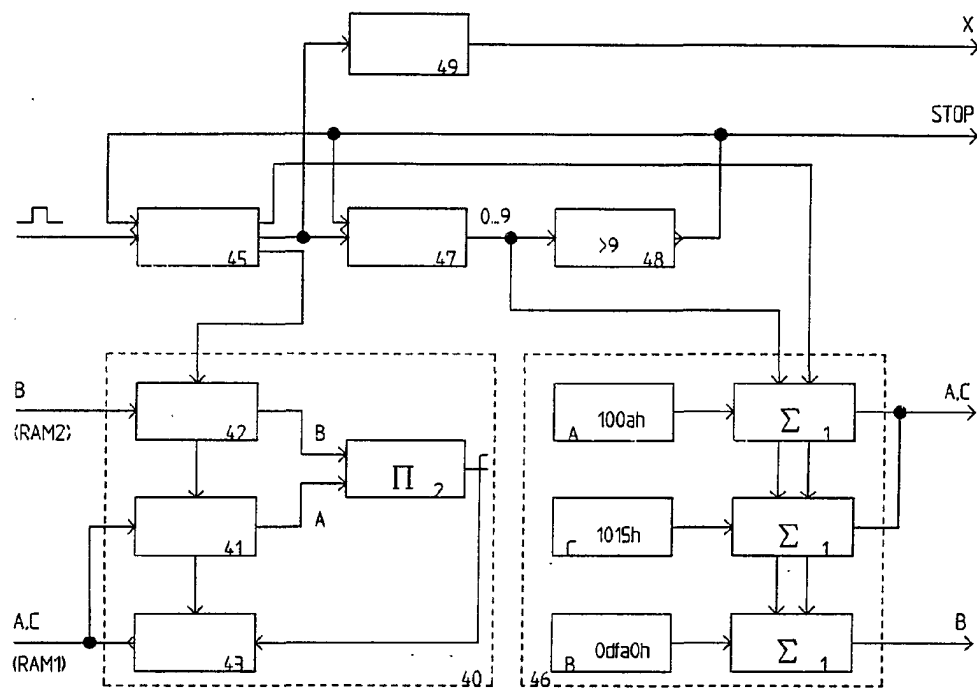


Fig. 18 a

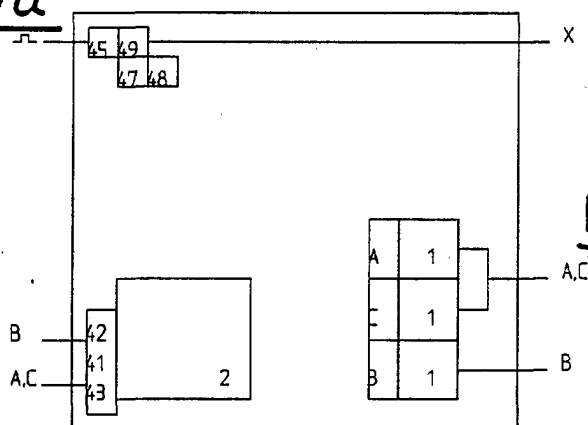


Fig. 18 b

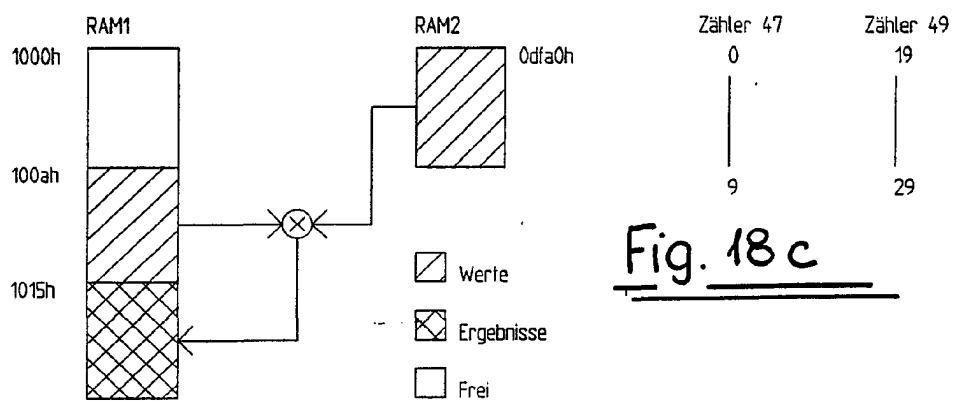
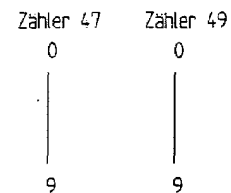
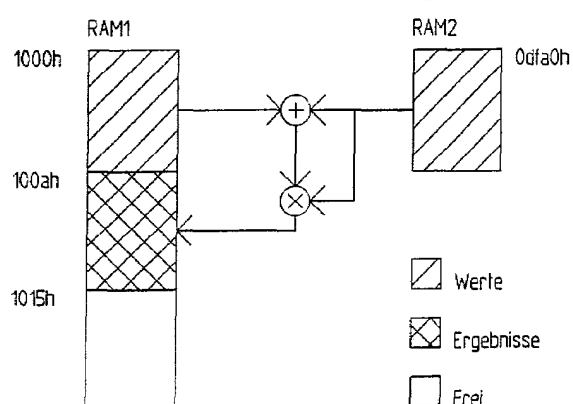
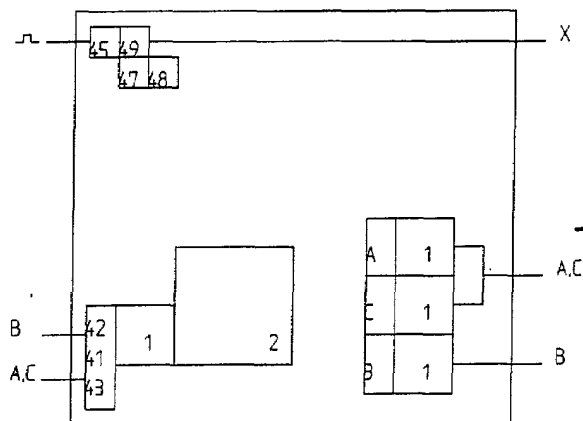
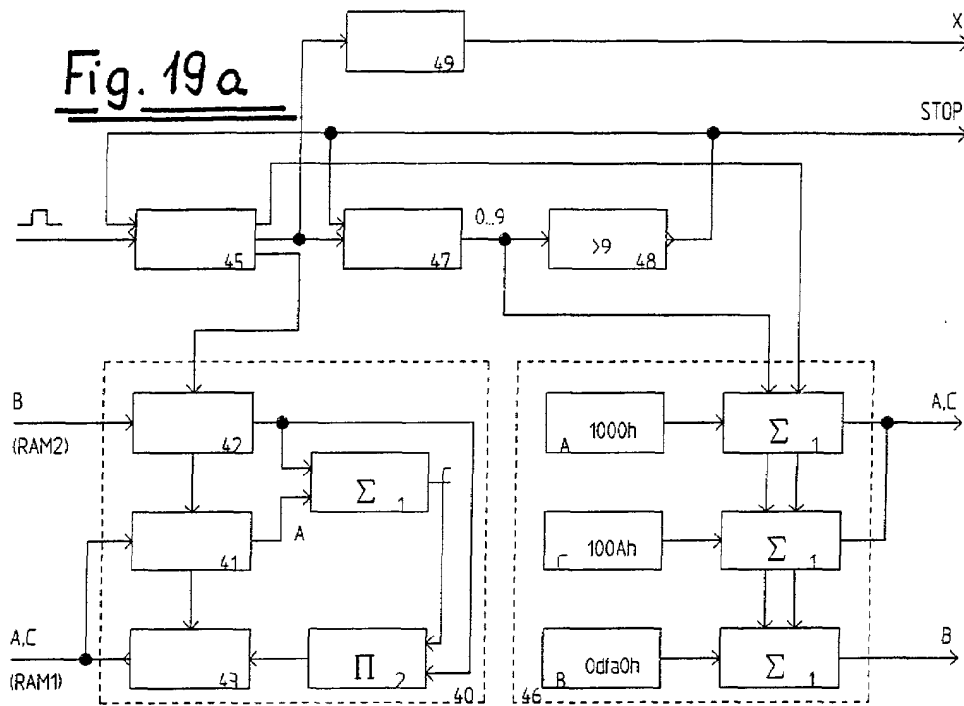


Fig. 18c

408 046/623



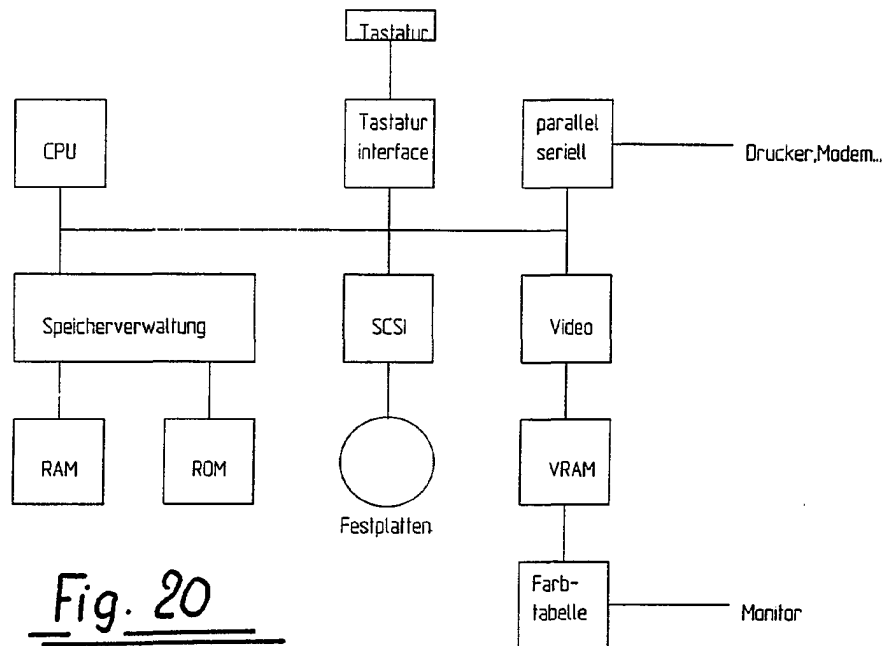


Fig. 20

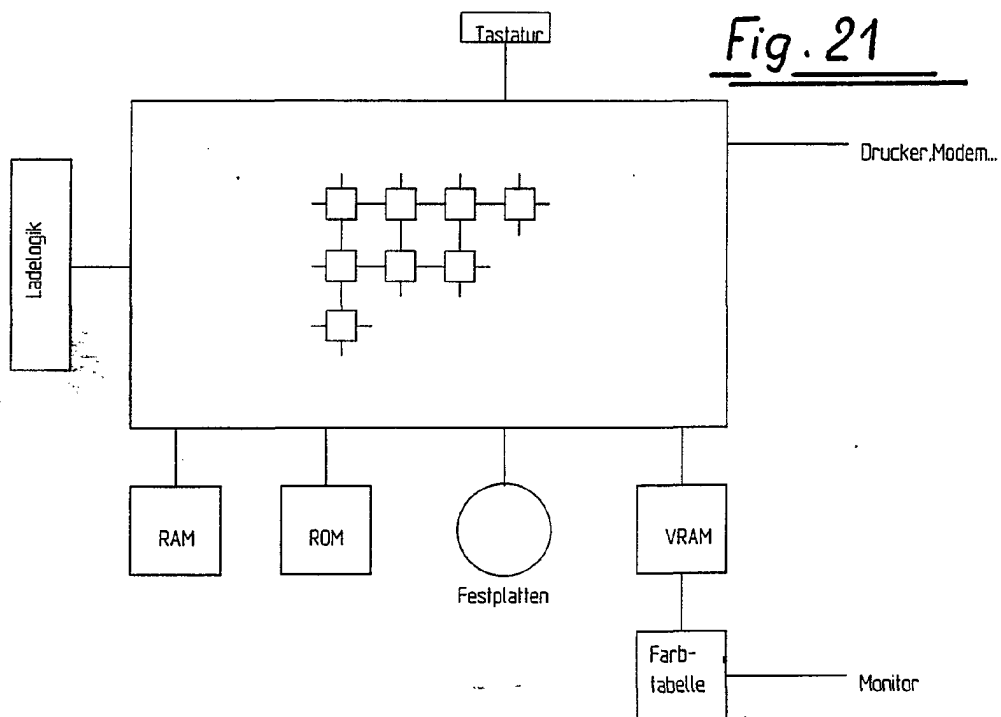
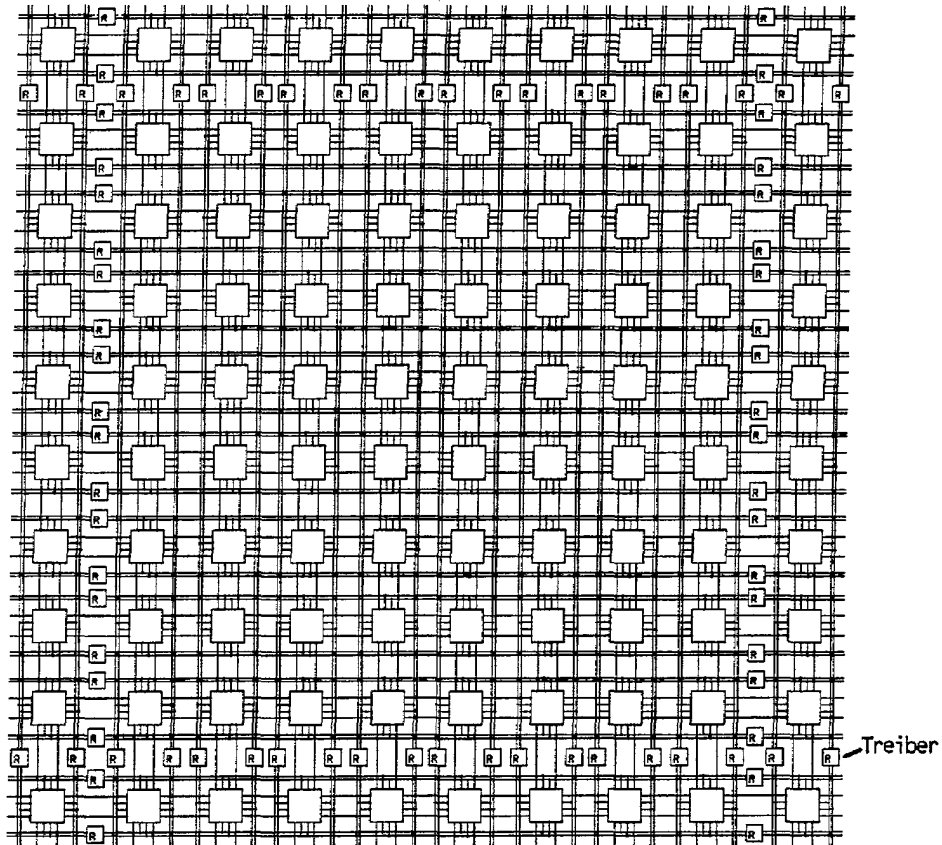


Fig. 21

Fig. 22





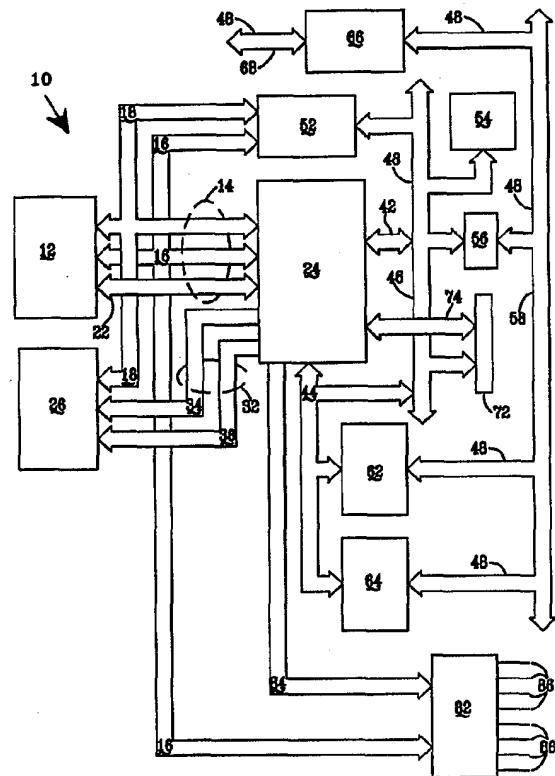
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(21) International Application Number: PCT/US94/04241 (22) International Filing Date: 18 April 1994 (18.04.94) (71) Applicant (for all designated States except US): GREEN LOGIC INC. [US/US]; 189 N. Bernardo Avenue, Mountain View, CA 94043 (US). (72) Inventor; and (75) Inventor/Applicant (for US only): DU, Shyun, Dii [-/US]; 1055 Loma Verde Avenue, Palo Alto, CA 94303 (US). (74) Agent: SCHREIBER, Donald, E.; Donald E. Schreiber, P.O. Box 64150, Sunnyvale, CA 94088-4150 (US).		(81) Designated States: CA, JP, KR, US, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE). Published With international search report.

(54) Title: AN IMPROVED SYSTEM LOGIC CONTROLLER FOR DIGITAL COMPUTERS

(57) Abstract

The present invention is a system logic controller ("SLC") (24) specially adapted for reducing and regulating a personal computer's ("PC's") (10) electrical power consumption. The PC (10) includes a CPU (12) and a direct port access buffer (82) between which the SLC (24) exchanges data that regulates the PC's power consumption. The SLC (24) reduces power consumption by low-power timed interval interrupt generators (142a, 142b through 142n). If the PC (10) enters a low-power "suspend" operating mode in which the CPU (12) is turned off, the SLC (24) permits quickly resuming normal operation. If the PC (10) incorporating the improved SLC (24) includes a super I/O chip (54) and/or PCMCIA sockets (72), the SLC (24) permits higher speed operation both of a hard disk connected to the super I/O chip (54), and/or of high speed PCMCIA cards. Furthermore, the SLC (24) prevents the application of an excessively high voltage to PCMCIA cards if the PC enters its "suspend" operating mode.



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AN IMPROVED SYSTEM LOGIC CONTROLLER FOR DIGITAL COMPUTERSTechnical Field

The present invention relates generally to the technical
5 field of digital computers and, more particularly, to an im-
proved, low-power system logic controller which provides facili-
ties that permit easily regulating a computer's electrical power
consumption, while concurrently permitting high performance.

10 Background Art

Present personal computers include an integrated circuit
("IC") central processing unit ("CPU") that is coupled by a high
speed CPU bus having both CPU address lines and CPU data lines
to various other ICs included in the computer. Such personal
15 computers conventionally also include a slower speed I/O bus for
exchanging signals with I/O cards that may be installed in the
computer. Between the high-speed CPU bus and the slower-speed
I/O bus these computers generally incorporate a system logic
controller ("SLC") IC which performs various functions essential
20 to the computer's operation including interfacing between the
high-speed CPU bus and the slower speed I/O bus. More specifi-
cally, in the instance of IBM Personal Computers and clone
personal computers which utilize Intel X86 IC microprocessors,
the high-speed bus may be called a VESA Local Bus ("VLB"), and
25 the slower speed I/O bus is generally either an Industry Standard
Architecture ("ISA") bus or an Extended Industry Standard
Architecture ("EISA") bus.

A system logic controller included in such a personal
computer is coupled to the CPU address lines, CPU data lines, and
30 CPU control lines included in the VLB, and to analogous signal
lines in the I/O bus. Accordingly, the system logic controller
includes a CPU interface controller for exchanging signals with
the CPU bus. Usually, the system logic controller also includes
a DRAM controller for generating RAS and CAS signals which are
35 required to access dynamic random access memory ("DRAM") included
in the computer, and for periodically refreshing the data stored
in the DRAM. The system logic controller also includes an I/O
bus controller which exchanges with I/O cards signals that are

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required to effect data transfers between an I/O device and the system logic controller and/or the DRAM. A system logic controller also includes a peripheral controller which performs a variety of functions also required to effect data transfers

5 between the system logic controller and/or DRAM and I/O devices such as hard and floppy disk drives. The functions performed by the peripheral controller include receiving and storing interrupts, and effecting direct memory access ("DMA") data transfers between I/O devices and the DRAM. The peripheral controller also

10 includes a clock into which the current date and time are stored when the computer is initialized, and by which the computer subsequently keeps time. The peripheral controller included in the system logic controller IC also includes counters which provides timing signals required for the DRAM controller's

15 periodic refreshing of data stored in the DRAM. Frequently, a system logic controller also includes a battery powered, real-time clock which the personal computer reads upon initialization, i.e. "booting", in order to obtain the date and the time which is then stored into the clock within the peripheral controller.

20 A book entitled "Intel's SL Architecture, Designing Portable Application" by Desmond Yuen, copyright 1993 by McGraw-Hill, Inc., which is hereby incorporated by reference, provides a more thorough and detailed description of various facilities provided by and the various operation performed by a system logic controller.

25 ler.

The traditional way of monitoring a number of different timed events in a digital computer is to assign a different timer for timing each different event. For example, one timer is assigned for timing keyboard events, a second timer is assigned

30 for timing parallel port events, a third timer is assigned for timing display events, etc. In such a computer system, each separate timer begins counting upon being enabled by a computer program's execution. When the count in the timer reaches a preset value, the timer generates an interrupt which notifies the

35 computer program that some type of timed event needs to be serviced. For example, a timed event may turn off a portion of a battery powered computer to conserve electrical power. The disadvantage of this scheme is that as many timers are required

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as there are different events to be timed. Since, comparatively speaking, a timer consumes a significant amount of electrical power, every additional timer increases the computer's power consumption merely for counting an interval of time. The amount
5 of power consumed by timers becomes substantial as the number of timed events increases.

To facilitate controlling power consumption in portable personal computers, Intel's 386 SL and 486 SL Enhanced IC microprocessors provide a System Management Mode ("SMM") of
10 operation. SMM in these microprocessors provides a separate environment for the execution of power management routines that is completely independent of the environment in which the operating system and application programs execute. For such microprocessors, a special system management interrupt ("SMI")
15 activates the SMM environment. When an SMI interrupt occurs, the microprocessor pauses execution of the current program, saves the internal data and states of the CPU to a preestablished memory location, e.g. 3000:0000h to 3000:FFFFh, enters SMM, and begins executing SMI routines stored in a dedicated system management
20 random access memory ("SMRAM"). For Intel's 386 SL and 486 SL microprocessors, power management routines executed in SMM in response to specific SMIs may cause the personal computer to enter a "Suspend" mode of operation in which the computer consumes a lesser amount of electrical power because certain
25 parts of the personal computer are turned off, e.g. the display and any backlighting for the display, the hard disk, the modem, etc. Subsequently, the microprocessor's execution of a resume operation restores power to, and thereby once again fully activates, the personal computer. In a particular "Suspend" mode
30 of operation in which the CPU receives no electrical power, restoring the application program that was executing prior to commencing the "Suspend" operating mode is delayed until a hard disk drive included in the computer becomes fully operational, and data essential to resuming application program execution has
35 been read from the hard disk.

There presently exist two different classes of IDE hard drives used in personal computers, those which are designed only to operate on the slower ISA Bus, and those which are designed

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to operate on the faster speed VLB. Present notebook computers frequently employ a single super I/O IC chip which provides electronic circuits for a serial port, a parallel port, a floppy disk controller, and an interface for an IDE hard disk drive. However, since such super I/O IC chips connect to the slower ISA bus, an IDE hard disk drive connected to the super I/O IC chip operates only at the slower ISA speeds, and cannot operate at the faster VLB speeds.

In addition to incorporating super I/O chips, present notebook computers frequently offer a Personal Computer Memory Card International Association ("PCMCIA") socket for receiving various different types of peripheral devices, e.g., modems, hard disk drives, "Flash" random access memory ("RAM") cards, etc. PCMCIA cards may operate at either five (5) volts or at three (3) volts. Each such PCMCIA card includes a Card Detect ("CD") pin and a 3V/5V pin. The CD pin permits a computer to detect insertion of a PCMCIA card into a PCMCIA socket. Upon insertion of a PCMCIA card into a computer's PCMCIA socket, a PCMCIA controller immediately interrogates the card's 3V/5V pin to determine whether the PCMCIA card being inserted operates at either 3 volts or 5 volts, and then provides the proper voltage to the PCMCIA card. However, if a notebook computer begins operating in its low power Suspend mode as described above, its PCMCIA controller is disabled. Consequently, if after the computer begins operating in Suspend mode the PCMCIA card is changed from a 5 volt card to a 3 volt card, the computer cannot sense this change. Under such circumstances, when the computer resumes operating in its higher power mode it will apply 5 volts, rather than the proper 3 volts, to the PCMCIA card. If 5 volt electrical power is applied to a 3 volt PCMCIA card, it is almost certain that the PCMCIA card will permanently be damaged. Since PCMCIA cards are comparatively expensive, e.g. \$250.00 for a modem which plugs into a PCMCIA socket, owners of PCMCIA cards can lose a significant financial investment if an excessively high voltage is applied to their PCMCIA card. Moreover, conventional PCMCIA controllers connect to the slower ISA Bus rather than the faster VLB. Consequently, the operating speed of any PCMCIA card plugged into a PCMCIA socket is limited to

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that of the ISA bus. However some of the devices, e.g. ROM or Flash memory, that are presently being incorporated into PCMCIA cards are capable of operating at the higher speed of the VLB.

Presently, manufacturers of personal computers are experiencing a continuing need to reduce electrical power consumption both for desk top computers and for notebook computers. Moreover, manufacturers are also experiencing a continuing demand for low-power notebook computers that provide performance equalling that of desktop computers. Since it is essential that any system logic controller capable of providing such improvements remain compatible with existing computer programs, the facilities which a system logic controller provides for managing the computer's electrical power consumption while concurrently facilitating construction of higher performance computers must remain compatible with facilities already present in contemporary personal computers, while at the same time solving technical problems which personal computer manufacturers encounter.

Disclosure of Invention

The present invention provides an improved system logic controller having facilities that permit easily controlling a computer's electrical power consumption, while at the same time permitting assembly of higher performance computers.

An object of the present invention is to provide an easy way to access a direct port access buffer which stores data that regulates a computer's electrical power consumption.

Another object of the present invention is to provide a system logic controller integrated circuit chip having as few pins as practical.

Another object of the present invention is to provide a system logic controller which permits assembling both a simpler and a more compact personal computer, while concurrently reducing the computer's manufacturing cost.

Another object of the present invention is to provide a system logic chip having low power consumption in those circuits which are necessary for effectively and efficiently regulating the computer's electrical power consumption.

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Another object of the present invention is to provide a Suspend mode of operation for the personal computer which consumes a small amount of power while swiftly resuming full operation.

5 Another object of the present invention is to facilitate construction of a notebook computer capable of high performance.

Another object of the present invention is to provide an interface to PCMCIA cards which under all circumstances prevents application of an excessively high voltage to the PCMCIA card.

10 Yet another object of the present invention is to provide a system logic controller that facilitates assembly of an energy efficient personal computer offering high performance.

Briefly the preferred embodiment of the present invention is a digital computer which includes an improved system logic
15 controller having an electrical power management unit. The power management unit generates a variety of different power management signals used in regulating electrical power consumed by the personal computer. To regulate electrical power consumption, the personal computer includes a direct port access buffer and the
20 power management unit includes a direct port access controller for supplying direct port access control signals to the direct port access buffer. Signals supplied to the direct port access buffer by the direct port access controller cause power management data to be stored into or read from the direct port access
25 buffer.

To effect a transfer of power management data between the personal computer's microprocessor and the direct port access buffer, upon receiving an I/O command from the microprocessor central processing unit ("CPU") that specifies an I/O operation
30 between the CPU and the direct port access buffer, the system logic controller transmits a hold control signal to the CPU which requests that the CPU halt operation. In response to this halt request, the CPU halts operation and tristates all the CPU address lines. After the CPU has tristated all the CPU address
35 lines, the direct port access controller transmits a direct port access control signal to the direct port access buffer which causes an exchange of data between the direct port access buffer and the system logic controller over the CPU address lines.

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After the power management data has been exchanged between the direct port access buffer and the system logic controller, the system logic controller transmits a signal to the CPU which causes the CPU to resume operating.

5 To provide low-power generation of timed interrupts which activate execution of power management routines by the CPU, the system logic controller includes a plurality of power management unit comparators each one of which respectively generates an independent power management timed interrupt. All of these power
10 management unit comparators simultaneously receive the same timing signals generated by a single continuously running master clock which can be read by a computer program executed by the CPU. Furthermore, each of the power management unit comparators also includes a time data storage register into which the CPU may
15 store time data representing a specific moment in time at which the power management unit comparator is to generate a power management timed interrupt. To generate the various power management interrupts at the proper times, each power management unit comparator continuously compares the timing signals which
20 it receives from the master clock with the time data stored in the time data storage register, and generates a power management timed interrupt when the stored time data equals the timing signals.

A system logic controller in accordance with the present
25 invention is also coupled to DRAM address lines, and the personal computer also includes DRAM that is coupled to the CPU data lines and to the DRAM address lines. In response to an initial SMI that specifies a particular Suspend mode of operation, the system logic controller provides a memory address to a first physical
30 memory SMI data storage area in the DRAM for storage of all CPU internal data and states. After the CPU internal data and states have been stored into the first physical memory SMI data storage area, the system logic controller requests that the CPU execute a power management routine which first disables the first
35 physical memory SMI data storage area so data cannot be stored into that area of the DRAM. The power management routine then establish a memory address to a second physical memory SMI data storage area into which CPU internal data and states will be

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stored in response to a subsequent system management interrupt. Finally, the power management routine preserves within the system logic controller SMI state information indicating that the system logic controller has caused the CPU internal data and states to
5 be stored into the first physical memory SMI data storage area, and that the second physical memory SMI data storage area has been established for storage of CPU internal data and states in response to a subsequent system management interrupt. The system logic controller then places the personal computer in a power
10 Suspend mode of operation in which it removes electrical power from the CPU while continuing to supply electrical power to the DRAM, and continuing to refresh the DRAM while awaiting an occurrence of a resume event. In response to a resume event, the system logic controller restores electrical power to the CPU, and
15 resumes execution of the power management routine which detects the SMI state information preserved in the system logic controller. When the power management routine detects that SMI state information has been preserved in the system logic controller, it directs the system logic controller to generate a fake SMI to
20 the CPU which causes the then existing CPU internal data and states to be stored into the second physical memory SMI data storage area, and initiates execution of the SMI routine. After the CPU internal data and states have been stored into the second physical memory SMI data storage area and upon the power
25 management routine's detection that SMI state information has been preserved within the system logic controller, the power management routine disables the second physical memory SMI data storage area so data cannot be stored into or retrieved from that area of the DRAM. The power management routine then reestablish-
30 es the memory address to the first physical memory SMI data storage area into which CPU internal data and states were stored in response to the initial system management interrupt. The Suspend mode of operation is then terminated immediately after which continued execution of the power management routine
35 restores the CPU internal data and states to that previously stored into the first physical memory SMI data storage area.

If the personal computer incorporating the improved system logic controller in accordance with the present invention

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includes a super I/O chip, the I/O bus includes a first section over which the system logic controller and super I/O chip exchange signals, and a second section over which the system logic controller exchanges signals with I/O cards that may be included in the personal computer. A bidirectional I/O bus section isolation buffer, located between the first and second sections of the I/O bus, selectively isolates the second section of the I/O bus from the first section in response to an I/O bus isolation control signal generated by the system logic controller. The system logic controller includes a hard disk access detection circuit for detecting I/O accesses to the super I/O chip's hard disk drive interface, and for transmitting the I/O bus isolation control signal to the I/O bus section isolation buffer. In response to the I/O bus isolation control signal, during access to the hard disk drive interface the I/O bus section isolation buffer isolates the second section of the I/O bus from the first section of the I/O bus. Thus, while the I/O bus section isolation buffer isolates the second section of the I/O bus from the first section, the system logic controller exchanges signals via the I/O bus with the super I/O chip at a faster speed so the personal computer may use a high speed rather than a slow speed IDE hard disk drive.

The improved system logic controller in accordance with the present invention includes a PCMCIA controller for exchanging data with a PCMCIA card inserted into a PCMCIA socket included in the personal computer. During normal operation of the personal computer, the power management unit included in the system logic controller generates power management signals which turn off the PCMCIA controller to reduce electrical power consumption, and subsequently generates power management signals which turn on the PCMCIA controller. These power management signals include a PCMCIA power restoration control signal transmitted from the power management unit to the PCMCIA controller which within the PCMCIA controller simulates an occurrence of the CD signal. Thus, every time the power management unit restores power to the PCMCIA controller, the PCMCIA controller determines if any PCMCIA card then present in the PCMCIA socket operates at the first lower voltage or at the

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second higher voltage. Furthermore, the improved system logic controller permits the PCMCIA controller to operate either at the speed of the I/O bus, e.g. ISA bus speed, or at a higher speed which can approach that of the CPU bus, e.g. the VLB speed.

5 These and other features, objects and advantages will be understood or apparent to those of ordinary skill in the art from the following detailed description of the preferred embodiment as illustrated in the various drawing figures.

10 Brief Description of Drawings

FIG. 1 is a functional block diagram depicting a digital computer that incorporates a system logic controller in accordance with the present invention, and which illustrates PCMCIA sockets preferably included in such a digital computer;

15 FIG. 2 is a functional block diagram depicting various functional units included in the system logic controller illustrated in FIG. 1 including a power management unit;

FIG. 3 is a functional block diagram illustrating several timed interrupt generators included in the power management unit
20 illustrated in FIG. 2; and

FIG. 4 is a functional block diagram depicting PCMCIA sockets illustrated in FIG. 1.

Best Mode for Carrying Out the Invention

25 FIG. 1 is a functional block diagram depicting a digital computer identified by the general reference character 10. The computer 10 includes an IC CPU 12 that is coupled to a high speed CPU bus 14, e.g. a VLB, having both CPU address lines 16 and CPU data lines 18. The CPU bus 14, which also includes CPU control
30 signal lines 22, couples the CPU 12 to a IC system logic controller 24. The CPU address lines 16 of the CPU bus 14 also couple the CPU 12 to a DRAM 26. A DRAM address and control bus 32, which includes both DRAM address lines 34 and DRAM control signal lines 36, couples the system logic controller 24 to the
35 DRAM 26.

I/O bus data lines 42 and I/O bus control signal lines 44 couple the system logic controller 24 to a first section 46 of an I/O bus 48, e.g. an ISA bus. A buffer 52 included in the

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computer 10 couples signals directly between the CPU address lines 16 and CPU data lines 18 of the CPU bus 14 and the first section 46 of the I/O bus 48. A single IC super I/O chip 54, which provides electronic circuits for a serial port, a parallel port, a floppy disk controller, and an interface for an IDE hard disk drive (none of which are illustrated in FIG. 1), is also coupled to the first section 46 of the I/O bus 48. A bidirectional I/O bus section isolation buffer 56 couples the first section 46 of the I/O bus 48 to a second section 58 of the I/O bus 48 to which I/O cards (not illustrated in FIG. 1) may be coupled. The I/O bus control signal lines 44 also couple the system logic controller 24 to an IC keyboard controller 62 and to an IC read only memory ("ROM") BIOS 64. The keyboard controller 62 and the ROM BIOS 64 are also coupled to the second section 58 of the I/O bus 48.

To reduce electrical power consumption within the computer 10, those circuits within the system logic controller 24 which do not interface directly with the I/O bus data lines 42 and the I/O bus control signal lines 44 of the I/O bus 48 operate with only three (3) volts of electrical power. Conversely, those circuits within the system logic controller 24 which interface directly with the I/O bus data lines 42 and the I/O bus control signal lines 44 of the I/O bus 48 operate with five (5) volts of electrical power. To permit achieving an even greater reduction in electrical power consumption, the computer 10 preferably includes a 3V/5V buffer 66 that is coupled between the second section 58 of the I/O bus 48 and a 3V extension 68 of the I/O bus 48.

The computer 10 also includes PCMCIA sockets 72 that are coupled to the system logic controller 24 by the first section 46 of the I/O bus 48, and by a PCMCIA control signal bus 74.

To facilitate regulation of electrical power consumption by a computer program executed by the CPU 12, the computer 10 includes a direct port access buffer 82 that is coupled to the system logic controller 24 by the CPU address lines 16 of the CPU bus 14, and by direct port access control signal lines 84. A plurality of electrical power control signal lines 86 couple the direct port access buffer 82 to various other units of the

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computer 10 such as a display and any backlighting for the display, a hard disk, a floppy disk, a modem, etc. By storing appropriate data into the direct port access buffer 82, a computer program executed by the CPU 12 may turn such units of
5 the computer 10 on or off thereby regulating electrical power consumption by the computer 10.

Referring now to the block diagram of FIG. 2 which illustrates various functional units included in the system logic controller 24, the system logic controller 24 includes a CPU
10 interface controller 102 that is coupled to the CPU address lines 16, to the CPU data lines 18, and to the CPU control signal lines 22 of the CPU bus 14. The system logic controller 24 also includes a DRAM controller 104 that is coupled to the DRAM address lines 34 and to the DRAM control signal lines 36. The
15 I/O bus control signal lines 44 are coupled to an ISA bus controller 106 included in the system logic controller 24, while the I/O bus data lines 42 are coupled to a ISA bus address/data buffer 108. The system logic controller 24 includes a peripheral controller 112, and preferably includes a real-time clock 118 in
20 accordance with the descriptions set forth herein above. A PCMCIA controller 122 included in the system logic controller 24 is coupled to the PCMCIA control signal bus 74, while a direct port access controller 126 included in a power management unit 128 of the system logic controller 24 is coupled to the direct
25 port access control signal lines 84.

Within the system logic controller 24, SLC data lines 132 and SLC address lines 134 couple signals between the CPU interface controller 102 and the ISA bus address/data buffer 108, while SLC control lines 136 couple signals between the CPU
30 interface controller 102 and the ISA bus controller 106. The SLC address lines 134 couple signals from the CPU interface controller 102 to the DRAM controller 104, while the SLC data lines 132 couple signals between the CPU interface controller 102 and both the real-time clock 118 and the peripheral controller 112. Thus,
35 for example, the CPU 12 may read the date and time from the real-time clock 118 and then store them into memory locations within the DRAM 26. Analogously, via the SLC data lines 132 and the SLC control lines 136, the peripheral controller 112 may

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periodically increment the contents of the memory location in the DRAM 26 into which the time data has been stored. The SLC control lines 136 also couple signals between the CPU interface controller 102 and the peripheral controller 112 to permit transmission of interrupts from the peripheral controller 112 to the CPU 12, and to permit the computer program executed by the CPU 12 to control the operation of the peripheral controller 112. Periodically, the peripheral controller 112 transmits a timing signal to the DRAM controller 104 over a DRAM refresh timing signal line 138 which causes the DRAM controller 104 to refresh data stored in the DRAM 26. The SLC control lines 136 and the SLC data lines 132 couple signals between the CPU interface controller 102 and the power management unit 128 including the direct port access controller 126. The SLC control lines 136 couple control signals between the CPU interface controller 102 and the PCMCIA controller 122 as does an extension of the I/O bus control signal lines 44 that is located within the system logic controller 24.

20 Direct Port Access

The power management unit 128 included in the system logic controller 24 provides a variety of functions which facilitate power reduction within the computer 10. For example, in addition to other features disclosed in greater detail herein, the power management unit 128 supports CPU clock modulation, detects if the CPU bus is idle, includes an analog-to-digital converter for monitoring battery voltage in a battery powered computer 10, and shadows write only registers. Specifically with regard to the direct port access buffer 82, the power management unit 128 provides a cost-effective method by which a computer program executed by the CPU 12 may store non time-critical power regulation data into or read non time-critical power regulation data from the direct port access buffer 82.

To store non time-critical power regulation data into the direct port access buffer 82, I/O Management Software ("IMS") for the direct port access buffer 82 executed by the CPU 12 transmits to the system logic controller 24 via the CPU bus 14 a write command for the address of the direct port access buffer 82. The

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system logic controller 24 receives the write command from the CPU 12, and latches the data value present on the CPU data lines 18 into a register within the system logic controller 24 (Not illustrated in FIG. 2.). The system logic controller 24 then asserts a HOLD control signal transmitted from the system logic controller 24 to the CPU 12 thereby requesting that the CPU 12 suspend its operation. After the CPU 12 suspends its operation, the CPU 12 transmits a HLDA (Hold Acknowledge) signal back to the system logic controller 24. Furthermore, concurrently with transmitting HLDA to the system logic controller 24, the CPU 12 tristates the CPU address lines 16. Upon receiving the HLDA signal, the system logic controller 24 then takes over the CPU address lines 16 to send the data from the register in the system logic controller 24 over the CPU address lines 16 to the direct port access buffer 82. To store the data from the system logic controller 24 into the direct port access buffer 82, the direct port access controller 126 first transmits a signal via the direct port access control signal lines 84 to the direct port access buffer 82 which cause the direct port access buffer 82 to receive the data from the CPU address lines 16. After the direct port access buffer 82 receives the data, the direct port access controller 126 transmits a pulse via the direct port access control signal lines 84 to the direct port access buffer 82 which causes the data on the CPU address lines 16 to be loaded into a register (Not separately depicted in FIG. 1) in the direct port access buffer 82 from which such data is transmitted via the electrical power control signal lines 86 to other units in the computer 10. After the data has been thus stored into the direct port access control signal lines 84, the system logic controller 24 removes the data from the CPU address lines 16 and negates the HOLD signal to the CPU 12 which then resumes operating.

To retrieve non time-critical power regulation data from the direct port access buffer 82, IMS for the direct port access buffer 82 executed by the CPU 12 transmits to the system logic controller 24 via the CPU bus 14 a read command for the address of the direct port access buffer 82. Upon receiving the read command from the CPU 12, the system logic controller 24 immediately asserts an AHOLD control signal transmitted from the system

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logic controller 24 to the CPU 12. Upon receiving the AHOLD signal, the CPU 12 immediately suspends the current CPU cycle, and tristates the CPU address lines 16. The system logic controller 24 then takes over the CPU address lines 16 so it may
5 read from the direct port access buffer 82. To retrieve data from the direct port access buffer 82 to the system logic controller 24, the direct port access controller 126 transmits control signals to the direct port access buffer 82 via the direct port access control signal lines 84 which cause the direct
10 port access buffer 82 to place the data present in the direct port access buffer 82 onto the CPU address lines 16. The system logic controller 24 then reads the data from the CPU address lines 16 and latches the data into a register within the system logic controller 24 (Not illustrated in FIG. 2.). The system
15 logic controller 24 then transmits control signals to the direct port access buffer 82 via the direct port access control signal lines 84 which cause the direct port access buffer 82 to disconnect from the CPU address lines 16. The system logic controller 24 then negates AHOLD, and at the same time places the
20 data that has been stored in the register onto the CPU data lines 18 from which it will be read by the CPU 12. The system logic controller 24 then transmits a READY control signal to the CPU 12 thereby causing the CPU 12 to read the data from the CPU data lines 18. The CPU 12 then finishes the current cycle for the CPU
25 bus 14, and resumes operating.

The direct port access buffer 82 of the present invention exchanges data with the system logic controller 24 over the CPU address lines 16 rather than the CPU data lines 18 of the CPU bus 14 to avoid placing any additional electrical load on the CPU
30 data lines 18. Because the CPU data lines 18 carry high speed signals particularly between the CPU 12 and the DRAM 26, any additional electrical load resulting from an extension of the CPU data lines 18 to the direct port access buffer 82 could increase the difficulty of designing the computer 10. Conversely, signals
35 present on the CPU address lines 16 are not as sensitive to additional electrical loading as those on the CPU data lines 18. Therefore, by using the CPU address lines 16 for exchanging data between the system logic controller 24 and the direct port access

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buffer 82, the system logic controller 24 eases the difficulty of designing the computer 10. By using the CPU address lines 16 for exchanging data with the direct port access buffer 82, the system logic controller 24 also avoids increasing the number of pins on its IC package.

Low Power Timed Interval Interrupt Generators

The power management unit 128 included in the system logic controller 24 is capable of generating a number of independently timed interrupts that may be used in regulating electrical power consumption by the computer 10. FIG. 3 is a block diagram depicting several timed interval interrupt generators 142a, 142b thru 142n in accordance with the present invention. Each of the timed interval interrupt generators 142a, 142b thru 142n receives timing signals from a continuously running master clock 144 via a timing signal lines 146. The master clock 144 has a comparatively long interval, e.g. one hour or longer, and a computer program executed by the 12 may read the timing signals that are present on the timing signal lines 146 via the SLC data lines 132 included in the system logic controller 24. In addition to receiving timing signals from the master clock 144, each of the timed interval interrupt generators 142a, 142b thru 142n includes a timed interrupt output signal lines 148a, 148b thru 148n over which the timed interrupt generator 142a, 142b ... 142n may transmit an interrupt to the CPU 12.

Within each of the timed interval interrupt generators 142a, 142b thru 142n, the timing signals present on the timing signal lines 146 are supplied to a first input of a timed event comparator 152. An output of each timed event comparator 152 is coupled to the timed interrupt output signal line 148a, 148b ... 148n of the timed interrupt generator 142a, 142b ... 142n to which the timed event comparator 152 belongs. Each of the timed interval interrupt generators 142a, 142b thru 142n also includes an interrupt time register 154 into which a computer program executed by the CPU 12 may store a numerical value via the SLC data lines 132 included in the system logic controller 24. In particular, the computer program executed by the CPU 12 stores a numerical value into the interrupt time register 154 which

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represents an instant in time at which the timed interrupt generator 142a, 142b ... 142n is to generate an interrupt. Each interrupt time register 154 supplies the numerical value which it holds to a second input of the timed event comparator 152 with which the interrupt time register 154 is associated. Each timed event comparator 152 continuously compares the number which it receives from its associated interrupt time register 154 with the timing signals that it receives from the master clock 144 via the timing signal lines 146. If the numerical value which the timed event comparator 152 receives from the interrupt time register 154 equals the timing signals that the timed event comparator 152 receives from the master clock 144, then the timed event comparator 152 transmits an interrupt signal on the timed interrupt output signal line 148a, 148b ... 148n to which it is coupled.

To set the instant at which one of the timed interval interrupt generators 142a, 142b thru 142n is to generate an interrupt, a computer program executed by the CPU 12 first reads the timing signals present on the timing signal lines 146 and adds to that time value the duration of a timed interval after which an interrupt is to occur. The computer program executed by the CPU 12 then stores the number thus computed into the appropriate interrupt time register 154 in a particular timed interrupt generator 142a, 142b ... 142n. When the timing signals from the master clock 144 equal the numerical value stored in the interrupt time register 154, the timed interrupt generator 142a, 142b ... 142n generates an interrupt which ultimately arrives at the CPU 12.

For example, if it were necessary to concurrently monitor both a hard disk drive and a parallel port in the manner summarized in the following table, then the sequence of operations set forth below performs that monitoring function.

Sequence	Hard Disk	Parallel Port	Comment
Start1	00:15	00:15	
End1	00:45	00:50	Service
Start2	00:46	Done	
End2	00:26 (Rippled)		Service

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1. A timer service routine executed by the CPU 12 receives a request to monitor both the hard disk and the parallel port to determine if any hard disk events occur during the next 30 minutes, or any parallel port events occur during the next 35 minutes.
2. The timer service routine executed by the CPU 12 first reads the master clock 144 which in the preceding example generates timing signals representing the time 00:15.
3. The timer service routine then:
 - a. adds 30 minutes to the numerical value which it read from the master clock 144 to compute the instant at which a hard disk drive interrupt will occur, which in the preceding example is 00:45, and stores this numerical value into the interrupt time register 154 for a particular timed interrupt generator 142a, 142b ... 142n; and
 - b. adds 35 minutes to the numerical value which it read from the master clock 144 to compute the instant at which a parallel port interrupt will occur, which in the preceding example is 00:50, and stores this numerical value into the interrupt time register 154 for a different timed interrupt generator 142a, 142b ... 142n.
4. The operating system executed by the CPU 12 then waits for an interrupt from the timed interval interrupt generators, e.g. 142a and 142b.
5. When the numerical value of the timing signals transmitted from the master clock 144 reach 00:45, the timed event comparator 152 receiving that numerical value from its associated interrupt time register 154 generates a hard disk interrupt that is transmitted to the CPU 12.
6. Upon receiving the hard disk interrupt, the operating system calls a hard disk interrupt service routine to service the interrupt.
7. During execution of the hard disk interrupt service routine, that routine calls the timer service routine to set a 40 minute interval for the next hard disk interrupt.

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8. The timer service routine again reads the master clock 144 which is presently generating a numerical value representing the time 00:46.
 9. The timer service routine adds 40 minutes to the numerical value read from the master clock 144 to compute the value 01:26, and then stores the value 00:26 into the interrupt time register 154 of the timed interrupt generator 142a, 142b ... 142n that is generating timed interrupts for the hard disk. The value 00:26 is stored into that interrupt time register 154 rather than the value 01:26 because in this example the period of the master clock 144 is only one hour long.
 10. The operating system then resumes waiting for the next interrupt from the timed interrupt generator 142a, 142b ... 142n.
 11. When the numerical value generated by the master clock 144 reaches 00:50, the timed event comparator 152 receiving that numerical value from its associated interrupt time register 154 generates a parallel port interrupt that is transmitted to the CPU 12.
 12. Upon receiving the parallel port interrupt, the operating system calls a parallel port interrupt service routine to service the interrupt.
 13. When the numerical value generated by the master clock 144 reaches 00:26, the timed event comparator 152 receiving that numerical value from its associated interrupt time register 154 generates a second hard disk interrupt that is transmitted to the CPU 12.
- 30 The timed interval interrupt generators 142a, 142b thru 142n as described above that are included in the system logic controller 24 consume a lesser amount of electrical power than an equal number of independent timers because a CMOS IC consumes electrical power in proportion to the number of circuits which change state (i.e. change from a 0 to a 1 or from a 1 to a 0) during some interval of time. Conversely, a modern CMOS IC maintaining a state consumes virtually no power. If separate timers were used for each event, then because each timer must

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continuously keep incrementing in order to keep time, each timer continuously consumes power. Conversely, in the present invention each of the timed interval interrupt generators 142a, 142b thru 142n consumes electrical power only when the timer service routine stores a numerical value into the interrupt time register 154, and when the timed event comparator 152 generates an interrupt because it detects coincidence between the numerical value that it receives from the master clock 144 and from its associated interrupt time register 154. Accordingly, the timed interval interrupt generators 142a, 142b thru 142n significantly reduce electrical power consumption by a system logic controller 24 which is concurrently timing a number of different events.

To facilitate generating a succession of interrupts each of which are separated by the same duration in time from the immediately preceding and from the immediately succeeding interrupt, each of the timed interval interrupt generators 142a, 142b thru 142n preferably includes an interrupt interval register 156. Via the SLC data lines 132, a computer program executed by the CPU 12 may store a numerical value into the interrupt interval register 156 that represents a duration of time between successive interrupts. Each of the timed interval interrupt generators 142a, 142b thru 142n also preferably includes an adder 158 having a first input which receives the numerical value present in the interrupt interval register 156. The interrupt time register 154 in each of the timed interval interrupt generators 142a, 142b thru 142n supplies the numerical value which it holds to a second input of the adder 158. The adder 158 in each of the timed interval interrupt generators 142a, 142b thru 142n stores the result of any addition operation back into the interrupt time register 154 from which it receives a numerical value. Each timed event comparator 152 supplies its output signal as a trigger signal to the adder 158 included in the timed interval interrupt generators 142a, 142b thru 142n to which it belongs. Accordingly, when a time a timed event comparator 152 generates an interrupt, the adder 158 with which it is associated adds together the numerical values present both in the interrupt interval register 156 and in the interrupt time register 154, and then stores the result of that addition back into the interrupt

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time register 154. Thus, if the numerical value stored in the interrupt interval register 156 is greater than zero, the timed interrupt generator 142a, 142b ... 142n automatically generates a succession of interrupts each one of which follows the immediately preceding interrupt by a duration of time specified by the numerical value present in the interrupt interval register 156.

Two different methods may be employed with the timed interval interrupt generators 142a, 142b thru 142n for determining which of several timed interrupt generator 142a, 142b ... 142n generated an interrupt. The present invention is compatible with the traditional method employed with conventional multiple timer systems. In such a traditional system, the power management unit 128 includes a timed interrupts register 162 which receives the output signals from all of the timed interval interrupt generators 142a, 142b thru 142n via the timed interrupt output signal lines 148a, 148b thru 148n. With this alternative strategy for identifying the source of an interrupt, when a timed interrupt occurs, an interrupt service routine executed by the CPU 12 reads the state of all the timed interval interrupt generators 142a, 142b thru 142n from the timed interrupts register 162 via the SLC data lines 132 to determine which one of several timed interval interrupt generators 142a, 142b thru 142n generated an interrupt. Alternatively, a specific device to be serviced in response to a timed interrupt may be identified if the timer service routine also stores the numerical value present in each interrupt time register 154 into a table which correlates the numerical value of an interrupt time with a device to be serviced at the specified time. When an interrupt occurs, the interrupt service routine first reads the value from the master clock 144 and compares it with the time values stored by the timer service routine into the table, and then services the device whose interrupt time value matches the time value read from the master clock 144.

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Suspend Mode Operation

In addition to a normal full-power operating mode, the system logic controller 24 is capable of placing the computer 10 into any one of three successively lower power operating modes to conserve electrical power. In the first power conservation mode called "sleep mode," the system logic controller 24 blocks the transmission of clock signals to all of the computer 10 except to the peripheral controller 112, the DRAM controller 104, and the real-time clock 118 included in the system logic controller 24, and to the DRAM 26. In the next lower power consumption operating mode called "5V Suspend," the system logic controller 24 also turns off electrical power to all of the computer 10 except to the peripheral controller 112, the DRAM controller 104, and the real-time clock 118 included in the system logic controller 24, and to the DRAM 26. Thus, in the 5V Suspend operating mode, the CPU 12 and the PCMCIA controller 122 receive no electrical power, and therefore lose all information about the state of the computer 10 which existed immediately before power is turned off. In the lowest power consumption operating mode called "0V Suspend," the system logic controller 24 turns off everything in the computer 10 except the real-time clock 118 included in the system logic controller 24. A computer program executed by the CPU 12 causes the system logic controller 24 to place the computer 10 into one of these three power conservation operating modes in response to an appropriate SMI interrupt.

The system logic controller 24 in accordance with the present invention permits the operating system controlling the operation of the computer 10 to quickly resume operating after entering the 5V Suspend mode of operation in which electrical power is removed from the CPU 12. To permit quickly resuming operation of the computer 10, if a SMI interrupt occurs that specifies the 5V Suspend mode of operation, then the system logic controller 24 stores all CPU internal data and states to a first preestablished area in the DRAM 26, e.g. A000:XXXXh. After the CPU internal data and states have been stored into this first physical memory area, the system logic controller 24 transmits signals to the CPU

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12 which request that a power management routine ("PMR") executed by the CPU 12:

1. disable the first physical memory area so data will no longer be stored into that area of the DRAM 26; and
 - 5 2. establish an address to a second preestablished area in the DRAM 26, e.g. 3F000:XXXXh, into which the system logic controller 24 will store CPU internal data and states in response to a subsequent SMI that specifies a suspend mode of operation.
- 10 Then the PMR stores information, e.g. sets a single bit, in the system logic controller 24 which records the occurrence of the preceding change in physical memory areas. After the PMR has stored this SMI state information into the system logic controller 24, the system logic controller 24 through data stored into
- 15 the direct port access buffer 82 turns off electrical power to the CPU 12 and other units included in the computer 10 while continuing to supply electrical power to the peripheral controller 112, to the DRAM controller 104, to the real-time clock 118, and to the DRAM 26, and while continuing to refresh the DRAM 26
- 20 while awaiting the occurrence of a resume event, e.g. opening of a notebook computer case or typing on the keyboard of the computer 10.

Upon the occurrence of a resume event, the system logic controller 24 restores electrical power to the CPU 12 thereby

25 ultimately causing the CPU 12 to resume execution of the PMR. When the PMR which is executed in response to reapplying electrical power to the CPU 12 detects that the SMI state information has been stored in the system logic controller 24, that PMR then requests the system logic controller 24 to generate

30 a "fake" SMI to the CPU 12 that specifies a suspend mode of operation. This "fake" SMI causes the then existing internal data and states of the CPU 12 to be stored into the second preestablished area in the DRAM 26, e.g. 3F000:XXXXh. After the system logic controller 24 has stored the CPU internal data and

35 states into the second preestablished area in the DRAM 26 in response to the "fake" SMI, the PMR executed in response to the "fake" SMI detects that SMI state information has been preserved within the system logic controller 24. Upon detecting the SMI

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state information has been stored in the system logic controller 24, the PMR being executed by the CPU 12 in response to the "fake" SMI disables the second preestablished area in the DRAM 26, e.g. 3F000:XXXXh so data cannot be stored into or retrieved from that area, and the PMR then reestablishes the first preestablished area in the DRAM 26, e.g. A000:XXXXh, into which CPU internal data and states were stored in response to the initial SMI. Upon reestablishment of the first preestablished area in the DRAM 26, the system logic controller 24 terminates the 5V Suspend mode of operation immediately after which execution of the PMR by the CPU 12 restores the CPU internal data and states to that previously stored in the first preestablished area in the DRAM 26 in response to the initial SMI.

By permitting the establishment of the second area in the DRAM 26 for the storage of the CPU internal data and states in response to the "fake" SMI, the system logic controller 24 permits restoring the operating state of the CPU 12 with only a few computer program instruction in comparison with the many computer program instructions that must be executed to retrieve CPU internal data and states stored on a hard disk. Furthermore, the use of the second preestablished area for the storage of CPU internal data and states when resuming operation avoids any need to save the first CPU internal data and states to a hard disk. By eliminating any need to access a hard disk for saving and restoring the CPU internal data and states, the 5V Suspend mode of operation disclosed above permits operation of the CPU 12 to be restored more quickly, and consumes a lesser amount of electrical energy in saving and restoring the CPU internal data and states. Finally, the present invention avoids any possibility that there might be insufficient space available on the hard disk to store the initial CPU internal data and states.

High Speed IDE Hard Disk I/O

Referring now to FIG. 1, the system logic controller 24 of the present invention operates in conjunction with super I/O chip 54 to provide both an ISA bus speed interface to an IDE hard disk drive (Not depicted in any of the FIGs.), or a higher speed interface to the IDE hard disk drive which approaches the speed

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of the VLB. To provide the higher speed interface to an IDE hard disk drive, the system logic controller 24 monitors the I/O device address to which a computer program executed by the CPU 12 attempts to read or write. If the CPU 12 attempts to access the IDE hard disk drive through the super I/O chip 54, then the system logic controller 24 exchanges signals between the CPU bus 14 and the I/O bus 48 at the higher speed rather than at the slower ISA bus speed. Since the super I/O chip 54 is capable of operating at the higher speed, the super I/O chip 54 passes the higher speed operation of the I/O bus 48 directly onto the IDE hard disk drive. To prevent the higher speed signals present on the first section 46 of the I/O bus 48 from reaching I/O cards attached to the I/O bus 48, before accessing the IDE drive at higher speeds the system logic controller 24 transmits a control signal to the I/O bus section isolation buffer 56 which causes the I/O bus section isolation buffer 56 to isolate the second section 58 of the I/O bus 48 from the first section 46 of the I/O bus 48 while the system logic controller 24 operates the first section 46 of the I/O bus 48 at the speed of the CPU bus 14.

20

PCMCIA Over-Voltage Protection

Referring now to FIG. 2, because the system logic controller 24 of the present invention includes both the power management unit 128 and the PCMCIA controller 122, it can prevent damage to a PCMCIA card inserted into the PCMCIA sockets 72 when the computer 10 incorporating the system logic controller 24 chip resumes operating after having entered a 5V Suspend mode of operation such as that described herein above. The power management unit 128 included in the system logic controller 24 prevents the PCMCIA controller 122 from applying an excessively high voltage to the PCMCIA card by providing the PCMCIA controller 122 with a control signal when the computer 10 resumes operating in its higher power mode that is electrically equivalent to the signal provided to the PCMCIA controller 122 by the PCMCIA card's CD pin. Accordingly, immediately upon resuming operation in the higher power mode the control signal provided by the power management unit 128 to the PCMCIA controller 122 causes the PCMCIA controller 122 to interrogate the PCMCIA cards

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3V/5V pin to determine the PCMCIA card's operating voltage, after which the PCMCIA controller 122 applies the proper voltage to the PCMCIA card.

5 High Speed Operation For PCMCIA Cards

Conventional PCMCIA controllers connect to the I/O bus 48. Consequently, the operating speed of any PCMCIA card plugged into a PCMCIA socket connected to such a PCMCIA controller is limited to the operating speed of the I/O bus 48. However some of the
10 devices, e.g. Flash memory solid state disks, that are being incorporated into PCMCIA cards are capable of operating at much higher speeds than the speed of the I/O bus 48.

Fig. 4 depicts the preferred embodiment of the PCMCIA sockets 72 included in the computer 10. The PCMCIA sockets 72
15 preferably includes a Type 2 PCMCIA socket 172 and a Type 3 PCMCIA socket 174 either of which may receive an appropriate PCMCIA card (Not illustrated in any of the FIGs.). The PCMCIA control signal bus 74 connects directly in parallel to the PCMCIA sockets 172 and 174 for exchanging control signals therewith.
20 Conversely, the first section 46 of the I/O bus 48 connects through bidirectional PCMCIA buffers 176 and 178 respectively to the PCMCIA sockets 172 and 174 for exchanging data signals therewith. Control signals supplied to the PCMCIA buffers 176 and 178 via the PCMCIA control signal bus 74 enable one or the
25 other of the PCMCIA buffers 176 or 178 for exchanging signals between the I/O bus 48 and a PCMCIA card plugged into the PCMCIA socket 172 or into the PCMCIA socket 174.

To permit effective utilization of PCMCIA cards having a capacity to operate at speeds higher than the ISA bus speed, the
30 ISA bus address/data buffer 108 detects the presence of such a PCMCIA card in either of the PCMCIA sockets 172 and 174. If the PCMCIA controller 122 detects that a PCMCIA card capable of operating only at the slower ISA bus speed is inserted into the PCMCIA sockets 72, then the PCMCIA controller 122 selects signals
35 supplied to it by the system logic controller 24 to operate the PCMCIA card at the ISA bus speed. However, if the PCMCIA controller 122 detects that a PCMCIA card inserted in the PCMCIA sockets 72 is capable of operating at a higher speed, then the

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PCMCIA controller 122 selects signals supplied to it by the system logic controller 24 to operate the PCMCIA card at a faster bus speed, while the system logic controller 24 concurrently transmits a control signal to the I/O bus section isolation 5 buffer 56 which causes the I/O bus section isolation buffer 56 to isolate the second section 58 of the I/O bus 48 from the first section 46 of the I/O bus 48.

Industrial Applicability

10 By including the 3V/5V buffer 66 and the 3V extension 68 of the I/O bus 48, the computer 10 may further reduce power consumption by using three (3) volt ICs for the keyboard controller 62 and the ROM BIOS 64 which connect to the 3V extension 68 of the I/O bus 48 (Not illustrated in FIG. 1) 15 instead of the five (5) volt ICs that are depicted in FIG. 1.

An essential element in the 5V Suspend operating mode provided by the system logic controller 24 is that after all the internal data and states of the CPU 12 have been stored into the first preestablished area in the DRAM 26 in response to the first 20 SMI interrupt, the system logic controller 24 prevents overwriting the data stored in that area of the DRAM 26 in response to a second fake SMI interrupt. While the preferred embodiment of the present invention prevents overwriting the data through the technique of providing a second preestablished area in the DRAM 25 26 for storage of the internal data and states of the CPU 12, the 5V Suspend operating mode disclosed herein is compatible with any alternative technique that prevents overwriting the internal data and states of the CPU 12 stored in the first preestablished area of the DRAM 26.

30 Depending upon details of the design of the system logic controller 24, the master clock 144 may be a separate circuit included in the power management unit 128. Alternatively, if the system logic controller 24 includes the real-time clock 118 as in the preferred embodiment depicted in FIG. 2, then the 35 real-time clock 118 may provide the timing signals via the timing signal lines 146 to each timed event comparator 152. The interrupt time register 154 included in each of the timed interval interrupt generators 142a, 142b thru 142n is preferably

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eight bits long. To permit generation of interrupts by the system logic controller 24 at intervals of time which differ by more than a factor of two hundred and fifty six (256), lower order bits in the timing signals generated by the master clock 5 144 are supplied to the timed event comparator 152 included in some of the timed interval interrupt generators 142a, 142b thru 142n, while higher order bits in the timing signals are supplied to the timed event comparator 152 included in other timed interval interrupt generators 142a, 142b thru 142n. Thus, the 10 timed interval interrupt generators 142a, 142b thru 142n which receive the lower order bits of the timing signals may be used to generate interrupts for which the time interval is comparatively short, while those timed interval interrupt generators 142a, 142b thru 142n which receive the higher order bits of the 15 timing signals are used to generate interrupts for which the time interval is comparatively long.

In current practical application, the system logic controller 24 may operate an IDE drive through the super I/O chip 54 or may operate a PCMCIA card through the PCMCIA controller 122 at 20 a clock speed between 12 and 24 MHz which is specified by configuration data supplied to the system logic controller 24.

Although the present invention has been described in terms of the presently preferred embodiment, it is to be understood that such disclosure is purely illustrative and is not to be 25 interpreted as limiting. Consequently, without departing from the spirit and scope of the invention, various alterations, modifications, and/or alternative applications of the invention will, no doubt, be suggested to those skilled in the art after having read the preceding disclosure. Accordingly, it is intended 30 that the following claims be interpreted as encompassing all alterations, modifications, or alternative applications as fall within the true spirit and scope of the invention.

The Claims

What is claimed is:

1. An improved system logic controller for use in a digital computer that includes a central processing unit which is coupled to a CPU bus having CPU address lines and CPU data lines, said system logic controller being coupled to the CPU address lines and to the CPU data lines, and including a CPU interface controller, a DRAM controller, a I/O bus controller, and a peripheral controller; wherein the improvement comprises:
 - a direct port access buffer included in the digital computer that is coupled to the CPU address lines and which stores data for regulating electrical power consumption by the digital computer;
 - a power management unit included in said system logic controller for generating power management signals used in regulating electrical power consumption by the digital computer, said power management unit including a direct port access controller for supplying direct port access control signals to the direct port access buffer; said system logic controller, upon receiving an I/O command from the central processing unit that specifies an I/O operation between the central processing unit and the direct port access buffer, transmitting a hold control signal to the central processing unit requesting that the central processing unit halt operation; the central processing unit, upon receiving the hold control signal from said system logic controller, halting operation and tristating the CPU address lines; after the central processing unit has tristated all the CPU address lines, the direct port access controller transmitting a direct port access control signal to the direct port access buffer which causes an exchange of data between the direct port access buffer and said system logic controller over the CPU address lines; and after data has been exchanged between the direct port access buffer and said system logic controller, said system logic controller transmitting a signal to the central processing unit which causes the central processing unit to resume operation.

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2. The improved system logic controller of claim 1 wherein the I/O command received by said system logic controller from the central processing unit is a write command; upon said system logic controller receiving the write command from the central processing unit, said system logic controller reading and storing data placed on the CPU data lines by the central processing unit before said system logic controller transmits the hold control signal to the central processing unit; after said system logic controller transmits the hold control signal to the central processing unit and before said system logic controller exchanges data with the direct port access buffer, said system logic controller receiving a hold acknowledge signal from the central processing unit notifying said system logic controller that central processing unit operation has halted and that all the CPU address lines have been tristated; and said system logic controller then placing the data received from the central processing unit onto the CPU address lines while said direct port access controller transmits the direct port access control signal to the direct port access buffer which causes the direct port access buffer to latch the data present on the CPU address lines into the direct port access buffer.

3. The improved system logic controller of claim 1 wherein the I/O command received by said system logic controller from the central processing unit is a read command; said system logic controller upon receiving the read command from the central processing unit, transmitting the hold control signal from said system logic controller to the central processing unit which causes the central processing unit to immediately halt operating and tristate the CPU address lines; the direct port access control signal transmitted by the direct port access controller to the direct port access buffer causing the direct port access buffer to place data then present in the direct port access buffer onto the CPU address lines from which said system logic controller then reads and stores the data present on the CPU address lines; after said system logic controller has stored the data read from the CPU address lines, said system logic controller placing the data onto the CPU data lines and releases the

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hold control signal transmitted from said system logic controller to the central processing unit thereby permitting the central processing unit to read the data from the CPU data lines.

5 4. The improved system logic controller of claim 1 wherein said power management unit further includes a plurality of low-power timed interval interrupt generators each timed interval interrupt generator being adapted for generating a power management timed interrupt for transmission from said system
10 logic controller to the central processing unit, each timed interval interrupt generator including:

 a timed event comparator which respectively generates the power management timed interrupt, all of said timed event comparators in said power management unit simulta-
15 neously receiving timing signals generated by a single continuously running master clock, said system logic controller also permitting a computer program executed by the central processing unit to read the timing signals generated by the master clock; and

20 an interrupt time register into which a computer program executed by the central processing unit may caused to be stored time data representing a specific moment in time at which said timed event comparator is to generate a power management timed interrupt, each timed event
25 comparator continuously comparing the timing signals received from the master clock with the time data stored in the interrupt time register and generating a power management timed interrupt when the stored time data equals the timing signals.

30 5. The improved system logic controller of claim 4 wherein said system logic controller is also coupled to DRAM address lines; the digital computer also including a dynamic random access memory that is coupled to the CPU data lines and to the
35 DRAM address lines; the central processing unit in response to a system management interrupt that specifies a suspend mode of operation, storing all CPU internal data and states to a preestablished area in the dynamic random access memory and then

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removing electrical power from the central processing unit; and in response to a resume event, restoring electrical power to the central processing unit after which the central processing unit executes another system management interrupt; wherein the improvement further comprises:

upon the occurrence of an initial system management interrupt which specifies the suspend mode of operation said system logic controller:

- a. providing a memory address to a first physical memory SMI data storage area in the dynamic random access memory for storage of the CPU internal data and states in response to the initial system management interrupt, after the CPU internal data and states have been stored into the first physical memory SMI data storage area, the central processing unit executing a SMI power management routine which:
 - i. alters dynamic random access memory addressing by the system logic controller so the CPU internal data and states stored in the first physical memory SMI data storage area cannot be overwritten; and
 - ii. preserves within said system logic controller SMI state information indicating that said system logic controller has caused the CPU internal data and states to be stored into the first physical memory SMI data storage area,;
- b. placing the digital computer in a power suspend mode of operation in which said system logic controller removes electrical power from the central processing unit while the system logic controller continues to supply electrical power to the dynamic random access memory and continues to refresh the dynamic random access memory while awaiting an occurrence of a resume event;
- c. after a resume event occurs, restoring electrical power to the central processing unit thereby resuming execution of a power management routine which, upon detecting that SMI state information has been stored in said system logic controller, directs said system logic control-

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ler to generate a fake system management interrupt to the central processing unit;

- 5 d. said system logic controller generating the fake system management interrupt thereby causing the central processing unit to resume executing the SMI power management routine which, upon detecting that SMI state information has been preserved within said system logic controller, restores dynamic random access memory addressing by the system logic controller to the first physical memory
- 10 SMI data storage area into which CPU internal data and states were stored in response to the initial system management interrupt; and
- 15 e. terminating the power suspend mode of operation immediately after which execution of the SMI power management routine by the central processing unit restores the CPU internal data and states to that previously stored in the first physical memory SMI data storage area.

6. The improved system logic controller of claim 5 wherein
- 20 the digital computer also includes a super I/O chip that includes electronic circuits for providing a hard disk drive interface; said system logic controller being coupled by a first section of an I/O bus to the super I/O chip for exchanging signals with the super I/O chip, and being adapted for being coupled by a second
- 25 section of the I/O bus for exchanging signals with other I/O cards that may be included in the digital computer, said system logic controller exchanging signals via the I/O bus with the super I/O chip and with other I/O cards that may be included in the digital computer at a slower I/O bus speed; wherein the
- 30 digital computer further includes:

- a bidirectional I/O bus section isolation buffer disposed in the I/O bus between the first section of the I/O bus and the second section of the I/O bus for selectively isolating the second section of the I/O bus from the first section of the I/O
- 35 bus in response to an I/O bus isolation control signal generated by said system logic controller; and

wherein the improvement in said system logic controller further comprises:

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a hard disk access detection circuit for detecting I/O accesses by a computer program executed by the central processing unit to the hard disk drive interface included in the super I/O chip; said system logic controller during I/O accesses to the hard disk drive interface transmitting the I/O bus isolation control signal to the I/O bus section isolation buffer for isolating the second section of the I/O bus from the first section of the I/O bus, and while the I/O bus section isolation buffer isolates the second section of the I/O bus from the first section said system logic controller exchanging signals via the I/O bus with the super I/O chip at a faster CPU bus speed.

7. The improved system logic controller of claim 6 wherein said system logic controller further comprises a PCMCIA controller; the PCMCIA controller being adapted for exchanging PCMCIA control signals with a PCMCIA card inserted into a PCMCIA socket included in the digital computer; while the PCMCIA controller is operating, the PCMCIA controller, in response to a CD signal generated upon insertion of a PCMCIA card into the PCMCIA socket, interrogating the PCMCIA card to determine if the PCMCIA card operates at a first lower voltage or at a second higher voltage; said power management unit included in said system logic controller generating power management signals which turn off the PCMCIA controller to reduce electrical power consumption by the digital computer, and subsequently generating power management signals which turn on the PCMCIA controller, such power management signals including a PCMCIA power restoration control signal transmitted from said power management unit to the PCMCIA controller which within the PCMCIA controller simulates an occurrence of the CD signal, whereby the PCMCIA controller determines if any PCMCIA card then present in the PCMCIA socket operates at the first lower voltage or at the second higher voltage every time the power management signals turn the PCMCIA controller on.

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8. The improved system logic controller of claim 7 wherein said system logic controller is coupled by a first section of the I/O bus to the PCMCIA socket for exchanging PCMCIA data signals

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with a PCMCIA card inserted in the PCMCIA socket; said PCMCIA controller detecting whether a PCMCIA card inserted into the PCMCIA socket possesses a speed capability for operating at the faster CPU bus speed of the CPU bus or is limited to operating at the slower I/O bus speed of the I/O bus; said system logic controller supplying signals to said PCMCIA controller which permit said PCMCIA controller to selectively operate a PCMCIA card inserted into the PCMCIA socket either at the slower I/O bus speed of the I/O bus or at the faster CPU bus speed of the CPU bus depending upon the speed capability of the PCMCIA card; said system logic controller including a PCMCIA card access detection circuit for detecting I/O accesses by a computer program executed by the central processing unit to a PCMCIA card inserted into the PCMCIA socket, and for transmitting the I/O bus isolation control signal to the I/O bus section isolation buffer for isolating the second section of the I/O bus from the first section of the I/O bus if said PCMCIA controller operates the PCMCIA card at the faster CPU bus speed.

9. The improved system logic controller of claim 1 wherein said system logic controller is also coupled to DRAM address lines; the digital computer also including a dynamic random access memory that is coupled to the CPU data lines and to the DRAM address lines; the central processing unit in response to a system management interrupt that specifies a suspend mode of operation, storing all CPU internal data and states to a preestablished area in the dynamic random access memory and then removing electrical power from the central processing unit; and in response to a resume event, restoring electrical power to the central processing unit after which the central processing unit executes another system management interrupt; wherein the improvement further comprises:

upon the occurrence of an initial system management interrupt which specifies the suspend mode of operation said system logic controller:

a. providing a memory address to a first physical memory SMI data storage area in the dynamic random access memory for storage of the CPU internal data and states in response

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to the initial system management interrupt, after the CPU internal data and states have been stored into the first physical memory SMI data storage area, the central processing unit executing a SMI power management routine which:

- 5 i. alters dynamic random access memory addressing by the system logic controller so the CPU internal data and states stored in the first physical memory SMI data storage area cannot be overwritten; and
- 10 ii. preserves within said system logic controller SMI state information indicating that said system logic controller has caused the CPU internal data and states to be stored into the first physical memory SMI data storage area,;
- 15 b. placing the digital computer in a power suspend mode of operation in which said system logic controller removes electrical power from the central processing unit while the system logic controller continues to supply electrical power to the dynamic random access memory and continues to
- 20 refresh the dynamic random access memory while awaiting an occurrence of a resume event;
- c. after a resume event occurs, restoring electrical power to the central processing unit thereby resuming execution of a power management routine which, upon detecting
- 25 that SMI state information has been stored in said system logic controller, directs said system logic controller to generate a fake system management interrupt to the central processing unit;
- d. said system logic controller generating the fake
- 30 system management interrupt thereby causing the central processing unit to resume executing the SMI power management routine which, upon detecting that SMI state information has been preserved within said system logic controller, restores dynamic random access memory addressing by
- 35 the system logic controller to the first physical memory SMI data storage area into which CPU internal data and states were stored in response to the initial system management interrupt; and

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e. terminating the power suspend mode of operation immediately after which execution of the SMI power management routine by the central processing unit restores the CPU internal data and states to that previously stored in the first physical memory SMI data storage area.

10. The improved system logic controller of claim 1 wherein the digital computer also includes a super I/O chip that includes electronic circuits for providing a hard disk drive interface; said system logic controller being coupled by a first section of an I/O bus to the super I/O chip for exchanging signals with the super I/O chip, and being adapted for being coupled by a second section of the I/O bus for exchanging signals with other I/O cards that may be included in the digital computer, said system logic controller exchanging signals via the I/O bus with the super I/O chip and with other I/O cards that may be included in the digital computer at a slower I/O bus speed; wherein the digital computer further includes:

a bidirectional I/O bus section isolation buffer disposed in the I/O bus between the first section of the I/O bus and the second section of the I/O bus for selectively isolating the second section of the I/O bus from the first section of the I/O bus in response to an I/O bus isolation control signal generated by said system logic controller; and

wherein the improvement in said system logic controller further comprises:

a hard disk access detection circuit for detecting I/O accesses by a computer program executed by the central processing unit to the hard disk drive interface included in the super I/O chip; said system logic controller during I/O accesses to the hard disk drive interface transmitting the I/O bus isolation control signal to the I/O bus section isolation buffer for isolating the second section of the I/O bus from the first section of the I/O bus, and while the I/O bus section isolation buffer isolates the second section of the I/O bus from the first section said system logic controller exchanging signals via the I/O bus with the super I/O chip at a faster CPU bus speed.

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11. The improved system logic controller of claim 1 wherein said system logic controller further comprises a PCMCIA controller; the PCMCIA controller being adapted for exchanging data with a PCMCIA card inserted into a PCMCIA socket included in the digital computer; while the PCMCIA controller is operating, the PCMCIA controller, in response to a CD signal generated upon insertion of a PCMCIA card into the PCMCIA socket, interrogating the PCMCIA card to determine if the PCMCIA card operates at a first lower voltage or at a second higher voltage; said power management unit included in said system logic controller generating power management signals which turn off the PCMCIA controller to reduce electrical power consumption by the digital computer, and subsequently generating power management signals which turn on the PCMCIA controller, such power management signals including a PCMCIA power restoration control signal transmitted from said power management unit to the PCMCIA controller which within the PCMCIA controller simulates an occurrence of the CD signal, whereby the PCMCIA controller determines if any PCMCIA card then present in the PCMCIA socket operates at the first lower voltage or at the second higher voltage every time the power management signals turn the PCMCIA controller on.

12. The improved system logic controller of claim 1 wherein said system logic controller is adapted for being coupled by a first section of an I/O bus to a PCMCIA socket included in the digital computer for exchanging PCMCIA data signals with a PCMCIA card inserted in a PCMCIA socket, and is also adapted for being coupled by a second section of the I/O bus for exchanging signals with other I/O cards that may be included in the digital computer with which said system logic controller exchanges signals via the I/O bus at a slower I/O bus speed; and wherein the digital computer further includes:

a bidirectional I/O bus section isolation buffer disposed in the I/O bus between the first section of the I/O bus and the second section of the I/O bus for selectively isolating the second section of the I/O bus from the first section of the I/O

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bus in response to an I/O bus isolation control signal generated by said system logic controller;

said system logic controller further comprising a PCMCIA controller adapted for exchanging PCMCIA control signals with a PCMCIA card inserted into the PCMCIA socket; said PCMCIA controller detecting whether a PCMCIA card inserted into the PCMCIA socket possesses a speed capability for operating at a faster CPU bus speed of the CPU bus or is limited to operating at the slower I/O bus speed of the I/O bus; said system logic controller including a PCMCIA card access detection circuit for detecting I/O accesses by a computer program executed by the central processing unit to a PCMCIA card inserted into the PCMCIA socket, and supplying signals to said PCMCIA controller which permit said PCMCIA controller to selectively operate a PCMCIA card inserted into the PCMCIA socket either at the slower I/O bus speed of the I/O bus or at the faster CPU bus speed of the CPU bus depending upon the speed capability of the PCMCIA card; said system logic controller transmitting the I/O bus isolation control signal to the I/O bus section isolation buffer for isolating the second section of the I/O bus from the first section of the I/O bus if said PCMCIA controller operates the PCMCIA card at the faster CPU bus speed.

13. An improved system logic controller for use in a digital computer that includes a central processing unit which is coupled to a CPU bus having CPU address lines and CPU data lines; said system logic controller being coupled to the CPU address lines and to the CPU data lines, and including a CPU interface controller, a DRAM controller, a I/O bus controller, and a peripheral controller; wherein the improvement comprises:

a power management unit included in said system logic controller for generating power management signals used in regulating electrical power consumption by the digital computer, said power management unit including a plurality of low-power timed interval interrupt generators each timed interval interrupt generator being adapted for generating a power management timed interrupt for transmission from said system logic controller to

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the central processing unit, each timed interval interrupt generator including:

5 a timed event comparator which respectively generates the power management timed interrupt, all of said timed event comparators in said power management unit simultaneously receiving timing signals generated by a single continuously running master clock, said system logic controller also permitting a computer program executed by the central processing unit to read the timing signals generated by the master clock; and

10 an interrupt time register into which a computer program executed by the central processing unit may cause to be stored time data representing a specific moment in time at which said timed event comparator is to generate a power management timed interrupt, each timed event comparator continuously comparing the timing signals received from the master clock with the time data stored in the interrupt time register and generating a power management timed interrupt when the stored time data equals the timing signals.

14. The improved system logic controller of claim 13 wherein said power management unit includes the master clock that supplies the timing signals received by all said timed event comparators.

15. The improved system logic controller of claim 13 wherein said system logic controller includes a real time clock that supplies the timing signals received by all said timed event comparators.

16. The improved system logic controller of claim 13 further comprising a timed interrupts register that may be read by a computer program executed by the central processing unit, said timed interrupts register concurrently storing the several power management timed interrupts generated by all said timed event comparators included in said timed interval interrupt generator.

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17. The improved system logic controller of claim 13 wherein each timed interval interrupt generator further includes:

a plurality of interrupt interval registers into which a computer program executed by the central processing unit may
5 cause to be stored time data representing a duration of time between immediately successive power management timed interrupts; and

an adder having a first input which receives from said interrupt interval registers the data representing a duration of
10 time between immediately successive interrupts, said adder also having a second input which receives from said interrupt time register the data representing a specific moment in time at which said timed event comparator is to generate a power management timed interrupt, said adder also having an adder output which
15 supplies a result of any addition performed by said adder to said interrupt time register, said adder also receiving a trigger signal from said timed event comparator every time said timed event comparator generates the power management timed interrupt in response to which said adder adds together the data present
20 in said interrupt interval registers and in said interrupt time register and stores the result of such addition back into said interrupt time register, whereby said timed interval interrupt generator generates a succession of power management timed interrupts each immediately successive pair of which are
25 separated by the same duration of time.

18. An improved system logic controller for use in a digital computer that includes a central processing unit which is coupled to a CPU bus having CPU address lines and CPU data
30 lines; said system logic controller being coupled to the CPU address lines, to the CPU data lines and to DRAM address lines, and including a CPU interface controller, a DRAM controller, a I/O bus controller, and a peripheral controller; the digital computer also including a dynamic random access memory that is
35 coupled to the CPU data lines and to the DRAM address lines; the central processing unit in response to a system management interrupt that specifies a suspend mode of operation, storing all CPU internal data and states to a preestablished area in the

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dynamic random access memory and then removing electrical power from the central processing unit; and in response to a resume event, restoring electrical power to the central processing unit after which the central processing unit executes another system

5 management interrupt; wherein the improvement comprises:

upon the occurrence of an initial system management interrupt which specifies the suspend mode of operation said system logic controller:

10 a. providing a memory address to a first physical memory SMI data storage area in the dynamic random access memory for storage of the CPU internal data and states in response to the initial system management interrupt, after the CPU internal data and states have been stored into the first physical memory SMI data storage area, the central processing unit executing a SMI power management routine which:

15 i. alters dynamic random access memory addressing by the system logic controller so the CPU internal data and states stored in the first physical memory SMI data storage area cannot be overwritten; and

20 ii. preserves within said system logic controller SMI state information indicating that said system logic controller has caused the CPU internal data and states to be stored into the first physical memory SMI data storage area,;

25 b. placing the digital computer in a power suspend mode of operation in which said system logic controller removes electrical power from the central processing unit while the system logic controller continues to supply electrical power to the dynamic random access memory and continues to refresh the dynamic random access memory while awaiting an occurrence of a resume event;

30 c. after a resume event occurs, restoring electrical power to the central processing unit thereby resuming execution of a power management routine which, upon detecting that SMI state information has been stored in said system logic controller, directs said system logic control-

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ler to generate a fake system management interrupt to the central processing unit;

- 5 d. said system logic controller generating the fake system management interrupt thereby causing the central processing unit to resume executing the SMI power management routine which, upon detecting that SMI state information has been preserved within said system logic controller, restores dynamic random access memory addressing by the system logic controller to the first physical memory
- 10 SMI data storage area into which CPU internal data and states were stored in response to the initial system management interrupt; and
- 15 e. terminating the power suspend mode of operation immediately after which execution of the SMI power management routine by the central processing unit restores the CPU internal data and states to that previously stored in the first physical memory SMI data storage area.

19. The improved system logic controller of claim 18
20 wherein said system logic controller:

- 25 a. alters dynamic random access memory addressing by establishing a memory address to a second physical memory SMI data storage area into which CPU internal data and states will be stored in response to a subsequent system management interrupt thereby preventing overwriting of the CPU internal data and states stored in response to the initial system management interrupt; and
- 30 b. upon the occurrence of the fake system management interrupt, causing the then existing CPU internal data and states to be stored into the second physical memory SMI data storage area.

20. An improved system logic controller for use in a
35 digital computer that includes a central processing unit which is coupled to a CPU bus having CPU address lines and CPU data lines, the digital computer also including a super I/O chip that includes electronic circuits for providing a hard disk drive

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interface; said system logic controller including a CPU interface controller, a DRAM controller, a I/O bus controller, and a peripheral controller, and said system logic controller being coupled to the CPU address lines and to the CPU data lines, and
5 also being adapted for being coupled by a first section of an I/O bus to the super I/O chip for exchanging signals with the super I/O chip, and also being adapted for being coupled by a second section of the I/O bus for exchanging signals with other I/O cards that may be included in the digital computer; said system
10 logic controller exchanging signals via the I/O bus with the super I/O chip and with other I/O cards that may be included in the digital computer at a slower I/O bus speed; wherein the digital computer further includes:

a bidirectional I/O bus section isolation buffer disposed
15 in the I/O bus between the first section of the I/O bus and the second section of the I/O bus for selectively isolating the second section of the I/O bus from the first section of the I/O bus in response to an I/O bus isolation control signal generated by said system logic controller; and

20 wherein the improvement in said system logic controller comprises:

a hard disk access detection circuit for detecting I/O accesses by a computer program executed by the central processing unit to the hard disk drive interface included in the super I/O
25 chip; said system logic controller during I/O accesses to the hard disk drive interface transmitting the I/O bus isolation control signal to the I/O bus section isolation buffer for isolating the second section of the I/O bus from the first section of the I/O bus, and while the I/O bus section isolation
30 buffer isolates the second section of the I/O bus from the first section said system logic controller exchanging signals via the I/O bus with the super I/O chip at a faster CPU bus speed.

21. The improved system logic controller of claim 20
35 wherein the hard disk drive interface included in the super I/O chip is an IDE hard disk drive interface.

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22. An improved system logic controller for use in a digital computer that includes a central processing unit which is coupled to a CPU bus having CPU address lines and CPU data lines; said system logic controller being coupled to the CPU address lines and to the CPU data lines, and including a CPU interface controller, a DRAM controller, a I/O bus controller, and a peripheral controller; wherein the improvement comprises: both a power management unit and a PCMCIA controller included in said system logic controller; the PCMCIA controller being adapted for exchanging data with a PCMCIA card inserted into a PCMCIA socket included in the digital computer; while the PCMCIA controller is operating, the PCMCIA controller, in response to a CD signal generated upon insertion of a PCMCIA card into the PCMCIA socket, interrogating the PCMCIA card to determine if the PCMCIA card operates at a first lower voltage or at a second higher voltage; said power management unit generating power management signals which turn off the PCMCIA controller to reduce electrical power consumption by the digital computer, and subsequently generating power management signals which turn on the PCMCIA controller, such power management signals including a PCMCIA power restoration control signal transmitted from said power management unit to the PCMCIA controller which within the PCMCIA controller simulates an occurrence of the CD signal, whereby the PCMCIA controller determines if any PCMCIA card then present in the PCMCIA socket operates at the first lower voltage or at the second higher voltage every time the power management signals turn the PCMCIA controller on.

23. An improved system logic controller for use in a digital computer that includes a central processing unit which is coupled to a CPU bus having CPU address lines and CPU data lines; said system logic controller being coupled to the CPU address lines and to the CPU data lines, and including a CPU interface controller, a DRAM controller, a I/O bus controller, and a peripheral controller; wherein the improvement further comprises:

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- said system logic controller being adapted for being coupled by a first section of an I/O bus to a PCMCIA socket included in the digital computer for exchanging PCMCIA data signals with a PCMCIA card inserted in a PCMCIA socket, and also being adapted
- 5 for being coupled by a second section of the I/O bus for exchanging signals with other I/O cards that may be included in the digital computer with which said system logic controller exchanges signals via the I/O bus at a slower I/O bus speed; and wherein the digital computer further includes:
- 10 a bidirectional I/O bus section isolation buffer disposed in the I/O bus between the first section of the I/O bus and the second section of the I/O bus for selectively isolating the second section of the I/O bus from the first section of the I/O bus in response to an I/O bus isolation control signal generated
- 15 by said system logic controller;
- said system logic controller further comprising a PCMCIA controller adapted for exchanging PCMCIA control signals with a PCMCIA card inserted into the PCMCIA socket; said PCMCIA controller detecting whether a PCMCIA card inserted into the
- 20 PCMCIA socket possesses a speed capability for operating at a faster CPU bus speed of the CPU bus or is limited to operating at the slower I/O bus speed of the I/O bus; said system logic controller including a PCMCIA card access detection circuit for detecting I/O accesses by a computer program executed by the
- 25 central processing unit to a PCMCIA card inserted into the PCMCIA socket, and supplying signals to said PCMCIA controller which permit said PCMCIA controller to selectively operate a PCMCIA card inserted into the PCMCIA socket either at the slower I/O bus speed of the I/O bus or at the faster CPU bus speed of the CPU
- 30 bus depending upon the speed capability of the PCMCIA card; said system logic controller transmitting the I/O bus isolation control signal to the I/O bus section isolation buffer for isolating the second section of the I/O bus from the first section of the I/O bus if said PCMCIA controller operates the
- 35 PCMCIA card at the faster CPU bus speed.

24. An improved digital computer that includes a central processing unit which is coupled to a CPU bus having CPU address

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lines and CPU data lines, said digital computer also including a system logic controller that is coupled to the CPU address lines and to the CPU data lines, the system logic controller including a CPU interface controller, a DRAM controller, a I/O
5 bus controller, and a peripheral controller, wherein the improvement comprises:

a direct port access buffer that is coupled to the CPU address lines and which stores data for regulating electrical power consumption by the digital computer; and
10 a power management unit included in said system logic controller for generating power management signals used in regulating electrical power consumption by the digital computer, said power management unit including a direct port access controller for supplying direct port access control signals to
15 the direct port access buffer; said system logic controller, upon receiving an I/O command from the central processing unit that specifies an I/O operation between the central processing unit and the direct port access buffer, transmitting a hold control signal to the central processing unit requesting that the central
20 processing unit halt operation; the central processing unit, upon receiving the hold control signal from said system logic controller, halting operation and tristating the CPU address lines; after the central processing unit has tristated all the CPU address lines, the direct port access controller transmitting
25 a direct port access control signal to the direct port access buffer which causes an exchange of data between the direct port access buffer and said system logic controller over the CPU address lines; and after data has been exchanged between the direct port access buffer and said system logic controller, said
30 system logic controller transmitting a signal to the central processing unit which causes the central processing unit to resume operation.

25. The improved digital computer of claim 24 wherein the
35 I/O command received by said system logic controller from the central processing unit is a write command; upon said system logic controller receiving the write command from the central processing unit, said system logic controller reading and storing

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data placed on the CPU data lines by the central processing unit before said system logic controller transmits the hold control signal to the central processing unit; after said system logic controller transmits the hold control signal to the central processing unit and before said system logic controller exchanges data with the direct port access buffer, said system logic controller receiving a hold acknowledge signal from the central processing unit notifying said system logic controller that central processing unit operation has halted and that all the CPU address lines have been tristated; and said system logic controller then placing the data received from the central processing unit onto the CPU address lines while said direct port access controller transmits the direct port access control signal to the direct port access buffer which causes the direct port access buffer to latch the data present on the CPU address lines into the direct port access buffer.

26. The improved digital computer of claim 24 wherein the I/O command received by said system logic controller from the central processing unit is a read command; said system logic controller upon receiving the read command from the central processing unit, transmitting the hold control signal from said system logic controller to the central processing unit which causes the central processing unit to immediately halt operating and tristate the CPU address lines; the direct port access control signal transmitted by the direct port access controller to the direct port access buffer causing the direct port access buffer to place data then present in the direct port access buffer onto the CPU address lines from which said system logic controller then reads and stores the data present on the CPU address lines; after said system logic controller has stored the data read from the CPU address lines, said system logic controller placing the data onto the CPU data lines and releases the hold control signal transmitted from said system logic controller to the central processing unit thereby permitting the central processing unit to read the data from the CPU data lines.

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27. The improved digital computer of claim 24 wherein said power management unit further includes a plurality of low-power timed interval interrupt generators each timed interval interrupt generator being adapted for generating a power management timed interrupt for transmission from said system logic controller to the central processing unit, each timed interval interrupt generator including:

10 a timed event comparator which respectively generates the power management timed interrupt, all of said timed event comparators in said power management unit simultaneously receiving timing signals generated by a single continuously running master clock, said system logic controller also permitting a computer program executed by the central processing unit to read the timing signals generated by the master clock; and

15 an interrupt time register into which a computer program executed by the central processing unit may cause to be stored time data representing a specific moment in time at which said timed event comparator is to generate a power management timed interrupt, each timed event comparator continuously comparing the timing signals received from the master clock with the time data stored in the interrupt time register and generating a power management timed interrupt when the stored time data equals the timing signals.

28. The improved digital computer of claim 24 wherein said system logic controller is also coupled to DRAM address lines; the digital computer also including a dynamic random access memory that is coupled to the CPU data lines and to the DRAM address lines; the central processing unit in response to a system management interrupt that specifies a suspend mode of operation, storing all CPU internal data and states to a preestablished area in the dynamic random access memory and then removing electrical power from the central processing unit; and in response to a resume event, restoring electrical power to the central processing unit after which the central processing unit

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executes another system management interrupt; wherein the improvement further comprises:

upon the occurrence of an initial system management interrupt which specifies the suspend mode of operation said
5 system logic controller:

- a. providing a memory address to a first physical memory SMI data storage area in the dynamic random access memory for storage of the CPU internal data and states in response to the initial system management interrupt, after the CPU
10 internal data and states have been stored into the first physical memory SMI data storage area, the central processing unit executing a SMI power management routine which:
 - i. alters dynamic random access memory addressing by the system logic controller so the CPU internal
15 data and states stored in the first physical memory SMI data storage area cannot be overwritten; and
 - ii. preserves within said system logic controller SMI state information indicating that said system
20 logic controller has caused the CPU internal data and states to be stored into the first physical memory SMI data storage area,;
- b. placing the digital computer in a power suspend mode of operation in which said system logic controller removes
25 electrical power from the central processing unit while the system logic controller continues to supply electrical power to the dynamic random access memory and continues to refresh the dynamic random access memory while awaiting an occurrence of a resume event;
- c. after a resume event occurs, restoring electrical
30 power to the central processing unit thereby resuming execution of a power management routine which, upon detecting that SMI state information has been stored in said system logic controller, directs said system logic controller to generate a fake system management interrupt to the
35 central processing unit;
- d. said system logic controller generating the fake system management interrupt thereby causing the central

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processing unit to resume executing the SMI power management routine which, upon detecting that SMI state information has been preserved within said system logic controller, restores dynamic random access memory addressing by the system logic controller to the first physical memory SMI data storage area into which CPU internal data and states were stored in response to the initial system management interrupt; and

5 e. terminating the power suspend mode of operation immediately after which execution of the SMI power management routine by the central processing unit restores the CPU internal data and states to that previously stored in the first physical memory SMI data storage area.

10

15 29. The improved digital computer of claim 24 wherein the digital computer also includes a super I/O chip that includes electronic circuits for providing a hard disk drive interface; said system logic controller being coupled by a first section of an I/O bus to the super I/O chip for exchanging signals with the super I/O chip, and being adapted for being coupled by a second section of the I/O bus for exchanging signals with other I/O cards that may be included in the digital computer, said system logic controller exchanging signals via the I/O bus with the super I/O chip and with other I/O cards that may be included in the digital computer at a slower I/O bus speed; wherein the digital computer further includes:

20

 a bidirectional I/O bus section isolation buffer disposed in the I/O bus between the first section of the I/O bus and the second section of the I/O bus for selectively isolating the second section of the I/O bus from the first section of the I/O bus in response to an I/O bus isolation control signal generated by said system logic controller; and

25

 wherein the improvement in said system logic controller further comprises:

30 a hard disk access detection circuit for detecting I/O accesses by a computer program executed by the central processing unit to the hard disk drive interface included in the super I/O chip; said system logic controller during I/O accesses to the

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hard disk drive interface transmitting the I/O bus isolation control signal to the I/O bus section isolation buffer for isolating the second section of the I/O bus from the first section of the I/O bus, and while the I/O bus section isolation
5 buffer isolates the second section of the I/O bus from the first section said system logic controller exchanging signals via the I/O bus with the super I/O chip at a faster CPU bus speed.

30. The improved digital computer of claim 24 wherein said
10 system logic controller further comprises a PCMCIA controller; the PCMCIA controller being adapted for exchanging data with a PCMCIA card inserted into a PCMCIA socket included in the digital computer; while the PCMCIA controller is operating, the PCMCIA controller, in response to a CD signal generated upon insertion
15 of a PCMCIA card into the PCMCIA socket, interrogating the PCMCIA card to determine if the PCMCIA card operates at a first lower voltage or at a second higher voltage; said power management unit included in said system logic controller generating power management signals which turn off the PCMCIA controller to reduce
20 electrical power consumption by the digital computer, and subsequently generating power management signals which turn on the PCMCIA controller, such power management signals including a PCMCIA power restoration control signal transmitted from said power management unit to the PCMCIA controller which within the
25 PCMCIA controller simulates an occurrence of the CD signal, whereby the PCMCIA controller determines if any PCMCIA card then present in the PCMCIA socket operates at the first lower voltage or at the second higher voltage every time the power management signals turn the PCMCIA controller on.

30

31. The improved digital computer of claim 24 wherein said system logic controller is adapted for being coupled by a first section of an I/O bus to a PCMCIA socket included in the digital computer for exchanging PCMCIA data signals with a PCMCIA card
35 inserted in a PCMCIA socket, and is also adapted for being coupled by a second section of the I/O bus for exchanging signals with other I/O cards that may be included in the digital computer with which said system logic controller exchanges signals via the

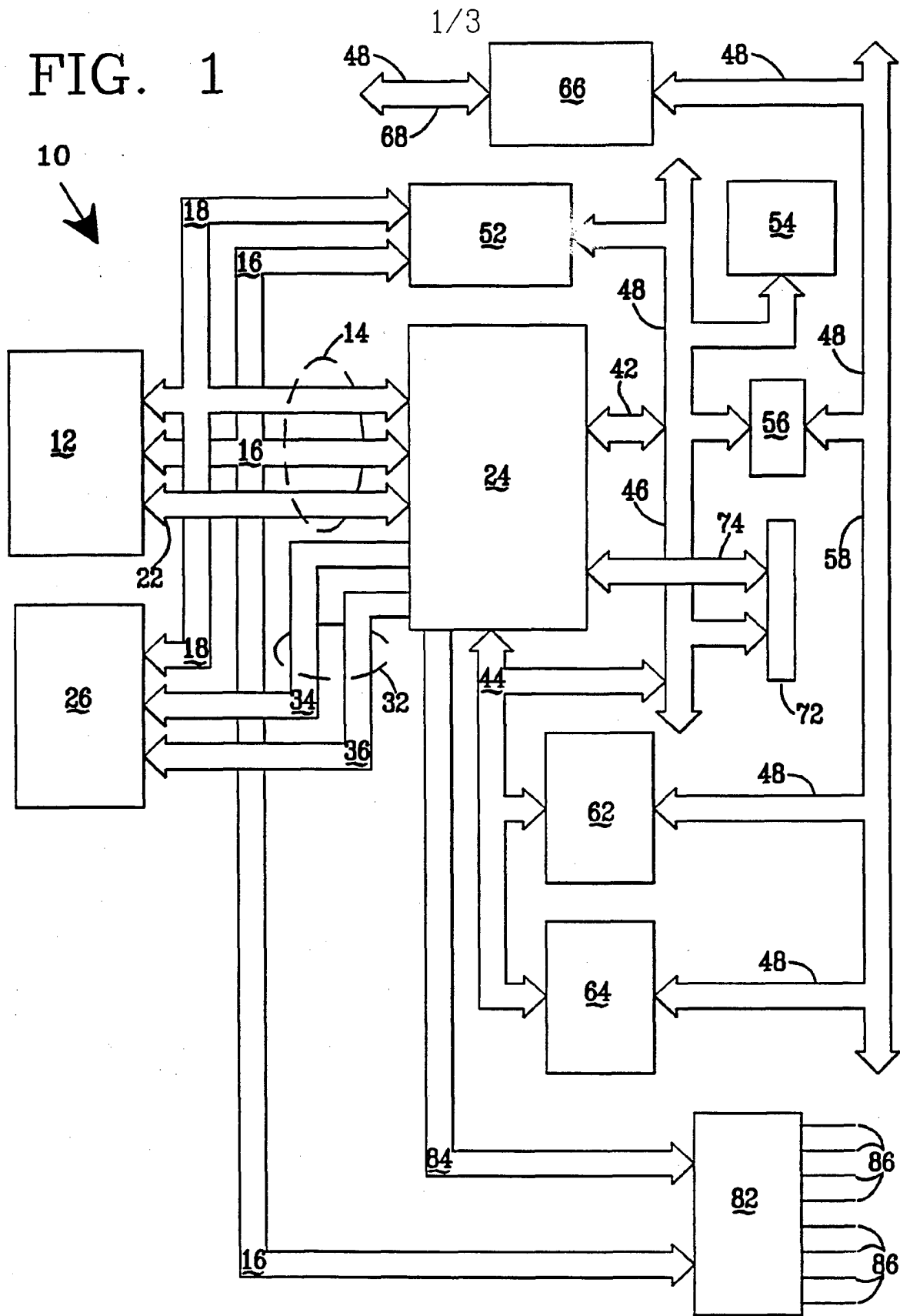
- 53 -

I/O bus at a slower I/O bus speed; and wherein the digital computer further includes:

5 a bidirectional I/O bus section isolation buffer disposed in the I/O bus between the first section of the I/O bus and the second section of the I/O bus for selectively isolating the second section of the I/O bus from the first section of the I/O bus in response to an I/O bus isolation control signal generated by said system logic controller;

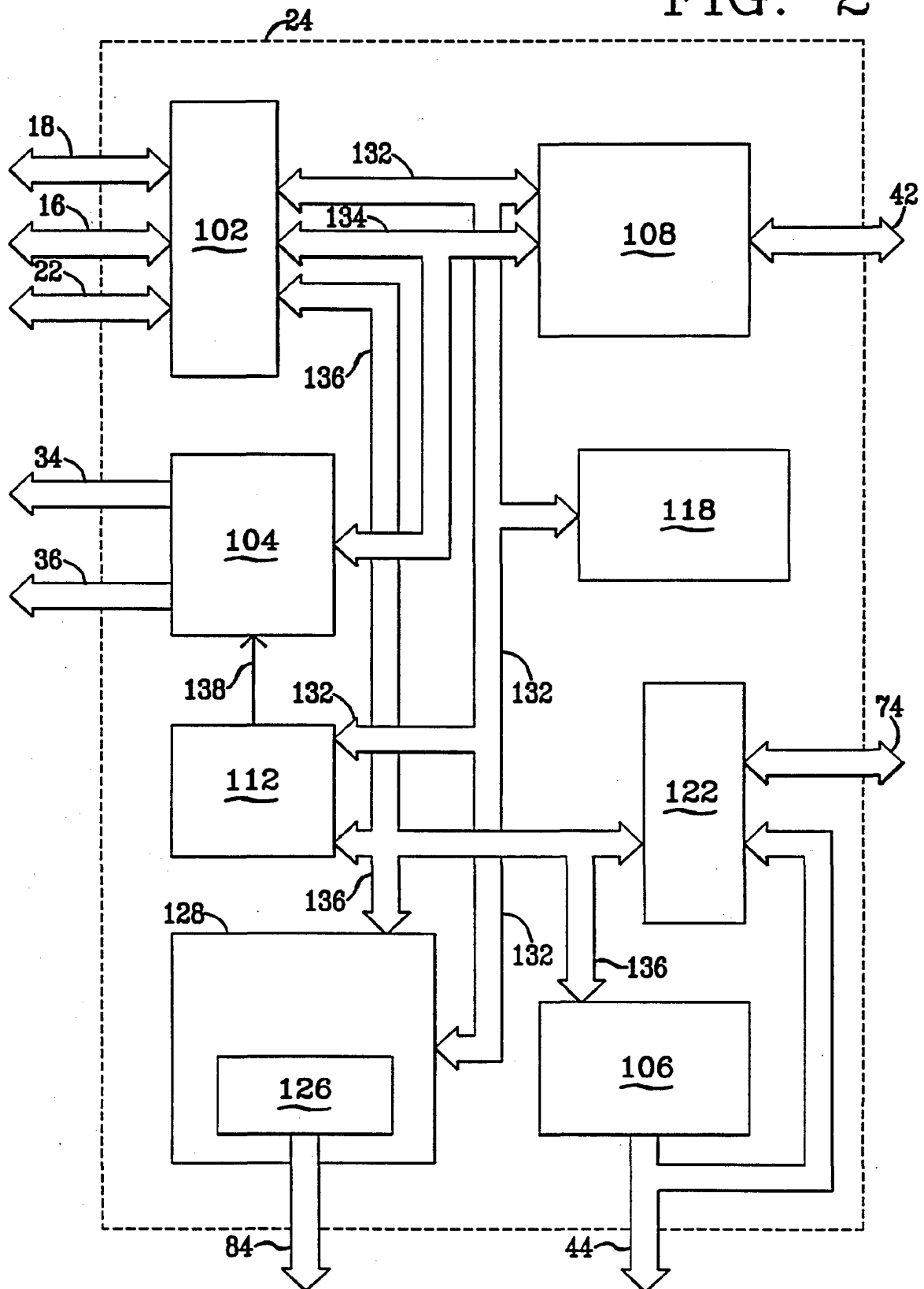
10 said system logic controller further comprising a PCMCIA controller adapted for exchanging PCMCIA control signals with a PCMCIA card inserted into the PCMCIA socket; said PCMCIA controller detecting whether a PCMCIA card inserted into the PCMCIA socket possesses a speed capability for operating at a faster CPU bus speed of the CPU bus or is limited to operating
15 at the slower I/O bus speed of the I/O bus; said system logic controller including a PCMCIA card access detection circuit for detecting I/O accesses by a computer program executed by the central processing unit to a PCMCIA card inserted into the PCMCIA socket, and supplying signals to said PCMCIA controller which
20 permit said PCMCIA controller to selectively operate a PCMCIA card inserted into the PCMCIA socket either at the slower I/O bus speed of the I/O bus or at the faster CPU bus speed of the CPU bus depending upon the speed capability of the PCMCIA card; said system logic controller transmitting the I/O bus isolation
25 control signal to the I/O bus section isolation buffer for isolating the second section of the I/O bus from the first section of the I/O bus if said PCMCIA controller operates the PCMCIA card at the faster CPU bus speed.

FIG. 1



2/3

FIG. 2



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FIG. 3

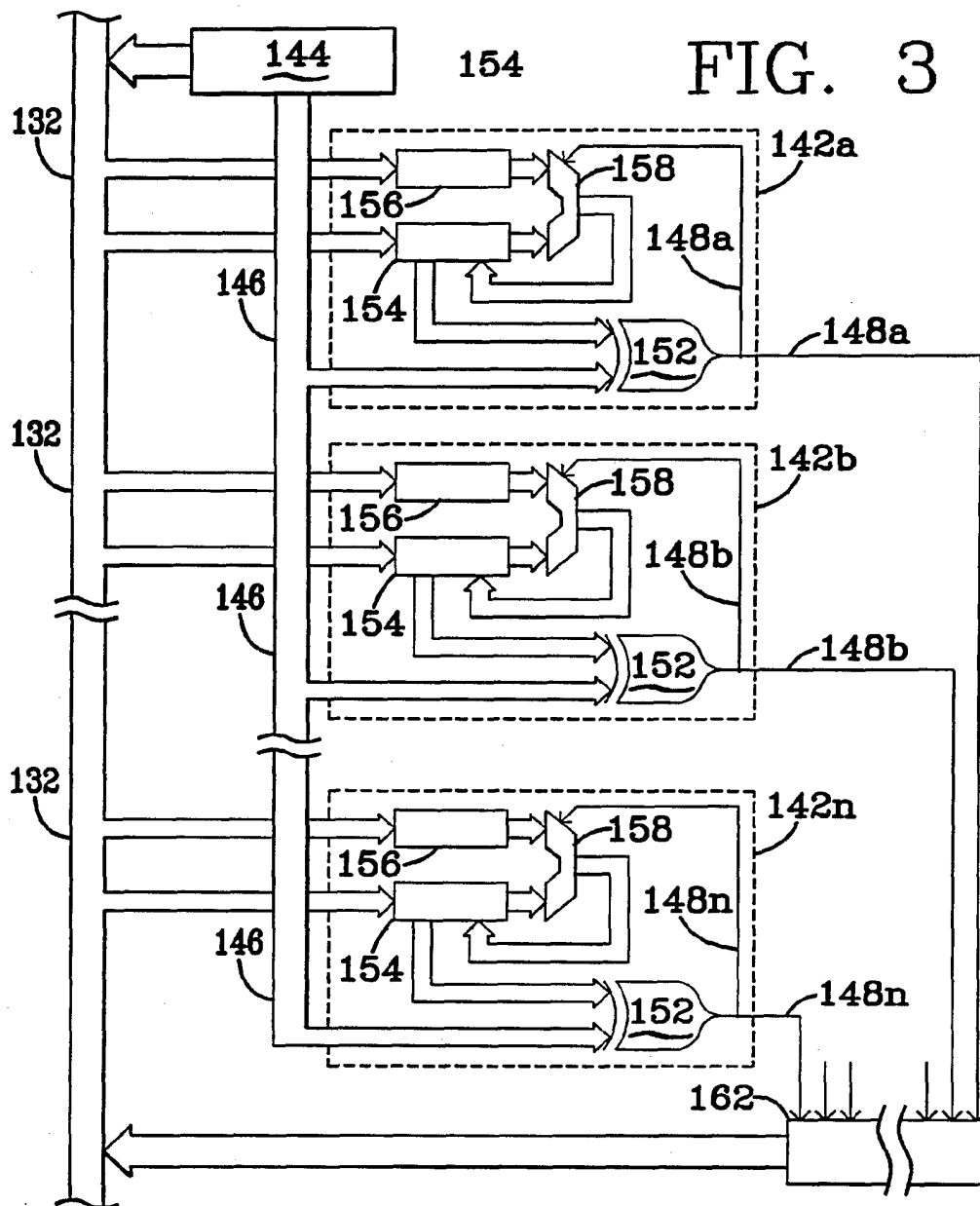
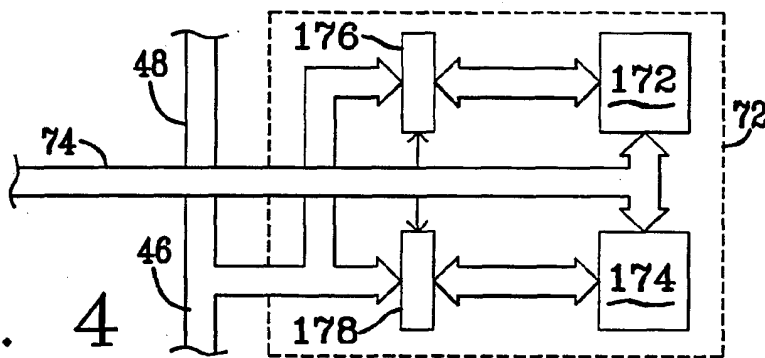


FIG. 4



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/04241

A. CLASSIFICATION OF SUBJECT MATTER

IPC(6) :G06F 1/32, 13/00
US CL :395/750,275,550; 364/707

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)

U.S. : 395/750,275,550; 364/707

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

Please See Extra Sheet.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Y	US, A, 5,167,024 (Smith et al.) 24 November 1992, See Fig.1 elements 11, 12, 27, and 28, Cols. 4-12	4, and 13-16
Y	US, A, 5,230,074 (Canova, Jr. et al.) 20 July 1993, See Figs. 1, and 3, Elements 12,14,30,100,106,108, and 110, Cols. 2 line 46- Col.9 line 60,	1-3 and 24-26
A	US, A, 5,083,266 (Watanabe) 21 January, 1992, See Figs. 1-2, Cols. 3-6,	1-4,13-16, and 24-26
A	US, A, 5,239,652 (Seibert et al.) 24 August 1993, See Fig. 1, Cols. 3-10	1,13, and 24
A	US, A, 4,851,987 (Day) 25 July 1989 See Fig.1 Cols. 3-6	1-3,13, 24

☒ Further documents are listed in the continuation of Box C. ☐ See patent family annex.

* Special categories of cited documents:	*T later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention
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Date of the actual completion of the international search

03 NOVEMBER 1994

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INTERNATIONAL SEARCH REPORT

International application No.
PCT/US94/04241

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
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A	US, A, 4,571,671 (Burns et al.) 18 February 1986, See Figs. 1-3 Cols. 2-5	6,8,10,12,20-21,23,29 and 31
A	US, A, 5,241,680 (Cole et al.) 31 August 1993 See Figs.3a-3b, and 4, Cols. 4-10	1-4,13-16, and 24-27
A	US, A, 4,615,005 (Maejima et al) 30 September 1986 See Cols. 3-7	1-3, and 24-26
A	US, A, 5,203,848 (Wang) 20 April 1993 See Fig. 3 Cols. 2-4	1-3, and 24-26
Y	US, A, 5,247,655 (Khan et al.) 21 September 1993 See Figs. 1-2, Col. 2 line 36- Col. 3 line 26	1-3 and 24-26
Y	US, A, 5,191,657 (Ludwig et al) 02 March 1993 See Fig. 1 elements 118,124, and 126, Col. 6 line 27- Col. 9 line 12,	6,10,20,23, and 29
Y,E	US, A, 5,343,319 (Moore) 30 August 1994 See Fig. 1 Cols. 3-8	7-8,11-12, 22-23, and 30-31
Y	US, A, 5,088,023 (Nakamura et al.) 11 February 1992 See Fig. 1 Cols. 3-8	1-3 and 24-26
A	WO 92/07317 (REDDY) 30 April 1992, see entire published PCT application.	1-31

Form PCT/ISA/210 (continuation of second sheet)(July 1992)*

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Vorbach, Martin	
Application No.: 13/653,639	Art Unit: 2116
Filed: 10-17-2012	
Title: METHODS AND DEVICES FOR TREATING AND PROCESSING DATA	Examiner: ELAMIN, ABDELMONIEM I
Attorney Docket No.: PACT-025-PCT- US-D1-2C1	Conf. #: 6103

Electronically Filed
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Information Disclosure Statement

Dear Sir:

Pursuant to 37 C.F.R § 1.56, § 1.97, and § 1.98, the Examiner's attention is hereby directed to the references cited on the attached PTO/SB/08A forms.

The listed documents include references cited in Altera's Invalidity Contentions and Document Production Pursuant to Patent Local Rules 3-3 and 3-4, served on January 5, 2015 and Altera's

Preliminary Election of Asserted Prior Art, served on January 12, 2015 in the concurrent litigation Altera Corporation v. PACT XPP Technologies, AG, Case No. Case 3:14-cv-02868-JD (N.D. Ca.) involving U.S. Patent Nos. 5,943,242, 6,859,869, 7,565,525, 6,338,106, 6,513,077 and 6,119,181.

Copies of references in compliance with the requirements of 37 CFR § 1.98(a)(2) are enclosed except the references listed below. The copies of these references below will be submitted as they become available to Applicant(s).

- Algotronix, Ltd. , “CAL 64K Datasheet”, Algotronix, Ltd. (Apr. 6, 1989).
- Rambus Inc. , “Rambus FPGA Proposal”, Rambus Inc. (Jan. 4, 1994).
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- Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, IEEE Computer Society Technical Committee on Computer Architecture, April 19, 1995.

The copies of the references listed below are subject to a Stipulated Protective Order dated 11/21/2014. Further, they are highly confidential to plaintiff Altera Corporation, not to defendant PACT XPP Technologies, AG, applicant herein. Pursuant to the protective order, neither PACT XPP Technologies, nor their patent prosecution counsel, may have access to these materials.

- *ARM, "AMBA: Advanced Microcontroller Bus Architecture Specification", Advanced RISC Machines, Ltd., Document No. ARM IHI 0001C, Sep. 1995.*
- *Algotronix, Ltd. , "CAL 4096 Datasheet", Algotronix, Ltd. (1992).*
- *Altera Corporation , "Chipdata, Database Information for z1120a", Altera Corporation, Sept. 11, 2012.*

April 1, 2015

Respectfully Submitted,

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Attorney/Agent for
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		13653639	
	Filing Date		2012-10-17	
	First Named Inventor	Martin Vorbach		
	Art Unit	2116		
	Examiner Name	ELAMIN, ABDELMONIEM I		
	Attorney Docket Number	PACT-025-PCT-US-D1-2C1		

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13653639
Filing Date	2012-10-17
First Named Inventor	Martin Vorbach
Art Unit	2116
Examiner Name	ELAMIN, ABDELMONIEM I
Attorney Docket Number	PACT-025-PCT-US-D1-2C1

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Application Number	13653639
Filing Date	2012-10-17
First Named Inventor	Martin Vorbach
Art Unit	2116
Examiner Name	ELAMIN, ABDELMONIEM I
Attorney Docket Number	PACT-025-PCT-US-D1-2C1

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Application Number:	13653639
International Application Number:	
Confirmation Number:	6103
Title of Invention:	METHODS AND DEVICES FOR TREATING AND PROCESSING DATA
First Named Inventor/Applicant Name:	Martin VORBACH
Customer Number:	73481
Filer:	Edward Peter Heller/Emi Rhodes
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Attorney Docket Number:	PACT-025-PCT-US-D1-2C1
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Application Type:	Utility under 35 USC 111(a)

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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Non Patent Literature	2-01- The_Programmable_Logic_Data_Book_1994_PG262_ALTR00274632.pdf	18146616 dbc7438cd4e4c3316a9f02f329d5097af3a6c4a	no	262

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2	Non Patent Literature	2-02a- The_Programmable_Logic_Data_Book_1996_PG999_ALTR00274894_compressed.pdf	11905608 74fba866d42e43e0c5849546e49c535676c2d063	no	909
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3	Non Patent Literature	2-03- The_XC6200_FastMap_Processor_Interface_ALTR00268249.pdf	319259 52ea94970c055db8383e0256e52ff8deaeda02b8	no	8
Warnings:					
Information:					
4	Non Patent Literature	2-04a- TMS320C80_MVP_Parallel_Processor_Users_Guide_ALTR00271097.pdf	23948012 1f783ece24ec838d12428a45f37879cc5a63fb1a	no	705
Warnings:					
Information:					
5	Non Patent Literature	2-05-TMS320C8x_System-Level_Synopsis_ALTR00271802.pdf	8284377 dabac06e8fd5e9d95ac7ae4c66634561dbcb1f75	no	75
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Information:					
6	Non Patent Literature	2-06- XC6200_Field_Programmable_Gate_Arrays_June_1_1996_ALTR00274598.pdf	1828224 f0c00b9d46fe36df9f58036f905863a2f175784f	no	34
Warnings:					
Information:					
7	Non Patent Literature	2-07- XC6200_Field_Programmable_Gate_Arrays_Apr-_24_1997_ALTR00278601.pdf	4748849 a65f3f66dda34414d1c496a253a3fac2298e5087	no	73
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Information:					
8	Non Patent Literature	2-09- Universal_Asynchronous_Receiver_Transmitter_a16450_September_1996_ver-_1_ALTR00283177.pdf	479775 9daa641e54dd2537b1db30d19a927017220b6a4d	no	15
Warnings:					
Information:					
9	Non Patent Literature	2-10- Asynchronous_Communications_Interface_Adapter_a6850_September_1996_ver-_1_ALTR00283118.pdf	630101 5fc00af2213b62b61e093eed0511e532e52b7f54	no	14
Warnings:					
Information:					

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			687b551c8565882ce778ea84d1d0a36b8bd8958f		
Warnings:					
Information:					
11	Non Patent Literature	2-12- A_Plug_and_Play_Interface_Us ing_Xilinx_FPGAs_ALTR002785 61.pdf	1857296	no	40
			132abe886b0dc93bedfb99b45440830cec86624a		
Warnings:					
Information:					
12	Non Patent Literature	2-13-16-Tap_8- Bit_FIR_Filter_Applications_Gui de_ALTR00269482.pdf	356856	no	5
			214b335c39fd7f46ac8610594e21b4d9f7158160		
Warnings:					
Information:					
13	Non Patent Literature	2-14- A_1-5_GIPS_Video_Signal_Proc essor_VSP_ALTR00274449.pdf	320676	no	4
			427467b5e959cc21ecc89b3c1206325792834cd3		
Warnings:					
Information:					
14	Non Patent Literature	2-15-A_2-4GOPS_Data- Driven_Reconfigurable_Multipr ocessor_IC_for_DSP_ALTR0027 5811.pdf	316277	no	3
			271ab7b4a1d4de114527fa6efe5e56d088711ff7		
Warnings:					
Information:					
15	Non Patent Literature	2-16- A_32x16_Reconfigurable_Corr elator_for_the_XC6200_ALTR0 0268335.pdf	788129	no	14
			2f2160dfc1d3a93aab0bf3268e0bf819c53c6c59		
Warnings:					
Information:					
16	Non Patent Literature	2-17-A_Data- Driven_Multiprocessor_Archite cture_for_ALTR00275814.pdf	7786113	no	164
			c7e4960a6e71ad51c1f8e10a648103ac8f0998a9		
Warnings:					
Information:					
17	Non Patent Literature	2-18-A_Data- Driven_VLSI_Array_for_Arbitrar y_Algorithms_ALTR00269666. pdf	1238727	no	14
			fd44f7c5a13785a8bb81beade12e5a04d06e8671		
Warnings:					
Information:					
18	Non Patent Literature	2-19- A_Fast_Constant_Coefficient_ Multiplier_ALTR00274461.pdf	314702	no	5
			68c39d03d8653d2de0de3958f4c80c809c998704		
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19	Non Patent Literature	2-20- A_Multiprocessor_DSP_System _Using_PADDI_-2_ALTR002710 93.pdf	695835 bcc604c23a976c7b89e1ff458c324004ddff ea93	no	4
Warnings:					
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20	Non Patent Literature	2-21- A_Reconfigurable_Multiproces sor_IC_for_Rapid_Prototyping_ ALTR00268239.pdf	779366 0bf1e1bc8387fd30c91559cf7a86ca08b752 80f	no	10
Warnings:					
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21	Non Patent Literature	2-22- A_Survey_of_Microcellular_Res earch_ALTR00269689.pdf	3093698 5325bdfc7e783e7a072d53cceb7454fbc885 150f	no	39
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Warnings:					
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Warnings:					
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26	Non Patent Literature	2-27- APRIL_A_Processor_Architectur e_for_Multiprocessing_ALTR00 264157.pdf	1161461 eda48eb6994c8b3fcd1bf6061139049c8591 508e	no	11
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Warnings:					
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28	Non Patent Literature	2-29- Colt_An_Experiment_in_Worm hole_Run- Time_Reconfiguration_ALTR00 268026.pdf	775913 6f22b00fb1fcc05baf9f73a7439102ec1d4e6 c1d	no	9
Warnings:					
Information:					
29	Non Patent Literature	2-30- Complex_Digital_Waveform_G enerator_ALTR00270208.pdf	98883 300baafe50e2a4e645f4388460751f5cc017 9b1d	no	2
Warnings:					
Information:					
30	Non Patent Literature	2-31- Dynamic_Reconfiguration_ALT R00264172.pdf	172875 8c39fe9d95e3891bacd72cf9a14b23d767c4 9815	no	2
Warnings:					
Information:					
31	Non Patent Literature	2-32a-Field- Programmable_Devices_1_ALT R00262028.pdf	15502596 bf81c0c12867cf36019e3447dd13dac1c1cc 1693	no	122
Warnings:					
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32	Non Patent Literature	2-32b-Field- Programmable_Devices_1_ALT R00262028.pdf	16995490 21b2ff14a3262ee4edad4bbfc96764c14512 3e4c	no	128
Warnings:					
Information:					
33	Non Patent Literature	2-33- Field_Programmable_Gate_Arr ays_ALTR00269074.pdf	21671026 61f6ea922e6e5fb2292a88de274ebc432e56 0910	no	219
Warnings:					
Information:					
34	Non Patent Literature	2-34- Field_Programmable_Gate_Arr ays_AT6000_Series_ALTR00266 710.pdf	726226 b747fba9c8877c39f4edc14f8abf79ab7538 5eed	no	16
Warnings:					
Information:					
35	Non Patent Literature	2-35a- Field_Programmable_Gate_Arr ays_FPGAs_ALTR00262277.pdf	20422085 d21a0ed4c34eb14664cb215790f46ce1ad4 9784b	no	103
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36	Non Patent Literature	2-35b- Field_Programmable_Gate_Arr ays_FPGAs_ALTR00262277.pdf	14580699 cfd5c01a5753af771e037ff7a45082b07360 d4f9	no	132
Warnings:					
Information:					
37	Non Patent Literature	2-36-Field- Programmable_Gate_Array_Te chnology_ALTR00272487.pdf	13808450 aff73dbe8c0c5dcdb6f40af7b4d7ff5f9f0278 7d	no	274
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38	Non Patent Literature	2-37-Field- Programmable_Logic_Architec tures_Synthesis_and_Applicati ons_ALTR00269501.pdf	873421 54f2b64b5d1568aa0fcbe797ef609acaa6da ee58	no	14
Warnings:					
Information:					
39	Non Patent Literature	2-38a- FPGAs_for_Custom_Computin g_Machines_ALTR00262745. pdf	21481874 41a39ba039d212870b5308381bade47bf20 e5194	no	111
Warnings:					
Information:					
40	Non Patent Literature	2-38b- FPGAs_for_Custom_Computin g_Machines_ALTR00262745. pdf	20738972 2d9bbb696d0fbe159e27a3d5c17f6a9f634f 0915	no	126
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41	Non Patent Literature	2-39- High_Performance_Low_Area_ Interpolator_Design_for_the_X C6200_ALTR00268274.pdf	594980 5b2123005eb4ffaa8013cc584fa6322f92578 518	no	10
Warnings:					
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42	Non Patent Literature	2-40a- IEEE_Symposium_on_FPGAs_f or_Custom_Computing_Machi nes_ALTR00262511.pdf	9663094 49c4c05e94baee6d9c4260b62efe5b61a8d 6e231	no	234
Warnings:					
Information:					
43	Non Patent Literature	2-41- Issues_in_wireless_video_codi ng_using_run-time- reconfigurable_FPGAsALTR002 76174.pdf	2635355 39e0cf2a16c5f6cc220e7ca8bbfb825d8e9a 041d	no	5
Warnings:					
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44	Non Patent Literature	2-42a- More_FPGAs_ALTR00269728. pdf	17746478 25c046c6640b13afbfbf1ded0b424cac877 daef5	no	149

Warnings:					
Information:					
45	Non Patent Literature	2-42b- More_FPGAs_ALTR00269728. pdf	18225906 d044f5eeda74eadb476b43624748ca24c819dd49	no	154
Warnings:					
Information:					
46	Non Patent Literature	2-42c- More_FPGAs_ALTR00269728. pdf	20657028 0639991811addb6b83a740f3204977e834a0fada	no	175
Warnings:					
Information:					
47	Non Patent Literature	2-43-New_SRAM- Based_FPGA_Architectures_Ad dress_New_Applications_ALTR 00268689.pdf	650508 4f834d6b0743f0adff4e2477ceab2b6ab5548dd4	no	6
Warnings:					
Information:					
48	Non Patent Literature	2-44- Proceedings_of_the_4th_Cana dian_Workshop_on_Field- Programmable_Devices_ALTR0 0263542.pdf	22465619 c1f66fb14ffaebb7d11a2cb687c86fac970dd6ee4	no	181
Warnings:					
Information:					
49	Non Patent Literature	2-45- Programmable_Arithmetic_De vices_for_High_Speed_Digital_ Signal_Processing_ALTR00268 045.pdf	7144435 a666b467dec47f8bdddd733cf8322d264c8b0d36	no	194
Warnings:					
Information:					
50	Non Patent Literature	2-46- The_Function_Processor_A_Da ta- Driven_Processor_Array_ALTR0 0274433.pdf	1280373 2ddf4b9c7acaec0690e2fe24a48a40e9fb91a9a2	no	16
Warnings:					
Information:					
51	Non Patent Literature	2-47- TUTCA_configurable_logic_cell _array_architecture_ALTR0027 2768.pdf	289585 497dfd965724beb51daefd5f9f6a1e03cab4a8ab	no	4
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52	Information Disclosure Statement (IDS) Form (SB08)	PACT-025-PCT-US- D1-2C1_150401_PTOSB08a_2. pdf	615279 1c88b2d6a64204c3831f45ebaf1de024d2efbe22	no	8
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	Filing Date		2012-10-17	
	First Named Inventor	Martin Vorbach		
	Art Unit	2116		
	Examiner Name	ELAMIN, ABDELMONIEM I		
	Attorney Docket Number	PACT-025-PCT-US-D1-2C1		

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Attorney Docket Number	PACT-025-PCT-US-D1-2C1

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Attorney Docket Number	PACT-025-PCT-US-D1-2C1

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	Filing Date		2012-10-17
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	Art Unit	2116	
	Examiner Name	ELAMIN, ABDELMONIEM I	
	Attorney Docket Number	PACT-025-PCT-US-D1-2C1	

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Filing Date	2012-10-17
First Named Inventor	Martin Vorbach
Art Unit	2116
Examiner Name	ELAMIN, ABDELMONIEM I
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Application Number:	13653639
International Application Number:	
Confirmation Number:	6103
Title of Invention:	METHODS AND DEVICES FOR TREATING AND PROCESSING DATA
First Named Inventor/Applicant Name:	Martin VORBACH
Customer Number:	73481
Filer:	Edward Peter Heller/Emi Rhodes
Filer Authorized By:	Edward Peter Heller
Attorney Docket Number:	PACT-025-PCT-US-D1-2C1
Receipt Date:	01-APR-2015
Filing Date:	17-OCT-2012
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Application Type:	Utility under 35 USC 111(a)

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2	Non Patent Literature	3-02- Unifying_FPGAs_and_SIMD_Ar rays_ALTR00268035.pdf	937006	no	10
			c8907d2d5dfdb58fcd5b57b0747e62263b12428		
Warnings:					
Information:					
3	Non Patent Literature	3-03- Using_Programmable_Logic_t o_Accelerate_DSP_Functions_ ALTR00269658.pdf	647120	no	8
			9bdc3f5b9ff8a42d57541b1642dca595d5ab8bbd		
Warnings:					
Information:					
4	Non Patent Literature	3-04- Using_the_Dedicated_Carry_L ogic_in_XC4000_ALTR0027021 4.pdf	630391	no	11
			f2e801fa7a4945ed14fde47ada0c0ee08d2f1bfe		
Warnings:					
Information:					
5	Non Patent Literature	3-05- Using_the_XC4000_RAM_Capa bility_ALTR00269632.pdf	688055	no	12
			a9ebb7f64b5227feb477b00bf86a25c77e36f7c1		
Warnings:					
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6	Non Patent Literature	3-06a- IEEE_Workshop_on_FPGAs_for _Custom_Computing_Machine s_ALTR00263233.pdf	21859651	no	100
			2522b799e85e3903f2019cb93b3f53bf03f355f8		
Warnings:					
Information:					
7	Non Patent Literature	3-06b- IEEE_Workshop_on_FPGAs_for _Custom_Computing_Machine s_ALTR00263233.pdf	24156704	no	112
			37acd726567ad5754eacb769cdea39beeca4ec6e		
Warnings:					
Information:					
8	Non Patent Literature	3-07- A_3-84_GIPS_Integrated_Mem ory_Array_Processor_ALTR002 75803.pdf	673507	no	8
			c6a3042c79706fcb75520d0a4f6118fa9e2b1818		
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9	Non Patent Literature	3-09- A_Multiprocessor_Implementa tion_of_a_Wavelet_Transforms _ALTR00264150.pdf	806625	no	7
			8e842e2f457cc04ea6d0c90d7cf2bc9dd87a7e2d		
Warnings:					
Information:					
10	Non Patent Literature	3-10-Altera_ships_100000- gate_EPLD_ALTR00268352.pdf	1619535	no	3
			960880187c16725152b68655ac2760a4fb20db61		
Warnings:					
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11	Non Patent Literature	3-12- Embedded_Programmable_Logic_Family_Data_Sheet_1995- ALTR00269293.pdf	1794754 e70f6fc1407634c2541c188989c1c776e800805f	no	56
Warnings:					
Information:					
12	Non Patent Literature	3-13-FLEX_10K_100000- Gate_Embedded_Array_Programmable_Logic_Family_ALTR00266414.pdf	3864677 f6a481a57c53e58104be22a0a900d067993ac8ec	no	28
Warnings:					
Information:					
13	Non Patent Literature	3-14- Implementing_Multipliers_in_FLEX_10K_Devices_ALTR00264413.pdf	829321 47c055869c8445de794bcb2441d448ac0a15f87a	no	8
Warnings:					
Information:					
14	Non Patent Literature	3-15- Intel_82375EB-82375SB_PCI-EISA_Bridge_PCEB_Advance_Information_ALTR00276470.pdf	6205040 6b7899cdd2543743b7dd51c6241ef0e5496c1d6	no	132
Warnings:					
Information:					
15	Non Patent Literature	3-17a- Proceedings_of_the_Parallel_Systems_Fair_ALTR00263444.pdf	23502320 208fe32005175e744dbf80486b8a162bbef191c	no	98
Warnings:					
Information:					
16	Non Patent Literature	3-18a- Proceedings_of_the_Workshop_on_Reconfigurable_Architectures_ALTR00262981.pdf	25808539 cb705c7369c1415ea07fd0bee89a86249416b8b0	no	159
Warnings:					
Information:					
17	Non Patent Literature	3-19a- The_Programmable_Logic_Conference_Exhibit_Proceedings_ALTR00263901.pdf	15612955 00bb7d446a1c8a433a962a92451e546d17114038	no	103
Warnings:					
Information:					
18	Non Patent Literature	3-19b- The_Programmable_Logic_Conference_Exhibit_Proceedings_ALTR00263901.pdf	19610058 5843da850496c298f9348de5d3cb363918d50864	no	131
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Warnings:					
Information:					
20	Non Patent Literature	3-21-Special_Purpose_Processor_Speeds_up_DSP_Functions_ALTR00269680.pdf	529302 09bfd3c9663c2648ed15be53dbd5a193822e96e6	no	9
Warnings:					
Information:					
21	Non Patent Literature	4-01-ALTR00263140.pdf	6818688 7a47bede601a2794ee08eb9f1adee8080383e74b	no	93
Warnings:					
Information:					
22	Non Patent Literature	4-02a-ALTR00266726_ATMEL.pdf	22058344 58386efc3ec7071be18b1c7cbb62cfd64edd9dd	no	206
Warnings:					
Information:					
23	Non Patent Literature	4-02b-ALTR00266726_ATMEL.pdf	19837125 bdadfa7aaa1c910125134530b7104c945cfb4db	no	205
Warnings:					
Information:					
24	Non Patent Literature	4-02c-ALTR00266726_ATMEL.pdf	19140255 8a6e5245dc45857b502de00ca737aca5b96c4f44	no	200
Warnings:					
Information:					
25	Non Patent Literature	4-03a-ALTR00267335_ATMEL2.pdf	23937163 5ce9f7eb9c0617d14252163afb142211bfa8428b	no	222
Warnings:					
Information:					
26	Non Patent Literature	4-03b-ALTR00267335_ATMEL3.pdf	24183882 28a99e47fef656b0afdf685daa2e9b5e7f52d278b	no	221
Warnings:					
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27	Non Patent Literature	4-03c-ALTR00267335_ATMEL2.pdf	25059557 b3fdc7e26a31e583503f172727d348d7873dc8e8	no	245
Warnings:					
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28	Non Patent Literature	4-04-ALTR00268645.pdf	2731271 8e13268874d2677b1e45e6a0e4e0c7c793c77d7	no	44

Warnings:					
Information:					
29	Non Patent Literature	4-05-ALTR00269478.pdf	259817	no	4
			6562420fe9fb7d152f009d728220fce7484c161		
Warnings:					
Information:					
30	Non Patent Literature	4-06a-ALTR00279005_Altera1998DataBook.pdf	23970919	no	914
			2095d1d196da4aca84a5f78f6a71c8b50654d118		
Warnings:					
Information:					
31	Non Patent Literature	4-07-ALTR00280032_AlteraFlex10KEmbeddedProgrammableLogicFamily1998.pdf	3861876	no	125
			5980e824fad26fe5c9ad269ff6226a5bf0d64ab		
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32	Non Patent Literature	4-08-ALTR00280157_AlteraImplementingRAMFunctions_1995.pdf	301806	no	8
			3e9c1daf806dd6b6c6bd9899e875c5b0c2d56978		
Warnings:					
Information:					
33	Non Patent Literature	4-09-ALTR00280165_Altera1993DataBook.pdf	21979378	no	565
			62065b1f45a048c575cecac6d9eaddb87f8e8858		
Warnings:					
Information:					
34	Non Patent Literature	4-10-ALTR00280730_Altera1995DataBook.pdf	24567950	no	688
			79892390f486022aab4ce61f933fbd7b97ab6681		
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35	Non Patent Literature	4-11-ALTR00281418.pdf	1538197	no	24
			69098589bc244683e9911159e5b38a6609ffc293		
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Information:					
36	Non Patent Literature	4-12-ALTR00281442.pdf	787825	no	20
			8d97a0f5bd6745b94d4a1571c223f1597bd1e660		
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Information:					
37	Non Patent Literature	4-13- ALTR00281462_AlteraFlex8000 Handbook.pdf	9602973 b898ebe1d19650bd4f2926b7888b0fc8c8 253e3	no	234
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38	Information Disclosure Statement (IDS) Form (SB08)	PACT-025-PCT-US- D1-2C1_150401_PTOSB08a_3. pdf	614441 d6ef7921889f1506a0822890c357673210bc 7451	no	7
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Emi Rhodes	(Depositor's name)
/Emi Rhodes/	(Signature)
April 14, 2015	(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/653,639	10/17/2012	Martin VORBACH	2885/162	6103

TITLE OF INVENTION: METHODS AND DEVICES FOR TREATING AND PROCESSING DATA

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$480	\$0	\$0	\$480	07/01/2015

EXAMINER	ART UNIT	CLASS-SUBCLASS
ELAMIN, ABDELMONIEM I	2116	713-300000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Edward P. Heller III

2 _____

3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

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(B) RESIDENCE: (CITY and STATE OR COUNTRY)

PACT XPP TECHNOLOGIES AG

Munich, Germany

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

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Authorized Signature /Edward P. Heller III/

Date April 14, 2015

Typed or printed name Edward P. Heller III

Registration No. 29,075

Electronic Patent Application Fee Transmittal

Application Number:	13653639			
Filing Date:	17-Oct-2012			
Title of Invention:	METHODS AND DEVICES FOR TREATING AND PROCESSING DATA			
First Named Inventor/Applicant Name:	Martin VORBACH			
Filer:	Edward Peter Heller/Emi Rhodes			
Attorney Docket Number:	PACT-025-PCT-US-D1-2C1			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Utility Appl Issue Fee	1501	1	960	960
Publ. Fee- Early, Voluntary, or Normal	1504	1	0	0
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				960

Electronic Acknowledgement Receipt

EFS ID:	22056869
Application Number:	13653639
International Application Number:	
Confirmation Number:	6103
Title of Invention:	METHODS AND DEVICES FOR TREATING AND PROCESSING DATA
First Named Inventor/Applicant Name:	Martin VORBACH
Customer Number:	73481
Filer:	Edward Peter Heller/Emi Rhodes
Filer Authorized By:	Edward Peter Heller
Attorney Docket Number:	PACT-025-PCT-US-D1-2C1
Receipt Date:	14-APR-2015
Filing Date:	17-OCT-2012
Time Stamp:	14:54:49
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$960
RAM confirmation Number	1276
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Page 569 of 635

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1	Issue Fee Payment (PTO-85B)	PACT-025-PCT-US-D1-2C1_150414_PIF.pdf	106800	no	1
			d7b01c1389f8d9ebe73bd0f09c6aaa4ea9bd62ee		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	32380	no	2
			825aa2a01ffdfa00d01bcb770f73646992e755db		
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	Applicant(s) VORBACH et al.	
	Filing Date Herewith	Group Art Unit Unassigned

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	Applicant(s) VORBACH et al.	
	Filing Date Herewith	Group Art Unit Unassigned

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						YES	NO
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	Filing Date Herewith	Group Art Unit Unassigned

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	Applicant(s) VORBACH et al.	
	Filing Date Herewith	Group Art Unit Unassigned

EXAMINER'S INITIALS	AUTHOR, TITLE, DATE, PERTINENT PAGES, ETC.
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EXAMINER	DATE CONSIDERED
/Abdelmoniem Elamin/	12/16/2012
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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/653,639	10/17/2012	Martin VORBACH	PACT-025-PCT-US-D1-2C1	6103
73481	7590	05/18/2015		
Alliacense Limited LLC 4880 Stevens Creek Boulevard Suite 103 San Jose, CA 95129			EXAMINER ELAMIN, ABDELMONIEM I	
			ART UNIT	PAPER NUMBER
			2116	
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13/653,639	17 October, 2012	VORBACH ET AL.	PACT-025-PCT-US-D1-

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/ABDELMONIEM ELAMIN/
Primary Examiner, Art Unit 2116

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49	Xilinx, Inc. , "Technical Data - XC5200 Logic Cell Array Family, Preliminary, v.1.0", Xilinx, Inc., (Apr. 1995).	☐
50	Xilinx, Inc. , "The Programmable Logic Data Book (1993)", Xilinx, Inc. (1993).	☐

If you wish to add additional non-patent literature document citation information please click the Add button [Add](#)

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.E./

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	13653639
Filing Date	2012-10-17
First Named Inventor	Martin Vorbach
Art Unit	2116
Examiner Name	ELAMIN, ABDELMONIEM I
Attorney Docket Number	PACT-025-PCT-US-D1-2C1

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.E./

EXAMINER SIGNATURE

Examiner Signature	/Abdelmoniem Elamin/	Date Considered	05/13/2015
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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/653,639	10/17/2012	Martin VORBACH	PACT-025-PCT-US-D1-2C1	6103

73481 7590 06/12/2015
Alliacense Limited LLC
4880 Stevens Creek Boulevard
Suite 103
San Jose, CA 95129

EXAMINER

ELAMIN, ABDELMONIEM I

ART UNIT	PAPER NUMBER
----------	--------------

2116

NOTIFICATION DATE	DELIVERY MODE
-------------------	---------------

06/12/2015

ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

emi@alliacense.com
ip@alliacense.com
ned@alliacense.com

**UNITED STATES DEPARTMENT OF COMMERCE****U.S. Patent and Trademark Office**

Address : COMMISSIONER FOR PATENTS

P.O. Box 1450

Alexandria, Virginia 22313-1450

APPLICATION NO./ CONTROL NO.	FILING DATE	FIRST NAMED INVENTOR / PATENT IN REEXAMINATION	ATTORNEY DOCKET NO.
13/653,639	17 October, 2012	VORBACH ET AL.	PACT-025-PCT-US-D1-

2C1

Alliacense Limited LLC 4880 Stevens Creek Boulevard Suite 103 San Jose, CA 95129		EXAMINER	
		ABDELMONIEM ELAMIN	
		ART UNIT	PAPER
		2116	20150609

DATE MAILED:

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner for Patents

correcting an error PTO 1449 dated 05/18/2015, on page 1 of 15, citaions 1 and 2 (missing digits)

/ABDELMONIEM ELAMIN/
Primary Examiner, Art Unit 2116



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P.O. Box 1450
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www.uspto.gov

APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
13/653,639	07/07/2015	9075605	PACT-025-PCT-US-D1-2C1	6103

73481 7590 06/17/2015
Alliacense Limited LLC
4880 Stevens Creek Boulevard
Suite 103
San Jose, CA 95129

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 0 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

Martin VORBACH, Lingenfeld, GERMANY;
Volker BAUMGARTE, Munchen, GERMANY;
PACT XPP TECHNOLOGIES AG, Munchen, GERMANY

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**UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION**Page 1 of 1

PATENT NO. : 9,075,605

APPLICATION NO.: 13/653,639

ISSUE DATE : July 7, 2015

INVENTOR(S) : Martin Vorbach, Volker Baumgarte

It is certified that an error appears or errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In Claim 1, column 15, line 8:

delete "cells" and insert --units--

MAILING ADDRESS OF SENDER (Please do not use Customer Number below):

Aaron Grunberger
Norton Rose Fulbright US LLP
1301 Avenue of the Americas, New York, NY 10019-6022

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.

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The **Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (*i.e.*, GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Letters Patent of : Scientia Sol Mentis AG

Patent No. : 9,075,605

Issue Date : July 7, 2015

For : METHODS AND DEVICES FOR TREATING AND
PROCESSING DATA

I hereby certify that this paper (along with any paper referred to as being attached or enclosed) is being transmitted via the Office electronic filing system in accordance with 37 CFR § 1.6(a)(4). Dated: <u>December 5, 2018</u> Signature: <u>/Farieza Juman/</u> Farieza Juman

**REQUEST FOR CERTIFICATE OF CORRECTION AND A REQUEST FOR
EXPEDITED ISSUANCE OF CERTIFICATE OF CORRECTION
PURSUANT TO 37 C.F.R. § 1.323**

Attention: Certificate of Correction Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Commissioner:

Please correct the typographical error in Claim 1 of the above-identified Letters Patent as shown below.

Please correct the error in the first sentence of Claim 1
from

“A method for operating a multiprocessor system comprising a plurality of data processing cells, each of the plurality of data processing units (a) including at least one Arithmetic Logic Unit (ALU) and a register unit and (b) being adapted for sequentially processing data, the method comprising:”

to

--A method for operating a multiprocessor system comprising a plurality of data processing units, each of the plurality of data processing units (a) including at least one Arithmetic Logic Unit (ALU) and a register unit and (b) being adapted for sequentially processing data, the method comprising:--

Transmitted herewith is a proposed Certificate of Correction form PTO/SB/44 effecting such amendment. Patentee respectfully solicits the expedited granting of the requested Certificate of Correction.

The Certificate of Correction fee of \$150.00 set forth in 37 C.F.R. § 1.20(a) is being charged to the Deposit Account of Norton Rose Fulbright US LLP Deposit Account number 50-0624.

The Commissioner is also hereby authorized to charge payment of any other fees or credit any overpayment associated with this paper to the deposit account of Norton Rose Fulbright US LLP Deposit Account number 50-0624.

Dated: December 5, 2018

By: /Aaron Grunberger/
Aaron Grunberger (Reg. No. 59,210)
NORTON ROSE FULBRIGHT US LLP
1301 Avenue of the Americas
New York, New York 10019-6022
Tel: (212) 318-3000
Fax: (212) 318-3400
CUSTOMER NO. 24972

Electronic Patent Application Fee Transmittal

Application Number:	13653639			
Filing Date:	17-Oct-2012			
Title of Invention:	METHODS AND DEVICES FOR TREATING AND PROCESSING DATA			
First Named Inventor/Applicant Name:	Martin VORBACH			
Filer:	Aaron Grunberger/Farieza Juman			
Attorney Docket Number:	PACT-025-PCT-US-D1-2C1			
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
CERTIFICATE OF CORRECTION	1811	1	150	150

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				150

Electronic Acknowledgement Receipt

EFS ID:	34492171
Application Number:	13653639
International Application Number:	
Confirmation Number:	6103
Title of Invention:	METHODS AND DEVICES FOR TREATING AND PROCESSING DATA
First Named Inventor/Applicant Name:	Martin VORBACH
Customer Number:	73481
Filer:	Aaron Grunberger/Farieza Juman
Filer Authorized By:	Aaron Grunberger
Attorney Docket Number:	PACT-025-PCT-US-D1-2C1
Receipt Date:	05-DEC-2018
Filing Date:	17-OCT-2012
Time Stamp:	14:07:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 150
RAM confirmation Number	120618INTEFSW00012197500624
Deposit Account	500624
Authorized User	Farieza Juman

The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows:
37 CFR 1.21 (Miscellaneous fees and charges)

INTEL - 1004

Page 633 of 635

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Request for Certificate of Correction	PACT_SB-44.pdf	166106	no	2
			28f54402231236bd4f0508cce5273b92b4d b987d		
Warnings:					
Information:					
2	Request for Certificate of Correction	PACT_Transmittal-Certificate-of-CorrectionI.pdf	102872	no	2
			76a3b1e180b26ed85724e2c76858f13a6f9 663cc		
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30456	no	2
			1094c6f9c7aa9a7e34585cdc2ad26c189eff 493		
Warnings:					
Information:					
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO. : 9,075,605 B2
APPLICATION NO. : 13/653639
DATED : July 7, 2015
INVENTOR(S) : Martin Vorbach and Volker Baumgarte

Page 1 of 1

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the Claims

In Claim 1, Column 15, Line 8:
Delete "cells" and insert --units--

Signed and Sealed this
First Day of January, 2019



Andrei Iancu
Director of the United States Patent and Trademark Office