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memory systems. There is a page descriptor for each page represented by at least one cache line in an second-level cache.

In a preferred embodiment of the invention, the interconnection between a second-level and the third-level is a fiber optic connection between the
5 multiprocessor modules 1A,...,1M and the third-level modules 40a,...,40m. Preferably, each third-level module 40 has a four or eight port connector, allowing up to four and eight multiprocessor modules 1 and third-level modules 40, respectively.

In another preferred embodiment, the interconnection is a shared bus between
10 third-level modules 40. The shared bus can also be used to interconnect the multiprocessor modules 1A,...,1M to the third-level modules 40a,...,40m. In that case, each multiprocessor module 1 is coupled to one third-level module 40, although multiple multiprocessor modules 1 can share a single third-level module 40. FIG. 6 is a block diagram of a third-level bus-based distributed shared-cache
15 memory system.

On a second-level cache miss going to the third-level, as previously described, the third-level interface first checks with the third-level directory 42 to see if the cache line is present in another second-level cache 18 in a different cluster. If so, the request is directed to a processor cluster containing the cache
20 line, which returns the data to satisfy the cache miss. The necessary consistency actions, such as transferring ownership, are performed at the same time. If the third-level directory cache 42 indicates the data is in the third-level memory area 46, the data is transferred from the third-level memory area 46, with cache tags in the cache directory entry being updated accordingly.

25 If the requested cache line is not present in the third-level directory cache 42, a software trap is taken by the processor 12 and a software look-up is performed using the translation table, mapping the physical address to the page descriptor. If the page descriptor is found, then the page descriptor describes the location of the data in DRAM memory. This software translation table is global across the third-
30 level modules 40a,...,40m, even though FIGs. 5 and 6 illustrate separate portions of

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third-level memory 46 per third-level module 40. If the data is retrieved from memory, the page descriptor is updated according to the consistency protocol. Also, a cache line entry is created in the third-level directory cache 42 for this cache line, possibly writing back an entry from this directory cache 42 to the associated page descriptor to make room for this new entry. The processor 12 then restarts the memory operation that caused the miss.

The look-up may determine that required data is in another of the third-level modules 40 from that associated with the faulting multiprocessor module 1. In that case, the third-level directory cache 42 in that third-level module 40 is loaded accordingly.

If the data is not present at the third-level at all, software allocates memory in the third-level module 40 associated with the faulting multiprocessor module 1 and transfers the data into this area of memory from a high-speed network connection, and then performs the actions described above. Thus, the software mimics the shared operation of the second level, where cache loads go to the portion of the cache of the requesting unit. Because the transfer from the network to the third level is done in software and it is advantageous to move this data immediately into the highest portion of the requesting units memory hierarchy, the network connection resides on the shared second-level cache bus 5. By placing the network connection on the shared second-level cache bus 5, the processor 12 is allowed to copy the data directly from the network interface to cache lines residing at the second-level.

There is a special form of a software page descriptor, referred to as a pageless page descriptor, which does not have a corresponding data page portion in DRAM memory. The page pool can convert a page descriptor into a pageless page descriptor and reclaim the associated data page area when the data of the page is contained in the second-level cache area 20. A scavenger process, similar to that used in conventional virtual memory systems, checks whether there have been any recent accesses to the data page and, if not, reclaims the data page and updates the directory cache 42 as appropriate. A processor may have to handle a write-back

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fault, which arises when a write-back occurs for a cache line having no third-level location recorded in the third-level directory cache 42.

The third-level memory area 46 is directly addressable as a portion of the physical address space. A reference to the third-level memory area 46 is detected at
5 the point of trap to a software process after a directory cache miss. A direct mapping to the memory for the cache line then takes place. Otherwise, access to this third-level memory area 46 is transparent to the processor 12 and handled in the directory and consistency mechanism, the same as other portions of memory. Each multiprocessor module 1 contains a local memory containing the software
10 instructions for third-level miss handling, so that a processor 12 never faults at the third-level on software instructions to handle third-level faults. Alternatively, software instructions to handle this miss handling can be provided in a memory module at the third level.

The directory cache 42 allows most third-level misses to be handled fast, by
15 retrieving the data either from another processor cluster or from the third-level memory area 46. By making the directory a cache, the cache directory 42 can support a very large physical address space without actually having that amount of physical memory. For example, a machine with less than a few hundred megabytes of data can support a physical address space addressed by 64 bits. Providing a very
20 large physical or shared address space allows the operating system to maximize the time between reuse of addresses. By maximizing the time between reuse of addresses, these addresses are meaningful over a longer period of time and confusion that can arise from reusing addresses quickly is minimized. Providing a directory large enough to hold entries covering the entire 64-bit physical address
25 space would be expensive.

In addition, preferred embodiments of the invention efficiently allow software control of the memory system at the cache line unit level. In particular, if a cache line of a page is not present locally, the software gains control and can retrieve the required cache line, even if the rest of the page is present locally.

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Furthermore, the software-managed page descriptor structure allows a more sophisticated management approach than is feasible with a pure hardware solution. In particular, a data page for every page descriptor is not required in preferred embodiments of the invention. Data pages can be used more for a prefetching and write-behind I/O storage, rather than primarily duplicating the second-level cache data entirely. Also, page descriptors can be used to refer to remote copies of the page. In addition, the global page descriptor data structure is used to ensure that there is only one copy of a page across all local third-level modules 40.

In another preferred embodiment of the invention, each third-level module 40 handles only one subset of the total processors in the node. For example, a directory cache entry may allow for only eight multiprocessor modules 1, by allowing eight M bits for multiprocessor module identification. However, the saving in M bits is not regarded as a significant benefit as a percentage of third-level directory cache entry size, and transferring ownership of cache lines between the third-level appears complicated.

In an alternative embodiment of the invention, the third-level modules 40 are divided based on an address range. While requiring no interaction between third-level modules 40, this embodiment leads to very uneven loads between modules depending on the distribution of the load on memory. This embodiment also requires every third-level module 40 to contain the maximum number of M bits per directory entry that any machine configuration would ever require.

In another preferred embodiment of the invention, the third-level modules 40 are divided based on the low-order bits of the page numbers. For example, with two third-level modules 40, the first module might handle all page addresses that are less than 4 modulo 8 whereas the other module handles all that are greater than or equal to 4 modulo 8. This embodiment distributes the load more evenly, but is more complicated and still limits the number of multiprocessor modules 1 in a configuration to the number of M bits in a third-level module 40.

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Page-Level Shared Cache System

FIG. 7 is a block diagram of a preferred distributed shared page cache memory system. A page cache is memory managed by the virtual memory system, largely in software but with some hardware assistance for address translation. In a preferred embodiment of the invention, the machine environment is a cluster of nodes 110a,...,110k connected by a high-speed network 100. Each node has a respective local DRAM memory module of several hundreds of megabytes or more. Pages are retrieved from a shared distributed file system, which stores pages on disk 200 connected to the high-speed network 100.

Each node 110 maintains a page frame pool 116 similar to that in conventional virtual memory systems. Each page is identified as a portion of a segment. Preferably, the pages are identified as in the V++ distributed system virtual memory system. This identification is global and uniquely identifying across the set of nodes sharing the file system. Each page frame pool 116 also maintains a list of pages resident at the other nodes in the network. Each such page is recorded as a special form of a standard page descriptor, referred to as a remote page descriptor. The page descriptors contain consistency information as required to support the third-level operation previously described, as well as for internode operation. The page descriptors are a natural extension of this level, and they are similar to that used in various distributed shared memory implementations.

Each page frame pool manager periodically multicasts the list of resident pages in the corresponding pool to the other nodes 110. On receiving such an update, a node 110 updates the list of pages at the sending node. The update can include specific mention of pages that have been discarded. In an alternative preferred embodiment, the page frame pool manager discards remote page descriptors after some time-out period without reconfirmation, or after requesting the page from a node 110 and discovering that the requested page is no longer present in that node.

On page look-up, the local process either finds a local page descriptor, a remote page descriptor, or no page descriptor. In the former case, the page data

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may be local and is satisfied immediately. However, because the cache line is the unit of consistency, that portion may have to be accessed from a remote node, which is described in a remote page descriptor 126. If a remote page descriptor 126 is found, the process requests the data from the node 110 identified by the remote page
5 descriptor 126. Otherwise, the page is requested from an appropriate disk subsystem 200 or file server 150, incurring the multi-millisecond cost of accessing the disk subsystems 200.

It is possible that the remote node from which the page is requested in the second case above has discarded the page. In that case, the remote node responds
10 negatively and the requesting node can remove the remote page descriptor 126 and then retry the operation.

The file server or disk server can have some page buffering and advertise the contents of associated caches. However, in a loaded system better performance can be obtained by limiting traffic to the file server 150 primarily to request requiring
15 disk I/O. By so limiting the traffic, page requests that can be satisfied from other nodes do not unnecessarily interfere with page requests that have to be handled by the server 150.

A page requestor may request a page from the file server 150 even though the page is present in another node's page frame pool 116, because the presence of
20 that page has not been propagated from the remote node to the requesting node. With a consistent file page caching protocol in place, it is necessary for the file server 150 to forward the request to a node with exclusive ownership of the cache line or the page. This type of redirect is feasible to handle in software and should not represent a performance problem provided that the redirection does not occur
25 frequently.

A preferred embodiment of a page-level shared-cache system provides the effect of having the totality of the page frame pools 116 forming a large shared-cache, which is much larger than the memory available on each node. In general, a page-level shared-cache system provides the advantages of the shared-cache among a

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set of network nodes, assuming that the network transfer time is substantially less than the disk transfer time, including latency.

An advantage of a preferred embodiment of a page-level shared-cache system is that the system allows pages to be duplicated at different nodes. The system
5 recognizes that even the network latency is significant for repeated second-level cache misses to the same page.

In a preferred embodiment of the invention, the page fault load is distributed from the file servers to other nodes. This distribution is important with point-to-point networks that appear to be a key aspect of future high-speed networking.
10 Rather than have all page requests congest the path from client nodes to server nodes, some of the requests are routed to clients, making better use of network resources and reducing congestion-induced delay. In a particular preferred embodiment of the invention, the requesting node takes the location and route to the node described by the remote page descriptor into consideration in selecting the node
15 from which to request when there are multiple nodes holding a page.

In addition, the dissemination of page frame pool 116 contents by best-efforts multicast avoids extra network loading, processing overhead, and extra latency in case of total miss of trying to apply the broadcast approach of the second-level cache to locating a page. With point-to-point networking, transmitting a multicast request
20 to every node as a result of a page fault can be a significant load during phases of significant page faulting. Because the page frame pool 116 is handled in software, each node incurs the cost of processing such a request. Moreover, because a page can be duplicated at several nodes, a multicast request can result in duplicate responses. In the case of a node requesting a page not present in any page frame
25 pool 116, the request must time-out before directing a request to the file server. Because time-outs with network and software processes have to be large to avoid unnecessary re-transmission, such a time-out adds significant delay to a page fault that requires going to disk.

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A preferred embodiment of a page-level shared-cache system also fits with the provision of extra page descriptors that have no corresponding data page, as introduced above with the third-level caching support.

Memory-based Messaging to Support

5 *Networking and Devices*

Parallel applications that use shared memory can benefit from high-performance communication. For example, if a program is structured such that processes allocate work from a shared work queue, it is more efficient in memory traffic for the processors to communicate by messages with a processor running this
10 allocator than trapping the code and data associated with the allocator into its cache and then executing the allocator itself, assuming that this processor is unlikely to have been the last to execute this allocator. That is, function shipping is intrinsically more efficient than data shipping in this case. Fast communication allows an application to effectively optimize for these situations rather than incur the
15 delay and memory overload of conventional shared memory techniques.

Large-scale memory systems can reduce communication performance because the cost of copying data in these machines increases, due to generally poor cache behavior of copying and the increasing ratio of processor speed to average memory access. Furthermore, maintaining shared-memory consistency semantics in
20 large-scale memory systems is increasingly costly due to increased memory latency. The cost of remapping data in multiprocessor systems also appears to be significantly greater than in uniprocessors because of the need to update or invalidate the TLBs, or page tables, in all processors. Moreover, the costs of queuing and notification become more significant in large-scale parallel machines. Consequently,
25 memory-based messaging techniques in these machines cause large amounts of memory contention on highly shared data structures, such as shared messages and message queues.

FIG. 8 is a block diagram of a multiprocessor module interfaced to an external device controller according to a preferred embodiment of the invention. A

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distributed shared cache can support high-performance device communication by allowing a device controller 160 to participate in the inter-cache protocol as a peer to the other local cache controllers 180 associated with data processors 12.

Particular examples of appropriate device controllers 160 include, but are not limited to, high-performance disk controllers for interfacing the processor cluster to a disk subsystem 200' and high-speed network interfaces for interfacing the processor cluster to other processor clusters 100' or a switch (not shown). It should be understood that other device controller can be used to interface with other computer peripherals.

10 As illustrated, the microprocessor module 1 includes an external interface port 165 that provides the device controller 160 with access to the second-level cache memory 188 via the shared bus 5. In particular, on read access to data at a given location, a device controller 160 requests the data from the peer-level local cache controllers 180 the same as if the device controller were a cache controller
15 whose associated processor 12 had missed an access to this data. On write to data, the device can similarly request ownership of the data from the peer-level cache controllers and update the data accordingly, directly updating the next level of memory if the data is not present in the peer-level cache memories.

In a particular embodiment, the distributed shared caches support a
20 memory-based messaging mode for cache line units. In particular, each cache line can be set in message mode as an alternative to one of the standard consistent shared memory modes of invalid, shared, or exclusively owned. A particular memory-based messaging technique is described in the above-referenced ParaDiGM architecture, which uses cache lines of shared memory as message buffers.

25 In a preferred embodiment, a memory segment is created to act as a communication channel, processes bind this segment into their respective address spaces, and messages are copied into and out of this segment to effect communication. A preferred memory-based message model is optimized over prior art models by providing address-valued signals, message-oriented memory
30 consistency, and automatic signal-on-write. These refinements represent a

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significant simplification of the kernel interface over that provided by other systems for memory-based messaging. They also allow for a significantly faster and simpler implementation, especially for scalable shared memory multiprocessor architectures.

FIG. 9 is a block diagram illustrating a preferred address-valued signal mechanism, which is a notification that is optimized for memory-based messaging. With address-valued signals, a process sends a signal S_x with a single virtual address parameter. The virtual address is mapped from a shared message region 113x (i.e., a range of virtual address space) in the address space 112x containing the virtual address to a shared segment 115, and the signal S_x is delivered to all processes that bind in that shared segment 115. The signal S_x is delivered as a call to a signal handler with a single parameter, which is the virtual address of the signaled area 113y, 113z in the recipient address space 112y, 112z.

A process sending a message writes the message data into a free area of the message region associated with the destination process(es) and then signals using the virtual address of this free area. The system delivers the signal to each recipient process, calling the process signal handler with the virtual address of the new message in the process address space. The signal handler uses this address to access the new message and deliver the message to the application.

Hardware provides a per-processor First-In-First-Out (FIFO) buffer in which memory addresses representing signals delivered to this processor (but not yet processed) are stored. The signaled processors 12x, 12y are determined from the physical address of the signal S_x (translated from the virtual address from the sender) combined with the cache directory entry associated with the cache line specified by the physical address. In particular, each cache line has a cache directory entry containing a 3-bit mode field and various other tag bits describing the state of the cache line. The FIFO buffer eliminates the need for software delivery of the address values and synchronized software queues to hold those addresses.

The mode field encodes the conventional shared, private and invalid states of an ownership-based consistency protocol as well as a special message mode. Tag

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bits include a set of processor identification bits, one per processor sharing the cache, that normally indicate which processors have copies of the cache line. In message mode, the processor identification bits indicate the processors to be signaled for this cache line. The memory system architecture uses a hierarchical cache structure, with a "global" bit to indicate notification to the next lower level of the memory hierarchy. The lower level maintains its own cache directory and further propagates the signal to other clusters of processors, as indicated by the cache tags. The tag bits are stored in software-maintained page frame descriptors and fetched when the memory is cached.

10 When a process writes a message cache line, hardware generates a signal at that virtual address (referred to as automatic signal-on-write) and maps the referenced virtual address to a physical address, using a standard virtual-to-physical address translation mechanism. The physical address is then mapped in hardware to a cache directory entry. A cache controller generates signals to all processors indicated by the cache tags as recipients, possibly including the next lower level cache (such as the third level cache), which then propagates the signal further as appropriate. The signal is transmitted over each bus as a special bus transaction specifying the address and control lines indicating the affected processors. With direct cache-to-cache transfer, the cache line can be transmitted as part of the same bus transaction.

20 When it receives a signal bus transaction, each processor's bus interface stores the address in the processor's FIFO buffer and interrupts the processor. When a processor receives the signal interrupt, the processor takes the next physical address from the FIFO buffer, maps the physical address to each virtual address and delivers the signal to each process associated with this signal area that is also assigned to this processor. In delivery of the signal, the kernel saves the process context and creates a stack frame to call the signal handler associated with the signaled memory region, passing the translated signal address as the parameter. On return from the signal handler, the process resumes without reentering the kernel.

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On systems without hardware support for automatic signal-on-write, a signal can be generated by a kernel operation.

Address-valued signaling provides a notification mechanism for memory-based messaging that is simple, yet efficient. The translated signal address provides a direct, immediate and asynchronous specification to the recipient(s) of the message, allowing each recipient to immediately locate the message within the segment. In particular, the same signal handler procedure can be used for several different segments and still immediately locate the signaled message using the supplied virtual address. Furthermore, different signal handlers can be bound to different memory regions. The particular signal handler is selected automatically based on the region of memory in which the signal occurs.

The additional hardware to support address-valued signaling is a small percentage of the overall hardware cost, and arguably close to zero cost in large configurations. In particular, a FIFO buffer is required for interprocessor and device interrupts on large-scale systems because the conventional approach of having a dedicated bus line from interrupter to interruptee is not feasible. The FIFO buffer stores the interrupt, allowing the sending processor or device to send the interrupt across the interconnection network and not hold a connection. Storing a single address, rather than the entire message, is essentially the same cost as storing a potentially smaller value such as processor identifier or device identifier. In a preferred embodiment, all device interrupts in the system are handled as address-valued signals, simplifying the hardware and operating system software.

Message-oriented memory consistency is a consistency mode for a segment of memory in which the reader of the segment is only guaranteed to see the last write to this memory after the reader has received an address-valued signal on this segment. In fact, a message and signal can be lost and the receiver is not guaranteed to see the update at all. A process can only expect a new packet to be available after an interrupt from the interface, not at the time the packet is written. Also, if a packet is not received, or is received in a corrupted form, the data is not available at all.

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Memory segments with message-oriented memory consistency are preferably used in a unidirectional fashion as part of memory-based messaging. One process binds the segment as writable and others bind it as read-only. Consequently, there is generally a single writer for a set of addresses within the segment. However, a
5 shared channel may have multiple writers, similar to a citizen-band type radio channel. For example, clients can use a well-known channel to multicast to locate a server.

The message-oriented consistency uses an additional mode for each cache line, as described above. Because there are extra code values available in a
10 particular preferred embodiment beyond those used by the conventional shared memory states, the additional message mode does not increase the cost per cache directory entry. The worst-case would be the addition of an extra bit per cache directory entry, still a small percentage space overhead.

In a preferred embodiment of the invention, there is logic in the cache
15 controller to handle message mode. This logic is relatively simple because message mode modifies actions already performed by the cache controller to comply with the shared memory consistency protocol, and does not require new types of actions. In particular, message mode requires the cache controller to generate an invalidation to each recipient processor after the cache line has been written, rather than before as
20 with consistent shared memory. In a particular preferred embodiment, it is even faster (and simpler) to have the cache controller perform no invalidations, leaving the signaled processors to invalidate their respective caches.

By supporting direct cache-to-cache transfers in hardware, the source processor's cache can transfer the cache line to the recipient processors' caches,
25 providing data transfer and notification in a single bus transaction. This avoids the cache line transfer that normally follows the invalidation after signal reception.

Message-oriented memory consistency reduces the number of bus transactions required to send a message compared with conventional memory consistency. FIGs. 10A-10B are block diagrams illustrating that message-oriented memory consistency
30 reduces the receiver's message invalidation (61), the signaling interrupt (63), the

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message transfer (64) and corresponding acknowledgements (62,65) into a single message delivery transaction (69). Rather than having to invalidate (61) the receivers' copies of each cache line being written by the sender, as in conventional ownership protocols (FIG. 10A), message-oriented memory consistency allows the memory system to simply transmit the update (69) when the message unit has been written (FIG. 10B). Transmitting the update (69) at this time also allows the signal notification to be piggybacked on the data transfer, or vice versa, rather than requiring a separate bus transaction for notification. Thus, the update traffic matches in behavior and efficiency that of a specialized communication facility. In contrast to write-update consistency protocols, message-oriented memory consistency allows updates after a full cache line, page or segment (depending on the consistency unit) rather than on each word write. In that vein, message-oriented memory consistency on single cache-line messages allows the sender to ensure that the receiver receives either all or none of the message, rather than receiving word-level updates. This property is exploited in a preferred embodiment of higher-level protocols.

The message-oriented memory consistency semantics also provides a simple network embodiment of a shared channel segment between two or more network nodes. In particular, an update generated at one node can be transmitted as a datagram to the set of nodes that also bind the affected shared segment. The best-efforts, but unreliable, update semantics of message-oriented consistency obviates the complexity of handling retransmission, timeout and error reporting at the memory level. A large-scale multiprocessor configuration can similarly afford to discard such bus and interconnection network traffic under load or error conditions without violating the consistency semantics.

Finally, message-oriented consistency minimizes the interference between the source and destination processors. The sending processor is not delayed to gain exclusive ownership of the cache line and the reading processors are not delayed by cache line flushes to provide consistent data. In contrast to other relaxed memory consistency models such as Stanford's DASH release consistency, message-oriented

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consistency reduces the base number of bus transactions and invalidations required, rather than just reordering them or allowing them to execute asynchronously.

The automatic signaling on write is on a per-cache line basis (or other consistency unit) so that writing the last byte of such a cache line causes the hardware to generate a signal without any further action by the writing processor. It is understood that the hardware can signal on any other portion of the cache line, but in a particular preferred embodiment the last byte is the easiest convention to use.

The cache controller monitors each write operation to the cache. If a write operation is to a cache line in message mode and the address is the last address of the cache line, the cache controller generates a signal bus transaction after allowing the write to complete.

In a preferred embodiment, the on-chip, or private, cache 14 (FIG. 1) does not support this logic. Consequently, the sender writes through the private cache 14 so that the second level cache controller 180 can detect last-byte writes, and generate the signal. Ideally, the first-level cache controller 140 (FIG. 4) supports this mechanism. This support adds very little complexity to an on-chip cache controller 140.

Automatic signal-on-write reduces the processing overhead on a sending processor when no process on this processor will receive the signal. Reduced sender overhead, in turn, shortens the latency of the message. In the absence of this facility, the sending process must explicitly execute a kernel call, map the signal virtual address to a physical address and then presumably access hardware facilities to generate the signal, or at least an interprocessor interrupt of some form. Providing kernel-level access to the cache controller to explicitly generate a signal is more expensive in hardware than providing the logic in the cache controller to detect and act on writes to the end of a cache line in message mode.

In automatic signal-on-write, the channel segment specifies the unit of signaling, transparent to the sending process. For example, a receiver can pass the sender a channel which signals on every cache line or every page, depending on the

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receiver's choice. Without automatic signal-on-write, the sender needs to explicitly signal and thus needs to be coded explicitly for each form of behavior, perhaps switching between different behaviors based on the type of channel.

In message mode, a holding memory for the cache line is notified of the
5 update after the cache line has been written, rather than before as occurs with conventional consistent shared memory. When a cache line in message mode is written, the cache line is transferred directly to the set of cache controllers that have indicated an interest in this cache line using the cache directory tags normally used to indicate those memories holding a shared copy when the cache line is in shared
10 mode. These tags are cached in the cache partition when the cache line is loaded into the local cache partition. The cache line can be invalidated in all caches when these tags are modified, thereby preserving consistency of the tags.

This transfer uses the same direct cache-to-cache transfer mechanism that is used to writeback a cache line in exclusive mode from one cache partition to the
15 peer-level owning cache partition. In the message-oriented consistency mode, the writing process overwrites the cache line and transmits the cache line to these other caches without first acquiring exclusive ownership of the cache line. In contrast, conventional shared memory consistency mechanisms require the writer of a cache line to first acquire exclusive ownership of the cache line, invalidating all copies of
20 the cache line that might occur in other caches.

Returning to FIG. 8, a device controller 160 participates in this protocol as follows. When data is to be written from the device to an address in memory that is set in message-oriented consistency mode, the data is transferred directly to the peer-level cache controllers 180 and other device controllers according to the cache
25 tag bits described above. In a particular preferred embodiment, a direct transfer only occurs if the transfer is to a single other controller, and otherwise, the data is transferred to a next-level memory area and the cache line is invalidated in the peer-level caches, notifying them of the revised cache line. A device controller 160 loads the tags to the affected area of memory as part of establishing access to this
30 memory area, either at the time a mapping of device data to this memory is setup or

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at the point the data is to be written to the area of memory. A device controller also participates by receiving direct transfers of cache lines in message mode from other cache controllers and device controllers, as occurs on processor and device writing to these cache lines.

5 Equivalents

Those skilled in art will know, or be able to ascertain using no more than routine experimentation, many equivalents to the specific embodiments of the invention described herein.

These and all other equivalents are intended to be encompassed by the
10 following claims.

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CLAIMS

The invention claimed is:

1. In a computer system having a plurality of data accessors, a cache memory
for providing stored cache lines to be accessed by the data accessors, the
5 cache memory comprising:
a plurality of cache memory areas at a common level of cache
memory, each cache memory area locally coupled to a respective data
accessor, the cache memory areas coupled together to form a cache memory
cluster; and
10 a plurality of local cache controllers, each local cache controller
coupled between a respective data accessor and a respective locally-coupled
cache memory area to request a cache line on behalf of the data accessor
from the respective locally-coupled cache memory area and from remaining,
remotely-coupled cache memory areas of the cache memory cluster in
15 response to an unsatisfied cache line request at the locally-coupled cache
memory area.
2. The cache memory according to Claim 1 further comprising a private cache
coupled between each data accessor and the respective local cache controller,
each data accessor having exclusive access to the respective private cache,
20 and wherein the private cache requests a cache line from the local cache
controller only upon the cache line request being unsatisfied by the private
cache.
3. The cache memory according to Claim 1 wherein the second plurality is less
than the first plurality.

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4. The cache memory according to Claim 1 wherein the cache memory areas are coupled by a shared cache interconnect.
5. The cache memory according to Claim 1 wherein there are less than or equal to four cache memory areas in the cache memory cluster.
- 5 6. The cache memory according to Claim 1 further comprising an external data accessor coupled to the cache memory cluster for accessing a cache line, each cache memory area in the cache memory cluster is remotely coupled to the external data accessor.
7. The cache memory according to Claim 1 wherein data has an associated
10 ownership in a holder memory area, the satisfaction of a memory reference from data in the holder memory area does not affect the ownership of the data in the holder memory area relative to more distant memory.
8. The cache memory according to Claim 1 wherein the cache line is accessed
15 for message data between data accessors.
9. A distributed shared cache computing system having a plurality of data accessors for referencing data in memory, each memory reference being satisfied from a hierarchical memory structure having a plurality of memory levels relative to the data accessors, comprising:
20 a first memory level of private cache memory in the hierarchical memory structure for satisfying memory references at the first memory level, each private cache memory providing exclusive access to a respective data accessor; and

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- a second memory level of at least one cluster of shared cache memory in the hierarchical memory structure for satisfying memory references at the second memory level, each cluster of shared cache memory being coupled to a respective group of data accessors and distributed such that each area of the cluster of shared cache memory is a local cache memory to a respective data
5 accessor from the group of data accessors and a remote cache memory to the remaining at least one data accessor from the group of data accessors.
10. The distributed shared cache computing system according to Claim 9 wherein there are four areas per cluster of shared cache memory and four data
10 accessor per group of data accessors.
11. The distributed shared cache computing system according to Claim 9 wherein each data accessor is coupled to the remote cache memory such that a cache miss for a memory reference request to the local cache memory is re-requested to the remote cache memory.
- 15 12. The distributed shared cache computing system according to Claim 11 wherein each data accessor is further coupled to at least one lower memory level, such that a cache miss for a memory reference to the respective cluster of shared cache memory is satisfied by a more distant memory unit.
13. The distributed shared cache computing system according to Claim 9 wherein
20 the data has an associated ownership in a holder memory area, the satisfaction of a memory reference from data in the holder memory area does not affect the ownership of the data in the holder memory area relative to more distant memory.
14. The distributed shared cache computing system according to Claim 9 wherein
25 the data is message data between data accessors.

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15. The distributed shared cache computing system according to Claim 9 further comprising an external data accessor coupled to a cluster of shared cache memory in the second memory level for accessing a cache line, each area of the cluster is remotely coupled to the external data accessor.
- 5 16. A computing system having a plurality of data accessors and a multiple level hierarchical memory structure, comprising:
- a plurality of first cache memory areas, each first cache memory area coupled to a respective data accessor for providing a private memory relative to the respective data accessor;
- 10 a plurality of second cache memory areas, each second cache memory area coupled to a respective private memory level, each second cache memory area providing a local cache memory relative to the respective data accessor, a local cache memory being searched to satisfy a first cache miss in the respective private memory; and
- 15 at least one shared cache interconnect to couple at least one cluster of second cache memory areas together such that a second cache miss in a local cache memory causes a search at the remaining second cache memory areas from the cluster of second cache memory areas to satisfy the second cache miss.
- 20 17. The computing system according to Claim 16 further comprising a plurality of cache controller, each cache controller coupling a respective second cache memory area to the respective private memory and the shared cache interconnect.

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18. The computing system according to Claim 16 wherein each cluster of second cache memory areas is a shared cache memory, each second cache memory area in the cluster of second cache memory areas being an equal subset of the shared cache memory.
- 5 19. The computing system according to Claim 16 wherein there are less than five second cache memory areas in each cluster of second cache memory areas.
20. The computing system according to Claim 19 wherein there are four second cache memory areas in each cluster of second cache memory areas.
- 10 21. The computing system according to Claim 16 further comprising an external data accessor coupled to a cluster of second memory areas to search the second cache memory areas to satisfy a memory reference by the external data accessor.
22. The computing system according to Claim 21 wherein the external data accessor includes a device controller.
- 15 23. The computing system according to Claim 16 further comprising an interface coupled to each shared cache interconnect for coupling each respective cluster of second cache memory areas to a respective main memory area, the main memory area being searched to satisfy a third cache miss from the cluster of second cache memory areas.
- 20 24. The computing system according to Claim 23 wherein each cluster of second cache memory areas and the respective coupled data accessors, first cache memory areas, and interface are integrated as a multiprocessor module.

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25. The computing system according to Claim 23 wherein there are a plurality of main memory areas, each main memory area coupled to at least one other main memory area to form a cluster of main memory areas, each main memory area serving as a local main memory to the respective cluster of second cache memory areas and as a remote main memory area to the at least one cluster of second cache memory areas coupled to respective remaining main memory areas of the plurality of main memory areas.
- 5
26. The computing system according to Claim 25 wherein the cluster of main memory areas are coupled by a fiber optic coupling system.
- 10
27. The computing system according to Claim 25 wherein the cluster of main memory areas are coupled by a shared bus.
28. The computing system according to Claim 16 wherein the shared cache interconnect is a shared bus.
29. The computing system according to Claim 16 wherein the shared cache interconnect is an interconnection network.
- 15
30. The computing system according to Claim 16 wherein the cache memory is accessed for message data between data accessors.
31. An integrated circuit for a multiple level hierarchical memory computing system, comprising:
- 20
- a data processor for requiring memory references;
 - a first cache memory for providing a private memory level relative to the data processor for storing a copy of data to satisfy memory references at the first cache memory; and

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a local cache controller coupled to the private memory level for controlling access to a respective local second cache memory and to a cluster of remote second cache memory for requesting memory references from the remote second cache memory.

- 5 32. The integrated circuit according to Claim 31 wherein the local cache controller is cooperatively shared with at least one remote data processor, such that the remote data processor can satisfy a memory reference from the respective local second cache memory.
- 10 33. The integrated circuit according to Claim 31 further comprising a private cache controller coupled between the data processor, the first cache memory, and the local cache controller for controlling access to the private memory level and requesting memory references from the local cache controller upon a cache miss in the respective first cache memory.
- 15 34. In a computer system having a plurality of data accessors, a method of providing stored cache lines from a cache memory to be accessed by the data accessors, comprising the steps of:
- 20 distributing the cache memory into a common level of cache memory areas, each cache memory area coupled to a respective data accessor;
- forming the cache memory areas into at least one cache memory cluster, the forming steps comprising:
- a) associating each cache memory area with a respective data accessor to form a local cache memory area for each data accessor;

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- 5 b) controlling access to each cache memory area such that a
memory reference from a data accessor is requested at the
respective local cache memory area and the remaining cache
memory areas in the cache memory cluster are searched to
satisfy a cache miss in a local cache memory area; and
returning data from memory to the data accessor in satisfaction
of the memory reference.
- 10 35. The method according to Claim 34 further comprising, before the step of
returning, the step of satisfying a cache miss in a cache memory cluster from
memory external to the cache memory cluster.
36. The method according to Claim 34 wherein there is an external data accessor
not locally coupled to a cache memory area and the step of controlling access
includes searching the cache memory areas in the cache memory cluster to
satisfy a memory access by the external data accessor.
- 15 37. The method according to Claim 34 wherein the cache lines are accessed for
message data between data accessors.
- 20 38. A method for locating a memory reference on a multiple-level hierarchial
memory computing system having at least one data accessor for requesting
memory references to be obtained from memory, each memory level having
at least one memory area for storing data to satisfy memory references,
comprising the steps of:
 at a memory level having at least one peer memory area, locating the
memory reference comprising the locating steps of:
 a) searching a memory area that is locally coupled to the data
25 accessor requiring the memory reference;

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- b) upon a memory miss at the locally-coupled memory area, searching at least one peer memory area that is remotely-coupled to the data accessor requiring the memory reference; and
- 5 returning the located memory reference to the data accessor.
39. The method according to Claim 38 further comprising, before the step of returning, the step of searching more distant memory relative to the data accessor to locate the memory reference at a more distant memory.
40. The method according to Claim 38 wherein there is at least one data accessor
10 not having a locally-coupled memory area in the memory level.
41. The method according to Claim 40 wherein the data accessor not having a locally-coupled memory area includes a device controller.
42. The method according to Claim 38 wherein the referenced memory contains message data between data accessors.
- 15 43. A method of communicating between data accessors in a cache memory computing system, comprising the steps of:
- providing a cache line in a cache memory area shared between the data accessors;
- binding at least one receiver data accessor to receive message data
20 from the cache line;
- from a sender data accessor, writing message data to the cache line;
- and
- delivering the message data from the cache line to the receiver data accessor.

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44. The method according to Claim 43 wherein the shared cache line is in a multi-level memory hierarchy.
45. The method according to Claim 43 wherein the cache line has a message mode and the step of binding comprises the step of setting tag bits associated
5 with the cache line to indicate the data accessors to receive message data from the cache line.
46. The method according to Claim 43 wherein at least one data accessor includes a device controller.

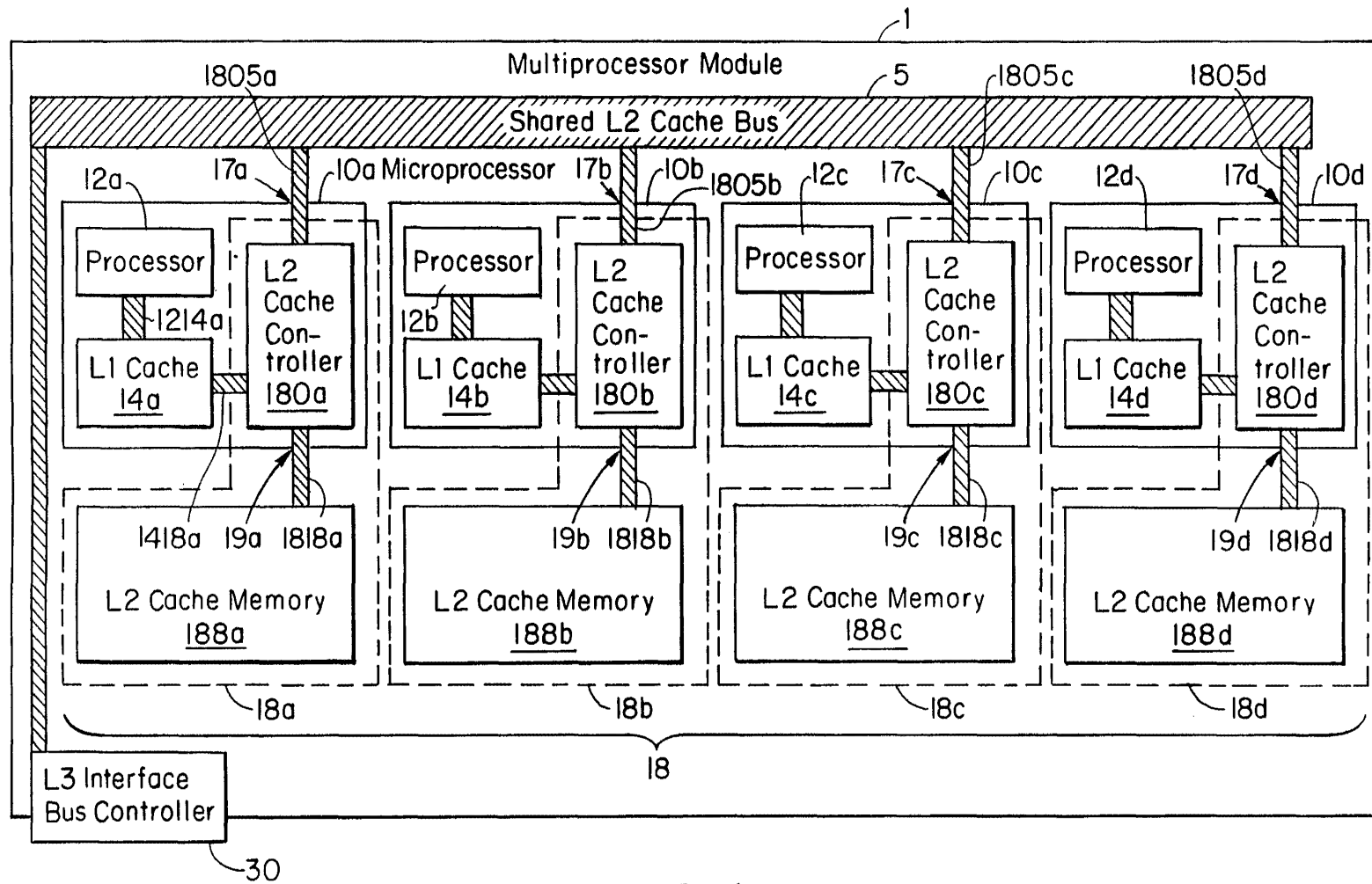


FIG. 1

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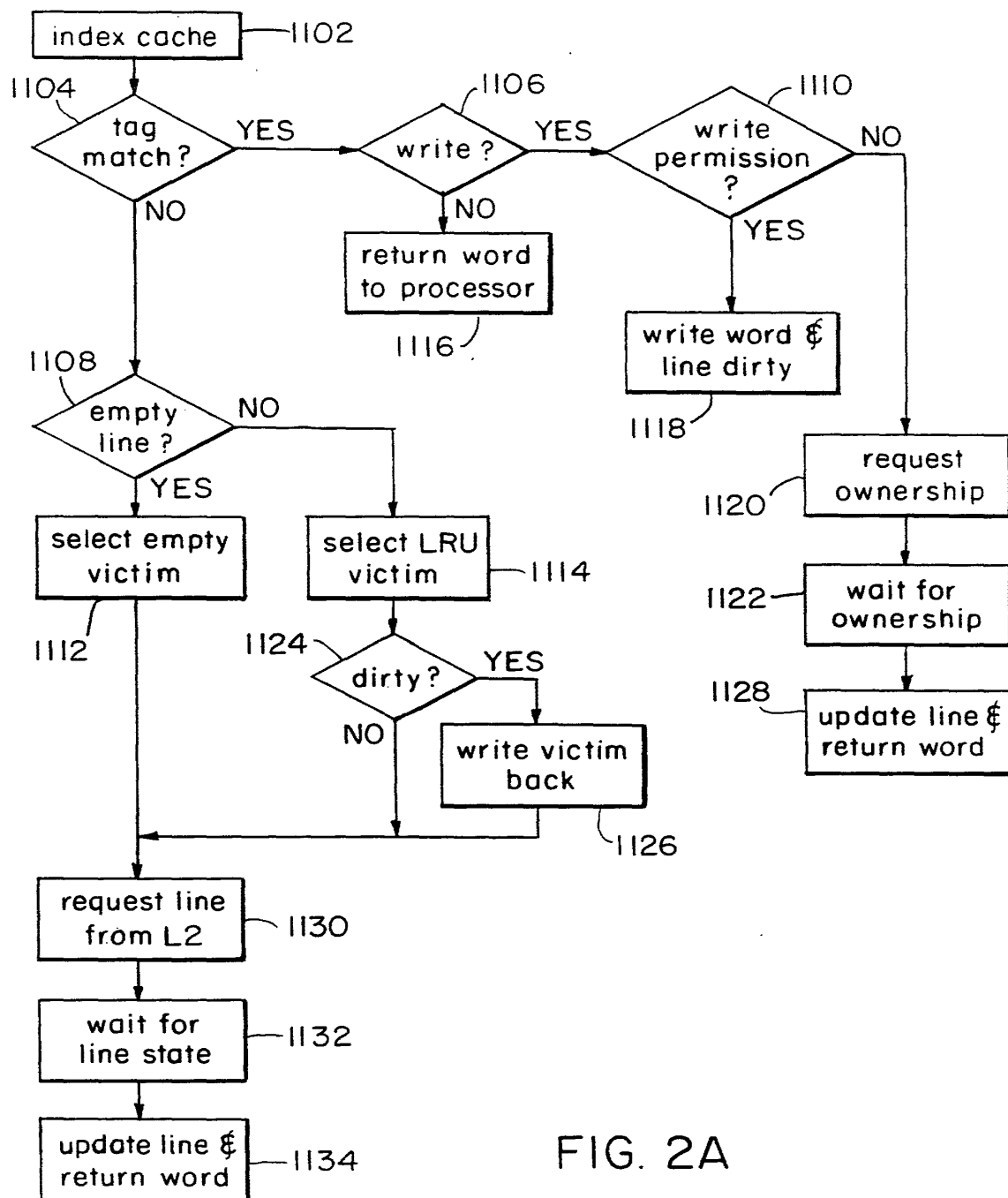
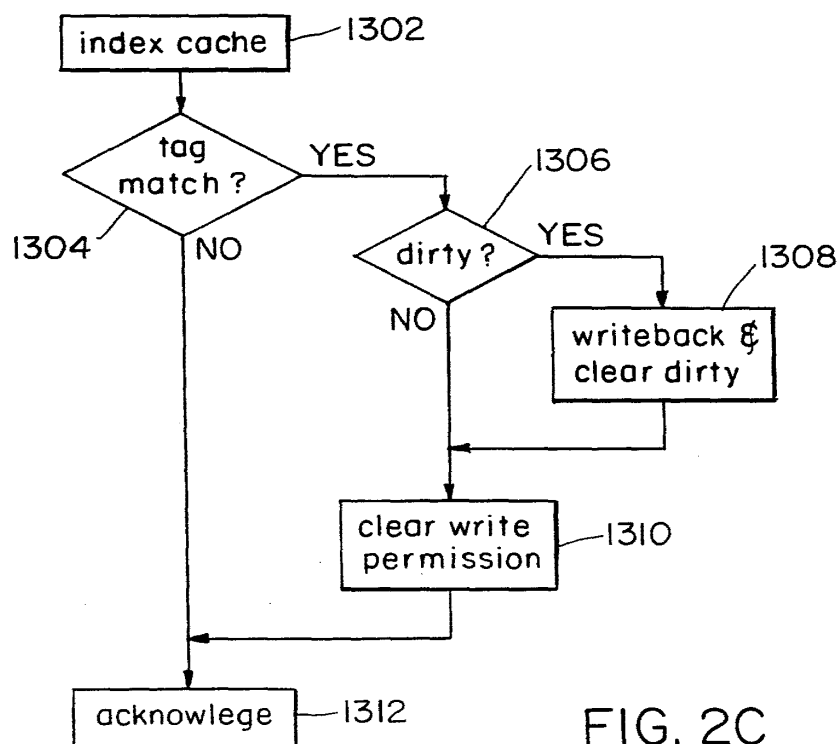
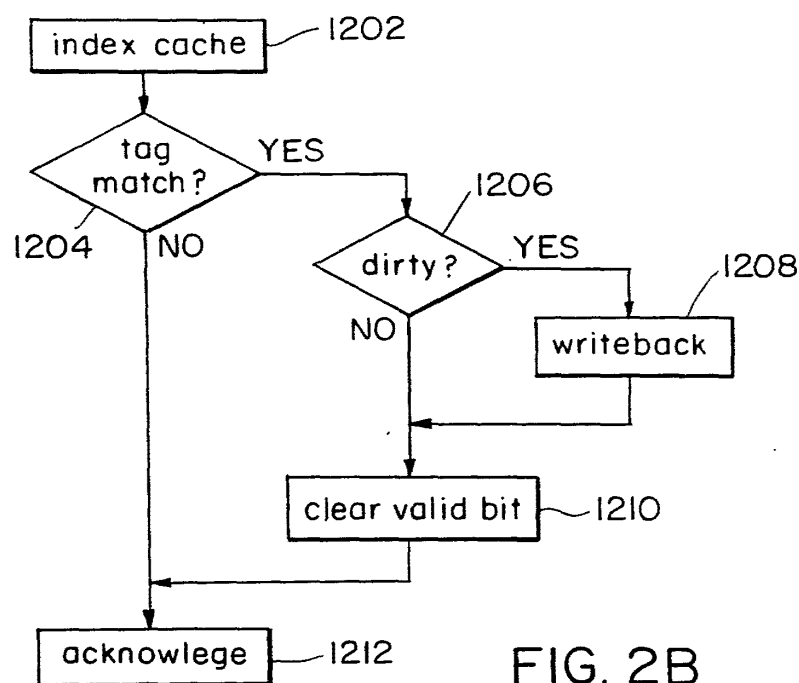


FIG. 2A

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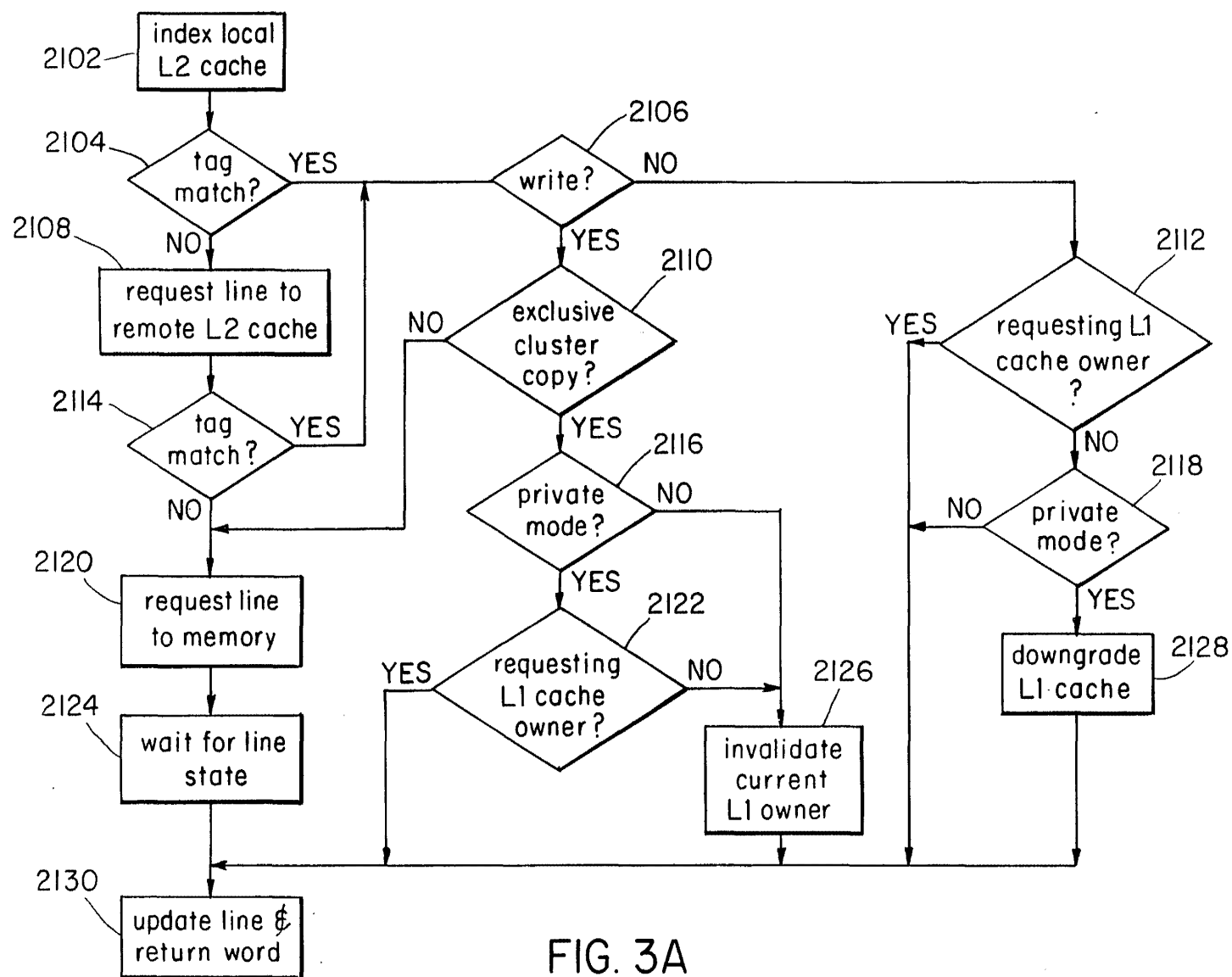
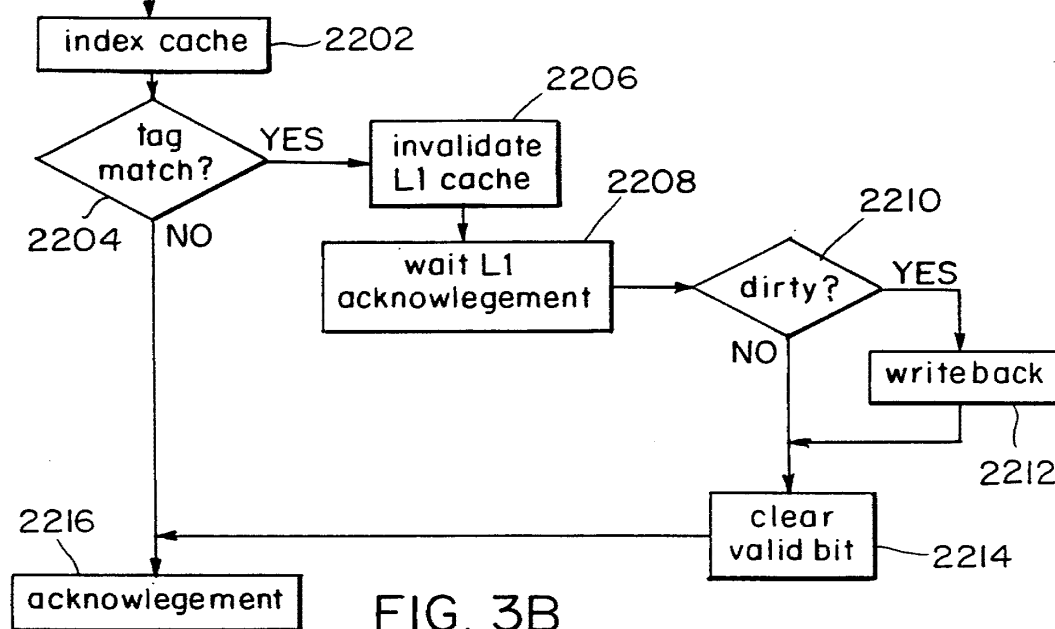
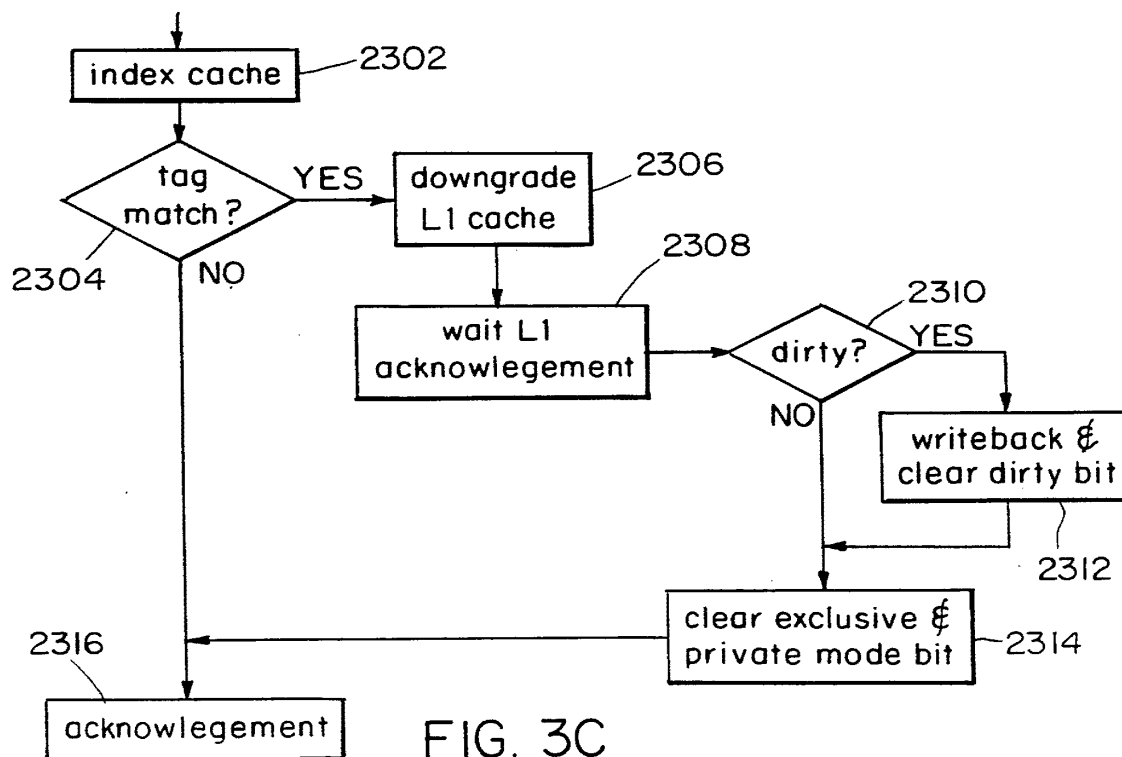


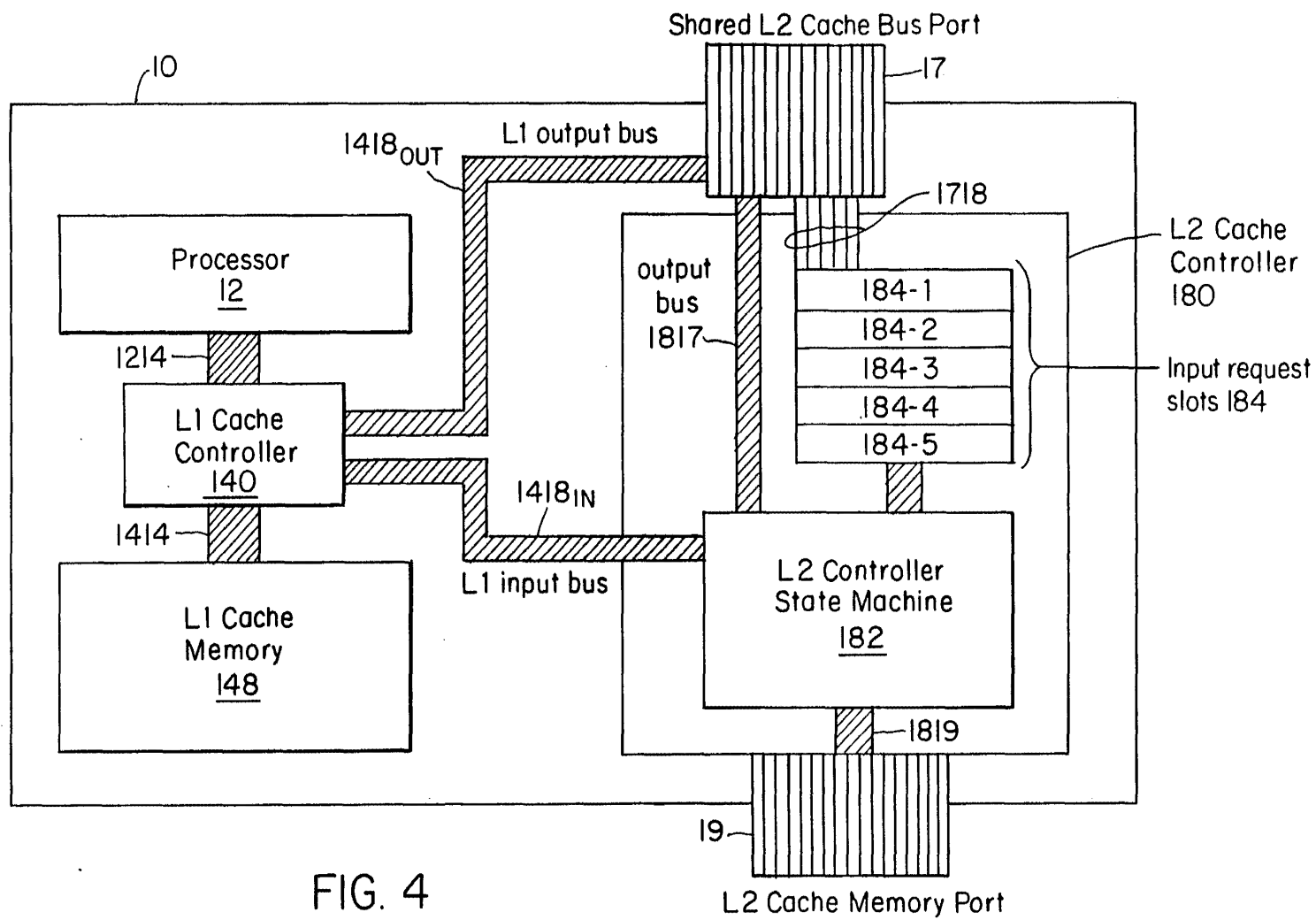
FIG. 3A

INVALIDATE request to
L2 CACHE from MEMORY



DOWNGRADE request to
L2 CACHE from L2 MEMORY





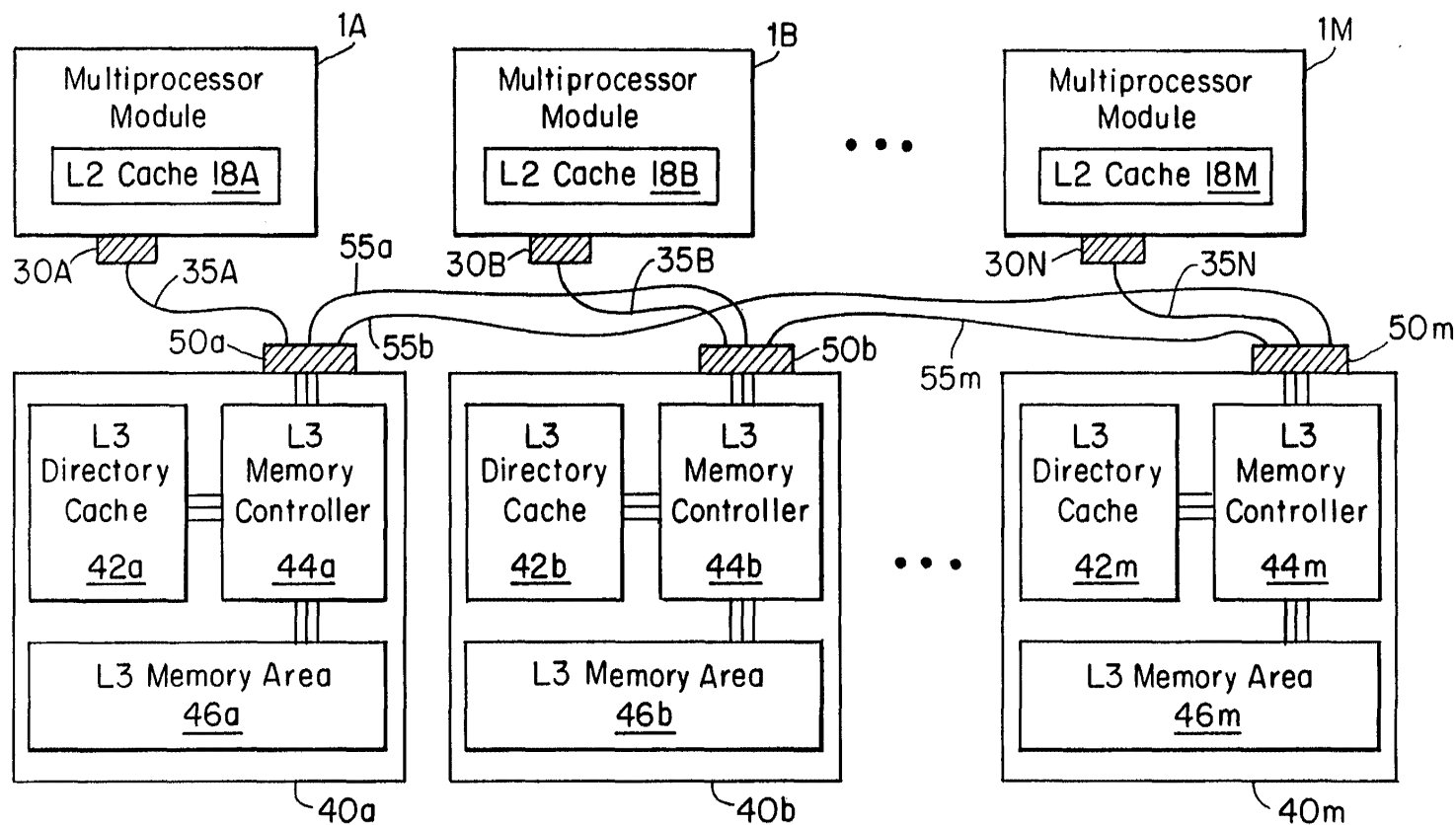


FIG. 5

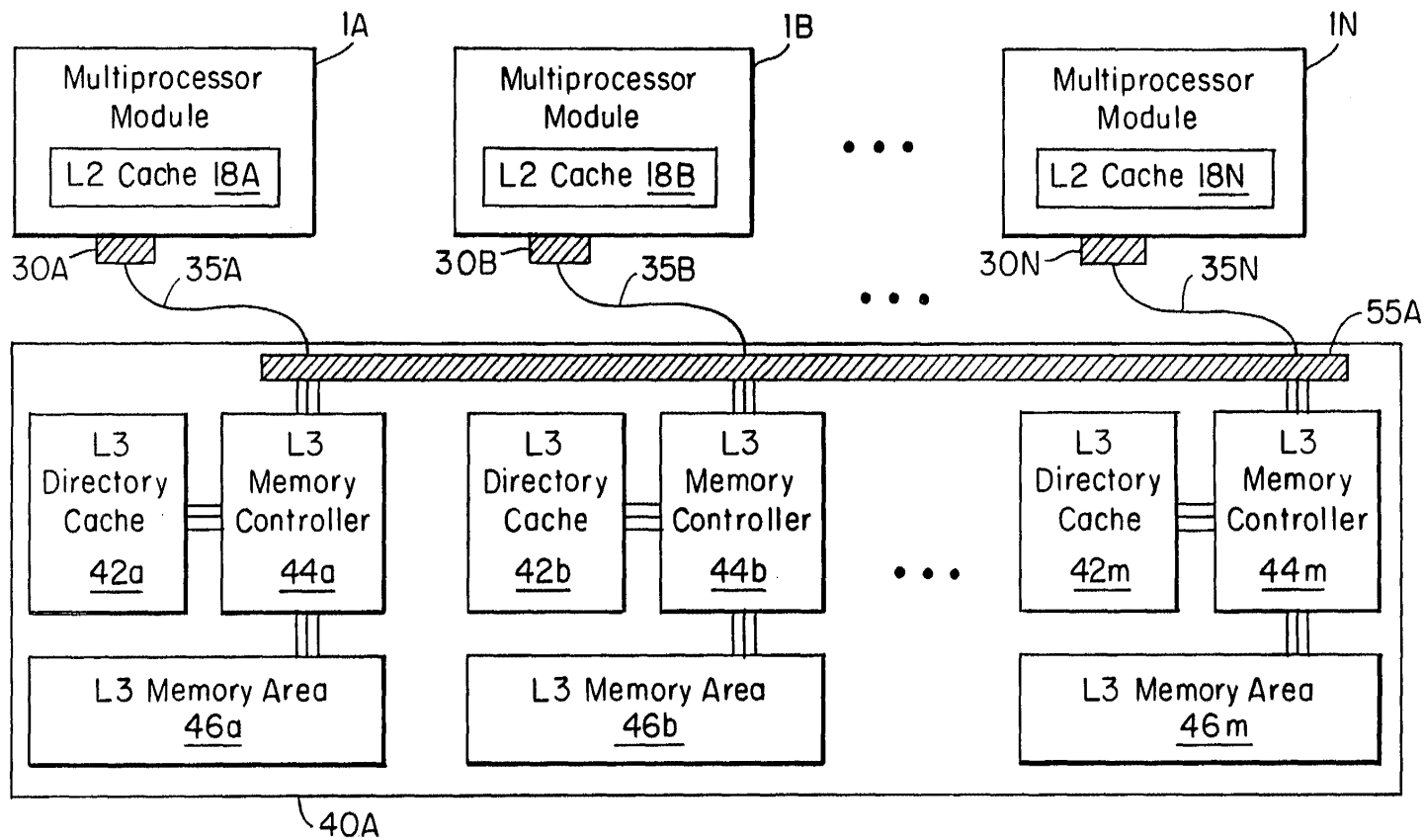


FIG. 6

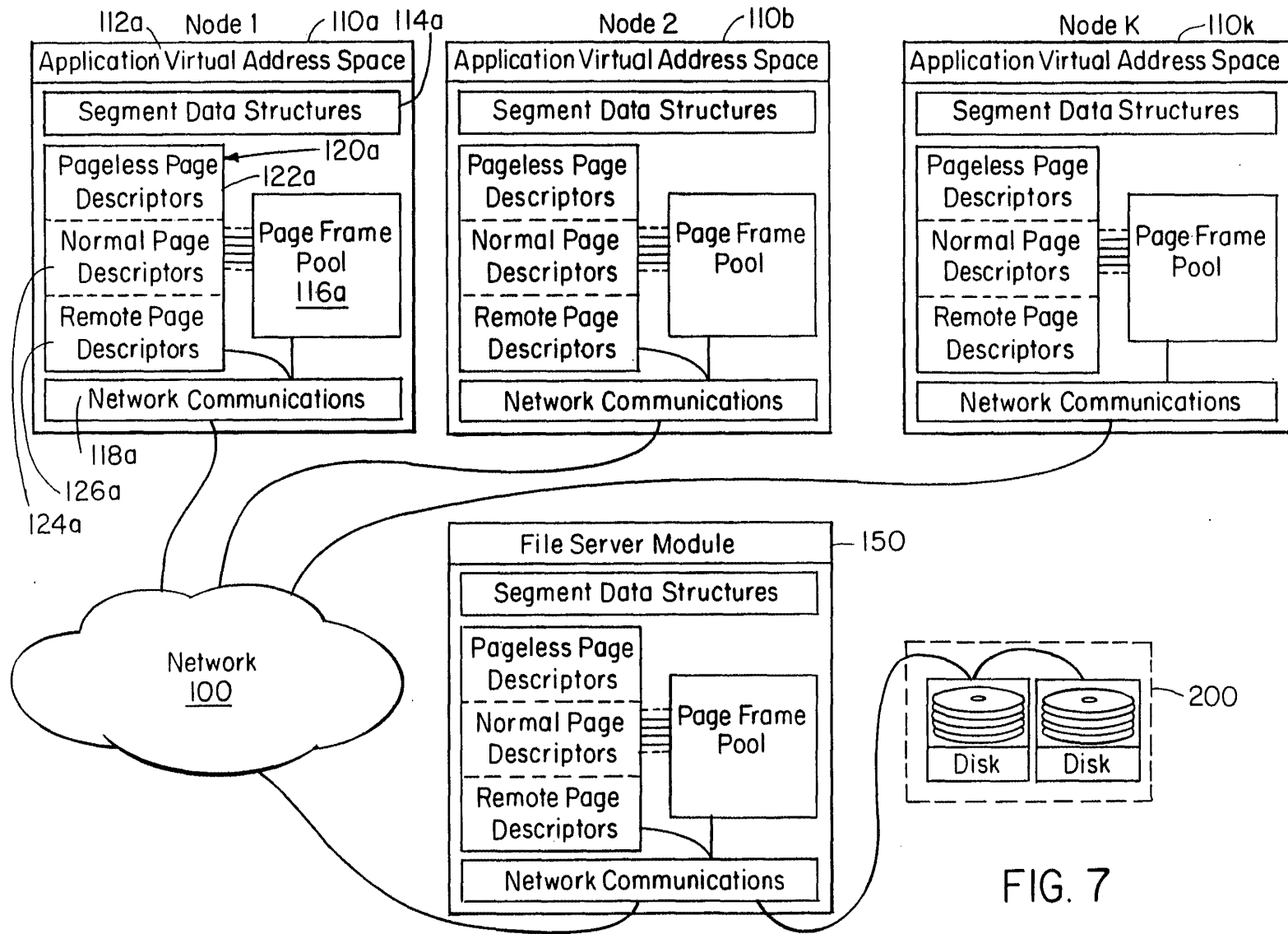


FIG. 7

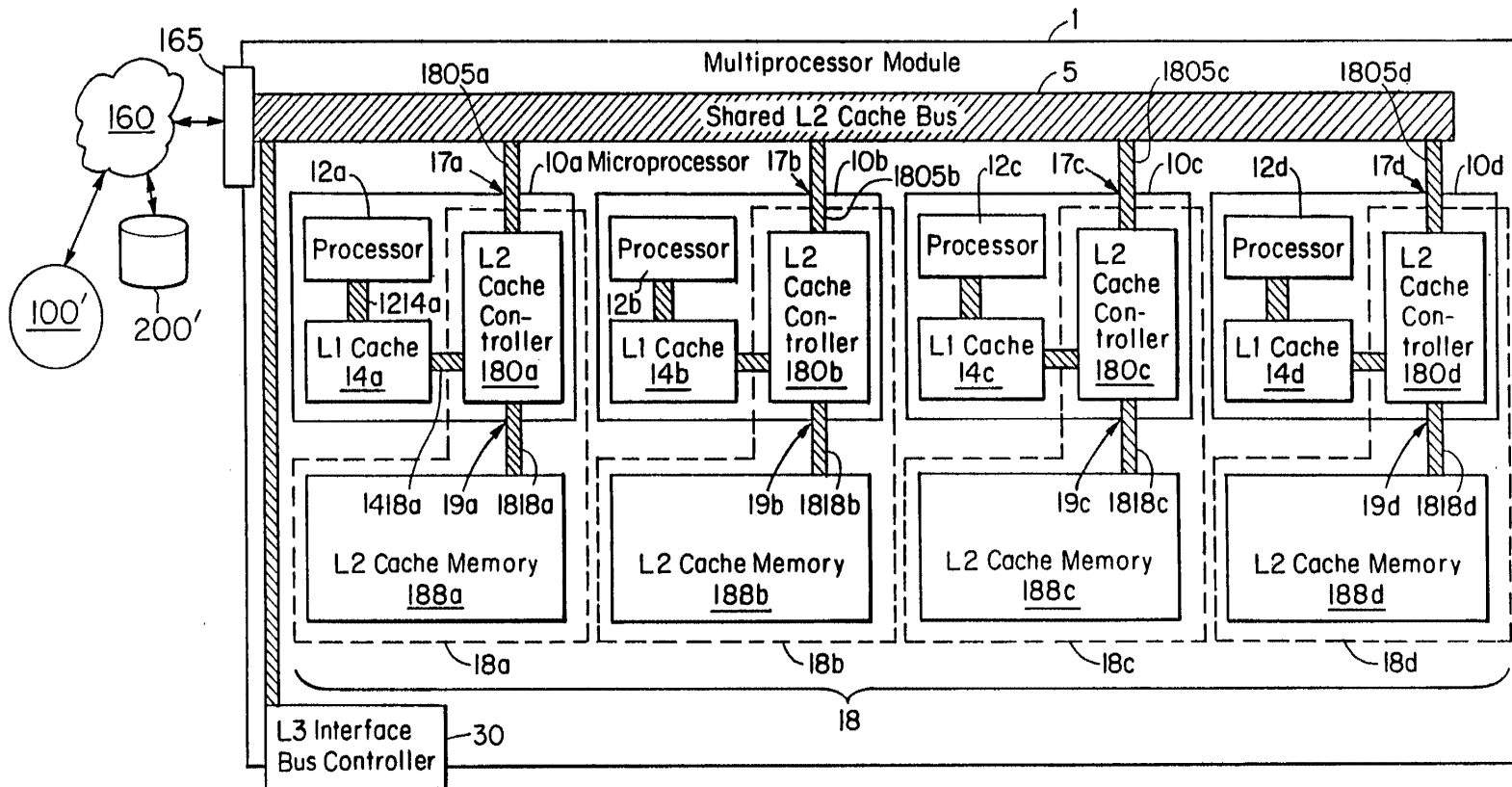


FIG. 8

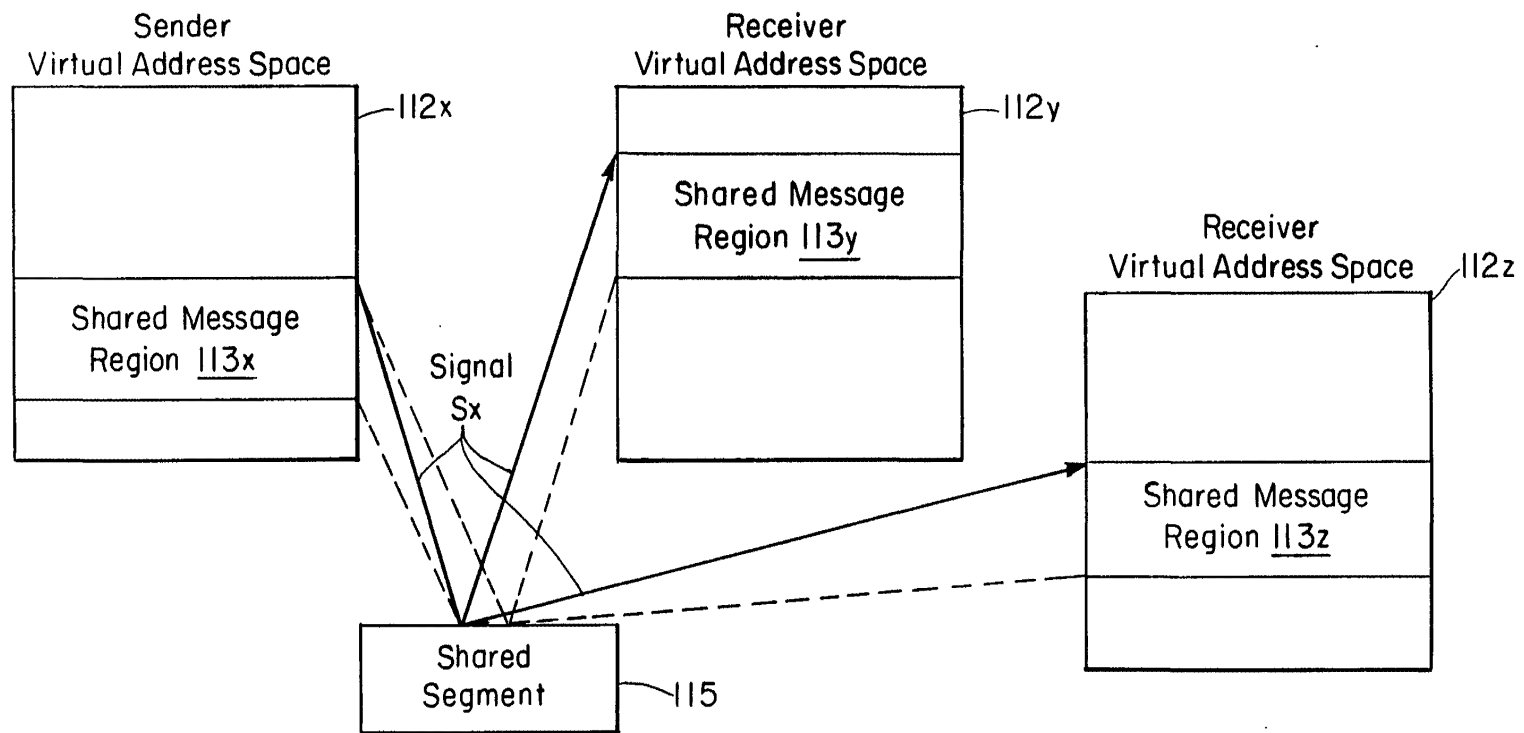


FIG. 9

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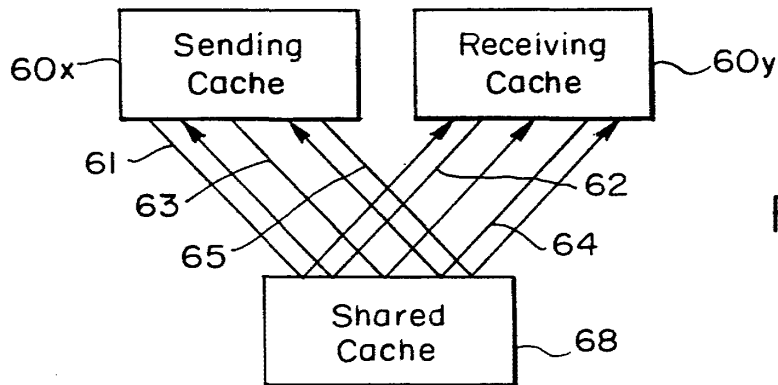


FIG. 10A

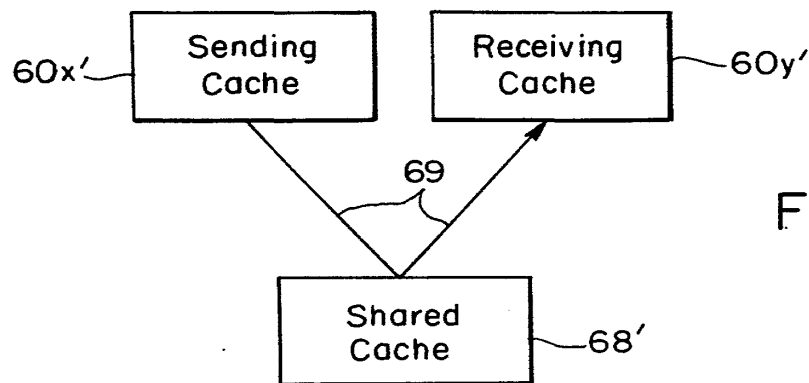


FIG. 10B

Electronic Patent Application Fee Transmittal				
Application Number:		14219945		
Filing Date:		19-Mar-2014		
Title of Invention:		Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply		
First Named Inventor/Applicant Name:		Martin VORBACH		
Filer:		Edward Peter Heller/Emi Rhodes		
Attorney Docket Number:		PACT-025-PCT-US-D1-2C1-D1		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
Total in USD (\$)				180

Electronic Acknowledgement Receipt	
EFS ID:	22363882
Application Number:	14219945
International Application Number:	
Confirmation Number:	7671
Title of Invention:	Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply
First Named Inventor/Applicant Name:	Martin VORBACH
Customer Number:	73481
Filer:	Edward Peter Heller/Emi Rhodes
Filer Authorized By:	Edward Peter Heller
Attorney Docket Number:	PACT-025-PCT-US-D1-2C1-D1
Receipt Date:	15-MAY-2015
Filing Date:	19-MAR-2014
Time Stamp:	16:59:57
Application Type:	Utility under 35 USC 111(a)

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			5ddd912fa6b4afa5058a9bc7275ebf44d4613afa		
Warnings:					
Information:					
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3	Foreign Reference	Cheriton_WO9525306.pdf	2695571	no	63
			90614ca635d1011190c784d0c6a610ce09fa1e70		
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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): Vorbach, Martin	Art Unit: 2116
Application No.: 14/219,945	
Filed: 03-19-2014	Examiner: ELAMIN, ABDELMONIEM I
Title: Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply	Conf. #: 7671
Attorney Docket No.: PACT-025-PCT- US-D1-2C1-D1	

Electronically Filed
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Information Disclosure Statement

Dear Sir:

Pursuant to 37 C.F.R § 1.56, § 1.97, and § 1.98, the Examiner's attention is hereby directed to the references cited on the attached PTO/SB/08A forms.

Copies of references in compliance with the requirements of 37 CFR § 1.98(a)(2) are enclosed except the references listed below. The copies of these references will be submitted as they become available to Applicant(s).

- LIBO HUANG ET AL: "A New Architecture For Multiple-Precision Floating-Point Multiply-Add Fused Unit Design" COMPUTER ARITHMETIC, 2007. ARITH '07. 18TH IEEE SYMPOSIUM ON, IEEE, PI, 1. June 2007 (2007-06-01), Pages 69-76.
- MANHWEE JO ET AL: "Implementation of floating-point operations for 3D graphics on a coarse-grained reconfigurable architecture" SOC CONFERENCE, 2007 IEEE INTERNATIONAL, IEEE, PISCATAWAY, NJ, USA, 26. September 2007 (2007-09-26), Pages 127-130.

Respectfully Submitted,

May 15, 2015

/Edward P. Heller III/
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Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

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	Filing Date		2014-03-19
	First Named Inventor	Martin Vorbach	
	Art Unit	2116	
	Examiner Name	ELAMIN, ABDELMONIEM I	
	Attorney Docket Number	PACT-025-PCT-US-D1-2C1-D1	

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	2	5197016		1993-03-23	Sugimoto et al.	
	3	5296759		1994-03-22	Sutherland et al.	
	4	5651137		1997-07-22	MacWilliams et al.	
	5	5685004		1997-11-04	Bruce et al.	
	6	5808487		1998-09-15	Roy	
	7	5893165		1999-04-06	Ebrahim	
	8	5905875		1999-05-18	Takahashi et al.	

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	Filing Date	2014-03-19
	First Named Inventor	Martin Vorbach
	Art Unit	2116
	Examiner Name	ELAMIN, ABDELMONIEM I
	Attorney Docket Number	PACT-025-PCT-US-D1-2C1-D1

	9	6038646		2000-03-14	Sproull	
	10	6108737		2000-08-22	Sharma et al.	
	11	6119219		2000-09-12	Webb et al.	
	12	6122719		2000-09-19	Mirsky et al.	
	13	6141734		2000-10-31	Razdan et al.	
	14	6209065		2001-03-27	Van Doren et al.	
	15	6263406		2001-07-17	Uwano et al.	
	16	6286090		2001-09-04	Steely Jr. et al.	
	17	6314484		2001-11-06	Zulian et al.	
	18	6341318		2002-01-22	Dakhil	
	19	6347346		2002-02-12	Taylor	

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	First Named Inventor	Martin Vorbach		
	Art Unit	2116		
	Examiner Name	ELAMIN, ABDELMONIEM I		
	Attorney Docket Number	PACT-025-PCT-US-D1-2C1-D1		

	20	6385672		2002-05-07	Wang et al.	
	21	6457100		2002-09-24	Ignatowski et al.	
	22	6467009		2002-10-15	Winegarden et al.	
	23	6522167		2003-02-18	Ansari et al.	
	24	6571322		2003-05-27	Arimilli et al.	
	25	7036106		2006-04-25	Wang et al.	
	26	7924837		2011-04-12	Shabtay et al.	
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	1	20040093186	A1	2004-05-13	Ebert Jeffrey Allen et al.	

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	Filing Date		2014-03-19	
	First Named Inventor	Martin Vorbach		
	Art Unit	2116		
	Examiner Name	ELAMIN, ABDELMONIEM I		
	Attorney Docket Number	PACT-025-PCT-US-D1-2C1-D1		

	2	20050257179	A1	2005-11-17	Stauffer David R. et al.	
	3	20060036988	A1	2006-02-16	Allen Tim et al.	

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	Filing Date	2014-03-19
	First Named Inventor	Martin Vorbach
	Art Unit	2116
	Examiner Name	ELAMIN, ABDELMONIEM I
	Attorney Docket Number	PACT-025-PCT-US-D1-2C1-D1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☒ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☒ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☐ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Edward P. Heller III/	Date (YYYY-MM-DD)	2015-07-02
Name/Print	Edward P. Heller III	Registration Number	29075

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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Electronic Patent Application Fee Transmittal				
Application Number:		14219945		
Filing Date:		19-Mar-2014		
Title of Invention:		Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply		
First Named Inventor/Applicant Name:		Martin VORBACH		
Filer:		Edward Peter Heller/Emi Rhodes		
Attorney Docket Number:		PACT-025-PCT-US-D1-2C1-D1		
Filed as Large Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Submission- Information Disclosure Stmt	1806	1	180	180
Total in USD (\$)				180

Electronic Acknowledgement Receipt	
EFS ID:	22815065
Application Number:	14219945
International Application Number:	
Confirmation Number:	7671
Title of Invention:	Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply
First Named Inventor/Applicant Name:	Martin VORBACH
Customer Number:	73481
Filer:	Edward Peter Heller/Emi Rhodes
Filer Authorized By:	Edward Peter Heller
Attorney Docket Number:	PACT-025-PCT-US-D1-2C1-D1
Receipt Date:	02-JUL-2015
Filing Date:	19-MAR-2014
Time Stamp:	14:25:27
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$180
RAM confirmation Number	1628
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Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
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Warnings:					
Information:					
2	Non Patent Literature	COMPTON_ET_AL_ReconfigurableComputing.pdf	11604113 397d76d1453bb763776bdfc933692b2f6bb5a41e	no	41
Warnings:					
Information:					
3	Fee Worksheet (SB06)	fee-info.pdf	30773 f145ce7179fd9bc07029924971438634106f88b8	no	2
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Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (01-10)

Approved for use through 07/31/2012. OMB 0651-0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14219945
	Filing Date		2014-03-19
	First Named Inventor	Martin Vorbach	
	Art Unit	2116	
	Examiner Name	ELAMIN, ABDELMONIEM I	
	Attorney Docket Number	PACT-025-PCT-US-D1-2C1-D1	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	4967340		1990-10-30	Dawes	
	2	5301340		1994-04-05	Cook	
	3	5327570		1994-07-05	Foster et al.	
	4	5459846		1995-10-17	Hyatt	
	5	5784636		1998-07-21	Rupp	
	6	5991900		1999-11-23	Garnett	
	7	6052773		2000-04-18	DeHon et al.	
	8	6079008		2000-06-20	Clery III	

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	Attorney Docket Number	PACT-025-PCT-US-D1-2C1-D1

	9	6119181		2000-09-12	Vorbach et al.	
	10	6138198		2000-10-24	Garnett et al.	
	11	6226714		2001-05-01	Safranek et al.	
	12	6321296		2001-11-20	Pescatore	
	13	6321373		2001-11-20	Ekanadham et al.	
	14	6425068		2002-07-23	Vorbach et al.	
	15	6457100		2002-09-24	Ignatowski et al.	
	16	6587961		2003-07-01	Garnett et al.	
	17	6643747		2003-11-04	Hammarlund et al.	
	18	6658578		2003-12-02	Laurenti et al.	
	19	6763327		2004-07-13	Songer et al.	

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	20	6868476		2005-03-15	Rosenbluth et al.	
	21	6895452		2005-05-17	Coleman et al.	
	22	7043416		2006-05-09	Lin	
	23	8463835		2013-06-11	Walke	
	24	9047440		2015-06-02	Vorbach et al.	
	25	6381687		2002-04-30	Sandstrom et al.	
	26	9147623		2015-09-29	Lua et al.	
	27	9099460		2015-08-04	Cho et al.	

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	1	20070050603	A1	2007-03-01	Vorbach Martin et al.	

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	Filing Date		2014-03-19	
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	Art Unit	2116		
	Examiner Name	ELAMIN, ABDELMONIEM I		
	Attorney Docket Number	PACT-025-PCT-US-D1-2C1-D1		

	2	20110060942	A1	2011-03-10	VORBACH Martin	
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	1	10028397.1	DE		2001-12-20	VORBACH		☒

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	1	Silberschatz and Galvin, Operating System Concepts, 1998, Addison Wesley, 5th edition, ISBN 0-201-59113-8, 31 pages						☐
	2	Altera FLEX 10K Embedded Programmable Logic Family Data Sheet; October 1998, ver. 3.13; pages 1 -21.						☐
	3	Hauser, John Reid, Augmenting a Microprocessor with Reconfigurable Hardware, University of California, Berkeley, Fall 2000.						☐

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	Attorney Docket Number	PACT-025-PCT-US-D1-2C1-D1

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

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☐ See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Edward P. Heller/	Date (YYYY-MM-DD)	2015-11-24
Name/Print	Edward P. Heller	Registration Number	29075

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**DEUTSCHES
PATENT- UND
MARKENAMT**

①⑫ **Offenlegungsschrift**
①⑩ **DE 100 28 397 A 1**

⑤① Int. Cl. 7:
G 06 F 15/80
G 06 F 9/38

②① Aktenzeichen: 100 28 397.7
②② Anmeldetag: 13. 6. 2000
④③ Offenlegungstag: 20. 12. 2001

DE 100 28 397 A 1

⑦① Anmelder:
PACT Informationstechnologie GmbH, 80807
München, DE

⑦④ Vertreter:
Pietruk, C., Dipl.-Phys., Pat.-Anw., 76229 Karlsruhe

⑦② Erfinder:
Vorbach, Martin, 80689 München, DE

Die folgenden Angaben sind den vom Anmelder eingereichten Unterlagen entnommen

- ⑤④ Registrierverfahren
⑤⑦ Beschrieben wird ein Verfahren zum Betrieb einer umkonfigurierbaren Einheit. Es wird dabei vorgeschlagen, dass Quittierungssignale der die umkonfigurierbaren Einheit bildenden Zellen zeitlich versetzt zu deren Konfiguration ausgewertet werden.

DE 100 28 397 A 1

DE 100 28 397 A 1

Beschreibung

Aufgabe der Erfindung und Anwendungsbereiche

- 5 [0001] RDY/ACK/REJ-Protokoll und Deadlock-Freiheit.
[0002] Das aus PACT10 bekannte RDY/ACK/REJ Protokoll kann nicht über mehrere Register gepipelined werden.
[0003] Zur Erhöhung der Grundfrequenz einer VPU sind mehrere Registerstufen jedoch zwingend notwendig. Dadurch ergibt sich eine unakzeptable Verzögerung bis zum Eintreffen der Quittierung der Konfigurationsdaten bei dem CT.
10 [0004] Es werden im folgenden zwei grundlegende Lösungen für dieses Problem aufgezeigt:

1. Lookup-Tabellen

- [0005] In eine CT oder 2602 interne Tabelle wird der Zustand der einzelnen PAEs verwaltet. D. h. für jede PAE existiert ein Eintrag, der anzeigt ob die PAE unkonfiguriert werden kann.

- a) Jede PAE sendet ein Statussignal an die Tabelle wenn sich ihr Zustand von "nicht unkonfigurierbar" auf "konfigurierbar" ändert. Dieses Statussignal kann gepipelined gesendet werden.
b) Ebenfalls ist es möglich, daß ein Statussignal für eine Gruppe von PAEs gesendet wird, das anzeigt, daß sich der Zustand für die gesamte Gruppe geändert hat. Über eine Liste werden sämtliche PAEs die zur Gruppe gehören ausgewählt und der Zustand für jede einzelne PAE in der Tabelle geändert.

- [0006] Zur Überprüfung des Zustandes einer PAE wird

- a) vor dem Ausführen der pa-Befehle wird jede darin enthaltene PAE geprüft, indem für jede PAE ein Lookup in der Tabelle durchgeführt wird. Eine nicht konfigurierbare PAE führt zu einem Abbruch, der pa-Befehl wird nicht ausgeführt; oder
b) beim Absenden der Adresse der Ziel-PAE durch ein pa-Befehl wird die Lookuptabelle abgefragt und dementsprechend ein ACK oder REJ generiert (dieser Ansatz entspricht dem herkömmlichen RDY/ACK/REJ Verfahren).

2. Auswerten der ACK/REJ Quittierung mit Latency

- [0007] Das RDY-Signal wird mit den Konfigurationsdaten über mehrere Pipeline-Stufen an die Ziel-PAE gesendet. Die Konfigurationsdaten werden nicht sofort im entsprechenden Konfigurationsregister gespeichert, sondern in ein temporäres Register geschrieben. Die PAE generiert die ACK/REJ-Quittierung gemäß des intern verwalteten Unkonfigurationsstatus (vgl. PACT10). Die Quittierung wird ebenfalls gepipelined an die CT zurückgesendet. In der CT existiert ein Zähler der bei jedem eintreffenden ACK um eins erhöht wird. In einem separaten Register wird gespeichert, ob ein REJ auftrat wurde.

- [0008] Nachdem der pa-Befehl abgeschlossen wurde wird nach einer Latency von n-Takten der Zähler und das Register ausgewertet. Ist in dem Register ein REJ vermerkt, muß der pa-Befehl nochmals ausgeführt werden. Dazu wird der Zählerstand entweder in den Offsetspeicher kopiert (pabmm) oder in das angegebene Register gespeichert (pabmr). Der Wert repräsentiert das Konfigurationswort, das mit einem REJ-quittiert wurde und nochmals ausgeführt werden muß.

- [0009] Terminiert der pa-Befehl ohne Auftreten eines REJ wird ein Signal STORE an die beteiligten PAEs gesendet. Daraufhin werden die Konfigurationswörter von dem temporären Register in das entsprechende Konfigurationsregister geschrieben und die Datenoperationen werden gestartet.

- [0010] IST DAS SAUBER? DEADLOCK, was ist mit PAEs, die nach dem REJ aufgrund der Latency noch Daten abbekamen?!

- [0011] Keine OK-Leitung verwenden, sondern ein Register bei den entsprechenden PAEs einfuehren.

Wave-Reconfiguration

- [0012] Durch eine geeignete Hardwarearchitektur (vgl. Fig. 10/11) ist es möglich mehrere Module zu überlappen. D. h. mehrere Module sind gleichzeitig in den PAEs vorkonfiguriert und es kann mit minimalem Zeitaufwand zwischen den Konfigurationen umgeschaltet werden, so daß aus einer Menge von mehreren Konfigurationen pro PAE immer genau eine Konfiguration aktiviert ist.

- [0013] Wesentlich ist, daß dabei in einer Menge von PAEs in die ein Modul A und B vorkonfiguriert ist, ein Teil der Menge mit einem Teil von A und eine anderer Teil der Menge gleichzeitig mit einem Teil B aktiviert sein kann. Dabei ist die Trennung der beiden Teile exakt durch die PAE gegeben, in der der Umschaltzustand zwischen A und B auftritt. Das bedeutet, daß ausgehend von einem bestimmten Zeitpunkt bei allen PAEs bei denen vor diesem Zeitpunkt A zur Ausführung aktiviert war B aktiviert ist und bei allen anderen PAEs nach diesem Zeitpunkt immer noch auf A aktiviert ist. Mit steigender Zeit wird bei immer mehr PAEs B aktiviert.

- [0014] Die Umschaltung erfolgt aufgrund von bestimmten Daten, Zuständen die sich aus der Berechnung der Daten ergeben oder aufgrund beliebiger anderer Ereignisse, die beispielsweise von extern oder der CT generiert werden.

- [0015] Das bewirkt, daß direkt nach Verarbeitung eines Datenpaketes zu einer anderen Konfiguration umgeschaltet werden kann. Gleichzeitig/Alternativ kann ein Signal (RECONFIG-TRIGGER) an den CT gesendet werden, das das Vorladen von neuen Konfigurationen durch den CT bewirkt. Das Vorladen kann dabei auf anderen von der aktuellen Datenverarbeitung abhängigen oder unabhängigen PAEs erfolgen. Durch eine Entkopplung der aktiven Konfiguration von

den zur Unkonfiguration zur Verfügung stehenden Konfigurationen (vgl. **Fig. 10/11**) können auch gerade arbeitende (aktive) PAEs, insbesondere auch die PAE, die den RECONFIG-TRIGGER erzeugt, mit neuen Konfigurationen geladen werden. Dies ermöglicht eine mit der Datenverarbeitung überlappende Konfiguration.

[0016] In **Fig. 13** ist das Grundprinzip der Wave-Reconfiguration (WRC) dargestellt. Dabei wird von einer Reihe von PAEs (PAE1–9) ausgegangen, durch die die Daten pipelineähnlich laufen. Es wird ausdrücklich darauf hingewiesen, daß WRC nicht auf Pipelines beschränkt ist und die Vernetzung und Gruppierung der PAEs jede beliebige Form annehmen kann. Die Darstellung wurde jedoch gewählt um ein einfaches Beispiel zum besseren Verständnis zu zeigen.

[0017] In **Fig. 13a** läuft ein Datenpaket in die PAE1. Die PAE besitzt 4 mögliche Konfigurationen (A, F, H, C), die durch eine geeignete Hardware (vgl. **Fig. 10/11**) wählbar sind. Die Konfiguration F ist in in PAE1 für das aktuelle Datenpaket aktiviert (schraffiert dargestellt).

[0018] Im nächsten Takt läuft das Datenpaket nach PAE2 und ein neues Datenpaket erscheint in PAE1. Auch in PAE2 ist F aktiv. Zusammen mit dem Datenpaket erscheint ein Ereignis (↑1) bei PAE1. Das Ereignis entsteht durch Eintreffen eines beliebigen Ereignisses von aussen bei der PAE (z. B. eines Statusflags oder Triggers) oder wird innerhalb der PAE durch die ausgeführte Berechnung generiert.

[0019] In **Fig. 13c** wird in PAE1 aufgrund des Ereignisses (↑1) die Konfiguration H aktiviert, gleichzeitig erscheint ein neues Ereignis (↑2), das im nächsten Takt (**Fig. 13d**) die Aktivierung von Konfiguration A bewirkt.

[0020] In **Fig. 13e** trifft (↑3) bei PAE1, die das Überschreiben von F mit G bewirkt (**Fig. 13f**). Durch das Eintreffen von (↑4) wird G aktiviert (**Fig. 13g**). (↑5) bewirkt das Laden von K anstelle von C (**Fig. 13h, i**) und (↑6) lädt und startet F anstelle von H (**Fig. 13j**).

[0021] In den **Fig. 13g*)** bis **13j*)** wird verdeutlicht, daß beim Durchlaufen einer Wave-Reconfiguration nicht alle PAEs nach demselben Muster arbeiten müssen. Wie eine PAE von einer Wave-Reconfiguration konfiguriert wird, ist prinzipiell abhängig von ihrer eigenen Konfiguration. Hier soll dargestellt werden, daß PAE4 bis PAE6 derart konfiguriert sind, daß sie anders auf die Ereignisse reagieren, als die übrigen PAEs. Beispielsweise wird in **Fig. 13g*)** aufgrund von Ereignis ↑2 nicht A sondern H aktiviert (vgl. **Fig. 13g**). Dasselbe gilt für **13h*)**. Aufgrund von Ereignis ↑3 wird in **Fig. 13i*)** nicht G geladen, sondern die Konfiguration F bleibt bestehen und A bleibt aktiviert. In **Fig. 13j*)** ist bei PAE7 angedeutet, daß Ereignis ↑3 wieder das Laden von G auslösen wird. In PAE4, bewirkt das Ereignis ↑4 das Aktivieren von F anstatt der Konfiguration G (vgl. **Fig. 13j**).

[0022] In **Fig. 13** bewegt sich eine Welle von Umkonfigurationen aufgrund von Ereignissen durch eine Menge von PAEs, die 2- oder mehrdimensional ausgestaltet sein kann.

[0023] Es ist nicht zwingend notwendig, daß eine einmal stattfindende Umkonfiguration durch die gesamten Fluß hinweg stattfindet. Beispielsweise könnte die Umkonfiguration mit der Aktivierung von A aufgrund des Ereignisses (↑2) nur lokal in den PAEs1 bis 3 und PAE7 stattfinden, während in allen anderen PAEs weiterhin die Konfiguration H aktiviert bleibt.

[0024] Mit anderen Worten:

- a) Es ist möglich, daß ein Ereignis nur lokal auftritt und daher nur lokal eine Umaktivierung zur Folge hat,
- b) ein globales Ereignis, hat möglicherweise keine Auswirkung auf manche PAEs; abhängig vom ausgeführten Algorithmus.

[0025] Bei den PAEs die nach (↑2) weiterhin H aktiviert halten, kann selbstverständlich das Eintreffen des Ereignisses (↑3) vollkommen andere Auswirkungen haben, (i) wie etwa das Aktivieren von C statt dem Laden von G, (ii) andererseits könnte (↑3) auf diese PAEs auch gar keinen Einfluß haben.

Das Prozessormodell

[0026] Die in den folgenden Figuren gezeigten Graphen besitzen als Graphenknotten immer in Modul, wobei davon ausgegangen wird, daß mehrere Module auf einen Zielbaustein abgebildet werden können. Das heißt, obwohl alle Module zeitlich voneinander unabhängig sind, wird nur bei den Modulen eine Umkonfiguration durchgeführt, und/oder ein Datenspeicher eingefügt, die mit einem vertikalen Strich und Δt markiert sind. Dieser Punkt wird Umkonfigurationszeitpunkt genannt.

[0027] Der Umkonfigurationszeitpunkt ist abhängig von den bestimmten Daten oder den Zuständen die sich aus der Verarbeitung der bestimmten Daten ergeben.

[0028] Das bedeutet zusammenfassend:

1. Große Module können an geeigneten Stellen partitioniert werden und in kleine zeitlich voneinander unabhängige Module zerlegt werden, die optimal in das Array aus PAEs passen.
2. Bei kleinen Modulen die gemeinsam auf einen Zielbaustein abgebildet werden können, wird auf die zeitliche Unabhängigkeit verzichtet. Dadurch werden Konfigurationsschritte eingespart und die Datenverarbeitung beschleunigt.
3. Die Umkonfigurationszeitpunkte werden entsprechend der Ressourcen der Zielbausteine positioniert. Dadurch ist eine beliebige Skalierung der Graphenlänge gegeben.
4. Module können überlagert konfiguriert werden.
5. Die Umkonfiguration von Modulen wird durch die Daten selbst oder dem Ergebnis der Verarbeitung der Daten gesteuert.
6. Die von den Modulen generierten Daten werden gespeichert und die zeitlich nachfolgenden Module lesen die Daten aus diesem Speicher aus und speichern die Ergebnisse wiederum in einen Speicher oder geben das Endergebnis an die Peripherie aus.

[0029] Zur Bestimmung der Zustände innerhalb eines Graphen werden die Statusregister der einzelnen Zellen (PAEs) über ein zusätzlich zum Datenbus (0801) existierendes, frei rout- und segmentierbares Status-Bussystem (0802) allen anderen Rechenwerken zur Verfügung gestellt (Fig. 8b). Das bedeutet, daß eine Zelle (PAE X) die Statusinformation einer andern Zelle (PAE Y) evaluieren kann und dementsprechend die Daten verarbeitet. Um den Unterschied zu bestehenden Parallelrechnersystemen zu verdeutlichen, ist in Fig. 8a der Stand der Technik angegeben. Dabei ist ein Multiprozessor-system gezeigt, dessen Prozessoren über einen gemeinsamen Datenbus (0803) miteinander verbunden sind. Ein explizites Bussystem für den synchronen Austausch von Daten und Status existiert nicht.

[0030] Mit anderen Worten ausgedrückt, stellt das Netzwerk der Statussignale (0802) ein frei und gezielt verteiltes Statusregister eines einzelnen herkömmlichen Prozessors (oder mehrerer Prozessoren eines SMP-Computers) dar. Der Status jeder einzelnen ALU (bzw. jedes einzelnen Prozessors) und insbesondere jede einzelne Information des Status steht jeweils dem oder den ALUs (Prozessoren) zur Verfügung, die die Information benötigen. Dabei entsteht keine zusätzliche Programm- oder Kommunikationslaufzeit (abgesehen von den Signallaufzeiten) um die Informationen zwischen den ALUs (Prozessoren) auszutauschen.

[0031] Abschließend soll angemerkt werden, daß je nach Aufgabe sowohl der Datenflußgraph, als auch der Kontrollflußgraph entsprechend dem beschriebenen Verfahren behandelt werden kann.

Virtual Machine Modell

[0032] Die Grundlagen der Datenverarbeitung mit VPU-Bausteinen sind entsprechend der vorhergehenden Abschnitte hauptsächlich datenflußorientiert. Um sequentielle Programme mit ordentlicher Leistung abzuarbeiten, ist es jedoch notwendig ein sequentielles Datenverarbeitungsmodell zur Verfügung zu haben. Dabei sind oftmals die Sequenzen in den einzelnen PAEs nicht ausreichend.

[0033] Die Architektur von VPUs ermöglicht jedoch grundsätzlich den Aufbau von beliebig komplexen Sequenzern aus einzelnen PAEs.

[0034] Das bedeutet:

1. Es können komplexe Sequenzen konfiguriert werden, die exakt den Anforderungen des Algorithmus entsprechen.
2. Der Datenfluß kann durch entsprechende Konfiguration, exakt die Rechenschritte des Algorithmus repräsentieren.

[0035] Dadurch kann eine Virtuelle Maschine auf VPUs implementiert werden, die insbesondere auch den sequentiellen Anforderungen eines Algorithmus entspricht.

[0036] Hauptvorteil der VPU-Architektur ist, daß ein Algorithmus durch einen Compiler so zerteilt werden kann, daß die Datenflußteile extrahiert werden durch einen "optimalen" Datenfluß repräsentiert werden, indem ein angepaßter Datenfluß konfiguriert wird UND die sequentiellen Teile des Algorithmus durch einen "optimalen" Sequenzer repräsentiert werden, indem ein angepaßter Sequenzer konfiguriert wird. Dabei können gleichzeitig mehrere Sequenzen und Datenflüsse auf einer VPU untergebracht werden, ausschließlich abhängig von den zur Verfügung stehenden Ressourcen.

[0037] Durch die große Anzahl an PAEs entstehen im Betrieb innerhalb einer VPU sehr viele lokalen Zustände. Bei Taskwechseln oder Unterprogramm-Aufrufen (Interrupts) müssen diese Zustände gesichert werden (vgl. PUSH/POP bei Standardprozessoren). Dies ist jedoch aufgrund der Menge an Zuständen nicht sinnvoll möglich.

[0038] Um die Zustände auf eine handhabbare Menge zu reduzieren muß zwischen zwei Arten von Zuständen unterschieden werden:

1. Zustandsinformationen des Maschinenmodells (MACHINE-STATE). Diese Zustandsinformationen sind nur innerhalb der Abarbeitung eines bestimmten Modules gültig und werden auch nur lokal in den Sequenzern und Datenflußeinheiten dieses bestimmten Modules verwendet. D. h. diese MACHINE-STATES repräsentieren die Zustände, die in Prozessoren nach dem Stand der Technik verdeckt innerhalb der Hardware ablaufen, implizit in den Befehlen und den Verarbeitungsschritten sind und nach Ablauf eines Befehles keine weitere Information für nachfolgende Befehle beinhalten. Derartige Zustände brauchen nicht gesichert zu werden. Bedingung dafür ist, daß Interrupts nur nach kompletter Ausführung aller gerade aktiven Module durchgeführt werden. Stehen Interrupts zur Ausführung an, werden keine neuen Module geladen, sondern nur noch aktive abgearbeitet; ebenfalls werden den aktiven Modulen, soweit es der Algorithmus zuläßt keine neuen Operanden mehr zugeführt. Dadurch wird ein Modul zu einer atomaren nicht unterbrechbaren Einheit, vergleichbar mit einer Instruktion eines Prozessors nach dem Stand der Technik.

2. Zustände der Datenverarbeitung (DATA-STATE). Die datenbezogenen Zustände müssen beim Auftreten eines Interrupts entsprechend den Prozessormodellen nach dem Stand der Technik gesichert und in den Speicher geschrieben werden. Das sind bestimmte notwendige Register und Flags oder – entsprechend der Begriffe der VPU-Technologie – Trigger.

[0039] Bei den DATA-STATES kann die Handhabung je nach Algorithmus weiter vereinfacht werden. Zwei grundlegende Strategien werden im Folgenden näher erläutert:

1. Mitlaufen der Zustandsinformation

[0040] Dabei werden alle relevanten und zu einem späteren Zeitpunkt benötigten Zustandsinformationen von einem

Modul zum nächsten übertragen, wie es in Pipelines oftmals standardmäßig implementiert ist. Die Zustandsinformationen werden dann zusammen mit den Daten implizit in einem Speicher abgelegt, sodaß die Zustände bei einem Abruf der Daten zugleich zur Verfügung stehen. Ein explizites Handhaben der Zustandsinformationen i. b. mittels PUSH und POP entfällt dadurch, was je nach Algorithmus einerseits zu einer wesentlichen Beschleunigung der Abarbeitung und andererseits zu einer vereinfachten Programmierung führt.

[0041] Die Zustandsinformaton kann wahlweise entweder mit dem jeweiligen Datenpaket gespeichert werden, oder nur im Falle eines Interrupts gesichert und besonders gekennzeichnet werden.

2. Sichern der Reentry Adresse

[0042] Bei der Verarbeitung von großen Datenmengen, die in einem Speicher abgelegt sind, ist kann es sinnvoll sein die Adresse mindestens einer der Operanden des gerade verarbeiteten Datenpaketes mit dem Datenpaket zusammen durch die PAEs zu leiten. Dabei wird die Adresse nicht modifiziert sondern steht beim Schreiben des Datenpaketes in ein RAM als Pointer auf den letzten verarbeiteten Operanden zur Verfügung.

[0043] Dieser Pointer kann wahlweise entweder mit dem jeweiligen Datenpaket gespeichert werden, oder nur im Falle eines Interrupts gesichert und besonders gekennzeichnet werden. Insbesondere, wenn sämtliche Pointer auf die Operanden durch eine Adresse (oder eine Gruppe von Adressen) berechnet werden können ist es sinnvoll nur eine Adresse (oder eine Gruppe von Adressen) zu sichern.

"ULIW"-/ "UCISC"-Modell

[0044] Für das Verständnis dieses (einem Prozessor nach dem Stand der Technik sehr ähnlichen) Modells ist eine Erweiterung der Betrachtungsweise der Architektur von VPUs erforderlich. Dabei dient das Virtual-Machine Modell als Grundlage.

[0045] Das Array aus PAEs (PA) wird als in ihrer Architektur konfigurierbare Recheneinheit betrachtet. Der/die CT(s) stellen eine Ladeeinheit (LOAD-UNIT) für Opcodes dar. Die IOAG(s) übernehmen das Businterface und/oder den Registersatz.

[0046] Diese Anordnung ermöglicht zwei grundsätzliche Funktionsweisen, die im Betrieb gemischt verwendbar sind:

1. Eine Gruppe von PAEs (das kann auch eine PAE sein) wird zur Ausführung eines komplexen Befehls oder Befehlsfolge konfiguriert und danach werden die auf diesen Befehl bezogenen Daten (das kann auch ein einziges Datenwort sein) verarbeitet. Danach wird diese Gruppe umkonfiguriert, zur Abarbeitung des nächsten Befehles. Dabei kann sich die Größe und Anordnung der Gruppe ändern. Gemäß den bereits besprochenen Partitionierungstechnologien obliegt es dem Compiler, möglichst optimale Gruppen zu schaffen. Durch den CT werden Gruppen als Befehle auf den Baustein "geladen", dadurch ist des Verfahren mit dem bekannten VLIW vergleichbar, nur daß erheblich mehr Rechenwerke verwaltet werden UND die Vernetzungsstruktur zwischen den Rechenwerken ebenfalls vom Instruktionswort abgedeckt werden kann (Ultra Large Instruction Word = "ULIW"). Dadurch läßt sich ein sehr hoher Instruktion Level Parallelism (ILP) erreichen. (siehe auch **Fig. 27**). Ein Instruktionswort entspricht dabei einem Modul. Mehrere Module können gleichzeitig verarbeitet werden, sofern es die Abhängigkeit der Daten zuläßt und genügend Ressourcen auf dem Baustein frei sind. Wie bei VLIW-Befehlen wird für gewöhnlich nach Ausführen des Instruktionswortes sofort das nächste Instruktionswort geladen. Zur zeitlichen Optimierung ist es dabei möglich das nächste Instruktionswort bereits während der Ausführung vorzuladen (vgl. **Fig. 10**). Bei mehreren möglichen nächsten Instruktionsworten können mehrere vorgeladen werden und vor der Ausführung wird z. B. durch ein Triggersignal das korrekte Instruktionswort ausgewählt. (siehe **Fig. 4a B1/B2**, **Fig. 15 ID C/D K**, **Fig. 36 A/B/C**)

2. Eine Gruppe von PAEs (das kann auch eine PAE sein) wird zur Ausführung einer häufig gebrauchten Befehlsfolge konfiguriert. Die Daten, das kann auch hier ein einzelnes Datenwort sein, werden bei Bedarf der Gruppe zugeführt und von der Gruppe empfangen. Diese Gruppe bleibt über eine Vielzahl von Takten ohne Umkonfiguration bestehen. Vergleichbar ist diese Anordnung mit einem speziellen Rechenwerk in einem Prozessor nach dem Stand der Technik (z. B. MMX), das für Spezialaufgaben vorgesehen ist und nur bei Bedarf verwendet wird. Durch diesen Ansatz sind Spezialbefehle entsprechend des CISC-Prinzipes generierbar, mit dem Vorteil, daß diese Befehle anwendungsspezifisch geschaffen werden können (Ultra-CISC = "UCISC").

Erweiterung des RDY/ACK-Protokolls (vgl. PACT02)

[0047] In PACT02 ist ein RDY/ACK-Standardprotokoll beschrieben, das die wesentlichen Anforderungen gemäß den Synchronisationen von DE 44 16 881 in Hinblick auf eine typische Datenflußapplikation beschreibt. Nachteil des Protokolls ist, daß lediglich Daten gesendet und der Empfang bestätigt werden kann. Der umgekehrte Fall, indem Daten angefordert werden und das Versenden bestätigt wird (im Folgenden REQ/ACK genannt, ist zwar elektrisch mit demselben Zweidrahtprotokoll lösbar, jedoch semantisch nicht erfaßt. Das gilt insbesondere, wenn REQ/ACK und RDY/ACK gemischt betrieben werden.

[0048] Daher wird die klare Unterscheidung der Protokolle eingeführt:

RDY: Daten liegen beim Versender für den Empfänger bereit

REQ: Daten werden vom Empfänger beim Versender angefordert

ACK: Allgemeine Bestätigung für erfolgten Empfang oder Versand

(Prinzipiell könnten auch zwischen ACK für ein RDY und einem ACK für ein REQ unterschieden werden, jedoch ist in den Protokollen die Semantik des ACKs für gewöhnlich implizit).

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Speichermodell

5 **[0049]** In VPU's können Speicher integriert werden (einer oder mehrere), die ähnlich einer PAE angesprochen werden. Es wird im folgenden ein Speichermodell beschrieben, das gleichzeitig ein Interface zu externer Peripherie und/oder externem Speicher darstellt:

[0050] Ein VPU-interner Speicher mit PAE-ähnlichen Busfunktionen kann verschiedene Speichermodi darstellen:

1. Standardspeicher (Random Access)
2. Cache (als Erweiterung des Standardspeichers)
- 10 3. Lookup-Tabelle
4. FIFO
5. LIFO (Stack)

[0051] Dem Speicher ist ein steuerbares Interface zugeordnet, das Speicherbereiche wahlweise wort- oder blockweise schreibt oder liest.

[0052] Dadurch ergeben sich folgende Nutzungsmöglichkeiten:

1. Entkopplung von Datenströmen (FIFO)
- 20 2. Schneller Zugriff auf selektierte Speicherbereiche eines externen Speichers, was eine Cacheähnliche Funktion darstellt (Standardspeicher, Lookup-Tabelle)
3. Stack mit variierbarer Tiefe (LIFO)

[0053] Dabei kann das Interface benutzt werden, es ist jedoch nicht zwingend notwendig, wenn die Daten z. B. ausschließlich lokal in der VPU verwendet werden und der Speicherplatz eines internen Speichers ausreicht.

Stack Modell

30 **[0054]** Durch Verwendung des REQ/ACK-Protokolls und der internen Speicher im LIFO-Modus kann ein einfacher Stack-Prozessor aufgebaut werden. Dabei werden temporäre Daten von den PAEs auf den Stack geschrieben und bei Bedarf von dem Stack geladen. Die hierfür notwendigen Compilertechnologien sind hinreichend bekannt. Durch die variierbare Stacktiefe, die durch einen Datenaustausch des internen Speicher mit einem externen Speicher erreicht wird, kann der Stack beliebig groß werden.

Akkumulator Modell

35 **[0055]** Jede PAE kann eine Recheneinheit nach dem Akkumulatorprinzip darstellen. Wie aus PACT02 bekannt ist es möglich die Ausgangsregister auf den Eingang der PAE rückzukoppeln. Dadurch entsteht ein Akkumulator nach dem Stand der Technik. In Verbindung mit dem Sequenzer nach **Fig. 11** lassen sich einfache Akkumulator-Prozessoren aufbauen.

Register Modell

40 **[0056]** Durch Verwendung des REQ/ACK-Protokolls und der internen Speicher im Standardspeicher-Modus kann ein einfacher Register-Prozessor aufgebaut werden. Dabei werden die Registeradressen von einer Gruppe von PAEs generiert, während eine andere Gruppe von PAEs die Verarbeitung der Daten übernimmt.

Architektur des Speichers

50 **[0057]** Der Speicher besitzt zwei Interface. Ein erstes, das den Speicher mit dem Array verbindet und ein zweites, das den Speicher mit einer IO-Einheit verbindet. Zur Verbesserung der Zugriffszeit sollte der Speicher als Dual-Ported-RAM ausgestaltet sein, wodurch Schreib- und Lesezugriffen unabhängig voneinander erfolgen können.

[0058] Das erste Interface ist übliches PAE-Interface (PAEI), das den Zugang zum Bussystem des Arrays gewährleistet, sowie die Synchronisation und Triggerverarbeitung sicherstellt. Trigger können verwendet werden und verschiedene Zustände des Speichers anzuzeigen oder Aktionen im Speicher zu erzwingen, beispielsweise

- 55 1. Empty/Full: Beim Einsatz als FIFO wird der FIFO-Zustand "voll", "fast-voll", "leer", "fast-leer" angezeigt;
2. Stack overrun/underrun: Beim Einsatz als Stack werden Überlauf und Unterlauf des Stacks signalisiert;
3. Cache hit/miss: Im Cache-Mode wird angezeigt, ob eine Adresse im Cache gefunden wurde;
4. Cache flush: Durch einen Trigger wird das Schreiben des Caches in den externen RAM erzwungen.

60 **[0059]** Dem PAE-Interface zugeordnet ist eine konfigurierbare Zustandsmaschine, die die verschiedenen Betriebsarten steuert. Der Zustandsmaschine ist ein Zähler zugeordnet um die Adressen im FIFO- und LIFO-Modus zu generieren. Die Adressen werden über einen Multiplexer an den Speicher geführt, damit zusätzlich Adressen, die im Array generiert werden an den Speicher geführt werden können.

65 **[0060]** Das zweite Interface dient zum Anschluß einer IO-Einheit (IOI). Die IO-Einheit ist als konfigurierbarer Controller mit einem externen Interface ausgestaltet. Der Controller liest oder schreibt wort- oder blockweise Daten in bzw. aus dem Speicher. Die Daten werden mit der IO-Einheit ausgetauscht. Weiterhin unterstützt der Controller mittels eines zusätzlichen TAG-Speichers diverse Cache-Funktionen.

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[0061] IOI und PAEI sind miteinander synchronisiert, sodaß keine Kollision der beiden Interface eintritt. Die Synchronisation ist je nach Betriebsart unterschiedlich, während beispielsweise im Standardspeicher- oder Stack-Mode immer nur entweder das IOI oder das PAEI auf den gesamten Speicher zugreifen kann, ist im FIFO-Modus die Synchronisation zeilenweise, d. h. während IOI auf eine Zeile x zugreift, kann das PAEI auf jede andere Zeile ungleich x gleichzeitig zugreifen.	5
[0062] Die IO-Einheit wird entsprechend der peripheren Erfordernisse ausgestaltet, beispielsweise:	
1. SDRAM Kontroller	
2. RDRAM Kontroller	
3. DSP-Bus Kontroller	10
4. PCI Kontroller	
5. Serieller Kontroller (z. B. NGIO)	
6. Spezial Purpose Kontroller (SCSI, Ethernet, USB, etc.)	
[0063] Eine VPU kann beliebige Speicherelemente mit beliebigen IO-Einheiten besitzen. Dabei können unterschiedliche IO-Einheiten auf einer VPU implementiert sein.	15
Funktionsweise	
1. Standardspeicher	20
1.1 intern/lokal	
[0064] Über das PAEI werden Daten und Adressen mit Speicher ausgetauscht. Die adressierbare Speichergröße ist durch die Speichergröße beschränkt.	25
1.2 extern/memory mapped window	
[0065] Über das PAEI werden Daten und Adressen mit dem Speicher ausgetauscht. Im Kontroller des IOI ist eine Basisadresse im externen Speicher angegeben. Der Kontroller liest blockweise Daten von der externen Speicheradresse und schreibt sie in den Speicher, wobei die internen und externen Adressen jeweils inkrementiert (oder dekrementiert) werden; so lange, bis der gesamte interne Speicher übertragen wurde oder eine voreingestellte Grenze erreicht wurde. Das Array arbeitet mit den lokalen Daten, bis diese vom Kontroller wieder in den externen Speicher geschrieben werden. Das Schreiben verläuft analog dem beschriebenen Lesevorgang.	30
[0066] Das Lesen und Schreiben durch den Kontroller kann	35
a) durch Trigger angestoßen werden oder	
b) durch einen Zugriff des Arrays auf eine nicht lokal	
gespeicherte Adresse. Greift das Array auf eine derartige Adresse zu, wird zunächst der interne Speicher in den externen geschrieben und danach der Speicherblock um die gewünschte Adresse nachgeladen.	40
[0067] Diese Betriebsart ist besonders für die Implementierung eines Registersatzes für einen Registerprozessor interessant. Durch einen Trigger kann in diesem Fall das Push/Pop des Registersatzes mit dem externen Speicher für einen Taskwechsel oder eine Kontextumschaltung realisiert werden.	45
1.3 extern/lookup table	
[0068] Die Lookup Tabellen Funktion ist eine Vereinfachung von 1.2. Dabei werden die Daten entweder einmal oder mehrmals durch einen CT-Aufruf oder einen Trigger vom externen RAM in den internen gelesen. Das Array liest Daten aus dem internen Speicher, schreibt jedoch keine Daten in den internen Speicher. Die Basisadresse im externen Speicher ist im Kontroller entweder durch die CT oder das Array gespeichert und kann zur Laufzeit verändert werden. Das Laden aus dem externen Speicher wird entweder von der CT oder durch einen Trigger aus dem Array ausgelöst und kann ebenfalls zur Laufzeit geschehen.	50
1.4 extern/cached	55
[0069] In diesem Modus greift das Array wahlweise auf den Speicher zu. Der Speicher arbeitet wie ein Cache-Speicher für den externen Speicher nach dem Stand der Technik. Durch einen Trigger aus dem Array oder durch die CT kann das Leeren des Caches (d. h. das vollständige Schreiben des Caches in den externen Speicher) hervorgerufen werden.	60
2. FIFO	
[0070] Der FIFO-Modus wird üblicherweise verwendet, wenn Datenströme von extern an die VPU geführt werden. Dann dient der FIFO als Entkopplung zwischen der externen Datenverarbeitung und der VPU-internen Datenverarbeitung, derart daß entweder von extern auf den FIFO geschrieben wird und von der VPU gelesen oder genau umgekehrt. Die Zustände des FIFOs werden durch Trigger zum Array und ggf. auch nach extern signalisiert. Der FIFO selbst wird nach dem Stand der Technik mit unterschiedlichen Schreib- und Lesezeigern implementiert.	65

3. Stack/intern

[0071] Durch ein Adressregister wird ein interner Stack aufgebaut. Bei jedem Schreibzugriff auf den Speicher durch das Array wird das Register je nach Mode (a) inkrementiert (b) dekrementiert. Bei Lesezugriffen vom Array aus wird das Register umgekehrt (a) dekrementiert und (b) inkrementiert. Das Register stellt für jeden Zugriff die erforderliche Adresse zur Verfügung. Der Stack ist durch die Größe des Speichers begrenzt. Fehler (Überlauf/Unterlauf) werden durch Trigger angezeigt.

4. Stack/extern

[0072] Sofern der interne Speicher zu klein für den Aufbau eines Stacks ist, kann er in den externen Speicher ausgelagert werden. Dazu besteht im Kontroller ein Adresszähler für die externe Stackadresse. Wird eine bestimmte Menge an Einträgen im internen Stack überschritten, wird blockweise eine Anzahl von Einträgen auf den externen Stack geschrieben. Der Stack wird vom Ende her, also vom ältesten Eintrag aus nach extern geschrieben, wobei eine Menge von neuesten Einträgen nicht nach extern geschrieben wird, sondern intern verbleibt. Der externe Adresszähler (ERC) wird zeilenweise modifiziert.

[0073] Nachdem Platz im internen Stack geschaffen wurde muß der verbleibende Stack-Inhalt an den Beginn des Stacks bewegt werden, die interne Stackadresse wird entsprechend angepaßt.

[0074] Eine effizientere Variante ist das Auslegen des Stacks als Ringspeicher (vgl. PACT04). Ein interner Adresszähler wird durch das Hinzufügen oder Entfernen von Stackeinträgen modifiziert. Sobald der interne Adresszähler (IAC) am oberen Ende des Speichers überschreitet, zeigt er auf die unterste Adresse. Unterschreitet der IAC die unterste Adresse, zeigt er auf die oberste. Ein zusätzlicher Zähler (FC) zeigt den Füllstand des Speichers an, d. h. mit jedem geschriebenen Wort wird der Zähler inkrementiert, mit jedem gelesenen dekrementiert. Anhand des FC ist erkennbar, wann der Speicher leer, bzw. voll ist. Diese Technologie ist von FIFOs bekannt. Wird damit ein Block in den externen Speicher geschrieben, reicht die Anpassung des FC um den Stack zu aktualisieren. Ein externer Adresszähler (EAC) zeigt immer auf den ältesten im internen Speicher befindlichen Eintrag und befindet sich damit an dem IAC entgegengesetzten Ende des Stacks. Der EAC wird modifiziert, wenn

- (a) Daten auf den externen Stack geschrieben werden, dann läuft er in Richtung des IAC,
- (b) Daten vom externen Stack gelesen werden, dann entfernt er sich vom IAC.

[0075] Durch Überwachung des FC wird sichergestellt, daß IAC und EAC nicht kollidieren.

[0076] Der ERC wird entsprechend der externen Stackoperation (Auf- oder Abbau) modifiziert.

MMU

[0077] Dem externen Speicherinterface kann eine MMU zugeordnet werden, die zwei Funktionen erfüllt:

- 1. Umrechnung der internen Adressen auf externe Adressen zur Unterstützung moderner Betriebssysteme
- 2. Überwachung der Zugriffe auf externe Adressen, z. B. generieren eines Fehlersignales als Trigger, wenn der externe Stack über- oder unterläuft.

Compiler

[0078] Das erfindungsgemäße Programmierprinzip der VPU-Technologie besteht darin, sequentiellen Code zu separieren und in möglichst viele kleine und unabhängige Teilalgorithmen zu zerlegen, während die Teilalgorithmen des Datenflußcodes direkt auf die VPU abgebildet wird.

Trennung zwischen VPU- und Standard-Kode

[0079] Innerhalb einer Sprache nach dem Stand der Technik repräsentativ für alle möglichen Compiler (Pascal, Java, Fortran, etc) soll C++ im weiteren verwendet werden, kann eine spezielle Erweiterung (VC = Vpu C) definiert werden, die die Sprachkonstrukte und Typen enthält, die besonders gut auf eine VPU-Technologie abbildbar sind. VCs dürfen vom Programmierer nur innerhalb von Prozeduren oder Funktionen verwendet werden, die keine anderen Konstrukte oder Typen verwenden. Diese Prozeduren und Funktionen sind direkt auf die VPU abbildbar und laufen besonders effizient ab. Der Compiler extrahiert die VC im Präprozessor und gibt sie direkt an das VC-Backend-Processing (VCBP) weiter.

Extraktion des parallelisierbaren Compiler-Kodes

[0080] Im nächsten Schritt analysiert der Compiler die restlichen C++ Codes und extrahiert die Teile (MC = mappable C), die gut parallelisierbar und ohne den Einsatz von Sequenzern auf die VPU-Technologie abbildbar sind. Jedes einzelne MC wird in ein virtuelles Array platziert und geroutet. Danach wird der Platzbedarf, sowie die zu erwartende Performance analysiert. Dazu wird das VCBP aufgerufen und die einzelnen MC werden zusammen mit den VC, die in jedem Fall abgebildet werden, partitioniert.

[0081] Die MCs, deren VPU-Implementierung den höchsten Leistungs-Zuwachs erzielen werden übernommen, die restlichen werden als C++ an die nächste Compilerstufe weitergereicht.

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Optimierender Sequenzer Generator

[0082]	Diese Compilerstufe ist je nach Architektur des VPU-Systems unterschiedlich implementierbar:	
	1. VPU ohne Sequenzer und externer Prozessor	5
[0083]	Sämtliche verbleibenden C++ Codes werden für den externen Prozessor kompiliert.	
	2. Nur VPU mit Sequenzer	10
	2.1 Sequenzer in den PAEs	
[0084]	Sämtliche verbleibenden C++ Codes werden für die Sequenzer der PAEs kompiliert.	
	2.2 Konfigurierbare Sequenzer im Array	15
[0085]	Der verbleibende C++ Code wird für jedes unabhängige Modul analysiert. Die jeweils am besten geeignete Sequenzer-Variante wird aus einer Datenbank ausgewählt und als VC-Code (SVC) abgelegt. Dieser Schritt ist meist iterativ, d. h. eine Sequenzer-Variante wird ausgewählt, der Code wird kompiliert, analysiert und mit dem kompilierten Code anderer Sequenzer-Varianten verglichen. Letztlich wird der Objectcode (SVCO) des C++ Codes für den gewählten SVC generiert.	20
	2.3 sowohl 2.1 als auch 2.2 werden verwendet	
[0086]	Die Funktionsweise entspricht der von 2.2. Für die Sequenzer in den PAEs bestehen besondere statische Sequenzer-Modelle in der Datenbank.	25
	3. VPU mit Sequenzer und externer Prozessor	
[0087]	Auch diese Funktionsweise entspricht 2.2. Für den externen Prozessor existieren besondere statische Sequenzer-Modelle in der Datenbank.	30
	Linker	
[0088]	Der Linker verbindet die einzelnen Module (VC, MC, SVC und SVCO) zu einem ausführbaren Programm. Dazu verwendet er das VCBP um die einzelnen Module zu platzieren, zu routen und die zeitliche Partitionierung festzulegen. Der Linker fügt ebenfalls die Kommunikationsstrukturen zwischen den einzelnen Modulen hinzu und fügt gegebenenfalls Register und Speicher ein. Aufgrund einer Analyse der Kontrollstrukturen und Abhängigkeiten der einzelnen Module werden Strukturen zum Speichern der internen Zustände des Arrays und der Sequenzer für den Fall einer Reconfiguration hinzugefügt.	35 40
	Bemerkungen zu den Prozessormodellen	
[0089]	Die verwendeten Maschinenmodell können innerhalb einer VPU beliebig kombiniert werden. Auch innerhalb eines Algorithmus kann je nach dem, welches Modell optimal ist, zwischen den Modellen gewechselt werden.	45
[0090]	Wird einem Register-Prozessor ein weiterer Speicher zugefügt, von dem die Operanden gelesen werden und in den die Ergebnisse geschrieben werden, kann eine Load/Store-Prozessor aufgebaut werden. Dabei können mehrere verschiedene Speicher zugeordnet werden, indem die einzelnen Operanden und das Ergebnis getrennt behandelt wird.	
[0091]	Diese Speicher arbeiten dann quasi als Load/Store-Einheit und stellen eine Art Cache für den externen Speicher dar. Die Adressen werden durch von der Datenverarbeitung separierte PAEs berechnet.	50
	Pointer Reordering	
[0092]	Hochsprachen wie C/C++ verwenden häufig Pointer, die sehr schlecht durch Pipelines gehandhabt werden können. Wenn ein Pointer erst direkt vor dem Verwenden der Datenstrukturen auf die er zeigt, berechnet wird, kann häufig die Pipeline nicht schnell genug gefüllt werden und die Verarbeitung wird speziell in VPUs ineffizient.	55
[0093]	Sicherlich ist es sinnvoll bei der Programmierung von VPUs möglichst keine Pointer zu verwenden, jedoch ist das oftmals nicht möglich.	
[0094]	Die Lösung ist, die Pointerstrukturen durch den Compiler so umzusortieren, daß die Pointeradressen möglichst lange vor deren Verwendung berechnet werden. Gleichzeitig sollte es möglichst wenig direkte Abhängigkeiten zwischen einem Pointer und den Daten auf die er zeigt geben.	60
	Erweiterungen der PAEs (gegenüber P196 5 075.9 und P196 54 846.2)	
[0095]	Durch P196 51 075.9 und P196 54 846.2 ist der Stand der Technik in Bezug auf die Konfigurationseigenschaften von Zellen (PAEs) definiert.	65
[0096]	Dabei soll auf zwei Eigenschaften eingegangen werden:	

1. Einer PAE (**0903**) ist gemäß P196 51 075.9 ein Satz von Konfigurationsregistern (**0904**) zugeordnet, der eine Konfiguration beinhaltet (**Fig. 9a**).
2. Eine Gruppe von PAEs (**0902**) kann gemäß P196 54 846.2 auf einen Speicher zum Speichern oder Lesen von Daten zugreifen (**Fig. 9b**)

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[**0097**] Aufgabe ist es,

- a) ein Verfahren zu schaffen, das das Umkonfigurieren von PAEs beschleunigt und zeitlich von der übergeordneten Ladeinheit entkoppelt, und
- 10 b) das Verfahren so auszulegen, daß gleichzeitig die Möglichkeit geschaffen wird über mehrere Konfigurationen zu sequenzen, und
- c) gleichzeitig mehrere Konfigurationen in einer PAE zu halten, von denen immer eine aktiviert ist und zwischen verschiedenen Konfigurationen schnell gewechselt werden kann.

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Entkopplung der Konfigurationsregister

[**0098**] Das Konfigurationsregister wird von der übergeordneten Ladeinheit (CT) entkoppelt (**Fig. 10**), indem ein Satz von mehreren Konfigurationsregistern (**1001**) verwendet wird. Immer genau eines der Konfigurationsregister bestimmt selektiv die Funktion der PAE. Die Auswahl des aktiven Registers wird über einen Multiplexer (**1002**) durchgeführt. In jedes der Konfigurationsregister kann die CT beliebig schreiben, sofern dieses nicht die aktuelle Konfiguration der PAE bestimmt, d. h. aktiv ist. Das Schreiben auf das aktive Register ist prinzipiell möglich, dazu stehen die in PACT10 beschriebenen Verfahren zur Verfügung.

[**0099**] Welches Konfigurationsregister von **1002** selektiert wird kann durch verschiedene Quellen bestimmt werden:

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1. Ein beliebiges Status-Signal oder eine Gruppe beliebiger Status-Signale, die über ein Bussystem (**0802**) an **1002** geführt werden (**Fig. 10a**). Die Status-Signale werden dabei von beliebigen PAEs generiert oder durch externe Anschlüsse des Bausteins zur Verfügung gestellt (vgl. **Fig. 8**)
2. Das Status-Signal der PAE, die von **1001/1002** konfiguriert wird, dient zur Selektion (**Fig. 10b**).
- 30 3. Ein von der übergeordneten CT generiertes Signal dient zur Selektion (**Fig. 10c**).

[**0100**] Dabei ist es möglich wahlweise die eingehenden Signale (**1003**) mittels eines Registers für einen bestimmten Zeitraum zu speichern und alternativ und wahlweise abzurufen.

[**0101**] Durch den Einsatz mehrere Register wird die CT zeitlich entkoppelt. Das bedeutet, die CT kann mehrere Konfigurationen "vorladen", ohne daß eine direkte zeitliche Abhängigkeit besteht.

[**0102**] Lediglich wenn das selektierte/aktivierte Register in **1001** noch nicht geladen ist, wird mit der Konfiguration der PAE so lange gewartet, bis die CT das Register geladen hat. Um festzustellen, ob ein Register eine gültige Information besitzt kann beispielsweise ein "Valid-Bit" (**1004**) pro Register eingeführt werden, das von der CT gesetzt wird. Ist **0906** bei einem selektierten Register nicht gesetzt, wird über ein Signal die CT zum schnellstmöglichen Konfigurieren des Registers aufgefordert.

[**0103**] Das in **Fig. 10** beschriebene Verfahren ist einfach zu einem Sequenzer erweiterbar (**Fig. 11**). Dazu wird ein Sequenzer mit Instruktionsdekoder (**1101**) zur Ansteuerung der Selektionssignale des Multiplexers (**1002**) verwendet. Der Sequenzer bestimmt dabei abhängig von der aktuell selektierten Konfiguration (**1102**) und einer zusätzlichen Statusinformation (**1103/1104**) die nächste zu selektierende Konfiguration. Die die Statusinformation kann

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- (a) der Status der Status-Signal der PAE, die von **1001/1002** konfiguriert wird sein (**Fig. 11a**)
- (b) ein beliebiges über **0802** zugeführtes Statussignal sein (**Fig. 11b**)
- (c) eine Kombination aus (a) und (b) sein.

[**0104**] **1001** kann auch als Speicher ausgestaltet sein, wobei anstatt **1002** ein Befehl von **1101** adressiert wird. Die Adressierung ist dabei abhängig vom Befehl selbst und von einem Statusregister. Insoweit entspricht der Aufbau einer "von Neumann" Maschine, mit dem Unterschied,

- (a) der universellen Einsetzbarkeit, also den Sequenzer nicht zu verwenden (vgl. **Fig. 10**)
- 55 (b) daß das Statussignal nicht von dem dem Sequenzer zugeordneten Rechenwerk (PAE) generiert werden muß, sondern von einem beliebigen anderen Rechenwerk stammen kann (vgl. **Fig. 11b**).

[**0105**] Wichtig ist, daß der Sequenzer Sprünge, insbesondere auch bedingte Sprünge, innerhalb von **1001** ausführen kann.

[**0106**] Ein weiteres zusätzliches oder alternatives Verfahren (**Fig. 12**) zum Aufbau von Sequenzern innerhalb von VPU's ist die Verwendung der internen Datenspeicher (**1201, 0901**) zum Speichern der Konfigurationsinformation für eine PAE oder eine Gruppe von PAEs. Dabei wird der Datenausgang eines Speichers auf einen Konfigurationseingang oder Dateneingang einer PAE oder mehrerer PAEs geschaltet (**1202**). Die Adresse (**1203**) für **1201** kann dabei von derselben PAE/denselben PAEs oder einer oder mehreren beliebigen anderen generiert werden.

[**0107**] Bei diesem Verfahren ist der Sequenzer nicht fest implementiert, sondern wird durch eine PAE oder eine Gruppe von PAEs nachgebildet. Die internen Speicher können Programme aus den externen Speichern nachladen (vgl. erfindungsgemäßes Speichersystem).

[**0108**] Zur Speicherung von lokalen Daten (z. B. für iterative Berechnungen und als Register für einen Sequenzer)

wird die PAE mit einem zusätzlichen Registersatz versehen, dessen einzelne Register entweder durch die Konfiguration bestimmt, zur ALU geführt oder von der ALU beschrieben werden; oder durch den Befehlssatz eines implementierten Sequenzers frei benutzt werden können (Register Mode). Ebenfalls kann eines der Register als Akkumulator (Akkumulator Mode) verwendet werden. Wird die PAE als vollwertige Maschine verwendet, ist es sinnvoll eines der Register als Adresszähler für externe Datenadressen zu verwenden.

[0109] Zur Verwaltung von Stacks und Akkumulatoren außerhalb der PAE (z. B. in den erfindungsgemäßen Speichern) wird das bereits beschriebene RDY/ACK REQ/ACK Synchronisationsmodell verwendet.

[0110] PAEs nach dem Stand der Technik (vgl. PACT02) sind zur Verarbeitung von bit-weisen Operationen schlecht geeignet, sofern die integrierte ALU bit-Operationen nicht besonders unterstützt, bzw. schmal (1-, 2-, 4-bit breit) ausgelegt ist. Die Verarbeitung von einzelnen Bits oder Signalen kann effizient gewährleistet, indem der ALU-Kern durch einen FPGA-Kern (LC) ersetzt wird, der konfigurierbar logische Operationen durchführt. Der LC ist dabei in seiner Funktion und internen Vernetzung frei konfigurierbar. Es können LC nach dem Stand der Technik eingesetzt werden. Für bestimmte Operationen ist es sinnvoll dem LC intern einen Speicher zuzuordnen. Die Interface-Baugruppen zwischen FC und dem Bussystem des Arrays werden nur geringfügig an den FC angepaßt, bleiben aber grundlegend bestehen. Zur flexibleren Gestaltung des Zeitverhaltens des FC ist es jedoch sinnvoll, die Register in den Interface-Baugruppen abschaltbar zu gestalten.

Figuren

[0111] In Fig. 4a sind einige grundlegenden Eigenschaften des erfindungsgemäßen Verfahrens dargestellt:

[0112] Die Module des Types A sind zu einer Gruppe zusammengefaßt und besitzen am Ende einen bedingten Sprung, entweder nach B1 oder B2. An dieser Position (0401) ist ein Umkonfigurationspunkt eingefügt, da es sinnvoll ist die Zweige des bedingten Sprunges als jeweils eine Gruppe zu betrachten (Fall 1). Würden dagegen beide Zweige von B (B1 und B2) zusätzlich zusammen mit A auf den Zielbaustein passen (Fall 2), wäre es sinnvoll nur einen Umkonfigurationspunkt bei 0402 einzufügen, da dadurch die Zahl der Konfigurationen verringert wird und sich die Verarbeitungsgeschwindigkeit erhöht. Beide Zweige (B1 und B2) springen bei 0402 nach C.

[0113] Die Konfiguration der Zellen auf dem Zielbaustein ist in Fig. 4b schematisch dargestellt. Dabei werden die Funktionen der einzelnen Graphenknoten auf die Zellen des Zielbausteins abgebildet. Jeweils eine Zeile stellt eine Konfiguration dar. Die gestrichelten Pfeile bei einem Zeilenwechsel zeigen eine Umkonfiguration an. S_n ist eine datenspeichernde Zelle, von beliebiger Ausgestaltung (Register, Speicher, etc.). Dabei ist S_nI ein Speicher, der Daten entgegennimmt und S_nO ein Speicher der Daten ausgibt. Der Speicher S_n ist für gleiche n jeweils derselbe, I und O kennzeichnen die Datentransferrichtung.

[0114] Beide Fälle des bedingten Sprunges (Fall 1, Fall 2) sind dargestellt.

[0115] Das Modell in Fig. 4 entspricht einem Datenflußmodell, jedoch mit der wesentlichen Erweiterung des Umkonfigurationspunkts und der damit erreichbaren Partitionierung des Graphen, wobei die zwischen den Partitionen übertragenen Daten zwischengespeichert werden.

[0116] Im Modell von Fig. 5a wird aus einer beliebigen Graphenmenge und -Konstellation (0501) selektiv ein Graph B_n aus einer Menge von Graphen B aufgerufen. Nach der Ausführung von B gelangen die Daten nach 0501 zurück.

[0117] Wird in 0501 ein ausreichend großer Sequencer (A) implementiert, ist mit dem Modell ein den typischen Prozessoren sehr ähnliches Prinzip implementierbar. Dabei gelangen

1. Daten in den Sequencer A, die dieser als Befehle dekodiert und entsprechend dem "von Neumann"-Prinzip darauf reagiert;
2. Daten in den Sequencer A, die als Daten betrachtet werden und an ein fest konfiguriertes Rechenwerk C zur Berechnung weitergeleitet werden.

[0118] Der Graph B stellt selektierbar ein besonderes Rechenwerk und/oder besondere Opcodes für bestimmte Funktionen zur Verfügung und wird alternativ zur Beschleunigung von C verwendet. Beispielsweise kann B1 ein optimierter Algorithmus zu Berechnung von Matrixmultiplikationen sein, während B2 einen FIR-Filter und B3 eine Mustererkennung darstellt. Entsprechend eines Opcodes der von 0501 dekodiert wird, wird der geeignete bzw. entsprechende Graph B aufgerufen.

[0119] Fig. 5b schematisiert die Abbildung auf die einzelnen Zellen, wobei in 0502 der pipelineartige Rechenwerks-Character symbolisiert wird.

[0120] Während in den Umkonfigurationspunkten von Fig. 4 vorzugsweise größere Speicher zum Zwischenspeichern der Daten eingefügt werden, ist eine einfache Synchronisation der Daten in den Umkonfigurationspunkten von Fig. 5 ausreichend, da der Datenstrom vorzugsweise als ganzer durch den Graphen B läuft und der Graph B nicht weiter partitioniert ist; dadurch ist das Zwischenspeichern der Daten überflüssig.

[0121] In Fig. 6a sind verschiedene Schleifen dargestellt. Schleifen können grundsätzlich auf drei Arten behandelt werden:

1. Hardware-Ansatz: Schleifen werden vollständig ausgewalzt auf die Zielhardware abgebildet (0601a/b). Wie bereits erläutert ist dies nur bei wenigen Schleifenarten möglich.
2. Datenfluß-Ansatz: Innerhalb des Datenflusses werden Schleifen über mehrere Zellen hinweg aufgebaut (0602a/b). Das Ende der Schleife wird auf den Schleifenanfang rückgekoppelt.
3. Sequenzer-Ansatz: Ein Sequenzer mit minimalem Befehlssatz führt die Schleife aus (0603a/b). Dabei sind die Zellen der Zielbausteine so ausgestaltet, daß sie den entsprechenden Sequenzer beeinhaltend (vgl. Fig. 11a/b).

[0122] Durch eine geeignete Zerlegung von Schleifen kann deren Ausführung ggf. optimiert werden:

1. Unter Verwendung von Optimierungsmethoden nach dem Stand der Technik läßt sich häufig der Schleifenrumpf, also der wiederholt auszuführende Teil, dadurch optimieren, daß bestimmte Operationen aus der Schleife entfernt werden und vor oder hinter die Schleife gestellt werden (**0604a/b**). Dadurch wird die Menge der zu sequenzierenden Befehle erheblich reduziert. Die entfernten Operationen werden nur einmal vor bzw. nach Ausführung der Schleife durchlaufen.
2. Eine weitere Optimierungsmöglichkeit ist das Teilen von Schleifen in mehrere kleinere oder kürzere Schleifen. Dabei findet die Teilung derart statt, daß mehrere parallele oder mehrere sequentielle (**0605a/b**) Schleifen entstehen.

[0123] Fig. 7 verdeutlicht die Implementierung einer Rekursion. Dabei werden dieselben Ressourcen (**0701**) in Form von Zellen für jede Rekursionsebene (**1–3**) verwendet. Die Ergebnisse einer jeden Rekursionsebene (**1–3**) werden beim Aufbau (**0711**) in einen nach dem Stack-Prinzip aufgebauten Speicher (**0702**) geschrieben. Gleichzeitig mit dem Abbau (**0712**) der Ebenen wird der Stack abgebaut.

[0124] In Fig. 14 wird das Virtual-Machine-Modell dargestellt. Aus einem externen Speicher werden Daten (**1401**) und zu den Daten gehörende Zustände (**1402**) in eine VPU (**1403**) gelesen.

[0125] **1401/1402** werden über eine von der VPU generierte Adresse **1404** selektiert. Innerhalb der VPU sind PAEs zu unterschiedlichen Gruppen zusammengefaßt (**1405, 1406, 1407**). Jede Gruppe besitzt einen datenverarbeitenden Teil (**1408**), der lokale implizite Zustände (**1409**) besitzt, die keinen Einfluß auf die umliegenden Gruppen besitzt. Daher werden dessen Zustände nicht außerhalb der Gruppe weitergeleitet. Er kann jedoch von den externen Zuständen abhängig sein. Ein weiterer Teil (**1410**) generiert Zustände, die Einfluß auf die umliegenden Gruppen haben.

[0126] Die Daten und Zustände der Ergebnisse werden in einen weiteren Speicher (**1411, 1412**) abgelegt. Gleichzeitig kann die Adresse von Operanden (**14004**) als Pointer gespeichert (**1413**) werden. Zur zeitliche Synchronisation kann **1404** über Register (**1414**) geführt werden.

[0127] In Fig. 14 ist zur Verdeutlichung ein einfaches Modell dargestellt. Die Vernetzung und Gruppierung kann wesentlich komplexer sein als in diesem Modell. Ebenfalls können Zustände und Daten auch an weitere Module als den Nachfolgenden übertragen werden. Es ist möglich, daß Daten an andere Module übertragen werden als die Zustände. Sowohl Daten als auch Zustände eines bestimmten Moduls können von mehreren unterschiedlichen Modulen empfangen werden. Innerhalb einer Gruppe kann **1408, 1409** und **1410** vorhanden sein. Abhängig vom Algorithmus können auch einzelne Teile fehlen (z. B. **1410** und **1409** vorhanden, **1410** jedoch nicht).

[0128] In Fig. 15 ist dargestellt wie aus einem Verarbeitungsgraphen Teilapplikationen extrahiert werden. Dabei wird der Graph so zerlegt, daß lange Graphen sinnvoll zerteilt werden und in Teilapplikationen (H, A, C, K) abgebildet werden. Nach Sprüngen werden neue Teilgraphen gebildet (C, K) wobei für jeden Sprung ein getrennter Teilgraph gebildet wird.

[0129] Jeder Teilgraph ist in dem ULIW-Modell von der CT (vgl. PACT10) getrennt ladbar. Wesentlich ist, daß Teilgraphen durch die Mechanismen in PACT10 verwaltet werden können. Dazu gehört insbesondere das intelligente Konfigurieren, Ausführen/Starten und Löschen der Teilapplikationen.

[0130] **1503** bewirkt das Laden oder Konfigurieren von Teilapplikation A, während Teilapplikation K ausgeführt wird. Dadurch ist

- a) Teilapplikation A zum Ausführungsende von Teilapplikation K bereits komplett in die PAEs konfiguriert, sofern die PAEs mehrere Konfigurationsregister aufweisen;
- b) Teilapplikation A zum Ausführungsende von Teilapplikation K bereits in die CT geladen, sofern die PAEs nur ein Konfigurationsregister aufweisen.

[0131] **1504** startet die Ausführung von Teilapplikation K.

[0132] D. h. zur Laufzeit werden die nächsten benötigten Programmteile während der Abarbeitung der aktuellen Programmteile unabhängig geladen. Dadurch ergibt sich ein wesentlich effizienterer Umgang mit dem Programmcode, als bei üblichen Cache-Mechanismen.

[0133] Bei Teilapplikationen A wird eine weitere Besonderheit dargestellt. Prinzipiell wäre es denkbar beide möglichen Zweige (C, K) des Vergleiches vorzukonfigurieren. Angenommen, die Zahl der zur Verfügung stehenden freien Konfigurationsregister reicht dazu nicht aus, wird der wahrscheinlichere der Zweige konfiguriert (**1506**). Das spart zudem Konfigurationszeit. Bei Ausführung des nicht konfigurierten Zweigs, wird (da die Konfiguration noch nicht in die Konfigurationsregister geladen ist) die Programmausführung unterbrochen, bis der Zweig konfiguriert ist.

[0134] Grundsätzlich ist es möglich auch nicht konfigurierte Teilapplikationen auszuführen (**1505**), diese müssen dann wie zuvor beschrieben vor der Ausführung geladen werden.

[0135] Ein FETCH-Befehl kann von einem Trigger mittels einer eigenen ID angestoßen werden. Damit können Teilapplikationen abhängig vom Zustand des Arrays vorgeladen werden.

[0136] Das ULIW-Modell unterscheidet sich im Wesentlichen vom VLIW-Modell, indem es

1. Das Routing der Daten mit beinhaltet
2. Größere Instruktionswörter bildet.

[0137] Ebenfalls kann das beschriebene Verfahren der Partitionierung von Compilern für heutige Standardprozessoren nach dem RISC/CISC-Prinzip ebenso eingesetzt werden. Wird dann eine Einheit (CT) nach PACT10 zur Steuerung des Befehls-Caches verwendet, kann dieser erheblich optimiert und beschleunigt werden.

[0138] Dazu werden "normale" Programme entsprechend in Teilapplikationen partitioniert. Gemäß PACT10 werden Verweise auf mögliche nachfolgende Teilapplikationen eingeführt (**1501, 1502**). Dadurch kann eine CT die Teilapplikationen bereits in den Cache vorladen bevor sie benötigt werden. Bei Sprüngen wird nur die angesprungen Teilapplikation ausgeführt, die andere (n) werden später durch neue Teilapplikationen überschrieben. Neben dem intelligenten Vorladen

hat das Verfahren den weiteren Vorteil, daß die Größe der Teilapplikationen beim Laden bereits bekannt ist. Dadurch können optimale Bursts beim Zugriff auf die Speicher von der CT ausgeführt werden, was den Speicherzugriff wiederum erheblich beschleunigt.

[0139] Fig. 16 zeigt den Aufbau eines Stack-Prozessors. Durch das PAE-Array (**1601**) werden Protokolle generiert um auf einen als LIFO konfigurierten Speicher (**1602**) zu schreiben oder zu lesen. Dabei wird ein RDY/ACK-Protokoll zum Schreiben und REQ/ACK-Protokoll zum Lesen verwendet. Die Vernetzung und Betriebsmodi werden von der CT (**1603**) konfiguriert. **1602** kann dabei seinen Inhalt auf den externen Speicher (**1604**) auslagern.

[0140] Eine Reihe der PAEs sollen in diesem Beispiel als Register-Prozessor arbeiten (Fig. 17). Jede PAE besteht aus einem Rechenwerk (**1701**) und einem Akkumulator (**1702**) auf den das Ergebnis von **1701** rückgekoppelt (**1703**) ist. Damit stellt in diesem Beispiel jede PAE einen Akkumulator-Prozessor dar. Eine PAE (**1705**) liest und schreibt die Daten in den als Standardspeicher konfigurierten RAM (**1704**). Eine weitere PAE (**1706**) generiert die Registeradressen.

[0141] Oftmals ist es sinnvoll eine getrennte PAE zum Lesen der Daten zu verwenden. Dann würde **1705** nur schreiben und die PAE **1707** lesen. Dabei wird eine weitere PAE (**1708**, gestrichelt unterlegt) zum Generieren der Leseadressen einzuführen.

[0142] Es ist nicht zwingend notwendig getrennte PAEs zum Generieren der Adressen zu verwendet. Oftmals sind die Register implizit und können dann als Konstanten konfiguriert werden von den datenverarbeitenden PAEs gesendet werden.

[0143] Die Verwendung von Akkumulator-Prozessoren für einen Register-Prozessor ist beispielhaft. Ebenso können zum Aufbau von Registerprozessoren PAEs ohne Akkumulator verwendet werden. Die in Fig. 17 gezeigte Architektur kann zur Ansteuerung von Registern als auch zum Ansteuern einer Load/Store-Einheit dienen.

[0144] Bei der Verwendung als Load/Store-Einheit ist es fast zwingend notwendig einen externen RAM (**1709**) nachzuschalten, sodaß **1704** nur einen temporären Ausschnitt aus **1709**, quasi als Cache, darstellt.

[0145] Auch bei der Verwendung von **1704** als Register-Bank ist es teilweise sinnvoll einen externen Speicher nachzuschalten. Dadurch können PUSH/POP Operationen nach dem Stand der Technik durchgeführt werden, die den Registerinhalt in einen Speicher schreiben oder aus diesem Lesen.

[0146] In Fig. 18 ist als Beispiel eine komplexe Maschine abgebildet bei der das PAE-Array (**1801**) einerseits einen Load/Store-Einheit (**1802**) mit nachgeschaltetem RAM (**1803**) ansteuert und gleichzeitig eine Register-Bank (**1804**) mit nachgeschaltetem RAM (**1805**) aufweist. **1802** und **1804** können jeweils von einer PAE oder einer beliebigen Gruppe von PAEs angesteuert werden. Die Einheit wird gemäß dem VPU-Prinzip von einer CT (**1806**) gesteuert.

[0147] Wichtig ist, daß zwischen der Load/Store-Einheit (**1802**) und der Register-Bank (**1804**) und deren Ansteuerung kein wesentlicher Unterschied besteht.

[0148] Die Fig. 19, 20, 21 zeigen einen erfindungsgemäßen internen Speicher, der zugleich eine Kommunikationseinheit mit externen Speichern und/oder Peripherie darstellt. Die einzelnen Figuren zeigen unterschiedliche Betriebsarten desselben Speichers. Die Betriebsarten, sowie einzelne Detail Einstellungen werden dabei konfiguriert.

[0149] Fig. 19a zeigt einen erfindungsgemäßen Speicher im "Register/Cache" Modus. Im erfindungsgemäßen Speicher (**1901**) sind Datenworte eines für gewöhnlich größeren und langsameren externen Speichers (**1902**) abgelegt.

[0150] Der Datenaustausch zwischen **1901**, **1902** und den über einen Bus (**1903**) angeschlossenen PAEs (nicht dargestellt) findet dabei wie folgt statt, wobei unter zwei Betriebsarten unterschieden wird:

A) Die von den PAEs von dem Hauptspeicher **1902** gelesenen oder gesendeten Daten werden in **1901** mittels eines Cache-Verfahrens gepuffert. Dabei kann jedes bekannte Cache-Verfahren zum Einsatz kommen.

B) Mittels einer Load/Store-Einheit werden die Daten bestimmter Adressen zwischen **1902** und **1901** übertragen. Dabei werden bestimmte Adressen, sowohl in **1902** als auch in **1901** vorgegeben, wobei für **1902** und **1901** gewöhnlicherweise unterschiedliche Adressen verwendet werden. Die einzelnen Adressen können dabei durch Konstante oder durch Berechnungen in PAEs erzeugt werden. In dieser Betriebsart arbeitet der Speicher **1901** als Registerbank.

[0151] Die Zuordnung der Adressen zwischen **1901** und **1902** kann dabei beliebig sein und hängt lediglich von den jeweiligen Algorithmen der beiden Betriebsarten ab.

[0152] In 19b ist die entsprechende Maschine als Blockdiagramm dargestellt. Dem Bus zwischen **1901** und **1902** ist eine Steuereinheit (**1904**) zugeordnet, die je nach Betriebsart als Load/Store-Einheit (nach dem Stand der Technik) oder als Cache-Kontroller (nach dem Stand der Technik) agiert. Dieser Einheit kann bei Bedarf eine Speicherverwaltungseinheit (MMU) (**1905**) mit Adressübersetzung und -überprüfung zugeordnet werden. Sowohl **1904** als auch **1905** kann von den PAEs angesteuert werden. So wird beispielsweise die MMU programmiert, die Load/Store Adressen gesetzt oder ein Cache-Flush ausgelöst.

[0153] Fig. 20 zeigt den Einsatz des Speichers (**2001**) im FIFO-Modus, in welchem nach dem bekannten FIFO-Prinzip Datenströme entkoppelt werden. Der typische Einsatz ist in einem Schreib-(**2001a**) oder Leseinterface (**2001b**). Dabei werden Daten zwischen den PAEs, die an dem internen Bussystem (**2002**) angeschlossen sind und dem Peripheriebus (**2003**) zeitlich entkoppelt.

[0154] Zur Steuerung des FIFOs ist eine Einheit (**2004**) vorgesehen, die den Schreib- und Lesezeiger des FIFOs abhängig von den Busoperationen von **2003** und **2002** steuert.

[0155] In Fig. 21 ist das Arbeitsprinzip der erfindungsgemäßen Speicher im Stack-Modus dargestellt. Ein Stack ist (nach dem Stand der Technik) ein Stapelspeicher, dessen oberstes/unterstes Element das gerade Aktive ist. Daten werden immer oben/unten angefügt, ebenso werden die Daten oben/unten entfernt. D. h. das zuletzt geschriebene Datum ist auch das, welches zuerst gelesen wird (Last In First Out). Ob ein Stack nach oben oder unten wächst, ist unbedeutend und implementierungsabhängig. Im folgenden Ausführungsbeispiel werden Stacks betrachtet, die nach oben wachsen.

[0156] Dabei sind die aktuellsten Daten im internen Speicher **2101** gehalten, der aktuellste Eintrag (**2107**) befindet sich ganz oben in **2101**. Alte Einträge sind auf den externen Speicher **2102** ausgelagert. Wächst der Stack weiter, reicht der

Platz im internen Speicher **2101** nicht mehr aus. Bei Erreichen einer bestimmten Datenmenge, die durch eine (frei wählbare) Adresse in **2101** oder einen (frei wählbaren) Wert in einem Eintragszähler repräsentiert sein kann, wird ein Teil von **2101** als Block an das aktuellere Ende (**2103**) des Stacks in **2102** geschrieben. Dieser Teil sind die ältesten und somit am wenigsten aktuellen Daten (**2104**). Danach werden die verbleibenden Daten in **2101** so verschoben, daß die nach **2102** kopierten Daten in **2101** mit den verbleibenden Daten (**2105**) überschrieben werden und somit genügend freier Speicher (**2106**) für neue Stackeinträge entsteht.

[0157] Nimmt der Stack ab, werden ab einem gewissen (frei wählbaren) Punkt die Daten in **2101** so verschoben, daß hinter den ältesten und unaktuellsten Daten freier Speicher entsteht. In den freigewordenen Speicher wird ein Speicherblock aus **2102** kopiert, der dann in **2102** gelöscht wird.

[0158] Mit anderen Worten repräsentieren **2101** und **2102** einen einzigen Stack, wobei die gerade aktuellen Einträge in **2101** liegen und die älteren und weniger aktuellen in **2102** ausgelagert sind. Quasi stellt das Verfahren einen Cache für Stacks dar. Da die Datenblöcke vorzugsweise per Blockoperationen übertragen werden, kann der Datentransfer zwischen **2101** und **2102** in den schnellen Burst-Betriebsarten moderner Speicher (SDRAM, RAMBUS, etc.) ausgeführt werden.

[0159] Es soll nochmals erwähnt werden, daß im Ausführungsbeispiel in **Fig. 21** der Stack nach oben wächst. Sollte der Stack nach unten wachsen (eine häufig verwendete Methode), sind die Positionen oben/unten und die Richtungen in die die Daten innerhalb eines Speichers bewegt werden genau vertauscht.

[0160] Sinnvollerweise wird der interne Stack **2101** als eine Art Ringspeicher ausgestaltet. Die Daten an einem Ende des Ringes werden zwischen PAEs und **2101** übertragen und am anderen Ende des Ringes zwischen **2101** und **2102**. Dadurch entsteht der Vorteil, daß einfach Daten zwischen **2101** und **2102** verschoben werden können, ohne Einfluß auf die internen Adressen in **2101** zu haben. Lediglich die Positionszeiger der unteren und oberen Daten und der Füllstandszeiger müssen jeweils angepaßt werden. Die Datenübertragung zwischen **2101** und **2102** kann durch die bekannten Ringspeicher-Flags "beinahe voll (almost full)/ voll (full)" und "beinahe leer (almost empty)/leer (empty)" ausgelöst werden.

[0161] Die notwendige Hardware ist als Blockschaltbild in **Fig. 21b** dargestellt. Dem internen Stack **2101** ist eine Einheit (**2110**) zur Verwaltung der Zeiger und Zähler zugeordnet. In den Bus (**2114**) zwischen **2101** und **2102** ist eine Einheit (**2111**) zur Steuerung der Datentransfers eingeschleift. Dieser Einheit kann eine MMU (**2112**) nach dem Stand der Technik mit den entsprechenden Prüfsystemen und Adressübersetzungen zugeordnet werden.

[0162] Die Verbindung zwischen den PAEs und **2101** wird über das Bussystem **2113** realisiert.

[0163] In **Fig. 22** ist ein Beispiel für das Umsortieren von Graphen gezeigt. Die linke Spalte (**22. a**) zeigt eine unoptimierte Anordnung von Befehlen. Dabei werden die Pointer A (**2207a**) und B (**2211a**) geladen. Jeweils bereits einen Takt später werden die Werte der Pointer benötigt (**2208a**, **2212a**). Diese Abhängigkeit ist zu kurz um effizient ausgeführt zu werden, da zum Laden aus dem Speicher eine bestimmte Zeit (**2220a**, **2221a**) benötigt wird. Durch umsordieren der Befehle (**22. b**) werden die Zeiträume maximal vergrößert (**2220b**, **2221b**). Obwohl in **2210** und in **2208** der Wert des Pointers von A benötigt wird, wird **2208** nach **2210** einsortiert, da dadurch mehr Zeit zur Berechnung von B gewonnen wird. Es ist möglich Berechnungen die von den Pointern unabhängig sind (**2203**, **2204**, **2206**) beispielsweise zwischen **2211** und **2212** einzufügen um mehr Zeit für die Speicherzugriffe zu erhalten. Ein Compiler oder Assembler kann hier anhand von Systemparametern, die die Zugriffszeiten repräsentieren, die entsprechende Optimierung vornehmen.

[0164] **Fig. 23** zeigt einen Sonderfall der **Fig. 4-7**. Häufig besteht ein Algorithmus, auch innerhalb von Schleifen, aus Datenflußteilen und sequentiellen Teilen. Derartige Strukturen können gemäß dem beschriebenen Verfahren unter Einsatz des in PACT07 beschriebenen Bussystems effizient aufgebaut werden. Hierzu wird das RDY/ACK-Protokoll des Bussystems zunächst um das erfindungsgemäße REQ/ACK-Protokoll erweitert. Dadurch können gezielt Registerinhalte einzelner PAEs von einer oder mehreren anderen PAEs oder von der CT abgefragt werden. Eine Schleife (**2305**) wird nun in mindestens zwei Graphen zerlegt, einen ersten (**2301**), der den Datenflußanteil repräsentiert und einen zweiten (**2302**), der den sequentiellen Anteil abbildet.

[0165] Ein bedingter Sprung wählt zwischen den beiden Graphen. Das besondere ist nun, daß **2302** den internen Zustand von **2301** kennen zur Ausführung benötigt und umgekehrt **2301** den Zustand von **2302** kennen muß.

[0166] Dies wird realisiert, indem der Zustand genau einmal, nämlich in den Registern der PAEs des performanteren Datenflußgraphen (**2301**) gespeichert wird.

[0167] Wird in **2302** gesprungen, liest der Sequenzer bei Bedarf die Zustände der jeweiligen Register mittels des Bussystems aus PACT07 aus (**2303**). Der Sequenzer führt seine Operationen aus und schreibt alle geänderten Zustände in die Register (wiederum über das Bussystem nach PACT07) zurück (**2304**). Abschließend soll angemerkt werden, daß es sich bei den besprochenen Graphen nicht unbedingt um enge Schleifen (**2305**) handeln muß. Das Verfahren ist generell auf jeden Teilalgorithmus verwendbar, der innerhalb eines Programmablaufes mehrfach ausgeführt wird (reentrant) und wahlweise entweder sequentiell oder parallel (datenflußartig) abgearbeitet wird, wobei die Zustände zwischen dem sequentiellen und dem parallelen Teil transferiert werden müssen.

[0168] Die Waverekonfigurierung bietet erhebliche Vorteile bei der Geschwindigkeit der Umkonfiguration, insbesondere bei einfachen sequentiellen Operationen.

[0169] Eine grundlegende Besonderheit dieser Verarbeitungsmethode ist, daß der Sequenzer auch als externen Mikroprozessor ausgestaltet sein kann. Das bedeutet, daß ein Prozessor über die Datenkanäle mit dem Array verbunden ist und lokale, temporäre Daten über Bussysteme mit dem Array austauscht. Sämtliche sequentielle Teile eines Algorithmus die nicht in das Array aus PAEs abgebildet werden können werden auf dem Prozessor abgewickelt.

[0170] Es muß zwischen drei Bussystemen unterschieden werden:

1. Datenbus, der den Austausch der verarbeiteten Daten zwischen VPU und Prozessor regelt.
2. Registerbus, der den Zugriff auf die Register der VPU ermöglicht und den somit den Datenaustausch (**2302**, **2304**) zwischen **2302** und **2301** gewährleistet.
3. Konfigurationsdatenbus, der das Array der VPU konfiguriert.

[0171] In **Fig. 24** sind die Auswirkungen zeitlich dargestellt.

[0172] Einfach schraffierte Flächen stellen datenverarbeitende PAEs dar, wobei **2401** PAEs nach der Umkonfiguration und **2403** PAEs vor der Umkonfiguration zeigen. Doppelt schraffierte Flächen (**2402**) zeigen PAEs die gerade umkonfiguriert werden oder auf die Umkonfiguration warten.

[0173] Fig. 24a zeigt den Einfluß der Wave-Rekonfigurierung auf einen einfachen sequentiellen Algorithmus. Hier ist es möglich exakt die PAEs umzukonfigurieren, denen eine neue Aufgabe zugeteilt wird. Da in jedem Takt eine PAE eine neue Aufgabe erhält kann dies effizient, nämlich zeitgleich durchgeführt werden.

[0174] Beispielsweise dargestellt ist eine Reihe von PAEs aus der Matrix aller PAEs einer VPU. Angegeben sind die Zustände in den Takten nach Takt *t* mit jeweils einem Takt Verzögerung.

[0175] In Fig. 24b ist die zeitliche Auswirkung der Umkonfiguration von großen Teilen dargestellt. Beispielsweise dargestellt ist eine Menge von PAEs einer VPU. Angegeben sind die Zustände in den Takten nach Takt *t* mit einer unterschiedlichen Verzögerung von jeweils mehreren Takten.

[0176] Während zunächst nur ein kleiner Teil der PAEs umkonfiguriert wird oder auf die Umkonfiguration wartet, wird diese Fläche mit zunehmender Zeit größer, bis alle PAEs umkonfiguriert sind. Das größer werden der Fläche bedeutet, daß, bedingt durch die zeitliche Verzögerung der Umkonfiguration immer mehr PAEs auf die Umkonfiguration warten (**2402**). Dadurch geht Rechenleistung verloren.

[0177] Es wird daher vorgeschlagen ein breiteres Bussystem zwischen der CT (insbesondere des Speichers der CT) und den PAEs einzusetzen, das genügend Leitungen zur Verfügung stellt, um innerhalb eines Taktes mehrere PAEs zugleich umzukonfigurieren.

[0178] Fig. 25 verdeutlicht die Skalierbarkeit der VPU-Technologie. Die Skalierbarkeit geht im Wesentlichen aus dem Ausrollen eines Graphens hervor, ohne daß eine zeitliche Abfolge einzelne Teilapplikationen trennt. Als Beispiel ist der Algorithmus aus Fig. 4 gewählt. In Fig. 25a werden die einzelnen Teilgraphen zeitlich nacheinander auf die VPU übertragen, wobei entweder B1 oder B2 geladen wird. In Fig. 25b werden alle Teilgraphen auf eine Menge von VPUs übertragen und mit Bussystemen untereinander verbunden. Dadurch können große Datenmengen ohne den negativen Einfluß des Umkonfigurierens leistungsfähig abgearbeitet werden.

[0179] Fig. 26 zeigt eine Schaltung zur Beschleunigung der (Um-)konfigurationszeit von PAEs. Gleichzeitig kann die Schaltung zur Verarbeitung von sequentiellen Algorithmen verwendet werden. Das Array von PAEs (**2605**) ist in mehrere Teile (**2603**) partitioniert. Jedem Teil ist eine eigenständige Einheit zur (Um-)konfiguration (**2602**) zugeordnet. Diesen Einheiten übergeordnet ist eine CT (**2601**) nach dem Stand der Technik (vgl. PACT10), die wiederum an eine weitere CT oder an einen Speicher angeschlossen ist (**2604**). Die CT lädt die Algorithmen in die Konfigurationseinheiten (**2602**). Die **2602** laden selbständig die Konfigurationsdaten in die ihnen zugeordneten PAEs.

[0180] In Fig. 27 ist ein Aufbau einer Konfigurationseinheit dargestellt. Kern der Einheit ist ein Sequenzer (**2701**) der eine Reihe von Befehlen beherrscht.

[0181] Die wesentlichen Befehle sind:

wait <trg#> Warten auf das Eintreffen eines bestimmten Triggers aus dem Array, der angibt, welche nächste Konfiguration geladen werden soll.

lookup <trg#> Gibt die Adresse des durch einen eintreffenden Trigger aufgerufenen Unterprogramms zurück.

jmp <adr> Sprung nach Adresse

call <adr> Sprung nach Adresse. Rücksprungsadresse wird auf dem Stack gespeichert

jmp <cond> <adr> Bedingter Sprung nach Adresse

call <cond> <adr> Bedingter Sprung nach Adresse. Rücksprungsadresse wird auf dem Stack gespeichert

ret Rücksprung auf die auf dem Stack gespeicherte Rücksprungsadresse

mov <target> <source> Überträgt ein Datenwort von Quelle (source) an ein Ziel (target). Quelle und Ziel können jeweils in einem Speicher oder eine Peripherieadresse sein.

[0182] Im wesentlichen sind die Befehle aus PACT10, d. h. der Beschreibung der CT bekannt. Wesentlicher Unterschied in der Implementierung der **2602** ist, daß nur sehr einfache Befehle zur Datenverwaltung verwendet werden und kein vollständiger Mikrokontroller verwendet wird.

[0183] Eine bedeutende Erweiterung des Befehlssatzes ist der "pabm"-Befehl zum Konfigurieren der PAEs. Es stehen zwei Befehle (pabmr, pabmm) zur Verfügung, die folgendermassen aufgebaut sind:

a)

5	pabmr	regno	count
	pa_adr ₀		pa_dta ₀
	pa_adr ₁		pa_dta ₁
10	...		...
	pa_adr _{count}		pa_dta _{count}

15	pabmm	000	count
	offset		
20	pa_adr ₀		pa_dta ₀
	pa_adr ₁		pa_dta ₁
	...		...
25	pa_adr _{count}		pa_dta _{count}

b)

30	pabmr	regno	count
	memref		

35	pabmm	000	count
	offset		
40	memref		

[0184] Die Befehle kopieren einen zugeordneten Block von PAE-Adressen und PAE-Daten vom Speicher zu dem PAE-Array. Durch <count> ist angegeben, wie groß der zu kopierende Datenblock ist. Der Datenblock ist entweder direkt an den Opcode angehängt (a) oder durch Angabe der erste Speicheradresse <memref> referenziert (b).

[0185] Jede pa_adr_n-pa_dta_n-Zeile stellt eine Konfiguration für eine PAE dar. Dabei gibt pa_adr_n, die Adresse und pa_dta_n das Konfigurationswort der PAE an.

[0186] Aus PACT10 ist das RDY/ACK-REJ Protokoll bekannt. Werden die Konfigurationsdaten von einer PAE angenommen, quittiert die PAE die gesendeten Daten mit einem ACK. Kann dagegen eine PAE die Konfigurationsdaten nicht annehmen, da sie sich nicht in einem umkonfigurierbaren Zustand befindet, sendet sie ein REJ zurück. Dadurch schlägt die Konfiguration des Teilalgorithmus fehl.

[0187] Die Stelle mit REJ zurückgewiesenen pa_adr_n-pa_dta_n-Zeile wird gespeichert. Die Befehle werden zu einem späteren Zeitpunkt erneut aufgerufen (vgl. PACT10, FILMO). Sofern der Befehl komplett abgearbeitet wurde, d. h. es trat kein REJ auf, führt der Befehl keine weitere Konfiguration durch sondern terminiert sofort. Trat ein REJ auf, springt der Befehl direkt an die Stelle der zurückgewiesenen pa_adr_n-pa_dta_n-Zeile. Je nach Befehl wird die Stelle unterschiedlich gespeichert:

pabmr: Die Adresse wird in dem mit <regno> genannten Register gespeichert.

pabmm: Die Adresse wird direkt im Befehl an der Speicherstelle <offset> gespeichert.

[0188] Die Befehle sind durch DMA-Strukturen als Speicher/IO-Transfers nach dem Stand der Technik implementierbar. Die DMAs werden durch eine Logik zum Überwachen der eingehenden ACK/REJ erweitert. Die Startadresse wird durch <regno>, bzw. <offset> bestimmt. Die letzte Adresse des Datenblocks wird durch die Adresse des Befehls plus dessen Opcode-Länge minus eins plus die Anzahl der pa_adr_n-pa_dta_n-Zeilen berechnet.

[0189] Es ist sinnvoll auch die in PACT10 beschriebene Schaltung durch die genannten Befehle zu erweitern.

[0190] Fig. 27 zeigt den Aufbau einer Einheit 2602. Die Einheit besteht aus einem Registersatz 2701 dem eine einfache ALU für Stackoperationen zugeordnet ist (2702). Die Struktur enthält Adressregister und Stackpointer. Optional kann eine vollwertige ALU eingesetzt werden. Ein Bussystem (2703) mit minimaler Breite verbindet Register und ALU. Die Breite ist dabei so bemessen, daß einfache Kontrollflußbefehle bzw. einfache ALU-Operationen sinnvoll dargestellt werden können. Zusätzlich werden die vorab beschriebenen PABM-Befehle, sowie die Befehle nach PACT10 unterstützt.

Register und ALU werden von einem Sequenzer **2706** gesteuert, der durch Ausführung von Befehlen einen vollständigen Microcontroller darstellt. An **2703** ist eine Einheit **2704** angeschlossen, die Trigger von den zugeordneten PAEs entgegennimmt und quittiert und gegebenenfalls ihrerseits Trigger an die PAEs sendet.

[0191] Eingehende Trigger lösen dabei in dem Sequenzer **2706** einen Interrupt aus oder werden durch den WAIT-Befehl abgefragt. Optional an **2703** angeschlossen ist ein Interface (**2705**) zu einem Datenbus der zugeordneten PAEs um Daten an die PAEs senden zu können. Beispielsweise werden die Assemblercodes eines in den PAEs implementierten Sequenzers über **2705** gesendet. Das Interface enthält sofern erforderlich einen Konverter zur Anpassung der unterschiedlichen Busbreiten. Die Einheiten **2701** bis **2706** sind über einen Multiplexer/Demultiplexer (**2707**) an ein um ein Vielfaches breiteres Bussystem (**2708**) angeschlossen, das zum Speicher (**2709**) führt. **2707** wird von den niederwertigen Adressen des Adress-/Stackregisters angesteuert, die höherwertigen Adressen führen direkt zum RAM (**2711**). Das Bussystem **2708** führt zu einem Interface (**2709**), das durch die PA-Befehle gesteuert wird und zum Konfigurationsbus der PAEs führt. **2708** ist bewußt breit ausgelegt um möglichst viele Konfigurationsbits pro Takteinheit über **2709** an die PAEs senden zu können. Ein weiteres Interface (**2710**) verbindet den Bus mit einer übergeordneten CT, die Konfigurations- und Steuerdaten mit **2602** austauscht. Die Interface **2710** und **2709** bereits mehrfach in PACT10, PACT?? beschrieben worden.

[0192] Wesentlich ist, daß **2706** einen reduzierten und auf die Aufgabe optimierten Minimalsbefehlssatz beherrscht, der vor allem auf die PA-Kommandos, Sprünge, Interrupts und Lookup-Befehle optimiert ist. Weiterhin ist das optimierte breite Bussystem **2708**, das über **2707** auf ein schmales Bussystem übertragen wird von besonderer Bedeutung für die Umkonfigurationsgeschwindigkeit der Einheit.

[0193] Fig. 27a ist eine spezielle Ausgestaltung von Fig. 27. Das Interface **2705** dient der Übertragung von Assemblercodes an im PAE-Array konfigurierte Sequenzer. Die Verarbeitungsleistung der Sequenzer hängt wesentlich von der Geschwindigkeit des Interfaces **2705** und dessen Speicherzugriffes ab. In Fig. 27a ist **2705** durch eine DMA-Funktion mit direktem Speicherzugriff (**2720_n**) ersetzt. **2720_n** führt eigene Speicherzugriffe aus und besitzt ein eigenes Bussystem (**2722_n**) mit entsprechender Anpassung der Busbreite (**2721_n**); dabei kann der Bus zum Laden von breiten Befehlssequenzen (ULIW) verhältnismäßig breit ausfallen, sodaß als Grenzfall **2721_n** komplett entfällt. Zur weiteren Steigerung der Geschwindigkeit ist der Speicher **2711** physikalisch in **2711a** und **2711b_n** getrennt worden. Der Adressraum über **2711a** und **2711b_n** verbleibt linear, jedoch kann von **2701**, **2702**, **2706** auf beide Speicherblöcke unabhängig gleichzeitig zugegriffen werden; **2720_n** kann nur auf **2711b_n** zugreifen. **2720_n**, **2721_n**, und **2711b_n** kann mehrfach (_n) implementiert sein, damit mehrere Sequenzer gleichzeitig verwaltet werden können. Dazu kann **2711b_n** nochmal in mehrere physikalisch unabhängige Speicherbereiche unterteilt werden. In Fig. 38 ist sind Implementierungsbeispiele für **2720_n** beschrieben.

[0194] In Fig. 28 wird der Aufbau von komplexen Programmen verdeutlicht. Die Basismodule der Programme sind die Komplex-Konfigurationen (**2801**) die die Konfigurationen einer oder mehrere PAEs und der dazugehörigen Bus- und Triggerkonfigurationen beinhalten. Die **2801** werden durch einen Opcode (**2802**) repräsentiert, der zusätzliche Parameter (**2803**) besitzen kann. Diese Parameter können einerseits konstante Datenwerte, variable Startwerte oder auch spezielle Konfigurationen beinhalten. Es existieren je nach Funktion ein, mehrere oder auch kein Parameter.

[0195] Mehrere Opcodes greifen auf einen gemeinsamen Satz von Komplex-Konfigurationen zurück und bilden damit eine Opcode-Gruppe (**2805**). Die unterschiedlichen Opcodes einer Gruppe unterscheiden sich durch besondere Ausgestaltungen der Komplex-Konfigurationen. Dazu werden Differenzierungen (**2807**) verwendet, die entweder zusätzliche Konfigurationsworte enthalten, oder in **2801** vorkommende Konfigurationsworte überschreiben.

[0196] Eine Komplex-Konfiguration wird, sofern keine Differenzierung erforderlich ist, direkt von einem Opcode aufgerufen (**2806**). Ein Programm (**2804**) setzt sich aus einer Abfolge von Opcodes mit den jeweiligen Parametern zusammen.

[0197] Eine komplexe Funktion kann einmal in das Array geladen werden und kann danach durch unterschiedliche Parameter oder Differenzierungen neu umkonfiguriert werden. Dabei werden nur die sich ändernden Teile der Konfiguration umkonfiguriert. Unterschiedliche Opcode-Gruppen greifen auf unterschiedliche Komplex-Konfigurationen zurück. (**2805a**, . . . , **2805n**).

[0198] Die unterschiedlichen Ebenen (Komplex-Konfiguration, Differenzierung, Opcode, Programm) werden in verschiedenen Ebenen von CTs abgearbeitet (vgl. CT Hierarchien in PACT10). Die unterschiedlichen Ebenen sind in **2810** dargestellt, wobei 1 die niederste und N die höchste Ebene darstellt. CTs können zu beliebig tiefen Hierarchien aufgebaut werden (vgl. PACT10).

[0199] Es wird in **2801** unter zwei Arten von Codes unterschieden:

1. Konfigurationsworte, die einen Algorithmus auf das Array aus PAEs abbilden. Der Algorithmus kann dabei auch als Sequenzer ausgestaltet sein. Die Konfiguration erfolgt über die Schnittstelle **2709**. Konfigurationsworte werden durch die Hardware definiert.
2. Algorithmusspezifische Codes, die von der möglichen Ausgestaltung eines Sequenzer oder Algorithmus abhängig sind. Diese Codes werden vom Programmierer oder Compiler definiert und dienen zur Ansteuerung eines Algorithmus. Ist beispielsweise ein Z80 als Sequenzer in die PAEs konfiguriert, stellen diese Codes den Opcode des Z80 Mikroprozessors dar. Algorithmusspezifische Codes werden über **2705** an das Array aus PAEs gesendet.

[0200] In Fig. 29 ist ein möglicher Grundaufbau einer PAE dargestellt. **2901** bzw. **2902** stellen die Eingangs- bzw. Ausgangsregister der Daten dar. Den Registern zugeordnet ist die komplette Vernetzungslogik zum Aufschalten auf den/die Datenbusse (**2920**, **2921**) des Arrays (vgl. PACT02). Die Triggerleitungen gem. PACT08 werden durch **2903** vom Triggerbus (**2922**) abgegriffen und mit **2904** auf den Triggerbus (**2923**) aufgeschaltet. Zwischen **2901** und **2902** ist eine ALU (**2905**) beliebiger Ausgestaltung geschaltet. Den Datenbussen (**2906**, **2907**) und der ALU zugeordnet ist ein Registersatz (**2915**), in welchem lokale Daten gespeichert werden. Die RDY/ACK-Synchronisationssignale der Datenbusse und Triggerbusse werden zu einer Statemachine (oder einem Sequenzer) (**2910**) geführt (**2908**), bzw. von der Einheit generiert

(2909).

[0201] Über eine Interfaceeinheit (2911) greift die CT mittels eines Bussystemes (2912) selektiv auf eine Mehrzahl von Konfigurationsregistern (2913) zu. 2910 wählt über einen Multiplexer (2914) jeweils eine bestimmte Konfiguration aus, oder sequenziert über eine Mehrzahl von Konfigurationswörtern, die dann Befehle für den Sequenzer darstellen.

5 [0202] Da die VPU-Technologie hauptsächlich gepipelinet arbeitet ist es von Vorteil entweder die Gruppe 2901 und 2903 oder die Gruppe 2902 und 2904 oder beide Gruppen zusätzlich mit FIFOs zu versehen. Dadurch kann verhindert werden, daß eine Pipeline durch einfache Verzögerungen (z. B. in der Synchronisation) stockt.

[0203] 2920 ist ein optionaler Buszugang, über den ein der Speicher einer CT (siehe Fig. 27, 2720) oder ein gewöhnlicher interner Speicher an Stelle der Konfigurationsregister an den Sequenzer 2910 geschaltet werden kann. Damit sind große sequentielle Programme in einer PAE ausführbar. Der Multiplexer 2914 wird dazu so geschaltet, daß er nur den internen Speicher verbindet.

[0204] Die Adressen werden

- a) für den CT-Speicher durch die Schaltung in Figur. 38 generiert.
- 15 b) für den internen Speicher direkt von 2910 generiert.

[0205] Fig. 30 zeigt eine mögliche Erweiterung der PAE um der CT oder einem anderen zuegeschalteten Mikroprozessor einen Zugriff auf die Datenregister zu ermöglichen. Der Adressraum und die Interface der Buseinheit (vormals 2911, 3003) werden um die zusätzlichen Datenbusse (3001) erweitert. Den jeweiligen Registern wird ein Multiplexer (3002) vorgeschaltet mittels dem 3003 über den Bus 3001 Daten in das Register schreiben kann. Die Ausgänge der Register werden über 3001 zurück an 3003 geführt. 3003 überträgt die Daten zur CT 2912.

[0206] Alternativ (3003a) zur Übertragung der Daten zu CT ist es möglich die Daten durch ein zusätzliches Interface (3004) auf einen von der CT unabhängigen Bus (3005) zu übertragen.

25 [0207] Fig. 31 zeigt die Kopplung des Arrays von PAEs (3101) mit einem übergeordneten Mikrokontroller. 3101 beinhaltet sind sämtliche IO-Kanäle gemäß den erfindungsgemäßen Speichern. Die Architektur arbeitet gemäß Fig. 23. 2912 in Fig. 31a stellt den Bus für die Konfigurationsdaten und Registerdaten gem. Fig. 30 zur Verfügung. Der Datenbus wird separat durch 3104 dargestellt. 3102 stellt die CT dar, die in Fig. 31a auch den Mikroprozessor darstellt.

[0208] Für sämtliche Bussysteme bestehen unabhängig voneinander folgende Anschlußmodelle an einen Prozessor, die je nach Programmiermodell und unter Abwägung von Preis und Performance gewählt werden:

1. Register-Modell

[0209] Beim Register-Modell wird der jeweilige Bus über ein Register angesprochen, das direkt in den Registersatz des Prozessors integriert ist und vom Assembler als Register oder Gruppe von Registern angesprochen wird. Dieses Modell ist am effizientesten wenn einige wenige Register für den Datenaustausch ausreichen.

2. IO-Modell

40 [0210] Der jeweilige Bus liegt im IO-Bereich des Prozessors. Dies ist meistens die einfachste und kostengünstigste Variante.

3. Shared-Memory-Modell

4. Shared-Memory-DMA-Modell

45 [0211] Prozessor und Bus teilen sich wie im vorigen Modell denselben Speicher. Zur weiteren Geschwindigkeitssteigerung existiert eine schnelle DMA (vgl. Fig. 38) die den Datenaustausch zwischen Bus und Speicher übernimmt.

[0212] Zur Steigerung der Übertragungszeit sollten die jeweiligen Speicher physikalisch vom übrigen Speicher trennbar sein (mehrere Speicherbanke), damit Prozessor und VPU unabhängig auf ihre Speicher zugreifen können.

50 [0213] In Fig. 31b übernimmt eine CT (3102) die Konfiguration des Arrays, während ein dedizierter Prozessor (3103) über 3006 das Programmiermodell nach Fig. 23 gewährleistet, indem er über 3006 Registerdaten mit dem Array austauscht und über 3104 die gewöhnlichen Daten austauscht.

[0214] Die Fig. 31c/d entsprechen den Fig. 31a/b, jedoch wurde für den Datenaustausch ein Shared-Memory (3105) zwischen dem jeweiligen Prozessor und 3101 gewählt.

55 [0215] Fig. 32 zeigt eine Schaltung die es den erfindungsgemäßen Speicherelementen ermöglicht gemeinsam auf einen Speicher oder eine Gruppe von Speichern zuzugreifen, wobei jeder einzelne Speicher der Gruppe einzeln und eindeutig adressierbar ist. Dazu werden die einzelnen Speicherelemente (3201) auf ein Bussystem geschaltet, bei dem jedes 3201 einen eigenen Bus besitzt. Der Bus kann bidirektional ausgestaltet sein oder durch zwei unidirektionale Busse realisiert werden. Pro Speicher existiert ein Adress/Datenmultiplexer, der einen Bus zum Speicher durchschaltet. Dazu werden 60 anliegenden Adressen jedes Busses dekodiert (3207) und danach jeweils ein Bus pro Zeiteinheit durch einen Arbitrer (3208) ausgewählt (3204). Die entsprechenden Daten und Adressen werden auf den jeweiligen Speicherbus (3205a) übertragen, wobei eine Zustandsmaschine (3206) die notwendigen Protokolle generiert. Treffen bei einer Leseanforderung die Daten vom Speicher ein, wird durch die jeweilige Zustandsmaschine die Adresse des Speichers auf den Bus geschaltet, der die Daten anfragte. Die Adressen aller eingehenden Busse werden pro Bus des Bussystems 3202 durch eine Multiplexereinheit ausgewertet und auf den entsprechenden Bus übertragen. Die Auswertung erfolgt entsprechend der 65 Auswertung der Ausgangsdaten, d. h. ein Dekoder (3209) je Eingangsbuss (3205b) leitet ein Signal auf einen Arbitrer (3210), der den Daten-Multiplexer ansteuert. Damit werden pro Zeiteinheit unterschiedliche Eingangsbusse auf das Bussystem 3202 geleitet.

[0216] In Fig. 33 wird zur flexibleren und einfacheren Auswertung der Trigger- und RDY/ACK-Signale die starre State-Machine / der starre Sequenzer **2910** durch einen frei programmierbaren (**3301**) ersetzt. Die vollständige Funktion von **3301** wird durch die Konfigurationsregister **2913** vor der Ausführung von Algorithmen durch die CT bestimmt. Das Laden von **3301** wird durch ein gegenüber **2911** um die Verwaltung von **3301** erweitertes CT-Interface (**3302**) gesteuert. Der Vorteil von **3301** liegt darin, daß erheblich flexibler mit den unterschiedlichen Trigger- und RDY/ACK-Signalen umgegangen werden kann, als in fest implementierten **2910**. Nachteilhaft wirkt sich die Größe eines von **3301** aus. 5

[0217] Ein Kompromiß der zu der höchsten Flexibilität bei vertretbarer Größe führt ist, die Trigger und RDY/ACK-Signale durch eine Einheit gemäß **3301** auszuwerten und sämtliche festen Abläufe innerhalb der PAE durch eine fest implementierte Einheit nach **2910** zu steuern.

[0218] Die erfindungsgemäße PAE zur Verarbeitung von logischen Funktionen ist in Fig. 34 abgebildet. Kern der Einheit ist eine nachfolgend detaillierter beschriebene Einheit zum Verknüpfen von einzelnen Signalen (**3401**). Über die üblichen Register **2901**, **2902**, **2903**, **2904** werden die Bussignale mit **3401** verbunden. Die Register werden hierzu um einen Feed-Mode erweitert, der einzelne Signale selektiv ohne sie takt synchron zu speichern (register) zwischen den Bussen und **3401** austauscht. Der Multiplexer (**3402**) und die Konfigurationsregister (**3403**) werden an die unterschiedlichen Konfigurationen von **3401** angepaßt. Ebenso ist das CT-Interface (**3404**) entsprechend ausgestaltet. 10

[0219] Fig. 35 zeigt mögliche Ausgestaltungen von **3401**. Ein globaler Datenbus verbindet die Logikzellen **3501** und **3502** mit den Registern **2901**, **2902**, **2903**, **2904**. Durch Busschalter, die als Multiplexer, Gatter, Transmissionsgates oder einfachen Transistoren ausgelegt sein können wird **3504** mit den Logikzellen verbunden. Die Logikzellen können entweder komplett einheitlich gestaltet sein, oder unterschiedliche Funktionalität besitzen (**3501**, **3502**). **3503** stellt einen RAM-Speicher dar. 15

[0220] Mögliche Ausgestaltung der Logikzellen sind: 20

- Lookup Tabellen
- Logik
- Multiplexer
- Register

[0221] Die Auswahl der Funktionen und Vernetzung kann entweder flexibel programmierbar durch SRAM-Zellen erfolgen oder mittels unveränderlicher ROM oder semistatischer FlashROM Speicher.

[0222] Zur Beschleunigung von sequentiellen Algorithmen, die schlecht parallelisiert werden können ist bei herkömmlichen Prozessoren spekulative Ausführung bereits Stand der Technik. Die parallele Variante für VPUs ist in Fig. 36 dargestellt. Die Operanden (**3601**) werden gleichzeitig an mehrere möglichen Pfade von Teilalgorithmen (**3602a**, **3602b**, **3602c**) geführt. Die Teilalgorithmen können dabei einen unterschiedlichen Flächen- und Zeitbedarf aufweisen. Jeweils nach den Teilalgorithmen werden die Daten erfindungsgemäß gespeichert (**3612a**, **3612b**, **3612c**), bevor sie nach einer Umkonfiguration von den nächsten Teilalgorithmen verarbeitet werden (**3603**). Auch die Umkonfigurationszeitpunkte der einzelnen Teilalgorithmen sind voneinander unabhängig, ebenso die Zahl der Teilalgorithmen selbst (**3603**, **3614**). Sobald entscheidbar ist, welcher der Pfade zu wählen ist, werden die Pfade über einen Bus oder Multiplexer zusammengeführt (**3605**). Von einer Bedingung generierte Triggersignale (vgl. PACT08) (**3606**) bestimmen welcher der Pfade gewählt und an die nachfolgenden Algorithmen weitergeleitet wird. 30

[0223] Fig. 37 zeigt den Aufbau eines Hochsprachencompilers, der gewöhnliche sequentielle Hochsprachen (C, Pascal, Java) auf ein VPU-System übersetzt. Sequentieller Code (**3711**) wird von parallelem Code (**3708**) getrennt, wodurch **3708** direkt in dem Array von PAEs verarbeitet wird. 35

[0224] Für **3711** gibt es drei Ausführungsmöglichkeiten:

1. Innerhalb eines Sequenzers einer PAE (**2910**) 45
2. Mittels eines in die VPU konfigurierten Sequenzers. Der Compiler erzeugt hierzu einerseits einen auf die Aufgabe optimierten Sequenzer, andererseits direkt den algorithmenspezifischen Sequenzercode (vgl. **2801**).
3. Auf einem gewöhnlichen externen Prozessor (**3103**) Welche Möglichkeit gewählt wird hängt von der Architektur der VPU, des Computersystems und des Algorithmus ab. 50

[0225] Der Code (**3701**) wird zunächst in einem Präprozessor (**3702**) in Datenflußcode (**3716**) (der in einer speziellen Version der jeweiligen Programmiersprache datenflußoptimiert geschrieben wurde) und gewöhnlichen sequentiellen Code getrennt (**3717**). **3717** wird auf parallelisierbare Teilalgorithmen untersucht (**3703**), die sequentiellen Teilalgorithmen werden ausgesondert (**3718**). Die parallelisierbaren Teilalgorithmen werden als Makros vorläufig platziert und geroutet. 55

[0226] In einem iterativen Prozess werden die Makros mit dem datenflußoptimierten Code (**3713**) zusammen platziert, geroutet und partitioniert (**3705**). Eine Statistik (**3706**) wertet die einzelnen Makros, sowie deren Partitionierung hinsichtlich der Effizienz aus, wobei die Umkonfigurationszeit und der Aufwand der Umkonfiguration in die Effizienzbeurteilung einfließt. Ineffiziente Makros werden entfernt und als sequentieller Code ausgesondert (**3714**).

[0227] Der verbleibende parallele Code (**3715**) wird zusammen mit **3716** kompiliert und assembliert (**3707**) und VPU Objektcode ausgegeben (**3708**). 60

[0228] Eine Statistik über die Effizienz des generierten Codes, sowie der einzelnen (auch der mit **3714** entfernten Makros) wird ausgegeben (**3709**), der Programmierer erhält dadurch wesentliche Hinweise auf Geschwindigkeitsoptimierungen des Programmes.

[0229] Jedes Makro des verbleibenden sequentiellen Codes wird auf seine Komplexität und Anforderungen untersucht (**3720**). Aus einer Datenbank die von der VPU-Architektur und dem Computersystem abhängt (**3719**) wird der jeweils geeignete Sequenzer ausgewählt und als VPU-Code (**3721**) ausgegeben. Ein Compiler (**3721**) generiert den Assemblercode des jeweiligen Makros für den jeweils von **3720** gewählten Sequenzer und gibt ihn aus (**3711**). Die **3710** und **3720** 65

sind eng miteinander verknüpft. Gegebenenfalls verläuft die Abarbeitung iterativ um den geeignetsten Sequenzer mit minimalsten und schnellsten Assemblercode zu finden.

[0230] Ein Linker (3722) faßt die Assemblercodes (3708, 3711, 3721) zusammen und generiert den ausführbaren Objektcode (3723).

- 5 [0231] Fig. 38 zeigt den internen Aufbau von 2720. Kern der Schaltung ist ein ladbarer Up/Down-Zähler (3801), der seinen Startwert von der Schaltung Fig. 27 von dem Bus 3803 (entspricht 2703) über den entsprechend gesetzten Multiplexer 3802 erhält. Der Zähler dient als Programmzähler (PC) für den zugeordneten Sequenzer, der Startwert ist die erste Adresse des auszuführenden Programmes. Der Wert von 3801 wird über einen Addierer (3805) und 3802 auf den Zähler zurückgeführt. Über den Bus 3804 wird von dem Sequenzer ein Offset an 3805 geführt, der entweder vom PC abgezogen oder hinzuaddiert wird. Damit sind relative Sprünge effizient implementierbar. Der PC wird über den Bus 3811 an das PAE-Array herausgeführt und kann für call-Operationen auf dem Stack gespeichert werden. Für ret-Operationen wird der PC über 3804 und 3802 vom Stack auf 3801 geführt.

- [0232] Über den Multiplexer 3806 wird entweder der PC oder ein vom PAE-Array zugeführter Stackpointer (3807) auf einen Addierer (3808) geführt. Hier wird ein Offset den Werten abgezogen oder hinzuaddiert, der im Register 3809 gespeichert wird und über 3803 geschrieben wird. 3808 ermöglicht die Verschiebung des Programmes innerhalb des Speichers 2711. Dadurch werden Garbage-Collector Funktionen zum Aufräumen des Speichers möglich (vgl. PACT10). Die Adressverschiebung die durch den Garbage-Collector auftritt wird durch eine Anpassung des Offsets in 3809 ausgeglichen.

- [0233] Fig. 38a ist eine Variante von Fig. 38 in der der Stackpointer (3820) ebenfalls integriert ist. Über 3804 wird nur noch der Offset für relative Sprünge an 3805 geführt (3804a). Der Stackpointer ist ein Up/Down-Zähler entsprechend 3801, dessen Startwert den Beginn des Stack repräsentiert, und über 3803 geladen wird. Der PC wird direkt an den Datenbus zum Speicher geführt um über einen Multiplexer bei call-Operationen auf den Stack geschrieben zu werden. Der Datenbus des Speichers wird über 3821 und 3802 auf 3801 zurückgekoppelt, zur Durchführung von ret-Operationen.

- [0234] Fig. 39 verdeutlicht die Funktionsweise der Speicher. Der Speicher (3901) wird über einen Multiplexer (3902) adressiert. Im Standard-Modus, Lookup-Modus und Register Modus werden die Adressen aus dem Array (3903) direkt an 3901 geführt. Im Stack-Modus und FIFO-Modus werden die Adressen in einem up/down-Zähler (3904) generiert. In diesem Fall werden die Adressen der IO-Seite von einem weiteren up/down-Zähler (3905) zur Verfügung gestellt. Die Adressen für den externen RAM (oder IO) werden von einem weiteren up/down-Zähler (3906) generiert, die Basisadresse wird von einem Register (3907) geladen. Das Register wird von der CT oder einem externen Host-Prozessor gesetzt. Die gesamte Steuerung übernimmt eine Statemachine (3908). Den Zustand des Speichers (voll, leer, halbvoll, etc.) entnimmt 3908 einem up/down-Zähler (3909) der die Anzahl der im Speicher befindlichen Worte zählt. Wird der Speicher blockweise verändert (Stadt auf externen Stack schreiben oder von externem Stack lesen) wird die Größe des Blocks als Konstante (3917) auf einen Addierer/Subtrahierer (3910) gegeben, auf den der Zählerstand von 3909 zurückgekoppelt ist. Das Ergebnis wird nach 3909 geladen. Damit läßt sich der Zählerstand schnell an blockweise Veränderungen anpassen. (Natürlich ist es möglich den Zähler auch mit jedem geschriebenen oder gelesenen Wort bei einer Blockoperation zu modifizieren). Für Cache-Operationen steht ein Cache-Kontroller (3911) nach dem Stand der Technik zur Verfügung, dem ein Tag-Speicher (3912) zugeordnet ist. Je nach Betriebsart wird der Wert von 3911 oder 3906 über einen Multiplexer (3913) als Adresse nach außen geführt (3914). Über den Bus 3915 werden die Daten nach außen geführt und über den Bus 3916 werden die Daten mit dem Array ausgetauscht.

40 Programmierbeispiele zur Verdeutlichung von Teilalgorithmen

[0235] Ein Modul kann beispielsweise folgendermaßen deklariert werden:

- ```

module example1
45 input (var1, var2 : ty1; var3 : ty2).
 output (res1, res2 : ty3).
 begin
 ...
 register <regname1> (res1).
50 register <regname2> (res2).
 terminate@ (res1 & res2; 1).
 end.
 module kennzeichnet den Beginn eines Modules.
 input/output definiert die Ein-/Ausgangsvariablen mit den Typen tyn.
55 begin ... end markieren den Rumpf des Modules.
 register <regname1/2> übergibt das Ergebnis an den Output,
 wobei des Ergebnis in dem durch <regname1/2> spezifizierten Register zwischengespeichert wird. <regname1/2> ist dabei eine globale Referenz auf ein bestimmtes Register.
```

- [0236] Als weitere Übergabemodi an den Output stehen beispielsweise folgende Speicherarten zur Verfügung:
- 60 fifo <fifoname>, wobei die Daten an einen nach dem FIFO-Prinzip arbeitenden Speicher übergeben werden. <fifoname> ist dabei eine globale Referenz auf einen bestimmten, im FIFO-Modus arbeitenden Speicher. terminate@ wird dabei um den Parameter bzw. das Signal "fifofull" erweitert, der/das anzeigt, daß der Speicher voll ist.
- stack <stackname>, wobei die Daten an einen nach dem Stack-Prinzip arbeitenden Speicher übergeben werden. <stackname> ist dabei eine globale Referenz auf einen bestimmten, im Stack-Modus arbeitenden Speicher.

- 65 [0237] terminate@ unterscheidet die Programmierung entsprechend des erfindungsgemäßen Verfahrens von der herkömmlichen sequentiellen Programmierung. Der Befehl definiert das Abbruchkriterium des Modules. Die Ergebnisvariablen res1 und res2 werden von terminate@ nicht mit ihrem tatsächlichen Wert evaluiert, statt dessen wird nur die Gültigkeit der Variablen (also deren Statussignal) geprüft. Dazu werden die beiden Signale res1 und res2 boolsch miteinander

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der verknüpft, z. B. durch eine UND-, ODER- oder XOR-Operation. Sind beide Variablen gültig, terminiert das Modul mit dem Wert 1. Das bedeutet, ein Signal mit dem Wert 1 wird an die übergeordneten Ladeinheit weitergeleitet, woraufhin die übergeordnete Ladeinheit das nachfolgende Module lädt.

```
module example2
input (var1, var2 : ty3; var3 : ty2)
output (res1, ty4).
begin
register <regname1> (var1, var2).
fifo <fifoname1> (res1, 256).
...
terminate@ (fifofull (<fifoname1>); 1).
end.
```

**[0238]** register wird in diesem Beispiel über input-Daten definiert. Dabei ist <regname1> derselbe wie in example1. Dies bewirkt, daß das Register, das die output-Daten in example1 aufnimmt, die input-Daten für example2 zur Verfügung stellt.

**[0239]** fifo definiert einen FIFO-Speicher der Tiefe 256 für die Ausgangsdaten res1. Das Full-Flag (fifofull) des FIFO-Speichers wird in terminate@ als Abbruchkriterium verwendet.

```
module main
input (in1, in2 : ty1; in3 : ty2).
output (out1 : ty4).
begin
define <regname1>: register(234)
define <regname2>: register(26).
define <fifoname1>: fifo(256,4). // FIFO Tiefe 256
...
(var12, var72) = call example1 (in1, in2, in3).
...
(out1) = call example2 (var12, var72, var243).
...
signal (out1)
terminate@ (example2).
end.
```

**[0240]** define definiert eine Schnittstelle für Daten (Register, Speicher, etc.). Bei der Definition werden die erforderlichen Ressourcen, sowie die Bezeichnung der Schnittstelle angegeben. Da die Ressourcen jeweils nur einmal zur Verfügung stehen, müssen sie eindeutig angegeben werden. Damit ist die Definition global, d. h. die Bezeichnung gilt für das gesamte Programm.

**[0241]** call ruft ein Modul als Unterprogramm auf.

**[0242]** signal definiert ein Signal als Ausgangssignal, ohne daß eine Zwischenspeicherung verwendet wird.

**[0243]** Durch terminate@ (example2) wird das Modul main terminiert, sobald das Unterprogramm example2 terminiert.

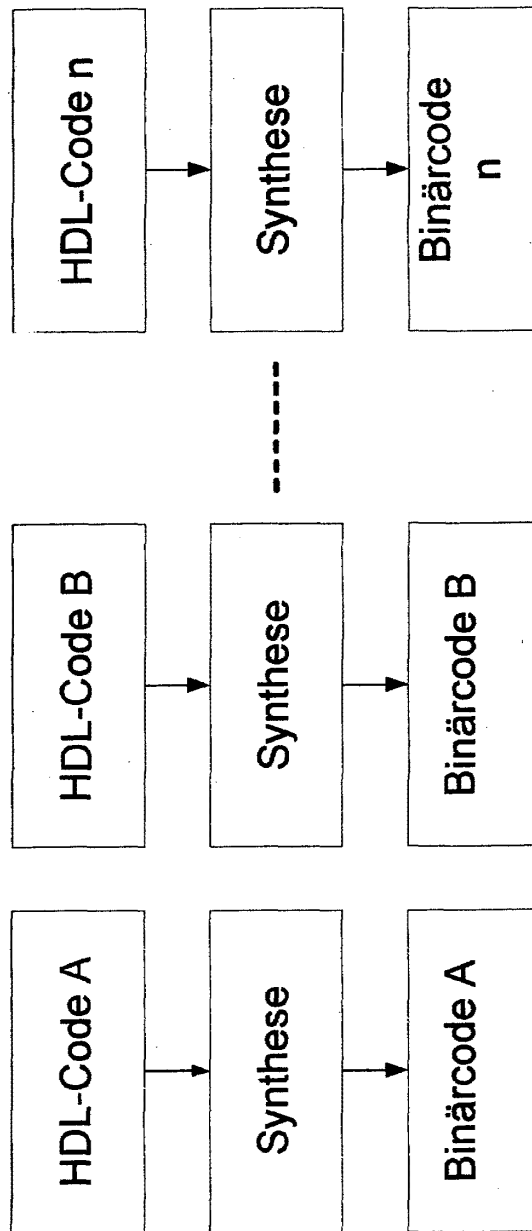
**[0244]** Durch die globale Deklaration "define . . ." ist es prinzipiell nicht mehr notwendig, die so definierten input/output Signale in die Schnittstellen-Deklaration der Module aufzunehmen.

## Patentansprüche

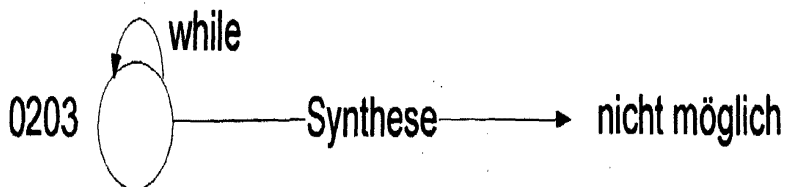
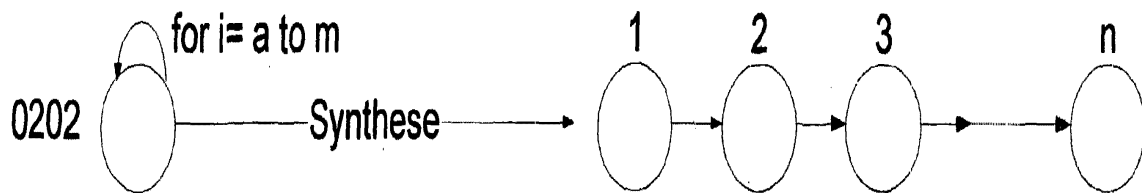
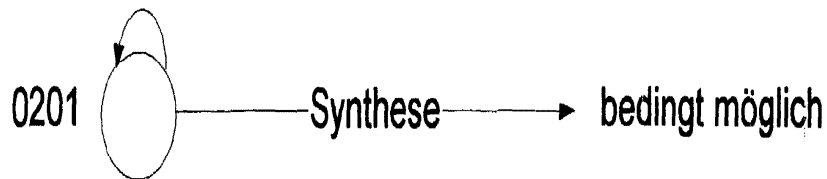
Verfahren zum Betrieb einer umkonfigurierbaren Einheit, **dadurch gekennzeichnet**, daß die Quittierungssignale der konfigurierbaren Zellen zeitlich versetzt zu deren Konfiguration ausgewertet werden.

Hierzu 44 Seite(n) Zeichnungen

- Leerseite -



**Fig. 1**    **Stand der Technik**



**Fig. 2 Stand der Technik**

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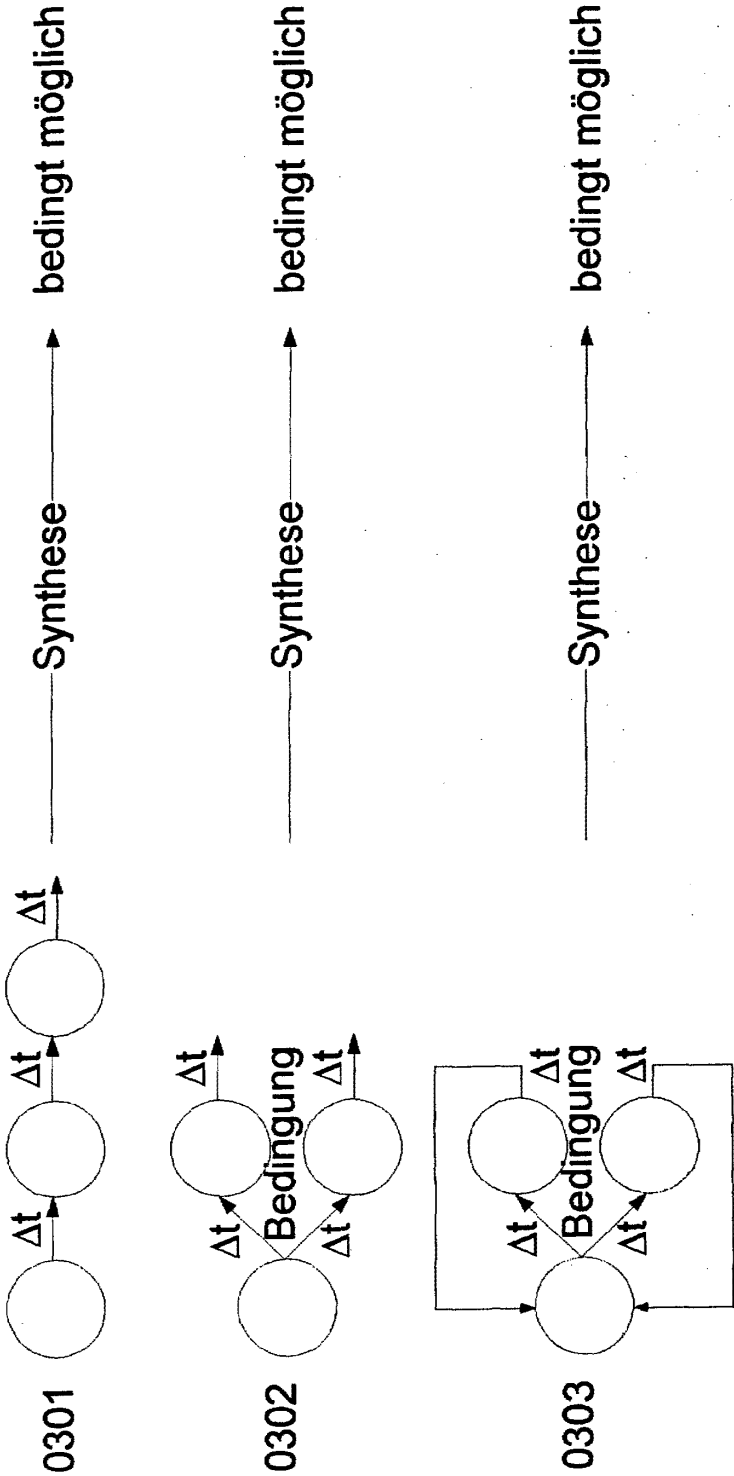
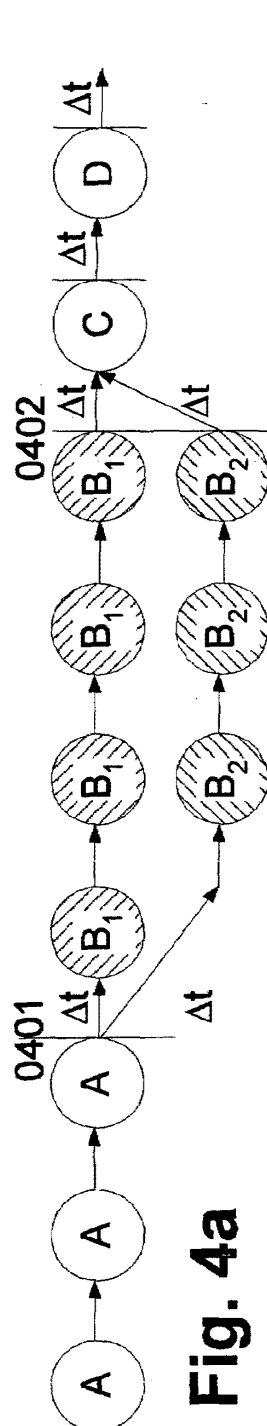
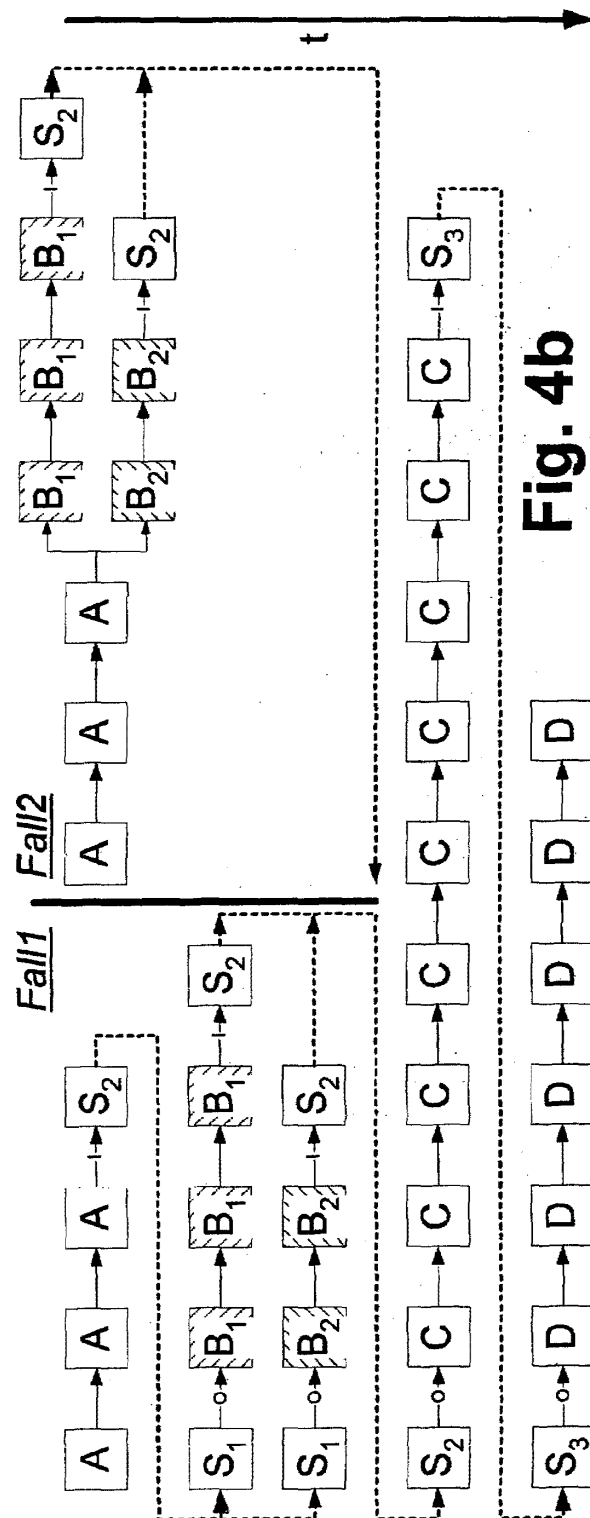


Fig. 3 Stand der Technik



**Fig. 4a**



**Fig. 4b**

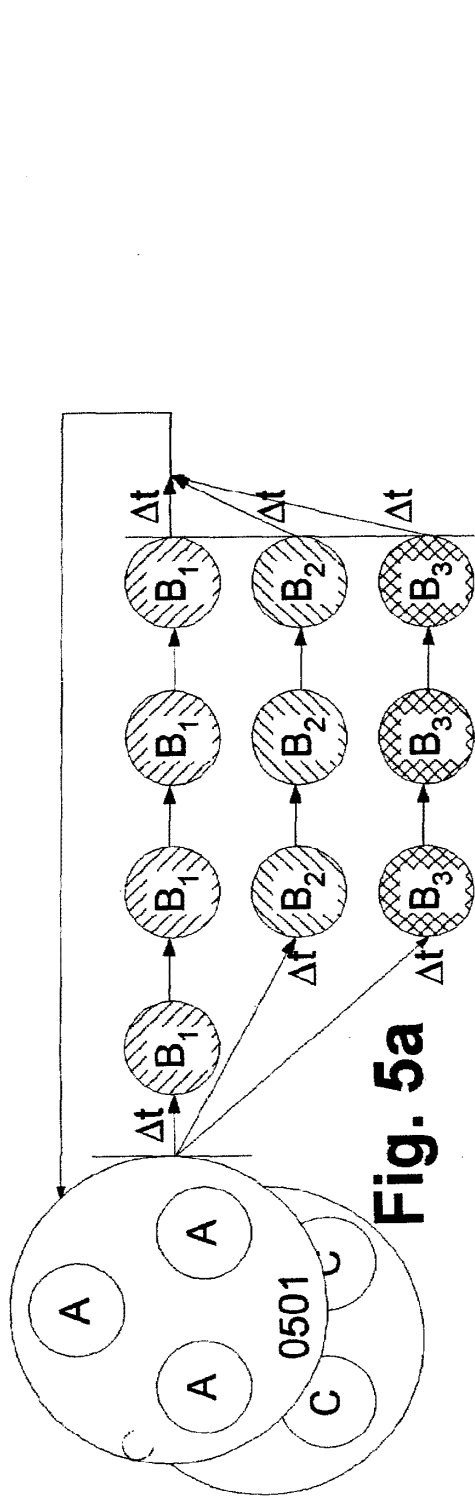


Fig. 5a

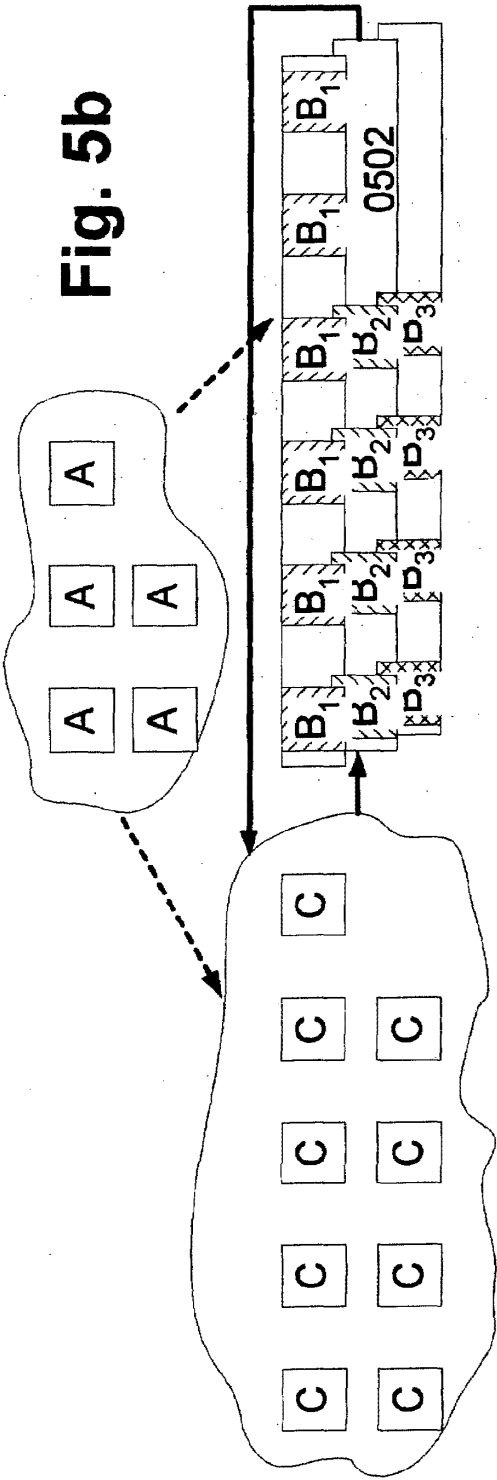
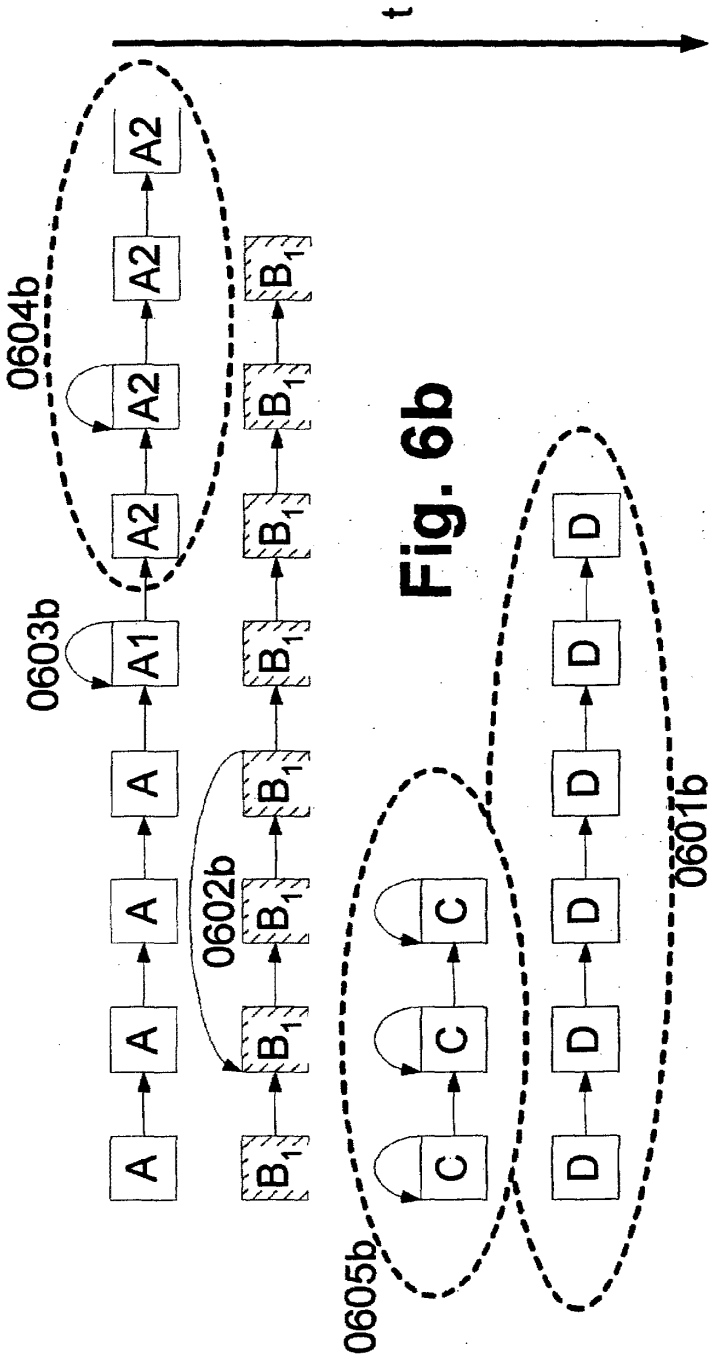
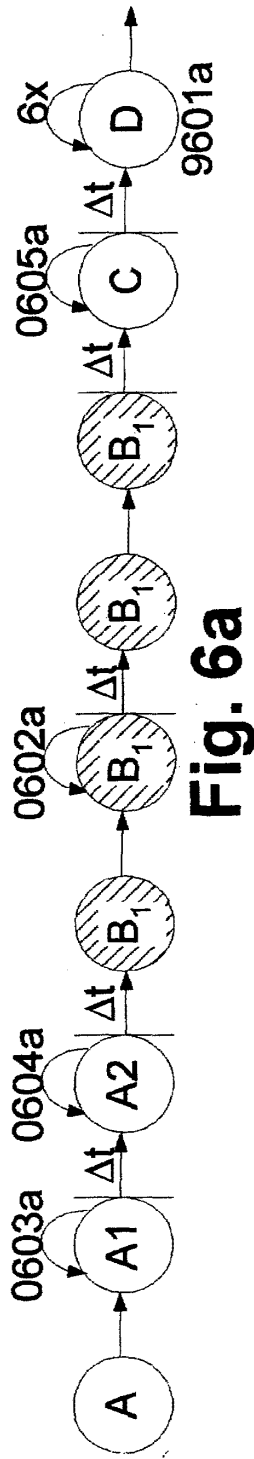
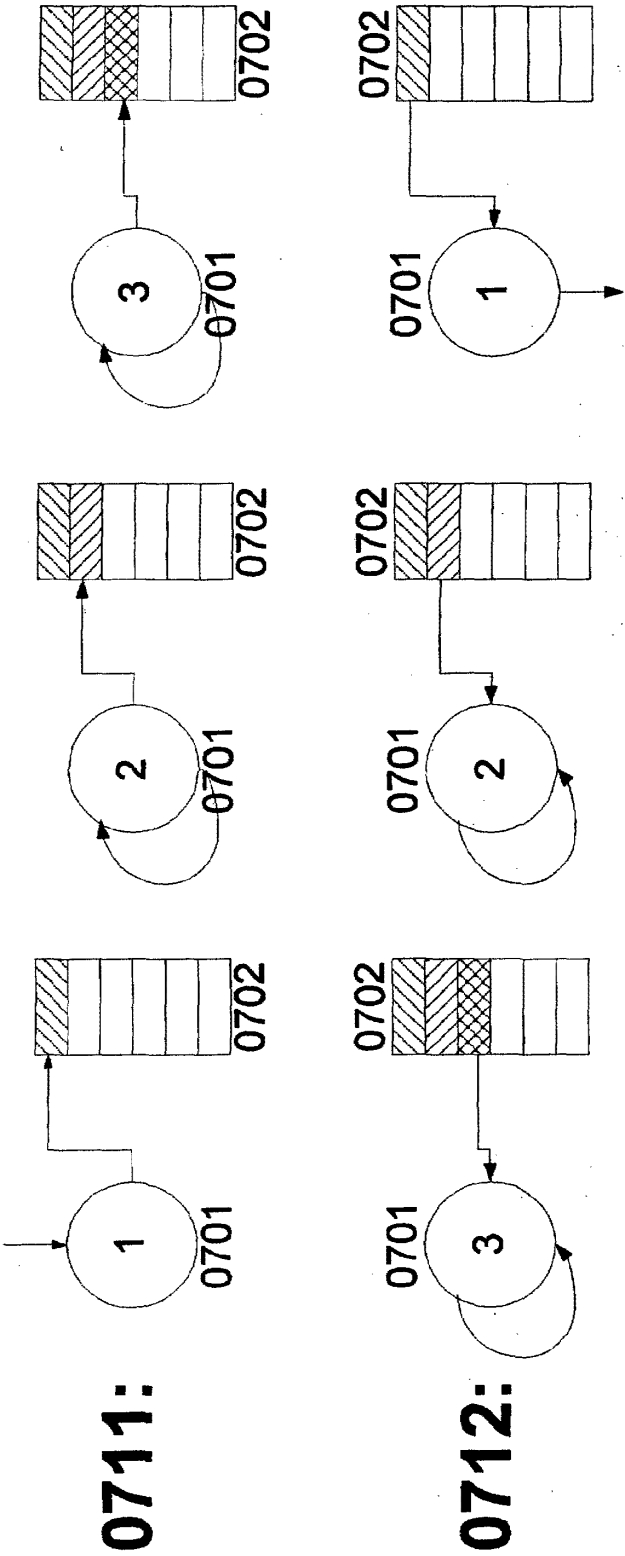


Fig. 5b





**Fig. 7**

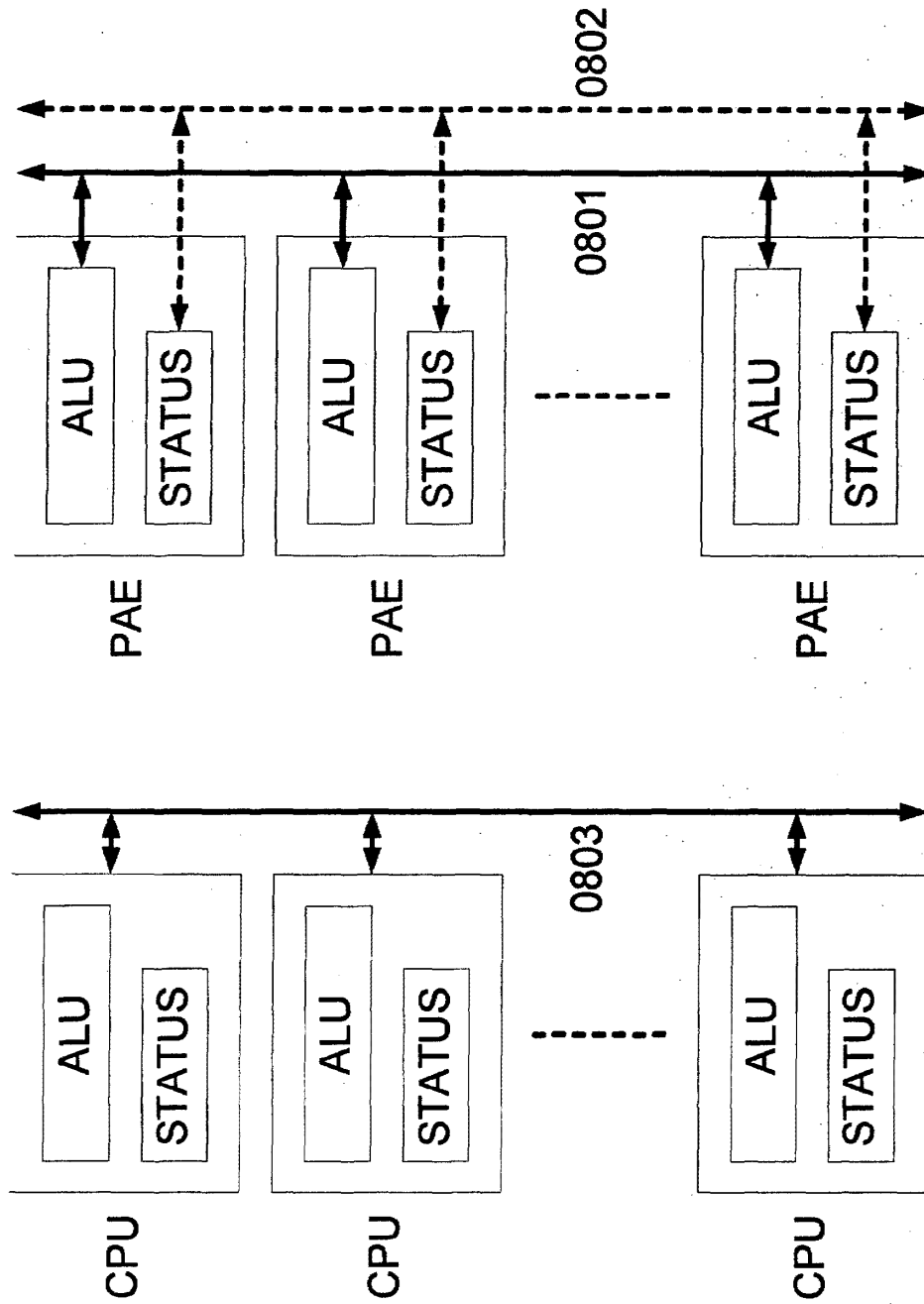
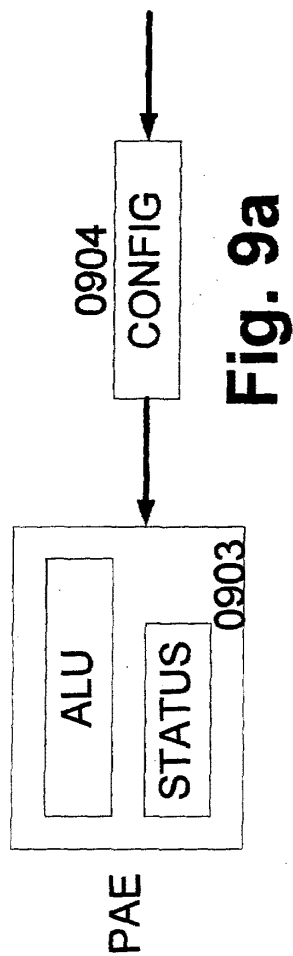
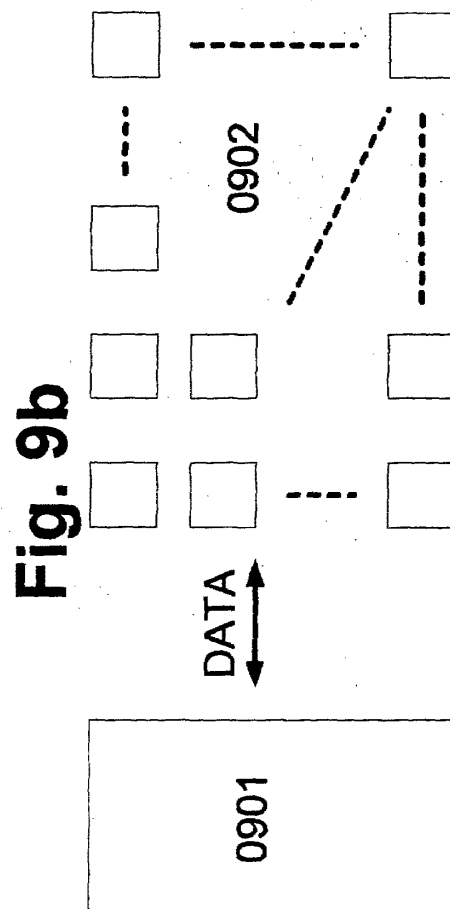


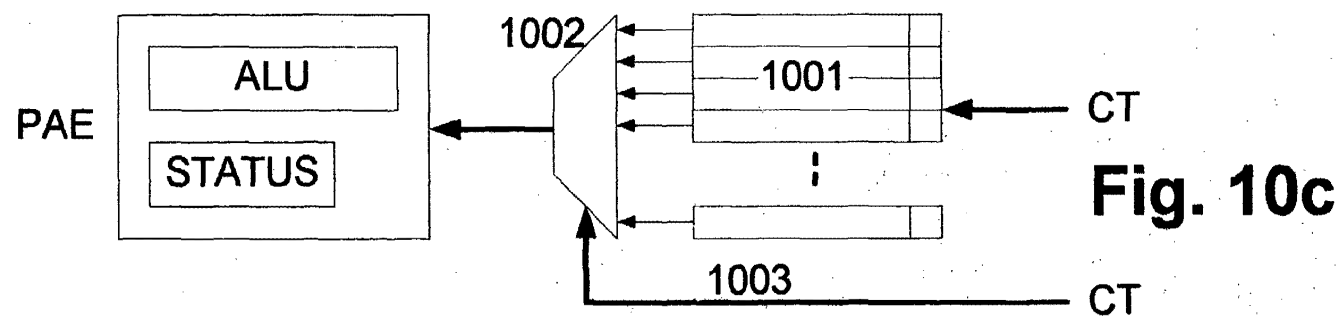
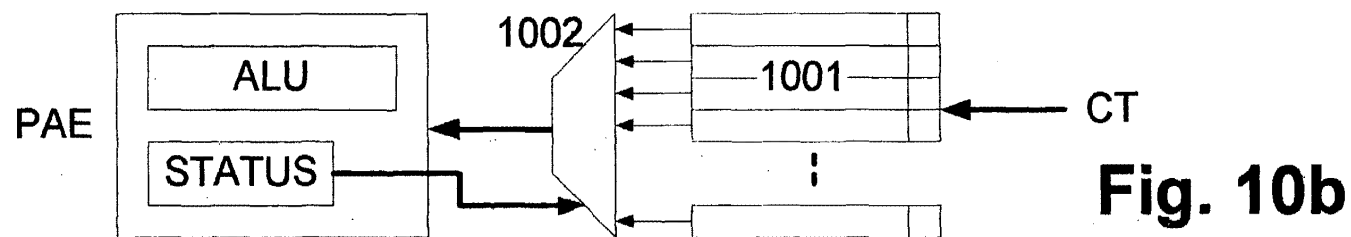
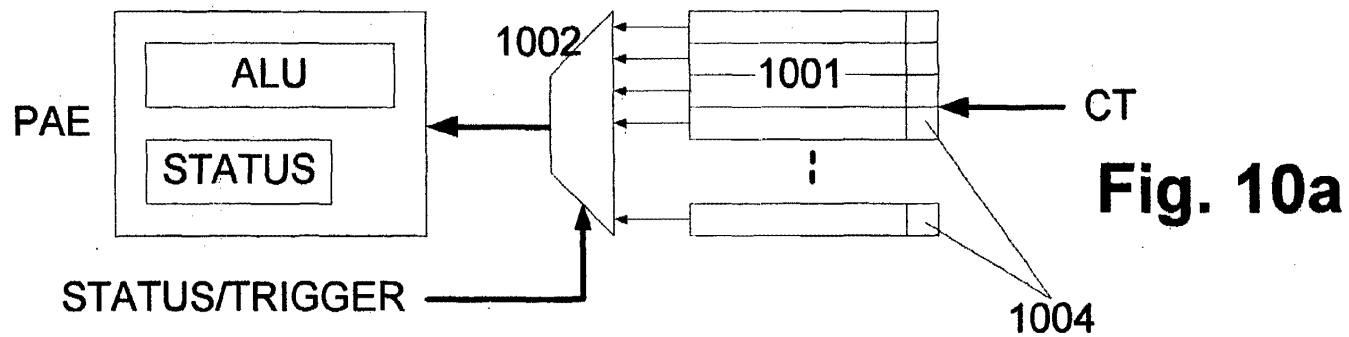
Fig. 8b

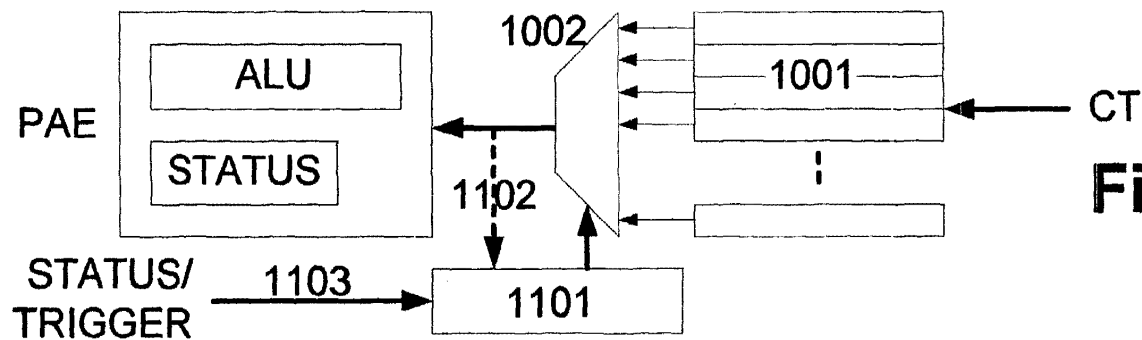
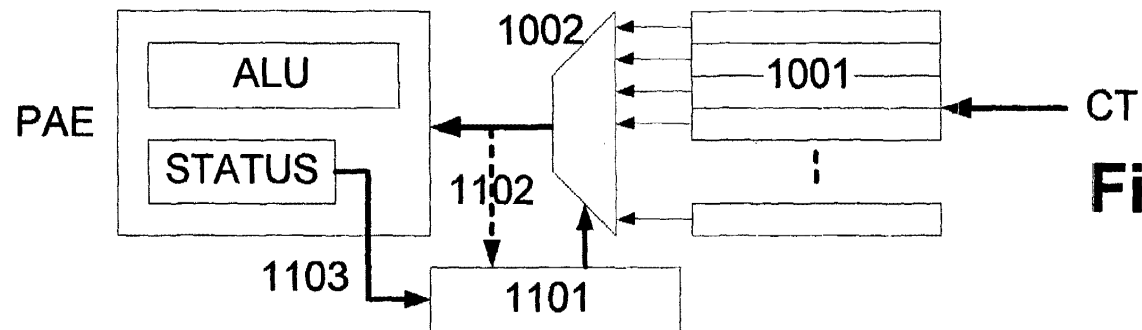
Fig. 8a Stand der Technik



# Stand der Technik







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**Fig. 12**

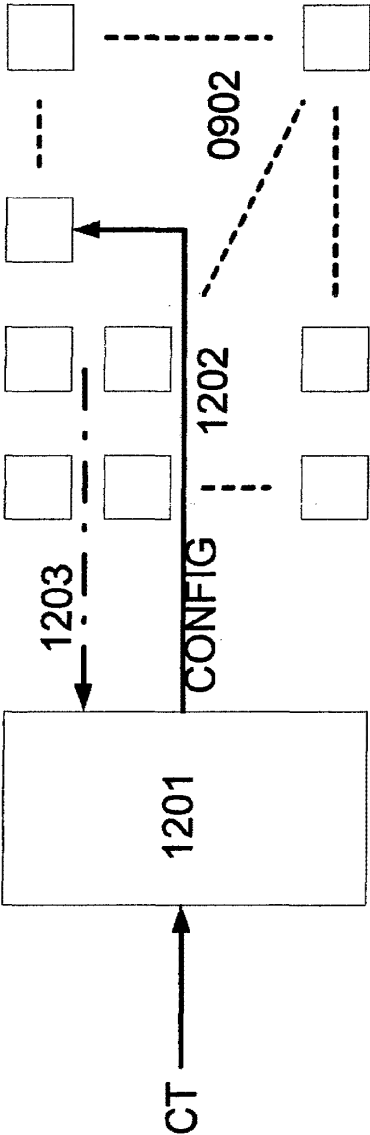


Fig.

13a

130

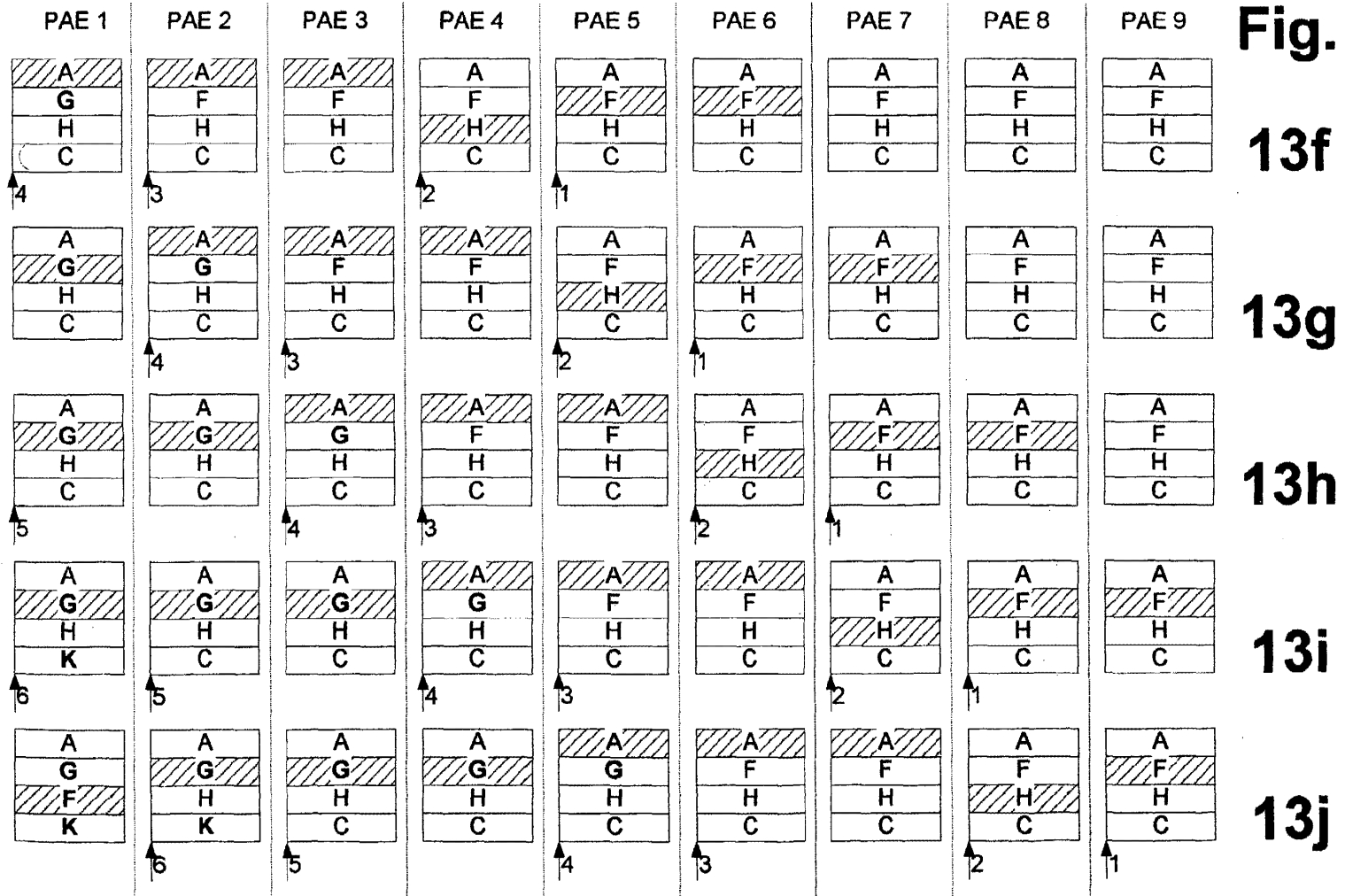
130

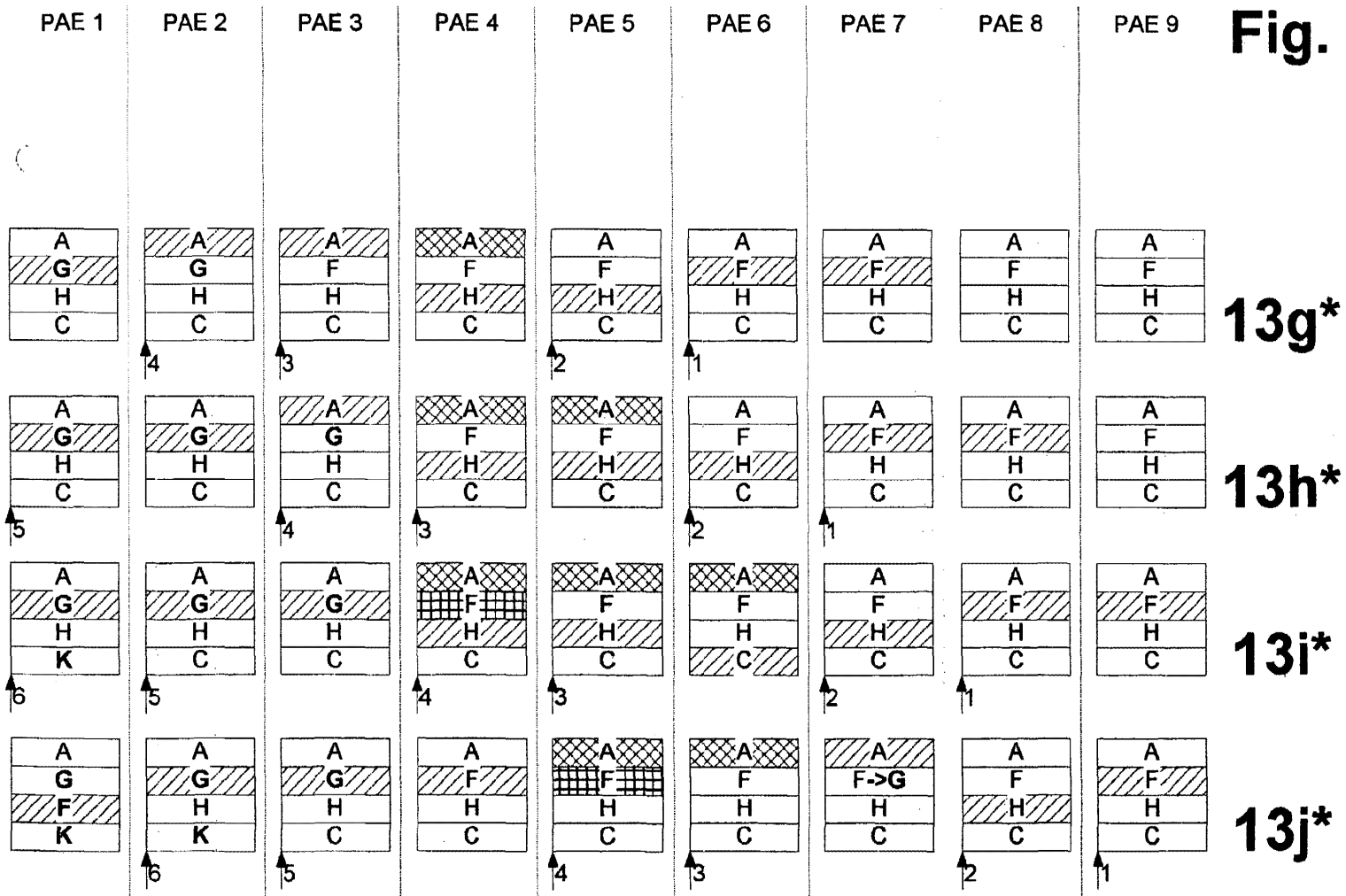
13d

136

|              |                             |                             |                             |                             |                             |
|--------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|-----------------------------|
| <b>PAE 9</b> | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            |
| <b>PAE 8</b> | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            |
| <b>PAE 7</b> | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            |
| <b>PAE 6</b> | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            |
| <b>PAE 5</b> | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br><del>F</del><br>H<br>C |
| <b>PAE 4</b> | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br><del>F</del><br>H<br>C | A<br><del>F</del><br>H<br>C |
| <b>PAE 3</b> | A<br>F<br>H<br>C            | A<br>F<br>H<br>C            | A<br><del>F</del><br>H<br>C | A<br><del>F</del><br>H<br>C | A<br>F<br><del>H</del><br>C |
| <b>PAE 2</b> | A<br>F<br>H<br>C            | A<br><del>F</del><br>H<br>C | A<br><del>F</del><br>H<br>C | A<br>F<br><del>H</del><br>C | <del>A</del><br>F<br>H<br>C |
| <b>PAE 1</b> | A<br><del>F</del><br>H<br>C | A<br><del>F</del><br>H<br>C | A<br>F<br><del>H</del><br>C | <del>A</del><br>F<br>H<br>C | <del>A</del><br>F<br>H<br>C |

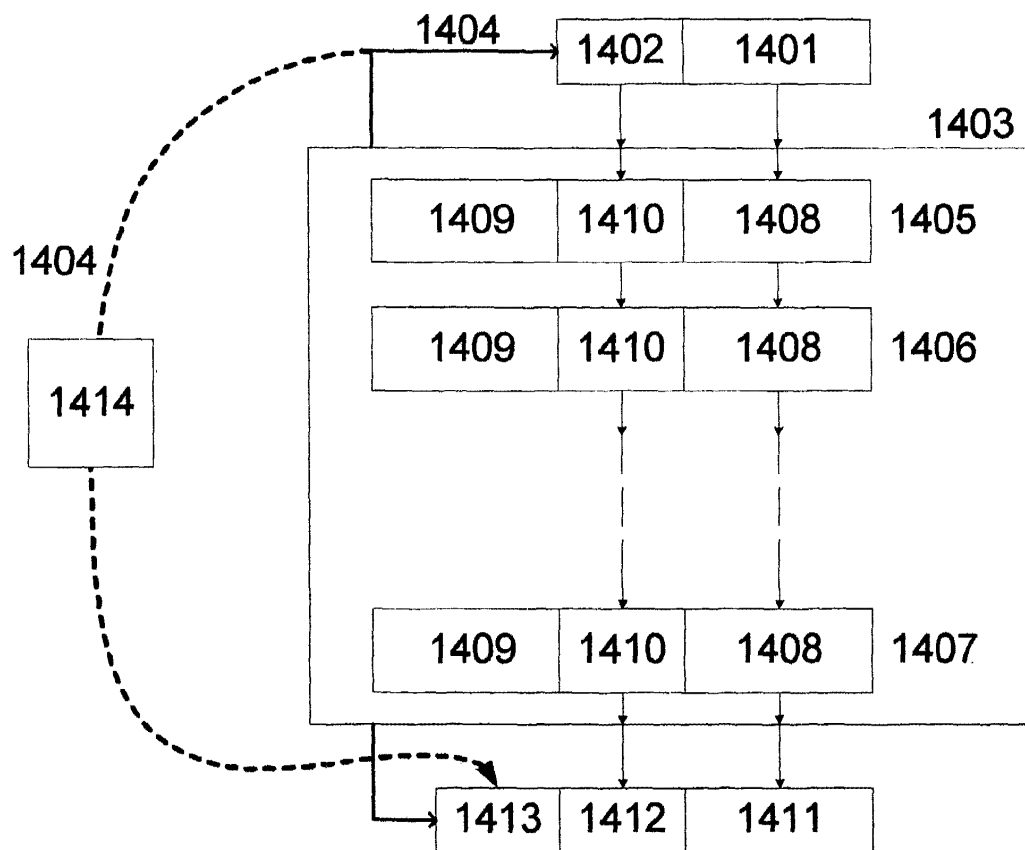
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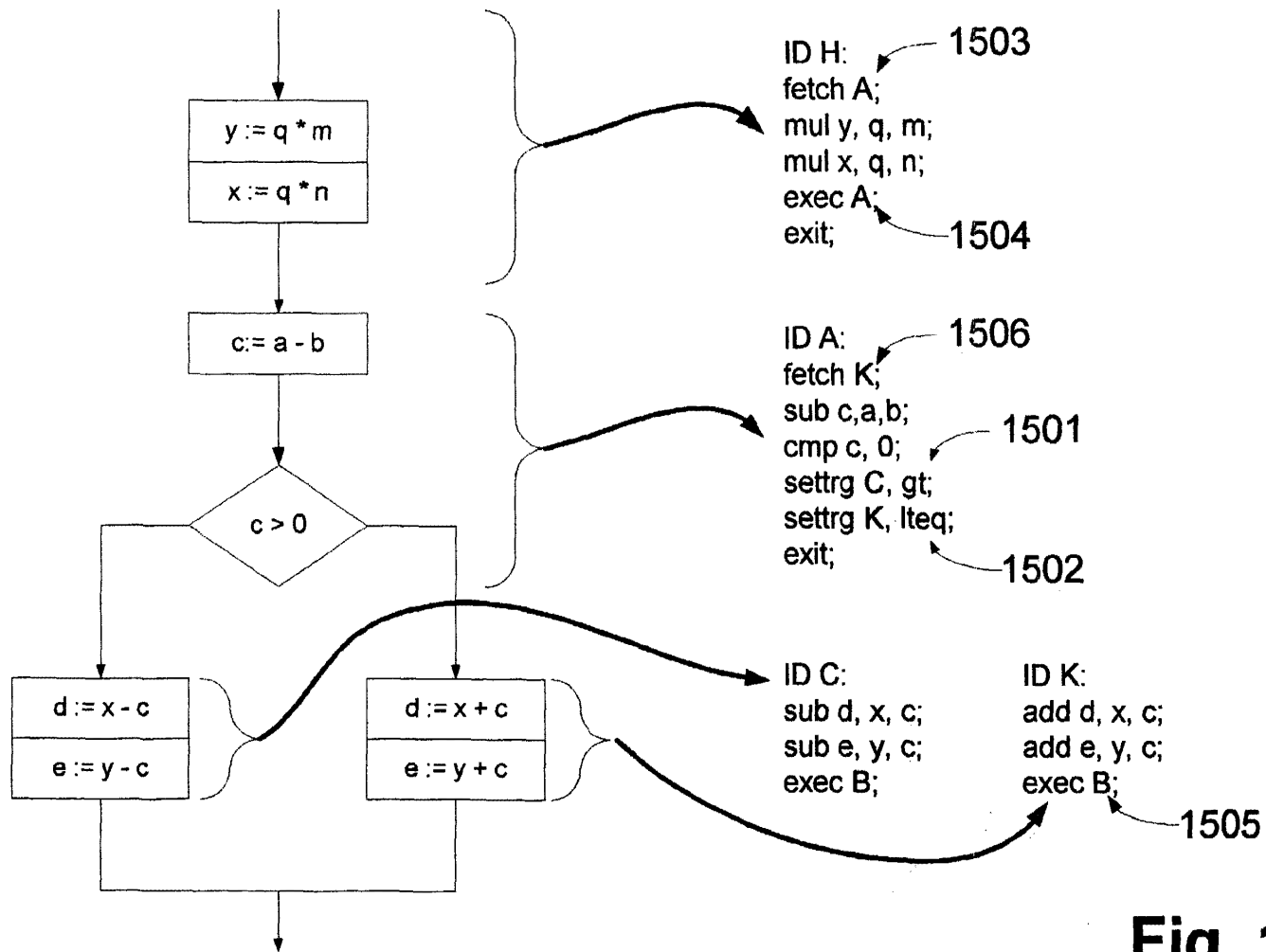


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**Fig. 14**



**Fig. 15**

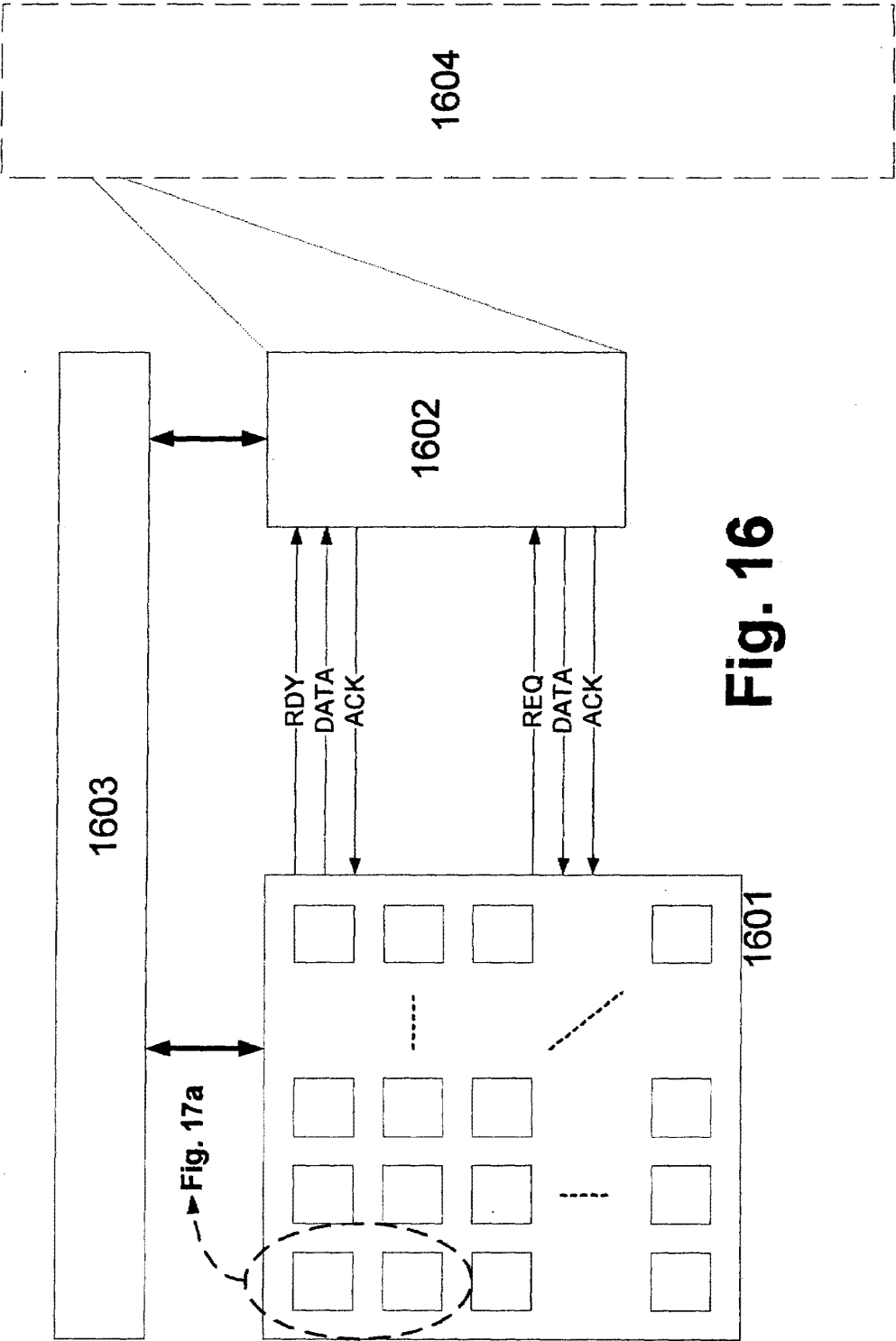
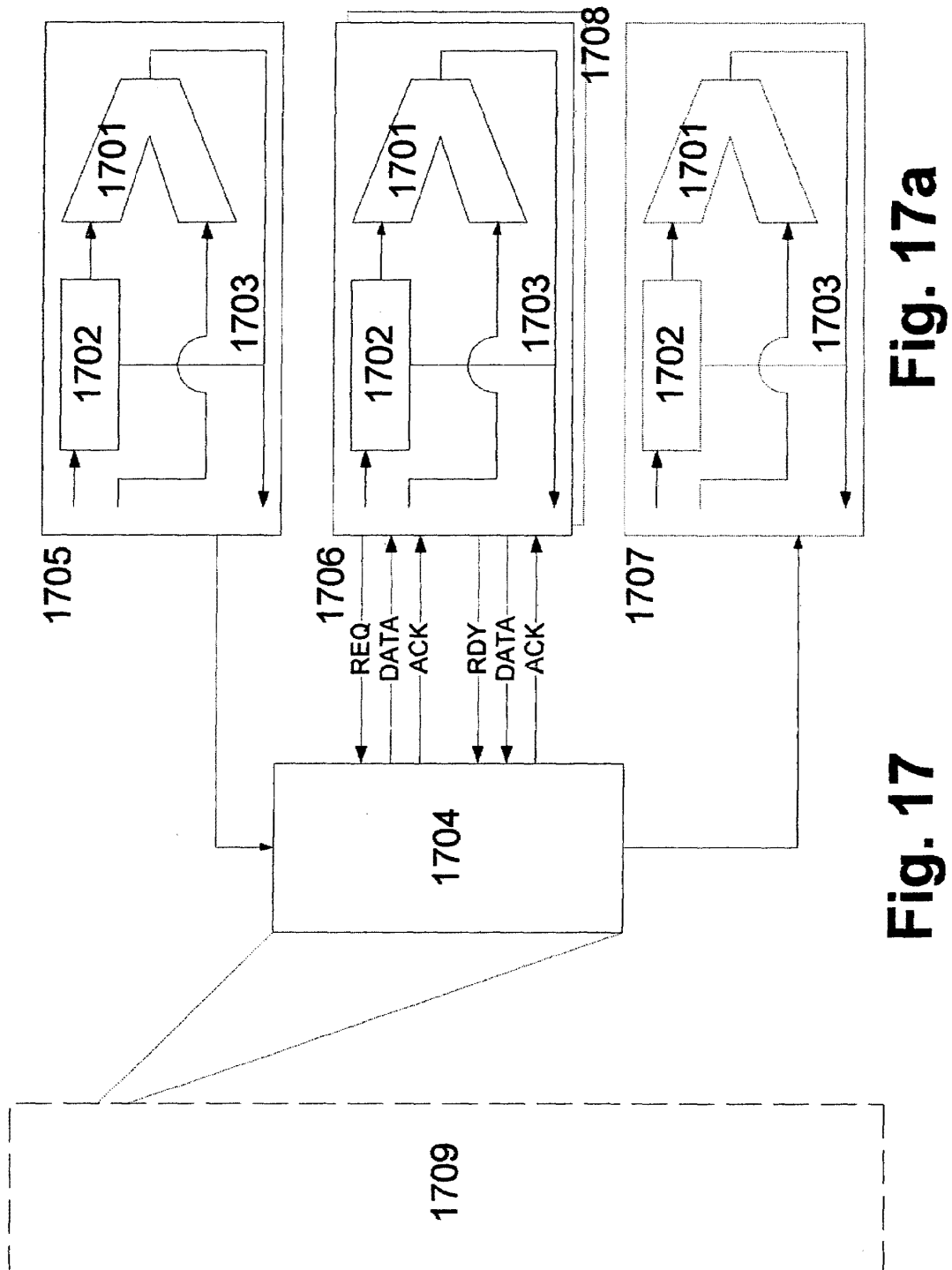


Fig. 16



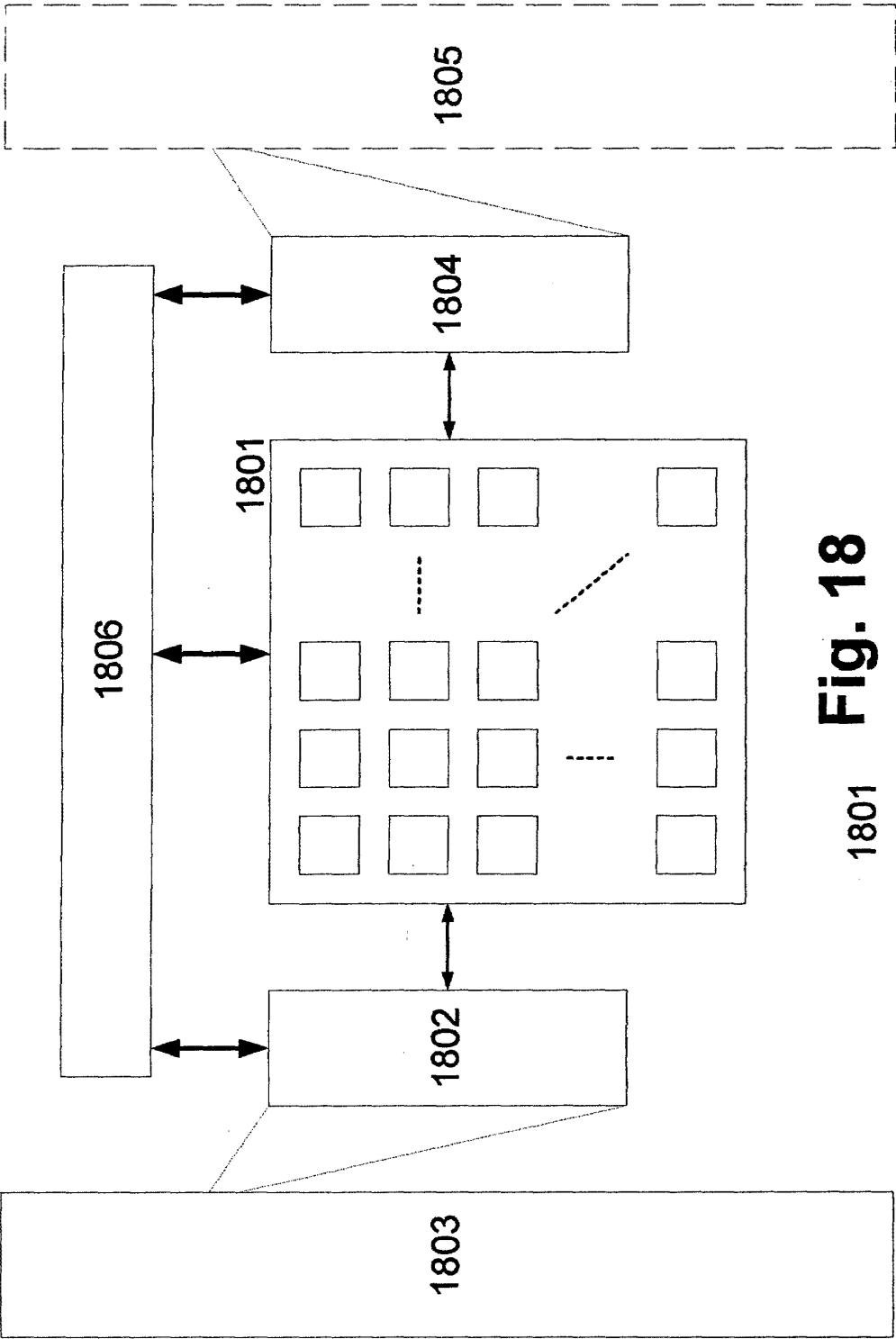
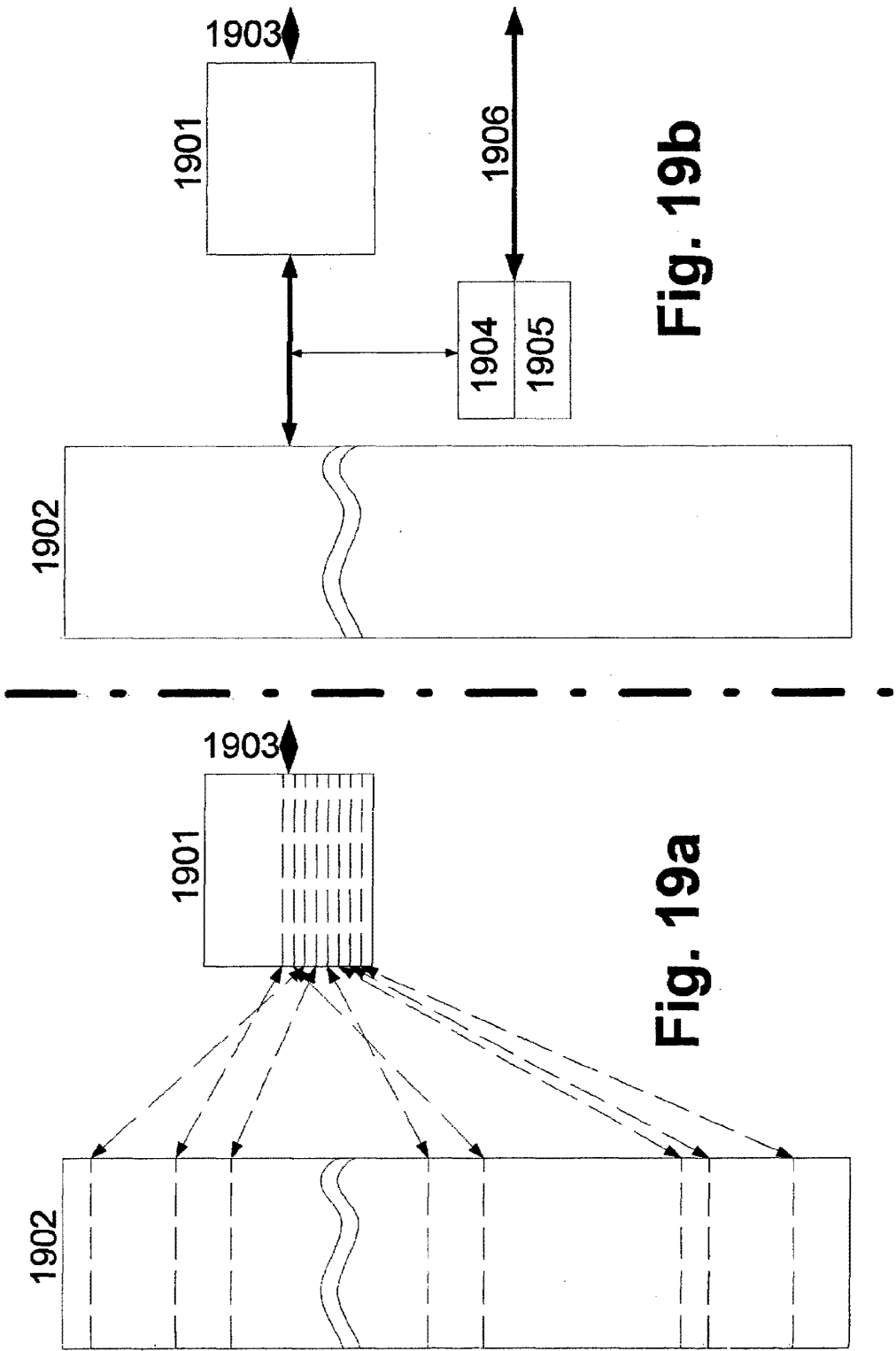
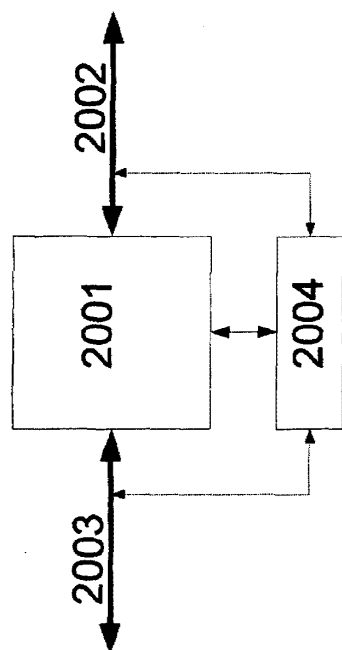
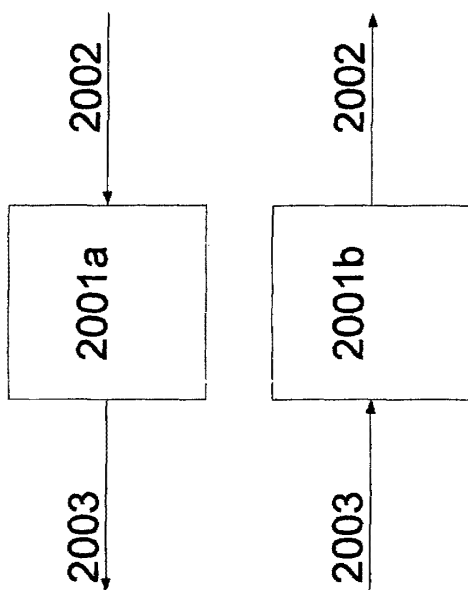


Fig. 18

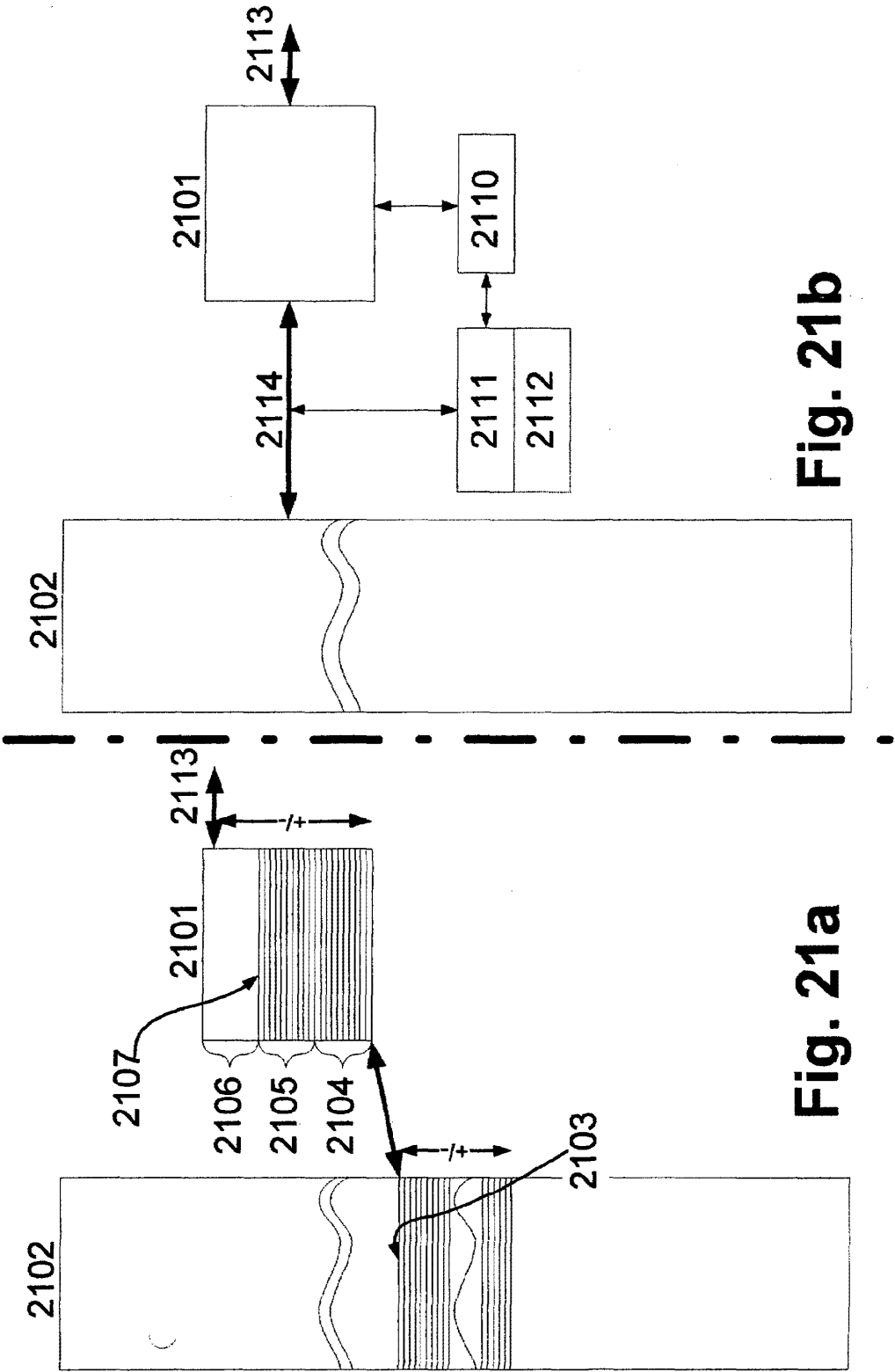


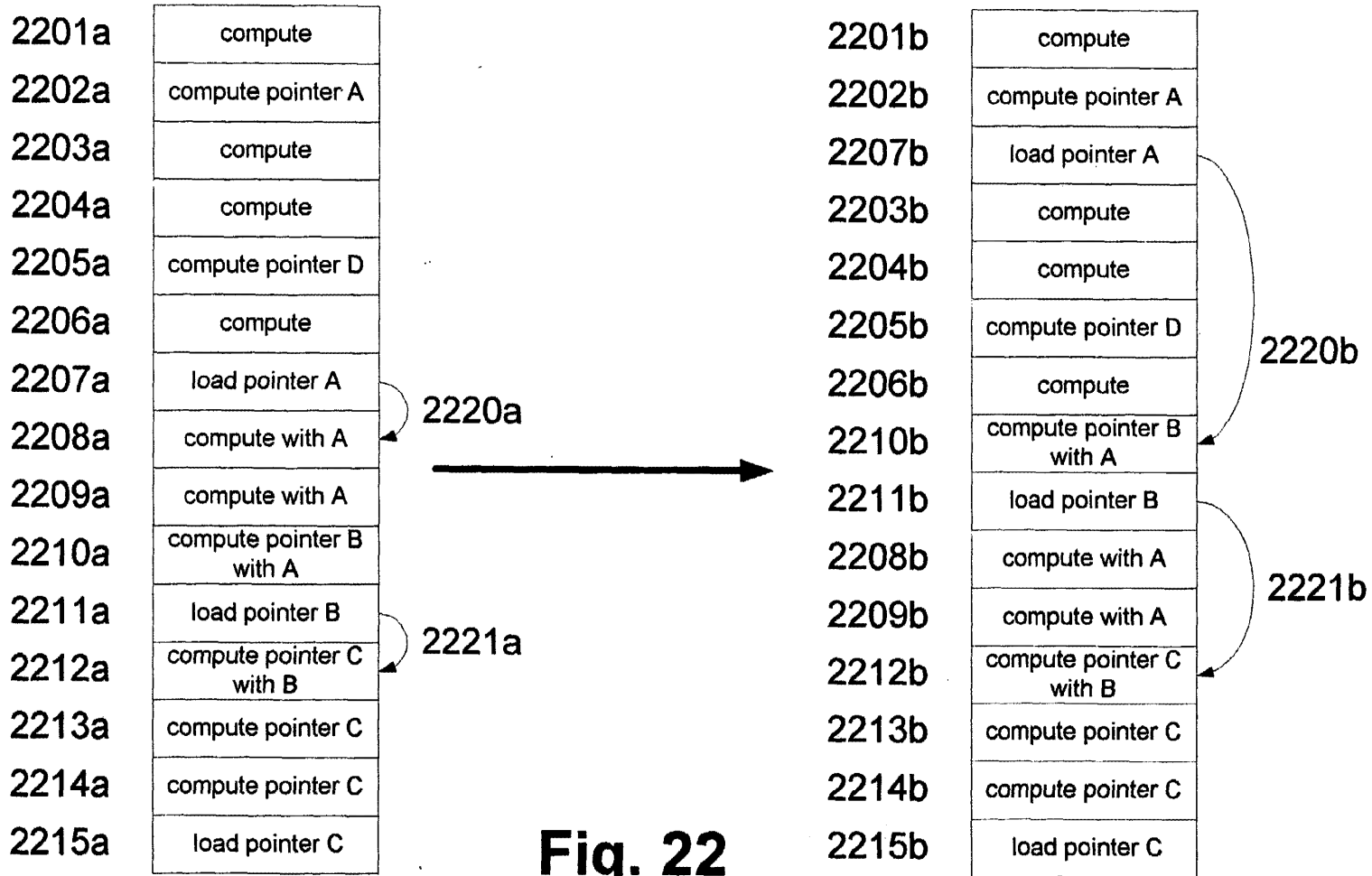


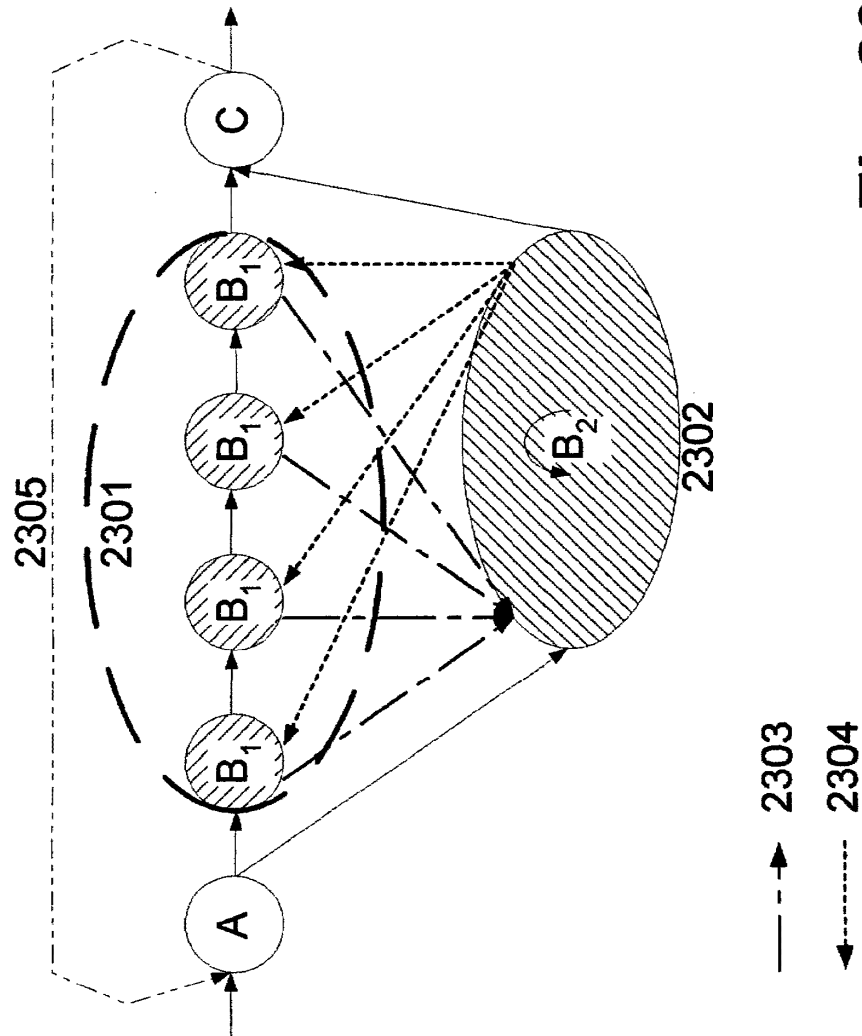
**Fig. 20b**



**Fig. 20a**







**Fig. 23**

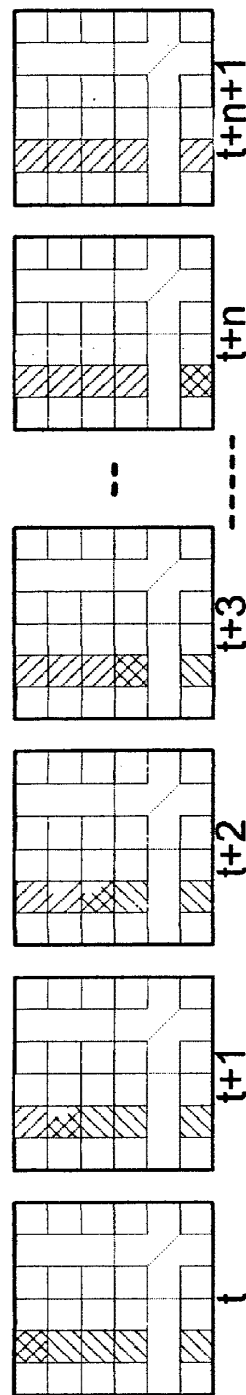


Fig. 24a

- 2401
- 2402
- 2403

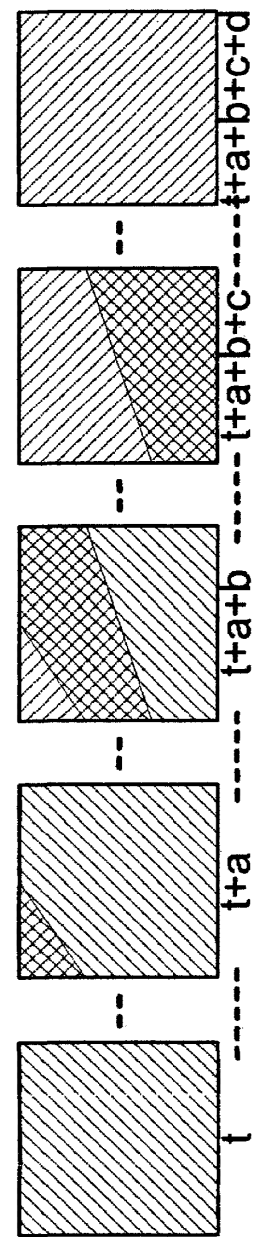
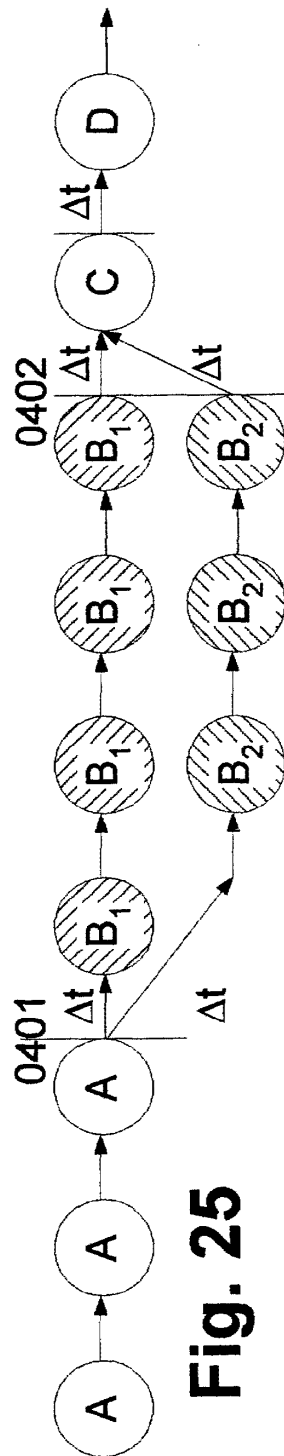
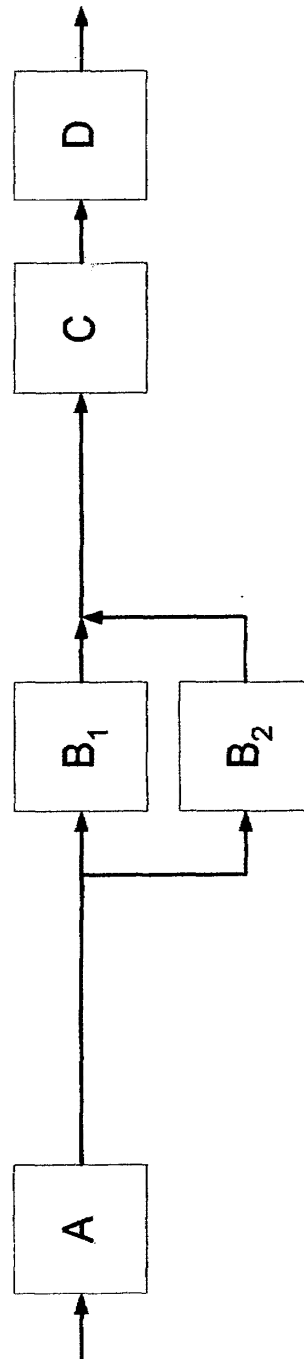
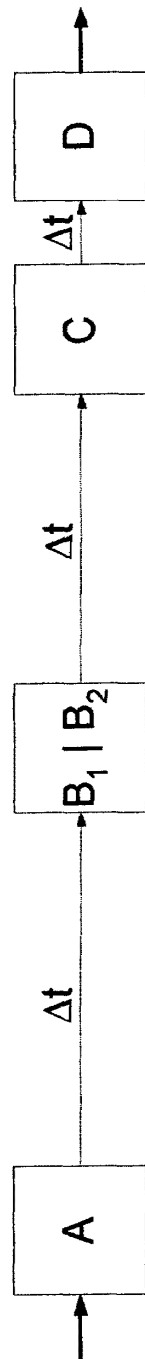


Fig. 24b



**Fig. 25**



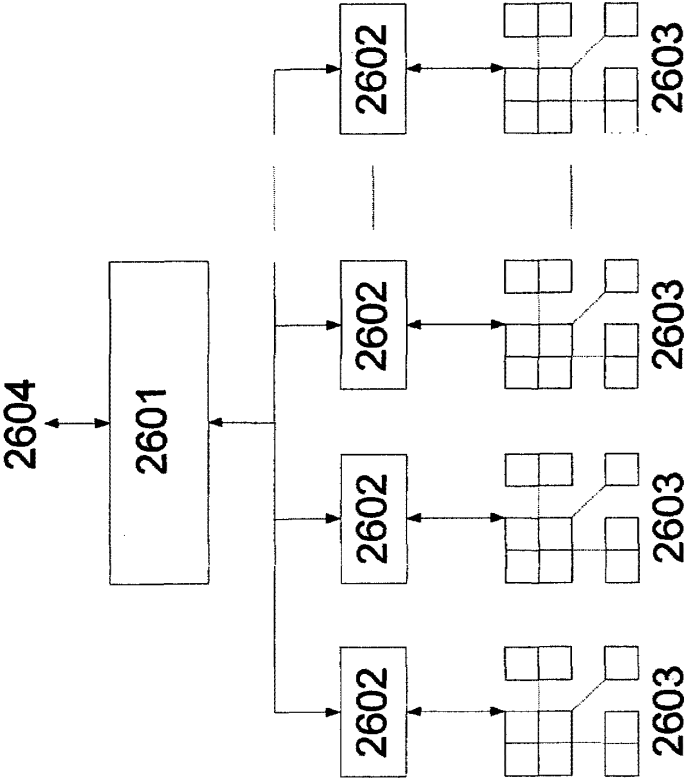
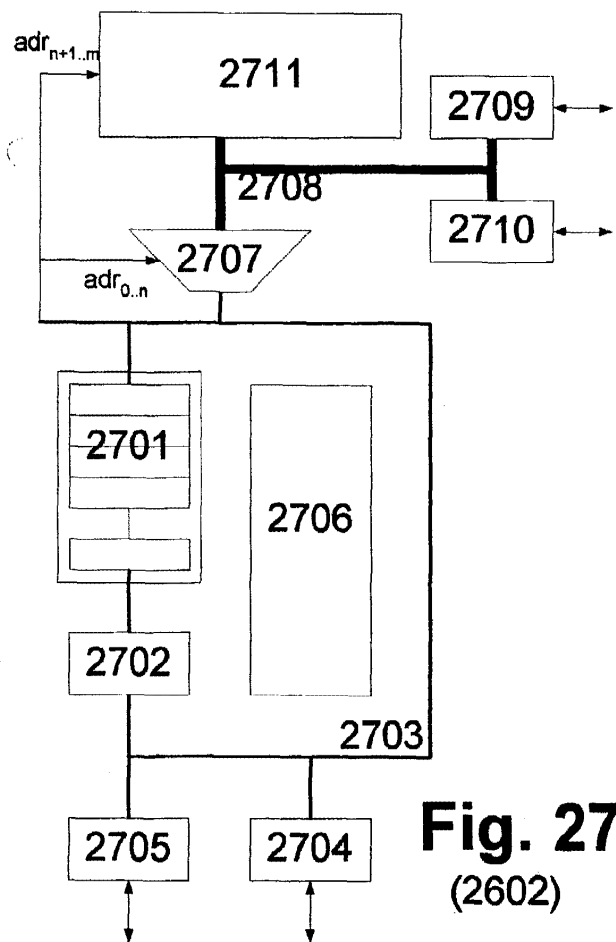
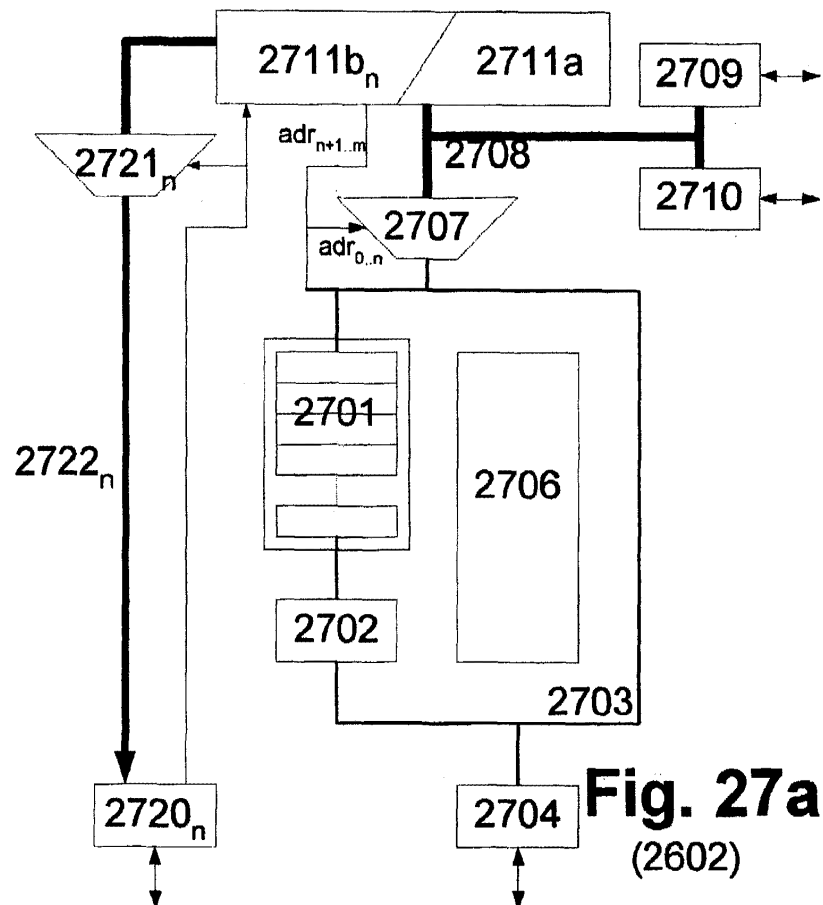


Fig. 26



**Fig. 27**  
(2602)



**Fig. 27a**  
(2602)

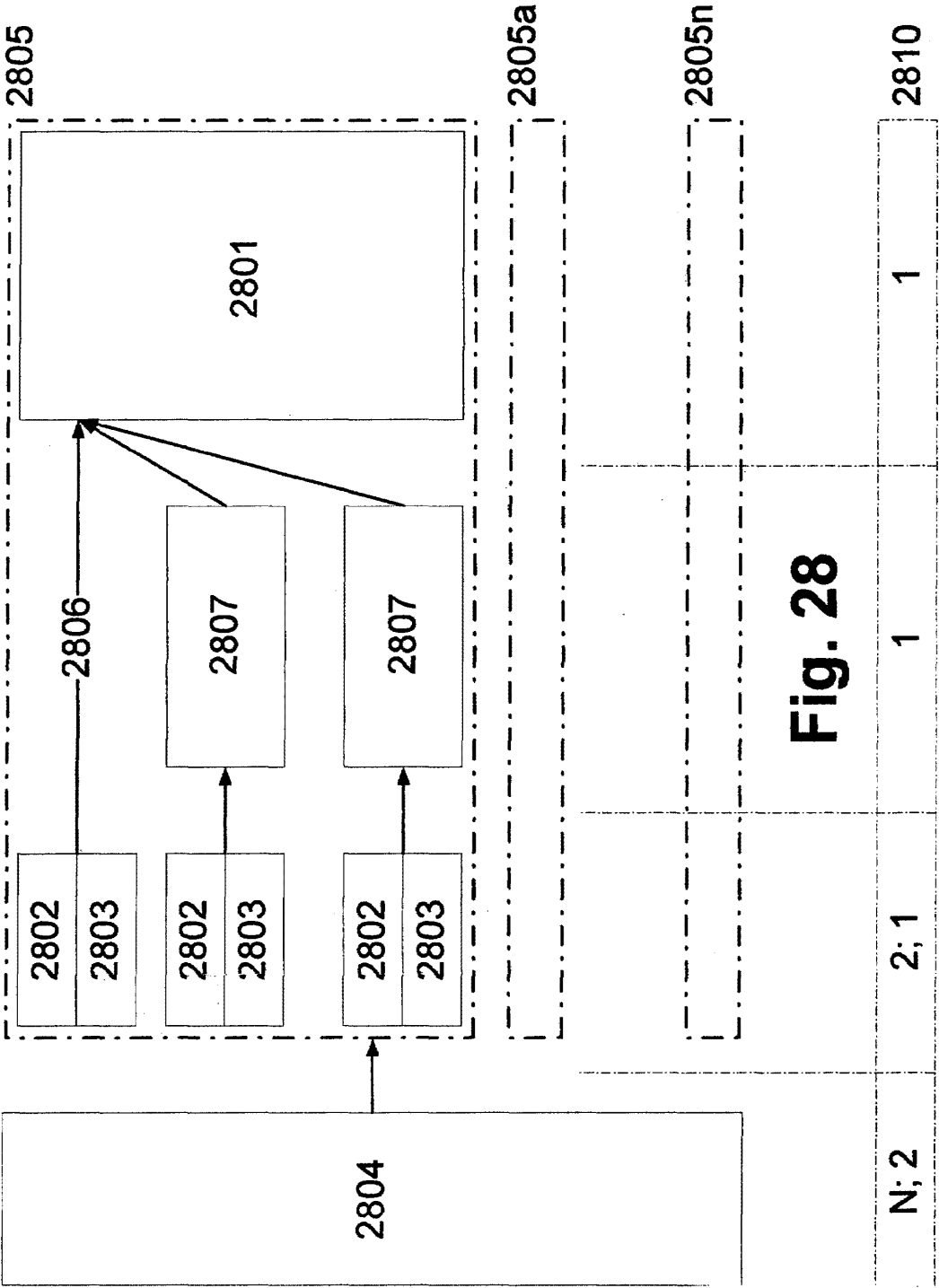
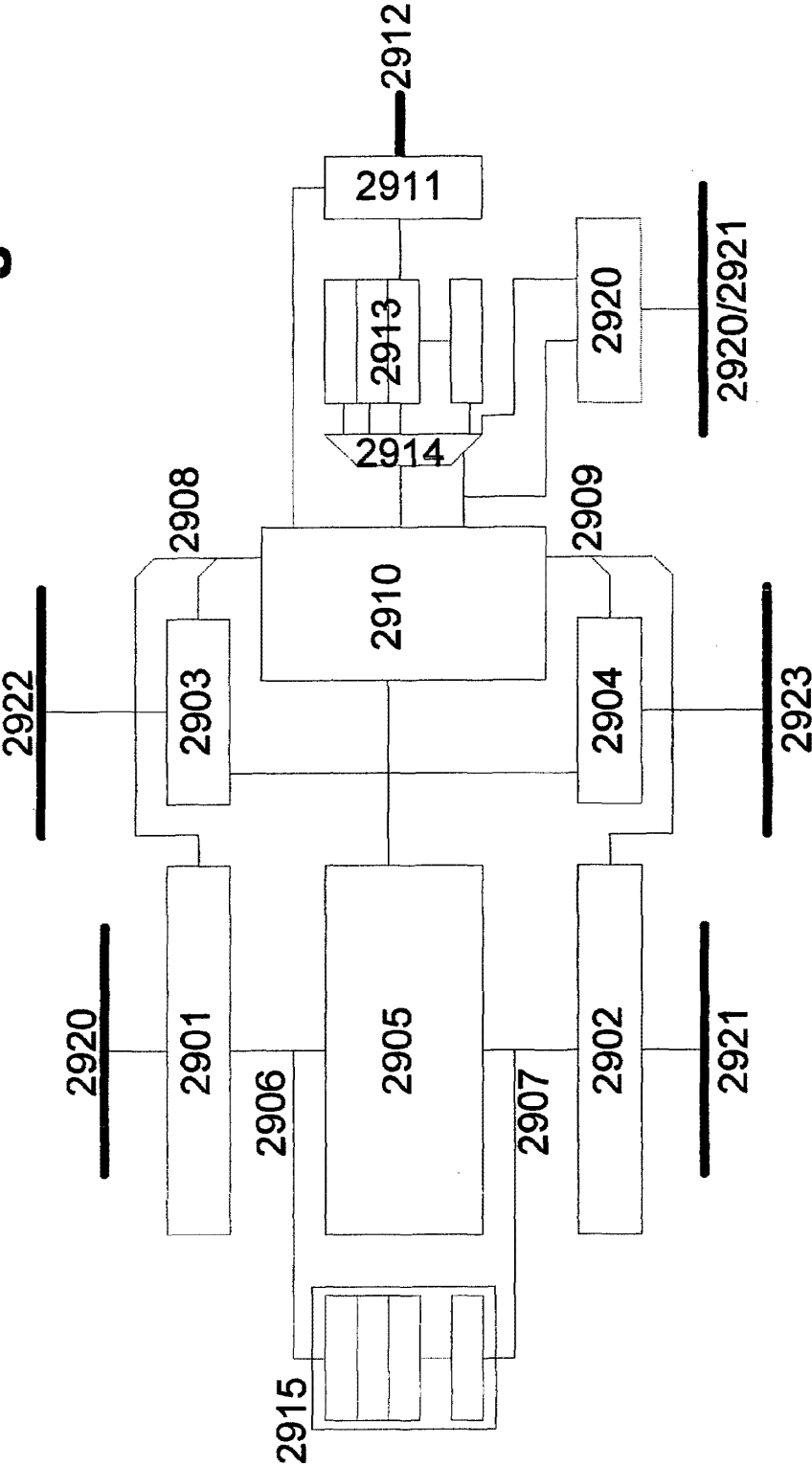
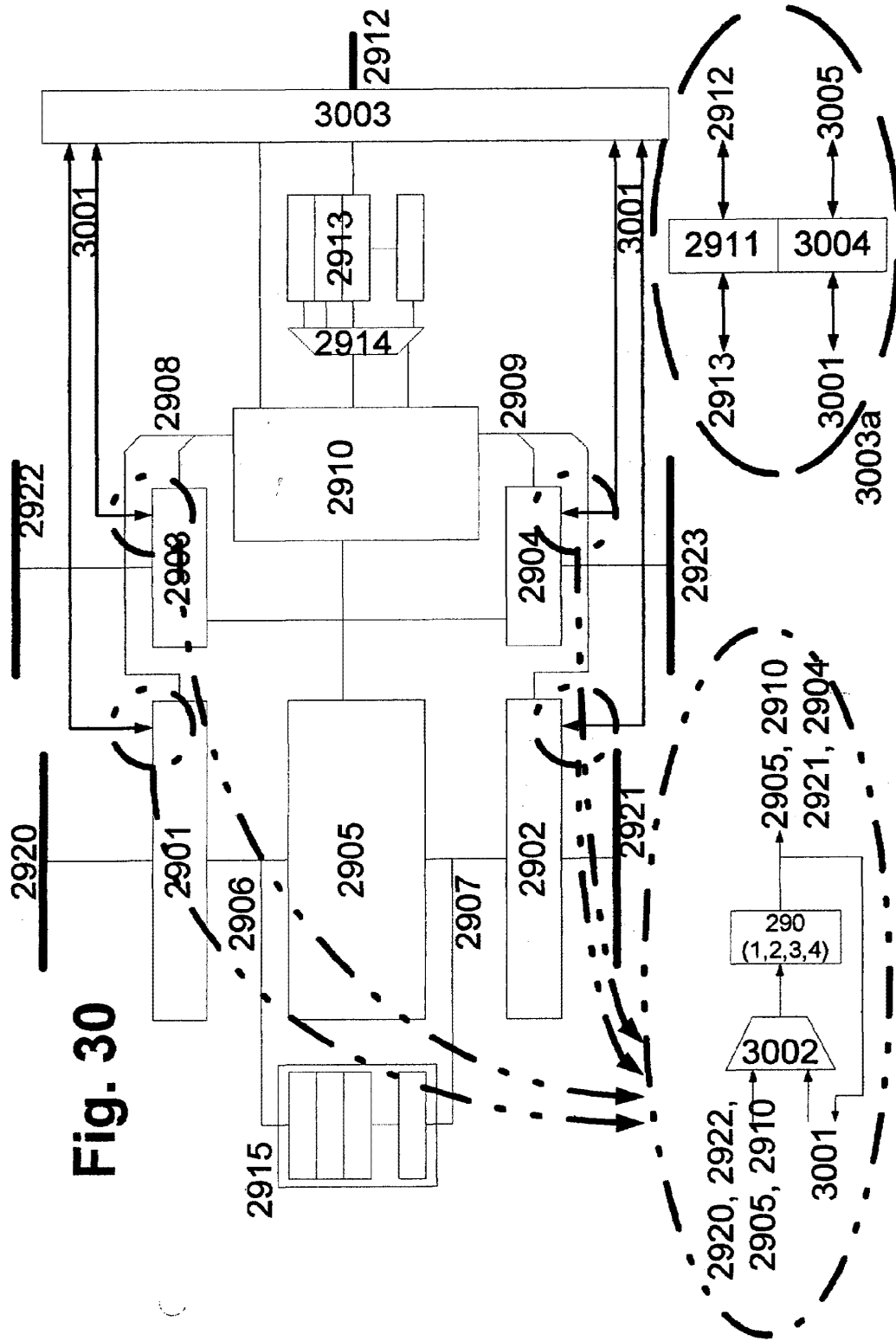


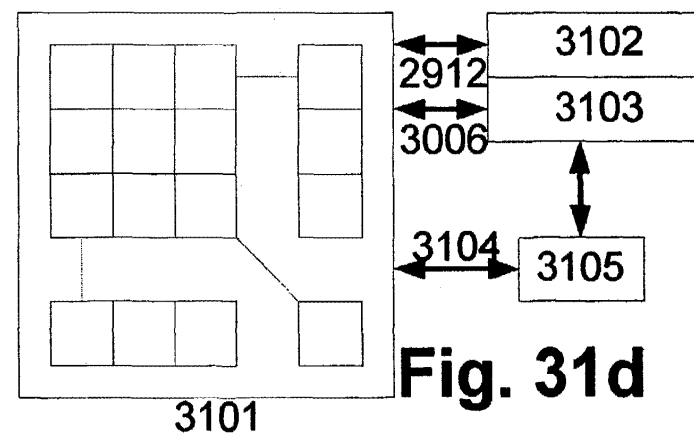
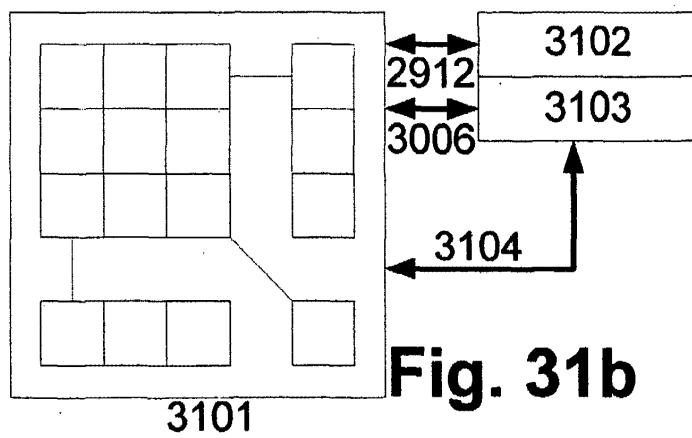
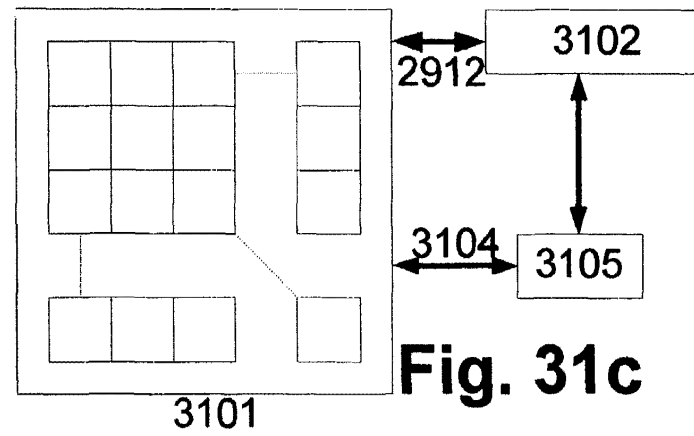
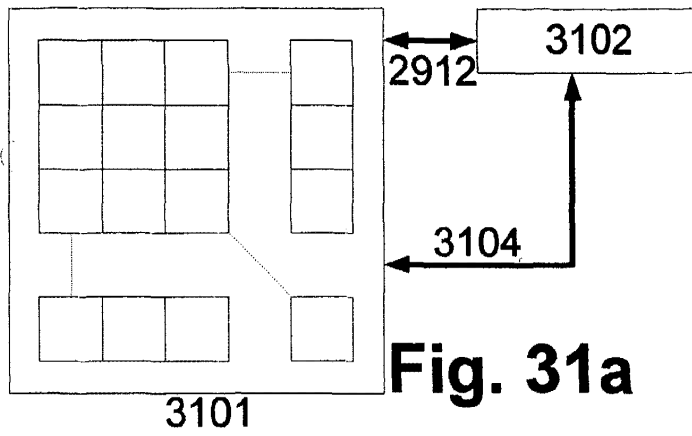
Fig. 29

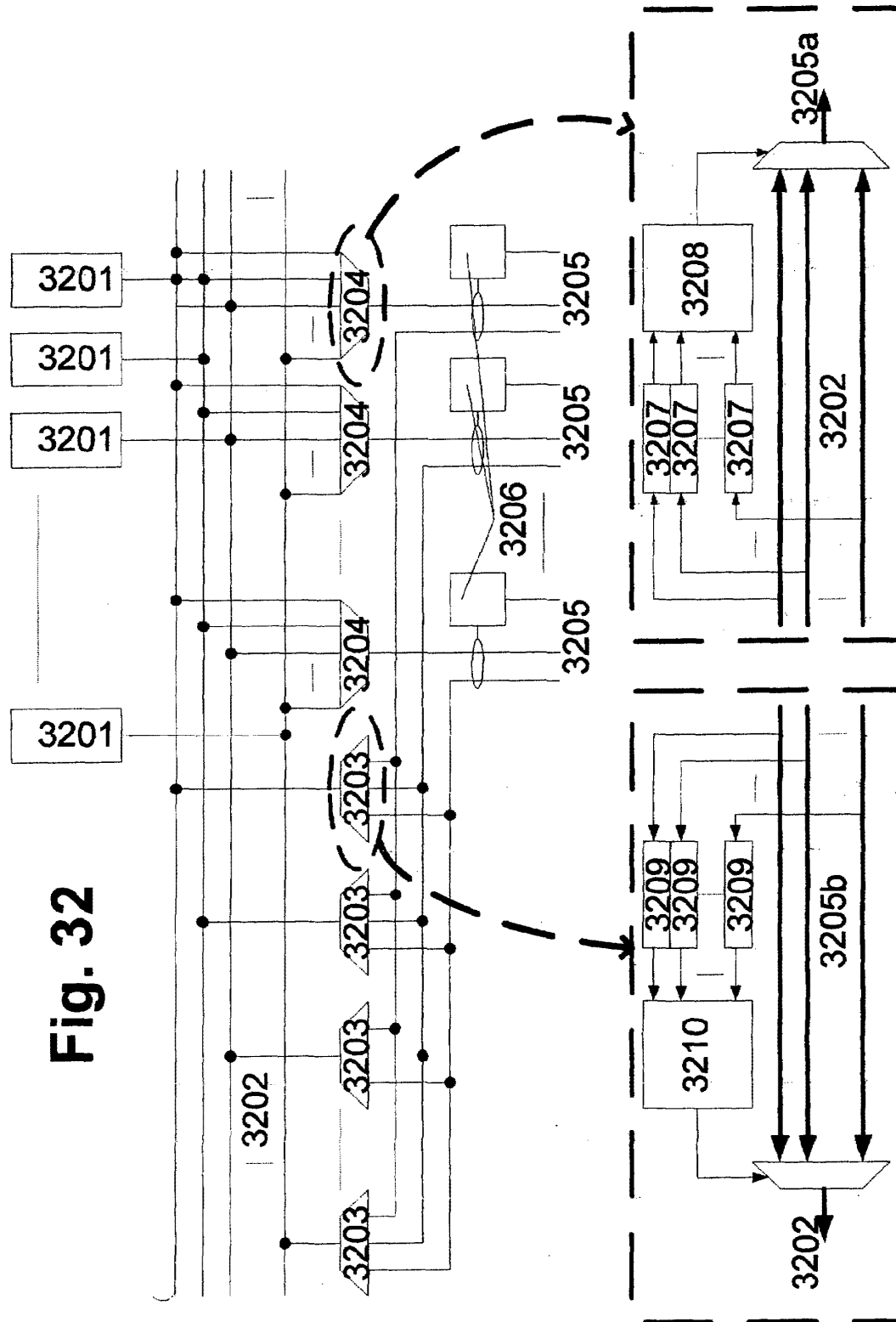


**Fig. 30**

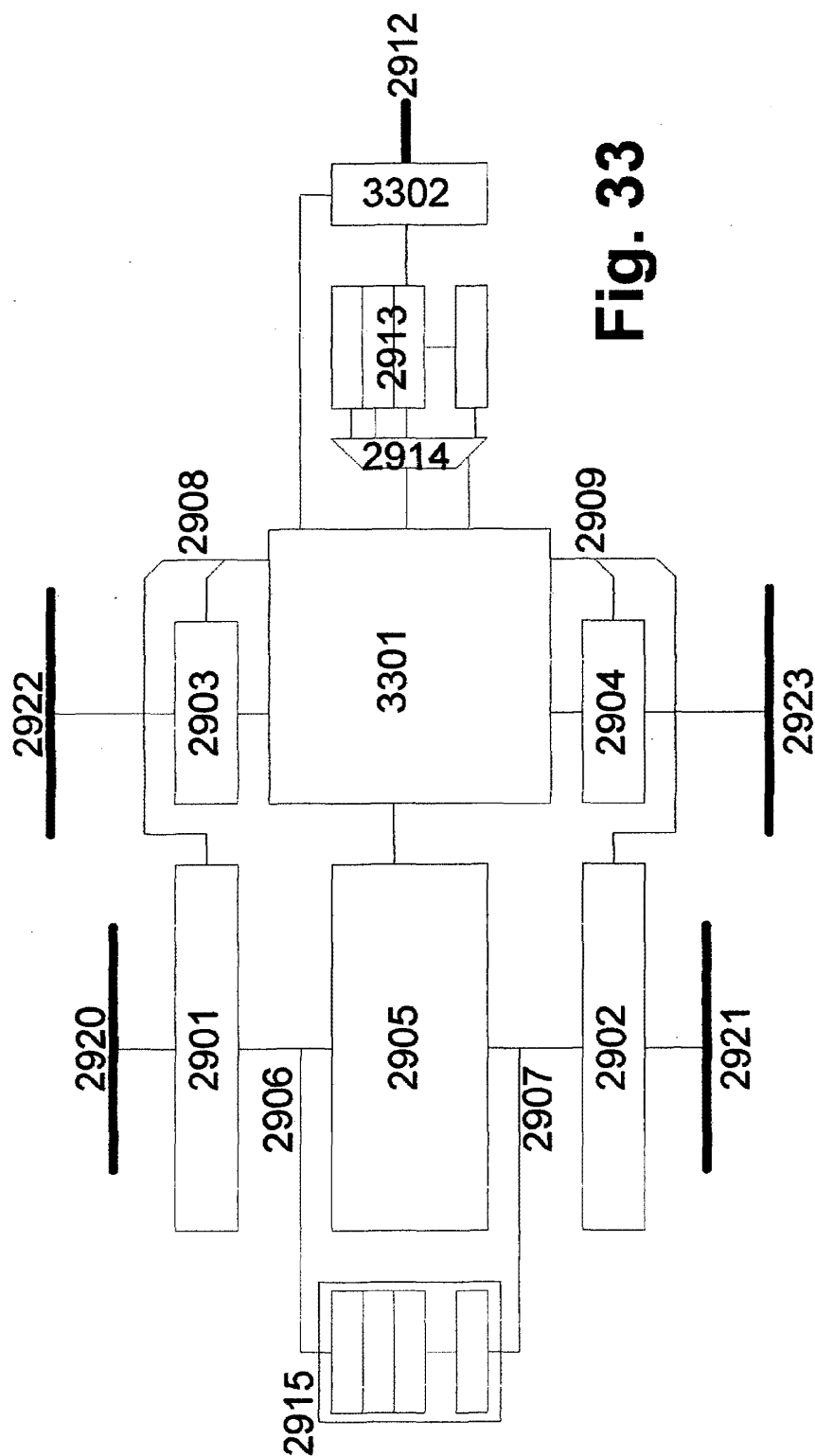


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**Fig. 33**

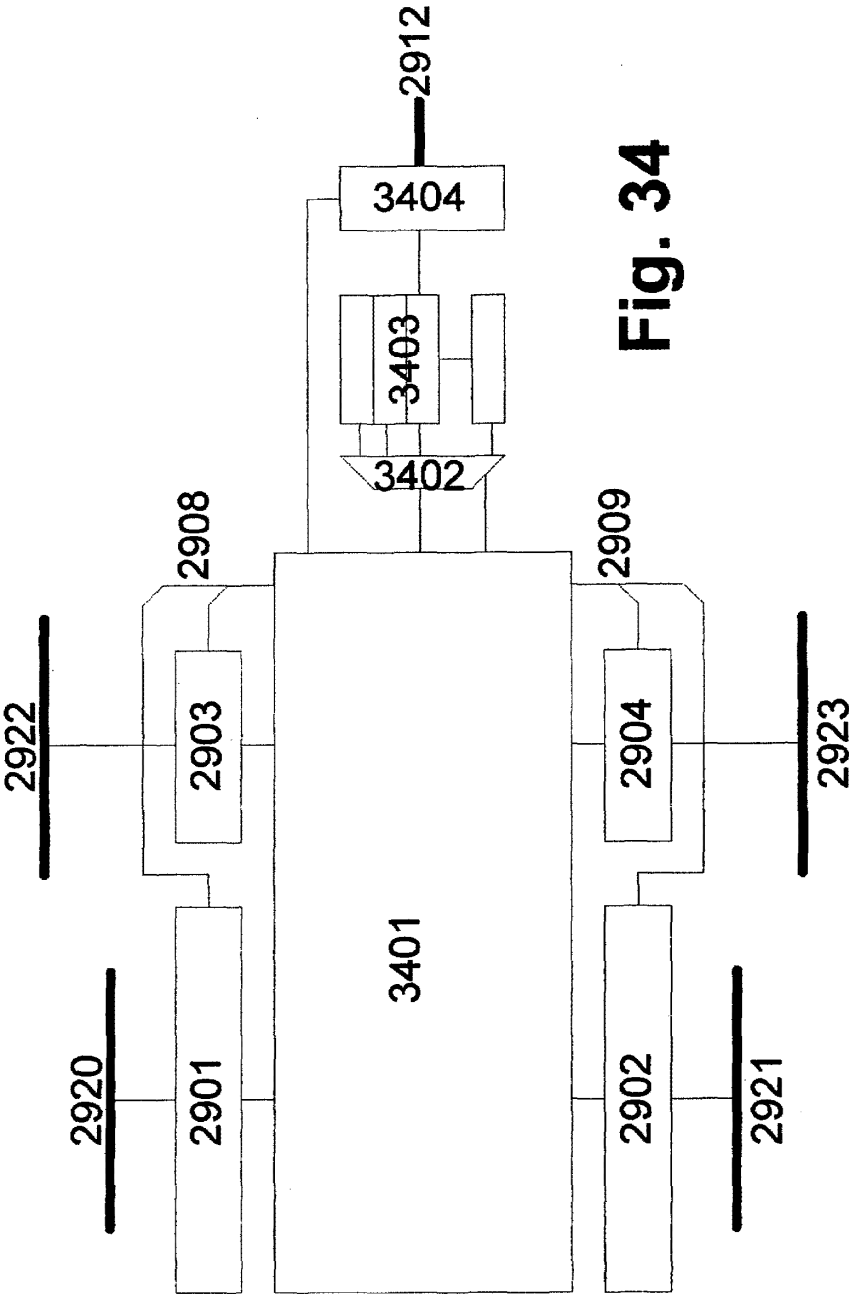


Fig. 34

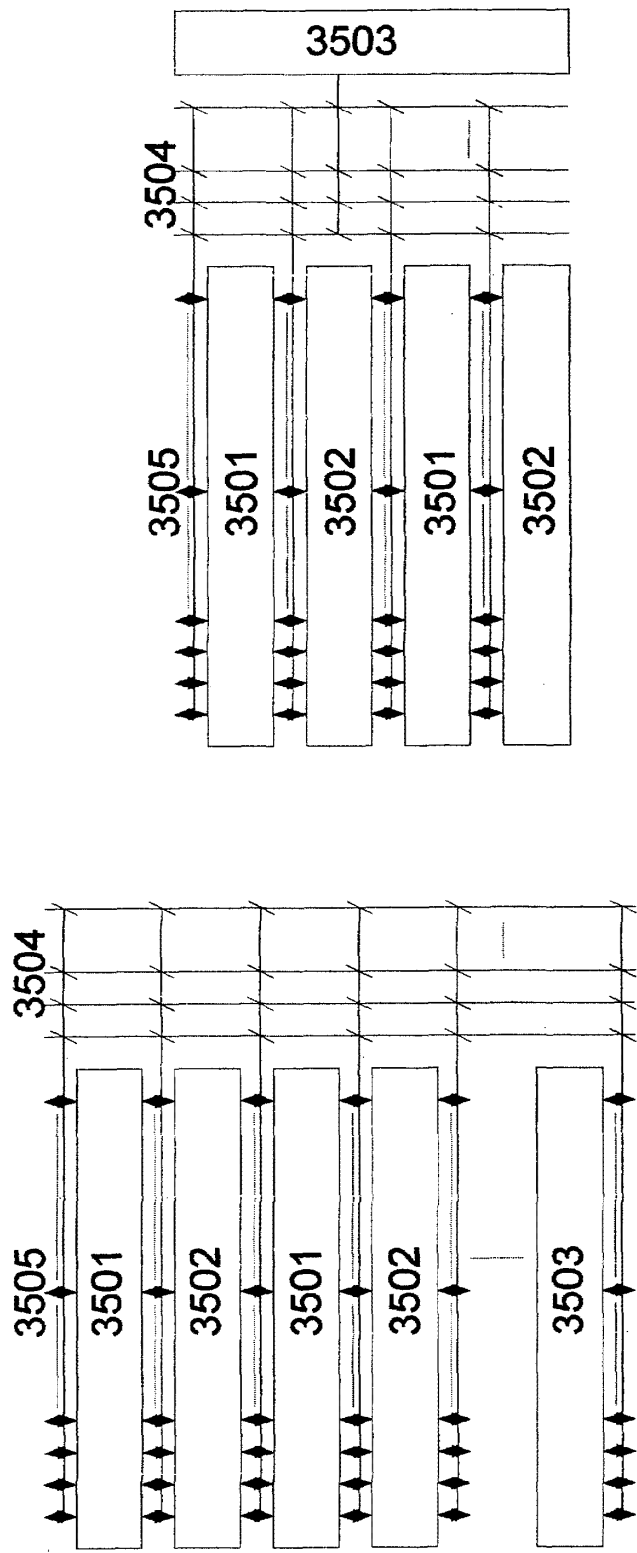
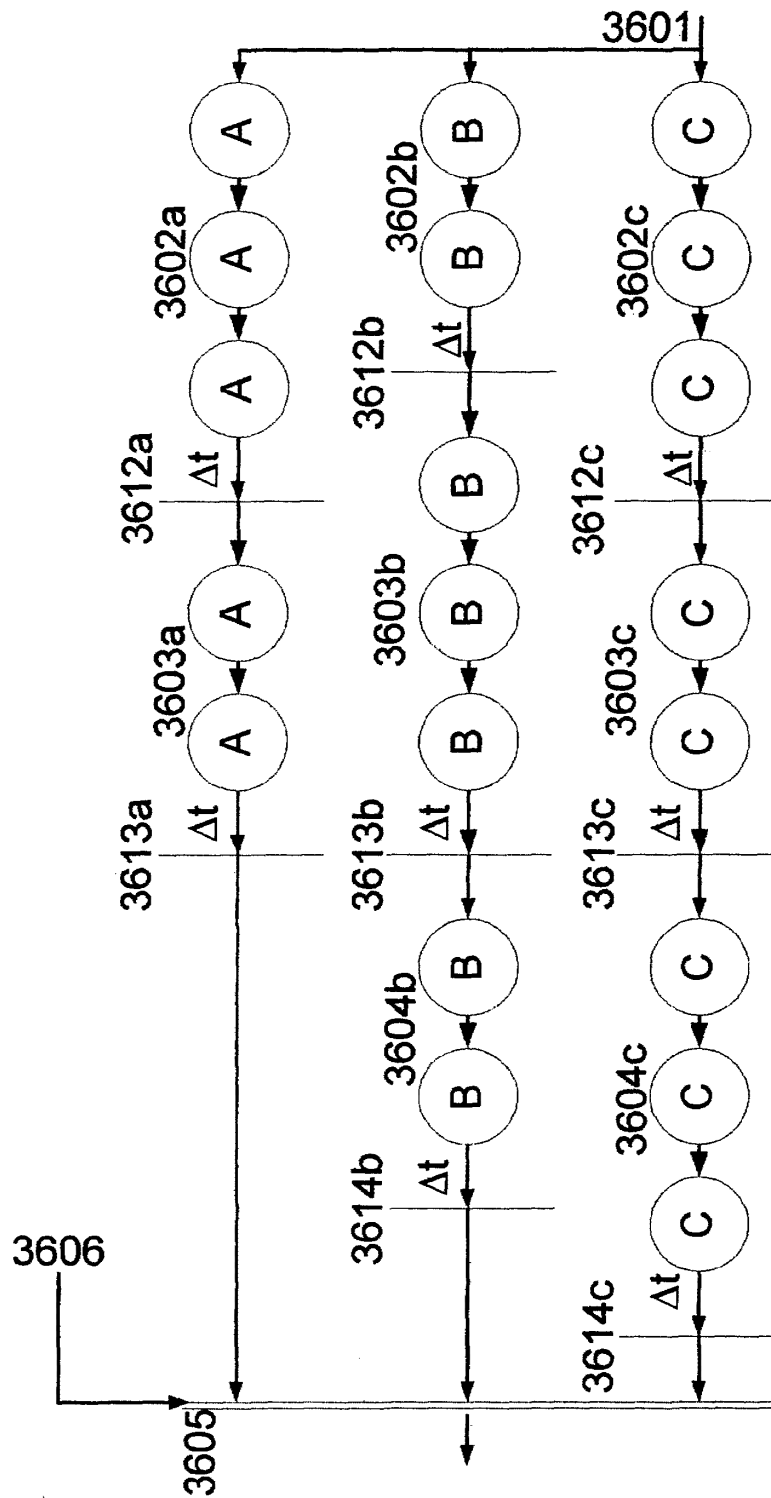


Fig. 35



**Fig. 36**

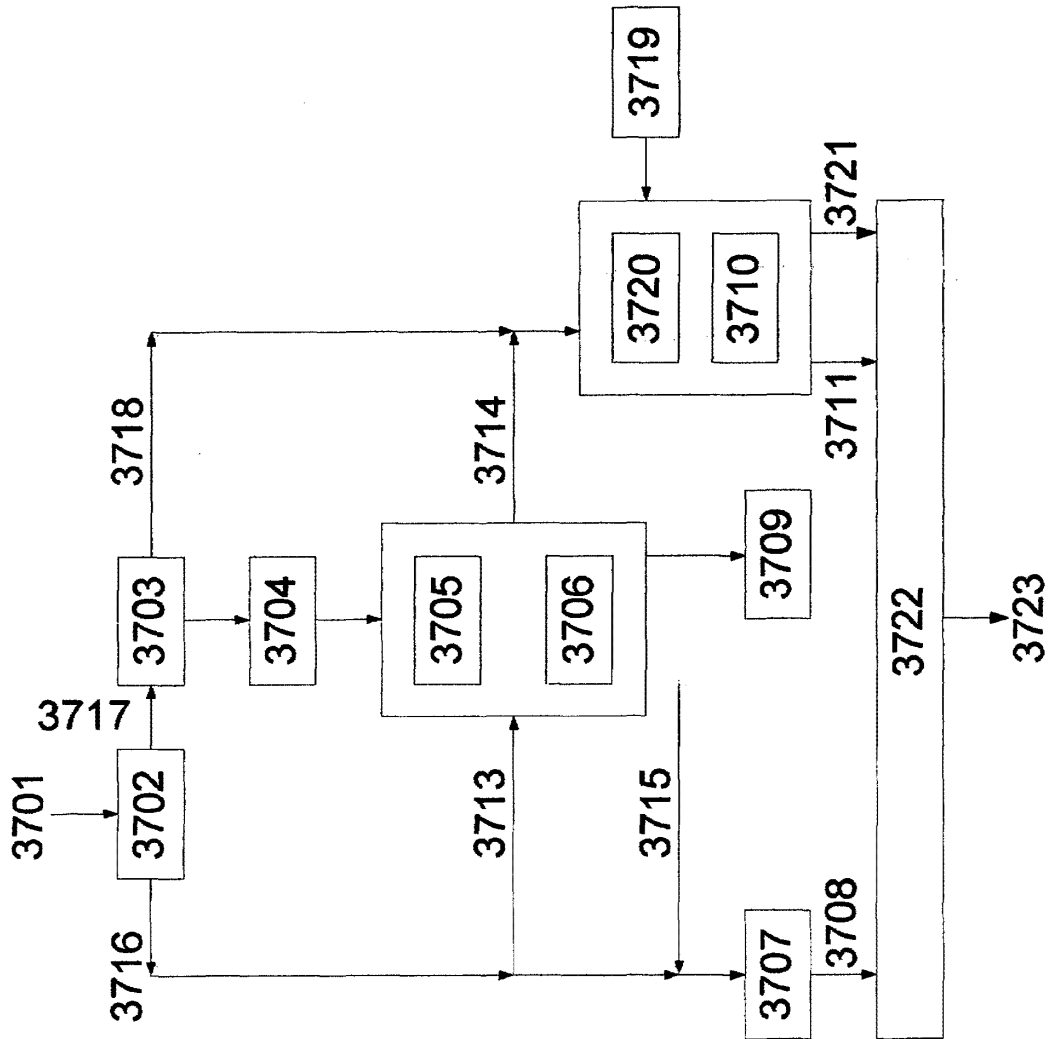
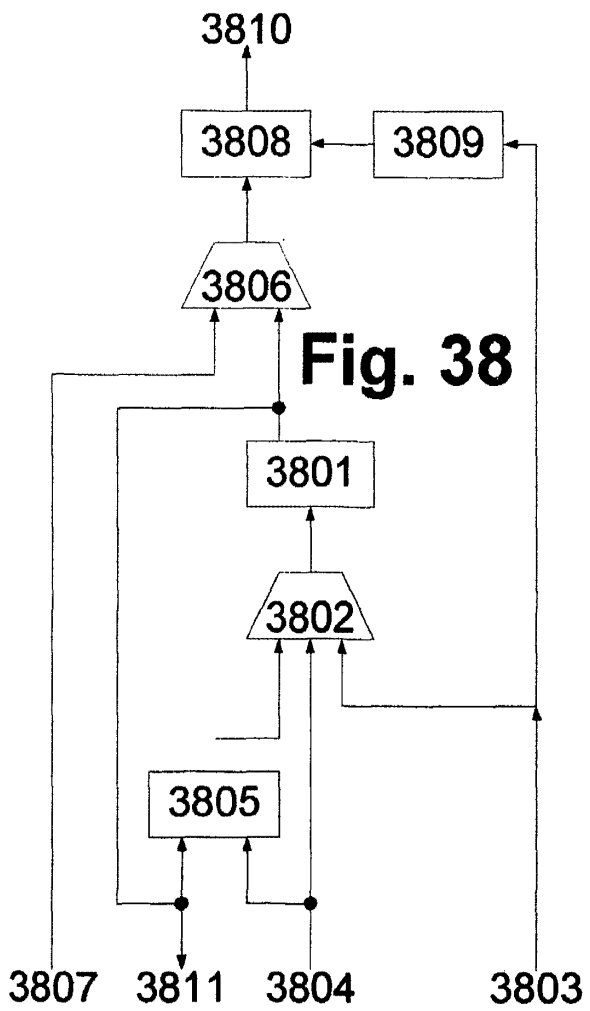
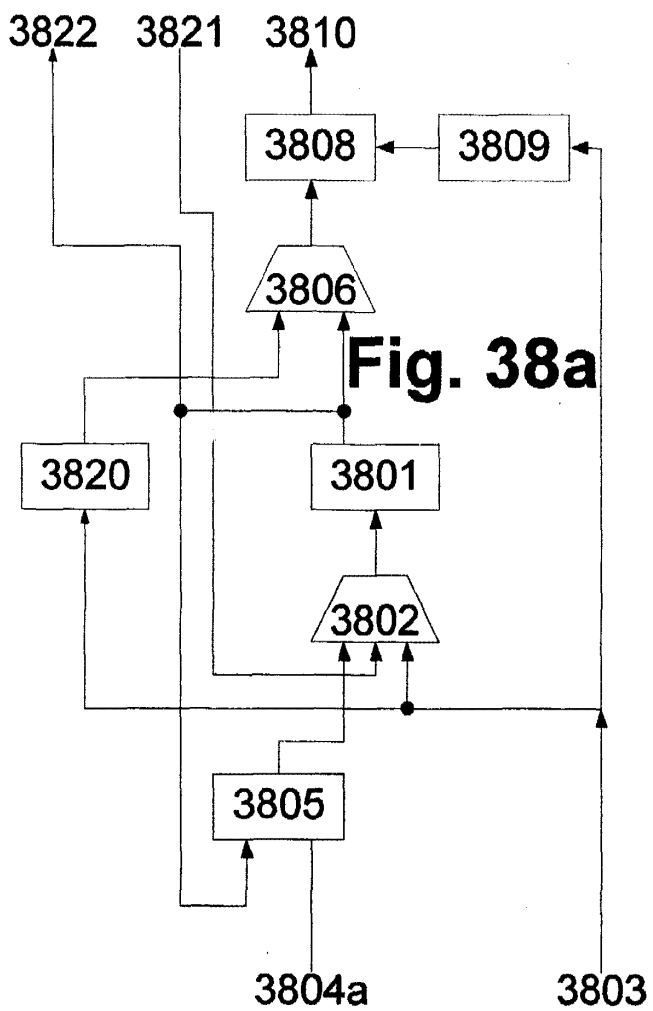
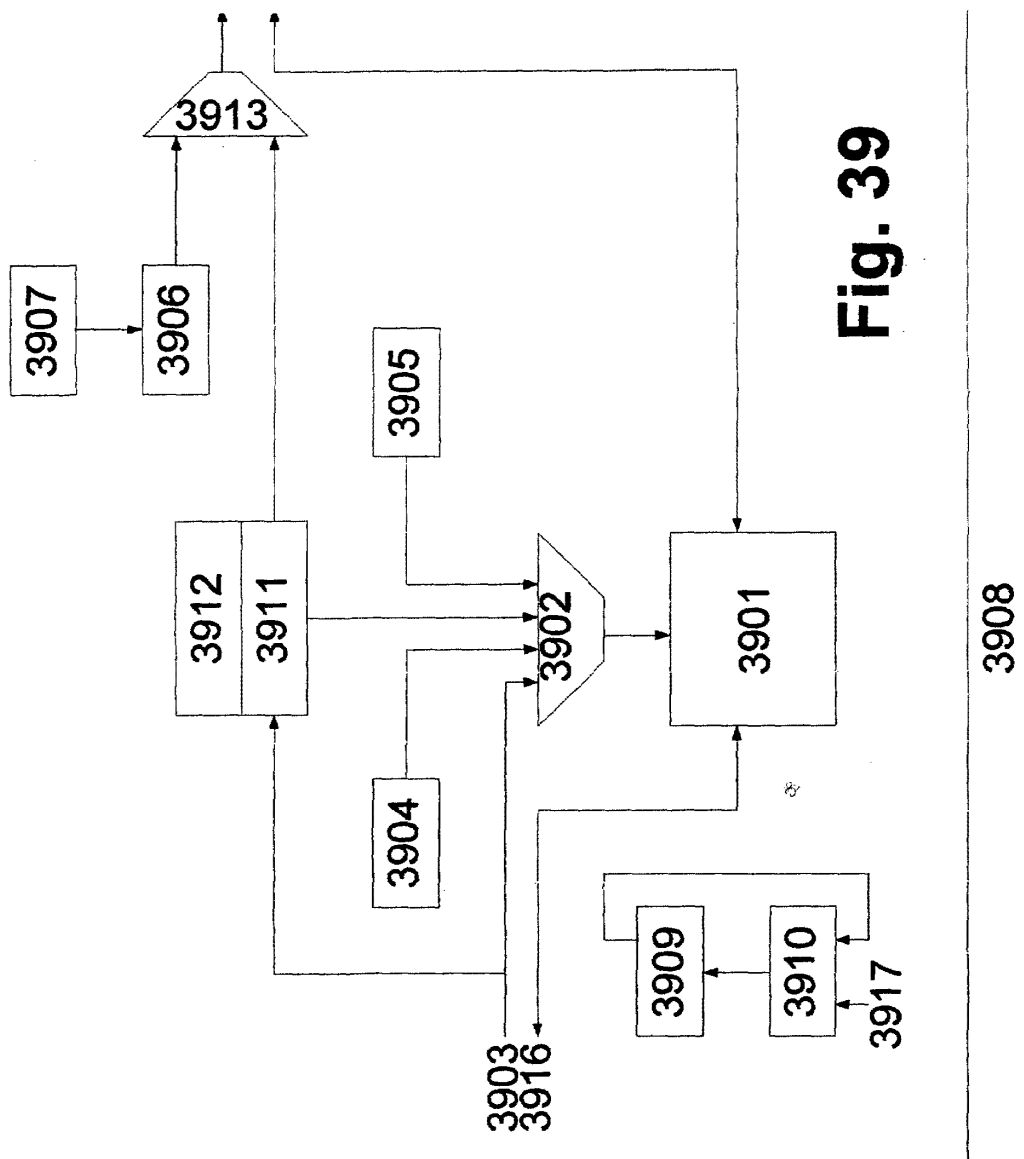


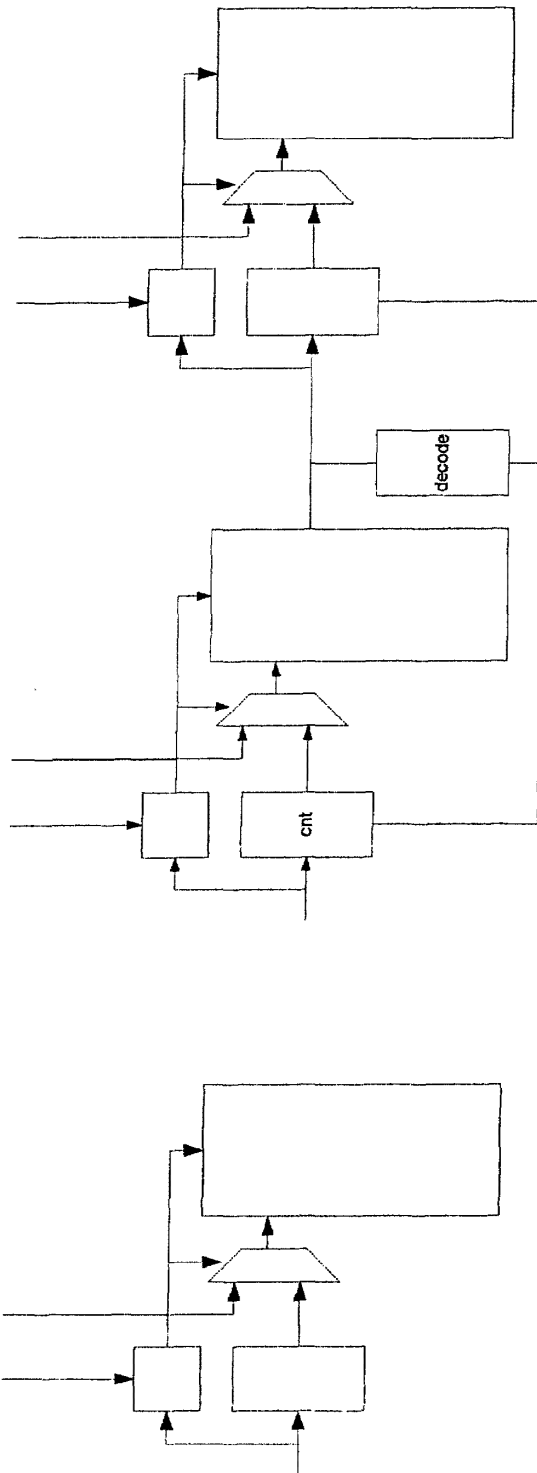
Fig. 37



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**Fig. 39**



**Fig. 40**

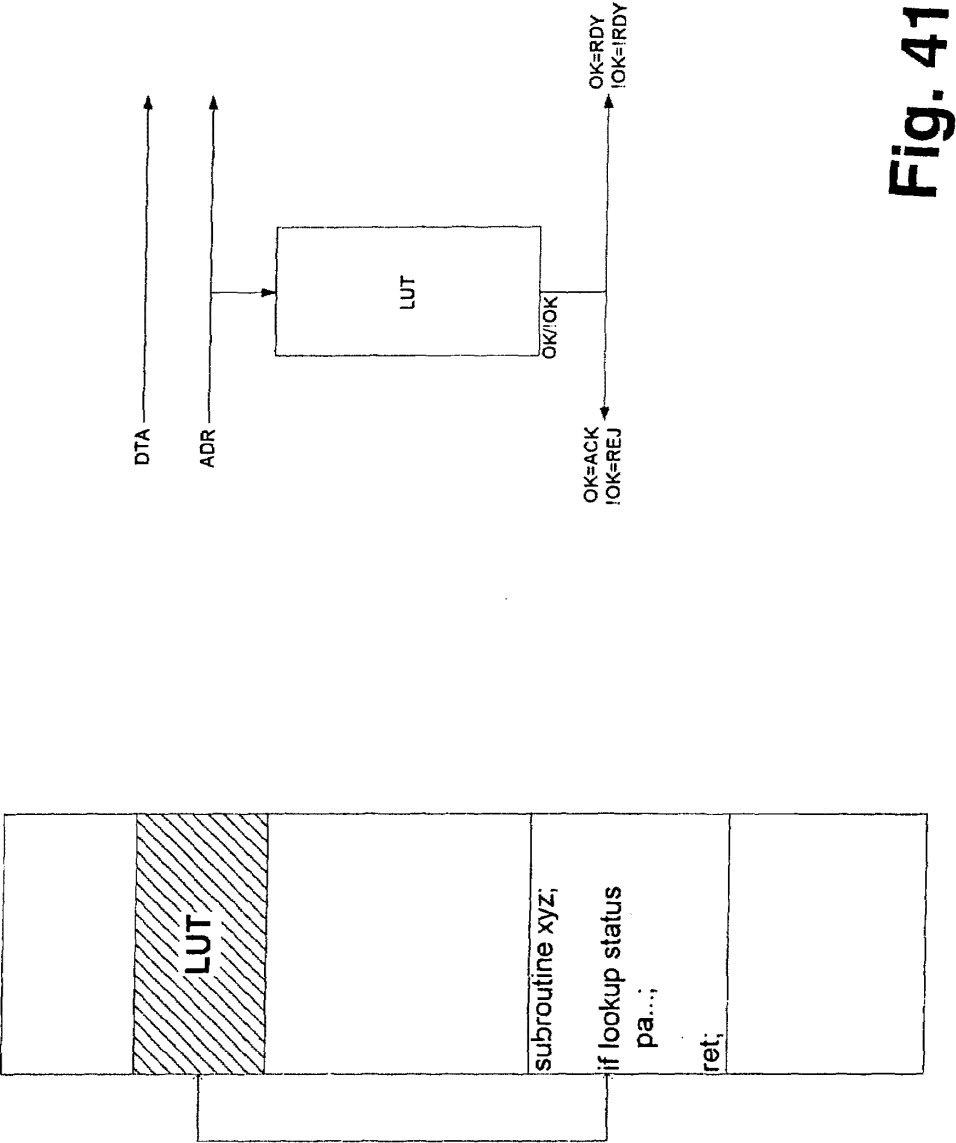
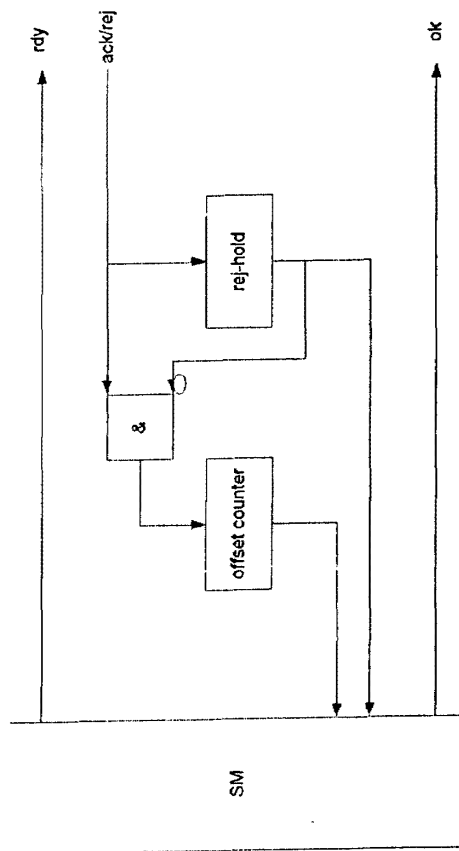


Fig. 41

**Fig. 42**



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**DE 000010028397 A1**

Registration Country: DE

Registration Number: 10028397

Registration date: 13.06.2000

Release Date: 20.12.2001

IPC version: 7

Main class: G06F 15/80

In addition to class: G06F 9/38

MCD secondary class: G06F 9/38 (2006.01, A)

MCD secondary class: G06F 15/78 (2006.01, A)

CPC: G06F 9/3885 (2013.01)

CPC: G06F 9/3897 (2013.01)

CPC: 15/7867 G06F (2013.01)

ECLA: G06F 9/38 T

ECLA: G06F 9/38 T8C2

ECLA: G06F 15/78 R

Inventor: Vorbach, Martin, 80689 München, DE

Applicant: PACT Informationstechnologie GmbH, 80807 München, DE

**[EN] Registration method in operating a reconfigurable unit, Involves Evaluating acknowledgment signal of configurable cells with time offset to Configuration**

**[DE] registration procedure**

**[EN]** The method Involves Evaluating the acknowledgment signal of the configurable cells with time offset to the configuration.

**[EN]** The invention relates to a method for operating a reconfigurable unit. It is proposed here that acknowledgment of the reconfigurable unit forming cells staggered to their configuration are evaluated.

**Page 1 --- (BI, AB)**

**Page 2 --- (DE)**

Object of the invention and application areas

**[0001]** RDY / ACK / REJ protocol and deadlock freedom.

**[0002]** The method known from PACT10 RDY / ACK / REJ protocol can not be pipelined over multiple registers.

**[0003]** However, to increase the fundamental frequency of a VPU multiple register stages are mandatory. This results in an unacceptable

Delay until the arrival of the acknowledgment of the configuration data for the CT.

**[0004]** There are shown basic solutions to this problem in the following two:

1. Lookup Tables

**[0005]** the state of the individual PAEs is managed in a CT or 2602 internal table. D. h. For each PAE existiert an entry indicating

whether the PAE can be unconfigured. a) Each PAE sends a status signal if her condition of "not reconfigurable" to the table on

"configurable" change. This status signal can be sent pipelined. b) It is also possible that a status signal for a group of PAEs is sent, indicating that the state of the entire group has changed. About a list, all PAEs to the group are selected and changed to the state for each of PAE in the table.

**[0006]** To check the status of a PAE

a) before executing the commands every pa contained therein PAE is checked by a lookup is performed in the table for each PAE. One

not configurable PAE leads to discontinuation of the PA command is not executed; or b) when sending the address of the target PAE through a pa-

Command queries the Lookuptabelle and accordingly generates an ACK or REJ (this approach corresponds to the conventional RDY / ACK /

REJ process).

2. Evaluating the ACK / REJ acknowledgment with Latency

**[0007]** The RDY signal is sent to the configuration data on several pipeline stages to the target PII. The configuration data not immediately stored in the appropriate configuration registers, but written in a temporary register. The PAE generates the ACK / REJ

Acknowledgment according to the internally managed Umkonfigurationsstatus (cf.. PACT10). The acknowledgment will also be sent back to the pipelined CT.

In the CT, a counter is incremented at each incoming ACK by one exists. In a separate register is saved if an REJ occurred has been.

**[0008]** After the pa-command has completed will be evaluated after a latency of n-cycles, the counter and the register. Is in the

Register noted a REJ, the PA command must be executed again. For this purpose, the count is either copied to the offset memory

(pabmm) or saved in the specified registry (pabmr). This value represents the configuration word, which was a REJ acknowledged and must be carried out again.

**[0009]** Terminates the PA command without occurrence of a REJ is sent to the participating PAEs a signal STORE. Subsequently, the

Configuration words from the temporary register written to the corresponding configuration register and the data operations started.

**[0010]** The clean? DEADLOCK, what PAEs that still abbekamen data after REJ due to the latency ?!

**[0011]** Do not use OK line, but to introduce a register in the corresponding PAEs.

Wave Reconfiguration

**[0012]** By a suitable hardware architecture (see. **Fig.** 10/11), it is possible to overlap a plurality of modules. Ie there are several modules.

at the same time pre-configured in the PAEs and it can be switched with a minimum of time between the configurations, so that from a

Crowd of several configurations per PAE configuration is activated always accurate.

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## Page 2

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**[0013]** It is essential that this in an amount of PAEs into a module A and B is pre-configured, part of the crowd with a portion of A and

a different part of the amount may be activated simultaneously with part B. The separation of the two parts is given exactly by the PAE,

in the Umschaltzustand between A and B occurs. This means that, starting from a certain time before all PAEs in which this time A was activated for execution B is activated and is in all other PAEs after that date still enabled on A. With increasing time is activated when an increasing number of PAEs B.

**[0014]** The switchover takes place on the basis of certain data, states that arise from the calculation of the data or due any other events that are generated, for example, by external or CT.

**[0015]** The causes directly after processing of a data packet can be switched to a different configuration. At the same time /

Alternatively, a signal (RECONFIG TRIGGER) are sent to the CT, which causes pre-charging of new configurations by the CT.

The preloading can dependent on another of the current data processing or carried out independent PAEs. By decoupling the active configuration

## Page 3 --- (DE)

the available for Unkonfiguration configurations (see **Fig.** 10/11) can also just working (active) PAEs, in particular the PAE, which produced the RECONFIG trigger, be loaded with new configurations. This allows for the data processing overlapping configuration.

**[0016]** In **Fig.** 13, the basic principle of wave reconfiguration is shown (WRC). This is based on a number of PAEs (PAE1-9),

through which the data passes pipeline similarly. It is expressly noted that WRC is not limited to pipelines and networking and grouping of the PAEs can take any form. The presentation, however, was chosen by a simple example to better To show understanding.

**[0017]** In **Fig.** 13a, a data packet passes in the PAE1. The PAE has 4 possible configurations (A, F, H, C), which by a suitable hardware (see **FIG.**

**Fig.** 10/11) are selectable. The configuration F (hatched) in in PAE1 activated for the current data packet.

[0018] In the next cycle, the data packet after PAE2 and a new data packet is running appears in PAE1. Also in PAE2 F is active. Together with the Data packet appears an event (& uarr; 1) at PAE1. The Ereignis caused by the arrival of any event from the outside in the PAE (z. B.

a status flag or trigger) or is generated within the PAE by the calculation performed.

Configuring H enabled simultaneously appears a new event; is [0019] In Figure 13c in PAE1 consequence of the occurrence (1 & uarr;). (& Uarr; 2)

the next cycle (Fig. 13d) causes the activation of configuration A.

. [0020] In Figure 13e applies (uarr; 3) at PAE1 that causes the overwriting of F and G (Fig 13f.). By the arrival of (uarr; 4) G is activated

(Fig. 13g). (uarr; 5) causes the loading of K instead of C and (uarr; 6) (Fig 13h, i.) loads and starts F instead of H (Figure 13j.).

[0021] FIGS. 13g \*) to 13j \*) clarifies that when passing through a wave reconfiguration not all PAEs according to the same pattern

have to work. As a PAE is configured by a wave reconfiguration, is principally dependent on their own configuration. Here is

be shown that PAE4 up PAE6 configured such that they react differently to the events than the other PAEs. For example, in Figure 13g \*) due to event & uarr;. 2 but not A H enabled (see Figure 13g)... The same applies to 13h \*). Due to event & uarr; 3 in FIG.

13i \*) not loaded G, but the configuration remains F and A remains activated. In Fig. 13j \*) is indicated at PAE7 that event & uarr; 3

again loading G will trigger. 4 Enabling F instead of configuration G (VG1 Figure 13j.); In PAE4, the event & uarr causes.

[0022] FIG. 13 is a wave of reconfigurations moved due to events by a number of PAEs, the 2- or can be designed in multi-dimensional.

[0023] It is not mandatory that a once held reconfiguration through the entire flow takes place away. For example, could the reconfiguration with the activation of A consequence of the occurrence (uarr; 2) only locally held in the PAEs1 to 3 and PAE7 while in

all other PAEs continue configuring H remains activated.

[0024] In other words:

a) It is possible that an event occurs only locally and therefore locally a Umaktivierung result has, b) a global event, may have

no effect on some PAEs; depending on the executed algorithm.

[0025] In the PAEs after (uarr; 2) continue to hold the H enabled, of course, the arrival of the event (uarr; 3) completely have other effects, (i) such as the activation of C instead of the load G, (ii) on the other hand could (uarr; 3) to this PAEs also do

have no influence.

The processor model

[0026] The graph shown in the following figures always have a graph node in the module, it being understood that several Modules can be mapped to a target device. That is, although all of the modules are independent of each other in time, is only at the

Modules performed reconfiguration, and / or a data memory is inserted, with a vertical line, and? T are marked. This Point is called Umkonfigurationszeitpunkt.

[0027] The Umkonfigurationszeitpunkt depends on the specific data or the states resulting from the processing of certain Data arise.

[0028] This means in summary:

1. Large modules can be partitioned at appropriate points and be broken down into small time-independent modules, the optimal fit into the array of PAEs. 2. In small modules that can be displayed together on a target block, is on the temporal independence waived. This configuration steps are saved and speeds up data processing. 3. The Umkonfigurationszeitpunkte be positioned according to the resources of the target blocks. This is an arbitrary scaling of the

Given graph length. 4. Modules can be configured superimposed. 5. The reconfiguration of modules is determined by the data itself or the

Result of the processing of the data is controlled. 6. The information generated by the modules data is stored and the time subsequent modules

read the data from this memory and save the results in turn in a memory or give the end result to the periphery out.

#### Page 4 --- (DE)

The state information of the processor model

[0029] To determine the states within a graph, the status register of the individual cells (PAEs) are in addition to a

Data bus **(0801)** existing, freely routable and Segmented status bus system **(0802)** all other arithmetic units provided (**Fig. 8b**).

This means that a cell (PAE X) can evaluate the status information of another cell (PAE Y) and accordingly processes the data.

To illustrate the difference to existing parallel computer systems, 8a of the prior art is shown in **Fig.** Here, a

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Quality.

Shown multiprocessor system, the processors are connected to one another via a common data bus **(0803)**. An explicit bus system

for the synchronous exchange of data and status does not exist.

**[0030]** In other words, the network provides the status signals **(0802)**, a free and selectively distributed a single status register

conventional processor (or several processors of an SMP computer). The status of each ALU (or each Processor) and in particular each of the status information is in each case the one or more ALUs (processors) available, the information the

need. In this case, no additional program or runtime communication occurs (apart from the Signallaufzeiten) to the information

between the ALUs (processors) exchange.

**[0031]** Finally, it should be noted that depending on the task of both the data flow graph, and the control flow according to the

The method described can be treated.

Virtual Machine Model

**[0032]** The basics of data processing with VPU-blocks are mainly in accordance with the preceding sections datenflußorientiert. In order to handle sequential programs with decent power, but it is necessary a sequential Computer model to have available. It is often not sufficiently the sequencer in the individual PAEs.

**[0033]** The architecture of VPUs allows but the basic construction of arbitrarily complex sequencers of individual PAEs.

**[0034]** The means:

1. It can be configured complex sequencer that exactly match the requirements of the algorithm. 2. The data flow can be obtained by

appropriate configuration, accurately represent the steps of the algorithm.

**[0035]** This can be implemented in VPUs a virtual machine, the particular needs of the sequential Algorithm corresponds.

**[0036]** The main advantage of the VPU architecture is that an algorithm can be divided by a compiler so that the extracted Datenflußteile

will be represented by an "optimal" data flow by an adapted data flow is configured and the sequential parts of the Algorithm can be represented by an "optimal" sequencer by an adapted sequencer is configured. It can simultaneously several sequencers and data flows can be accommodated on a VPU, solely dependent standing available from the resources.

**[0037]** Due to the large number of PAEs arise in operation within a VPU very many local states. When Task Switch or Subroutine calls (interrupts) must these states are saved (cf.. PUSH / POP with standard processors). However, this is due to

the amount of states does not make sense possible.

Must **[0038]** To the states to reduce to a manageable amount between two types of states can be distinguished:

1. status information of the machine model (MACHINE-STATE). This state information only within the execution of a Modules certain valid and also be used locally in the sequencers and Datenflußeinheiten this particular module. D. h. This MACHINE-States represent the states that hides in processors according to the prior art occurring within the hardware, implicitly

are in the commands and the processing steps and after an instruction do not include additional information for subsequent commands.

Such conditions do not need to be backed up. Condition for this is that interrupts only after complete execution of all currently active

Modules are performed. Standing interrupts for performance, no new modules are loaded, but only active processed; also no new operand longer be the active modules, the extent permitted by the algorithm supplied. This is a module to an atomic uninterruptible unit, comparable to an instruction of a processor according to the prior art. 2. states of Data processing (DATA-STATE). The data-related states need after the occurrence of an interrupt in accordance with processor models

be secured to the prior art and written into the memory. These are certain necessary registers and flags, or - in accordance with the terms of the VPU technology - Trigger.

**[0039]** In the DATA states, the handling can be further simplified, depending on the algorithm. Two basic strategies are in Below Näher explained:

1. rotating with the state information

**[0040]** All relevant and required at a later date state information from a

#### **Page 5 --- (DE)**

Transfer module to the next, as it is implemented by default often in pipelines. The state information is then combined with the data implicitly stored in a memory, so that the states are available in a retrieval of data at the same time. An explicit handling

the state information by PUSH and POP deleted by what the in a substantial acceleration depending on the algorithm one hand

Processing and on the other hand leads to a simplified programming.

**[0041]** The Zustandsinformaton can be saved either to either the respective data packet, or only in the event of an interrupt

be secured and clearly marked.

2. Secure the reentry address

**[0042]** In the processing of large amounts of data that are stored in a memory, it may be useful to address at least one of the operands to conduct with the data package together through the PAEs of the currently processed data packet.

In this case, the address is not

but is modified in writing the data packet in a RAM as a pointer to the last processed operands available.

**[0043]** This pointer can be stored optionally either with the respective data packet, or backed up only in case of interrupts and

are specially marked. Particularly if all pointers to the operands by an address (or a group of addresses) can be calculated is to secure meaningful only an address (or a group of addresses).

"ULIW" - "UCISC" model

**[0044]** (very ähnlichen a processor according to the prior art) In order to understand this model is an extension of the approach

architecture required by VPUs. Here, the virtual machine is used as a basis model.

**[0045]** The array of PAEs (PA) is considered to be configurable in their architecture computing unit. The / CT (s) provide a charging unit (LOAD

UNIT) for opcodes represent. The IOAG (s) take the bus interface and / or the register set.

**[0046]** This arrangement enables two basic modes of operation, which are mixed in the operation used:

1. A group of PAEs (which may also be a PAE) is configured to run a complex command or command sequence and then be the data related to the command data (which may also be a single data word) is processed. Then this group is reconfigured,

for execution of the next instruction. The size and arrangement of the group may change. According to the already discussed

Partitioning technologies it is for the compiler to create the best possible groups. The CT groups are on as commands

"Loading" the block, characterized the Verfahren with the known VLIW is similar, except that significantly more processing plants are managed

And the cross-linking structure between the arithmetic units can also be covered by the instruction word (Ultra Large Instruction Word =

"ULIW"). This is a very high instruction level parallelism (ILP) can be achieved. (see also **Fig. 27**). An instruction word corresponds to

a module. Several modules can be processed simultaneously, as long as it allows the dependence of data and sufficient resources to

are the building block free. As with VLIW commands immediately the next instruction word is loaded usually after executing the instruction word.

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Quality.

The temporal optimization, the next instruction word it is already possible to summon during execution (see. **Fig. 10**). For more

possible next Instruktionswörten several can be summoned and before execution is z. B. the correct by a trigger signal

Instruction word is selected. (see **Fig. 4a B1 / B2**, **Fig. 15 ID C / ID K**, **Fig. 36 A / B / C**) 2. A group of PAEs (which may also be a passport) is configured to carry out a frequently used command string. The data, which may be a single data word also be found here, if required, the

Fed group and received by the Group. This group remains a plurality of clocks without reconfiguration. Is comparable This arrangement with a special calculating unit in a processor according to the prior art (eg. B. MMX), which provided for special tasks

and is used only when necessary. Through this approach, special commands can be generated according to the CISC principle, with the advantage that

these commands can be created for specific applications (Ultra-CISC = "UCISC").

Expansion of the RDY / ACK protocol (cf.. PACT02)

**[0047]** In PACT02 describes a RDY / ACK-standard protocol that the essential requirements in accordance with the synchronization of DE

44 16 881 describes in terms of a typical Datenflußapplikation. Disadvantage of the protocol is that only data is sent and the receiving

can be confirmed. The opposite case, data is requested by, and sending is confirmed (hereinafter referred REQ / ACK, Although electrically with the same two-wire protocol solvable, but semantically not detected. This is especially true if REQ / ACK and RDY / ACK operate mixed.

**[0048]** Therefore, the clear distinction of the protocols will be introduced:

RDY: data from the sender to the recipient ready

REQ: data is requested by the receiver from the sender

ACK: General confirmation of receipt or delivery made

(Principle could also be distinguished between ACK for a RDY and an ACK for a REQ, however, is in the logs of the semantics

ACKs usually implicitly).

#### **Page 6 --- (DE)**

##### Memory model

**[0049]** In VPU's can be integrated storage (one or more) that are addressed similar to a PAE. An hereinafter Described memory model that simultaneously represents an interface to external peripherals and / or external memory:

**[0050]** A VPU-internal memory with PAE similar bus functions can represent different storage modes:

1. Standard memory (Random Access) 2 cache (as an extension of the standard memory) 3. Lookup table 4. 5. FIFO LIFO (stack)

**[0051]** The memory is assigned a controllable interface that memory areas word alternatively or in blocks writes or reads.

**[0052]** This results in the following uses:

1. Separation of data streams (FIFO) 2. Fast access to selected storage areas of an external memory, what a cache Similar

Function is (Standard memory lookup table) 3. Stack with variable depth (LIFO)

**[0053]** In this case, the interface can be used, but it is not absolutely necessary if the data z. B. only locally in the VPU be used and sufficient storage space of an internal memory.

##### Stack Model

**[0054]** By using the REQ / ACK protocol, and the internal memory in the LIFO stack mode, a simple processor can set up become. In this case the temporary data of PAEs are written onto the stack and loaded on demand from the stack. The necessary

Compiler technologies are well known. By variable stack depth with by a data exchange of internal memory a external storage is reached, the stack can be arbitrarily large.

##### Battery model

**[0055]** Each PAE may represent a computing unit after Akkumulatorprinzip. As it is known from PACT02 possible the output register

feed back to the input of the PAE. Characterized an accumulator is produced according to the prior art. In connection with the sequencer of FIG.

11 can be built simple accumulator processors.

##### Register Model

**[0056]** By using the REQ / ACK protocol and the internal memory in the default storage mode, a simple register-processor being build up. The register addresses are generated by a group of PAEs, while another group of PAEs processing the data takes.

##### Architecture of Memory

**[0057]** The memory has two interface. A first which connects the memory with the array and a second, the memory with an IO

Unit connects. To improve the access time of the memory should be designed as a dual-ported RAM, which write and read accesses can be carried out independently.

**[0058]** The first interface is common PAE Interface (PAEI), which ensures access to the bus system of the array, as well as synchronization

and trigger processing ensures. Triggers can be used, and view or actions in the different states of the memory

To enforce memory, for example,

1. Empty / Full: When used as a FIFO is the FIFO state "full", "almost-full", "empty", "almost-empty"; 2. Stack overrun / underrun: When used as a

Stack overflow and underflow of the stack are signaled; 3. Cache hit / miss: Cached mode is displayed, if an address in the cache found

has been; 4. Cache flush: By a trigger writing of the cache will be enforced in the external RAM.

**[0059]** is assigned to the PII interface configurable state machine that controls the various operating modes. Of the State machine is assigned to the addresses in the FIFO and LIFO mode to generate a counter. The addresses are through a multiplexer

out to the memory so that additionally addresses that are generated in the array can be performed on the memory.

**[0060]** The second interface is used to connect an IO unit (IOI). The IO unit is configurable as a controller with an external Interface designed. The controller reads or writes words or blocks data in or out of the memory. The data with the IO unit replaced. Furthermore, the controller by means of an additional TAG memory supports multiple cache functions.

#### **Page 7 --- (DE)**

**[0061]** IOI and PAEI are synchronized with each other, so that no collision occurs between the two interface. The Synchronisation is depending on the operating mode

different, for example, while the standard memory or Stack mode only either the IOI or the PAEI on the whole

Can access memory in FIFO mode synchronization is line by line, ie while IOI accesses a line x, the PAEI may in any other

Line access equal to x at the same time.

**[0062]** The IO unit is configured according to the peripheral requirements, for example:

#### **Page 5**

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Quality.

1. SDRAM controller 2. RDRAM controller 3. DSP bus controller 4. PCI controller 5. Serial controller (z. B. NGIO) 6.

Special Purpose Controller

(SCSI, Ethernet, USB, etc.)

**[0063]** A VPU may have any storage elements with any IO units. It may have different IO units on a VPU be implemented.

Funktionsweise 1. Standardspeicher 1.1 internally / locally

**[0064]** About the PAEI be data and addresses exchanged with memory. The addressable memory size is limited by the memory size limited.

1.2 External / memory mapped window

**[0065]** About the PAEI be data and addresses exchanged with the memory. In controller of IOI is a base address in the external memory

indicated. The controller reads in blocks data from the external memory address and writes it in the memory, the internal and external

Addresses each incremented (or decremented) are; until all internal memory has been transferred or a preset

Limit has been reached. The array works with the local data until it is written back into the external memory by the controller. That

Writing is analogous to that described read operation.

**[0066]** The reading and writing by the controller can

a) be initiated by trigger or b). by an access of the array to a not locally stored address Accesses the array on a

Such an address to the internal memory is written into the first external and thereafter the memory block to the required address

reloaded.

**[0067]** This mode is particularly interesting for the implementation of a register file for a processor register. By a trigger can be realized in this case, the push / pop of the register file to the external memory for a task switch or a context switch become.

1.3 External / lookup table

**[0068]** The lookup table function is a simplification of 1.2. The data is either once or several times through a CT Call read or a trigger from the external RAM to the internal. The array reads data from the internal memory, but does not write data into the internal memory. The base address in the external memory is saved in the controller through either the CT or the array and can at runtime to be changed. The loading from the external memory is triggered from either the CT or by a trigger from the array and can also happen at runtime.

#### 1.4 External / cached

**[0069]** In this mode, the array selectively engages to the memory. The memory operates as a cache memory for the external memory according to the prior art. By a trigger from the array or by the CT of clearing the cache (ie the full writing of Caches are caused in the external memory).

#### 2. FIFO

**[0070]** The FIFO mode is usually used when the data streams are guided externally of the VPU. Then the FIFO serves as Decoupling between the external data processing and the VPU-internal data processing, so that by either external to the FIFO is written and read by the VPU or reversed. The states of FIFOs are triggers for array and possibly even after external signals. The FIFO is implemented even after the state of the art with different write and read pointers.

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#### 3. Stack / intern

**[0071]** An address register An internal stack is built up. With each write access to the memory array by the register per by Mode (a) incremented decremented (b). In the case of read accesses from the array of the registers is reversed (a) is decremented and incremented (b). The register provides the required address available for each access. The stack is limited by the amount of memory. Error (overflow / Underflow) are indicated by trigger.

#### 4. Stack / external

**[0072]** If the internal memory is too small to build a stack, it can be outsourced to external memory. For this purpose is in Controller an address counter for the external stack address. If a certain amount of entries exceeded the internal stack is blockwise a number of entries written in the external stack. The stack is therefore written from the end from the oldest entry from externally, where a lot of the latest entries will not be written to an external number, but remains internally. The external address counter (ERC) is line by line modified.

**[0073]** the remaining stack content after place in the internal stack has been created must be moved to the top of stack, internal Stack address is adjusted accordingly.

**[0074]** A more efficient option is the laying out of the stack as a ring memory (cf.. PACT04). An internal address counter by adding modified or removing stack entries. Once the internal address counter (IAC) exceeds the upper end of the memory, to point to the lowest address. Falls below the IAC the lowest address, pointing to the top. An additional counter (FC) shows the level of the memory, ie with every written word of the counter is incremented, decremented with each read. Based on the FC can be seen when the

Memory is empty or full. This technology is known from FIFOs. Thus, a block written in the external memory, the adjustment ranges

of FC to update the stack. An external address counter (EAC) always points to the oldest in mem-ory and entry is thus at the IAC opposite end of the stack. The EAC is modified if

a) data is written to the external stack, then it runs in the direction of IAC, b) data is read from the external stack, then removed he from IAC.

**[0075]** By monitoring the FC ensures that IAC and EAC not collide.

**[0076]** The ERC will be modified according to the external stack operation (increasing or decreasing).

#### MMU

**[0077]** The external memory interface can be associated with a MMU, which performs two functions:

1. Conversion of the internal addresses to external addresses to support modern operating systems 2. Monitoring of accesses to external

Addresses, for. Example, generate an error signal as a trigger, when the external stack over or underflows.

Compiler

[0078] The programming principle of the invention the VPU technology is to separate and sequential code in as many small and independent part of algorithms to decompose, while the part of the algorithms Datenflußcodes is mapped directly to the VPU.

Separation between the VPU and standard code

[0079] representative within a language according to the state of the art for all sorts of compiler (Pascal, Java, Fortran, etc) to C

++ Be used in another, you can define a special extension (VC = Vpu C) that contains the language constructs and types are particularly well imaged on a VPU technology. VCs may be used by the programmer only within Procedures or functions

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Quality.

are not using other constructs or types. This Procedures and functions directly imaged on the VPU and run particularly efficient from. The compiler extracts the VC in the preprocessor and passes it directly to the VC-Backend Processing (VCBP) further.

Extraction of parallelizable compiler code

[0080] In the next step, the compiler analyzes the remaining C ++ code and extracts the parts (MC = mappable C) that run in parallel and

without the use of sequencers are imaged on the VPU technology. Each MC is placed and routed in a virtual array. After that

is the space requirement, as well as the expected performance analyzed. For this purpose the VCBP is called and the individual MC along with

the VC, which are mapped in each case partitioned.

[0081] The MCs whose VPU implementation will achieve the highest performance increase adopted, are as C ++, the rest of the

Next Level Compiler passed.

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Optimizing sequencer generator

[0082] This compiler level is different depending on the architecture of the implemented VPU system:

1. VPU without sequencer and external processor

[0083] All remaining C ++ code to be compiled for the external processor.

2. Only VPU with Sequencer2.1 sequencer in the PAEs

[0084] All remaining C ++ code to be compiled for the sequencer of PAEs.

2.2 Configurable sequencer in the array

[0085] The remaining C ++ code is analyzed for each independent module. The most appropriate variant of a sequencer Database selected and stored as VC code (SVC). This step is usually iteratively, that is, a sequencer variant is selected, the code is

compiled, analyzed, and compared with the compiled code sequencer other variants. Ultimately, the object code (SVCO) of C ++ code

generated for the selected SVC.

2.3 both 2.1 and 2.2 are used

[0086] corresponds to the operation of 2.2. There are special static sequencer models for the sequencer in the PAEs in Database.

3. VPU with sequencer and external processor

[0087] Also, this operation corresponds to 2.2. For the external processor exist special static sequencer models in the database.

Left

[0088] The linker connects the individual modules (VC, MC, SVC and SVCO) to an executable program. For this he uses the VCBP order

to place the individual modules to route and determine the temporal partitioning. The linker also adds the communication structures

added between the individual modules and accompanied where appropriate by a register and memory. Based on an analysis of the control structures and

Dependencies of the individual modules are structures for storing the internal states of the array and the sequencer for the case of

Reconfiguration added.

Comments on the processor models

[0089] The machine model used can be combined within a VPU. Also within an algorithm, depending on the the which model is optimal to switch between the models.

[0090] If a register processor added another memory from which the operands are read and in which the results are written, a load / store processor can be built. Several different memory can be allocated by the single operand and the result is treated separately.

[0091] This memory then work as a kind of load / store unit and provide a kind of cache for the external memory is. The addresses

calculated by separated from the data processing PAEs.

Pointer reordering

[0092] high-level languages such as C / C ++ often use pointers, which can be handled very badly by pipelines. When a pointer only

directly before using the data structures to which it points is calculated, can often not be filled fast enough and that the pipeline

Processing is especially inefficient in VPUs.

[0093] It is certainly possible to use any pointers useful when programming VPUs, but this is often not possible.

[0094] The solution is to re-sort the pointer structures by the compiler so that the pointer addresses use as long as possible prior to their

be calculated. At the same time there should be as few direct dependencies between a pointer and the data to which it points.

Extensions of PAEs (compared to P196 5 075.9 54 846.2 and P196)

[0095] By P196 P196 54 51 075.9 and 846.2 of the prior art is defined in terms of the configuration properties of cells (PAEs).

[0096] It will be dealt with on two properties:

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1. One of PAE **(0903)** 51 075.9 according to P196, a set of configuration registers **(0904)** assigned), which includes a configuration **(Fig. 9a)**. . 2

A group of PAEs **(0902)**, according to P196 54 846.2 on a memory for storing or reading data access **(Fig. 9b)**

[0097] job is,

a) to provide a method which speeds up the reconfiguration of PAEs and temporally decoupled from the parent loading unit, and b) the

Procedures interpreted as meaning that at the same time creates the possibility of multiple configurations to sequences, and c) at the same time more

To keep configurations in a PAE of which always is activated and quickly switch between different configurations can.

Decoupling the configuration register

[0098] The configuration register is used by the higher-level loading unit (CT) decoupled **(Fig. 10)** by a set of several Configuration registers **(1001)** is used. Always exactly one of the configuration registers selectively determines the function of the PAE. The selection

the active register is via a multiplexer **(1002)** performed). In each of the configuration register can write any CT, provided this is not the current configuration of PAE determined, ie is active. The writing on the active tab is possible in principle to stand in the

PACT10 described methods.

[0099] Which configuration register from **1002** is selected may be determined by various sources:

1. Any state signal or a group of any status signals via a bus system **(0802)** to **1002** will be performed **(Fig. 10a)**. The Status signals are generated by any PAEs or provided by external connectors of the module (see. **Fig. 8**) 2. The

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Quality.

Status signal of PAE that of **1001/1002** is configured is used to select **(Fig. 10b)**. 3. An image generated from the higher level CT signal is used

for selection **(Fig. 10c)**.

[0100] It is possible either the incoming signals **(1003)** by means of a register for a specified period and to store alternatively and selectively retrieve.

[0101] The use of a plurality of registers, the CT is temporally decoupled. This means that CT can have multiple configurations "subpoena" without a direct temporal dependency.

[0102] Only when the selected / activated Register in **1001** has not yet been charged, is serviced with the configuration of the PAE until

the CT has loaded the register. To determine if a register has a valid information, for example, a "valid bit" (**1004**) by Register to be introduced, which is set by the CT. If **0906** is not set in a selected register, the CT is a signal for Configure the register as soon as possible prompted.

[0103] The in **FIG.** Described method 10 can be expanded easily to a sequencer (**Fig. 11**). For this purpose a sequencer Instruction decoder (**1101**) for controlling the selection signals of the multiplexer (**1002** used). The sequencer determines dependent on

the currently selected configuration (**1102**) and an additional status information (1103/1104) the next to be selected configuration. Those who

Status information can

a) the status of the status signal of the PAE, of **1001/1002** is configured (**Fig. 11a**), b) over any **0802** to be supplied to status signal

(**Fig. 11b**) c) be a combination of (a) and (b).

[0104] **1001** can also be configured as a memory, rather than **1002**, a command of **1101** is addressed. Addressing is dependent

the command itself and a status register. To this extent, the construction of a "von Neumann" machine, with the difference

a) the universal use, so do not use the sequencer (see. **Fig. 10**) b) that the status signal is not from the sequencer associated arithmetic unit (PAE) must be generated, but may be from a beliebigen other calculating unit (see. **Fig. 11b**).

[0105] It is important that the sequencer jumps, particularly conditional jumps, within **1001** can perform.

[0106] A further additional or alternative method (**Fig. 12**) for setting on sequencers within VPU is the use of the internal data memory (1201, **0901**) for storing the configuration information for a PAE or a group of PAEs. In this case, the

Switched data output of a memory to a configuration input or data input of a PAE or more PAEs (1202). The address (1203) for **1201** can be generated from the same PAE / PAEs same or any one or more others.

[0107] In this method, the sequencer is not firmly implemented, but is modeled by a PAE or a group of PAEs. The internal memory can run programs from the external memory to reload (cf.. inventive storage system).

[0108] For storing local data (eg. As for iterative calculations and as register for a sequencer)

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the PAE is provided with an additional set of registers, the individual registers determined either by the configuration, led to the ALU

or are described by the ALU; can be used freely or through the instruction set of a sequencer implemented (Register Mode).

Also, one of the registers are used as an accumulator (battery mode). If the PAE used as full-fledged machine, it is make good use of one of the registers as an address counter for external data addresses.

[0109] To manage stacks and accumulators outside the PAE (z. B. in the inventive storing) is that already described RDY / ACK REQ / ACK Synchronisationsmodell used.

[0110] PAEs according to the prior art (see. PACT02) are for the processing of bit-wise operations ill-suited, as long as the integrated

ALU bit operations not specifically supports or narrow (1-, 2-, 4-bit wide) is designed. The processing of individual bits or signals can

efficiently ensured by the ALU core is replaced by a FPGA core (LC) that performs configurable logic operations. The LC is

while in its function and internal networking freely configurable. It can be used in accordance with the LC prior art. For certain

Operations, it is useful to assign a LC internal memory. The interface modules between FC and the bus system of the array

only slightly adapted to the FC, but remain fundamentally. To increase flexibility of the time behavior of the FC, it is advisable,

to make the register can be switched off in the interface modules.

characters

[0111] In **Fig. 4a**, some basic characteristics of the process of the invention are shown:

[0112] The modules of type A are combined to form a group and hold at the end of a conditional jump, either B1 or B2. At this position (**0401**) a Umkonfigurationspunkt is inserted because it is useful to the branches of the conditional jump as single

To consider group (case 1). On the other hand would both branches of B (B1 and B2) addition along with A fit on the target device (case

**2), it would make sense only in a Umkonfigurationspunkt 0402** insert, as a result, the number of configurations is reduced and the

Processing speed increases. Both branches (B1 and B2) jump in **0402** by C.

**[0113]** The configuration of the cells on the target block is in **Fig. 4b** schematically. The functions of the individual are Graph nodes mapped to the cells of the target block. One line represents a configuration. The dashed arrows in a Line breaks indicate a reconfiguration. S

n

is a data-storing cell of any configuration (registers, memory, etc.). This

is S

n

I is a memory that accepts data and S

n

O outputs a memory of the data. The memory S

n

is for the same n are each the same, I and O

characterize the data transfer direction.

**[0114]** Both cases of conditional jump (Case 1, Case 2) are shown.

**[0115]** The model in **Fig. 4** corresponds to a data flow, however with the significant expansion of the Umkonfigurationspunkts and the resulting

achievable partitioning of the graph, the data transmitted between the partitions data is cached.

**[0116]** In the model of **Fig. 5a** of an arbitrary graph quantity and -Konstellation (**0501**) selectively a graph B

n

from a set of graphs

B called. After execution of the B data from leaving the **0501** return.

**[0117]** If in **0501** implemented a sufficiently large Sequencer (A), is the model a typical processors very similar principle implementable. Reach Here

1. Data in the sequencer A that this decoded as commands and react in accordance with the "von Neumann" principle it;

2. Data in the

A sequencer, which are regarded as data and forwarded to a fixed configured arithmetic unit C for calculation.

**[0118]** The graph B represents a special selectable arithmetic units and / or special opcodes for certain functions and is alternatively used for accelerating C. For example, B1 be an optimized algorithm for calculation of matrix multiplications, while B2 represents an FIR filter and B3 a pattern recognition. According to an opcode of the **0501** is decoded, the appropriate

or corresponding Graph B called.

**[0119]** **FIG. 5b** schematically the picture to the individual cells, where in **0502** symbolized the pipelined arithmetic logic unit Character.

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Quality.

**[0120]** While in the Umkonfigurationspunkten of **Fig. 4** preferably larger memory are inserted for temporarily storing the data,

a simple synchronization of the data in the Umkonfigurationspunkten of **Fig. 5** is sufficient, because the data stream as a whole preferably by

the graph B is running and the graph B not partitioned; characterized the temporary storage of the data is unnecessary.

**[0121]** In **Fig. 6a** are shown different loops. Loops can be basically treated in three ways:

1. hardware approach: loops are fully rolled out to the target hardware ready (**0601** A / B). As already explained, this is only a few

Loop types possible. 2. dataflow approach: Within the data flow loops are constructed across cells (**0602** / b). That

End of the loop is fed back to the loop start. 3. sequencer approach: A sequencer with minimal instruction set executes the loop

(**0603** a / b). Here (see., The cells of the target blocks are designed so that they keep striking the appropriate sequencer **Fig. 11a** / b).

**[0122]** By a suitable separation of loops whose execution can be optimized if necessary:

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1. Using optimization methods according to the prior art often leaves the loop body, ie the repeated executed

Part, thus optimizing that certain operations are removed from the loop and before or be placed behind the loop (**0604** / b). Characterized the set of instructions to sequencenden is considerably reduced. The remote operations are only once before or after execution

the loop through. 2. Another possibility for optimization is the sharing of loops into several smaller or shorter loops. It finds the division place so that a plurality of parallel or sequential multiple (**0605** a / b) loops are formed.

**[0123]** FIG. 7 illustrates the implementation of a recursion. Here are the same resources (**0701**) in the form of cells for each

Recursion level (**1-3**) is used. The results of each recursion level (**1-3**) to build (**0711** :) in a stack according to the principle built memory (**0702**) is written. Simultaneously with the reduction (**0712** :) the levels degrades the stack.

**[0124]** In Fig. 14, the virtual machine model shown. From an external memory, data (**1401**) and belonging to the data States (in **1402**) in a VPU (**1403** read).

**[0125]** **1401/1402** will be a generated by the VPU address **1404** selected. Within the VPU PAEs are to different groups summarized (**1405**, **1406**, **1407**). Each group has a data processing part (**1408**), the local impilzite states (**1409** has), the has no influence on the surrounding groups. Therefore, the states will not be forwarded outside the group. He may, however, by

be the external conditions depends. Another part (**1410**) generates conditions which affect the surrounding groups.

**[0126]** The data and states of the results in a further memory (**1411**, **1412**) filed. At the same time, the address of Operand (**14004**) stored as a pointer (in **1413** be). For time synchronization may **1404** via registers (**1414**) will be performed.

**[0127]** In FIG. 14, a simple model is shown for clarity. The networking and grouping may be more complex than in this model. Also states and data can also be transferred to other modules as the following. It is possible that Data is transferred to other modules than the states. Both data and states of a particular module can be of several received different modules. Within a group, in **1408**, **1409** and **1410** be present. Depending on the algorithm can (z. B. also parts missing in **1410** and **1409** exist, in **1410** but not).

**[0128]** In Fig. 15 is shown to be extracted from a processing graph subapplications like. Here the graph is so broken that long

Graphs are divided sense and be displayed in the sub-applications (H, A, C, K). After jumps new subgraphs are formed (C, K)

where a separate part graph is formed for each jump.

**[0129]** Each sub-graph in the ULIW model of the CT separately (see. PACT10) loaded. It is essential that subgraphs in the mechanisms

PACT10 can be managed. This includes in particular the intelligent configure, run / start, and delete the part of applications.

**[0130]** **1503** causes the loading or configuring subapplication A while subapplication K runs. This is

a) A partial application already fully configured for execution by the end subapplication K in the PAEs, provided that PAEs more

Have configuration registers; b) A partial application already loaded for execution end of subapplication K in the CT, provided that PAEs only

Have configuration registers.

**[0131]** **1504** starts the execution of subapplication K.

**[0132]** D. h. at runtime are independently loaded the next required program components during execution of the current program parts.

This results in a much more efficient use of the program code, as in conventional cache mechanisms.

**[0133]** In subapplications A is represented another peculiarity. In principle, it is conceivable both possible branches (C, K) of the comparison

preconfigure. Assuming that the number of available free configuration register is not sufficient for this purpose, is the more probable

the branches configured (**1506**). This also saves configuration time. In embodiments of the non-configured branch, is (since the configuration yet

is not loaded in the configuration register) program execution pauses until the branch is configured.

**[0134]** In principle it is possible to perform not configured subapplications (**1505**), this must be as described before Execution load.

**[0135]** A FETCH command can be triggered by a trigger by its own ID. This part applications can depend on State of the array are preloaded.

**[0136]** The ULIW model differs substantially from the VLIW model by

1. The routing of data includes 2 Larger instruction words forming.

**[0137]** Also, the described method of partitioning of compilers for today's standard processors in accordance with the RISC / CISC principle

also be used. Then, a unit (CT) is used to PACT10 for controlling the instruction cache, this can greatly optimizes

and are accelerated.

[0138] These "normal" programs are partitioned accordingly in part applications. According PACT10 are references to possible subsequent subapplications introduced (1501, 1502). Thus, a CT which subapplications already summoned into the cache before it needs

become. If there are jumps only jumped subapplication is executed, the other (s) will be overwritten later by new member applications.

In addition to the intelligent preloading

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initiated the procedure has the further advantage that the size of the part of applications loading is already known. This allows optimum bursts at

Access running on the memory of the CT, which in turn will speed up memory access considerably.

[0139] FIG. 16 shows the structure of a stack processor. By PAE array (1601) logs are generated by an as LIFO configured storage (1602 to write) or read. Here, a RDY / ACK protocol for writing and REQ / ACK protocol for reading used. The crosslinking and operating modes of the CT (1603 configured). 1602 can thereby its contents to the external memory (1604) outsource.

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Quality.

[0140] A number of PAEs to in this example as Registrar processor work (Fig. 17). Each PAE consists of an arithmetic logic unit (1701)

and an accumulator (1702) on the outcome of 1701 is fed back (1703) is. This provides in this example, each PAE an accumulator

Processor. A PAE (1705) reads and writes the data to the configured as the default memory RAM (1704). Another PAE (1706) generated the register addresses.

[0141] It is often useful to use a separate PAE to read the data. Then would 1705 just write and the PAE 1707 read.

Here another PAE (is 1708, dashed lined) introduce to generate the read addresses.

[0142] It is not absolutely necessary to use separate PAEs to generate the addresses. Often, the registers are implied and can

are then configured as constants are sent from the data processing PAEs.

[0143] The use of battery-processors for a processor register is exemplary. Similarly, to build

Register processors PAEs be used without battery. The in Fig. Architecture shown can 17 to control registers as well as for

Serve driving a load / store unit.

[0144] When used as load / store unit, it is almost imperative an external RAM (1709) downstream of, so that in 1704 only one

temporary detail from 1709, as a kind of cache represents.

[0145] Even with the use of 1704 as a register bank, it is partially useful downstream of an external memory. As a result, PUSH / POP operations according to the prior art are performed, the writing to the register content in a memory or from reading this.

[0146] In Fig. 18 is an example of a complex machine shown in the PAE-array (1801) on the one hand a load / store-unit (1802) with

downstream RAM (1803) activates while maintaining a register bank (1804) with a downstream RAM (1805) has. 1802 and 1804

can be driven by a PAE or any group of PAEs respectively. The unit is in accordance with the principle of a CT VPU (1806) controlled.

[0147] It is important that between the load / store unit (1802) and the register bank (1804) and their control is no substantial difference consists.

[0148] The FIG. 19, 20, 21 show an internal memory according to the invention, at the same time a communication unit with external memories

and / or peripheral represents. The individual figures show different operating modes of the same memory. The operating modes, as well as individual

Detail settings are configured here.

**[0149] FIG. 19a** shows a memory according to the invention in the "Register / Cache" mode. In memory of the invention **(1901)** are data words

a usually larger and slower external memory **(1902)** is stored.

**[0150]** The data exchange between **1901**, **1902** and through a bus **(1903)** PAEs connected (not shown) takes place as follows

instead, being under two operating modes are distinguished:

A) by the PAEs from the main memory **1902** read or transmitted data in **1901** backed by a cache method.

Here, any known cache method used. B) By means of a load / store unit, the data of certain addresses between **1902** and **1901** transfer. Here are some addresses, both in **1902** and in **1901** set, which for **1902** and **1901** usually different addresses are used. The individual addresses this by constant or by calculation in PAEs are generated. In this mode, the memory works in **1901** as a register bank.

**[0151]** The assignment of addresses between **1901** and **1902** can be arbitrary and depends only on the respective algorithms of the two

Modes from.

**[0152]** In the corresponding machine **19b** is shown as a block diagram. Transportation in **1901** and **1902** is a control unit **(1904)**

assigned, depending on the operating mode as a load / store unit (prior art), or as a cache controller (according to the prior art)

acting. This unit can, if required, a memory management unit (MMU) **(1905)** be associated with address translation and verification).

Both in **1904** and **1905** can be driven by the PAEs. Thus, the MMU will be programmed, for example, set the Load / Store addresses

or a cache flush triggered.

**[0153] FIG. 20** shows the use of the memory **(2001)** in the FIFO mode in which according to the known FIFO data streams decoupled

become. The typical use is in a write **(2001 a)** or reading interface **(2001 b)**. Here are data between the PAEs which internal to the

Bus system **(2002)** are connected and the peripheral bus **(2003)** temporally decoupled.

**[0154]** For the control of the FIFO is a unit **(2004)** provided) corresponding to the write and read pointers of the FIFO depends on the bus operations of **2003** and **2002** controls.

**[0155]** In **Fig. 21**, the operation principle of the memory according to the invention is shown in Stack mode. A stack (the prior art) a

Stack whose top / lowest element that is currently active. Data / added always top down, as the data above / bottom removed. I.e. The date last written is also the one that is read first (Last In First Out). Whether a stack up or down growing, is insignificant and implementation dependent. In the following embodiment stacks are considered that grow upwards.

**[0156]** In this case, the most recent data in the internal memory are **2101** held, the most recent entry **(2107)** is at the top in **2101**. Old

Entries are to the external memory **2102** outsourced. Grows the stack further extends the

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Place in the internal memory in **2101** no longer sufficient. Upon reaching a certain amount of data by a (freely selectable) address in **2101**, or

an (arbitrary) value can be represented in an entry counter, is a part of **2101** as a block at the end of more recent **(2103)** of the stack

in **2102** wrote. This part is the oldest, and therefore the least recent data **(2104)**. Thereafter, the remaining data in will be in **2101**

shifted so that after **2102** copied data in **2101** with the remaining data **(2105)** to overwrite) and thus enough free Memory **(2106)** for new stack entries arises.

**[0157]** If from the stack, the data are from a certain (arbitrary) point in **2101** shifted so that behind the oldest and unaktuellsten data free memory is created. In the vacated memory, a memory block is **2102** copies, which then **2102** is deleted.

**[0158]** In other words, representing **2101** and **2102** in a single stack, with the currently active listings in **2101** are and older and less recent in **2102** are outsourced. Quasi, the method provides a cache for stacks. Since the blocks of data preferably

are transmitted by block operations, the data transfer between may **2101** and **2102** in the fast burst modes modern memory

(SDRAM, RAMBUS, etc.) are executed.

[0159] It should be noted again that in the embodiment in FIG. 21, the stack grows upward. Should the stack grow downwards (a commonly used method), the positions up / down and the directions are in moving data within a memory exactly reversed.

[0160] It makes sense to the internal stack is **2101** configured as a kind of ring buffer. The data at one end of the ring to be between

PAEs and in **2101** transferred to the other end of the ring between **2101** and **2102**. This gives the advantage that easily transfer data between

**2101** and **2102** can be moved without affecting the internal addresses in **2101** to have. Only the cursor and the lower upper data and the level meter must be adapted to each case. The data transmission between **2101** and **2102**, by the well-known

Ring memory flags "almost full (almost full) / Full (Full)" and "almost empty (almost empty) / empty (empty)" are triggered.

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[0161] The necessary hardware is a block diagram in Fig. 21B. The internal stack **2101** is a unit (**2110**) for the management of

Associated pointers and counters. In the bus (**2114**) is between **2101** and **2102** a unit (is **2111**) looped to control data transfers.

This unit can be a MMU (**2112**) according to the prior art with the corresponding inspection systems and address translations associated become.

[0162] The connection between the PAEs and **2101** is over the bus system **2113** implemented.

[0163] In Fig. 22 an example of the re-sorting of the graph shown. The left column (22 .a) shows an unoptimized arrangement of commands.

The pointer A (be **2207** a) and B (**2211** a) loaded. In each case already one clock later, the values of the pointers are needed (**2208** a, **2212** a).

This dependence is to be performed too short to efficiently because of loading from the memory a certain period of time (**2220** a, **2221** a) is required.

By rearrange the commands (22 .b) the periods are maximum increases (**2220** b, **2221** b). Although in **2210** and in **2208** the value of the pointer

is needed by A, is **2208** by **2210** sorted, as more time for the calculation of B is obtained. It is possible for the calculations regardless of the pointers are (**2203**, **2204**, **2206**) for example, between **2211** and **2212** to add more time for memory accesses to

obtain. A compiler or assembler can here based on system parameters which represent the access times, the corresponding optimization make.

[0164] FIG. 23 shows a special case of Fig. 4-7. Often there is an algorithm, even within loops, and from Datenflußteilen sequential parts. Such structures can according to the described method using the bus system described in PACT07 be built efficiently. To this end, the RDY / ACK protocol of the bus system is first extended by REQ / ACK protocol according to the invention.

This can be retrieved from one or more other PAEs or from the CT targeted register contents of individual PAEs. A bow (**2305**) is now divided into at least two graphs, the first one (**2301**) representing the Datenflußanteil and second (**2302**) of the sequential share maps.

[0165] A conditional branch chooses between the two graphs. The special feature is that in **2302** the internal state of **2301** to know for

Execution required and vice versa in **2301** the state of **2302** needs to know.

[0166] This is realized by the state only once, namely in the registers of the PAEs of performant dataflow (**2301**) is stored.

[0167] If in **2302** jumped, reads the sequencer when needed, the states of the respective registers of the bus system by means of PACT07 from

(**2303**). The sequencer performs its operations and writes any changed conditions in the registry (again via the bus system by

PACT07) back (in **2304**). Finally, it should be noted that it is the graph discussed not necessarily to close loops (**2305**) must act. The method is generally applicable to any part of the algorithm, which is executed several times within a program run

(reentrant) and optionally either sequentially or in parallel (datenflußartig) is processed, the states between the sequential and must be transferred to the parallel part.

**[0168]** The Waverekonfigurierung provides considerable advantages in the speed of the reconfiguration, especially in simple sequential

Operations.

**[0169]** A basic feature of this processing method that the sequencer be configured as external microprocessor can. This means that a processor is connected via the data channels of the array and local temporary data bus systems with the Array exchanges. All parts of a sequential algorithm which can not be displayed in the array of PAEs are on the processor handled.

**[0170]** It is necessary to distinguish between three Bussystemem:

1. Data, which regulates the exchange of data between the VPU and verarbeiteten processor. 2. register bus, the access to the registers of VPU

permits and thus the exchange of data (2302, **2304**), **between 2302 and 2301** guaranteed. 3. configuration data, of the array of VPU

configured.

**[0171]** In **Fig. 24** the effects are presented chronologically.

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**[0172]** Just hatched areas represent data processing PAEs, with **2401** PAEs after reconfiguration and **2403** PAEs before Show reconfiguration. Double shaded areas (**2402**) show PAEs that are being reconfigured or waiting for reconfiguration.

**[0173]** **FIG. 24a** shows the influence of wave reconfiguration to a simple sequential algorithm. Here it is possible exactly the PAEs

reconfigure, where a new task is assigned. Since each clock a PAE receives a task this can efficiently, namely at the same time

be performed.

**[0174]** illustrated example, a number of PAEs from the matrix of all PAEs of a VPU. Indicated the states are in bars after Clock t with one clock delay.

**[0175]** In **Fig. 24b** the temporal effect of the reconfiguration is shown by large sections. For example, shown is a lot of PAEs

a VPU. Indicated the states are in bars after clock t with a different delay of each multiple clocks.

**[0176]** While at first only a small part of PAEs reconfigured or waiting for the reconfiguration, this area increases will Time bigger until all PAEs are reconfigured. The larger the area will mean that, due to the delay by the Reconfiguration increasingly PAEs on the reconfiguration waiting (2402). This is lost computing power.

**[0177]** It is therefore proposed a wider bus between the CT (especially the memory of the CT) and the PAEs use, the enough lines makes available to reconfigure multiple PAEs simultaneously within a cycle.

**[0178]** **FIG. 25** illustrates the scalability of VPU technology. The scalability is mainly due to the roll-out of a graphene out without a temporal sequence separated individual part applications. As an example of the algorithm is **Fig. 4** is selected. In **Fig. 25a**, the

transmit individual subgraphs consecutively on the VPU, being either B1 or B2 loaded. In **Fig. 25b**, all subgraphs are on transferred a lot of VPUs and linked to bus systems with each other. This allows large amounts of data without the negative influence

the Umkonfigurierens be processed efficiently.

**[0179]** **FIG. 26** shows a circuit for accelerating the (re) configuration time of PAEs. At the same time, the circuit can for processing

sequential algorithms are used. The array of PAEs (**2605**) is divided into several parts (**2603** partitioned). Each part is an independent

Unit for (re) configuration (**2602** assigned). These units is superior to a CT (**2601**) according to the prior art (see **FIG. PACT10**), the

is in turn connected to a further CT or to a memory (2604). The CT invites the algorithms in the configuration units (2602). The

**2602** load automatically your configuration data in their assigned PAEs.

**[0180]** In **Fig. 27**, a structure of a configuration unit is shown. The core unit is a sequencer (**2701**) of a set of commands dominated.

**[0181]** The main commands are:

wait <trg #> Wait for the arrival of a specific trigger from the array, indicating which next configuration to be loaded.

Lookup <trg #> Returns the address of the called by an incoming trigger subroutine.

JMP <addr> leap address

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Quality.

call <addr> leap address. Return address is stored on the stack

JMP <cond> <addr> Conditional jump by Address

call <cond> <addr> Conditional jump by Address. Return address is stored on the stack

ret Return to the return address stored on the stack

mov <target> <source> Transfers a word of data from source (source) to a destination (target). Source and destination may be located in a memory or a

Its periphery address.

**[0182]** Essentially, the commands from PACT10, that the description of the CT known. A significant difference in the implementation of

**2602** is that only very simple commands are used for data management and not a complete microcontroller is used.

**[0183]** A significant extension of the instruction set is the "PQBm" - command to configure the PAEs. There are two commands (pabmr, pabmm)

available which are composed as follows:

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**[0184]** The commands to copy an assigned block of addresses and PAE PAE data from memory to the PAE array. By <count> is

given how large the data block is to be copied. The data block is either attached directly to the opcode (a) or by specifying the first

Memory address <MEMREF> referenced (b).

**[0185]** Each pa\_adr

n

-pa\_dta

n

-line Illustrates a configuration for a PAE. It is pa\_adr

n

, The address and pa\_dta

n

the configuration of the word

PAE on.

**[0186]** From PACT10 the RDY / ACK REJ protocol is known. If the configuration data accepted by a PAE, the PAE acknowledges the

transmitted data with an ACK. By contrast, if PAE configuration data not accept, because they are not in a reconfigurable State, it sends back a REJ. This fails to configure the algorithm part.

**[0187]** The point with REJ rejected pa\_adr

n

-pa\_dta

n

-line Is stored. The commands are again at a later time

called (cf.. PACT10, FILMO). If the command has been completely processed, ie it did not occur REJ, the command does not further

Configuration through but terminated immediately. Trat a REJ on, the command skips directly to the site of the rejected pa\_adr

n

-pa\_dta

n

-Row. Ever

according to command the body is stored differently:

pabmr: The address is stored in the register referred to with <regno>.

pabmm: The address is gespeichert directly in command at the storage location <offset>.

**[0188]** The commands are implemented by DMA structures as memory / IO transfers according to the prior art. The DMAs are

extended logic to monitor the incoming ACK / REJ. The start address is determined by <regno>, or <offset>. The last address of the

Data block is determined by the address of the instruction plus the opcode length minus one plus the number of pa\_adr

n

-pa\_dta  
n

-lines Calculated.

[0189] It is useful to expand the circuit described in PACT10 by the above commands.

[0190] FIG. 27 shows the structure of unit 2602. The unit consists of a set of registers 2701 to a simple ALU operations for Stack

is assigned (2702). The structure contains address registers and stack pointer. Optionally, a complete ALU be used. A bus system

(2703) with a minimum width combines registers and ALU. The width is dimensioned so that simple or easy Kontrollflußbefehle ALU

Operations can be shown useful. In addition, the above-described PQBm commands, and the commands after PACT10 be supports.

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Register and ALU are from a sequencer 2706 controlled, which is by executing commands a complete microcontroller. At 2703 is a unit 2704 connected to the trigger receives from the associated PAEs and acknowledged and, optionally, in turn, trigger sends to the PAEs.

[0191] Incoming triggers solve it in the sequencer 2706 an interrupt or be polled by the WAIT command. Optional on 2703 connected is an interface (2705) to a data bus of the associated PAEs to be able to send data to the PAEs. For example, the assembler code of an implemented in the PAEs sequencer over 2705 sent. The interface includes a converter if necessary to

Adjustment of different bus widths. The units 2701 bis 2706 are connected via a multiplexer / demultiplexer (2707) to a by a multiple

wider bus system (2708) connected to the memory (2709 results). 2707 is the low-order addresses of the address / Stack register

driven, the high-order address leading directly to the RAM (2711). The bus system 2708 results in an interface (2709) obtained by the PA

Commands is controlled and leads to the configuration bus of PAEs. 2708 is designed deliberately broad, lowest configuration bits per clock unit

over 2709 to send to the PAEs. Another interface (2710) connects the bus with a higher level CT, configuration and Control data with 2602 exchanges. The Interface 2710 and 2709 on several occasions in PACT10, PACT ?? been described.

[0192] It is essential that in 2706 a reduced and optimized to the task minimum instruction set dominates, the mainly to the PA

Commands, jumps, interrupts and lookup commands is optimized. Furthermore, the optimized wide bus system in 2708, the more than 2707 narrow on a

Is transmitted bus system is of particular importance for the Umkonfigurationsgeschwindigkeit the unit.

[0193] FIG. 27A is a specific configuration of Fig. 27. The interface 2705 is used for transferring assembly code to the PAE array

configured sequencer. The processing power of the sequencer essentially depends on the speed of the interface 2705 and the

Memory access from. In Fig. 27a is 2705 through a DMA function with direct memory access (2720

n

) Replaced. 2720

n

performs its own memory accesses

and has its own bus system (2722

n

) With a corresponding adjustment of the bus width (2721

n

); while the bus can for loading wide

Command sequences (ULIW) turn out relatively wide, so that as a limiting case in 2721

n

completely unnecessary. To further increase the speed is

the memory 2711 physically in 2711 a and 2711 b

n

been separated. The address space about 2711 a and 2711 b

n

remains linear, but may be from 2701,  
 2702, **2706** are accessed independently simultaneously to both memory blocks; **2720**  
 n  
 can only **2711** b  
 n  
 access. **2720**  
 n  
 , **2721**  
 n  
 And **2711** b  
 n  
 can  
 several times (  
 n  
 Be implemented), so that multiple sequencers may be managed simultaneously. For this purpose, **2711** b  
 n  
 again in several physical  
 independent memory areas are divided. In **Fig. 38** are examples of implementation **2720**  
 n  
 described.

**[0194]** In **FIG. 28**, the structure of complex programs is illustrated. The basic modules of the programs are the complexing configurations

(**2801**) containing the configuration one or more PAEs and the associated bus and trigger configurations. The **2801** will be an opcode (**2802**) represents the additional parameters (**2803**) may possess. These parameters can on the one hand constant data values, variable

Home values or special configurations include. There each one according to function, several or no parameter.

**[0195]** Several opcodes draw on a common set of complex configurations back and thus form an opcode group (**2805**). The different opcodes a group distinguished by particular embodiments of the complex configurations. To differentiations (**2807**) used which contain either additional configuration words, or in **2801** occurring configuration words override.

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**[0196]** A complex-configuration unless differentiation is necessary, called directly by an opcode (**2806**). A program (**2804**) consists of a sequence of opcodes together with the relevant parameters.

**[0197]** A complex function can even be loaded into the array and can then by different parameters or differentiations are newly reconfigured. Only the changing parts of the configuration to be reconfigured. Different opcode groups access different complex configurations back. (**2805** a,..., **2805** n).

**[0198]** The different levels (complex configuration, differentiation, opcode, program) are in various levels of CTs processed (see. CT hierarchies in PACT10). The different levels are in **2810** represented, where 1 is the lowest and N the highest level

represents. CTs can be set up to arbitrarily deep hierarchies (cf.. PACT10).

**[0199]** It is in **2801** differed under two types of codes:

1. configuration words that depict an algorithm on the array of PAEs. The algorithm can be configured as a sequencer. The

Configuration is done via the interface 2709. Configuration words are defined by the hardware. 2. algorithm-specific codes of

the possible configuration of a sequencer or algorithm depend. These codes are defined by the programmer or compiler and

are used to control an algorithm. For example, a Z80 configured as a sequencer in the PAEs, these codes the opcode of the Z80

The microprocessor represents. Algorithm Specific codes are **2705** sent to the array of PAEs.

**[0200]** In **Fig. 29**, a possible basic structure of a PAE is shown. **2901** and **2902** represent the input and output registers of the data

assigned to represent. the registers is a complete networking logic for switching on / data buses (**2920**, **2921**) of the array (see **PACT02**).

The trigger lines acc. PACT08 be **2903** from the trigger bus (**2922** tapped) and with **2904** on the trigger bus (**2923** switched).

Between **2901** and **2902** an ALU (is **2905**) **any configuration connected**. The data buses (**2906**, **2907**) and the ALU is **assigned a**

Register set (**2915**), in which local data is stored. The RDY / ACK Synchronisationssignale the data buses and coaches will trigger

a state machine (or sequencer) (**2910**) carried out (**2908**), or generated by the unit (**2909**).

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[**0201**] About an interface unit (**2911**) accesses the CT by means of a bus system (**2912**) selectively to a plurality of configuration registers (**2913**)

to. **2910** selected via a multiplexer (**2914**) each having a particular configuration of, or a plurality of Konfigurationswörtern sequenzt that

then represent commands for the sequencer.

[**0202**] Since the VPU technology works mainly pipelined, it is advantageous either the group in **2901** and **2903** or the Group in **2902** and

**2904** or both groups additionally to be provided with FIFOs. This can prevent that a pipeline by simple delays (z. B. increase in the synchronization).

[**0203**] **2920** is an optional bus access, via a memory of a CT (see Fig. 27, **2720**) or a **gewöhnlicher internal memory in place of**

the configuration register to the sequencer **2910** can be switched. This means that large sequential programs executed in a PAE. Of the

Multiplexer **2914** is connected thereto so that it only connects the internal memory.

[**0204**] The addresses

a) for the memory CT through the circuit in FIG. 38 generated. b) for the internal memory directly from **2910** generated.

[**0205**] FIG. 30 shows a possible extension of PAE to the CT or another zuegschalteten microprocessor access to the To enable data register. The address space and the interface of the bus unit (formerly **2911**, **3003**) **are the additional data buses** (**3001**)

extended. The respective registers, a multiplexer (**3002**) upstream mittles the **3003** via the bus **3001** to write data to the register

can. The outputs of the registers are about **3001** back to **3003** out. **3003** transfers the data to the CT **2912**.

[**0206**] Alternatively, (**3003** a) for transmitting the data to CT data, it is possible through an additional interface (**3004**) to one of the CT

independent bus (**3005**) to be transferred.

[**0207**] FIG. 31 shows the coupling of the array of PAEs (**3101**) with a host microcontroller. **3101** includes, all IO Channels according to the memories of the invention. The architecture operates in accordance with FIG. 23, **2912** in Fig. 31a represents the bus for the configuration data

and register data acc. Fig. 30 are available. The data bus is separately through **3104** illustrated. **3102** represents the CT, which in Fig. Also the 31a

Represents microprocessor.

[**0208**] are applicable to all bus systems independently following port models to a processor, depending on the programming model

and are chosen under consideration of price and performance:

#### 1. Register model

[**0209**] In the register model of each bus is addressed via a register that is integrated directly into the register file of the processor and

is addressed by the assembler as a register or group of registers. This model is on effizientestens if a few registers for Data exchange sufficient.

#### 2. IO Model

[**0210**] The respective bus is in the IO area of the processor. This is usually the easiest and most cost-effective option.

#### 3. shared memory model4. Shared-memory DMA model

[**0211**] processor and bus share as in the previous model the same memory. To further speed increase, there is a rapid DMA (see. Fig. 38) which takes care of the data exchange between bus and memory.

[**0212**] In order to increase the transmission time of each memory should physically separable from the remainder memory be (multiple

Memory banks), so CPU and VPU can independently access its memory.

[**0213**] In Fig. 31b a CT (assumes **3102**) while a dedicated processor (the configuration of the array, **3103**) over **3006**, the Programming model according to FIG. Guaranteed 23 by about **3006** exchanges register data with the array and over **3104** the ordinary data exchanges.

[0214] The Fig. 31c / d corresponding to Fig. 31a / b, however, for the exchange of data, a shared memory (was **3105**) **between the respective** Processor and **3101** selected.

[0215] FIG. 32 shows a circuit which allows the memory elements of the present invention in common to a memory or a Group access of memories, each single storage group is individually and uniquely addressable. For this purpose, the individual

Storage elements (**3201**) connected to a bus system, wherein each **3201** has its own bus. The bus may be bidirectional or **ausgestaltet**

be implemented by two unidirectional buses. For storage there is an address / data multiplexer which switches through a bus to memory. To

are the adjacent addresses of each bus decodes (**3207**) and thereafter a bus per unit time through an arbiter (**3208**) selected

(**3204**). The corresponding data and addresses to the respective memory bus (**3205** transmit a), wherein a state machine (**3206**)

the necessary protocols generated. Meeting at a read request data from a memory is, by the respective state machine

Address of the memory connected to the bus, the data inquired. The addresses of all incoming buses per bus of the bus system **3202**

evaluated by a multiplexer unit and transmitted to the corresponding bus. The evaluation is carried out in accordance with the evaluation of the

Output data, ie, a decoder (**3209**) per input bus (**3205** b) passes a signal to an arbiter (**3210**), which controls the data multiplexer. In order to

per unit time are different input busses on the bus system **3202** passed.

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[0216] In Fig. 33 is for more flexible and simpler evaluation of the trigger and RDY / ACK signals the rigid state machine / sequencer of rigid

**2910** by a freely programmable (**3301** replaced). The full feature of **3301** is determined by the configuration register **2913** prior to

Execution of algorithms defined by the CT. The loading of **3301** is compared with a **2911** order to manage **3301** Advanced CT Interface (**3302**) controlled. The advantage of **3301** is that much more flexible to the different trigger and RDY / ACK signals

can be dealt with, as in fixed-implemented **2910**. A disadvantage affects the size of a **3301** made.

[0217] according to a compromise which is resulting in the highest flexibility at a reasonable size, the trigger and RDY / ACK signals by a unit

**3301** evaluate and fixed all processes within the PAE by a fixed unit implemented by **2910** to control.

[0218] The PAE according to the invention for the processing of logical functions in Fig. Ready to 34. Core of the unit is below

detail described unit for linking individual signals (**3401**). About the usual registers **2901**, **2902**, **2903**, **2904**, the Bus signals with **3401** connected. The registers are added to this, a feed mode, the individual signals isochronously selectively without them

to store (register) between the buses and **3401** exchanges. The multiplexer (**3402**) and the configuration registers (**3403**) are the

different configurations of **3401** adjusted. Also, the CT-Interface (is **3404**) **adapted accordingly**.

[0219] FIG. 35 shows possible configurations of **3401**. A global data bus connects the logic cells **3501** and **3502** with the registers **2901**,

**2902**, **2903**, **2904**. Through bus switch which can be designed as a multiplexer, gates, transmission gates or single transistors **3504** with

the logic cells connected. The logic cells can be designed either completely uniform, or different functionality own (**3501**, **3502**). **3503** represents a RAM memory.

[0220] Possible Ausgestaltung the logic cells are:

- Lookup Tables - Logic - Multiplexers - Register

[0221] The selection of the functions and crosslinking can either be done flexibly programmable by SRAM cells or by unalterable ROM or semi-static FlashROM.

[0222] To speed sequential algorithms that can be bad parallelization is speculative in conventional processors

Execution already prior art. The parallel variant for VPU is in FIG. 36 is shown. The operand (**3601**) are at the same time

several possible paths of subalgorithms (3602 a, 3602 b, 3602 c) out. The Teilalgorithmen possibility to a different area and

Have time requirement. In each case according to the Part algorithms, the data are stored according to the invention (3612 a, 3612 b, 3612 c) before after

Processed reconfiguration of the next part of algorithms (3603). The Umkonfigurationszeitpunkte the individual partial algorithms are

independently, as is the number of partial algorithms themselves (3603, 3614). Once decidable, which is to choose the paths that are

the paths via a bus multiplexer or merged (3605). From a condition generated trigger signals (see FIG. PACT08) (3606 determine)

selected which of the paths, and is forwarded to the following algorithms.

[0223] FIG. 37 shows the structure of a high-level language compiler, the ordinary sequential high-level language (C, Pascal, Java) to a VPU system

translated. Sequential Code (3711) is of parallel code (3708 separately), which 3708 is processed directly in the array of PAEs.

[0224] For 3711, there are three design options:

1. Within a sequencer of a PAE (2910) 2. By using a configured in the VPU sequencer. The compiler generates this one hand, a

on the task optimized sequencer, on the other hand directly to specific algorithms Sequenzercode (see. 2801). 3. On a common

external processor (3103) Which option is selected depends on the architecture of the VPU, the computer system and the algorithm.

[0225] The Code (3701) is first in a preprocessor (3702) in Datenflußcode (3716) (in a special version of the respective Programming was written datenflußoptimiert) and ordinary sequential code separately (3717). 3717 is on parallelizable Subalgorithms examined (3703), the sequential subalgorithms be discarded (3718). The parallelizable algorithms as part Macros provisionally placed and routed.

[0226] In an iterative process the macros with the datenflußoptimierten code (be 3713) placed, routed and partitioned together

(3705). A Statistics (3706) evaluates the individual macros and their partitioning from in terms of efficiency, the reconfiguration time and

the effort of reconfiguring flows into the efficiency analysis. Inefficient macros are removed and discarded as sequential code

(3714).

[0227] The remaining parallel code (3715) is compiled with 3716 and assembled (3707) and VPU object code is output (3708).

[0228] A statistic on the efficiency of the generated code, and the individual (even with the 3714 remote macros) is output (3709)

the programmer receives by substantial evidence of speed optimizations of the program.

[0229] Each of the remaining macro-sequential codes is examined for its complexity and requirements (3720). From a database

which depends on the VPU architecture and the computer system (3719) to select the respective suitable sequencer and as VPU code (3721)

output. A compiler (3721) generates the assembly language code of the respective macros for each of 3720 sequencer selected and outputs it

(3711). The 3710 and 3720

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are closely interlinked. Optionally, the processing proceeds iteratively to the appropriate sequencer with minimal and fastest

Find assembler code.

[0230] A linker (3722) summarizes the assembler code (3708, 3711, 3721 together) and generates executable object code (3723).

[0231] FIG. 38 shows an internal structure of 2720. Core of the circuit is a loadable up / down counter (3801), the start value of his

Circuit Fig. 27 from the bus 3803 (corresponding to 2703) via the multiplexer according to set 3802 receives. The counter serves as a program counter

(PC) for the associated sequencer, the start value is the first address of the program to be executed. The value of 3801 is a

Adder (3805) and 3802 attributed to the counter. The bus 3804, an offset is from the sequencer to 3805 out of either the

Will be deducted or added PC. This relative jumps are efficiently implemented. The PC is via the bus **3811** to the PAE array drawn out and can be stored for call operations on the stack. For RET operations of the PC is about **3804** and **3802** from the stack on **3801** out.

**[0232]** The multiplexer **3806** either the PC or supplied by the PAE array stack pointer (is **3807**) to an adder (**3808**) out. Here, an offset is subtracted or added to the values of the register **3809** is stored and over **3803** is written. **3808** allows the displacement of the program within the memory 2711. This will garbage collector functions to clean up the memory possible (see. PACT10). The address shift that is occurring by the garbage collector by adjusting the offsets in **3809** compensated.

**[0233]** Fig. 38a is a variant of Fig. 38 in which the stack pointer (**3820**) is also integrated. About **3804** is only the offset for relative

Jumps to **3805** conducted (**3804** a). The stack pointer is an up / down counter in accordance with **3801**, its start value of the beginning of the stack represents, and about **3803** being charged. The PC is passed directly to the data bus to the memory via a multiplexer to call in operations

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to be written to the stack. The data bus of the memory is about **3821** and **3802** to **3801** fed back, to carry out rescue Operations.

**[0234]** FIG. 39 illustrates the operation of the memory. The memory (**3901**) is via a multiplexer (**3902** addressed). In standard mode,

Lookup mode and register mode, the address of the array (**3903**) led directly to 3,901th In stack mode and FIFO mode, the

Addresses in an up / down counter (**3904** generates). In this case, the addresses of the IO-side of a further up / down counter (be **3905**) to

Provided. The addresses for the external RAM (or IO) are a further up / down counter (**3906**) is generated, the base address is

from a register (**3907**) loaded. The register is set by the CT or an external host processor. The complete control takes a state machine (**3908**). The state of the memory (full, empty, half full, etc.) takes **3908** an up / down counter (**3909**) of the number of the

Storage located words count. If the memory blocks changed (City write on external stack, or read from an external stack) is

the size of block as a constant (**3917**) to an adder / subtractor (**3910** shown) to which the count of **3909** is fed back. That Earnings after **3909** loaded. Thus, the count can quickly adapt to changes in blocks. (Of course, it is possible to counter with every read or written word at a. To modify block operation). For cache operations is a cache controller (**3911**) according to the prior art are available, to which a tag memory (**3912**) is associated. Depending on the mode, the value of **3911** or **3906**

via a multiplexer (**3913** out) as an address to the outside (**3914**). The bus **3915** the data will be routed to the outside and the bus **3916**

the data is exchanged with the array.

Programming examples for clarification of subalgorithms

**[0235]** A module can be, for example, declared as follows:

```
module example1
input (var1, var2: ty
1
; var3: ty
2
).
Output (res1, res2: ty
3
).
begin
', '
Register <regname1> (res1).
Register <regname2> (res2).
```

terminate @ (res1 & res2; 1).

end.

modules marks the beginning of a module.

Input / Output defines the input / Ausgangsvariablen with the types ty  
n

,  
begin. , , end mark the hull of the module.

Register <regname1 / 2> returns the result to the output,

wherein the result is latched in the register specified by <regname1 / 2>. <regname1 / 2> is a global reference in a particular register.

**[0236]** For example, the following types of memory are provided as further Übergabemodi to the output available:

FIFO <fifoname>, the data is passed to an operating according to the FIFO principle storage. <fifoname> is a global reference

to a specific, working in FIFO mode memory. @ terminate is extended to include the parameters or the signal "fifofull" who / that

indicating that the memory is full.

stack <stack name>, where the data is passed to an operating according to the principle stack memory. <stack name> is a global

Reference to a specific, working in the stack mode memory.

**[0237]** terminate @ differentiates the programming in accordance with the inventive method of the conventional sequential Programming. The command defines the termination criterion of the module. The outcome variables res1 and res2 be of

@ terminate not with her

actual value evaluated, instead only the validity of the variables (ie whose status signal) tested. For this purpose, the two signals are res1

and res2 Boolean together

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linked, z. B. by an AND, OR or XOR operation. If both variables valid, terminated the module to the value 1. This means a Signal having the value 1 is transmitted to the superordinate load unit, whereupon the parent loading unit loads the subsequent modules.

Modules example2

input (var1, var2: ty

3

; var3: ty

2

)

Output (res1, ty

4

).

begin

Register <regname1> (var1, var2).

fifo <fifoname1> (res1, 256).

, , ,

terminate @ (fifofull (<fifoname1>); 1).

end.

**[0238]** register is defined in this example, via input data. Where <regname1> same as in example1. This causes the register,

which receives the output data in example1, provides the input data for example2 available.

**[0239]** FIFO defines a FIFO depth of 256 for the output data res1. The Full flag (fifofull) of the FIFO memory is in terminate @

used as termination criterion.

modules Main

input (in1, in2: ty

1

; IN3: ty

2

).

Output (OUT1: ty

4

).

```

begin
define <regname1>: register (234)
define <regname2>: Register (26).
define <fifoname1>: FIFO (256.4). // FIFO depth 256
', '
(var12, var72) = call example1 (in1, in2, in3).
', '
(out1) = call example2 (var12, var72, var243).
', '
signal (OUT1)
terminate @ (example2).

```

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end.

[0240] define defines an interface for data (register, memory, etc.). When defining the necessary resources, and the Given name of the interface. Since the resource only once available, they must be clearly identified.

So the definition is global, that is, the designation is valid for the entire program.

[0241] Call will run a module as a subroutine.

[0242] signal defines a signal as an output signal without any intermediate storage is used.

[0243] Due to terminate @ (example2) the main module is terminated as soon as the subroutine example2 terminated.

[0244] Due to the global declaration "define..." it is in principle not necessary, the so-defined input / output signals in the interface

Declaration of the modules incorporated.

A method of operating a reconfigurable unit, **characterized** in that the acknowledgment signals of configurable cells temporally

offset will be evaluated for their configuration.

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Page 65 --- (DR)  
Page 66 --- (DR)

| Electronic Patent Application Fee Transmittal      |                 |                                                                                 |               |                             |
|----------------------------------------------------|-----------------|---------------------------------------------------------------------------------|---------------|-----------------------------|
| <b>Application Number:</b>                         |                 | 14219945                                                                        |               |                             |
| <b>Filing Date:</b>                                |                 | 19-Mar-2014                                                                     |               |                             |
| <b>Title of Invention:</b>                         |                 | Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply |               |                             |
| <b>First Named Inventor/Applicant Name:</b>        |                 | Martin VORBACH                                                                  |               |                             |
| <b>Filer:</b>                                      |                 | Edward Peter Heller/Emi Rhodes                                                  |               |                             |
| <b>Attorney Docket Number:</b>                     |                 | PACT-025-PCT-US-D1-2C1-D1                                                       |               |                             |
| Filed as Large Entity                              |                 |                                                                                 |               |                             |
| <b>Filing Fees for Utility under 35 USC 111(a)</b> |                 |                                                                                 |               |                             |
| <b>Description</b>                                 | <b>Fee Code</b> | <b>Quantity</b>                                                                 | <b>Amount</b> | <b>Sub-Total in USD(\$)</b> |
| <b>Basic Filing:</b>                               |                 |                                                                                 |               |                             |
| <b>Pages:</b>                                      |                 |                                                                                 |               |                             |
| <b>Claims:</b>                                     |                 |                                                                                 |               |                             |
| <b>Miscellaneous-Filing:</b>                       |                 |                                                                                 |               |                             |
| <b>Petition:</b>                                   |                 |                                                                                 |               |                             |
| <b>Patent-Appeals-and-Interference:</b>            |                 |                                                                                 |               |                             |
| <b>Post-Allowance-and-Post-Issuance:</b>           |                 |                                                                                 |               |                             |
| <b>Extension-of-Time:</b>                          |                 |                                                                                 |               |                             |

| Description                             | Fee Code | Quantity | Amount | Sub-Total in USD(\$) |
|-----------------------------------------|----------|----------|--------|----------------------|
| <b>Miscellaneous:</b>                   |          |          |        |                      |
| Submission- Information Disclosure Stmt | 1806     | 1        | 180    | 180                  |
| <b>Total in USD (\$)</b>                |          |          |        | <b>180</b>           |

| Electronic Acknowledgement Receipt          |                                                                                 |
|---------------------------------------------|---------------------------------------------------------------------------------|
| <b>EFS ID:</b>                              | 24184760                                                                        |
| <b>Application Number:</b>                  | 14219945                                                                        |
| <b>International Application Number:</b>    |                                                                                 |
| <b>Confirmation Number:</b>                 | 7671                                                                            |
| <b>Title of Invention:</b>                  | Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply |
| <b>First Named Inventor/Applicant Name:</b> | Martin VORBACH                                                                  |
| <b>Customer Number:</b>                     | 73481                                                                           |
| <b>Filer:</b>                               | Edward Peter Heller/Emi Rhodes                                                  |
| <b>Filer Authorized By:</b>                 | Edward Peter Heller                                                             |
| <b>Attorney Docket Number:</b>              | PACT-025-PCT-US-D1-2C1-D1                                                       |
| <b>Receipt Date:</b>                        | 24-NOV-2015                                                                     |
| <b>Filing Date:</b>                         | 19-MAR-2014                                                                     |
| <b>Time Stamp:</b>                          | 17:55:27                                                                        |
| <b>Application Type:</b>                    | Utility under 35 USC 111(a)                                                     |

### Payment information:

|                                                                                                                |             |
|----------------------------------------------------------------------------------------------------------------|-------------|
| Submitted with Payment                                                                                         | yes         |
| Payment Type                                                                                                   | Credit Card |
| Payment was successfully received in RAM                                                                       | \$180       |
| RAM confirmation Number                                                                                        | 5762        |
| Deposit Account                                                                                                |             |
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| The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: |             |

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|------------------------------|----------------------------------------------------|---------------------------------------------------------------------|------------------------------------------|------------------|------------------|
|                              |                                                    |                                                                     |                                          |                  |                  |
| File Listing:                |                                                    |                                                                     |                                          |                  |                  |
| Document Number              | Document Description                               | File Name                                                           | File Size(Bytes)/ Message Digest         | Multi Part /.zip | Pages (if appl.) |
| 1                            | Information Disclosure Statement (IDS) Form (SB08) | PACT-025-PCT-US-D1-2C1-D1_151124_IDS_SB08a.pdf                      | 613284                                   | no               | 7                |
|                              |                                                    |                                                                     | 3560ac18d6d2200a5d37d00f98f4a35e2eed54b9 |                  |                  |
| Warnings:                    |                                                    |                                                                     |                                          |                  |                  |
| Information:                 |                                                    |                                                                     |                                          |                  |                  |
| 2                            | Non Patent Literature                              | Altera_FLEX10K_Embedded_Programmable_Logic_Family_DS.pdf            | 673742                                   | no               | 21               |
|                              |                                                    |                                                                     | cbc493361b2f17591fe6a3a0cde125258329fe5e |                  |                  |
| Warnings:                    |                                                    |                                                                     |                                          |                  |                  |
| Information:                 |                                                    |                                                                     |                                          |                  |                  |
| 3                            | Non Patent Literature                              | Hauser_John_AugmentingAMicroprocessorwithReconfigurableHardware.pdf | 9572145                                  | no               | 255              |
|                              |                                                    |                                                                     | 6eb7e8419e69de818a057499c9298d590cc9d3cb |                  |                  |
| Warnings:                    |                                                    |                                                                     |                                          |                  |                  |
| Information:                 |                                                    |                                                                     |                                          |                  |                  |
| 4                            | Non Patent Literature                              | Silberschatz_Operating_System_Concepts.pdf                          | 4989235                                  | no               | 31               |
|                              |                                                    |                                                                     | 5ba3a6be7f6d97ce34d6067e88d699fbc62e48c7 |                  |                  |
| Warnings:                    |                                                    |                                                                     |                                          |                  |                  |
| Information:                 |                                                    |                                                                     |                                          |                  |                  |
| 5                            | Foreign Reference                                  | DE10028397A1.pdf                                                    | 2842196                                  | no               | 66               |
|                              |                                                    |                                                                     | 505dd8661acfdb06815507d3931faa85ef5eb0af |                  |                  |
| Warnings:                    |                                                    |                                                                     |                                          |                  |                  |
| Information:                 |                                                    |                                                                     |                                          |                  |                  |
| 6                            | Foreign Reference                                  | DE000010028397A1_EnglishTranslation.pdf                             | 312648                                   | no               | 27               |
|                              |                                                    |                                                                     | db220757f026407cb6cf054358e6e1232f4215f  |                  |                  |
| Warnings:                    |                                                    |                                                                     |                                          |                  |                  |
| Information:                 |                                                    |                                                                     |                                          |                  |                  |
| 7                            | Fee Worksheet (SB06)                               | fee-info.pdf                                                        | 30773                                    | no               | 2                |
|                              |                                                    |                                                                     | 4f9cf3b91d65913078a9f43a7a11819c0811c7c2 |                  |                  |
| Warnings:                    |                                                    |                                                                     |                                          |                  |                  |
| Information:                 |                                                    |                                                                     |                                          |                  |                  |
| Total Files Size (in bytes): |                                                    |                                                                     | 19034023                                 |                  |                  |

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**New Applications Under 35 U.S.C. 111**

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

**National Stage of an International Application under 35 U.S.C. 371**

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

**New International Application Filed with the USPTO as a Receiving Office**

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.



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| APPLICATION NO.                                                                           | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.              | CONFIRMATION NO.            |
|-------------------------------------------------------------------------------------------|-------------|----------------------|----------------------------------|-----------------------------|
| 14/219,945                                                                                | 03/19/2014  | Martin VORBACH       | PACT-025-PCT-US-D1-2C1-D1        | 7671                        |
| 73481                                                                                     | 7590        | 05/16/2016           |                                  |                             |
| Alliacense Limited LLC<br>4880 Stevens Creek Boulevard<br>Suite 103<br>San Jose, CA 95129 |             |                      | EXAMINER<br>ELAMIN, ABDELMONIE M |                             |
|                                                                                           |             |                      | ART UNIT<br>2116                 | PAPER NUMBER                |
|                                                                                           |             |                      | NOTIFICATION DATE<br>05/16/2016  | DELIVERY MODE<br>ELECTRONIC |

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

emi@alliacense.com  
ip@alliacense.com  
ned@alliacense.com

|                              |                                       |                                       |                                                  |
|------------------------------|---------------------------------------|---------------------------------------|--------------------------------------------------|
| <b>Office Action Summary</b> | <b>Application No.</b><br>14/219,945  | <b>Applicant(s)</b><br>VORBACH ET AL. |                                                  |
|                              | <b>Examiner</b><br>Abdelmoniem ELAMIN | <b>Art Unit</b><br>2116               | <b>AIA (First Inventor to File) Status</b><br>No |

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --**

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1) ☒ Responsive to communication(s) filed on 03/19/2014.  
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on \_\_\_\_.

2a) ☐ This action is **FINAL**.                      2b) ☒ This action is non-final.

3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on \_\_\_\_; the restriction requirement and election have been incorporated into this action.

4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims\***

5) ☒ Claim(s) 2-46 is/are pending in the application.  
5a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.

6) ☐ Claim(s) \_\_\_\_ is/are allowed.

7) ☒ Claim(s) 2-46 is/are rejected.

8) ☐ Claim(s) \_\_\_\_ is/are objected to.

9) ☐ Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

\* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see [http://www.uspto.gov/patents/init\\_events/pph/index.jsp](http://www.uspto.gov/patents/init_events/pph/index.jsp) or send an inquiry to [PPHfeedback@uspto.gov](mailto:PPHfeedback@uspto.gov).

**Application Papers**

10) ☐ The specification is objected to by the Examiner.

11) ☐ The drawing(s) filed on \_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

**Priority under 35 U.S.C. § 119**

12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

**Certified copies:**

a) ☒ All    b) ☐ Some\*\*    c) ☐ None of the:

1. ☐ Certified copies of the priority documents have been received.
2. ☒ Certified copies of the priority documents have been received in Application No. 10/469,909.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\*\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)

2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)  
Paper No(s)/Mail Date 04/03/2015; 05/15/2015; 07/15/2015; 11/24/2015.

3) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.

4) ☐ Other: \_\_\_\_.

### DETAILED ACTION

1. The present application is being examined under the pre-AIA first to invent provisions.

#### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of pre-AIA 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 2-46 are rejected under pre-AIA 35 U.S.C. 102(b) as being anticipated by Kikinis, US. Pat. No. 5,502,838.

4. Claims 2, 20-22, 34-35, 41-43, 45-46, Kikinis teaches a multiprocessor system comprising:

a plurality of data processing units [*see Figs 4 and 5*], each of the data processing units:

(a) being programmable [*abstract, see also Figs 4-5 and related disclosure*]; and

(b) being adaptable for sequentially processing data in a clocked manner [*controller 65 of fig. 4 allocates workload between processors*]; and including

(c1) at least one Arithmetic Logic Unit (ALU) [*inherent*] and

(c2) at least one data register set, for storing intermediate results in sequential data processing at least one bus system for at least interconnecting at least some of the data processing units, each being provided a supply voltage by a voltage supply [*abstract, see also Figs 4-5 and related disclosure*];

wherein for at least some of the data processing units, the clock frequency is adjustable at runtime without affecting the clock frequency of at least one of: one other of

the data processing units and the bus system [*each processor is provided with individual operational clock rate, see Fig. 2*]; and

wherein the voltage supply is adapted to supply higher supply voltages for data processing at higher clock frequencies [*the operating voltage to each functional circuit is adjusted as a function of the altered clock rate, see claim 10 of Kikinis*].

5. Claims 3, 33, 36, Kikinis teaches for at least some of the data processing units, the clock frequency is adjustable at runtime according to a state of the multiprocessor system [*abstract, col. 3, lines 34-41*].
6. Claims 4, 37, Kikinis teaches for at least some of the data processing units, the clock frequency is adjustable at runtime according to a state of the data processing entity [*abstract, col. 3, lines 34-41*].
7. Claims 5, 38, Kikinis teaches for at least some of the data processing units, the clock frequency is adjustable at runtime according to a state of others of the data processing units [*see Fig. 3, col. 4, lines 23-40*].
8. Claims 6, 23, 39, Kikinis teaches for at least some of the data processing units, the clock frequency is adjustable at runtime according to a priority of a sequential task [*col. 5, lines 14-24*].
9. Claims 7, 24, 40, Kikinis teaches the processor is adapted to reduce the supply voltage when the clock frequency is reduced [*operating voltage is lowered as operating frequency is lowered, see abstract*].
10. Claims 8, 44, Kikinis teaches subsequently reduce the clock frequency in accordance with a hysteresis characteristics [*abstract*].

11. Claims 9, 25, Kikinis teaches a heterogeneous plurality of clocked data processing units [*see Fig.4 and related disclosure*].
12. Claims 10, Kikinis teaches subsequently reduce the clock frequency in accordance with a hysteresis characteristics [*abstract*].
13. Claims 11-12, 26, Kikinis teaches a plurality of temperature sensors and a heterogeneous plurality of clocked data processing units, the multiprocessor having a plurality of regions, a temperature sensor being provided for each of said plurality of regions to measure the temperature of said specific region; and the clock frequencies of said data processing units being dynamically adjustable in accordance with the sensed temperatures [*each microprocessor package has a temperature sensor mounted in a manner to sense the temperature of each individual microprocessor package, see col. 5, lines 5-23*].
14. Claims 13, 27, Kikinis teaches (i) setting a clock frequency of at least a part of the multiprocessor system to a value in accordance with a first processor load, the value being less than a maximum value [*abstract, col. 5, lines 43-52*]; (ii) subsequently increasing the clock frequency of the at least the part of the multiprocessor system to a maximum in accordance with a second processor load [*see Fig. 6, col. 4, lines 33-40*]; and (iii) subsequently reducing the clock frequency of the at least the part of the multiprocessor system in accordance with an operating temperature threshold for preventing over temperature [*see step 111 of Fig. 6, col. 4, lines 33-40*].
15. Claims 14, 28, Kikinis teaches subsequently reduce the clock frequency in accordance with a hysteresis characteristics [*abstract*].

16. Claims 15, 28, 29, Kikinis teaches a low power operation mode is provided such that a first data processing unit is active while a plurality of other data processing units are deactivated [see col. 6, line 62 thru col. 7, line 2].
17. Claims 16, 30, Kikinis teaches the first data processing unit is adapted to activate at least some of the other data processing units for data processing in response to an event [see col. 6, line 62 thru col. 7, line 2].
18. Claims 17, 31, Kikinis teaches in the low power mode the minimum clock rate of the plurality of other units is set in accordance clock rate necessary for preserving the memory contents [inherent].
19. Claims 18, 32, Kikinis teaches selectively set the clock frequency of at least some of the processing units in response to a prioritization of a task assigned [each processor is provided with individual operational clock rate, see Fig. 2].
20. Claims 19, the plurality of data processing units are disposed within a mobile device [see Figs 4 and 5].

### ***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abdelmoniem ELAMIN whose telephone number is (571)272-3674. The examiner can normally be reached on MON - FRI 10:00 AM - 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Abdelmoniem Elamin/  
Primary Examiner, Art Unit 2116  
May 11, 2016

|                                   |                                       |                                                              |             |
|-----------------------------------|---------------------------------------|--------------------------------------------------------------|-------------|
| <b>Notice of References Cited</b> | Application/Control No.<br>14/219,945 | Applicant(s)/Patent Under<br>Reexamination<br>VORBACH ET AL. |             |
|                                   | Examiner<br>Abdelmoniem ELAMIN        | Art Unit<br>2116                                             | Page 1 of 1 |

**U.S. PATENT DOCUMENTS**

| * |   | Document Number<br>Country Code-Number-Kind Code | Date<br>MM-YYYY | Name             | CPC Classification | US Classification |
|---|---|--------------------------------------------------|-----------------|------------------|--------------------|-------------------|
| * | A | US-7,100,061 B2                                  | 08-2006         | Halepete; Sameer | G06F1/08           | 713/322           |
| * | B | US-5,502,838 A                                   | 03-1996         | Kikinis; Dan     | G05D23/1919        | 713/501           |
|   | C | US-                                              |                 |                  |                    |                   |
|   | D | US-                                              |                 |                  |                    |                   |
|   | E | US-                                              |                 |                  |                    |                   |
|   | F | US-                                              |                 |                  |                    |                   |
|   | G | US-                                              |                 |                  |                    |                   |
|   | H | US-                                              |                 |                  |                    |                   |
|   | I | US-                                              |                 |                  |                    |                   |
|   | J | US-                                              |                 |                  |                    |                   |
|   | K | US-                                              |                 |                  |                    |                   |
|   | L | US-                                              |                 |                  |                    |                   |
|   | M | US-                                              |                 |                  |                    |                   |

**FOREIGN PATENT DOCUMENTS**

| * |   | Document Number<br>Country Code-Number-Kind Code | Date<br>MM-YYYY | Country | Name | CPC Classification |
|---|---|--------------------------------------------------|-----------------|---------|------|--------------------|
|   | N |                                                  |                 |         |      |                    |
|   | O |                                                  |                 |         |      |                    |
|   | P |                                                  |                 |         |      |                    |
|   | Q |                                                  |                 |         |      |                    |
|   | R |                                                  |                 |         |      |                    |
|   | S |                                                  |                 |         |      |                    |
|   | T |                                                  |                 |         |      |                    |

**NON-PATENT DOCUMENTS**

| * |   | Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages) |
|---|---|-------------------------------------------------------------------------------------------|
|   | U |                                                                                           |
|   | V |                                                                                           |
|   | W |                                                                                           |
|   | X |                                                                                           |

\*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)  
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office  
PTO-892 (Rev. 01-2001)  
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**Notice of References Cited**

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## BIB DATA SHEET

CONFIRMATION NO. 7671

| SERIAL NUMBER                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | FILING or 371(c)<br>DATE | CLASS | GROUP ART UNIT | ATTORNEY DOCKET<br>NO. |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|-------|----------------|------------------------|
| 14/219,945                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 03/19/2014               | 713   | 2116 PACT      | 025-PCT-US-D1-2C-D1    |
| <b>APPLICANTS</b><br>PACT XPP TECHNOLOGIES AG, Munich, GERMANY;<br><b>INVENTORS</b><br>Martin VORBACH, Munchen, GERMANY;<br>Volker BAUMGARTE, Munchen, GERMANY;<br><b>** CONTINUING DATA *****</b><br>This application is a DIV of 13/653,639 10/17/2012 PAT 9075605<br>which is a CON of 12/570,984 09/30/2009 PAT 8312301<br>which is a CON of 12/257,075 10/23/2008 PAT 8099618<br>which is a DIV of 10/469,909 09/21/2004 PAT 7444531<br>which is a 371 of PCT/EP02/02402 03/05/2002<br><b>** FOREIGN APPLICATIONS *****</b><br>GERMANY 101 10 530.4 03/05/2001<br>GERMANY 101 11 014.6 03/07/2001<br>GERMANY 101 29 237.6 06/20/2001<br>GERMANY 101 35 210.7 07/24/2001<br>GERMANY 101 35 211.5 07/24/2001<br>GERMANY 101 39 170.6 08/16/2001<br>GERMANY 101 42 231.8 08/29/2001<br>GERMANY 101 42 894.4 09/03/2001<br>GERMANY 101 42 903.7 09/03/2001<br>GERMANY 101 42 904.5 09/03/2001<br>GERMANY 101 44 732.9 09/11/2001<br>GERMANY 101 44 733.7 09/11/2001<br>GERMANY 101 45 792.8 09/17/2001<br>GERMANY 101 45 795.2 09/17/2001<br>GERMANY 101 46 132.1 09/19/2001<br>GERMANY 101 54 260.7 11/05/2001<br>GERMANY 101 54 259.3 11/05/2001<br>GERMANY 102 02 044.2 01/19/2002<br>GERMANY 102 02 175.9 01/20/2002<br>GERMANY 102 06 653.1 02/15/2002<br>GERMANY 102 06 857.7 02/18/2002<br>GERMANY 102 06 856.9 02/18/2002<br>GERMANY 102 07 226.4 02/21/2002<br>GERMANY 102 07 224.8 02/21/2002<br>GERMANY 102 07 225.6 02/21/2002<br>GERMANY 102 08 435.1 02/27/2002<br>GERMANY 102 08 434.3 02/27/2002<br>EUROPEAN PATENT OFFICE (EPO) 1115021.6 06/20/2001<br>EUROPEAN PATENT OFFICE (EPO) 1129923.7 12/14/2001<br>EUROPEAN PATENT OFFICE (EPO) 2001331.4 01/18/2002<br>EUROPEAN PATENT OFFICE (EPO) PCT/EP01/06703 06/13/2001 |                          |       |                |                        |

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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.E./

| U.S. PATENTS      |         |               |                        |            |                                                 | Remove                                                                   |
|-------------------|---------|---------------|------------------------|------------|-------------------------------------------------|--------------------------------------------------------------------------|
| Examiner Initial* | Cite No | Patent Number | Kind Code <sup>1</sup> | Issue Date | Name of Patentee or Applicant of cited Document | Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear |
|                   | 1       | US347316      | A                      | 1969-10-14 | Wahlstrom et al.                                |                                                                          |
|                   | 2       | US353166      | A                      | 1970-09-29 | Spandorfer et al.                               |                                                                          |
|                   | 3       | 4020469       |                        | 1977-04-26 | Manning                                         |                                                                          |
|                   | 4       | 4642487       |                        | 1987-02-10 | Carter                                          |                                                                          |
|                   | 5       | 4700187       |                        | 1987-10-13 | Furtek                                          |                                                                          |
|                   | 6       | 4706216       |                        | 1987-11-10 | Carter                                          |                                                                          |
|                   | 7       | 4722084       |                        | 1988-01-26 | Morton                                          |                                                                          |
|                   | 8       | 4724307       |                        | 1988-02-09 | Dutton et al.                                   |                                                                          |

|                                                                                                     |                        |                           |            |
|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |                           | 14219945   |
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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |

|  |    |         |  |            |                   |  |
|--|----|---------|--|------------|-------------------|--|
|  | 9  | 4758985 |  | 1988-07-19 | Carter            |  |
|  | 10 | 4768196 |  | 1988-08-30 | Jou et al.        |  |
|  | 11 | 4786904 |  | 1988-11-22 | Graham III et al. |  |
|  | 12 | 4791603 |  | 1988-12-13 | Henry             |  |
|  | 13 | 4918440 |  | 1990-04-17 | Furtek            |  |
|  | 14 | 5036473 |  | 1991-07-30 | Butts et al.      |  |
|  | 15 | 5055997 |  | 1991-10-08 | Sluijter et al.   |  |
|  | 16 | 5103311 |  | 1992-04-07 | Sluijter et al.   |  |
|  | 17 | 5113498 |  | 1992-05-12 | Evan et al.       |  |
|  | 18 | 5123109 |  | 1992-06-16 | Hillis            |  |
|  | 19 | 5144166 |  | 1992-09-01 | Camarota et al.   |  |

|                                                                                                     |                        |                           |            |
|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |                           | 14219945   |
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|                                                                                                     | Art Unit               | 2116                      |            |
|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |            |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |

|  |    |         |  |            |                     |  |
|--|----|---------|--|------------|---------------------|--|
|  | 20 | 5212777 |  | 1993-05-18 | Gove et al.         |  |
|  | 21 | 5243238 |  | 1993-09-07 | Kean                |  |
|  | 22 | 5245227 |  | 1993-09-14 | Furtek et al.       |  |
|  | 23 | 5287511 |  | 1994-02-15 | Robinson et al.     |  |
|  | 24 | 5296759 |  | 1994-03-22 | Sutherland et al.   |  |
|  | 25 | 5298805 |  | 1994-03-29 | Garverick et al.    |  |
|  | 26 | 5336950 |  | 1994-08-09 | Popli et al.        |  |
|  | 27 | 5355508 |  | 1994-10-11 | Kan                 |  |
|  | 28 | 5357152 |  | 1994-10-18 | Jennings III et al. |  |
|  | 29 | 5361373 |  | 1994-11-01 | Gilson              |  |
|  | 30 | 5386154 |  | 1995-01-31 | Goetting et al.     |  |

|                                                                                                     |                        |                           |
|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     | 14219945                  |
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|                                                                                                     | Art Unit               | 2116                      |
|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |

|  |    |         |  |            |                     |  |
|--|----|---------|--|------------|---------------------|--|
|  | 31 | 5386518 |  | 1995-01-31 | Reagle et al.       |  |
|  | 32 | 5394030 |  | 1995-02-28 | Jennings III et al. |  |
|  | 33 | 5408129 |  | 1995-04-18 | Farmwald et al.     |  |
|  | 34 | 5410723 |  | 1995-04-25 | Schmidt et al.      |  |
|  | 35 | 5412795 |  | 1995-05-02 | Larson              |  |
|  | 36 | 5421019 |  | 1995-05-30 | Holsztynski et al.  |  |
|  | 37 | 5426378 |  | 1995-06-20 | Ong                 |  |
|  | 38 | 5440711 |  | 1995-08-08 | Sugimoto            |  |
|  | 39 | 5448496 |  | 1995-08-08 | Butts et al.        |  |
|  | 40 | 5469003 |  | 1995-11-21 | Kean                |  |
|  | 41 | 5488582 |  | 1996-01-30 | Camarota            |  |

|                                                                                                     |                        |                           |            |  |
|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|--|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |                           | 14219945   |  |
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|                                                                                                     | Art Unit               | 2116                      |            |  |
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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |  |

|  |    |         |  |            |                      |  |
|--|----|---------|--|------------|----------------------|--|
|  | 42 | 5500609 |  | 1996-03-19 | Kean                 |  |
|  | 43 | 5504439 |  | 1996-04-02 | Tavana               |  |
|  | 44 | 5525971 |  | 1996-06-11 | Flynn                |  |
|  | 45 | 5574930 |  | 1996-11-12 | Halverson Jr. et al. |  |
|  | 46 | 5596743 |  | 1997-01-21 | Bhat et al.          |  |
|  | 47 | 5600597 |  | 1997-02-04 | Kean et al.          |  |
|  | 48 | 5608342 |  | 1997-03-04 | Trimberger           |  |
|  | 49 | 5619720 |  | 1997-04-08 | Garde et al.         |  |
|  | 50 | 5625836 |  | 1997-04-29 | Barker et al.        |  |
|  | 51 | 5631578 |  | 1997-05-20 | Clinton et al.       |  |
|  | 52 | 5635851 |  | 1997-06-03 | Tavana               |  |

|                                                                                                     |                        |                           |
|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|
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|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |

|  |    |         |  |            |                   |  |
|--|----|---------|--|------------|-------------------|--|
|  | 53 | 5642058 |  | 1997-06-24 | Trimberger et al. |  |
|  | 54 | 5646544 |  | 1997-07-08 | Iadanza           |  |
|  | 55 | 5646546 |  | 1997-07-08 | Bertolet et al.   |  |
|  | 56 | 5652529 |  | 1997-07-29 | Gould et al.      |  |
|  | 57 | 5656950 |  | 1997-08-12 | Duong et al.      |  |
|  | 58 | 5659785 |  | 1997-08-19 | Pechanek et al.   |  |
|  | 59 | 5671432 |  | 1997-09-23 | Bertolet et al.   |  |
|  | 60 | 5675262 |  | 1997-10-07 | Duong et al.      |  |
|  | 61 | 5682491 |  | 1997-10-28 | Pechanek et al.   |  |
|  | 62 | 5687325 |  | 1997-11-11 | Chang             |  |
|  | 63 | 5696976 |  | 1997-12-09 | Nizar et al.      |  |

|                                                                                                     |                        |                           |            |
|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |                           | 14219945   |
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|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |            |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |

|  |    |         |  |            |                   |  |
|--|----|---------|--|------------|-------------------|--|
|  | 64 | 5701091 |  | 1997-12-23 | Kean              |  |
|  | 65 | 5705938 |  | 1998-01-06 | Kean              |  |
|  | 66 | 5715476 |  | 1998-02-03 | Kundu et al.      |  |
|  | 67 | 5734869 |  | 1998-03-31 | Chen              |  |
|  | 68 | 5742180 |  | 1998-04-21 | DeHon et al.      |  |
|  | 69 | 5748979 |  | 1998-05-05 | Trimberger        |  |
|  | 70 | 5752035 |  | 1998-05-12 | Trimberger        |  |
|  | 71 | 5761484 |  | 1998-06-02 | Agarwal et al.    |  |
|  | 72 | 5778439 |  | 1998-07-07 | Trimberger et al. |  |
|  | 73 | 5781756 |  | 1998-07-14 | Hung              |  |
|  | 74 | 5805477 |  | 1998-09-08 | Perner            |  |

|                                                                                                     |                        |                           |
|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|
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|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |

|  |    |         |  |            |                   |  |
|--|----|---------|--|------------|-------------------|--|
|  | 75 | 5815004 |  | 1998-09-29 | Trimberger et al. |  |
|  | 76 | 5828858 |  | 1998-10-27 | Athanas et al.    |  |
|  | 77 | 5857109 |  | 1999-01-05 | Taylor            |  |
|  | 78 | 5894565 |  | 1999-04-13 | Furtek et al.     |  |
|  | 79 | 5943242 |  | 1999-08-24 | Vorbach et al.    |  |
|  | 80 | 5956518 |  | 1999-09-21 | DeHon et al.      |  |
|  | 81 | 6011407 |  | 2000-01-04 | New               |  |
|  | 82 | 6023564 |  | 2000-02-08 | Trimberger        |  |
|  | 83 | 6052773 |  | 2000-04-18 | DeHon et al.      |  |
|  | 84 | 6128720 |  | 2000-10-03 | Pechanek et al.   |  |
|  | 85 | 6145072 |  | 2000-11-07 | Shams et al.      |  |

|                                                                                                     |                        |                           |            |  |
|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|--|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |                           | 14219945   |  |
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|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |            |  |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |  |

|  |    |         |  |            |                 |  |
|--|----|---------|--|------------|-----------------|--|
|  | 86 | 6178494 |  | 2001-01-23 | Casselman       |  |
|  | 87 | 6247036 |  | 2001-06-12 | Landers et al.  |  |
|  | 88 | 6405185 |  | 2002-06-11 | Pechanek et al. |  |
|  | 89 | 6526461 |  | 2003-02-25 | Cliff           |  |
|  | 90 | RE34444 |  | 1993-11-16 | Kaplinsky       |  |

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|-------------------|---------|--------------------------------------|---------------------------|------------------------|------------------|-------------------------------------------------|------------------------------------------------------------------------|--------------------------|
|                   | 1       | DE4416881                            | DE                        | A1                     | 1994-11-17       | Vorbach et al.                                  |                                                                        | <input type="checkbox"/> |

|                                                                                                     |                        |                           |            |  |
|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|--|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |                           | 14219945   |  |
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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |  |

|  |   |              |    |  |            |    |  |                          |
|--|---|--------------|----|--|------------|----|--|--------------------------|
|  | 2 | WO1995028671 | WO |  | 1995-10-26 | Du |  | <input type="checkbox"/> |
|  | 3 |              |    |  |            |    |  | <input type="checkbox"/> |

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|                                 | 1       | File History of U.S. Application No. 08/388,230                                                                                                                                                                                                                 |  |  |  |  |  | <input type="checkbox"/> |
|                                 | 2       | File History of U.S. Provisional Application No. 60/010,317                                                                                                                                                                                                     |  |  |  |  |  | <input type="checkbox"/> |
|                                 | 3       | File History of U.S. Provisional Application No. 60/022,131                                                                                                                                                                                                     |  |  |  |  |  | <input type="checkbox"/> |
|                                 | 4       | Chan, Pak K. , "A Field-Programmable Prototyping Board: XC4000 BORG User's Guide", University of California, Santa Cruz (Apr. 1994) .                                                                                                                           |  |  |  |  |  | <input type="checkbox"/> |
|                                 | 5       | Schewel, John , "A Hardware/Software Co-Design System Using Configurable Computing Technology".                                                                                                                                                                 |  |  |  |  |  | <input type="checkbox"/> |
|                                 | 6       | Hartenstein, Reiner W. et al. , "A New FPGA Architecture for Word-Oriented Datapaths", Lecture Notes in Computer Science, Vol. 849 (1994).                                                                                                                      |  |  |  |  |  | <input type="checkbox"/> |
|                                 | 7       | Knittel, Guntar , "A PCI-Compatible FPGA-Coprocessor for 2D/3D Image Processing", IEEE 1996.                                                                                                                                                                    |  |  |  |  |  | <input type="checkbox"/> |

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.E./

|                                                                                                     |                        |                           |
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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |

|    |                                                                                                                                                                                 |                          |
|----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|
| 8  | Schue, Rick , "A Simple DRAM Controller for 25/16 MHz i960® CA/CF Microprocessors", Intel Corporation, Application Note AP-704 (Feb. 20, 1995).                                 | <input type="checkbox"/> |
| 9  | Alfke, Peter and New, Bernie , "Additional XC3000 Data", Xilinx, Inc., Xilinx Application Note, XAPP024.000 (1994).                                                             | <input type="checkbox"/> |
| 10 | Altera Corporation , "Altera 1996 Data Book", Altera Corporation (June 1996).                                                                                                   | <input type="checkbox"/> |
| 11 | Altera Corporation , "Altera Applications Handbook", Altera Corporation (Apr. 1992).                                                                                            | <input type="checkbox"/> |
| 12 | Electronic Engineering , "Altera puts memory into its FLEX PLDs", Electronic Engineering Times, Issue 840, March 20, 1995.                                                      | <input type="checkbox"/> |
| 13 | ARM , "AMBA: Advanced Microcontroller Bus Architecture Specification", Advanced RISC Machines, Ltd., Document No. ARM IHI 0001C, Sep. 1995.                                     | <input type="checkbox"/> |
| 14 | Margolus, Norman , "An FPGA architecture for DRAM-based systolic computations", The 5th Annual IEEE Symposium on Field-Programmable Custom Computing Machines (April 16, 1997). | <input type="checkbox"/> |
| 15 | Krishnamohan, K. , "Applying Rambus Technology to Desktop Computer Main Memory Subsystems, Version 1.0", Rambus Inc. (Mar. 1992).                                               | <input type="checkbox"/> |
| 16 | New, Bernie , "Boundary-Scan Emulator for XC3000", Xilinx, Inc., Xilinx Application Note, XAPP007.001 (1994).                                                                   | <input type="checkbox"/> |
| 17 | New, Bernie , "Bus-Structured Serial Input/Output Device", Xilinx Application Note, XAPP010.001 (1994).                                                                         | <input type="checkbox"/> |
| 18 | Berkeley Design Technology Group , "Buyer's Guide to DSP Processors", Berkeley Design Technology Group (1995).                                                                  | <input type="checkbox"/> |

|                                                                                                     |                        |                           |
|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     | 14219945                  |
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|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |

|    |                                                                                                                                                                                |                          |
|----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|
| 19 | Algotronix, Ltd. , "CAL 4096 Datasheet", Algotronix, Ltd. (1992).                                                                                                              | <input type="checkbox"/> |
| 20 | Algotronix, Ltd. , "CAL 64K Datasheet", Algotronix, Ltd. (Apr. 6, 1989).                                                                                                       | <input type="checkbox"/> |
| 21 | Algotronix, Ltd. , "CHS2x4 User Manual", Algotronix, Ltd. (1991).                                                                                                              | <input type="checkbox"/> |
| 22 | Altera Corporation , "ClockLock & ClockBoost Circuitry for High-Density PLDS", The Altera Advantage News & Views, Newsletter for Altera Customers, Third Quarter, August 1996. | <input type="checkbox"/> |
| 23 | Altera Corporation , "Configuring FLEX 10K Devices", Altera Corporation, December 1995, ver. 1, Application Note 59.                                                           | <input type="checkbox"/> |
| 24 | Schmidt, Ulrich, and Knut, Cesar, "Datawave: A Single-Chip Multiprocessor for Video Applications", IEEE Micro (1991).                                                          | <input type="checkbox"/> |
| 25 | Electronic Design, "Embedded Configurable Memory and Logic Boost FPGA Functionality", Electronic Design, Volume 43, Number 14, July 10, 1995.                                  | <input type="checkbox"/> |
| 26 | Xilinx, Inc., "Fully Compliant PCI Interface in an XC3164A-2 FPGA", Xilinx, Inc. Application Note (Jan. 1995).                                                                 | <input type="checkbox"/> |
| 27 | Epstein, Dave, "IBM Extends DSP Performance with Mfast", Microprocessor Reports, Vol. 9, No. 16 (Dec. 4, 1995).                                                                | <input type="checkbox"/> |
| 28 | IEEE, "IEEE Standard Test Access Port and Boundary-Scan Architecture", IEEE Std 1149.1 Approved February 15, 1990.                                                             | <input type="checkbox"/> |
| 29 | Alfke, Peter and New, Bernie, "Implementing State Machines in LCA Devices", Xilinx, Inc., Xilinx Application Note, XAPP027.001 (1994).                                         | <input type="checkbox"/> |

|                                                                                                     |                        |                           |            |
|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |                           | 14219945   |
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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |

|  |    |                                                                                                                                                                              |                          |
|--|----|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|
|  | 30 | Camilleri, Nick, and Lockhard, Chris, "Improving XC4000 Design Performance", Xilinx Application Note, XAPP043.000 (1994).                                                    | <input type="checkbox"/> |
|  | 31 | Intel Corporation, "Intel 82375EB/82375SB PCI-EISA Bridge (PCEB) Advance Information", Intel Corporation (Mar. 1996).                                                        | <input type="checkbox"/> |
|  | 32 | Wilkie, Bill, "Interfacing XC6200 to Microprocessors (MC68020 Example)", Xilinx Application Note, XAPP 063, v. 1.1 (Oct. 9, 1996).                                           | <input type="checkbox"/> |
|  | 33 | Wilkie, Bill, "Interfacing XC6200 To Microprocessors (TMS320C50 Example)", Xilinx Application Note, XAPP064 (Oct. 9, 1996).                                                  | <input type="checkbox"/> |
|  | 34 | XCELL, "Introducing the XC6200 FPGA Architecture: The First FPGA Architecture Optimized for Coprocessing in Embedded System Applications", XCELL, Iss. 18, 3d Quarter, 1995. | <input type="checkbox"/> |
|  | 35 | Altera Corporation, "JTAG Boundary – Scan Testing in Altera Devices", Altera Corporation, November 1995, ver. 3, Application Note 39.                                        | <input type="checkbox"/> |
|  | 36 | Margolus, Norman, "Large-scale logic-array computation", Boston University Center for Computational Science, SPIE Vol. 2914 (May 1996).                                      | <input type="checkbox"/> |
|  | 37 | Alfke, Peter , "Megabit FIFO in Two Chips: One LCA Device and One DRAM", Xilinx Application Note, XAPP030.000 (1994).                                                        | <input type="checkbox"/> |
|  | 38 | del Corso, D. et al. , "Microcomputer Buses and Links", Academic Press (1996).                                                                                               | <input type="checkbox"/> |
|  | 39 | Bakkes, P.J. and du Plessis, J.J. , "Mixed Fixed and Reconfigurable Logic for Array Processing", IEEE (1996).                                                                | <input type="checkbox"/> |
|  | 40 | Altera Corporation , "PCI Bus Applications in Altera Devices", Altera Corporation, April 1995, ver. 1, Application Note 41.                                                  | <input type="checkbox"/> |

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|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |                           | 14219945   |
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|  |    |                                                                                                                       |                          |
|--|----|-----------------------------------------------------------------------------------------------------------------------|--------------------------|
|  | 41 | Altera Corporation , "PCI Bus Target Megafunction", Altera Corporation, Solution Brief 6, ver. 1, November 1996.      | <input type="checkbox"/> |
|  | 42 | Altera Corporation , "PCI Compliance of Altera Devices", Altera Corporation, May 1995, ver. 2, Application Brief 140. | <input type="checkbox"/> |
|  | 43 | SIG , "PCI Local Bus Specification", PCI Special Interest Group, Production Version, Revision 2.1 (June 1, 1995).     | <input type="checkbox"/> |
|  | 44 | Rambus Inc. , "Rambus Architectural Overview", Rambus Inc. (1992).                                                    | <input type="checkbox"/> |
|  | 45 | Rambus Inc. , "Rambus FPGA Proposal", Rambus Inc. (Jan. 4, 1994).                                                     | <input type="checkbox"/> |
|  | 46 | Rambus Inc. , "Rambus Product Catalog", Rambus Inc. (1993).                                                           | <input type="checkbox"/> |
|  | 47 | Xilinx, Inc. , "Series 6000 User Guide", Xilinx, Inc. (1997).                                                         | <input type="checkbox"/> |
|  | 48 | Cartier, Lois , "System Design with New XC4000EX I/O Features", Xilinx Application Note, XAPP056 (Feb.21, 1996).      | <input type="checkbox"/> |
|  | 49 | Xilinx, Inc. , "Technical Data - XC5200 Logic Cell Array Family, Preliminary, v.1.0", Xilinx, Inc., (Apr. 1995).      | <input type="checkbox"/> |
|  | 50 | Xilinx, Inc. , "The Programmable Logic Data Book (1993)", Xilinx, Inc. (1993).                                        | <input type="checkbox"/> |

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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |

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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |  |

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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |

|    |                                                                                                                                                                                     |                          |
|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|
| 1  | New, Bernie , "Ultra-Fast Synchronous Counters", Xilinx Application Note, XAPP 014.001 (1994).                                                                                      | <input type="checkbox"/> |
| 2  | Bolotski, Michael, DeHon, André, and Knight, Thomas , "Unifying FPGAs and SIMD Arrays", 2nd International Workshop on Field-Programmable Gate Arrays, February 13-15, 1994.         | <input type="checkbox"/> |
| 3  | Knapp, Steven K. , "Using Programmable Logic to Accelerate DSP Functions", Xilinx, Inc. (1995).                                                                                     | <input type="checkbox"/> |
| 4  | New, Bernie , "Using the Dedicated Carry Logic in XC4000", Xilinx Application Note, XAPP 013.001 (1994).                                                                            | <input type="checkbox"/> |
| 5  | Iwanczuk, Roman , "Using the XC4000 RAM Capability", Xilinx Application Note, XAPP 031.000 (1994).                                                                                  | <input type="checkbox"/> |
| 6  | "IEEE Workshop on FPGAs for Custom Computing Machines", IEEE Computer Society Technical Committee on Computer Architecture, April 10-13, 1994.                                      | <input type="checkbox"/> |
| 7  | Nobuyuki Yamashita, et.al. , "A 3.84 GIPS Integrated Memory Array Processor with 64 Processing Elements and a 2-Mb SRAM", IEEE Journal of Solid-State Circuits, Vol. 29, Nov. 1994. | <input type="checkbox"/> |
| 8  | Athanas, Peter , "FUN with the XC6200, Presentation at Cornell University", Cornell University (October 1996).                                                                      | <input type="checkbox"/> |
| 9  | Achour, C. , "A Multiprocessor Implementation of a Wavelet Transforms", Proceedings on the 4th Canadian Workshop on Field-Programmable Devices, May 13-14, 1996.                    | <input type="checkbox"/> |
| 10 | Electronic Engineering Times , "Altera ships 100,000-gate EPLD", Electronic Engineering Times, Issue 917, Sept. 20, 1996.                                                           | <input type="checkbox"/> |
| 11 | Altera Corporation , "Chipdata, Database Information for z1120a", Altera Corporation, Sept. 11, 2012.                                                                               | <input type="checkbox"/> |

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|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |                           | 14219945   |
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|  |    |                                                                                                                                                                                     |                          |
|--|----|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|
|  | 12 | Altera Corporation , "Embedded Programmable Logic Family Data Sheet", Altera Corporation, July 1995, ver. 1.                                                                        | <input type="checkbox"/> |
|  | 13 | Altera Corporation , "FLEX 10K 100, 000-Gate Embedded Array Programmable Logic Family", Altera Advantage News & Views, Newsletter for Altera Customers, Second Quarter, May 1995.   | <input type="checkbox"/> |
|  | 14 | Altera Corporation , "Implementing Multipliers in FLEX 10K Devices", Altera Corporation, March 1996, ver. 1, Application Note 53.                                                   | <input type="checkbox"/> |
|  | 15 | Intel 82375EB/82375SB PCI-EISA Bridge (PCEB) Advance Information, Xilinx Application Note, XAPP 063, v. 1.1 (Oct. 9, 1996).                                                         | <input type="checkbox"/> |
|  | 16 | Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines, IEEE Computer Society Technical Committee on Computer Architecture, April 19, 1995.                       | <input type="checkbox"/> |
|  | 17 | Proceedings of the Parallel Systems Fair, The International Parallel Processing Symposium, IEEE Computer Society Technical Committee for Parallel Processing, April 27, 1994.       | <input type="checkbox"/> |
|  | 18 | Proceedings of the Workshop on Reconfigurable Architectures, 8th International Parallel Processing Symposium, IEEE Computer Society, April 26, 1994.                                | <input type="checkbox"/> |
|  | 19 | The Programmable Logic Conference & Exhibit Proceedings, Electronic Engineering Times, April 25-27, 1995.                                                                           | <input type="checkbox"/> |
|  | 20 | Britton, Barry K. et al. , "Optimized Reconfigurable Cell Array Architecture for High-Performance Field Programmable Gate Arrays", IEEE Custom Integrated Circuits Conference 1993. | <input type="checkbox"/> |
|  | 21 | Landers, George , "Special Purpose Processor Speeds up DSP Functions, Reconfigurable Arithmetic Datapath Device", Professional Program Proceedings, Electro April 30-May2, 1996.    | <input type="checkbox"/> |
|  | 22 | Proceedings of the Third Workshop on Reconfigurable Architectures, at Sheraton Waikiki Hotel, Honolulu, Hawai, April 15, 1996.                                                      | <input type="checkbox"/> |

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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |

|  |    |                                                                                                                                 |                          |
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|  | 23 | Proceedings of the Third Workshop on Reconfigurable Architectures, at Sheraton Waikiki Hotel, Honolulu, Hawaii, April 15, 1996. | <input type="checkbox"/> |
|  | 24 | Atmel Corporation, "Configurable Logic Design and Application Book 1993-1994 - PLD, PFGE, Gate Array", 1993.                    | <input type="checkbox"/> |
|  | 25 | Atmel Corporation, "Configurable Logic Design and Application Book 1994-1995 - PLD, PFGE, Gate Array", 1994.                    | <input type="checkbox"/> |
|  | 26 | N. Wirth, "An Extension-Board with an FPGA for Experimental Circuit Design", ETH Zurich, Department Informatik, July 1993.      | <input type="checkbox"/> |
|  | 27 | F. Furtek et al. "Labyrinth: A Homogeneous Computational Medium", IEEE 1990 Custom Integrated Circuits Conference, 1990.        | <input type="checkbox"/> |
|  | 28 | Altera Corporation , "Altera 1998 Data Book", Altera Corporation (January 1998).                                                | <input type="checkbox"/> |
|  | 29 | Altera Corporation, "FLEX 10K - Embedded Programmable Logic Family", Data Sheet, ver.3.13, October 1998.                        | <input type="checkbox"/> |
|  | 30 | Altera Corporation, "Implementing RAM Functions in FLEX 10K Devices", Application Note 52, Ver. 1, November 1995.               | <input type="checkbox"/> |
|  | 31 | Altera Corporation , "Altera 1993 Data Book", Altera Corporation (August 1993).                                                 | <input type="checkbox"/> |
|  | 32 | Altera Corporation , "Altera 1995 Data Book", Altera Corporation (March 1995).                                                  | <input type="checkbox"/> |
|  | 33 | Altera Corporation, "User-Configurable Microprocessor Peripheral EPB1400", REV. 1.0, 1987.                                      | <input type="checkbox"/> |

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|  |    |                                                                                                        |                          |
|--|----|--------------------------------------------------------------------------------------------------------|--------------------------|
|  | 34 | Altera Corporation, "EPB2001 - Card Interface Chip for PS/2 Micro Channel", Data Sheet, December 1989. | <input type="checkbox"/> |
|  | 35 | Altera Corporation, " FLEX 8000 Handbook", May 1994.                                                   | <input type="checkbox"/> |

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|                   | 1       | 4967340       |                        | 1990-10-30 | Dawes                                           |                                                                          |
|                   | 2       | 5301340       |                        | 1994-04-05 | Cook                                            |                                                                          |
|                   | 3       | 5327570       |                        | 1994-07-05 | Foster et al.                                   |                                                                          |
|                   | 4       | 5459846       |                        | 1995-10-17 | Hyatt                                           |                                                                          |
|                   | 5       | 5784636       |                        | 1998-07-21 | Rupp                                            |                                                                          |
|                   | 6       | 5991900       |                        | 1999-11-23 | Garnett                                         |                                                                          |
|                   | 7       | 6052773       |                        | 2000-04-18 | DeHon et al.                                    |                                                                          |
|                   | 8       | 6079008       |                        | 2000-06-20 | Clery III                                       |                                                                          |

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|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |
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|  |    |         |  |            |                   |  |
|--|----|---------|--|------------|-------------------|--|
|  | 9  | 6119181 |  | 2000-09-12 | Vorbach et al.    |  |
|  | 10 | 6138198 |  | 2000-10-24 | Garnett et al.    |  |
|  | 11 | 6226714 |  | 2001-05-01 | Safranek et al.   |  |
|  | 12 | 6321296 |  | 2001-11-20 | Pescatore         |  |
|  | 13 | 6321373 |  | 2001-11-20 | Ekanadham et al.  |  |
|  | 14 | 6425068 |  | 2002-07-23 | Vorbach et al.    |  |
|  | 15 | 6457100 |  | 2002-09-24 | Ignatowski et al. |  |
|  | 16 | 6587961 |  | 2003-07-01 | Garnett et al.    |  |
|  | 17 | 6643747 |  | 2003-11-04 | Hammarlund et al. |  |
|  | 18 | 6658578 |  | 2003-12-02 | Laurenti et al.   |  |
|  | 19 | 6763327 |  | 2004-07-13 | Songer et al.     |  |

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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |  |

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|  | 20 | 6868476 |  | 2005-03-15 | Rosenbluth et al. |  |
|  | 21 | 6895452 |  | 2005-05-17 | Coleman et al.    |  |
|  | 22 | 7043416 |  | 2006-05-09 | Lin               |  |
|  | 23 | 8463835 |  | 2013-06-11 | Walke             |  |
|  | 24 | 9047440 |  | 2015-06-02 | Vorbach et al.    |  |
|  | 25 | 6381687 |  | 2002-04-30 | Sandstrom et al.  |  |
|  | 26 | 9147623 |  | 2015-09-29 | Lua et al.        |  |
|  | 27 | 9099460 |  | 2015-08-04 | Cho et al.        |  |

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|--------------------|---------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|
|                    | 1       | Silberschatz and Galvin, Operating System Concepts, 1998, Addison Wesley, 5th edition, ISBN 0-201-59113-8, 31 pages                                                                                                                                             | <input type="checkbox"/> |
|                    | 2       | Altera FLEX 10K Embedded Programmable Logic Family Data Sheet; October 1998, ver. 3.13; pages 1 -21.                                                                                                                                                            | <input type="checkbox"/> |
|                    | 3       | Hauser, John Reid, Augmenting a Microprocessor with Reconfigurable Hardware, University of California, Berkeley, Fall 2000.                                                                                                                                     | <input type="checkbox"/> |

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|                   | 1       | 4539637       |                        | 1985-09-03 | DeBruler                                        |                                                                          |
|                   | 2       | 5197016       |                        | 1993-03-23 | Sugimoto et al.                                 |                                                                          |
|                   | 3       | 5296759       |                        | 1994-03-22 | Sutherland et al.                               |                                                                          |
|                   | 4       | 5651137       |                        | 1997-07-22 | MacWilliams et al.                              |                                                                          |
|                   | 5       | 5685004       |                        | 1997-11-04 | Bruce et al.                                    |                                                                          |
|                   | 6       | 5808487       |                        | 1998-09-15 | Roy                                             |                                                                          |
|                   | 7       | 5893165       |                        | 1999-04-06 | Ebrahim                                         |                                                                          |
|                   | 8       | 5905875       |                        | 1999-05-18 | Takahashi et al.                                |                                                                          |

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|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |            |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |

|  |    |         |  |            |                   |  |
|--|----|---------|--|------------|-------------------|--|
|  | 9  | 6038646 |  | 2000-03-14 | Sproull           |  |
|  | 10 | 6108737 |  | 2000-08-22 | Sharma et al.     |  |
|  | 11 | 6119219 |  | 2000-09-12 | Webb et al.       |  |
|  | 12 | 6122719 |  | 2000-09-19 | Mirsky et al.     |  |
|  | 13 | 6141734 |  | 2000-10-31 | Razdan et al.     |  |
|  | 14 | 6209065 |  | 2001-03-27 | Van Doren et al.  |  |
|  | 15 | 6263406 |  | 2001-07-17 | Uwano et al.      |  |
|  | 16 | 6286090 |  | 2001-09-04 | Steely Jr. et al. |  |
|  | 17 | 6314484 |  | 2001-11-06 | Zulian et al.     |  |
|  | 18 | 6341318 |  | 2002-01-22 | Dakhil            |  |
|  | 19 | 6347346 |  | 2002-02-12 | Taylor            |  |

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|  |    |         |  |            |                   |  |
|--|----|---------|--|------------|-------------------|--|
|  | 20 | 6385672 |  | 2002-05-07 | Wang et al.       |  |
|  | 21 | 6457100 |  | 2002-09-24 | Ignatowski et al. |  |
|  | 22 | 6467009 |  | 2002-10-15 | Winegarden et al. |  |
|  | 23 | 6522167 |  | 2003-02-18 | Ansari et al.     |  |
|  | 24 | 6571322 |  | 2003-05-27 | Arimilli et al.   |  |
|  | 25 | 7036106 |  | 2006-04-25 | Wang et al.       |  |
|  | 26 | 7924837 |  | 2011-04-12 | Shabtay et al.    |  |
|  | 27 | 7933838 |  | 2011-04-26 | Ye                |  |

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|                   | 1       | 20040093186        | A1                     | 2004-05-13       | Ebert Jeffrey Allen et al.                      |                                                                          |

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|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|--|
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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |  |

|  |   |             |    |            |                          |  |
|--|---|-------------|----|------------|--------------------------|--|
|  | 2 | 20050257179 | A1 | 2005-11-17 | Stauffer David R. et al. |  |
|  | 3 | 20060036988 | A1 | 2006-02-16 | Allen Tim et al.         |  |

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|                                 | 1       | Katherine Compton, Scott Hauck, Reconfigurable computing: a survey of systems and software, ACM Computing Surveys (CSUR), v.34 n.2, p.171-210, June 2002.                                                                                                       |  |  |  |  |  | <input type="checkbox"/> |

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|                   | 1       | 4412303       |                        | 1983-10-25 | Barnes et al.                                   |                                                                          |
|                   | 2       | 4454578       |                        | 1984-06-12 | Matsumoto et al.                                |                                                                          |
|                   | 3       | 4748580       |                        | 1988-05-31 | Ashton et al.                                   |                                                                          |
|                   | 4       | 4837735       |                        | 1989-06-06 | Allen Jr. et al.                                |                                                                          |
|                   | 5       | 4862407       |                        | 1989-08-29 | Fette et al.                                    |                                                                          |
|                   | 6       | 4959781       |                        | 1990-09-25 | Rubinstein et al.                               |                                                                          |
|                   | 7       | 5070475       |                        | 1991-12-03 | Normoyle et al.                                 |                                                                          |
|                   | 8       | 5081575       |                        | 1992-01-14 | Hiller et al.                                   |                                                                          |

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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |

|  |    |         |  |            |                   |  |
|--|----|---------|--|------------|-------------------|--|
|  | 9  | 5119499 |  | 1992-06-02 | Tonomura et al.   |  |
|  | 10 | 5261113 |  | 1993-11-09 | Jouppi            |  |
|  | 11 | 5296759 |  | 1994-03-22 | Sutherland et al. |  |
|  | 12 | 5430885 |  | 1995-07-04 | Kaneko et al.     |  |
|  | 13 | 5469003 |  | 1995-11-21 | Kean              |  |
|  | 14 | 5572680 |  | 1996-11-05 | Ikeda et al.      |  |
|  | 15 | 5581778 |  | 1996-12-03 | Chin et al.       |  |
|  | 16 | 5675777 |  | 1997-10-07 | Glickman          |  |
|  | 17 | 5721921 |  | 1998-02-24 | Kessler et al.    |  |
|  | 18 | 5752035 |  | 1998-05-12 | Trimberger        |  |
|  | 19 | 5765009 |  | 1998-06-09 | Ishizaka          |  |

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|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |

|  |    |         |  |            |                  |  |
|--|----|---------|--|------------|------------------|--|
|  | 20 | 5774704 |  | 1998-06-30 | Williams         |  |
|  | 21 | 5812844 |  | 1998-09-22 | Jones et al.     |  |
|  | 22 | 5832288 |  | 1998-11-03 | Wong             |  |
|  | 23 | 5892962 |  | 1999-04-06 | Cloutier         |  |
|  | 24 | 5898602 |  | 1999-04-27 | Rothman et al.   |  |
|  | 25 | 5913925 |  | 1999-06-22 | Kahle et al.     |  |
|  | 26 | 5915123 |  | 1999-06-22 | Mirsky et al.    |  |
|  | 27 | 5933642 |  | 1999-08-03 | Greenbaum et al. |  |
|  | 28 | 5956518 |  | 1999-09-21 | DeHon et al.     |  |
|  | 29 | 5966534 |  | 1999-10-12 | Cooke et al.     |  |
|  | 30 | 5978583 |  | 1999-11-02 | Ekanadham et al. |  |

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|  |    |         |  |            |                    |  |
|--|----|---------|--|------------|--------------------|--|
|  | 31 | 5978830 |  | 1999-11-02 | Nakaya et al.      |  |
|  | 32 | 5990910 |  | 1999-11-23 | Laksono et al.     |  |
|  | 33 | 6023742 |  | 2000-02-08 | Ebeling et al.     |  |
|  | 34 | 6034542 |  | 2000-03-07 | Ridgeway           |  |
|  | 35 | 6049859 |  | 2000-04-11 | Gliese et al.      |  |
|  | 36 | 6052773 |  | 2000-04-18 | DeHon et al.       |  |
|  | 37 | 6058465 |  | 2000-05-02 | Nguyen             |  |
|  | 38 | 6075935 |  | 2000-06-13 | Ussery et al.      |  |
|  | 39 | 6076157 |  | 2000-06-13 | Borkenhagen et al. |  |
|  | 40 | 6077315 |  | 2000-06-20 | Greenbaum et al.   |  |
|  | 41 | 6096091 |  | 2000-08-01 | Hartmann           |  |

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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |

|  |    |         |  |            |                  |  |
|--|----|---------|--|------------|------------------|--|
|  | 42 | 6104696 |  | 2000-08-15 | Kadambi et al.   |  |
|  | 43 | 6122720 |  | 2000-09-19 | Cliff            |  |
|  | 44 | 6124868 |  | 2000-09-26 | Asaro et al.     |  |
|  | 45 | 6148407 |  | 2000-11-14 | Aucsmith         |  |
|  | 46 | 6209020 |  | 2001-03-27 | Angle et al.     |  |
|  | 47 | 6215326 |  | 2001-04-10 | Jefferson et al. |  |
|  | 48 | 6216174 |  | 2001-04-10 | Scott et al.     |  |
|  | 49 | 6219833 |  | 2001-04-17 | Solomon et al.   |  |
|  | 50 | 6226717 |  | 2001-05-01 | Reuter et al.    |  |
|  | 51 | 6237059 |  | 2001-05-22 | Dean et al.      |  |
|  | 52 | 6289369 |  | 2001-09-11 | Sundaresan       |  |

|                                                                                                     |                        |                           |            |
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|  |    |         |  |            |                   |  |
|--|----|---------|--|------------|-------------------|--|
|  | 53 | 6308191 |  | 2001-10-23 | Dujardin et al.   |  |
|  | 54 | 6321296 |  | 2001-11-20 | Pescatore         |  |
|  | 55 | 6321298 |  | 2001-11-20 | Hubis             |  |
|  | 56 | 6374286 |  | 2002-04-16 | Gee et al.        |  |
|  | 57 | 6421757 |  | 2002-07-16 | Wang et al.       |  |
|  | 58 | 6425068 |  | 2002-07-23 | Vorbach et al.    |  |
|  | 59 | 6501999 |  | 2002-12-31 | Cai               |  |
|  | 60 | 6526430 |  | 2003-02-25 | Hung et al.       |  |
|  | 61 | 6538470 |  | 2003-03-25 | Langhammer et al. |  |
|  | 62 | 6539438 |  | 2003-03-25 | Ledzius et al.    |  |
|  | 63 | 6587939 |  | 2003-07-01 | Takano            |  |

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| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     | 14219945                  |
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|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |
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|  |    |         |  |            |                |  |
|--|----|---------|--|------------|----------------|--|
|  | 64 | 6633181 |  | 2003-10-14 | Rupp           |  |
|  | 65 | 6658564 |  | 2003-12-02 | Smith et al.   |  |
|  | 66 | 6665758 |  | 2003-12-16 | Frazier et al. |  |
|  | 67 | 6708325 |  | 2004-03-16 | Cooke et al.   |  |
|  | 68 | 6757892 |  | 2004-06-29 | Gokhale et al. |  |
|  | 69 | 6795939 |  | 2004-09-21 | Harris et al.  |  |
|  | 70 | 6799265 |  | 2004-09-28 | Dakhil         |  |
|  | 71 | 6865662 |  | 2005-03-08 | Wang           |  |
|  | 72 | 6871341 |  | 2005-03-22 | Shyr           |  |
|  | 73 | 6925641 |  | 2005-08-02 | Elabd          |  |
|  | 74 | 7000161 |  | 2006-02-14 | Allen et al.   |  |

|                                                                                                     |                        |                           |            |  |
|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|--|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |                           | 14219945   |  |
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|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |            |  |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |  |

|  |    |         |  |            |                 |  |
|--|----|---------|--|------------|-----------------|--|
|  | 75 | 7210129 |  | 2007-04-24 | May et al.      |  |
|  | 76 | 7266725 |  | 2007-09-04 | Vorbach et al.  |  |
|  | 77 | 7340596 |  | 2008-03-04 | Crosland et al. |  |
|  | 78 | 7581076 |  | 2009-08-25 | Vorbach         |  |
|  | 79 | 7928763 |  | 2011-04-19 | Vorbach         |  |
|  | 80 | 8156284 |  | 2012-04-10 | Vorbach et al.  |  |
|  | 81 | 7188234 |  | 2007-03-06 | Wu et al.       |  |
|  | 82 | 4577293 |  | 1986-03-18 | Matick et al.   |  |

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|-------------------|---------|--------------------|------------------------|------------------|-------------------------------------------------|--------------------------------------------------------------------------|
|                   | 1       | 20010003834        | A1                     | 2001-06-14       | Shimonishi Hideyuki                             |                                                                          |

|                                                                                                     |                        |                           |            |
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|  |    |             |    |            |                               |  |
|--|----|-------------|----|------------|-------------------------------|--|
|  | 2  | 20010032305 | A1 | 2001-10-18 | Barry Edwin F.                |  |
|  | 3  | 20020004916 | A1 | 2002-01-10 | Marchand Patrick R. et al.    |  |
|  | 4  | 20020010840 | A1 | 2002-01-24 | Barroso Luiz A. et al.        |  |
|  | 5  | 20020145545 | A1 | 2002-10-10 | Brown Russell A.              |  |
|  | 6  | 20030014743 | A1 | 2003-01-16 | COOKE LAURENCE H. et al.      |  |
|  | 7  | 20030033514 | A1 | 2003-02-13 | Appleby-Allis John et al.     |  |
|  | 8  | 20030046530 | A1 | 2003-03-06 | Poznanovic Daniel             |  |
|  | 9  | 20030101307 | A1 | 2003-05-29 | Gemelli Riccardo et al.       |  |
|  | 10 | 20030120904 | A1 | 2003-06-26 | Sudharsanan Subramania et al. |  |
|  | 11 | 20060095716 | A1 | 2006-05-04 | Ramesh Tirumale K.            |  |
|  | 12 | 20060259744 | A1 | 2006-11-16 | Matthes Wolfgang              |  |

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|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|--|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |                           | 14219945   |  |
|                                                                                                     | Filing Date            |                           | 2014-03-19 |  |
|                                                                                                     | First Named Inventor   | Martin Vorbach            |            |  |
|                                                                                                     | Art Unit               | 2116                      |            |  |
|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |            |  |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |  |

|  |    |             |    |            |                        |  |
|--|----|-------------|----|------------|------------------------|--|
|  | 13 | 20070143577 | A1 | 2007-06-21 | Smith Graeme Roy       |  |
|  | 14 | 20070143578 | A1 | 2007-06-21 | Horton James A. et al. |  |
|  | 15 | 20100153654 | A1 | 2010-06-17 | VORBACH MARTIN et al.  |  |
|  | 16 | 20110060942 | A1 | 2011-03-10 | VORBACH Martin         |  |
|  | 17 | 20110145547 | A1 | 2011-06-16 | VORBACH Martin         |  |
|  | 18 | 20120017066 | A1 | 2012-01-19 | Vorbach Martin et al.  |  |
|  | 19 | 20140297914 | A1 | 2014-10-02 | Vorbach Martin         |  |
|  | 20 | 20140297948 | A1 | 2014-10-02 | VORBACH Martin et al.  |  |
|  | 21 | 20070043965 | A1 | 2007-02-22 | Mandelblat et al.      |  |
|  | 22 | 20050080994 | A1 | 2005-04-14 | Cohen et al.           |  |

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|                                                                                                     | Filing Date            |                           | 2014-03-19 |  |
|                                                                                                     | First Named Inventor   | Martin Vorbach            |            |  |
|                                                                                                     | Art Unit               | 2116                      |            |  |
|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |            |  |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |  |

| Examiner Initial* | Cite No | Foreign Document Number <sup>3</sup> | Country Code <sup>2</sup> j | Kind Code <sup>4</sup> | Publication Date | Name of Patentee or Applicant of cited Document | Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear | T <sup>5</sup>           |
|-------------------|---------|--------------------------------------|-----------------------------|------------------------|------------------|-------------------------------------------------|--------------------------------------------------------------------------|--------------------------|
|                   | 1       | WO9525306                            | WO                          |                        | 1995-09-21       | CHERITON, David, R                              |                                                                          | <input type="checkbox"/> |

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|                                 | 1       | GOLDBERG D: "WHAT EVERY COMPUTER SCIENTIST SHOULD KNOW ABOUT FLOATING-POINT ARITHMETIC", ACM COMPUTING SURVEYS, ACM, NEW YORK, NY, US, US, vol. 23, no. 1, 1 March 1991 (1991-03-01), pages 5-48.                                                                                                                                                     |  |  |  |  |  | <input type="checkbox"/> |
|                                 | 2       | HAUSER ET AL. "Garp: A MIPS Processor with a Reconfigurable Coprocessor", April 1997, pgs. 12-21.                                                                                                                                                                                                                                                     |  |  |  |  |  | <input type="checkbox"/> |
|                                 | 3       | LIBO HUANG ET AL: "A New Architecture For Multiple-Precision Floating-Point Multiply-Add Fused Unit Design" COMPUTER ARITHMETIC, 2007. ARITH '07. 18TH IEEE SYMPOSIUM ON, IEEE, PI, 1. Juni 2007 (2007-06-01), Seiten 69-76.                                                                                                                          |  |  |  |  |  | <input type="checkbox"/> |
|                                 | 4       | MANHWEE JO ET AL: "Implementation of floating-point operations for 3D graphics on a coarse-grained reconfigurable architecture" SOC CONFERENCE, 2007 IEEE INTERNATIONAL, IEEE, PISCATAWAY, NJ, USA, 26. September 2007 (2007-09-26), Seiten 127-130.                                                                                                  |  |  |  |  |  | <input type="checkbox"/> |
|                                 | 5       | MIRSKY E. ET AL., "MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources", 1996, IEEE, pp. 157-166.                                                                                                                                                                                     |  |  |  |  |  | <input type="checkbox"/> |
|                                 | 6       | SHIRAZI ET AL., "Quantitative analysis of floating point arithmetic on FPGA based custom computing machines," IEEE Symposium on FPGAs for Custom Computing Machines, I EEE Computer Society Press, Apr. 19-21, 1995, pp. 155-162.                                                                                                                     |  |  |  |  |  | <input type="checkbox"/> |
|                                 | 7       | VERMEULEN ET AL., Silicon Debug of a Co-Processor Array for Video Applications, 2000, IEEEExplore, 0-7695-0786-7/00, Pages 47-52, [retrieved on 2/1/2015], retrieved from URL <a href="http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&amp;arnumber=889558&amp;tag=1">http://ieeexplore.ieee.org/stamp/stamp.jsp?tp=&amp;arnumber=889558&amp;tag=1</a> |  |  |  |  |  | <input type="checkbox"/> |

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| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     | 14219945                  |
|                                                                                                     | Filing Date            | 2014-03-19                |
|                                                                                                     | First Named Inventor   | Martin Vorbach            |
|                                                                                                     | Art Unit               | 2116                      |
|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |

| EXAMINER SIGNATURE                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           |                      |                 |            |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------|-----------------|------------|
| Examiner Signature                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                           | /Abdelmoniem Elamin/ | Date Considered | 05/09/2016 |
| *EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.                                                                                                                                                                                                                                                                                                                                                                                                  |                      |                 |            |
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|                                                                                                                    |                                            |                                                                  |
|--------------------------------------------------------------------------------------------------------------------|--------------------------------------------|------------------------------------------------------------------|
| <b><i>Index of Claims</i></b><br> | <b>Application/Control No.</b><br>14219945 | <b>Applicant(s)/Patent Under Reexamination</b><br>VORBACH ET AL. |
|                                                                                                                    | <b>Examiner</b><br>M ELAMIN                | <b>Art Unit</b><br>2116                                          |

|   |                 |   |                   |   |                     |   |                 |
|---|-----------------|---|-------------------|---|---------------------|---|-----------------|
| ✓ | <b>Rejected</b> | - | <b>Cancelled</b>  | N | <b>Non-Elected</b>  | A | <b>Appeal</b>   |
| = | <b>Allowed</b>  | ÷ | <b>Restricted</b> | I | <b>Interference</b> | O | <b>Objected</b> |

| <input type="checkbox"/> Claims renumbered in the same order as presented by applicant |          | <input type="checkbox"/> CPA |  | <input type="checkbox"/> T.D. |  | <input type="checkbox"/> R.1.47 |  |  |  |
|----------------------------------------------------------------------------------------|----------|------------------------------|--|-------------------------------|--|---------------------------------|--|--|--|
| CLAIM                                                                                  |          | DATE                         |  |                               |  |                                 |  |  |  |
| Final                                                                                  | Original | 05/11/2016                   |  |                               |  |                                 |  |  |  |
|                                                                                        | 1        | -                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 2        | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 3        | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 4        | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 5        | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 6        | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 7        | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 8        | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 9        | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 10       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 11       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 12       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 13       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 14       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 15       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 16       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 17       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 18       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 19       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 20       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 21       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 22       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 23       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 24       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 25       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 26       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 27       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 28       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 29       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 30       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 31       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 32       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 33       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 34       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 35       | ✓                            |  |                               |  |                                 |  |  |  |
|                                                                                        | 36       | ✓                            |  |                               |  |                                 |  |  |  |

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|------------------------------------------------------------------------------------------------------------------------|--------------------------------------------|------------------------------------------------------------------|
| <p><b><i>Index of Claims</i></b></p>  | <b>Application/Control No.</b><br>14219945 | <b>Applicant(s)/Patent Under Reexamination</b><br>VORBACH ET AL. |
|                                                                                                                        | <b>Examiner</b><br>M ELAMIN                | <b>Art Unit</b><br>2116                                          |

|   |                 |
|---|-----------------|
| ✓ | <b>Rejected</b> |
| = | <b>Allowed</b>  |

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| ÷ | <b>Restricted</b> |

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| N | <b>Non-Elected</b>  |
| I | <b>Interference</b> |

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| A | <b>Appeal</b>   |
| O | <b>Objected</b> |

| <input type="checkbox"/> Claims renumbered in the same order as presented by applicant <input type="checkbox"/> CPA <input type="checkbox"/> T.D. <input type="checkbox"/> R.1.47 |          |            |  |  |  |  |  |  |  |  |
|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|------------|--|--|--|--|--|--|--|--|
| CLAIM                                                                                                                                                                             |          | DATE       |  |  |  |  |  |  |  |  |
| Final                                                                                                                                                                             | Original | 05/11/2016 |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 37       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 38       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 39       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 40       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 41       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 42       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 43       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 44       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 45       | ✓          |  |  |  |  |  |  |  |  |
|                                                                                                                                                                                   | 46       | ✓          |  |  |  |  |  |  |  |  |

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| <b><i>Search Notes</i></b><br><br> | <b>Application/Control No.</b><br><br>14219945 | <b>Applicant(s)/Patent Under Reexamination</b><br><br>VORBACH ET AL. |
|                                                                                                                     | <b>Examiner</b><br><br>M ELAMIN                | <b>Art Unit</b><br><br>2116                                          |

| CPC- SEARCHED |      |          |
|---------------|------|----------|
| Symbol        | Date | Examiner |
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| CPC COMBINATION SETS - SEARCHED |      |          |
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| Symbol                          | Date | Examiner |
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| US CLASSIFICATION SEARCHED |          |      |          |
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| Class                      | Subclass | Date | Examiner |
|                            |          |      |          |

| SEARCH NOTES |           |          |
|--------------|-----------|----------|
| Search Notes | Date      | Examiner |
| WEST         | 5/10/2016 | AE       |
| WEST         | 5/11/2016 | AE       |

| INTERFERENCE SEARCH     |                         |      |          |
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| US Class/<br>CPC Symbol | US Subclass / CPC Group | Date | Examiner |
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## WEST Search History

DATE: Wednesday, May 11, 2016

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| <input type="checkbox"/> | L12                                   | L2 and ((load or workload or us\$6 or utiliz\$5) with (frequency or clock)) | 1                |
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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |  |

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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |

|    |                                                                                                                                                 |                          |
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| 1  | Xilinx, Inc. , "The Programmable Logic Data Book (1994)", Xilinx, Inc. (1994).                                                                  | <input type="checkbox"/> |
| 2  | Xilinx, Inc. , "The Programmable Logic Data Book (1996)", Xilinx, Inc. (Jan. 1996).                                                             | <input type="checkbox"/> |
| 3  | Churcher, Stephen et al. , "The XC6200 FastMap Processor Interface", FPL (Aug. 1995).                                                           | <input type="checkbox"/> |
| 4  | Texas Instruments Incorporated , "TMS320C80 (MVP) Parallel Processor User's Guide", Texas Instruments Incorporated (1995).                      | <input type="checkbox"/> |
| 5  | Texas Instruments Incorporated , "TMS320C8x System-Level Synopsis", Texas Instruments Incorporated (Sept. 1995).                                | <input type="checkbox"/> |
| 6  | Xilinx, Inc. , "XC6200 Field Programmable Gate Arrays, Advance Product Specification, v. 1.0, June 1, 1996", Xilinx, Inc. (June 1, 1996).       | <input type="checkbox"/> |
| 7  | Xilinx, Inc. , "Xilinx XC6200 Field Programmable Gate Arrays, Product Specification, v.1.10, Apr. 24, 1997", Xilinx, Inc. (Apr. 24, 1997).      | <input type="checkbox"/> |
| 8  | Altera Corporation , "Programmable Peripheral Interface Adapter a8255, September 1996, ver. 1", Altera Corporation, September 1996, ver. 1.     | <input type="checkbox"/> |
| 9  | Altera Corporation , "Universal Asynchronous Receiver/Transmitter a16450, September 1996, ver. 1", Altera Corporation, September 1996, ver. 1.  | <input type="checkbox"/> |
| 10 | Altera Corporation , "Asynchronous Communications Interface Adapter a6850, September 1996, ver. 1", Altera Corporation, September 1996, ver. 1. | <input type="checkbox"/> |
| 11 | Schmit, Herman et al. , "Behavioral Synthesis for FPGA-based Computing", IEEE (1994).                                                           | <input type="checkbox"/> |

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|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |                           | 14219945   |
|                                                                                                     | Filing Date            |                           | 2014-03-19 |
|                                                                                                     | First Named Inventor   | Martin Vorbach            |            |
|                                                                                                     | Art Unit               | 2116                      |            |
|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |            |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |

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|----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|
| 12 | Allaire, Bill and Knapp, Steve , "A Plug and Play Interface Using Xilinx FPGAs", Xilinx, Inc. (May 1995).                                                                                         | <input type="checkbox"/> |
| 13 | Goslin, Greg and Newgard, Bruce , "16-Tap, 8-Bit FIR Filter Applications Guide", Xilinx Application Note v. 1.01 (Nov. 21, 1994).                                                                 | <input type="checkbox"/> |
| 14 | Veendrick, H. , "A 1.5 GIPS Video Signal Processor (VSP)", IEEE 1994 Custom Integrated Circuits Conference (1994).                                                                                | <input type="checkbox"/> |
| 15 | Yeung, Alfred K. and Rabaey, Jan M. , "A 2.4GOPS Data-Driven Reconfigurable Multiprocessor IC for DSP", IEEE International Solid-State Circuits Conference (1995).                                | <input type="checkbox"/> |
| 16 | Duncan, Ann , "A 32x16 Reconfigurable Correlator for the XC6200", Xilinx Application Note, XAPP 084, v. 1.0 (July 25, 1997).                                                                      | <input type="checkbox"/> |
| 17 | Yeung, Kwok Wah , "A Data-Driven Multiprocessor Architecture for High Throughput Digital Signal Processing", U.C. Berkeley (July 10, 1995).                                                       | <input type="checkbox"/> |
| 18 | Koren, Israel et al. , "A Data-Driven VLSI Array for Arbitrary Algorithms", IEEE (1988).                                                                                                          | <input type="checkbox"/> |
| 19 | Xilinx, Inc. , "A Fast Constant Coefficient Multiplier", Xilinx, Inc., Xilinx Application Note, XAPP 082, v. 1.0 (Aug. 24, 1997).                                                                 | <input type="checkbox"/> |
| 20 | Sutton, Roy A. et al. , "A Multiprocessor DSP System Using PADDI -2", U.C. Berkeley (1998).                                                                                                       | <input type="checkbox"/> |
| 21 | Chen, Dev C. and Rabaey, Jan M. , "A Reconfigurable Multiprocessor IC for Rapid Prototyping of Algorithmic-Specific High-speed DSP Data Paths", IEEE Journal of Solid State Circuits (Dec. 1992). | <input type="checkbox"/> |
| 22 | Minnick, Robert , "A Survey of Microcellular Research", J. of the Association for Computing Machinery, Vol. 14, No. 2 (April 1967).                                                               | <input type="checkbox"/> |

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|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|
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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |

|  |    |                                                                                                                                                           |                          |
|--|----|-----------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|
|  | 23 | Trimberger, Steve et al. , "A Time-Multiplexed FPGA", IEEE (1997).                                                                                        | <input type="checkbox"/> |
|  | 24 | New, Bernie , "Accelerating Loadable Counters in XC4000", Xilinx Application Note, XAPP 023.001 (1994).                                                   | <input type="checkbox"/> |
|  | 25 | Athanas, Peter , "An Adaptive Machine Architecture and Compiler for Dynamic Processor Reconfiguration", Brown University (May 1992).                      | <input type="checkbox"/> |
|  | 26 | Atmel Corporation , "Application Note AT6000 Series Configuration", Published in May 1993.                                                                | <input type="checkbox"/> |
|  | 27 | Agarwal, Anant et al. , "APRIL: A Processor Architecture for Multiprocessing", IEEE (1990).                                                               | <input type="checkbox"/> |
|  | 28 | Allaire, Bill and Fischer, Bud , "Block Adaptive Filter", Xilinx Application Note, XAPP 055, v. 1.0 (Aug. 15, 1996).                                      | <input type="checkbox"/> |
|  | 29 | Bittner, Jr., Ray A. et al. , "Colt: An Experiment in Wormhole Run-Time Reconfiguration", Proc. of SPIE, Vol. 2914 (Oct. 21, 1996).                       | <input type="checkbox"/> |
|  | 30 | New, Bernie , "Complex Digital Waveform Generator", Xilinx Application Note, XAPP 008.002 (1994).                                                         | <input type="checkbox"/> |
|  | 31 | Alfke, Peter , "Dynamic Reconfiguration", Xilinx Application Note, XAPP 093, v. 1.1 (Nov. 10, 1997).                                                      | <input type="checkbox"/> |
|  | 32 | Canadian Microelectronics Corp , "Field-Programmable Devices", 1994 Canadian Workshop on Field-Programmable Devices, June 13-16, 1994, Kingston, Ontario. | <input type="checkbox"/> |
|  | 33 | S. Brown et al., Published by Kluwer Academic Publishers , "Field Programmable Gate Arrays", Atmel Corporation, 1992.                                     | <input type="checkbox"/> |

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|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|
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|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |

|  |    |                                                                                                                                                                                                                                                                                                                                 |                          |
|--|----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|
|  | 34 | Atmel Corporation , "Field Programmable Gate Arrays, AT6000 Series", Atmel Corporation, 1993.                                                                                                                                                                                                                                   | <input type="checkbox"/> |
|  | 35 | International Society for Optical Engineering, , "Field Programmable Gate Arrays (FPGAs) for Fast Board Development and Reconfigurable Computing", International Society for Optical Engineering, Vol. 2607, October 25-26, 1995.                                                                                               | <input type="checkbox"/> |
|  | 36 | Trimberger, Stephen M., "Field-Programmable Gate Array Technology", Kluwer Academic Publishers (1994).                                                                                                                                                                                                                          | <input type="checkbox"/> |
|  | 37 | Hartenstein, Reiner Servit, Michal (Eds.) , "Field-Programmable Logic – Architectures, Synthesis and Applications", 4th Intl Workshop on Field-Programmable Logic and Applications, FPL '94, Prague, Czech Republic, September 7-9,1994.                                                                                        | <input type="checkbox"/> |
|  | 38 | IEEE Computer Society , "FPGAs for Custom Computing Machines", FCCM '93, IEEE Computer Society, April 5-7, 1993.                                                                                                                                                                                                                | <input type="checkbox"/> |
|  | 39 | Cowie, Beth , "High Performance, Low Area, Interpolator Design for the XC6200", Xilinx Application Note, XAPP 081, v. 1.0 (May 7, 1997).                                                                                                                                                                                        | <input type="checkbox"/> |
|  | 40 | IEEE Computer Society Technical Committee on Computer Architecture , "IEEE Symposium on FPGAs for Custom Computing Machines", IEEE Computer Society Technical Committee on Computer Architecture, April 19-21, 1995.                                                                                                            | <input type="checkbox"/> |
|  | 41 | B. Schoner, C. Jones and J. Villasenor , "Issues in wireless video coding using run-time-reconfigurable FPGAs", Proceedings of the IEEE Symposium on FPGAs for Custom Computing Machines (Apr. 19, 1995).                                                                                                                       | <input type="checkbox"/> |
|  | 42 | Moore, Will and Luk, Wayne , "More FPGAs", Abingdon EE&CS Books (1994).                                                                                                                                                                                                                                                         | <input type="checkbox"/> |
|  | 43 | Fawcett, Bradly K. , "New SRAM-Based FPGA Architectures Address New Applications", IEEE (Nov. 1995).                                                                                                                                                                                                                            | <input type="checkbox"/> |
|  | 44 | Department of Electrical and Computer Engineering, The University of Toronto , "Proceedings of the 4th Canadian Workshop on Field-Programmable Devices", Proceedings of the 4th Canadian Workshop on Field-Programmable Devices, Department of Electrical and Computer Engineering, The University of Toronto, May 13-14, 1996. | <input type="checkbox"/> |

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|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |

|  |    |                                                                                                                                                                                 |                          |
|--|----|---------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------------|
|  | 45 | Chen, Devereaux C. , "Programmable Arithmetic Devices for High Speed Digital Signal Processing", U.C. Berkeley (1992).                                                          | <input type="checkbox"/> |
|  | 46 | Vasell, Jasper, et al. , "The Function Processor: A Data-Driven Processor Array for Irregular Computations", Future Generations Computer Systems, Vol. 8, Issue 4 (Sept. 1992). | <input type="checkbox"/> |
|  | 47 | T. Korpiharju, J. Viitanen, H. Kiminkinen, J. Takala, K. Kaski , "TUTCA configurable logic cell array architecture", IEEE (1991).                                               | <input type="checkbox"/> |
|  | 48 |                                                                                                                                                                                 | <input type="checkbox"/> |
|  | 49 |                                                                                                                                                                                 | <input type="checkbox"/> |
|  | 50 |                                                                                                                                                                                 | <input type="checkbox"/> |

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#### EXAMINER SIGNATURE

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| Examiner Signature | /Abdelmoniem Elamin/ | Date Considered | 05/09/2016 |
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

|                                                                                               |                                 |
|-----------------------------------------------------------------------------------------------|---------------------------------|
| Applicant(s): Martin Vorbach et al.                                                           |                                 |
| Application No.: 14/219,945                                                                   | Art Unit: 2116                  |
| Filed:                                                                                        | Confirmation No.: 7671          |
| Title: <b>Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply</b> | Examiner: Elamin, Abdelmoniem I |
| Attorney Docket No.: PACT-025-PCT-US-D1-2C1-D1                                                |                                 |

Electronically filed  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

RESPONSE AFTER NON-FINAL

Dear Sir:

In response to the Non-Final Office Action of May 16, 2016, please find:

- a listing of claims that begins at 2; and
- Remarks that begin at 13.

Claims:

1. (canceled)
2. (Currently amended) A multiprocessor system comprising:
  - a plurality of data processing units, each of the data processing units:
    - (a) being programmable; and
    - (b) being adaptable for sequentially processing data in a clocked manner; and including
      - (c1) at least one Arithmetic Logic Unit (ALU)<sub>i</sub> and
      - (c2) at least one data register set<sub>i</sub> for storing intermediate results in sequential data processing<sub>i</sub>
  - at least one bus system for at least interconnecting at least some of the data processing units, each being provided a supply voltage by a voltage supply;
  - wherein for at least some of the data processing units, the clock frequency is adjustable at runtime without affecting the clock frequency of at least one of:
    - one other of the data processing units<sub>j</sub> and
    - the bus system; and

wherein the voltage supply is adapted to supply higher supply voltages for data processing at higher clock frequencies.

3. (Original) The system of claim 2 wherein for at least some of the data processing units, the clock frequency is adjustable at runtime according to a state of the multiprocessor system.
4. (Original) The system of claim 2 wherein for at least some of the data processing units, the clock frequency is adjustable at runtime according to a state of the data processing entity.
5. (Original) The system of claim 2 wherein for at least some of the data processing units, the clock frequency is adjustable at runtime according to a state of others of the data processing units.
6. (Original) The system of claim 2 wherein for at least some of the data processing units, the clock frequency is adjustable at runtime according to a priority of a sequential task.
7. (Original) The system of claim 2, wherein the processor is adapted to reduce the supply voltage when the clock frequency is reduced.
8. (Original) The system of claim 7 adapted to subsequently reduce the clock frequency in accordance with a hysteresis characteristics.
9. (Original) The system of claim 2 further comprising: a heterogeneous plurality of clocked data processing units.

10. (Original) The system of claim 9 adapted to subsequently reduce the clock frequency in accordance with a hysteresis characteristics.

11. (Currently amended) The system of claim 2, further comprising:

a plurality of temperature sensors and a heterogeneous plurality of clocked data processing units; and wherein

the multiprocessor having a plurality of regions, a temperature sensor being provided for each of said plurality of regions to measure the temperature of said specific region; and

the clock frequencies of said data processing units being dynamically adjustable in accordance with the sensed temperatures.

12. (Original) The system of claim 11 adapted to subsequently reduce the clock frequency in accordance with a hysteresis characteristics.

13. (Original) A system of claim 2 adapted to:

(i) setting a clock frequency of at least a part of the multiprocessor system to a value in accordance with a first processor load, the value being less than a maximum value;

(ii) subsequently increasing the clock frequency of the at least the part of the multiprocessor system to a maximum in accordance with a second processor load; and

- (iii) subsequently reducing the clock frequency of the at least the part of the multiprocessor system in accordance with an operating temperature threshold for preventing overtemperature.
14. (Original) The system of claim 13 adapted to subsequently reduce the clock frequency in accordance with a hysteresis characteristics.
15. (Original) The system of claim 2, wherein a low power operation mode is provided such that a first data processing unit is active while a plurality of other data processing units are deactivated.
16. (Original) The system of claim 15, wherein the first data processing unit is adapted to activate at least some of the other data processing units for data processing in response to an event.
17. (Original) The system of claim 2, wherein in the low power mode the minimum clock rate of the plurality of other units is set in accordance clock rate necessary for preserving the memory contents.
18. (Original) The system of claim 2 adapted to selectively set the clock frequency of at least some of the processing units in response to a prioritization of a task assigned.
19. (Original) The system of claim 2, wherein the plurality of data processing units are disposed within a mobile device.

20. (Currently amended) A mobile device comprising:

a multiprocessor system including: a plurality of data processing units, each of the data processing units:

(a) being programmable; and

(b) being adaptable for sequentially processing data in a clocked manner;  
and including

(c1) at least one Arithmetic Logic Unit (ALU), and

(c2) at least one data register set, for storing intermediate results in sequential data processing;

at least one bus system for at least interconnecting at least some of the data processing units, each of the data processing units being provided a supply voltage by a voltage supply;

wherein for at least some of the data processing units, the clock frequency is adjustable at runtime without affecting the clock frequency of at least one of: one other of the data processing units and the bus system; and

wherein the voltage supply is adapted to supply higher supply voltages for data processing at higher clock frequencies.

21. (Original) The mobile device of claim 20 further comprising a battery.
22. (Original) The mobile device of claim 21 further comprising a heat sink for the multiprocessor system.
23. (Original) The mobile device of claim 20, wherein for at least some of the data processing units, the clock frequency is adjustable at runtime according to a priority of a sequential task.
24. (Original) The mobile device of claim 23, wherein the processor is adapted to reduce the supply voltage when the clock frequency is reduced.
25. (Original) The mobile device of claim 24 further comprising: a heterogeneous plurality of clocked data processing units.
26. (Original) The mobile device according to claim 21 further comprising:
- a plurality of temperature sensors and a heterogeneous plurality of clocked data processing units,
- the multiprocessor having a plurality of regions, a temperature sensor being provided for each of said plurality of regions to measure the temperature of said specific region; and

the clock frequencies of said data processing units being  
dynamically adjustable in accordance with the sensed  
temperatures

27. (Original) The mobile device according to claim 21 adapted to:

- (i) setting a clock frequency of at least a part of the multiprocessor system to a value in accordance with a first processor load, the value being less than a maximum value;
- (ii) subsequently increasing the clock frequency of the at least the part of the multiprocessor system to a maximum in accordance with a second processor load; and
- (iii) subsequently reducing the clock frequency of the at least the part of the multiprocessor system in accordance with an operating temperature threshold for preventing overtemperature.

28. (Original) The mobile device according to claim 21 adapted to subsequently reduce the clock frequency in accordance with a hysteresis characteristics.

29. (Original) The mobile device according to claim 21, wherein a low power operation mode is provided such that a first data processing unit is active while a plurality of other units are deactivated.

30. (Original) The mobile device of claim 29, wherein the first entity is adapted to activate at least some of the other units for data processing in response to an event.
31. (Original) The mobile device of claim 29, wherein in the low power mode the minimum clock rate of the plurality of other units is set in accordance clock rate necessary for preserving the memory contents.
32. (Original) The mobile device of according to claim 21 adapted to selectively set the clock frequency of at least some of the processing units in response to a prioritization of a task assigned.
33. (Original) The mobile device of claim 20 wherein for at least some of the data processing units, the clock frequency is adjustable at runtime according to at least one of: a state of the multiprocessor system, a state of the data processing entity, a state of others of the data processing units, and a priority of a sequential task.
34. (Original) The mobile device according to claims 21 wherein the mobile device is a mobile computer.
35. (Currently amended) A method of operating a multiprocessor system, the multiprocessor system comprising:
- ~~sequentially processing data in a clocked manner via a plurality of data processing units, each of the data processing units being~~

a plurality of Pprogrammable data processing units, each  
~~and~~ including

at least one Arithmetic Logic Unit (ALU), and

at least one data register set for storing intermediate results  
~~in the~~for sequential data processing;

the method comprising:

sequentially processing data in a clocked manner via the plurality  
of programmable data processing units;

interconnecting at least some of the data processing units via at  
least one bus system;

supplying to at least some of the data processing units a supply  
voltage from a voltage supply; and

for at least some of the data processing units;

adjusting a clock frequency at runtime, without affecting the  
clock frequency of at least one of: one other of the data  
processing units and the bus system; and

supplying higher supply voltage for data processing at  
higher clock frequencies.

36. (Original) The method of claim 35, wherein the adjusting the clock frequency at runtime is adjusted according to a state of the multiprocessor system.
37. (Original) The method of claim 35, wherein the adjusting the clock frequency at runtime is adjusted according to a state of a least one data processing unit.
38. (Original) The method of claim 35, wherein the adjusting the clock frequency at runtime is adjusted according to a state of others data processing units.
39. (Original) The method of claim 35, wherein the adjusting the clock frequency at runtime is adjusted according to a priority of a sequential task.
40. (Original) The method according to claim 35, wherein the clock rate is set in response to an amount of data buffered for processing.
41. (Original) The method according to claim 35, wherein the clock rate is set in response to an increase rate of an amount of data buffered for processing.
42. (Original) The method according to claim 35, wherein the clock rate is set in response to a decrease rate of an amount of data buffered for processing.
43. (Original) The method according to claim 35, wherein the clock rate is set in response to a release condition for execution.

44. (Original) The method according to claim 35, wherein the clock rate is set in response to a hysteresis behavior.
45. (Original) The method according to claim 35, wherein the clock rate is set in response to one or more measured temperatures.
46. (Original) The method according to claim 35, wherein the clock rate is set in response to an overtemperature condition.

## REMARKS

Claims 2-46 are pending; 2, 20 and 35, independent. Each of the independent claims is directed to a microprocessor system having a plurality of programmable sequential data processors and each claim further requires a register set for storing intermediate results for sequential data processing. According to the specification, at [0025], a sequential data processor may pass onto one or more other processors for subsequent processing of data. Paragraph [0019] describes that the multiprocessor system may have a register unit or set which may be assigned the remaining processors such subsequent sequential data processing.

Sequential data processors process a set of data using one or more arithmetic or logic operations on sets of *data* as opposed to the more common general purpose data processor that typically executes one instruction on a pair of input operands before loading and executing the next *instruction*. The more general processor is generally known as a sequential instruction processor.

While the present invention certainly includes controlling the clocking of the various processors to prevent over-temperature conditions, the invention is broader than that because it includes controlling the clocking without regard to temperature. For example, when configurations of processors are limited by their interconnections (space, capacitance and other factors) such that propagation time is affected, the various processors can be separately clocked according to

their functional and timing requirements. See, e.g., paragraph [0024]. Because their data results might be needed by subsequent processors, when particular processor configurations are computationally more complex and take more time, they might need to be clocked at a higher rate. It is significant therefor that the present invention involves and is limited to processors of the sequential data processor type that have data register sets for storing intermediate results for subsequent data processing by sequential data processors, but not limited to controlling processing to respond to temperature conditions.

The examiner has rejected all claims over Kikinis, US. Pat. No. 5,502,838. However, Kikinis does not disclose a multiprocessor system comprising sequential data processors. All the Kikinis processors are conventional processors and all the same architecture. See, the architecture disclosed in Fig. 2, and at, e.g., 5:10-9-13, where “computational and logic load [may be shifted] for one microprocessor to another, fighting load management to limit temperature rise.” Such shifting of computational load is only possible if the computations are not affected by the microprocessor selected. In contrast, as well known, with sequential data processing architectures, where results in one processor are fed to another, for each to perform a separate computation that may be computationally different from the other processors. Because they also depend upon each other, i.e., the results of one are fed to the next, it is not always possible to speed up or slow down one in a plurality of computationally interconnected processors for “temperature reasons” without affecting the others in terms of performance.

In serial data processors, in contrast, where one has more calculations to do than another, or where the processing of one processor takes longer than another for any reason, it is highly desirable to speed up the processing of the one that is the slowest.

Applicant respectfully submits that the claims are limited to sequential data processors that have register sets for storing data for sequential data processing, and neither are disclosed in Kikinis. Kikinis relates only to data processors of conventional architecture or at least which all have the same processor design. These limitations are significant and define over Kikinis. Applicant therefore respectfully traverses the rejections of all claims over Kikinis.

Applicant also wishes to respectfully bring the examiner's attention to claims 5, 33 and 38 that all require, in varying language, that the "the clock frequency is adjustable at runtime according to a state of others of the data processing units." This requires coordination of the frequency of one data processor to accommodate the needs of another. As described, e.g., at [0023] and [0024], when one processor has more processing to do, or is slower or faster than another for any reason, the two processors or groups of interrelated sequential data processors may be frequency controlled to coordinate processing. Nothing of the sort is disclosed in Kikinis.

Finally, applicant wishes to point to the requirement for a *hysteresis* in claims 8, 10, 12, 14, 28 and 44. According to the specification, e.g. at [0107], hysteresis is a beneficial characteristic to

determine clock rates when temperature sensitive change of the clock frequencies is to be performed. Nothing of the sort is described the Kikinis.

Applicant has introduced minor punctuation and other such changes to the independent claims only for the purposes of clarity. Applicant respectfully request reconsideration based in view of the above remarks.

Respectfully Submitted,

Date: Wednesday, August 10, 2016

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| Electronic Acknowledgement Receipt          |                                                                                 |
|---------------------------------------------|---------------------------------------------------------------------------------|
| <b>EFS ID:</b>                              | 26606152                                                                        |
| <b>Application Number:</b>                  | 14219945                                                                        |
| <b>International Application Number:</b>    |                                                                                 |
| <b>Confirmation Number:</b>                 | 7671                                                                            |
| <b>Title of Invention:</b>                  | Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply |
| <b>First Named Inventor/Applicant Name:</b> | Martin VORBACH                                                                  |
| <b>Customer Number:</b>                     | 73481                                                                           |
| <b>Filer:</b>                               | Edward Peter Heller                                                             |
| <b>Filer Authorized By:</b>                 |                                                                                 |
| <b>Attorney Docket Number:</b>              | PACT-025-PCT-US-D1-2C1-D1                                                       |
| <b>Receipt Date:</b>                        | 10-AUG-2016                                                                     |
| <b>Filing Date:</b>                         | 19-MAR-2014                                                                     |
| <b>Time Stamp:</b>                          | 16:44:59                                                                        |
| <b>Application Type:</b>                    | Utility under 35 USC 111(a)                                                     |

### Payment information:

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| 1               | Amendment/Req. Reconsideration-After Non-Final Reject | PACT-025-PCT-US-D1-2C1-D1-ROA.pdf | 200378<br><br>14a56845a813a658939be1b3a57e86ce47a894ca | no               | 16               |

### Warnings:

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| <b>Information:</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             |        |
| <b>Total Files Size (in bytes):</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 200378 |
| <p>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b><br/> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b><br/> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b><br/> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p> |        |

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

| PATENT APPLICATION FEE DETERMINATION RECORD                                                                                     |                                                                                                                                                                                                                               |                                  |       | Application or Docket Number       |               | Filing Date     |  | <input type="checkbox"/> To be Mailed |  |
|---------------------------------------------------------------------------------------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------------------------|-------|------------------------------------|---------------|-----------------|--|---------------------------------------|--|
| Substitute for Form PTO-875                                                                                                     |                                                                                                                                                                                                                               |                                  |       | 14/219,945                         |               | 03/19/2014      |  |                                       |  |
| ENTITY: <input checked="" type="checkbox"/> LARGE <input type="checkbox"/> SMALL <input type="checkbox"/> MICRO                 |                                                                                                                                                                                                                               |                                  |       |                                    |               |                 |  |                                       |  |
| APPLICATION AS FILED – PART I                                                                                                   |                                                                                                                                                                                                                               |                                  |       |                                    |               |                 |  |                                       |  |
| (Column 1)                                                                                                                      |                                                                                                                                                                                                                               | (Column 2)                       |       |                                    |               |                 |  |                                       |  |
| FOR                                                                                                                             | NUMBER FILED                                                                                                                                                                                                                  | NUMBER EXTRA                     |       | RATE (\$)                          |               | FEE (\$)        |  |                                       |  |
| <input type="checkbox"/> BASIC FEE<br>(37 CFR 1.16(a), (b), or (c))                                                             | N/A                                                                                                                                                                                                                           | N/A                              |       | N/A                                |               |                 |  |                                       |  |
| <input type="checkbox"/> SEARCH FEE<br>(37 CFR 1.16(k), (i), or (m))                                                            | N/A                                                                                                                                                                                                                           | N/A                              |       | N/A                                |               |                 |  |                                       |  |
| <input type="checkbox"/> EXAMINATION FEE<br>(37 CFR 1.16(o), (p), or (q))                                                       | N/A                                                                                                                                                                                                                           | N/A                              |       | N/A                                |               |                 |  |                                       |  |
| TOTAL CLAIMS<br>(37 CFR 1.16(i))                                                                                                | minus 20 =                                                                                                                                                                                                                    | *                                |       | X \$ =                             |               |                 |  |                                       |  |
| INDEPENDENT CLAIMS<br>(37 CFR 1.16(h))                                                                                          | minus 3 =                                                                                                                                                                                                                     | *                                |       | X \$ =                             |               |                 |  |                                       |  |
| <input type="checkbox"/> APPLICATION SIZE FEE<br>(37 CFR 1.16(s))                                                               | If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s). |                                  |       |                                    |               |                 |  |                                       |  |
| <input type="checkbox"/> MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))                                                      |                                                                                                                                                                                                                               |                                  |       |                                    |               |                 |  |                                       |  |
| * If the difference in column 1 is less than zero, enter "0" in column 2.                                                       |                                                                                                                                                                                                                               |                                  |       | TOTAL                              |               |                 |  |                                       |  |
| APPLICATION AS AMENDED – PART II                                                                                                |                                                                                                                                                                                                                               |                                  |       |                                    |               |                 |  |                                       |  |
| (Column 1)                                                                                                                      |                                                                                                                                                                                                                               | (Column 2)                       |       | (Column 3)                         |               |                 |  |                                       |  |
| AMENDMENT                                                                                                                       | 08/10/2016                                                                                                                                                                                                                    | CLAIMS REMAINING AFTER AMENDMENT |       | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE (\$)       |  | ADDITIONAL FEE (\$)                   |  |
|                                                                                                                                 | Total (37 CFR 1.16(i))                                                                                                                                                                                                        | * 45                             | Minus | ** 45                              | = 0           | X \$80 =        |  | 0                                     |  |
|                                                                                                                                 | Independent (37 CFR 1.16(h))                                                                                                                                                                                                  | * 3                              | Minus | ***3                               | = 0           | X \$420 =       |  | 0                                     |  |
|                                                                                                                                 | <input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))                                                                                                                                                                |                                  |       |                                    |               |                 |  |                                       |  |
|                                                                                                                                 | <input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))                                                                                                                                      |                                  |       |                                    |               |                 |  |                                       |  |
|                                                                                                                                 |                                                                                                                                                                                                                               |                                  |       |                                    |               | TOTAL ADD'L FEE |  | 0                                     |  |
| (Column 1)                                                                                                                      |                                                                                                                                                                                                                               | (Column 2)                       |       | (Column 3)                         |               |                 |  |                                       |  |
| AMENDMENT                                                                                                                       |                                                                                                                                                                                                                               | CLAIMS REMAINING AFTER AMENDMENT |       | HIGHEST NUMBER PREVIOUSLY PAID FOR | PRESENT EXTRA | RATE (\$)       |  | ADDITIONAL FEE (\$)                   |  |
|                                                                                                                                 | Total (37 CFR 1.16(i))                                                                                                                                                                                                        | *                                | Minus | **                                 | =             | X \$ =          |  |                                       |  |
|                                                                                                                                 | Independent (37 CFR 1.16(h))                                                                                                                                                                                                  | *                                | Minus | ***                                | =             | X \$ =          |  |                                       |  |
|                                                                                                                                 | <input type="checkbox"/> Application Size Fee (37 CFR 1.16(s))                                                                                                                                                                |                                  |       |                                    |               |                 |  |                                       |  |
|                                                                                                                                 | <input type="checkbox"/> FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))                                                                                                                                      |                                  |       |                                    |               |                 |  |                                       |  |
|                                                                                                                                 |                                                                                                                                                                                                                               |                                  |       |                                    |               | TOTAL ADD'L FEE |  |                                       |  |
| * If the entry in column 1 is less than the entry in column 2, write "0" in column 3.                                           |                                                                                                                                                                                                                               |                                  |       |                                    |               |                 |  |                                       |  |
| ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20".                                       |                                                                                                                                                                                                                               |                                  |       |                                    |               |                 |  |                                       |  |
| *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3".                                        |                                                                                                                                                                                                                               |                                  |       |                                    |               |                 |  |                                       |  |
| The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1. |                                                                                                                                                                                                                               |                                  |       |                                    |               |                 |  |                                       |  |

This collection of information is required by 37 CFR 1.16. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

If you need assistance in completing the form, call 1-800-PTO-9199 and select option 2.



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
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www.uspto.gov

## NOTICE OF ALLOWANCE AND FEE(S) DUE

73481 7590 12/02/2016  
Alliacense Limited LLC  
2310 Homestead Rd  
# C1-505  
Los Altos, CA 94024-7339

EXAMINER

ELAMIN, ABDELMONIEM I

ART UNIT PAPER NUMBER

2116

DATE MAILED: 12/02/2016

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.       | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------------|------------------|
| 14/219,945      | 03/19/2014  | Martin VORBACH       | PACT-025-PCT-US-D1-2C1-D1 | 7671             |

TITLE OF INVENTION: Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply

| APPLN. TYPE    | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE   |
|----------------|---------------|---------------|---------------------|----------------------|------------------|------------|
| nonprovisional | UNDISCOUNTED  | \$960         | \$0                 | \$0                  | \$960            | 03/02/2017 |

**THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.**

**THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.**

### HOW TO REPLY TO THIS NOTICE:

I. Review the ENTITY STATUS shown above. If the ENTITY STATUS is shown as SMALL or MICRO, verify whether entitlement to that entity status still applies.

If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

For purposes of this notice, small entity fees are 1/2 the amount of undiscounted fees, and micro entity fees are 1/2 the amount of small entity fees.

II. PART B - FEE(S) TRANSMITTAL, or its equivalent, must be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted. If an equivalent of Part B is filed, a request to reapply a previously paid issue fee must be clearly made, and delays in processing may occur due to the difficulty in recognizing the paper as an equivalent of Part B.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

**IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.**

**PART B - FEE(S) TRANSMITTAL**

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

73481 7590 12/02/2016  
Alliacense Limited LLC  
2310 Homestead Rd  
# C1-505  
Los Altos, CA 94024-7339

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

**Certificate of Mailing or Transmission**

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

|                    |
|--------------------|
| (Depositor's name) |
| (Signature)        |
| (Date)             |

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.       | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------------|------------------|
| 14/219,945      | 03/19/2014  | Martin VORBACH       | PACT-025-PCT-US-D1-2C1-D1 | 7671             |

TITLE OF INVENTION: Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply

| APPLN. TYPE    | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE   |
|----------------|---------------|---------------|---------------------|----------------------|------------------|------------|
| nonprovisional | UNDISCOUNTED  | \$960         | \$0                 | \$0                  | \$960            | 03/02/2017 |

| EXAMINER              | ART UNIT | CLASS-SUBCLASS |
|-----------------------|----------|----------------|
| ELAMIN, ABDELMONIEM I | 2116     | 713-322000     |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, 1 \_\_\_\_\_
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 2 \_\_\_\_\_
- 3 \_\_\_\_\_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies \_\_\_\_\_

4b. Payment of Fee(s): (**Please first reapply any previously paid issue fee shown above**)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number \_\_\_\_\_ (enclose an extra copy of this form).

5. **Change in Entity Status** (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

**NOTE:** Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

**NOTE:** If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

**NOTE:** Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature \_\_\_\_\_

Date \_\_\_\_\_

Typed or printed name \_\_\_\_\_

Registration No. \_\_\_\_\_



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|                                                                                     |             |                      |                           |                  |
|-------------------------------------------------------------------------------------|-------------|----------------------|---------------------------|------------------|
| APPLICATION NO.                                                                     | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.       | CONFIRMATION NO. |
| 14/219,945                                                                          | 03/19/2014  | Martin VORBACH       | PACT-025-PCT-US-D1-2C1-D1 | 7671             |
| 73481                                                                               | 7590        | 12/02/2016           | EXAMINER                  |                  |
| Alliacense Limited LLC<br>2310 Homestead Rd<br># C1-505<br>Los Altos, CA 94024-7339 |             |                      | ELAMIN, ABDELMONIEM I     |                  |
|                                                                                     |             |                      | ART UNIT                  | PAPER NUMBER     |
|                                                                                     |             |                      | 2116                      |                  |

DATE MAILED: 12/02/2016

## Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

## OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450. Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

### Privacy Act Statement

**The Privacy Act of 1974 (P.L. 93-579)** requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

|                               |                                       |                                       |                                                  |
|-------------------------------|---------------------------------------|---------------------------------------|--------------------------------------------------|
| <b>Notice of Allowability</b> | <b>Application No.</b><br>14/219,945  | <b>Applicant(s)</b><br>VORBACH ET AL. |                                                  |
|                               | <b>Examiner</b><br>ABDELMONIEM ELAMIN | <b>Art Unit</b><br>2116               | <b>AIA (First Inventor to File) Status</b><br>No |

**-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--**

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendment filed on 08/10/2016.  
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on \_\_\_\_\_.
2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on \_\_\_\_\_; the restriction requirement and election have been incorporated into this action.
3. ☒ The allowed claim(s) is/are 2-46. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see [http://www.uspto.gov/patents/init\\_events/pph/index.jsp](http://www.uspto.gov/patents/init_events/pph/index.jsp) or send an inquiry to PPHfeedback@uspto.gov.
4. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

**Certified copies:**

- a) ☒ All    b) ☐ Some    \*c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
  2. ☒ Certified copies of the priority documents have been received in Application No. 13/653,639.
  3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

\* Certified copies not received: \_\_\_\_\_.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.

**THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.**

5. ☐ CORRECTED DRAWINGS ( as "replacement sheets") must be submitted.  
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date \_\_\_\_\_.  
**Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).**
6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

**Attachment(s)**

- |                                                                                                            |                                                                           |
|------------------------------------------------------------------------------------------------------------|---------------------------------------------------------------------------|
| 1. <input type="checkbox"/> Notice of References Cited (PTO-892)                                           | 5. <input checked="" type="checkbox"/> Examiner's Amendment/Comment       |
| 2. <input type="checkbox"/> Information Disclosure Statements (PTO/SB/08),<br>Paper No./Mail Date _____    | 6. <input type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| 3. <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit<br>of Biological Material | 7. <input type="checkbox"/> Other _____.                                  |
| 4. <input type="checkbox"/> Interview Summary (PTO-413),<br>Paper No./Mail Date _____.                     |                                                                           |

/ABDELMONIEM ELAMIN/  
Primary Examiner, Art Unit 2116

1. The present application is being examined under the pre-AIA first to invent provisions.

**EXAMINER'S AMENDMENT**

2. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

**IN THE SPECIFICATION:**

Please amend specification as follows:

On page 1, before "FIELD OF THE INVENTION," insert the following:

--BENEFIT CLAIM

This application is a divisional of U.S. Pat. App. Ser. No. 13/653,639, filed Oct. 17, 2012, now US Pat. No. 9,075,605, which is a continuation of U.S. Pat. App. Ser. No. 12/570,984, filed on September 30, 2009, now US Pat. No. 8,312,301, which is a continuation of U.S. Pat. App. Ser. No. 12/257,075, filed on October 23, 2008, now US Pat. No. 8,099,618, which is a divisional of U.S. Pat. App. Ser. No. 10/469,909, filed on September 21, 2004, now US Pat. No. 7,444,531, which is a national phase of Int. Pat. App. No. PCT/EP02/02402, filed on March 5, 2002, which claims priority to German Patent Application Serial No. DE 101 10 530.4, filed on March 5, 2001, the entire contents of each of which are expressly incorporated herein by reference thereto.--

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ABDELMONIEM ELAMIN whose telephone number is (571)272-3674. The examiner can normally be reached on MON - FRI 10:00 AM - 6:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim Huynh can be reached on 571-272-4147. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/ABDELMONIEM ELAMIN/  
Primary Examiner, Art Unit 2116

November 22, 2016

|                                                                                                                  |                                            |                                                                  |  |
|------------------------------------------------------------------------------------------------------------------|--------------------------------------------|------------------------------------------------------------------|--|
| <b>Issue Classification</b><br> | <b>Application/Control No.</b><br>14219945 | <b>Applicant(s)/Patent Under Reexamination</b><br>VORBACH ET AL. |  |
|                                                                                                                  | <b>Examiner</b><br>M ELAMIN                | <b>Art Unit</b><br>2116                                          |  |

| CPC    |  |    |  |      |      |            |
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| Symbol |  |    |  |      | Type | Version    |
| G06F   |  | 1  |  | 324  | F    | 2013-01-01 |
| G06F   |  | 1  |  | 206  | I    | 2013-01-01 |
| G06F   |  | 1  |  | 3296 | I    | 2013-01-01 |
| Y02B   |  | 60 |  | 1217 | A    | 2013-01-01 |
| Y02B   |  | 60 |  | 1285 | A    | 2013-01-01 |
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| NONE                                         |            | <b>Total Claims Allowed:</b> |                   |
| (Assistant Examiner)                         | (Date)     | 45                           |                   |
| /M ELAMIN/<br>Primary Examiner.Art Unit 2116 | 11/22/2016 | O.G. Print Claim(s)          | O.G. Print Figure |
| (Primary Examiner)                           | (Date)     | 1                            | 2                 |

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|------------------------------------------------------------------------------------------------------------------|--------------------------------------------|------------------------------------------------------------------|
| <b>Issue Classification</b><br> | <b>Application/Control No.</b><br>14219945 | <b>Applicant(s)/Patent Under Reexamination</b><br>VORBACH ET AL. |
|                                                                                                                  | <b>Examiner</b><br>M ELAMIN                | <b>Art Unit</b><br>2116                                          |

| US ORIGINAL CLASSIFICATION |                                   |          |  |  |  | INTERNATIONAL CLASSIFICATION |   |   |   |                     |             |  |  |  |  |  |  |  |  |  |
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| CLASS                      |                                   | SUBCLASS |  |  |  | CLAIMED                      |   |   |   |                     | NON-CLAIMED |  |  |  |  |  |  |  |  |  |
|                            |                                   |          |  |  |  | G                            | 0 | 6 | F | 1 / 32 (2006.01.01) |             |  |  |  |  |  |  |  |  |  |
| CROSS REFERENCE(S)         |                                   |          |  |  |  |                              |   |   |   |                     |             |  |  |  |  |  |  |  |  |  |
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| NONE                                         |            | <b>Total Claims Allowed:</b> |                   |
|                                              |            | 45                           |                   |
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| /M ELAMIN/<br>Primary Examiner.Art Unit 2116 | 11/22/2016 | O.G. Print Claim(s)          | O.G. Print Figure |
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| <b>Issue Classification</b><br> | <b>Application/Control No.</b><br>14219945 | <b>Applicant(s)/Patent Under Reexamination</b><br>VORBACH ET AL. |
|                                                                                                                  | <b>Examiner</b><br>M ELAMIN                | <b>Art Unit</b><br>2116                                          |

| <input type="checkbox"/> <b>Claims renumbered in the same order as presented by applicant</b> <input type="checkbox"/> <b>CPA</b> <input type="checkbox"/> <b>T.D.</b> <input type="checkbox"/> <b>R.1.47</b> |          |       |          |       |          |       |          |       |          |       |          |       |          |       |          |
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| Final                                                                                                                                                                                                         | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original | Final | Original |
| -                                                                                                                                                                                                             | 1        | 16    | 17       | 32    | 33       |       |          |       |          |       |          |       |          |       |          |
| 1                                                                                                                                                                                                             | 2        | 17    | 18       | 33    | 34       |       |          |       |          |       |          |       |          |       |          |
| 2                                                                                                                                                                                                             | 3        | 18    | 19       | 34    | 35       |       |          |       |          |       |          |       |          |       |          |
| 3                                                                                                                                                                                                             | 4        | 19    | 20       | 35    | 36       |       |          |       |          |       |          |       |          |       |          |
| 4                                                                                                                                                                                                             | 5        | 20    | 21       | 36    | 37       |       |          |       |          |       |          |       |          |       |          |
| 5                                                                                                                                                                                                             | 6        | 21    | 22       | 37    | 38       |       |          |       |          |       |          |       |          |       |          |
| 6                                                                                                                                                                                                             | 7        | 22    | 23       | 38    | 39       |       |          |       |          |       |          |       |          |       |          |
| 7                                                                                                                                                                                                             | 8        | 23    | 24       | 39    | 40       |       |          |       |          |       |          |       |          |       |          |
| 8                                                                                                                                                                                                             | 9        | 24    | 25       | 40    | 41       |       |          |       |          |       |          |       |          |       |          |
| 9                                                                                                                                                                                                             | 10       | 25    | 26       | 41    | 42       |       |          |       |          |       |          |       |          |       |          |
| 10                                                                                                                                                                                                            | 11       | 26    | 27       | 42    | 43       |       |          |       |          |       |          |       |          |       |          |
| 11                                                                                                                                                                                                            | 12       | 27    | 28       | 43    | 44       |       |          |       |          |       |          |       |          |       |          |
| 12                                                                                                                                                                                                            | 13       | 28    | 29       | 44    | 45       |       |          |       |          |       |          |       |          |       |          |
| 13                                                                                                                                                                                                            | 14       | 29    | 30       | 45    | 46       |       |          |       |          |       |          |       |          |       |          |
| 14                                                                                                                                                                                                            | 15       | 30    | 31       |       |          |       |          |       |          |       |          |       |          |       |          |
| 15                                                                                                                                                                                                            | 16       | 31    | 32       |       |          |       |          |       |          |       |          |       |          |       |          |

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| NONE<br><br>(Assistant Examiner) _____ (Date) _____                                       |  | <b>Total Claims Allowed:</b><br>45 |                        |
| /M ELAMIN/<br>Primary Examiner.Art Unit 2116<br><br>(Primary Examiner) _____ (Date) _____ |  | O.G. Print Claim(s)<br>1           | O.G. Print Figure<br>2 |



PALM INTRANET

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Date: 11/22/2016  
Time: 11:45:35

**Inventor Name Search Result**

Your Search was:

Last Name = BAUMGARTE

First Name = VOLKER

| Application#             | Patent#                 | PG Pub#     | Status | Date Filed | Title                                                                          | Examiner Name      | Inventor Name     |
|--------------------------|-------------------------|-------------|--------|------------|--------------------------------------------------------------------------------|--------------------|-------------------|
| <a href="#">10297959</a> | <a href="#">7003660</a> | 20040025005 | 150    | 06/19/2003 | PIPELINE CONFIGURATION UNIT PROTOCOLS AND COMMUNICATION                        | ELAMIN,ABDELMONIEM | BAUMGARTE, VOLKER |
| <a href="#">10398546</a> | <a href="#">7595659</a> | 20040128474 | 150    | 01/20/2004 | LOGIC CELL ARRAY AND BUS SYSTEM                                                | TAN,VIBOL          | BAUMGARTE, VOLKER |
| <a href="#">10469909</a> | <a href="#">7444531</a> | 20050066213 | 150    | 09/21/2004 | METHODS AND DEVICES FOR TREATING AND PROCESSING DATA                           | ELAMIN,ABDELMONIEM | BAUMGARTE, VOLKER |
| <a href="#">10469910</a> | Not Issued              | 20070299993 | 161    | 02/17/2005 | Method and Device for Treating and Processing Data                             | MAMO,ELIAS         | BAUMGARTE, VOLKER |
| <a href="#">10501845</a> | <a href="#">8281108</a> | 20060090062 | 150    | 08/26/2005 | RECONFIGURABLE GENERAL PURPOSE PROCESSOR HAVING TIME RESTRICTED CONFIGURATIONS | VICARY,KEITH       | BAUMGARTE, VOLKER |
| <a href="#">10504684</a> | <a href="#">8127061</a> | 20070150637 | 150    | 07/14/2006 | BUS SYSTEMS AND RECONFIGURATION METHODS                                        | CLEARY,THOMAS      | BAUMGARTE, VOLKER |
| <a href="#">10523764</a> | <a href="#">8156284</a> | 20070050603 | 150    | 08/02/2005 | DATA PROCESSING METHOD AND DEVICE                                              | THAI,TUAN          | BAUMGARTE, VOLKER |
| <a href="#">11122500</a> | <a href="#">8301872</a> | 20050223212 | 150    | 05/04/2005 | PIPELINE CONFIGURATION PROTOCOL AND CONFIGURATION UNIT COMMUNICATION           | ELAMIN,ABDELMONIEM | BAUMGARTE, VOLKER |
| <a href="#">12257075</a> | <a href="#">8099618</a> | 20090100286 | 150    | 10/23/2008 | METHODS AND DEVICES FOR TREATING AND PROCESSING DATA                           | ELAMIN,ABDELMONIEM | BAUMGARTE, VOLKER |
| <a href="#">12371040</a> | <a href="#">8058899</a> | 20090146691 | 150    | 02/13/2009 | LOGIC CELL ARRAY AND BUS SYSTEM                                                | TAN,VIBOL          | BAUMGARTE, VOLKER |
| <a href="#">12389116</a> | Not Issued              | 20090210653 | 161    | 02/19/2009 | METHOD AND DEVICE FOR TREATING AND PROCESSING DATA                             | VICARY,KEITH       | BAUMGARTE, VOLKER |

|                          |                         |             |     |            |                                                                                     |                    |                   |
|--------------------------|-------------------------|-------------|-----|------------|-------------------------------------------------------------------------------------|--------------------|-------------------|
| <a href="#">12570943</a> | <a href="#">8914590</a> | 20100153654 | 150 | 09/30/2009 | DATA PROCESSING METHOD AND DEVICE                                                   | THAI,TUAN          | BAUMGARTE, VOLKER |
| <a href="#">12570984</a> | <a href="#">8312301</a> | 20100023796 | 150 | 09/30/2009 | METHODS AND DEVICES FOR TREATING AND PROCESSING DATA                                | ELAMIN,ABDELMONIEM | BAUMGARTE, VOLKER |
| <a href="#">12743356</a> | Not Issued              | 20100281235 | 161 | 06/29/2010 | RECONFIGURABLE FLOATING-POINT AND BIT-LEVEL DATA PROCESSING UNIT                    | PETRANEK,JACOB     | BAUMGARTE, VOLKER |
| <a href="#">13289296</a> | <a href="#">8471593</a> | 20120072699 | 150 | 11/04/2011 | LOGIC CELL ARRAY AND BUS SYSTEM                                                     | TAN,VIBOL          | BAUMGARTE, VOLKER |
| <a href="#">13324048</a> | Not Issued              | 20120151113 | 161 | 12/13/2011 | BUS SYSTEMS AND METHODS FOR CONTROLLING DATA FLOW IN A FIELD OF PROCESSING ELEMENTS | CLEARY,THOMAS      | BAUMGARTE, VOLKER |
| <a href="#">13491894</a> | <a href="#">8468329</a> | 20120311301 | 150 | 06/08/2012 | PIPELINE CONFIGURATION PROTOCOL AND CONFIGURATION UNIT COMMUNICATION                | ELAMIN,ABDELMONIEM | BAUMGARTE, VOLKER |
| <a href="#">13653639</a> | <a href="#">9075605</a> | 20130042137 | 150 | 10/17/2012 | METHODS AND DEVICES FOR TREATING AND PROCESSING DATA                                | ELAMIN,ABDELMONIEM | BAUMGARTE, VOLKER |
| <a href="#">13872779</a> | Not Issued              | 20140325175 | 161 | 04/29/2013 | PIPELINE CONFIGURATION PROTOCOL AND CONFIGURATION UNIT COMMUNICATION                | ROSSITER,SEAN      | BAUMGARTE, VOLKER |
| <a href="#">13903470</a> | <a href="#">9047440</a> | 20140359254 | 150 | 05/28/2013 | LOGICAL CELL ARRAY AND BUS SYSTEM                                                   | TAN,VIBOL          | BAUMGARTE, VOLKER |
| <a href="#">14219945</a> | Not Issued              | 20140208143 | 71  | 03/19/2014 | Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply     | ELAMIN,ABDELMONIEM | BAUMGARTE, VOLKER |
| <a href="#">14318211</a> | <a href="#">9250908</a> | 20140310466 | 150 | 06/27/2014 | Multi-processor bus and cache interconnection system                                | MISIURA,BRIAN      | BAUMGARTE, VOLKER |
| <a href="#">14465157</a> | Not Issued              | 20150033000 | 61  | 08/21/2014 | Parallel Processing Array of Arithmetic Unit having a Barrier Instruction           | MEHTA,JYOTI        | BAUMGARTE, VOLKER |
| <a href="#">14500618</a> | <a href="#">9141390</a> | 20150026431 | 150 | 09/29/2014 | Method of Processing Data with an Array of Data Processors According to             | NGUYEN,THAN        | BAUMGARTE, VOLKER |

|                          |                         |             |     |            | Application ID                                                                                |             |                   |
|--------------------------|-------------------------|-------------|-----|------------|-----------------------------------------------------------------------------------------------|-------------|-------------------|
| <a href="#">14572643</a> | <a href="#">9170812</a> | 20150106596 | 150 | 12/16/2014 | Data Processing System Having Integrated Pipelined Array Data Processor                       | THAI,TUAN   | BAUMGARTE, VOLKER |
| <a href="#">14718516</a> | <a href="#">9256575</a> | 20150261722 | 150 | 05/21/2015 | DATA PROCESSOR CHIP WITH FLEXIBLE BUS SYSTEM                                                  | TAN,VIBOL   | BAUMGARTE, VOLKER |
| <a href="#">14728422</a> | <a href="#">9411532</a> | 20150261474 | 150 | 06/02/2015 | Methods and Systems for Transferring Data between a Processing Device and External Devices    | SUN,MICHAEL | BAUMGARTE, VOLKER |
| <a href="#">14923702</a> | Not Issued              | 20160055120 | 61  | 10/27/2015 | Integrated data processing core and array data processor and method for processing algorithms | THAI,TUAN   | BAUMGARTE, VOLKER |
| <a href="#">15018376</a> | Not Issued              | 20160154758 | 51  | 02/08/2016 | Array Processor Having a Segmented Bus System                                                 | TAN,VIBOL   | BAUMGARTE, VOLKER |
| <a href="#">15225638</a> | Not Issued              | 0           | 30  | 08/01/2016 | Method of Transferring Data between External Devices and an Array Processor                   | SUN,MICHAEL | BAUMGARTE, VOLKER |
| <a href="#">60238855</a> | Not Issued              |             | 159 | 10/06/2000 | Dataprocessor and applications                                                                | ,           | BAUMGARTE, VOLKER |

Inventor Search Completed: No Records to Display.

Search Another: Inventor
 

|                                        |                                     |
|----------------------------------------|-------------------------------------|
| Last Name                              | First Name                          |
| <input type="text" value="BAUMGARTE"/> | <input type="text" value="VOLKER"/> |

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|                                                                                                              |                                                |                                                                      |
|--------------------------------------------------------------------------------------------------------------|------------------------------------------------|----------------------------------------------------------------------|
| <b>Search Notes</b><br><br> | <b>Application/Control No.</b><br><br>14219945 | <b>Applicant(s)/Patent Under Reexamination</b><br><br>VORBACH ET AL. |
|                                                                                                              | <b>Examiner</b><br><br>M ELAMIN                | <b>Art Unit</b><br><br>2116                                          |

| CPC- SEARCHED |            |          |
|---------------|------------|----------|
| Symbol        | Date       | Examiner |
| G06F1/206     | 11/22/2016 | AE       |
| G06F1/324     | 11/22/2016 | AE       |
| G06F1/3296    | 11/22/2016 | AE       |
| Y02B60/1217   | 11/22/2016 | AE       |
| Y02B60/1285   | 11/22/2016 | AE       |

| CPC COMBINATION SETS - SEARCHED |      |          |
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| Symbol                          | Date | Examiner |
|                                 |      |          |

| US CLASSIFICATION SEARCHED |          |      |          |
|----------------------------|----------|------|----------|
| Class                      | Subclass | Date | Examiner |
|                            |          |      |          |

| SEARCH NOTES             |            |          |
|--------------------------|------------|----------|
| Search Notes             | Date       | Examiner |
| WEST                     | 5/10/2016  | AE       |
| WEST                     | 5/11/2016  | AE       |
| WEST                     | 11/22/2016 | AE       |
| CLASS/SUBCLASS WITH TEXT | 11/22/2016 | AE       |
| INVENTOR'S NAME SEARCH   | 11/22/2016 | AE       |

| INTERFERENCE SEARCH     |                         |            |          |
|-------------------------|-------------------------|------------|----------|
| US Class/<br>CPC Symbol | US Subclass / CPC Group | Date       | Examiner |
| G06F                    | 1/206, 1/324, 1/3296    | 11/22/2016 | AE       |
| Y02B                    | 60/1217, 60/1285        | 11/22/2016 | AE       |

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|--|---------------------------------------------------------|
|  | /ABDELMONIEM ELAMIN/<br>Primary Examiner, Art Unit 2116 |
|--|---------------------------------------------------------|



Day : Tuesday  
Date: 11/22/2016  
Time: 11:45:08

**Inventor Name Search Result**

Your Search was:

Last Name = VORBACH

First Name = MARTIN

| Application#             | Patent#                 | PG Pub# | Status | Date Filed | Title                                                                                                                                                                                                                  | Examiner Name  | Inventor Name   |
|--------------------------|-------------------------|---------|--------|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|-----------------|
| <a href="#">08946810</a> | <a href="#">6425068</a> |         | 150    | 10/08/1997 | UNIT FOR PROCESSING NUMERICAL AND LOGICAL OPERATIONS FOR USE IN CENTRAL PROCESSING UNITS (CPUS), MULTIPROCESSOR SYSTEMS, DATA - FLOW PROCESSORS (DSPS), SYSTOLIC PROCESSORS AND FIELD PROGRAMMABLE GATE ARRAYS (FPGAS) | ELLIS,RICHARD  | VORBACH, MARTIN |
| <a href="#">08946811</a> | Not Issued              |         | 169    | 10/08/1997 | INTERNAL BUS SYSTEM FOR DFPS AS WELL AS MODULES HAVING TWO OR MULTI DIMENSIONAL PROGRAMMABLE CELL STRUCTURES FOR MANAGING LARGE QUNATITIES OF DATA ENTAILING A HIGH NETWORKING COMPLEXITY                              |                | VORBACH, MARTIN |
| <a href="#">08946812</a> | <a href="#">6081903</a> |         | 150    | 10/08/1997 | METHOD OF THE SELF-SYNCHRONIZATION OF CONFIGURABLE ELEMENTS OF A PROGRAMMABLE UNIT                                                                                                                                     | BUTLER,DENNIS  | VORBACH, MARTIN |
| <a href="#">08946998</a> | <a href="#">6021490</a> |         | 150    | 10/08/1997 | RUN-TIME RECONFIGURATION METHOD FOR PROGRAMMABLE UNITS                                                                                                                                                                 | HECKLER,THOMAS | VORBACH, MARTIN |
| <a href="#">08946999</a> | <a href="#">6032650</a> |         | 150    | 10/08/1997 | METHOD FOR THE AUTOMATIC ADDRESS GENERATION OF MODULES WITHIN                                                                                                                                                          | NGUYEN,THAN    | VORBACH, MARTIN |

|                          |                         |  |     |            |                                                                                                                                                                                                                      |                |                    |
|--------------------------|-------------------------|--|-----|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|--------------------|
|                          |                         |  |     |            | CLUSTERS<br>COMPRISED OF A<br>PLURALITY OF<br>THESE MODULES                                                                                                                                                          |                |                    |
| <a href="#">08947002</a> | <a href="#">6088793</a> |  | 150 | 10/08/1997 | PROCESS FOR<br>AUTOMATIC<br>DYNAMIC<br>RELOADING OF<br>DATA-FLOW<br>PROCESSORS (DFPS)<br>AND UNITS WITH<br>TWO-OR THREE-<br>DIMENSIONAL<br>PROGRAMMABLE<br>CELL<br>ARCHITECTURES<br>(FPGAS, DPGAS AND<br>THE LIKE)   | MAI,RIJUE      | VORBACH,<br>MARTIN |
| <a href="#">08947254</a> | <a href="#">6119181</a> |  | 150 | 10/08/1997 | I/O AND MEMORY<br>BUS SYSTEM FOR<br>DFPS AND UNITS<br>WITH TWO- OR<br>MULTI-<br>DIMENSIONAL<br>PROGRAMMABLE<br>CELL<br>ARCHITECTURES                                                                                 | RAY,GOPAL      | VORBACH,<br>MARTIN |
| <a href="#">09000724</a> | Not<br>Issued           |  | 168 | 12/30/1997 | PROCESS FOR<br>AUTOMATIC<br>DYNAMIC<br>RELOADING OF<br>DATA FLOW<br>PROCESSORS (DFPS)<br>AND UNITS WITH<br>TWO- OR THREE-<br>DIMENSIONAL<br>PROGRAMMABLE<br>CELL<br>ARCHITECTURES<br>(FPGAS, DPGAS, AND<br>THE LIKE) | MAI,RIJUE      | VORBACH,<br>MARTIN |
| <a href="#">09145139</a> | <a href="#">6405292</a> |  | 150 | 08/28/1998 | INTERNAL BUS<br>SYSTEM FOR DFPS<br>AND UNITS WITH<br>TWO-OR MULTI-<br>DIMENSIONAL<br>PROGRAMMABLE<br>CELL<br>ARCHITECTURES,<br>FOR MANAGING<br>LARGE VOLUMES OF<br>DATA WITH A HIGH<br>INTERCONNECTION<br>COMPLEXITY | VO,TIM         | VORBACH,<br>MARTIN |
| <a href="#">09290342</a> | <a href="#">6859862</a> |  | 150 | 04/12/1999 | DATA PROCESSING<br>SYSTEM                                                                                                                                                                                            | WHITMORE,STACY | VORBACH,<br>MARTIN |
| <a href="#">09329132</a> | <a href="#">6728871</a> |  | 150 | 06/09/1999 | RUNTIME<br>CONFIGURABLE<br>ARITHMETIC AND<br>LOGIC CELL                                                                                                                                                              | ELLIS,RICHARD  | VORBACH,<br>MARTIN |

|                          |                         |  |     |            |                                                                                                                                                                               |                 |                 |
|--------------------------|-------------------------|--|-----|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----------------|
| <a href="#">09335974</a> | <a href="#">6338106</a> |  | 150 | 06/18/1999 | I/O AND MEMORY BUS SYSTEM FOR DFPS AND UNITS WITH TWO OR MULTI-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES                                                                    | RAY,GOPAL       | VORBACH, MARTIN |
| <a href="#">09369653</a> | <a href="#">6542998</a> |  | 150 | 08/06/1999 | METHOD OF SELF-SYNCHRONIZATION OF CONFIGURABLE ELEMENTS OF A PROGRAMMABLE MODULE                                                                                              | HECKLER,THOMAS  | VORBACH, MARTIN |
| <a href="#">09494567</a> | <a href="#">7174443</a> |  | 150 | 01/31/2000 | RUN-TIME RECONFIGURATION METHOD FOR PROGRAMMABLE UNITS                                                                                                                        | DOLLINGER,TONIA | VORBACH, MARTIN |
| <a href="#">09537932</a> | <a href="#">6526520</a> |  | 150 | 03/29/2000 | METHOD OF SELF-SYNCHRONIZATION OF CONFIGURABLE ELEMENTS OF A PROGRAMMABLE UNIT                                                                                                | BUTLER,DENNIS   | VORBACH, MARTIN |
| <a href="#">09598926</a> | <a href="#">6697972</a> |  | 150 | 06/21/2000 | METHOD OF REPAIRING INTEGRATED CIRCUITS                                                                                                                                       | LAMARRE,GUY     | VORBACH, MARTIN |
| <a href="#">09613217</a> | <a href="#">6477643</a> |  | 150 | 07/10/2000 | PROCESS FOR AUTOMATIC DYNAMIC RELOADING OF DATA FLOW PROCESSORS (DFPS) AND UNITS WITH TWO-OR THREE-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES (FPGAS,DPGAS, AND THE LIKE)    | MAI,RIJUE       | VORBACH, MARTIN |
| <a href="#">09623052</a> | <a href="#">6480937</a> |  | 150 | 01/09/2001 | METHOD FOR HIERARCHICAL CACHING OF CONFIGURATION DATA HAVING DATAFLOW PROCESSORS AND MODULES HAVING TWO-OR MULTIDIMENSIONAL PROGRAMMABLE CELL STRUCTURE (FPGAS, DPGS, ETC.)-- | ELMORE,STEPHEN  | VORBACH, MARTIN |
| <a href="#">09623113</a> | <a href="#">6571381</a> |  | 150 | 01/09/2001 | METHOD FOR DEADLOCK-FREE                                                                                                                                                      | KIK,PHALLAKA    | VORBACH, MARTIN |

|                          |                         |             |     |            |                                                                                                                                                                                  |                 |                 |
|--------------------------|-------------------------|-------------|-----|------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------|-----------------|
|                          |                         |             |     |            | CONFIGURATION OF DATAFLOW PROCESSORS AND MODULES WITH A TWO-OR MULTIDIMENSIONAL PROGRAMMABLE CELL STRUCTURE (FPGAS, DPGAS, ETC.)                                                 |                 |                 |
| <a href="#">09915213</a> | <a href="#">6513077</a> | 20020099888 | 150 | 07/25/2001 | I/O AND MEMORY BUS SYSTEM FOR DFPS AND UNITS WITH TWO- OR MULTI-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES                                                                      | RAY,GOPAL       | VORBACH, MARTIN |
| <a href="#">09967497</a> | <a href="#">7266725</a> | 20030046607 | 150 | 09/28/2001 | METHOD FOR DEBUGGING RECONFIGURABLE ARCHITECTURES                                                                                                                                | LE,DIEU MINH    | VORBACH, MARTIN |
| <a href="#">09967498</a> | Not Issued              | 20040015899 | 161 | 09/28/2001 | Method for processing data                                                                                                                                                       | RAMPURIA,SATISH | VORBACH, MARTIN |
| <a href="#">09967847</a> | <a href="#">7210129</a> | 20030056202 | 150 | 09/28/2001 | METHOD FOR TRANSLATING PROGRAMS FOR RECONFIGURABLE ARCHITECTURES                                                                                                                 | INGBERG,TODD    | VORBACH, MARTIN |
| <a href="#">10009649</a> | <a href="#">8230411</a> |             | 150 | 05/29/2002 | METHOD FOR INTERLEAVING A PROGRAM OVER A PLURALITY OF CELLS                                                                                                                      | DAO,THUY        | VORBACH, MARTIN |
| <a href="#">10116986</a> | <a href="#">7010667</a> | 20030135686 | 150 | 04/05/2002 | INTERNAL BUS SYSTEM FOR DFPS AND UNITS WITH TWO- OR MULTI-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES, FOR MANAGING LARGE VOLUMES OF DATA WITH A HIGH INTERCONNECTION COMPLEXITY | VO,TIM          | VORBACH, MARTIN |
| <a href="#">10156397</a> | <a href="#">7237087</a> | 20030056085 | 150 | 05/28/2002 | RECONFIGURABLE MULTIDIMENSIONAL ARRAY PROCESSOR ALLOWING RUNTIME RECONFIGURATION OF SELECTED INDIVIDUAL ARRAY CELLS                                                              | ELLIS,RICHARD   | VORBACH, MARTIN |
| <a href="#">10191926</a> | <a href="#">6687738</a> | 20030074518 | 150 | 07/09/2002 | METHOD OF HIERARCHICAL CACHING OF                                                                                                                                                | ELMORE,STEPHEN  | VORBACH, MARTIN |

|                                 |                                |             |     |            |                                                                                                                                                                              |                    |                 |
|---------------------------------|--------------------------------|-------------|-----|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|-----------------|
|                                 |                                |             |     |            | CONFIGURATION DATA HAVING DATAFLOW PROCESSORS AND MODULES HAVING TWO-OR MULTIDIMENSIONAL PROGRAMMABLE CELL STRUCTURE (FPGAS, DPGAS, ETC.)                                    |                    |                 |
| <a href="#"><u>10265846</u></a> | <a href="#"><u>7028107</u></a> | 20030093662 | 150 | 10/07/2002 | PROCESS FOR AUTOMATIC DYNAMIC RELOADING OF DATA FLOW PROCESSORS (DFPS) AND UNITS WITH TWO- OR THREE-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES (FPGAS, DPGAS, AND THE LIKE) | KNAPP,JUSTIN       | VORBACH, MARTIN |
| <a href="#"><u>10297959</u></a> | <a href="#"><u>7003660</u></a> | 20040025005 | 150 | 06/19/2003 | PIPELINE CONFIGURATION UNIT PROTOCOLS AND COMMUNICATION                                                                                                                      | ELAMIN,ABDELMONIEM | VORBACH, MARTIN |
| <a href="#"><u>10304252</u></a> | <a href="#"><u>6721830</u></a> | 20030097513 | 150 | 11/26/2002 | L/O AND MEMORY BUS SYSTEM FOR DFPS AND UNITS WITH TWO- OR MULTI-DIMENSIONAL PROGRAMMABLE CELL ARCHITECTURES                                                                  | RAY,GOPAL          | VORBACH, MARTIN |
| <a href="#"><u>10373595</u></a> | <a href="#"><u>6968452</u></a> | 20040052130 | 150 | 02/24/2003 | METHOD OF SELF-SYNCHRONIZATION OF CONFIGURABLE ELEMENTS OF A PROGRAMMABLE UNIT                                                                                               | BUTLER,DENNIS      | VORBACH, MARTIN |
| <a href="#"><u>10379403</u></a> | <a href="#"><u>7036036</u></a> | 20040083399 | 150 | 03/04/2003 | METHOD OF SELF-SYNCHRONIZATION OF CONFIGURABLE ELEMENTS OF A PROGRAMMABLE MODULE                                                                                             | YANCHUS III,PAUL   | VORBACH, MARTIN |
| <a href="#"><u>10398546</u></a> | <a href="#"><u>7595659</u></a> | 20040128474 | 150 | 01/20/2004 | LOGIC CELL ARRAY AND BUS SYSTEM                                                                                                                                              | TAN,VIBOL          | VORBACH, MARTIN |
| <a href="#"><u>10469909</u></a> | <a href="#"><u>7444531</u></a> | 20050066213 | 150 | 09/21/2004 | METHODS AND DEVICES FOR TREATING AND PROCESSING DATA                                                                                                                         | ELAMIN,ABDELMONIEM | VORBACH, MARTIN |
| <a href="#"><u>10469910</u></a> | Not Issued                     | 20070299993 | 161 | 02/17/2005 | Method and Device for Treating and Processing Data                                                                                                                           | MAMO,ELIAS         | VORBACH, MARTIN |

|                                 |                                |             |     |            |                                                                                                                                                                        |                |                 |
|---------------------------------|--------------------------------|-------------|-----|------------|------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------------|-----------------|
| <a href="#"><u>10471061</u></a> | <a href="#"><u>7581076</u></a> | 20050086462 | 150 | 10/29/2004 | METHODS AND DEVICES FOR TREATING AND/OR PROCESSING DATA                                                                                                                | NGUYEN,THAN    | VORBACH, MARTIN |
| <a href="#"><u>10480903</u></a> | <a href="#"><u>7657872</u></a> | 20040243984 | 150 | 06/18/2004 | METHOD FOR PROCESSING DATA                                                                                                                                             | BROPHY,MATTHEW | VORBACH, MARTIN |
| <a href="#"><u>10486771</u></a> | <a href="#"><u>7996822</u></a> | 20050086649 | 150 | 09/20/2004 | METHOD FOR THE TRANSLATION OF PROGRAMS FOR RECONFIGURABLE ARCHITECTURES                                                                                                | DAO,THUY       | VORBACH, MARTIN |
| <a href="#"><u>10487681</u></a> | <a href="#"><u>7577822</u></a> | 20040249880 | 150 | 08/05/2004 | PARALLEL TASK OPERATION IN PROCESSOR AND RECONFIGURABLE COPROCESSOR CONFIGURED BASED ON INFORMATION IN LINK LIST INCLUDING TERMINATION INFORMATION FOR SYNCHRONIZATION | KIM,KENNETH    | VORBACH, MARTIN |
| <a href="#"><u>10487687</u></a> | <a href="#"><u>7480825</u></a> | 20050022062 | 150 | 08/25/2004 | METHOD FOR DEBUGGING RECONFIGURABLE ARCHITECTURES                                                                                                                      | CONTINO,PAUL   | VORBACH, MARTIN |
| <a href="#"><u>10490079</u></a> | <a href="#"><u>7434191</u></a> | 20050053056 | 150 | 11/02/2004 | ROUTER                                                                                                                                                                 | LIN,SUN        | VORBACH, MARTIN |
| <a href="#"><u>10490081</u></a> | <a href="#"><u>8429385</u></a> | 20060245225 | 150 | 11/29/2004 | DEVICE INCLUDING A FIELD HAVING FUNCTION CELLS AND INFORMATION PROVIDING CELLS CONTROLLED BY THE FUNCTION CELLS                                                        | FENNEMA,ROBERT | VORBACH, MARTIN |
| <a href="#"><u>10501845</u></a> | <a href="#"><u>8281108</u></a> | 20060090062 | 150 | 08/26/2005 | RECONFIGURABLE GENERAL PURPOSE PROCESSOR HAVING TIME RESTRICTED CONFIGURATIONS                                                                                         | VICARY,KEITH   | VORBACH, MARTIN |
| <a href="#"><u>10501903</u></a> | Not Issued                     | 20050132344 | 161 | 03/01/2005 | Method of compilation                                                                                                                                                  | LOUIE,JUE      | VORBACH, MARTIN |
| <a href="#"><u>10504684</u></a> | <a href="#"><u>8127061</u></a> | 20070150637 | 150 | 07/14/2006 | BUS SYSTEMS AND RECONFIGURATION METHODS                                                                                                                                | CLEARY,THOMAS  | VORBACH, MARTIN |
| <a href="#"><u>10508559</u></a> | Not Issued                     | 20060075211 | 161 | 06/20/2005 | Method and device for data processing                                                                                                                                  | GIROUX,GEORGE  | VORBACH, MARTIN |
| <a href="#"><u>10523763</u></a> | <a href="#"><u>7657861</u></a> | 20060248317 | 150 | 11/22/2005 | METHOD AND DEVICE FOR PROCESSING DATA                                                                                                                                  | DINH,PAUL      | VORBACH, MARTIN |
| <a href="#"><u>10523764</u></a> | <a href="#"><u>8156284</u></a> | 20070050603 | 150 | 08/02/2005 | DATA PROCESSING METHOD AND DEVICE                                                                                                                                      | THAI,TUAN      | VORBACH, MARTIN |
| <a href="#"><u>10526595</u></a> | <a href="#"><u>7394284</u></a> | 20060192586 | 150 | 01/09/2006 | RECONFIGURABLE SEQUENCER STRUCTURE                                                                                                                                     | LE,DON         | VORBACH, MARTIN |

|                          |               |                             |     |                            |                                          |              |                    |
|--------------------------|---------------|-----------------------------|-----|----------------------------|------------------------------------------|--------------|--------------------|
| <a href="#">10551891</a> | Not<br>Issued | <a href="#">20070011433</a> | 161 | <a href="#">08/28/2006</a> | Method and device for<br>data processing | VICARY,KEITH | VORBACH,<br>MARTIN |
|--------------------------|---------------|-----------------------------|-----|----------------------------|------------------------------------------|--------------|--------------------|

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**Search Another: Inventor**

| Last Name                            | First Name                          |                                       |
|--------------------------------------|-------------------------------------|---------------------------------------|
| <input type="text" value="VORBACH"/> | <input type="text" value="MARTIN"/> | <input type="button" value="Search"/> |

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## WEST Search History

DATE: Tuesday, November 22, 2016

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|--------------------------|---------------------------------------|--------------------------------------------------------------------------------------------------------|----------------------------|
|                          | <i>DB=PGPB,USPT; PLUR=YES; OP=ADJ</i> |                                                                                                        |                            |
| <input type="checkbox"/> | L70                                   | L66 and l8                                                                                             | 11                         |
| <input type="checkbox"/> | L69                                   | L66 and l21                                                                                            | 45                         |
| <input type="checkbox"/> | L68                                   | L66 and l57                                                                                            | 2                          |
| <input type="checkbox"/> | L67                                   | L66 and l59                                                                                            | 65                         |
| <input type="checkbox"/> | L66                                   | L65 or l54 or l63                                                                                      | 19357                      |
| <input type="checkbox"/> | L65                                   | (( G06F1/32 ).IPCR.)                                                                                   | 13643                      |
| <input type="checkbox"/> | L64                                   | (( 713/3\$2 ).CCLS.)                                                                                   | 22345                      |
| <input type="checkbox"/> | L63                                   | (( G06F1/206   G06F1/324   G06F1/3296   Y02B60/1217   Y02B60/1285 ).CPC.)                              | 8837                       |
| <input type="checkbox"/> | L62                                   | 20140208143                                                                                            | 1                          |
| <input type="checkbox"/> | L61                                   | L59.ti,ab,clm.                                                                                         | 57                         |
| <input type="checkbox"/> | L60                                   | L59 with temperature                                                                                   | 4                          |
| <input type="checkbox"/> | L59                                   | multi\$1process\$4 with ((clock or frequency) near5 (adjust\$4 or modif\$7 or chang\$4 or dynamic\$5)) | 152                        |
| <input type="checkbox"/> | L57                                   | L50 same (clock or frequency)                                                                          | 69                         |
| <input type="checkbox"/> | L55                                   | L50 with (clock or frequency)                                                                          | 27                         |
| <input type="checkbox"/> | L50                                   | multi\$1process\$4 with pip\$                                                                          | 2243                       |
| <input type="checkbox"/> | L49                                   | l1 and function\$5                                                                                     | 1                          |
| <input type="checkbox"/> | L48                                   | l1 and core                                                                                            | 0                          |
| <input type="checkbox"/> | L47                                   | l1 and parallel                                                                                        | 1                          |
| <input type="checkbox"/> | L46                                   | 6895520.pn. and (task)                                                                                 | 1                          |
| <input type="checkbox"/> | L45                                   | 6895520.pn. and (priority or import\$7 or critical)                                                    | 1                          |
| <input type="checkbox"/> | L44                                   | 6895520.pn. and (alu)                                                                                  | 1                          |
| <input type="checkbox"/> | L43                                   | 6895520.pn. and (pipe\$7 or sequen\$7)                                                                 | 1                          |
| <input type="checkbox"/> | L42                                   | 6895520.pn. and ((clock or frequency) with voltage)                                                    | 1                          |
| <input type="checkbox"/> | L39                                   | 6609209.pn. and (voltage)                                                                              | 1                          |
| <input type="checkbox"/> | L37                                   | 6609209.pn. and process\$4                                                                             | 1                          |
| <input type="checkbox"/> | L35                                   | 20140208143 and run\$2time                                                                             | 1                          |
| <input type="checkbox"/> | L31                                   | 6609209.pn. and (clock or frequency)                                                                   | 1                          |
| <input type="checkbox"/> | L30                                   | 6611920.pn. and (clock or frequency)                                                                   | 1                          |
| <input type="checkbox"/> | L29                                   | L28 and (clock or frequency)                                                                           | 1                          |

|                          |     |                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                |      |
|--------------------------|-----|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------|
| <input type="checkbox"/> | L28 | 6651176.pn.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 1    |
| <input type="checkbox"/> | L27 | l25 and (sensor)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 1    |
| <input type="checkbox"/> | L26 | l25 and (temp\$7 or heat\$4 or overheat\$5 or hot)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 6    |
| <input type="checkbox"/> | L25 | (6611920   20020069348   6651176   6317839   6851068   6247134   5452434   6609209   5799199   6233690   20020188828   5987620   20020104032)! [PN]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                            | 13   |
| <input type="checkbox"/> | L24 | ("7076681") [PN]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 1    |
| <input type="checkbox"/> | L23 | 7,076,681.pn.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 1    |
| <input type="checkbox"/> | L22 | ((adjust\$4 or modif\$7 or chang\$4) near3 (independent\$4 or selectiv\$5)) with (process\$4 near3 (sequen\$7 or pipe\$1line))                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                 | 21   |
| <input type="checkbox"/> | L21 | L10 and (process\$4 near3 (sequen\$7 or pipe\$1line))                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                          | 130  |
| <input type="checkbox"/> | L20 | L10 same (process\$4 near3 (sequen\$7 or pipe\$1line))                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 4    |
| <input type="checkbox"/> | L19 | L17 and sequen\$7                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                              | 1    |
| <input type="checkbox"/> | L17 | 7444531.pn.                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    | 1    |
| <input type="checkbox"/> | L15 | 6895520.pn. and (pipe\$7 or sequen\$7)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 1    |
| <input type="checkbox"/> | L14 | l13 and l10<br>(7482792   6867502   5734808   20020083354   6141762   6342795   20070033425   6647502   20080229128   20020184547   6079017   7337334   5502838   6611920   7598630   8037445   RE36839   7523336   7181631   8044697   7284137   20100011233   20080082839   6693412   7062933   4893227   6864600   6820209   20050223251   7206954   20070023878   7698576   20050162188   4588903   20060288246   20020109413   20080028244   20030210247   20070043964   6940163   7076681   7681054   20060174149   20040123170   5781783   6802014   7034344   20060053326   7685445   7032117   20060282692   7194643   7406588   7647452   20040088519   20060117192   6150724   6938176   7664971   6021506   7366926   20020152407   6434704   20090099705   20060218424   20050040810   6788035   20050046400   7555664   5768213   20050210905   7026797   6577535   5677849   6600296   20030122429   20030131268   20040117678   20030210274   7383449   7913064   7395440   20030126477   7051306   5951689   7313706   20050289367   5913068   20110296208   7178044   20070192638   6895520   7110266   7263457   6452247   5392437   20030135768   7218085   6247134   6983389   7363522   6804632   6954210   7536597   20080028236   20090313489   5585745   6625740   6393579   7126798   20070198863   20060149974   6812565   20050154931   6727118   20060020838   7275168   7275164   6822481   6754086   20070271473   6803805   6915438   20040158750   7202648   6873136   7568115   20080136397   20060085660   6424128   20060006432   20050289365   20040019814   7600145   20060288241)! [PN] | 8    |
| <input type="checkbox"/> | L13 | 20060218424   20050040810   6788035   20050046400   7555664   5768213   20050210905   7026797   6577535   5677849   6600296   20030122429   20030131268   20040117678   20030210274   7383449   7913064   7395440   20030126477   7051306   5951689   7313706   20050289367   5913068   20110296208   7178044   20070192638   6895520   7110266   7263457   6452247   5392437   20030135768   7218085   6247134   6983389   7363522   6804632   6954210   7536597   20080028236   20090313489   5585745   6625740   6393579   7126798   20070198863   20060149974   6812565   20050154931   6727118   20060020838   7275168   7275164   6822481   6754086   20070271473   6803805   6915438   20040158750   7202648   6873136   7568115   20080136397   20060085660   6424128   20060006432   20050289365   20040019814   7600145   20060288241)! [PN]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 135  |
| <input type="checkbox"/> | L12 | ("9021279"   "9021279"   "7797561"   "9021279"   "7797561") [PN]                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                               | 2    |
| <input type="checkbox"/> | L11 | L10 with (process\$4 near3 (sequen\$7 or pipe\$1line))                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 4    |
| <input type="checkbox"/> | L10 | ((clock or frequency) near5 (adjust\$4 or modif\$7 or chang\$4)) near3 (independent\$4 or selectiv\$5)                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                         | 9000 |
| <input type="checkbox"/> | L9  | L8 and temperature                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                             | 29   |
| <input type="checkbox"/> | L8  | L6 with ((clock or frequency) near5 (adjust\$4 or modif\$7 or chang\$4))                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       | 114  |
| <input type="checkbox"/> | L7  | L6 with (clock or frequency) with temperature                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                  | 1    |

|                          |    |                                |       |
|--------------------------|----|--------------------------------|-------|
| <input type="checkbox"/> | L6 | pipe\$1lin\$4 near3 process\$4 | 56131 |
| <input type="checkbox"/> | L5 | 20140208143 and sequen\$7      | 1     |
| <input type="checkbox"/> | L4 | 5502838.pn. and ser\$7         | 1     |
| <input type="checkbox"/> | L1 | 5502838.pn.                    | 1     |

END OF SEARCH HISTORY

# PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail Stop ISSUE FEE**  
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73481 7590 12/02/2016  
**Alliacense Limited LLC**  
**2310 Homestead Rd**  
**# C1-505**  
**Los Altos, CA 94024-7339**

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|                    |
|--------------------|
| (Depositor's name) |
| (Signature)        |
| (Date)             |

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.       | CONFIRMATION NO. |
|-----------------|-------------|----------------------|---------------------------|------------------|
| 14/219,945      | 03/19/2014  | Martin VORBACH       | PACT-025-PCT-US-D1-2C1-D1 | 7671             |

TITLE OF INVENTION: Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply

| APPLN. TYPE    | ENTITY STATUS | ISSUE FEE DUE | PUBLICATION FEE DUE | PREV. PAID ISSUE FEE | TOTAL FEE(S) DUE | DATE DUE   |
|----------------|---------------|---------------|---------------------|----------------------|------------------|------------|
| nonprovisional | UNDISCOUNTED  | \$960         | \$0                 | \$0                  | \$960            | 03/02/2017 |

| EXAMINER              | ART UNIT | CLASS-SUBCLASS |
|-----------------------|----------|----------------|
| ELAMIN, ABDELMONIEM I | 2116     | 713-322000     |

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
- ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list

- (1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
- (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 Edward P Heller III  
2 \_\_\_\_\_  
3 \_\_\_\_\_

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

PACT XPP TECHNOLOGIES AG

MUNICH (DE)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

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- ☒ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies \_\_\_\_\_

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number \_\_\_\_\_ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

**NOTE:** Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

**NOTE:** If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

**NOTE:** Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Edward P Heller III/  
Typed or printed name Edward P Heller III

Date 12/06/2016  
Registration No. 29,075

| Electronic Patent Application Fee Transmittal      |                 |                                                                                 |               |                             |
|----------------------------------------------------|-----------------|---------------------------------------------------------------------------------|---------------|-----------------------------|
| <b>Application Number:</b>                         |                 | 14219945                                                                        |               |                             |
| <b>Filing Date:</b>                                |                 | 19-Mar-2014                                                                     |               |                             |
| <b>Title of Invention:</b>                         |                 | Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply |               |                             |
| <b>First Named Inventor/Applicant Name:</b>        |                 | Martin VORBACH                                                                  |               |                             |
| <b>Filer:</b>                                      |                 | Edward Peter Heller                                                             |               |                             |
| <b>Attorney Docket Number:</b>                     |                 | PACT-025-PCT-US-D1-2C1-D1                                                       |               |                             |
| Filed as Large Entity                              |                 |                                                                                 |               |                             |
| <b>Filing Fees for Utility under 35 USC 111(a)</b> |                 |                                                                                 |               |                             |
| <b>Description</b>                                 | <b>Fee Code</b> | <b>Quantity</b>                                                                 | <b>Amount</b> | <b>Sub-Total in USD(\$)</b> |
| <b>Basic Filing:</b>                               |                 |                                                                                 |               |                             |
| <b>Pages:</b>                                      |                 |                                                                                 |               |                             |
| <b>Claims:</b>                                     |                 |                                                                                 |               |                             |
| <b>Miscellaneous-Filing:</b>                       |                 |                                                                                 |               |                             |
| <b>Petition:</b>                                   |                 |                                                                                 |               |                             |
| <b>Patent-Appeals-and-Interference:</b>            |                 |                                                                                 |               |                             |
| <b>Post-Allowance-and-Post-Issuance:</b>           |                 |                                                                                 |               |                             |
| UTILITY APPL ISSUE FEE                             | 1501            | 1                                                                               | 960           | 960                         |

| Description        | Fee Code | Quantity | Amount | Sub-Total in USD(\$) |
|--------------------|----------|----------|--------|----------------------|
| Extension-of-Time: |          |          |        |                      |
| Miscellaneous:     |          |          |        |                      |
| Total in USD (\$)  |          |          |        | 960                  |

| Electronic Acknowledgement Receipt          |                                                                                 |
|---------------------------------------------|---------------------------------------------------------------------------------|
| <b>EFS ID:</b>                              | 27712603                                                                        |
| <b>Application Number:</b>                  | 14219945                                                                        |
| <b>International Application Number:</b>    |                                                                                 |
| <b>Confirmation Number:</b>                 | 7671                                                                            |
| <b>Title of Invention:</b>                  | Multiprocessor Having Runtime Adjustable Clock and Clock Dependent Power Supply |
| <b>First Named Inventor/Applicant Name:</b> | Martin VORBACH                                                                  |
| <b>Customer Number:</b>                     | 73481                                                                           |
| <b>Filer:</b>                               | Edward Peter Heller                                                             |
| <b>Filer Authorized By:</b>                 |                                                                                 |
| <b>Attorney Docket Number:</b>              | PACT-025-PCT-US-D1-2C1-D1                                                       |
| <b>Receipt Date:</b>                        | 06-DEC-2016                                                                     |
| <b>Filing Date:</b>                         | 19-MAR-2014                                                                     |
| <b>Time Stamp:</b>                          | 17:13:03                                                                        |
| <b>Application Type:</b>                    | Utility under 35 USC 111(a)                                                     |

### Payment information:

|                                                                                                                |                       |
|----------------------------------------------------------------------------------------------------------------|-----------------------|
| Submitted with Payment                                                                                         | yes                   |
| Payment Type                                                                                                   | CARD                  |
| Payment was successfully received in RAM                                                                       | \$960                 |
| RAM confirmation Number                                                                                        | 120716INTEFSW17152900 |
| Deposit Account                                                                                                |                       |
| Authorized User                                                                                                |                       |
| The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: |                       |

| <b>File Listing:</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                   |                             |                                        |                                          |                  |                  |
|--------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-----------------------------|----------------------------------------|------------------------------------------|------------------|------------------|
| Document Number                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        | Document Description        | File Name                              | File Size(Bytes)/<br>Message Digest      | Multi Part /.zip | Pages (if appl.) |
| 1                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Issue Fee Payment (PTO-85B) | PACT-025-PCT-US-D1-2C1-D1_IssueFee.pdf | 85233                                    | no               | 1                |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                             |                                        | bdb11b0e5da29be05aea3656af2bd3dea99649b8 |                  |                  |
| <b>Warnings:</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                             |                                        |                                          |                  |                  |
| <b>Information:</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                             |                                        |                                          |                  |                  |
| 2                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                      | Fee Worksheet (SB06)        | fee-info.pdf                           | 30641                                    | no               | 2                |
|                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                        |                             |                                        | 46f2628fe6b3bab1c971c62eb026112987c322da |                  |                  |
| <b>Warnings:</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                       |                             |                                        |                                          |                  |                  |
| <b>Information:</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                             |                                        |                                          |                  |                  |
| <b>Total Files Size (in bytes):</b>                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                                    |                             |                                        | 115874                                   |                  |                  |
| <p><b>This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.</b></p> <p><b><u>New Applications Under 35 U.S.C. 111</u></b><br/> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.</p> <p><b><u>National Stage of an International Application under 35 U.S.C. 371</u></b><br/> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.</p> <p><b><u>New International Application Filed with the USPTO as a Receiving Office</u></b><br/> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.</p> |                             |                                        |                                          |                  |                  |



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|                                                                                             |             |                      |                                   |                             |
|---------------------------------------------------------------------------------------------|-------------|----------------------|-----------------------------------|-----------------------------|
| APPLICATION NO.                                                                             | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.               | CONFIRMATION NO.            |
| 14/219,945                                                                                  | 03/19/2014  | Martin VORBACH       | PACT-025-PCT-US-D1-2C1-D1         | 7671                        |
| 7590<br>Alliacense Limited LLC<br>2310 Homestead Rd<br># C1-505<br>Los Altos, CA 94024-7339 |             |                      | EXAMINER<br>ELAMIN, ABDELMONIEM I |                             |
|                                                                                             |             |                      | ART UNIT<br>2116                  | PAPER NUMBER                |
|                                                                                             |             |                      | NOTIFICATION DATE<br>12/16/2016   | DELIVERY MODE<br>ELECTRONIC |

## NOTICE REQUIRING INVENTOR'S OATH OR DECLARATION

☐ An inventor's oath or declaration in compliance with 37 CFR 1.63 or substitute statement in compliance with 37 CFR 1.64 executed by or with respect to each inventor has not yet been submitted.

The inventor's oath or declaration or substitute statement dated \_\_\_\_\_ is defective. The inventor's oath or declaration does not comply with 37 CFR 1.63 or the substitute statement does not comply with 37 CFR 1.64 because it:

☐ does not include a statement that the person executing the oath or declaration or substitute statement believes the named inventor or joint inventor to be the original inventor or an original joint inventor of a claimed invention in the application for which the oath or declaration is being submitted.

☐ does not state that the application was made or was authorized to be made by the person executing the oath or declaration or substitute statement.

☐ does not acknowledge that any willful false statement made in such oath or declaration or substitute statement is punishable under section 1001 of title 18 by fine or imprisonment of not more than 5 years, or both.

☐ does not identify the person executing the oath or declaration or substitute statement by his or her legal name.

☐ does not identify the application to which the oath or declaration or substitute statement is directed.

☐ Other: \_\_\_\_\_

The substitute statement dated 3/25/2014 does not comply with 37 CFR 1.64 because it:

☐ does not identify the inventor with respect to whom the statement applies.

☐ does not identify the relationship to the non-signing inventor.

☐ does not identify the circumstances permitting execution of the statement.

☒ was signed by someone other than the applicant.

☐ Other: \_\_\_\_\_

An oath or declaration in compliance with 37 CFR 1.63, or a substitute statement in compliance with 37 CFR 1.64, executed by or with respect to each inventor **MUST** be filed **no later than the date on which the issue fee is paid**. See 35 U.S.C. 115(f). Failure to timely comply will result in ABANDONMENT of this application. This period for reply is not extendable under 37 CFR 1.136(a).

Questions relating to this Notice should be directed to the Application Assistance Unit at 571-272-4200.

(571)-272-4200 or 1(888)-786-0101

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|---------------------------------------------------------------------------------------------|-------------|----------------------|-----------------------------------|-----------------------------|
| APPLICATION NO.                                                                             | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO.               | CONFIRMATION NO.            |
| 14/219,945                                                                                  | 03/19/2014  | Martin VORBACH       | PACT-025-PCT-US-D1-2C1-D1         | 7671                        |
| 7590<br>Alliacense Limited LLC<br>2310 Homestead Rd<br># C1-505<br>Los Altos, CA 94024-7339 |             |                      | EXAMINER<br>ELAMIN, ABDELMONIEM I |                             |
|                                                                                             |             |                      | ART UNIT<br>2116                  | PAPER NUMBER                |
|                                                                                             |             |                      | NOTIFICATION DATE<br>12/27/2016   | DELIVERY MODE<br>ELECTRONIC |

## Letter Withdrawing a Notice Requiring Inventor's Oath or Declaration

The Notice Requiring Inventor's Oath or Declaration mailed on 12-16-16 was sent in error, and is hereby withdrawn. The time period set forth in the Notice of Allowance and Fee(s) Due to file a reply and pay the required fees continues to run from the mailing date of the Notice of Allowance and Fee(s) Due. Any time period set forth in the Notice of Allowability continues to run from the mailing date of the Notice of Allowability.

Questions relating to this Notice should be directed to the Application Assistance Unit at 571-272-4200.

(571)-272-4200 or 1(888)-786-0101

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|                                                                                                     |                        |                           |            |
|-----------------------------------------------------------------------------------------------------|------------------------|---------------------------|------------|
| <b>INFORMATION DISCLOSURE<br/>STATEMENT BY APPLICANT</b><br>( Not for submission under 37 CFR 1.99) | Application Number     |                           | 14219945   |
|                                                                                                     | Filing Date            |                           | 2014-03-19 |
|                                                                                                     | First Named Inventor   | Martin Vorbach            |            |
|                                                                                                     | Art Unit               | 2116                      |            |
|                                                                                                     | Examiner Name          | ELAMIN, ABDELMONIEM I     |            |
|                                                                                                     | Attorney Docket Number | PACT-025-PCT-US-D1-2C1-D1 |            |

ALL REFERENCES CONSIDERED EXCEPT WHERE LINED THROUGH. /A.E./

| U.S. PATENTS                                       |         |                                      |                        |            |                                                 | Remove                                                                   |
|----------------------------------------------------|---------|--------------------------------------|------------------------|------------|-------------------------------------------------|--------------------------------------------------------------------------|
| Examiner Initial*                                  | Cite No | Patent Number                        | Kind Code <sup>1</sup> | Issue Date | Name of Patentee or Applicant of cited Document | Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear |
| Change(s) applied to document, /C.C.B./ 12/16/2016 | 1       | <del>US 3,473,160</del><br>3,473,160 | A                      | 1969-10-14 | Wahlstrom et al.                                |                                                                          |
|                                                    | 2       | <del>US 3,531,662</del><br>3,531,662 | A                      | 1970-09-29 | Spandorfer et al.                               |                                                                          |
|                                                    | 3       | 4020469                              |                        | 1977-04-26 | Manning                                         |                                                                          |
|                                                    | 4       | 4642487                              |                        | 1987-02-10 | Carter                                          |                                                                          |
|                                                    | 5       | 4700187                              |                        | 1987-10-13 | Furtek                                          |                                                                          |
|                                                    | 6       | 4706216                              |                        | 1987-11-10 | Carter                                          |                                                                          |
|                                                    | 7       | 4722084                              |                        | 1988-01-26 | Morton                                          |                                                                          |
|                                                    | 8       | 4724307                              |                        | 1988-02-09 | Dutton et al.                                   |                                                                          |

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| APPLICATION NO. | ISSUE DATE | PATENT NO. | ATTORNEY DOCKET NO.       | CONFIRMATION NO. |
|-----------------|------------|------------|---------------------------|------------------|
| 14/219,945      | 01/24/2017 | 9552047    | PACT-025-PCT-US-D1-2C1-D1 | 7671             |

73481 7590 01/04/2017  
Alliacense Limited LLC  
2310 Homestead Rd  
# C1-505  
Los Altos, CA 94024-7339

### ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

#### **Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)** (application filed on or after May 29, 2000)

The Patent Term Adjustment is 52 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

PACT XPP TECHNOLOGIES AG, Munich, GERMANY;  
Martin VORBACH, Munchen, GERMANY;  
Volker BAUMGARTE, Munchen, GERMANY;

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