IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE

PACT XPP SCHWEIZ AG	)	
	)	
Plaintiff,	)	C.A. No. 19-1006-JDW
	)	
v.	)	
	)	
INTEL CORPORATION,	)	
	)	
Defendant.	)	

JOINT CLAIM CONSTRUCTION CHART

Pursuant to Paragraph 9 of the Scheduling Order (D.I. No. 20), Plaintiff PACT XPP Schweiz AG ("PACT") and Intel Corporation ("Intel") hereby submit this Joint Claim Construction Chart, identifying for the Court the terms and phrases of the claims in issue, including each party's proposed construction of the disputed claim language with citations only to the intrinsic evidence in support of their respective proposed constructions.

TABLE OF EXHIBITS

Exhibit No.	Document
1	U.S. Patent No. 7,928,763
2	U.S. Patent No. 8,301,872
3	U.S. Patent No. 8,312,301
4	U.S. Patent No. 8,471,593
5	U.S. Patent No. 8,686,549
6	U.S. Patent No. 8,819,505
7	U.S. Patent No. 9,037,807
8	U.S. Patent No. 9,075,605
9	U.S. Patent No. 9,170,812
10	U.S. Patent No. 9,250,908
11	U.S. Patent No. 9,436,631
12	U.S. Patent No. 9,552,047
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19	Intentionally Left Blank
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21	Excerpts of File History of U.S. Patent No. 9,170,812 relied on by Plaintiff
22	Intentionally Left Blank
23	Intentionally Left Blank
24	Excerpts of File History of U.S. Patent No. 9,552,047 relied on by Plaintiff
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29	Intentionally Left Blank
30	Excerpts of File History of U.S. Patent No. 8,819,505 relied on by Defendant
31	Intentionally Left Blank
32	Excerpts of File History of U.S. Patent No. 9,075,605 relied on by Defendant
33	Excerpts of File History of U.S. Patent No. 9,170,812 relied on by Defendant
34	Intentionally Left Blank
35	Excerpts of File History of U.S. Patent No. 9,436,631 relied on by Defendant
36	Excerpts of File History of U.S. Patent No. 9,552,047 relied on by Defendant
37	DE 196 54 846 A1

STIPULATED CLAIM TERMS

Patent	Claim Terms and Phrases	Stipulated Claim Construction
’605	Preamble (claim 1)	Preamble is limiting.
’908	“train mission” (claim 4)	transmission
’631	“may executed” (claim 1)	may be executed
’872	Preambles (claims 2, 10, 14, 15)	Preambles are not limiting.
’807	Preambles (claims 1-6, 24, 26-27, 29, 32, 44, and 73-74)	Preambles are not limiting.

TERMS PROPOSED BY PLAINTIFF

Patent	Claim Terms and Phrases	Plaintiff’s Proposed Construction	Defendant’s Proposed Construction	Plaintiff’s Intrinsic Evidence	Defendant’s Intrinsic Evidence
’763	“interconnecting at runtime at least one of data processing cells and memory cells with at least one of memory cells and one or more of the at least one interface unit” (claims 1, 31)	connect at least one data processing cell, at least one memory cell, and at least one interface unit with each other at runtime.	*See* Intel’s construction for “programmably interconnecting at runtime” / “dynamically interconnecting at runtime”	Ex. 1, Figs. 1, 2(a)-2(c), 3, 4, 5 7:47-11:12; 11:21-45.	*See e.g.*, Ex. 1 (’763 patent) at 2:16-23; 12:5-17; 4:4-10; 12:38-83; 9:3-9:6; 6:56-7:6; 1:26-28; 8:45-55.

Patent	Claim Terms and Phrases	Plaintiff's Proposed Construction	Defendant's Proposed Construction	Plaintiff's Intrinsic Evidence	Defendant's Intrinsic Evidence
'763	"the data processing cells are adapted to connect simultaneously to a plurality of at least one of cells and units of at least one of the memory cells, the data processing cells, and the at least one interface units" (claim 10)	each of the data processing cells is adapted to simultaneously connect to a plurality of elements; each of the elements is either one of the memory cells, another one of the data processing cells, or the interface unit.	*See* Intel's construction for "programmably interconnecting at runtime" / "dynamically interconnecting at runtime"	Ex. 1, Figs. 1, 2(a)-2(c), 3, 4, 5 7:47-11:12; 11:21-45.	*See e.g.*, Ex. 1 ('763 patent) at 2:16-23; 12:5-17; 4:4-10; 12:38-83; 9:3-9:6; 6:56-7:6; 1:26-28; 8:45-55.

Patent	Claim Terms and Phrases	Plaintiff's Proposed Construction	Defendant's Proposed Construction	Plaintiff's Intrinsic Evidence	Defendant's Intrinsic Evidence
'763	"cells of the data processing cells are adapted to connect simultaneously to other cells of the data processing cells and to a plurality of at least one of cells and units of at least one of the memory cells, the data processing cells, and the at least one interface units" (claim 11)	the data processing cells are adapted to simultaneously connect each other and to a plurality of elements; each of the elements is either one of the memory cells, another one of the data processing cells, or the interface unit.	*See* Intel's construction for "programmably interconnecting at runtime" / "dynamically interconnecting at runtime"	Ex. 1, Figs. 1, 2(a)-2(c), 3, 4, 5 7:47-11:12; 11:21-45.	*See e.g.*, Ex. 1 ('763 patent) at 2:16-23; 12:5-17; 4:4-10; 12:38-83; 9:3-9:6; 6:56-7:6; 1:26-28; 8:45-55.

Patent	Claim Terms and Phrases	Plaintiff's Proposed Construction	Defendant's Proposed Construction	Plaintiff's Intrinsic Evidence	Defendant's Intrinsic Evidence
'763	"interconnect a data processing cell simultaneously to a plurality of at least one of cells and units of at least one of the memory cells, others of the data processing cells, and the at least one interface units" (claim 12)	simultaneously interconnect a data processing cell to a plurality of elements; each of the elements is either one of the memory cells, another one of the data processing cells, or the interface unit.	*See* Intel's construction for "programmably interconnecting at runtime" / "dynamically interconnecting at runtime"	Ex. 1, Figs. 1, 2(a)-2(c), 3, 4, 5 7:47-11:12; 11:21-45.	*See e.g.*, Ex. 1 ('763 patent) at 2:16-23; 12:5-17; 4:4-10; 12:38-83; 9:3-9:6; 6:56-7:6; 1:26-28; 8:45-55;

Patent	Claim Terms and Phrases	Plaintiff's Proposed Construction	Defendant's Proposed Construction	Plaintiff's Intrinsic Evidence	Defendant's Intrinsic Evidence
'763	"interconnect a plurality of data processing cells simultaneously to a plurality of at least one of cells and units of at least one of the memory cells and the interface units" (claim 13)	simultaneously interconnect each one of a plurality of data processing cells to a plurality of elements; each of the elements is either one of the memory cells or the interface unit.	*See* Intel's construction for "programmably interconnecting at runtime" / "dynamically interconnecting at runtime"	Ex. 1, Figs. 1, 2(a)-2(c), 3, 4, 5 7:47-11:12; 11:21-45.	*See e.g.*, Ex. 1 ('763 patent) at 2:16-23; 12:5-17; 4:4-10; 12:38-83; 9:3-9:6; 6:56-7:6; 1:26-28; 8:45-55.
'763	Preambles (claims 1 and 31)	Preambles are limiting.	Preambles are not limiting / no construction necessary	Ex. 1, Fig. 1, 2(a)-(c), 3, 4, 5, 6, 2:52-59; 5:53-6:21; 7:31-8:10; 8:26-31; 10:34-11:2; 11:13-20; Claims 20, 50.	Preambles are not limiting / no construction necessary

Patent	Claim Terms and Phrases	Plaintiff's Proposed Construction	Defendant's Proposed Construction	Plaintiff's Intrinsic Evidence	Defendant's Intrinsic Evidence
'301	Preambles (claims 3, 6, 8, 10, 12)	Preambles are limiting.	Claims 6, 8, 10, 12: Preambles are not limiting / no construction necessary. Claim 3: *See* Intel's construction for "data processing element" and/or "data processing elements adapted for programmably processing sequences"	Ex. 24, August 10, 2016 Remarks at 13-16; Ex. 3, Fig. 1; 1:25-36; 2:1-19; 4:43-46; 6:7-61; 8:64-9:2; 9:3-11; 9:44-55; 10:23-36; 12:66-13:11; claim 3.	Claims 6, 8, 10, 12: Preambles are not limiting / no construction necessary. Claim 3: "reconfigurable and sequential data processors where the data results from one processor are fed to another, for each processor to perform a separate computation" (*See* term "reconfigurable and sequential data processors where the data results from one processor are fed to another, for each processor to perform a separate computation")
'593	Preambles (claims 1 and 16)	Preambles are limiting.	Preambles are not limiting / no construction necessary	Ex. 4, 2:17-36, 3:34-39, 6:7-58, 7:41-59, 8:55-58, 9:22-26, 9:34-10:26, 12:7-16; Figs. 1-2, 9	*See e.g.*, Ex. 4 ('593 patent) at 3:34-44; 2:18-34.
'505	Preambles (claims 1, 14, 16-18, 27)	Preambles are limiting.	Preambles are not limiting / no construction necessary	Ex. 6, Figs. 1-19; 1:20-60; 6:55-67; 7:5-35; 12:20-13:17.	*See, e.g.*, Ex. 6 ('505 patent) at 2:40-42; *See, e.g.*, Ex. 30 ('505 File History) at 4863.

Patent	Claim Terms and Phrases	Plaintiff's Proposed Construction	Defendant's Proposed Construction	Plaintiff's Intrinsic Evidence	Defendant's Intrinsic Evidence
'605	"sequentially processing data"	passing results onto one or more other data processing units which are subsequently processing data	*See* Intel's construction for "data processing unit" and/or "data processing unit…adapted for sequentially processing data"	Ex. 24, August 10, 2016 Remarks at 13-16. Ex. 8, 4:50-53; Figs. 1, 2, 7:66-8:18, 8:34-59, 9:4-18, 9:37-44, 11:31-12:3; claim 1.	*See* term "data processing element" and/or "data processing elements adapted for programmably processing sequences"
'812	Preamble (claim 12)	Preamble is limiting.	Preamble is not limiting / no construction necessary	Ex. 9, Abstract, 2:5-14, 2:47-3:15, 8:7-20, 11:17-26, 31:56-32:6, 34:30-38 44:19-22, 159:20-23; Figs. 16, 18, 20, 77, 80. Ex. 21, Amendment & Remarks (May 18, 2015), Office Action (Feb. 3, 2015)	*See*, *e.g.*, Ex. 9 ('812 patent) at Abstract, 2:10-14, 2:47-3:15, 3:47-4:37, 5:29-7:2, 7:52-8:62, 9:1-10:29.

Patent	Claim Terms and Phrases	Plaintiff's Proposed Construction	Defendant's Proposed Construction	Plaintiff's Intrinsic Evidence	Defendant's Intrinsic Evidence
'047	"sequentially processing data" (claims 1-5, 8, 10, 15, 19, 22, 24)	passing results onto one or more other data processing units which are subsequently processing data	*See* Intel's construction for "data processing element" and/or "data processing unit…adaptable for sequentially processing data"	Ex. 24, August 10, 2016 Remarks at 13-16. Ex. 12, 4:54-57. Ex. 8, 7:66-8:18, 8:34-59, 9:37-44 (corresponding disclosures in Ex. 12)	*See* term "data processing element" and/or "data processing elements adapted for programmably processing sequences"
'047	Preambles (claims 1, 19)	Preambles are limiting.	Preambles are not limiting / no construction necessary	Ex. 12, Fig. 1; 2:24-34; 4:58-67; 8:1-7; 9:20-37; 11:57-2:4; Claims 19, 33. Ex. 8, 1:28-48, 2:45-67, 3:61-4:49, 6:14-67, 8:29-9:3, 13:54-14:3, Fig. 4, 5 (corresponding disclosures in Ex. 12)	Preamble is not limiting / no construction necessary

TERMS PROPOSED BY DEFENDANT

Patent	Claim Terms and Phrases	Plaintiff's Proposed Construction	Defendant's Proposed Construction	Plaintiff's Intrinsic Evidence	Defendant's Intrinsic Evidence
'763	"data processing cells, each adapted for sequentially executing" (claims 1, 31)	Plain and ordinary meaning. No construction necessary.	"reconfigurable processor function cells adapted for sequentially executing"	Ex. 1, Figs. 2(a)-2(c), 4; 1:23-44; 2:16-45; 3:18-33; 4:19-39; 5:17-6:35; 8:61-10:30; 10:23-30.	*See e.g.*, Ex. 1 ('763 patent) at 7:20-28; 1:23-25; 1:61-2:2; 3:18-33; 10:61-11:2; 3:58-4:2; 1:23-25; 3:34-51; 7:52-60; *see e.g.*, Ex. 37 (DE 196 54 846 A1) at Col. 17.

Patent	Claim Terms and Phrases	Plaintiff's Proposed Construction	Defendant's Proposed Construction	Plaintiff's Intrinsic Evidence	Defendant's Intrinsic Evidence
'763	"programmably interconnecting at runtime" / "dynamically interconnecting at runtime" (claims 1, 31)	No construction necessary for "programmably" or "dynamically." Plain and ordinary meaning. For "interconnecting at runtime," *See* PACT's proposed construction of "interconnecting at runtime at least one of data processing cells and memory cells with at least one of memory cells and one or more of the at least one interface unit."	"programmably reconfiguring interconnects at runtime" / "dynamically reconfiguring interconnects at runtime"	Ex. 1, Figs. 2(a)-2(c); 1:23-44; 2:16-45; 5:17-6:35; 8:61-10:30	*See e.g.*, Ex. 1 ('763 patent) at 2:16-23; 12:5-17; 4:4-10; 12:38-83; 9:3-9:6; 6:56-7:6; 1:26-28; 8:45-55.

Patent	Claim Terms and Phrases	Plaintiff's Proposed Construction	Defendant's Proposed Construction	Plaintiff's Intrinsic Evidence	Defendant's Intrinsic Evidence
'301	"data processing element" and/or "data processing elements adapted for programmably processing sequences" (claims 3, 6, 8-10, 12-14, 16-18, 23-26, 30, 32, 35)	Plain and ordinary meaning. No construction necessary.	"reconfigurable and sequential data processors where the data results from one processor are fed to another, for each processor to perform a separate computation"	Ex. 24, August 10, 2016 Remarks at 13-16. Ex. 3, 1:25-36; 2:1-19; 3:31-40, 7:58-8:11; 4:43-46, 6:7-61; 9:44-55; claim 3. Ex. 8, Abstract, 1:28-48, 2:45-67, 3:61-4:49, 6:14-67, 8:29-9:3, 11:31-12:3, 12:16-34, 13:53-14:3, Fig. 1, 4, 5 (corresponding disclosures in Ex. 3)	*See e.g.*, Ex. 36 ('047 File History) at 551-53; *See, e.g.*, Ex. 3 ('301 patent) at 4:43-46; 2:1-3; 11:23-28; 10:62; 11:49-58; 2:22-24; 1:26-36; 4:66-5:4; 5:21-32; 8:27-30.
'605	"data processing unit" and/or "data processing unit . . . adapted for sequentially processing data" (claim 1)	*See* PACT's proposed construction of "sequentially processing data."	"reconfigurable and sequential data processors where the data results from one processor are fed to another, for each processor to perform a separate computation"	Ex. 24, August 10, 2016 Remarks at 13-16. Ex. 8, 1:25-38; 2:4-23; 4:50-53. claim 1. Ex. 8, Abstract, 2:45-63, 11:31-12:3, 12:16-34, 13:53-59, Fig. 1, 4	*See* term "data processing element" and/or "data processing elements adapted for programmably processing sequences"

Patent	Claim Terms and Phrases	Plaintiff's Proposed Construction	Defendant's Proposed Construction	Plaintiff's Intrinsic Evidence	Defendant's Intrinsic Evidence
'605	"to a minimum" (claim 1)	Plain and ordinary meaning. No construction necessary.	"to a level no more than is required for the preservation of memory contents or the like"	Ex. 8, col.3:22-36; 4:18-33; 4:57-58; 5:28-56; 5:63-6:14; 7:3-20; 7:24-54; 7:55-61; 8:34-59; 10:1-19; 11:67-12:3; 13:8-30. Ex. 12, claims 16, 30.	*See, e.g.*, Ex. 32 ('605 File History) at 378; Ex. 8 at 3:24-30.

Patent	Claim Terms and Phrases	Plaintiff's Proposed Construction	Defendant's Proposed Construction	Plaintiff's Intrinsic Evidence	Defendant's Intrinsic Evidence
'812	"instruction dispatch unit…configured to dispatch software threads to the array data processor for parallel execution by the parallel processing arithmetic units" (claim 12)	Plain and ordinary meaning.	Subject to 35 U.S.C. §112, sixth paragraph Function: Dispatch software threads to the array data processor for parallel execution by the parallel processing arithmetic units. Structure: Fig. 80A, configuration unit (CT).	Ex. 9, 13:55-59, 16:44-45, 19:60-20:8, 20:56-58, 25:9-12, 26:37-46, 28:55-29:2, 31:43-55, 32:60-33:24, 34:29-48, 35:34-37, 36:7-14, 39:26-37, 43:33-35, 44:1-10, 44:42-58, 138:37-139:4, 140:21-27, 140:44-56, 158:46-49, 159:20-160:38, 162:62-66, 163:11-22, 164:53-56, 165:16-21 Figs. 13, 16-18, 20, 80A-C Ex. 21, Amendment & Remarks (May 18, 2015), Office Action (Feb. 3, 2015)	*See e.g.*, Ex. 33 ('812 File History) at Response to Rejection (5/18/15), Non-Final Rejection (2/17/15). *See e.g.*, Ex. 9 ('812 patent) at Fig. 77A-J, 80A-C.

Patent	Claim Terms and Phrases	Plaintiff's Proposed Construction	Defendant's Proposed Construction	Plaintiff's Intrinsic Evidence	Defendant's Intrinsic Evidence
'631	"a plurality of bus segments for each processor of the multiprocessor system" (claim 1)	Plain and ordinary meaning. No construction necessary.	"a plurality of bus segments for each processor of the multiprocessor system, each bus segment connected to only one of the processors"	Ex. 11, Claim 1; 13:52-15:60; Fig. 5 25:49-62; Fig. 6 26:38-41.	*See*, *e.g.*, Ex. 11 ('631 patent) at Figs. 5, 6; 15:25-27, 24:58-61, 26:42-47, 27:22-35; *See, e.g.*, Ex. 35 ('631 File History) at Response After Final, 1/14/16; *see also* Final Rejection, 10/29/15 (Claim Rejections - 35 USC 103).
'047	"data processing unit" and/or "data processing unit . . . adaptable for sequentially processing data" (claims 1-5, 8, 10, 15, 19, 22, 24)	*See* PACT's proposed construction of "sequentially processing data."	"reconfigurable and sequential data processors where the data results from one processor are fed to another, for each processor to perform a separate computation"	Ex. 24, August 10, 2016 Remarks at 13-16. '047 Patent, col.4:54-57. Ex. 12, 1:29-39; 2:4-23; claims 1-5, 8, 10, 15, 19, 22, 24; Ex. 8, Abstract, 2:45-63, 11:31-12:3, 12:16-34, 13:53-59, Fig. 1, 4 (corresponding disclosures in Ex. 12)	*See* term "data processing element" and/or "data processing elements adapted for programmably processing sequences"

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