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HYSTERESIS IN ELECTRONIC CIRCUITS: A CIRCUIT THEORIST'S PERSPECTIVE

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SUMMARY

In this exposition we hope to dispel some common misconceptions about the nature of hysteresis in electronic circuits. We show that the jumps which one observes when measuring the driving point or transfer characteristics of common 'hysteretic' elements are associated with parasitic dynamics in the circuit and therefore should not be considered part of the static characteristics.

We examine the Schmitt trigger circuit, which exhibits 'hysteresis' in its transfer characteristic, and study a neural-type pulse oscillator, one of a class of oscillators which relies for its operation on driving point 'hysteresis'. We illustrate the concepts of DC characteristics, the dynamic route, the jump phenomenon and parasitic dynamics. We show how a clear understanding of these circuit theoretic principles leads to better analysis and synthesis methods for 'hysteretic' circuits.

1. INTRODUCTION

In this paper we study the phenomenon whereby the driving point or transfer characteristic of an electronic circuit exhibits a 'loop'. The presence of such a 'loop' is commonly referred to as 'hysteresis' because the value of the output depends on both the present and past values of the input.

The principal features of electronic hysteresis elements which endear them to design engineers are rapid switching between states, inherent noise immunity and memory of the input. Consequently, these elements have become indispensable building blocks in a variety of noise rejection and oscillator circuits.

Traditionally, driving point and transfer hysteresis characteristics have been exploited in comparators, Schmitt triggers[1] and multivibrator circuits.[2] They are used in noisy environments to guard against false triggers, in communication systems to convert slowly varying analogue signals to digital form and in non-linear oscillators to produce relaxation wave forms.[2–4] More recently, they have been used to generate chaos[3,5] and in artificial neural networks[4,6] to model biological behaviours.

Despite its pervasive use, the loop hysteresis phenomenon is not widely understood. Consequently, models of it are often misleading; typical representations of the driving point (DP) and transfer characteristics (TC) of hysteretic elements consist of closed loops or disjoint line segments connected together by dashed lines and labelled with arrows,[1,2,7,8] quite unlike 'normal' DC characteristics (see Figure 1). In particular, the symbol commonly used in the integrated circuits literature to denote a Schmitt trigger is a stylized representation of a hysteresis loop in a transfer characteristic (see Figure 2). The loop consists of a flat top and bottom, joined together by two line segments. These joining lines are usually very steep, suggesting a region of high gain in the transfer characteristic. This begs the questions: what is the value of this gain? How do we measure it? Indeed, does it make sense to talk about a gain at all?[9]

In this work we hope to dispel some common misconceptions about the nature of hysteresis in electronic circuits. We will explain how it arises and, with an understanding of the mechanism, how to model it. We will show by example that resistive models of hysteresis which assume discontinuous characteristics and jumps are incorrect. Not only do they complicate the analysis unnecessarily at times, but they do not always yield solutions. Further, we will show that it is necessary to augment these resistive models with parasitic energy storage elements in order to explain the mechanism for switching between states.

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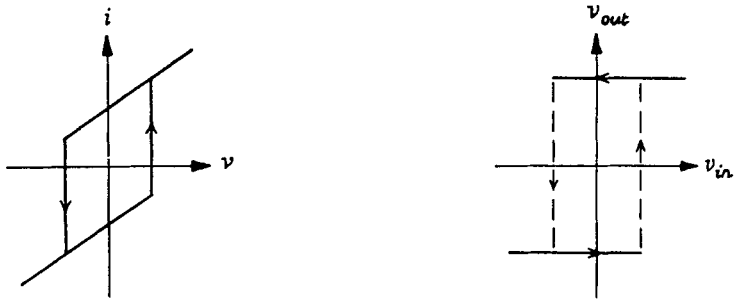
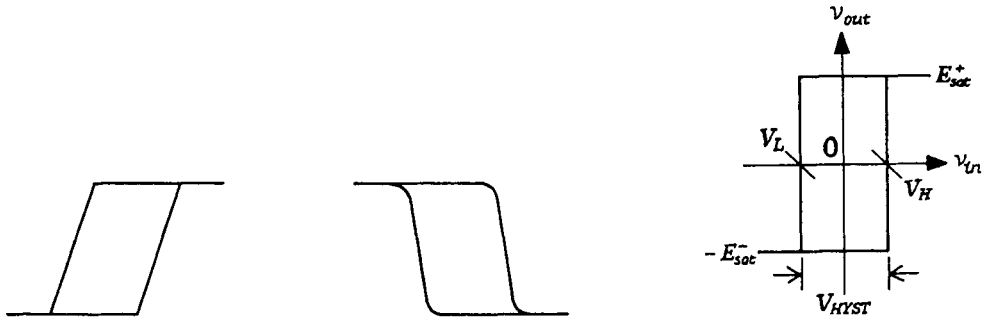


(a) (b)

Figure 1. Typical representations of hysteresis in (a) driving point and (b) transfer characteristics (adapted from References 2 and 7 respectively)



(a) (b) (c)

Figure 2. Schmitt trigger symbols: (a) from Reference 1; (b) from Reference 8; (c) adapted from Reference 10

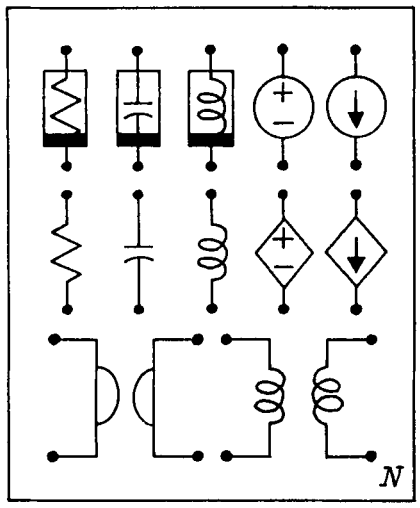
In Section 2 we review the concepts of driving point and transfer characteristics. In Sections 3 and 4 we examine representative examples of circuits which exhibit hysteretic behaviour—the regenerative comparator (more commonly known as the Schmitt trigger), whose voltage transfer characteristic exhibits a 'hysteresis loop', and the neural-type pulse oscillator,[10] which relies for its operation on a 'hysteresis resistor' driving point characteristic.[2] We show how the operation of these circuits can be explained precisely by using non-linear circuit theory.[11,12]

The circuits which we present here are not new; most will be well known to students and practising engineers alike. Some of the behaviours, though, may be quite surprising. Our objective is to present an alternative perspective on hysteresis in electronic circuits: to illustrate the conceptual framework of non-linear circuit theory in the context of which hysteretic behaviour is readily understood.

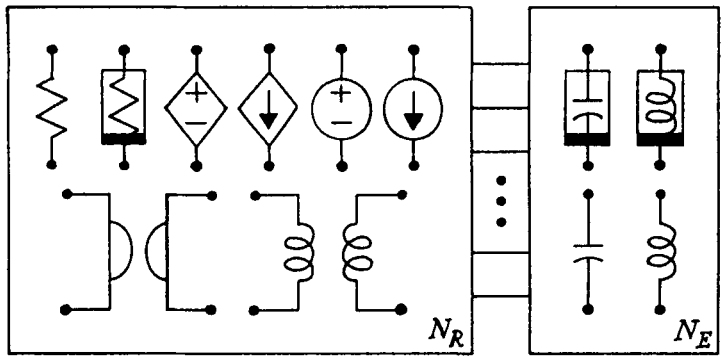
2. DRIVING POINT AND TRANSFER CHARACTERISTICS

Before we proceed further, it is important to be clear on what are meant by the driving point (DP) and transfer characteristics (TC) of a network.[11] This section briefly reviews these concepts.

The goal of circuit modelling is to produce a simple mathematical macromodel of a network which gives an adequate analytical description of its operation. The first step in analysing a circuit model N (such as that shown in Figure 3(a)) which contains resistive and energy storage elements is to split the network into two parts. The energy storage subnetwork N_E is formed by extracting all capacitors and inductors from N. What remains are the resistive elements (resistors, independent and controlled sources, ideal transformers, gyrators) which are grouped together to form a single resistive subnetwork N_R (Figure 3(b)).



(a)



(b)

Figure 3. (a) Network N to be analysed; (b) partition the network into resistive and energy storage subnetworks (N_R and N_E respectively)

A solution or operating point of this resistive subnetwork is a set of branch voltages and currents (normally piled up to form a solution vector) which satisfy Kirchhoff's current law (KCL), Kirchhoff's voltage law (KVL) and the constitutive relations of the resistive elements which comprise the circuit.[11] The locus of operating points is the set of all solutions of the network. We typically describe the locus of operating points by looking at two components of the solution vector (branch voltages or currents) at a time. If we apply an ideal DC voltage or current source at one branch of the circuit N_R and measure the corresponding voltage or current at another branch, we obtain a graphical relationship between two components. This relationship is called a driving point or transfer characteristic depending on where the measurements are made.

The locus of operating points in the $V-I$ plane obtained by applying a voltage source V_S (current source I_S, respectively) at one pair of terminals of N_R (called the driving point terminals) and measuring the resulting current i into (voltage v across, respectively) the same pair of terminals (as shown in Figure 4) is called a *driving point* (DP) characteristic.

The locus of operating points obtained by making measurements at a pair of terminals (called the transfer terminals) different from the driving point terminals (see Figure 5) is called *transfer characteristic* (TC).

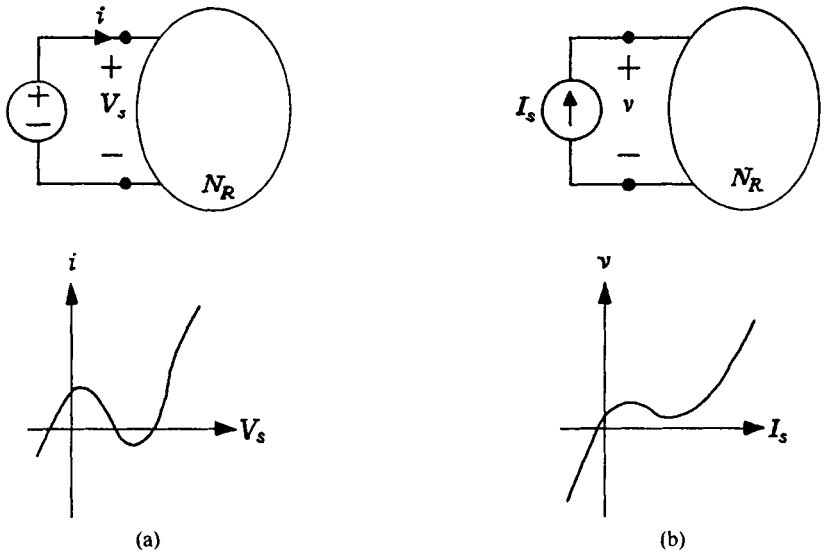


Figure 4. Driving point characteristics of resistive subnetworks N_R: (a) N_R voltage-controlled and driven by a voltage source; (b) N_R current-controlled and driven by a current source

Clearly, each graphical relationship between a pair of branch voltages and/or currents is either a driving point or a transfer characteristic.

The importance of the DP representation at a pair of terminals of N_R is that it can be interpreted as the $V-I$ curve of the equivalent two-terminal resistor obtained by considering the entire network N_R as a two-terminal black box as far as the driving point terminals are concerned.[11] We will use this fact when analysing the switching behaviour of 'hysteretic' elements in Sections 3 and 4.

The DP characteristic of a 'black box' network is independent of how the box is connected to other

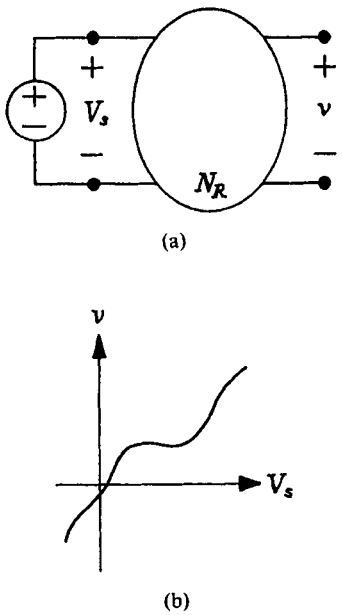


Figure 5. Voltage transfer characteristic for a resistive network N_R. Note that the dependent voltage must be measured without loading the measurement port[11]

components and is thus a true characterization of the network.[11] In contrast the TC is an incomplete characterization of the network since it is defined for a specific load on the measurement port (open circuit for a transfer voltage, short circuit for a transfer current) and therefore changes when the transfer terminals are connected to a different load. Consequently, the TC is of little use in predicting the behaviour of a circuit when embedded in a larger network unless the load matches that specified in the definition.

It is important to keep in mind that the driving point and transfer characteristic are defined and meaningful only for resistive networks. To use them to represent a network as a 'black box' is to assume that the effects of internal dynamics are negligible; equivalently, one supposes that the circuit is entirely resistive. Therein lies the problem with describing 'hysteretic' elements in terms of their driving point and transfer characteristics: the 'hysteretic' behaviour is caused by parasitic energy storage elements, which one fails to include in a purely resistive model. If parasitic dynamics are included in the model, the switching mechanism and associated hysteresis are readily understood.

3. HYSTERETIC TRANSFER CHARACTERISTICS

3.1. The Schmitt trigger

In this subsection we study a class of circuits which have 'hysteretic' transfer characteristics. By a hysteretic transfer characteristic we mean that the output changes state at one value of the input if the latter is increasing and at a different value of the input if it is decreasing. The most common example of such an element is the regenerative comparator, usually referred to as the Schmitt trigger.[13]

The Schmitt trigger is widely used in mixed mode systems to convert a slowly varying analogue input voltage to an almost discontinuous signal having abrupt jumps. This circuit has extensive applications for noise rejection in line receivers, comparators and other signal-processing circuits. The basic voltage-follower Schmitt trigger can be realized by using positive feedback around an operational amplifier as shown in Figure 6.[14]

Like many op amp circuits, the Schmitt trigger is routinely described in terms of its transfer characteristic. In the following we will show that the discontinuous voltage transfer characteristic which one obtains (by measurement or simulation) by increasing the input voltage and then decreasing it, all the while monitoring the output voltage, is typically not the complete DC transfer characteristic of the Schmitt trigger.

Further, by definition, even the correct DC transfer characteristic is insufficient to describe the behaviour of the circuit because switching is a dynamic phenomenon which results from the presence of parasitic energy storage elements.

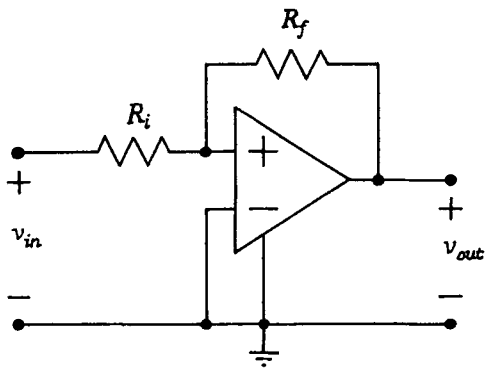


Figure 6. Non-inverting operational amplifier Schmitt trigger circuit. $R_i = 10\ k\Omega$, $R_f = 20\ k\Omega$, the op amp is 1/4 TL074

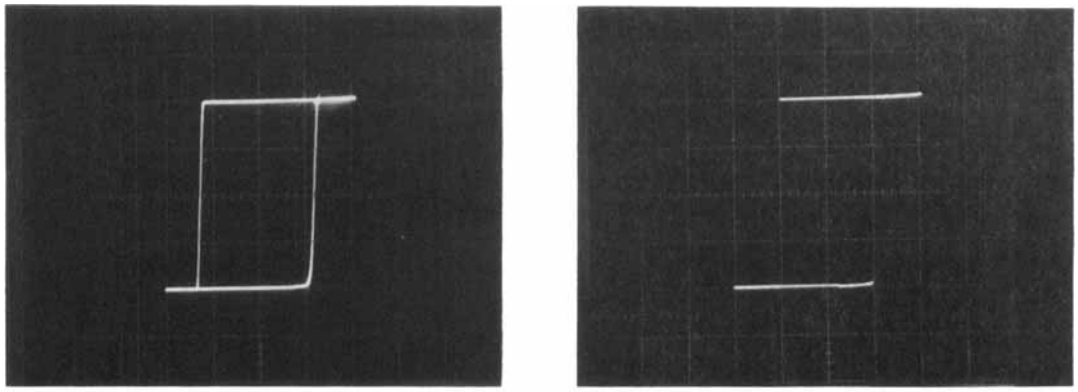


Figure 7. Experimentally measured voltage transfer characteristics for the op amp Schmitt trigger circuit in Figure 6: (a) hysteresis loop; (b) discontinuous characteristic. Horizontal and vertical scales are v_{in} and v_{out}, respectively, 2 V/div each

Experimental observations. If one measures the characteristics of the op amp Schmitt trigger circuit shown in Figure 6 by slowly increasing the input voltage v_{in} and recording the output v_{out}, one finds that as the input is increased from a large negative value, the output remains in negative saturation until a positive threshold voltage V_H is reached, at which time the output quickly switches to positive saturation. The output remains in positive saturation until the input is reduced through V_L, the lower threshold for switching, at which point it jumps back to negative saturation. The difference between V_H and V_L is called the *hysteresis voltage* V_{HYST} (see Figure 2(c)).

Figure 7 shows two $X-Y$ oscilloscope traces produced by applying a triangular voltage wave form v_{in} at the input of the Schmitt trigger in Figure 6 (X-axis) and plotting the output on the Y-channel. With an input sweep frequency of 10 kHz we obtain a closed 'hysteresis' loop (Figure 7(a)). If the frequency is reduced almost to DC, the jumps become breaks and the measured transfer characteristic appears to be discontinuous (Figure 7(b)).

Our experimental observations (Figure 7) that the shape of the input–output voltage transfer characteristic varies with frequency suggest that switching is a dynamic phenomenon. We shall show in Section 3.3 that the jump mechanism is indeed a manifestation of parasitic dynamics. Before we begin

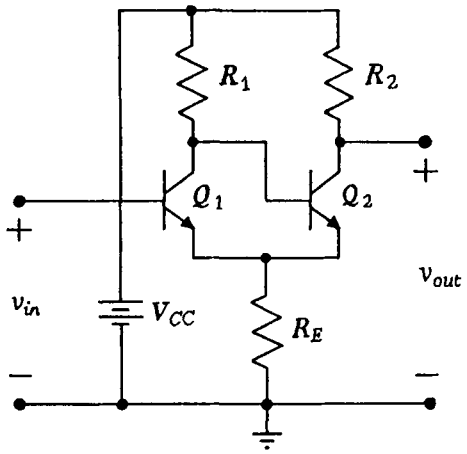


Figure 8. TTL Schmitt trigger circuit (adapted from Reference 1). $V_{CC} = 5$ V, $R_1 = 3{\cdot}9$ kΩ, $R_2 = 2{\cdot}7$ kΩ, $R_E = 1$ kΩ, Q_1 and Q_2 are 2N1893

to develop a complete dynamic model of the circuit, though, we should be sure that the resistive subnetwork accurately reflects its DC characteristics.

Simulation results. Computer simulations as well as experimental observations can easily lead one to believe that the TC of the Schmitt trigger is discontinuous. Consider the transistor circuit shown in Figure 8. This is the standard circuit configuration which is used in the digital TTL series Schmitt trigger.[1,15] We measured the transfer characteristic of this circuit experimentally by applying 0–5 V sawtooth voltage wave form at the input. The sweep frequency was 0·05 Hz. The observed TC is shown in Figure 9(a). Note that it consists of two disconnected horizontal segments.

Using SPICE 2G6 and the default BJT model parameters, we plotted the DC transfer characteristic of the network by increasing the input voltage from zero to 4 V and then decreasing it back to zero. The resulting transfer characteristic is shown in Figure 9(b). This characteristic too is discontinuous.

It is tempting to conclude that the Schmitt trigger has a two-segment discontinuous transfer characteristic. The fact that the segments are disconnected (or are possibly connected by steep sides) should not cause concern. Because the DC characteristics of networks are relationships (between voltages and currents which satisfy Kirchhoff's voltage and current laws) and not necessarily functions, it is perfectly legitimate from a circuit theoretic point of view to have a discontinuous transfer characteristic. It is also perfectly legitimate to have vertical segments joining the horizontal portions of the characteristic to form a loop.

It might come as a surprise, therefore, to learn that the true DC transfer characteristic of the Schmitt trigger neither exhibits a loop nor is discontinuous. With careful analysis, experimental methods and simulation techniques we will show how to determine the true DC characteristics of these circuits.

3.2 The non-inverting op amp Schmitt trigger: transfer characteristic

In this subsection we will derive the complete DC transfer characteristic of the op amp Schmitt trigger shown in Figure 6 by using piecewise-linear (PWL) circuit analysis.[12] Similar PWL studies of other Schmitt trigger circuit configurations can be found in References 16 and 17.

While the characteristics which we derive here can be obtained by other (possibly quicker) means, PWL analysis has the advantage that it provides an algorithm for reducing a complex non-linear problem to an equivalent set of linear problems.[18,19] The solutions and regions of validity of these linear circuits are determined symbolically either by hand (as we do here) or by computer. The linear regions are then jointed together to reconstruct the solution of the original non-linear problem.

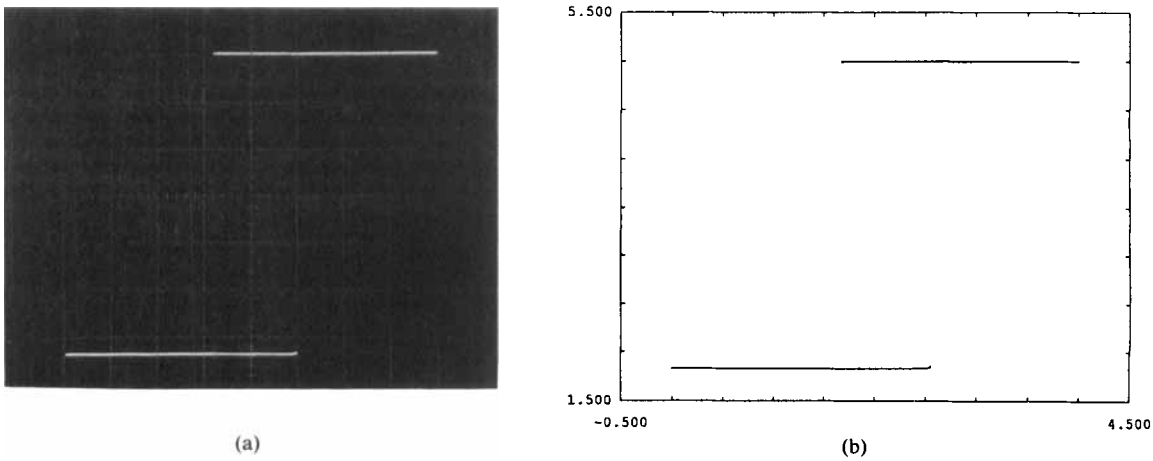


Figure 9. Partial input–output voltage transfer characteristics for the TTL Schmitt trigger of Figure 8: (a) measured (horizontal and vertical scales v_{in} and v_{out} 500 mV/div); (b) SPICE simulation (default BJT model parameters)

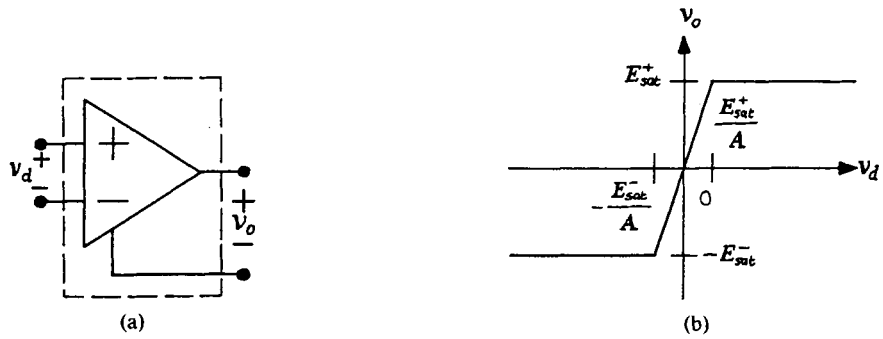


Figure 10. (a) Finite gain op amp model[12] and (b) its three-segment PWL voltage transfer characteristic

Throughout this paper we model the op amp by a voltage-controlled voltage source with a three-segment piecewise-linear DC transfer characteristic (finite gain non-linear op amp model[12]). The transfer characteristic of the finite gain op amp model is shown in Figure 10 and summarized in Table I; the value of v_d determines whether the op amp is operating in the negative saturation, linear or positive saturation region. For completeness, this model takes into account the finite gain A associated with the linear region region of a real op amp; by letting A become infinite, we recover the ideal (infinite gain) op amp model.[12]

Piecewise-linear circuit analysis of the op amp Schmitt trigger is performed by replacing the op amp with its linear and saturation models in turn and performing a linear analysis in each region. We first substitute the idealized finite gain model of Figure 10 for the real op amp in Figure 6 and then replace this voltage-controlled voltage source by its equivalent circuit in each of the three regions of operation, as shown in Figure 11. We analyse the resulting three linear circuits shown in Figure 12. For convenience we have abbreviated v_{in} by v_i and v_{out} by v_o in the analysis.

Op amp in negative saturation (Figure 12(a)). Writing KCL at the non-inverting input of the op amp, we obtain

$$i = G_i(v_d - v_i) + G_f(v_d - v_o) = -G_i v_i + (G_f + G_i)v_d - G_f v_o$$

Table I

− Sat	Linear	+ Sat
$v_d \leqslant -\frac{E_{sat}^-}{A}$	$-\frac{E_{sat}^-}{A} \leqslant v_d \leqslant \frac{E_{sat}^+}{A}$	$v_d \geqslant \frac{E_{sat}^+}{A}$
$v_o = -E_{sat}^-$	$v_o = Av_d$	$v_o = E_{sat}^+$

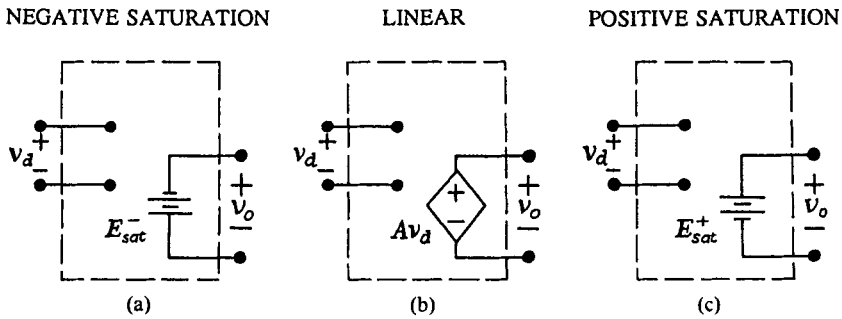


Figure 11. Equivalent finite gain op amp models for (a) the negative saturation region, (b) the linear region and (c) the positive saturation region

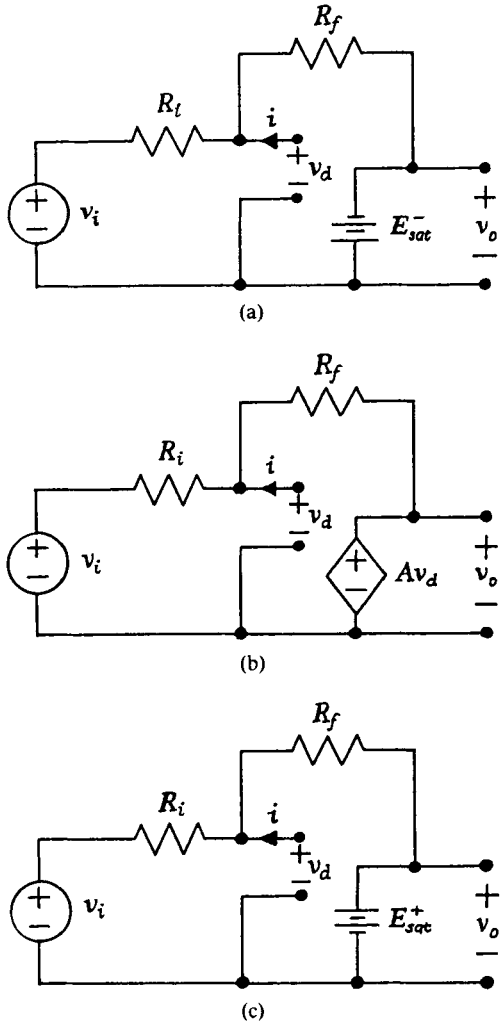


Figure 12. Equivalent circuits for the non-inverting op amp Schmitt trigger (Figure 6) in each region of the finite gain op amp model: (a) negative saturation region; (b) linear region; (c) positive saturation region

where $G_i = 1/R_i$ and $G_f = 1/R_f$. In this region $v_o = -E_{sat}^-$. Hence

$$i = G_i v_i + (G_f + G_i)v_d + G_f E_{sat}^- \tag{1}$$

For the ideal op amp model the controlling branch is an open circuit ($i = 0$); this gives

$$v_d = \frac{G_i v_i - G_f E_{sat}^-}{G_i + G_f}$$

To determine the boundary of the negative saturation region, we have from Table I that $v_o = -E_{sat}^-$ when $v_d \leqslant -E_{sat}^-/A$. Equivalently,

$$\frac{G_i v_i - G_f E_{sat}^-}{G_i + G_f} \leqslant \frac{E_{sat}^-}{A}$$

Thus the op amp is in negative saturation when

$$v_i \leqslant -\frac{(1 - A)G_f + G_i}{AG_i} E_{sat}^-$$

Op amp linear (Figure 12(b)). In the linear region $v_o = Av_d$. Hence

$$i = -G_i v_i + (G_f + G_i)v_d - G_f A v_d = -G_i v_i + [(1 - A)G_f + G_i]\, v_d \tag{2}$$

With $i = 0$ as before this gives

$$v_d = \frac{G_i v_i}{(1 - A)G_f + G_i}$$

The input-output voltage gain for the Schmitt trigger when the op amp is in its linear region is thus defined by

$$v_o = \frac{AG_i}{(1 - A)G_f + G_i}\, v_i$$

To determine the extent of the linear region, recall that the op amp operates in its linear region whenever

$$-\frac{E_{sat}^-}{A} \leqslant v_d \leqslant \frac{E_{sat}^+}{A}$$

Equivalently,

$$-\frac{E_{sat}^-}{A} \leqslant \frac{G_i v_i}{(1 - A)G_f + G_i} \leqslant \frac{E_{sat}^+}{A}$$

Thus the op amp behaves linearly for

$$\frac{(1 - A)G_f + G_i}{AG_i}\, E_{sat}^+ \leqslant v_i \leqslant -\frac{(1 - A)G_f + G_i}{AG_i}\, E_{sat}^-$$

Op amp in positive saturation (Figure 12(c)). In this region $v_o = E_{sat}^+$. Hence

$$i = -G_i v_i + (G_f + G_i)v_d - G_f E_{sat}^+ \tag{3}$$

With $i = 0$ once more,

$$v_d = \frac{G_i v_i + G_f E_{sat}^+}{G_i + G_f}$$

Now $v_o = E_{sat}^+$ when

$$v_d \geqslant \frac{E_{sat}^+}{A}$$

Equivalently,

$$\frac{G_i v_i + G_f E_{sat}^+}{G_i + G_f} \geqslant \frac{E_{sat}^+}{A}$$

Thus the op amp is in positive saturation when

$$v_i \geqslant \frac{(1 - A)G_f + G_i}{AG_i}\, E_{sat}^+$$

The resulting transfer characteristic is shown graphically in Figure 13 and summarized in Table II.

Note that the characteristic consists of three distinct segments whose endpoints correspond to the breakpoints of the piecewise-linear TC of the op amp. Because the characteristic is folded back on itself to form a mirrored letter Z, a given value of v_i between the folds (in the region of 'hysteresis') does not produce a unique output voltage v_o. Nevertheless, the output is uniquely determined by specifying both v_i and v_d.

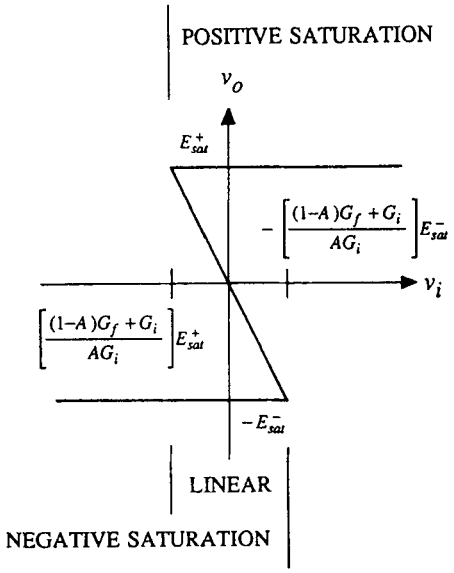


Figure 13. Voltage transfer characteristic (summarized in Table II) for the op amp Schmitt trigger shown in Figure 6 (identify v_i with v_{in} and v_o with v_{out})

Experimental verification. We confirmed this analysis experimentally by using the circuit shown in Figure 14. The network consists of a summing amplifier (top), a Schmitt trigger (with AC feedback, bottom) and an independent voltage source (top left). To measure the TC, we must find all operating points of the Schmitt trigger, where each operating point corresponds to a DC solution of this circuit.† For simplicity we assume that the op amps are ideal;[12] they have infinite input impedance, zero output impedance and exhibit infinite gain in their linear regions of operation. We shall see that this model accurately reflects the behaviour of the real circuit. In particular, the error is assuming $A \to \infty$ instead of the typical experimental value of 100 000 is just 0·001%.

At DC the capacitor C_f draws no current, so we can replace it by an open circuit when drawing the DC equivalent circuit for the network. Since no current flows into the input terminals of the ideal op amp model,[12] the voltage drop across R_b at DC is zero. Hence we can also remove R_b and examine the reduced DC equivalent circuit, shown in Figure 15.

Table II

Op amp	v_d	v_o	Valid for
– Sat	$v_d \leqslant -\dfrac{E^-_{sat}}{A}$	$-E^-_{sat}$	$v_i \leqslant -\dfrac{(1-A)G_f+G_i}{AG_i}E^-_{sat}$
Linear	$-\dfrac{E^-_{sat}}{A} \leqslant v_d \leqslant \dfrac{E^+_{sat}}{A}$	$\dfrac{AG_i}{(1-A)G_f+G_i}v_i$	$\dfrac{(1-A)G_f+G_i}{AG_i}E^+_{sat} \leqslant v_i \leqslant -\dfrac{(1-A)G_f+G_i}{AG_i}E^-_{sat}$
– Sat	$v_d \geqslant \dfrac{E^+_{sat}}{A}$	E^+_{sat}	$v_i \geqslant \dfrac{(1-A)G_f+G_i}{AG_i}E^+_{sat}$

† A real op amp such as the TL074 has a small non-zero output impedance which in this case is considerably smaller than R_H and consequently has negligible loading effect on the TC.

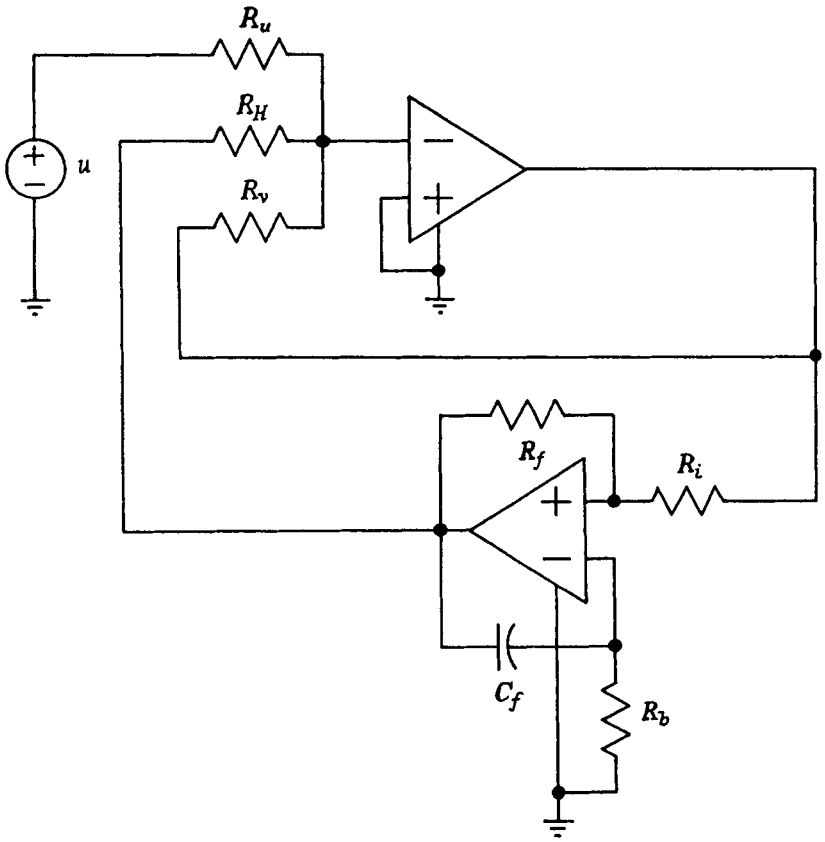


Figure 14. Op amp network for determining the TC of the Schmitt trigger of Figure 6. The circuit consists of an independent voltage source u (top left), an inverting summer (top) and a Schmitt trigger with AC feedback (bottom). $R_u = 20\ k\Omega$, $R_H = 20\ k\Omega$, $R_v = 20\ k\Omega$, $R_f = 20\ k\Omega$, $R_i = 10\ k\Omega$, $R_b = 470\ \Omega$, $C_f = 470\ pF$, op amps are 1/4 TL074

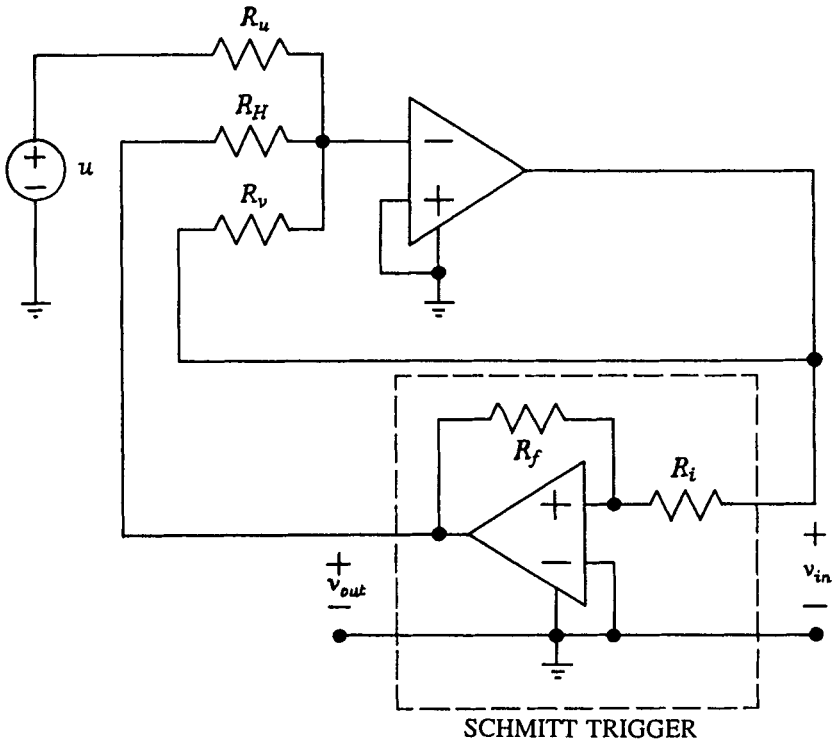


Figure 15. DC equivalent circuit of Figure 14. Note the Schmitt trigger at the bottom, which is similar to that in Figure 6

We assume initially that the upper op amp is operating in its linear region; therefore its inverting input is a virtual ground. Writing KCL at the inverting input of the upper op amp, we obtain

$$G_u u + G_H v_{out} + G_v v_{in} = 0$$

where $G_u = 1/R_u$, $G_H = 1/R_H$ and $G_v = 1/R_v$. We recognize this as the governing equation of an inverting summing amplifier.

If we let $G_u = G_H = G_v$, then the summing amplifier is simply imposing the constraint

$$u + v_{out} + v_{in} = 0$$

or equivalently,

$$u = -(v_{out} + v_{in})$$

Setting $u = 0$, we obtain $v_{out} = -v_{in}$. Since the ideal op amp model has zero output impedance (and is therefore insensitive to loading effects), the DC solution(s) (operating point(s) of the circuit) can be determined by intersecting the line $v_{out} = -v_{in}$ with the transfer characteristic of the Schmitt trigger.

The particular set of values in our experimental circuit ($A \to \infty$, $E_{sat}^{+} = 4$ V, $E_{sat}^{-} = 4$ V, $R_f = 20$ kΩ, $R_i = 10$ kΩ) yields the three-segment piecewise-linear transfer characteristic shown graphically in Figure 16(a) and summarized in Table III.

Intersecting the line $v_{out} = v_{in}$ with the characteristic (as shown in Figure 16(b)) now gives a unique operating point at the origin, exactly as is found experimentally. It is instructive to note that this immediately rules out the possibility that the TC is either discontinuous (which would yield no operating point (Figure 16(c)) or forms a loop (which would produce multiple solutions (Figure 16(d)).

By sweeping u from -8 to 8 V, we traced out the entire transfer characteristic. The resulting plot of v_{out} versus v_{in} is shown in Figure 16(e) and confirms our analysis. Note that $-8 < u < 8$ V implies that $-4 < v_{in} < 4$ V, so the summing op amp remains in its linear region throughout; this validates our earlier assumption that its inverting terminal is a virtual ground.

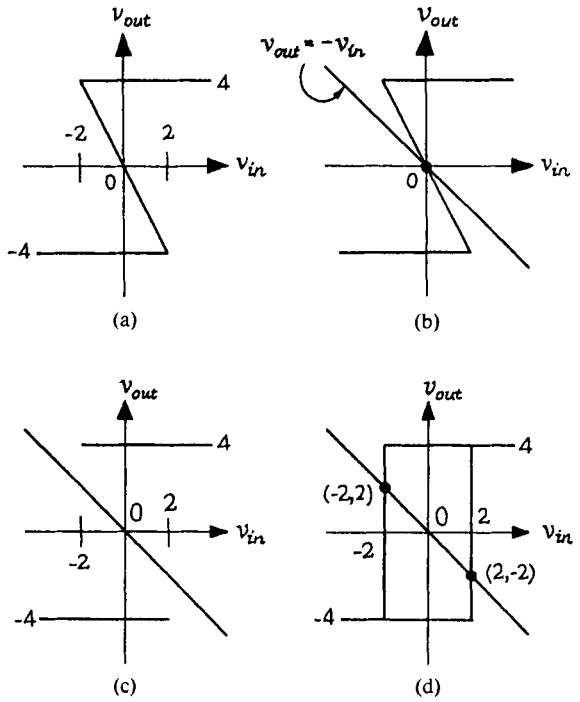
Verification by simulation. How do we reconcile this transfer characteristic with the SPICE results which suggested that the TC might be discontinuous? The reason for the discrepancy is simply that the two-segment transfer characteristic is incomplete because circuit simulation programmes such as SPICE which use the Newton–Raphson method[20] for DC analysis have trouble locating more than one solution. The Newton–Raphson method depends for its convergence on having a good initial guess of the answer. If there are multiple solutions (as in the 'hysteresis' region of the transfer characteristic), the simulator either finds one operating point or bounces back and forth between solutions without converging (as happens at the turning points of the TC).

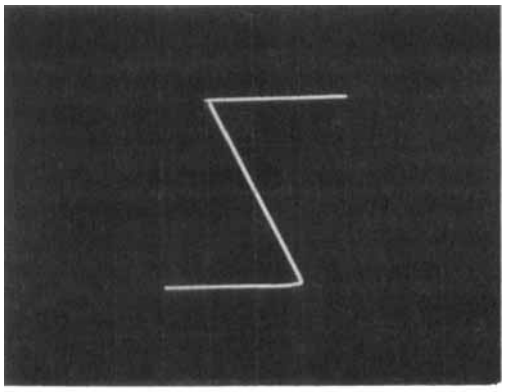
With more care we plotted the complete DC transfer characteristic of the TTL Schmitt trigger circuit using SPICE; the result is a continuous curve (Figure 17(a)). The upper and lower horizontal segments are exactly as before (compare with Figure 9); the middle segment of this plot was obtained by starting the DC analysis almost at the centre of the negative gain portion ($v_{in} = 2{\cdot}1$ V), increasing v_{in} and then restarting from the centre and decreasing v_{in}. These results were confirmed experimentally (Figure 17(b)) by using the constraining circuit shown in Figure 18.† Once again our experimental observations match the SPICE simulations exactly and confirm that the TC is continuous.

3.3. *Hysteresis: the complete picture*

We have shown that the TC of the op amp Schmitt trigger circuit is neither a loop nor discontinuous but is shaped like a mirrored letter Z. Nevertheless, even this complete TC cannot explain the switching

† The unity-gain buffer on the lower left is necessary because the TC description specifies non-instrusive (no-load) voltage and current measurements.[11]





(e)

Figure 16. Complete transfer characteristics of the non-inverting op amp Schmitt trigger oscillator. (a) Theoretical solution. (b) DC solution for the circuit of Figure 14 determined by intersecting the line $v_{out} = -(v_{in} + u)$ with the theoretical input–output voltage transfer characteristic. With $u = 0$ there is a unique solution at the origin. (c,d) DC solutions for the circuit of Figure 14 (with $u = 0$) predicted by assuming (c) a discontinuous TC and (d) a loop TC with vertical sides. The discontinuous TC predicts no solution; the loop ought to have two solutions at $(v_{in}, v_{out}) = (2, -2)$ and $(-2, 2)$. (e) Experimentally measured TC for the circuit in Figure 14 (horizontal and vertical scales are 2 V/div each); compare with (a)

Table III

Op amp	v_{out}	Valid for
− Sat	− 4 V	$v_{in} \leqslant 2$ V
Linear	$-2v_{in}$	-2 V $\leqslant v_{in} \leqslant 2$ V
+ Sat	4 V	$v_{in} \geqslant 2$ V

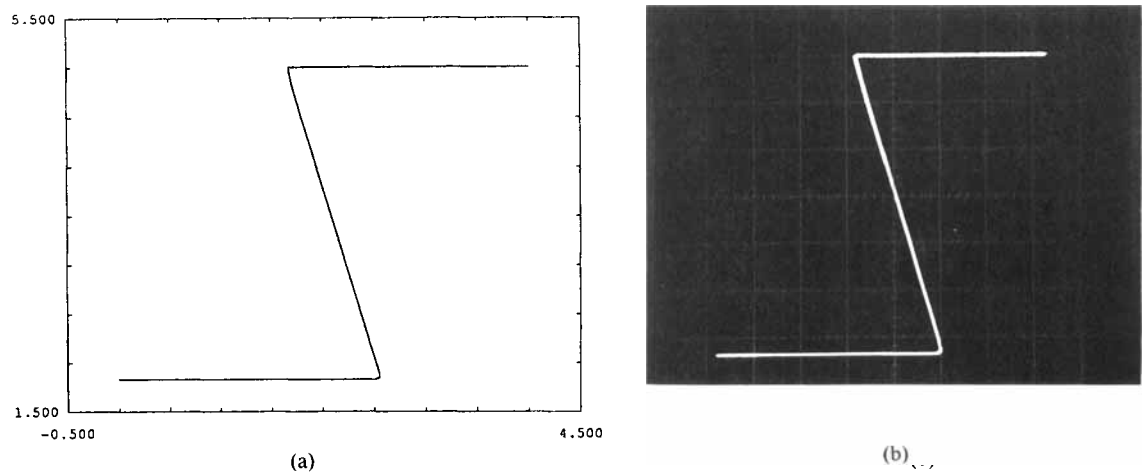


Figure 17. Complete input–output voltage transfer characteristic for the TTL Schmitt trigger of Figure 8: (a) SPICE simulation; (b) measured (horizontal and vertical scales 500 mV/div)

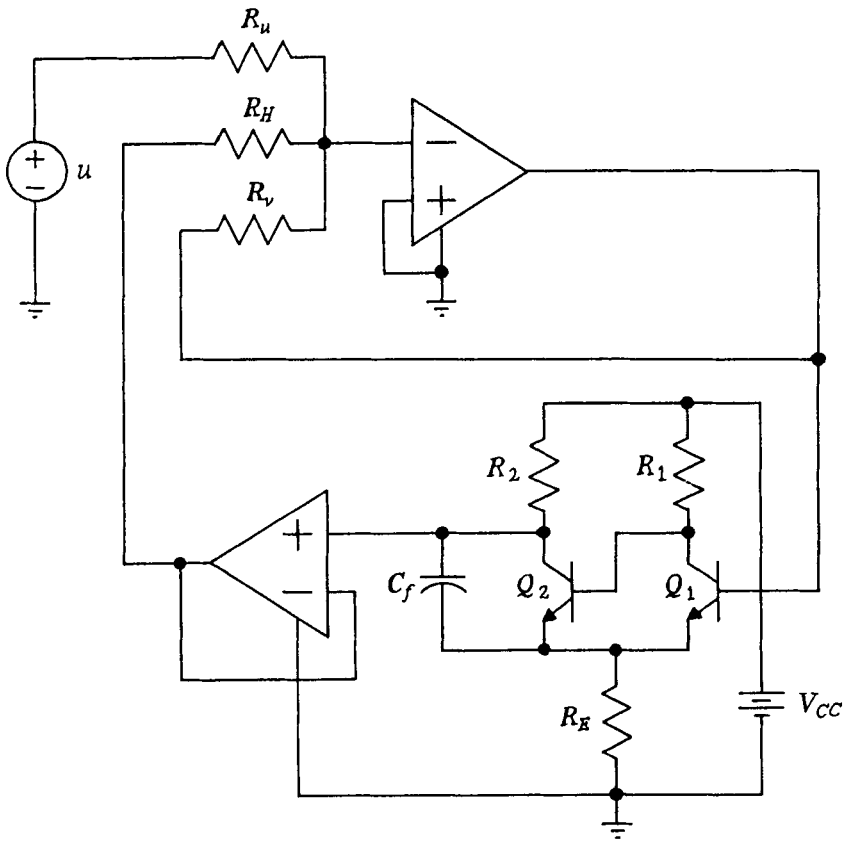


Figure 18. Circuit to measure the voltage TC of the TTL Schmitt trigger shown in Figure 8. Capacitor C_f provides stabilizing AC feedback. The unity-gain buffer isolates the output from the load R_H. $R_u = 18\ k\Omega$, $R_H = 18\ k\Omega$, $R_v = 18\ k\Omega$, $R_1 = 3{\cdot}9\ k\Omega$, $R_2 = 2{\cdot}7\ k\Omega$, $R_E = 1\ k\Omega$, $C_f = 5\ \mu F$, Q_1 and Q_2 are 2N1893, op amps are 1/4 TL074

mechanism. The inadequacy of the TC description stems from the simple fact that the DC transfer characteristic of any circuit is a static object which characterizes only the resistive part of the network.

Recall that every DC operating point lies on the transfer characteristic. Our experimental evidence (Figure 7(a)) shows that in the course of switching, when the input voltage increases monotonically, the output voltage also increases monotonically. In particular, the output voltage does not move from $-E_{sat}^{-}$ to E_{sat}^{+} along the (static) transfer characteristic, since this would require that the input should decrease while the output switched from negative to positive saturation (in order to follow the Z-characteristic). The jumps which occur when one measures the physical circuit are clearly not part of the transfer characteristic and therefore must be dynamic phenomena which result from the presence of parasitic energy storage elements.

Equivalently, we known from Section 3·2 that the TC of the op amp Schmitt trigger is continuous: it consists of three connected segments. Experimentally we could measure just the two saturated segments of the open-loop characteristic. We could not see the middle segment; therefore it is unstable, implying that dynamics are involved.

By expecting to be able to characterize the Schmitt trigger with a transfer characteristic, one implicitly assumes that the network is resistive, i.e. that the effects of parasitics are negligible at the frequencies of interest. This is clearly not a valid assumption. Therefore a complete model of the Schmitt trigger must include at least one energy storage element.

3.4. Dynamical analysis of the op amp Schmitt trigger

Let us consider the op amp Schmitt trigger circuit once more, this time assuming that there is a small amount of parasitic capacitance C_p across the input terminals of the op amp (see Figure 19). Once again, for the sake of completeness, we use the finite gain (resistive) op amp model:[12] the input terminals draw no current, the output resistance is zero and the voltage transfer relation is a three-segment piecewise-linear characteristic (see Figure 10). The op amp has finite gain A ($\gg 1$) in its linear region.

The equivalent circuit N is shown in Figure 20(a), where $f(\cdot)$ is the voltage transfer characteristic of the op amp. Choosing v_d as the state variable and writing the state equation, we obtain

$$C_p \frac{dv_d}{dt} = G_i(v_i - v_d) + G_f(v_o - v_d)$$

where $G_i = 1/R_i$ and $G_f = 1/R_f$.

The output voltage is defined by the piecewise-linear read-out map

$$v_o = f(v_d)$$

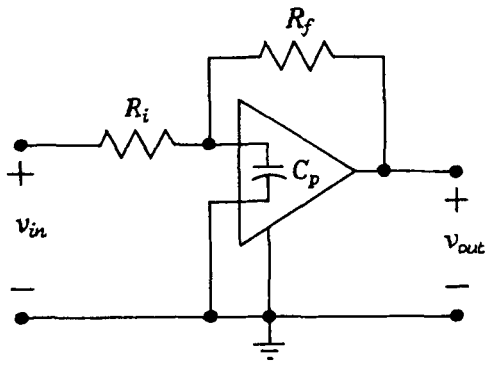


Figure 19. Op amp Schmitt trigger with parasitic input capacitance C_p

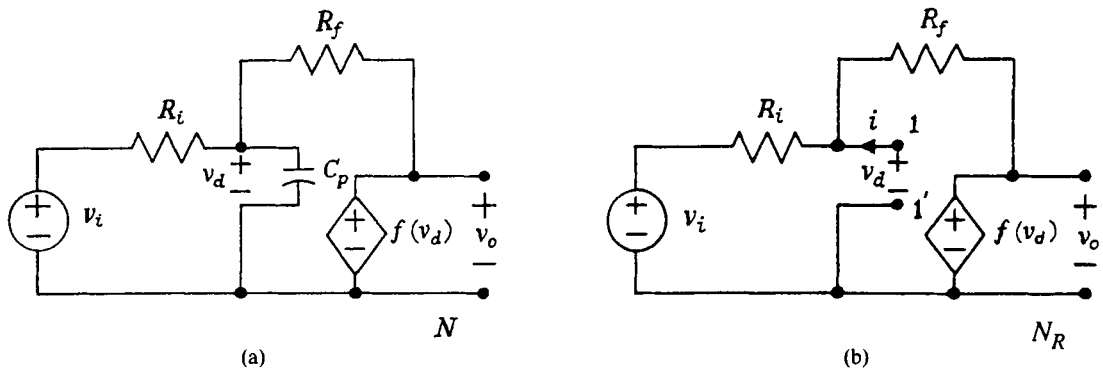


Figure 20. (a) Equivalent circuit model N for Figure 19, showing the input voltage v_i as a voltage source. (b) Resistive subnetwork N_R formed by extracting the energy storage elements (just the single capacitor C_p) from N

Substituting for v_o in the state equation gives

$$C_p \frac{dv_d}{dt} = G_i v_i + [G_f f(v_d) - G_f v_d - G_i v_d] = -g(v_d, v_i)$$

Let us now extract the energy storage element C_p and form the resistive subnetwork N_R shown in Figure 20(b). The driving point characteristic of this network (from the point of the capacitor C_p) can be obtained by applying an ideal voltage source across its terminals 1–1′ and determining the current which flows. The DP plot (which is described by equations (1)–(3) from Section 3.2) is shown in Figure 21. Note that the curve is parametrized by v_i, the effect of which is to shift the characteristic up or down by an amount equal to $-G_i v_i$.

We have seen in Section 2 that the DP plot of a network is the v–i characteristic of the equivalent resistor connected across the driving point terminals. Thus N_R can be replaced by a single non-linear resistor described by $i_R = g(v_R, v_i)$. When v_i is fixed, we can drop the dependence on v_i and write $i_R = g(v_R)$.

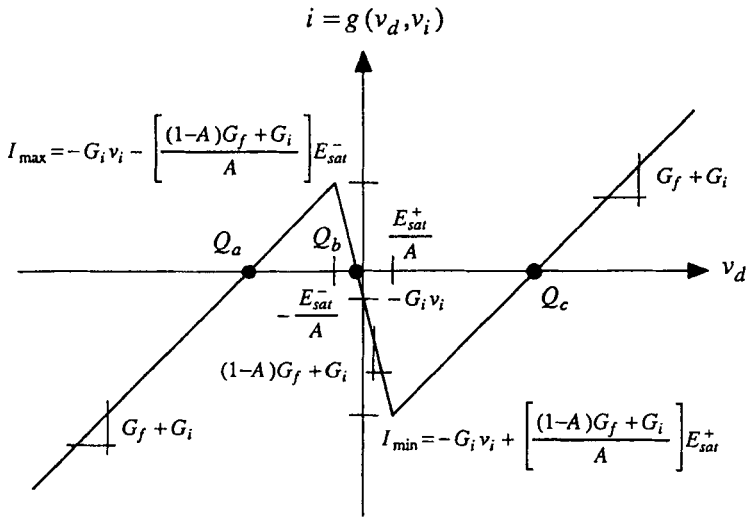


Figure 21. Driving point characteristic at terminals 1–1′ of N_R in Figure 20(b) assuming the finite gain PWL op amp model.[12] The port exhibits negative resistance when the op amp is operating in its linear region

Equilibrium points. The network N is now equivalent to the first-order RC circuit shown in Figure 22, whose equilibrium points (Q_a, Q_b and Q_c in Figure 21) are defined by $g(v_R) = 0$. Note that $v_d = v_R$ and that $i = i_R$. The function $g(\cdot)$ has a local minimum at

$$I_{min} = -G_i v_i + \frac{(1-A)G_f + G_i}{A} E_{sat}^+$$

and a local maximum defined by

$$I_{max} = -G_i v_i - \frac{(1-A)G_f + G_i}{A} E_{sat}^-$$

The number of equilibrium points depends on the signs of I_{min} and I_{max}: one if $I_{min} > 0$ or $I_{max} < 0$; two if $I_{min} = 0$ or $I_{max} = 0$; and three if $I_{min} < 0$ and $I_{max} > 0$.

There is an equilibrium point Q_b for which the op amp is in its linear region of operation only if

$$-\frac{E_{sat}^-}{A} \leqslant v_d \leqslant \frac{E_{sat}^+}{A}$$

Equivalently,

$$\frac{(1-A)G_f + G_i}{AG_i} E_{sat}^+ \leqslant v_i \leqslant -\frac{(1-A)G_f + G_i}{AG_i} E_{sat}^-$$

Otherwise, the op amp is in saturation at equilibrium.

Stability. We can determine the stability of the equilibrium points by considering the linearization of the state equation in each of the three regions of operation of the op amp.

We have that

$$C_p \frac{dv_d}{dt} = G_i v_i + [G_f f(v_d) - G_f v_d - G_i v_d]$$

Linearizing about an equilibrium point v_{d_Q}, we obtain

$$C_p \frac{dv_d}{dt} = [G_f(f'(v_{d_Q}) - 1) - G_i] v_d$$

When $v_{d_Q} > E_{sat}^+/A$ or $v_{d_Q} < -E_{sat}^-/A$ (corresponding to saturation), $f'(\cdot) = 0$; in the linear region $f'(\cdot) = A$. Thus equilibrium points Q_a and Q_c in the saturated regions are stable for all positive resistors R_i and R_f. On the other hand, an equilibrium point Q_b in the linear region is almost always unstable† since we have assumed $A \gg 1$. Therefore noise in the circuit will prevent us from observing an equilibrium point in the linear region. Hence the output of the Schmitt trigger is only ever observed in the saturated region. This is why we could not see the central portion of the TC when we tried to measure it in Section 3.1. Let us now see how switching occurs.

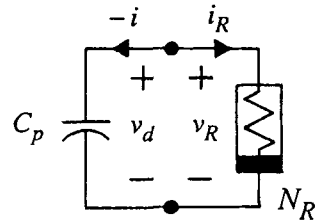


Figure 22. Reduced equivalent circuit for N of Figure 19. N_R has been replaced by a single non-linear resistor with driving point characteristic $i_R = g(v_R)$ given by Figure 21. Note that $v_d = v_R$ and that $i = i_R$

† Q_b is stable only if $G_f(A - 1) < G_i$.

The jump mechanism. The state equation for our *RC* equivalent circuit for N is $C_p\, dv_d/dt = -i$. This implies that v_d decreases when $i > 0$ and v_d increases when $i < 0$. We denote this graphically by marking the driving point characteristic with arrows to indicate the dynamic route (Figure 23(a)).[11,12]

Let us assume initially that the Schmitt trigger is in negative saturation, with a stable equilibrium point Q_a. Of the other two equilibrium points, point Q_b (corresponding to the linear regime) is unstable while Q_c is stable. As v_i is increased slowly,† the driving point characteristic $g(v_d, v_i)$ slides downwards (Q_a

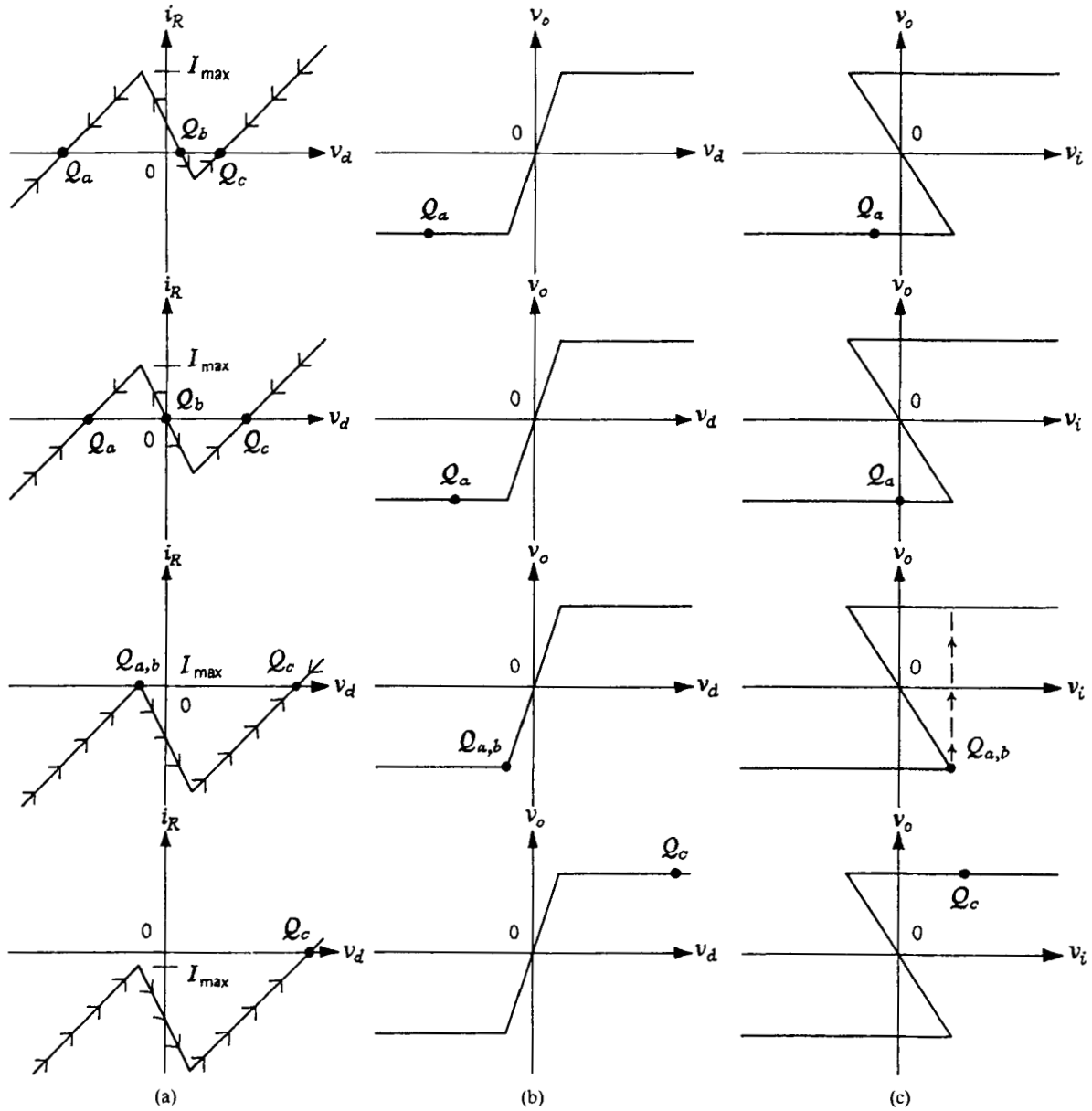


Figure 23. The jump mechanism. Column (a) shows how the DP characteristic of Figure 21 moves downwards as v_i is increased. The stable operating point Q_a eventually collides with the unstable one Q_b at $I_{max} = 0$, where the two coalesce and disappear, leaving just one stable equilibrium Q_c when $I_{max} < 0$, to which all initial conditions converge. Columns (b) and (c) show the corresponding behaviour of the $v_d - v_o$ and $v_i - v_o$ transfer characteristics. Note that only the $v_i - v_o$ TC exhibits a 'jump'

† We are assuming that v_i is varying much slower than the dynamics on the dynamic route. This is a quasi-static condition which enables us to assume that v_i is always fixed and thereby to drop the v_i-dependence of $g(\cdot,\cdot)$.

moves to the right, Q_b moves left) until $I_{max} = 0$ (Figure 23(a)), where Q_a and Q_b coalesce. This is the threshold for switching. For this value of input there are just two equilibrium points: $Q_{a,b}$ is one-sided stable; Q_c is asymptotically stable (and corresponds to positive saturation).

When v_i is increased beyond this value, the equilibrium points at Q_a and Q_b disappear, leaving just one stable equilibrium point (Q_c) to which all initial conditions will settle. In the course of switching, the capacitor voltage trajectory follows the dynamic route along the driving point characteristic from $Q_{a,b}$ through the linear region until it reaches equilibrium at Q_c. It must follow this route since the driving point characteristic is the set of all possible solutions. Correspondingly, the output voltage ($v_o = f(v_d)$) moves smoothly from negative saturation through the linear region to positive saturation (Figure 23(b)). On the transfer characteristic alone does the transition between saturation states appear as a jump (Figure 23(c)). The time constant associated with switching is very small since the linear region has a negligible resistance (approximately equal to $1/AG_f$, and $A \gg 1$); this is why switching between saturated states is so fast.

In summary, we have seen that the TC of a Schmitt trigger is neither discontinuous nor does it consist of a loop. The discontinuities which arise when one tries to measure the transfer characteristic of the circuit are due to the instability of the central portion, which in turn is caused by unmodelled parasitic dynamics. The mechanism for switching between states can be explained by including at least one parasitic energy storage element in the model.

4. HYSTERESIS DRIVING-POINT CHARACTERISTICS

4.1. Hysteresis resistors

The second class of circuits which we examine are those which exhibit hysteresis in their driving point characteristics; such circuits have been called 'hysteresis resistors'.[2] Their hysteretic behaviour manifests itself in a manner similar to transfer characteristic hysteresis. When the driving voltage applied to a current-controlled hysteresis resistor is increased beyond a threshold V_H, there is a sudden and rapid jump in current. The driving voltage must reduced below a lower threshold V_L before the current switches back to its original value. The difference between V_H and V_L is called the hysteresis voltage V_{HYST}. Because the current experiences jumps, this type of hysteresis resistor has been labelled 'jump-along-i'.[2] The dual element is a 'jump-along-v' hysteresis resistor which has associated with it a hysteresis current I_{HYST}.

Just like transfer hysteresis elements, the DP characteristic of hysteresis resistors are variously denoted by disconnected curves or loops with open- or short-circuit-like segments, dots and arrows (see Figure 1(a)).

One might suspect, having seen the mechanism which produces TC hysteresis, that DP hysteresis occurs in a similar manner. We shall see that this is indeed the case, that 'hysteresis resistance' is due to negative resistance and unmodelled parasitic dynamics.

Hysteresis oscillators. Many oscillator circuits which are commonly used in digital systems depend for their operation on the hysteretic driving point characteristic of a resistor.[2,3] These oscillators appear throughout the literature under various classifications: as multivibrators,[11,15] first-order 'hysteresis resistor' oscillators[2] and neural-type pulse oscillators.[4]

Such circuits have traditionally found applications in pulse and digital systems. More recently, they are being used in neural-type microsystems,[4] circuits which perform computation and signal processing by mimicking the pulse-handling capabilities of biological neural systems.[21] Several authors have stressed the importance of 'hysteresis' in the generation of neural-type pulses and in biological membrane oscillations.[2,10]

The operation of this class of first-order hysteretic oscillator circuits is readily understood in terms of non-linear resistors. Although we shall concentrate in this section on a particular 'hysteresis oscillator'[22] which is of interest in neural-type microsystems, the principles and method which we apply can be used to analyse any other oscillator in this class. We shall show that a thorough understanding of the

underlying mechanism of 'hysteresis' resistance simplifies both the analysis and design of 'hysteretic' oscillators.

4.2. Hysteretic neural-type pulse oscillator

Figure 24 shows the 'hysteretic neural-type pulse oscillator' of Kiruthi *et al.*[10] (later implemented in modified form by Linares-Barranco *et al.*[23]), which consists of an integrating amplifier fed by an independent input voltage u, with a linear resistor R_v and a 'hysteresis' element H (the op amp Schmitt trigger analysed in Section 3) in the feedback loop. With the input voltage u fixed 'within the design range of the circuit'[10] the neural-type pulse oscillator produces a periodic output. The independent input voltage u can be used to control the 'firing rate' (oscillation frequency) of the neuron. $H(\cdot)$ is the binary-valued relation between the input and output voltages of the 'hysteresis' element and is described by

$$H(v) = \begin{cases} H_+ & v > V_+ \\ \{H_+, -H_-\}, & -V_- < v < V_+ \\ -H_-, & -V_- > v \end{cases}$$

where $\{H_+, -H_-\}$ is the two-element set comprised of H_+ and $-H_-$. The relation is shown graphically in Figure 25.

In Reference 10 it has been shown that the circuit operates as a neural-type pulse oscillator when the following constraints are met:

$$-H_- < -\frac{G_v}{G_H}\frac{G_f}{G_i}H_- - \frac{G_u}{G_H}u < \frac{G_v}{G_H}\frac{G_f}{G_i}H_+ - \frac{G_u}{G_H}u < H_+$$

with $G_v = 1/R_v$, $G_H = 1/R_H$, $G_f = 1/R_f$ and $G_i = 1/R_i$.

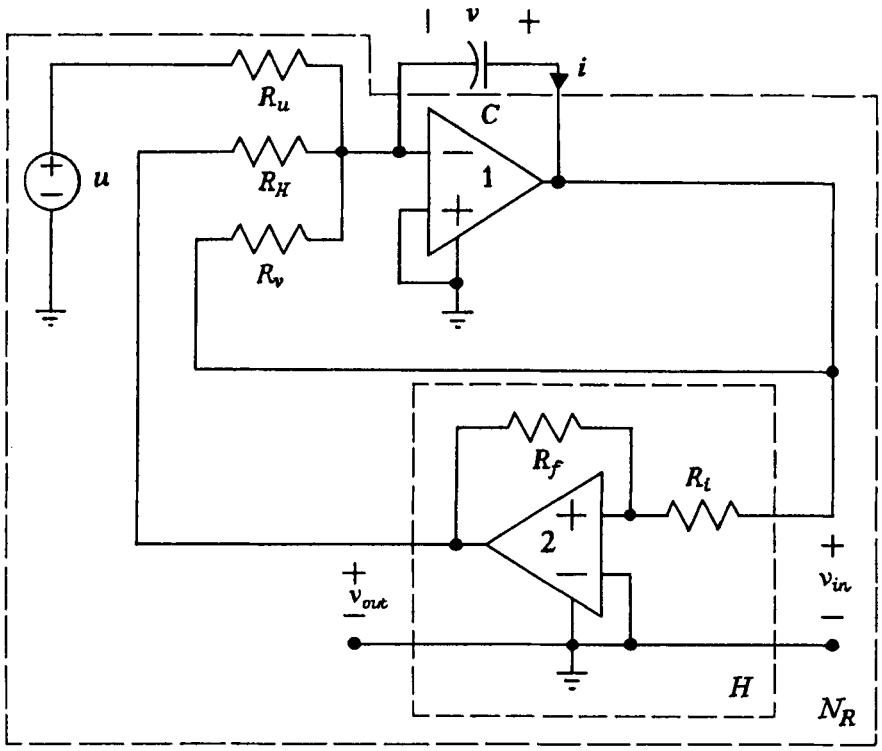


Figure 24. Hysteretic neural-type pulse oscillator (from Reference 10) showing the 'hysteresis' element H at the bottom. We group the resistive elements into a single non-linear resistive one-port N_R, across which is connected the capacitor C

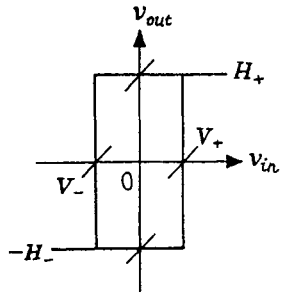


Figure 25. Suggested TC of the 'hysteresis' element H in Figure 24 (from Reference 10)

The authors have shown that the period of oscillation is 'of the order of R_vC', where R_v and C are as shown in Figure 24. Because of 'hysteresis', it was not possible to obtain a more accurate estimate of the oscillation frequency. Because of 'hysteresis' too, it was not possible to write state equations for the circuit; only semi-state equations[24] could be derived. We shall show that by using non-linear circuit theory, one can calculate exactly the frequency of oscillation of first-order PWL RC oscillators of this type.

Exact analysis: conditions for oscillation. Let us assume that the op amps in Figure 24 are modelled by the finite gain op amp model.[12] For maximum accuracy in our derivation we use the finite gain model. Later we will see that the error caused by assuming infinite gain is negligible.

We can determine the driving point characteristic at the terminals of the capacitor by using standard piecewise-linear circuit analysis.[12] As before, we apply an ideal voltage source at the port and measure the current which flows when the op amps are replaced in turn by their negative saturation, linear and positive saturation models. The validating equations then determine the boundaries of the piecewise-linear regions in the v–i plane (see Appendix I for the complete analysis).

The resulting DC resistive driving point characteristic seen at the terminals of the capacitor is shown in Figure 26. At this point we can replace the resistive part N_R of the op amp circuit by a single two-terminal resistor with the same driving point characteristic ($v = h(i, u)$) as far as the capacitor is concerned. Note that u does not affect the shape of the driving point characteristic; its only effect is to displace the characteristic vertically. The equivalent circuit for the entire network is now just the capacitor C and, attached to it, a non-linear resistor R described by $v = h(i, u)$ (shown in Figure 27).

From non-linear circuit theory[12] we know that this circuit will oscillate if the piecewise-linear driving point characteristic (see Figure 43) exhibits negative resistance and if the equilibrium point lies in the negative resistance region. For comparison with References 10 and 22 we let $A \to \infty$, set $E^+_{sat2} = E^+_{sat1} = E^+_{sat}$ and set $E^-_{sat2} = E^-_{sat1} = E^-_{sat}$. This yields the following three conditions for oscillation:

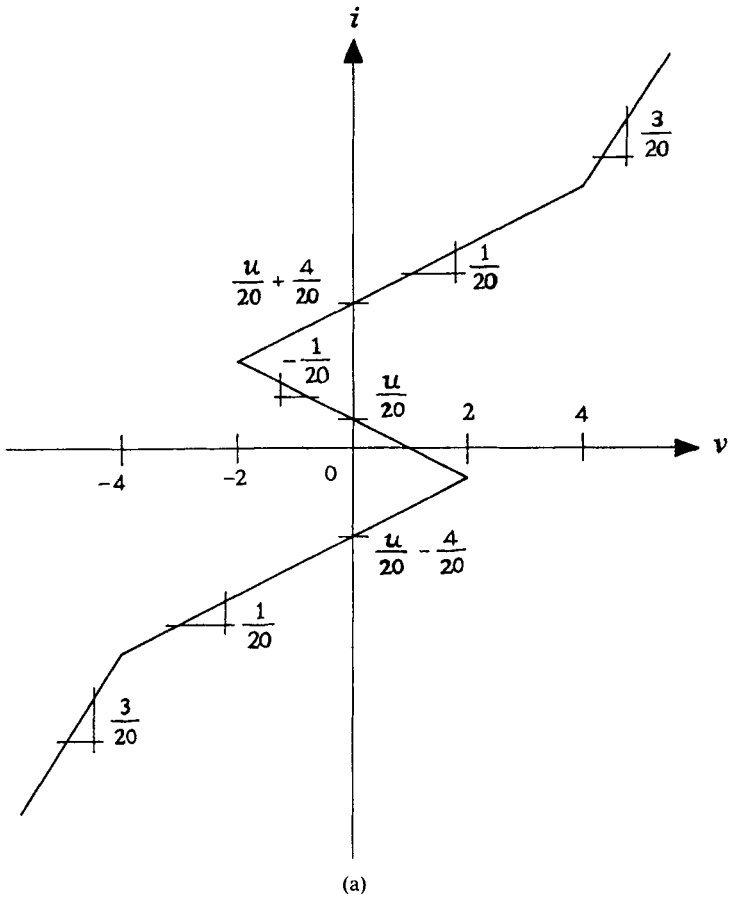
$$G_H E^+_{sat} + G_u u > -G_H E^-_{sat} + G_u u$$

$$G_H E^+_{sat} + G_u u - \frac{G_f G_v}{G_i} E^+_{sat} > 0$$

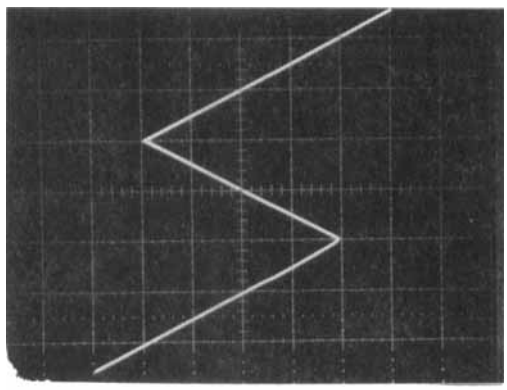
$$-G_H E^-_{sat} + G_u u + \frac{G_f G_v}{G_i} E^-_{sat} < 0$$

If we identify E^+_{sat} with H_+ and E^-_{sat} with H_-, we see that these conditions are exactly equivalent to those derived in Reference 10 but have been determined from graphical considerations of a simple first-order piecewise-linear RC network. Note that we have made no reference to 'hysteresis'.

Exact analysis of the capacitor voltage wave-form. This analysis uses the circuit theoretic concepts of the dynamic route and jump rule.[12] We assume that the input voltage u to the oscillator is held at some fixed value. Although parametrized by u, once the independent voltage source is fixed, the driving point



(a)



(b)

Figure 26. Driving point characteristics of N_R at the terminals of the capacitor C in the hysteretic neural-type pulse oscillator. The independent voltage source u sets the vertical bias of the characteristic. (a) PWL model with $A \to \infty$ (derived in Appendix I). (b) Experimentally measured from the circuit of Figure 24

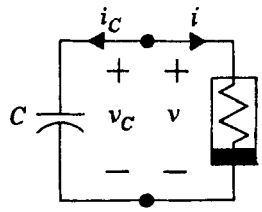


Figure 27. Equivalent circuit for the hysteretic neural-type pulse oscillator in Figure 24 with fixed input u. The DP characteristic of the non-linear resistor is shown in Figure 26

characteristic of the equivalent non-linear resistor is fixed, so we can write $v = h(i)$. Applying KCL and KVL to the equivalent circuit (Figure 27), we find that $i_c = C\,\mathrm{d}v_c/\mathrm{d}t$, $v_c = v$ and $i_c = -i$. Hence

$$i = -C\frac{\mathrm{d}v}{\mathrm{d}t}$$

Thus v decreases while i is positive, and when i is negative, v increases. As before, we draw arrows on the DP characteristic to illustrate the direction of travel of trajectories (see Figure 28). Consider an initial condition at point 'a'. Since i is positive, v decreases along the characteristic in the direction of the arrows, aiming for the virtual equilibrium point 'c' (where $\mathrm{d}v/\mathrm{d}t = 0$). After some finite time the voltage reaches point 'b'. This is not an equilibrium condition, since i is non-zero. From here the voltage cannot further decrease while staying on the DP characteristic of the resistor. This is known as an impasse point[12,25,26] and results from using an incomplete model of the circuit. What happens in practice is that the current jumps instantaneously to another point on the characteristic, without changing v, since the voltage on a capacitor cannot change discontinuously. Thus the trajectory jumps to point 'd'. Now i is negative, so v begins to increase once again along the direction of the arrows, this time aiming for the virtual equilibrium point 'f'. Before it gets to 'f', though, it reaches the impasse point 'e' and jumps back to the upper branch of the characteristic at 'a', from where it begins to head back towards 'c' once more. It should be clear that this is an oscillatory condition, with the operating point circulating repeatedly around the loop 'abde'.

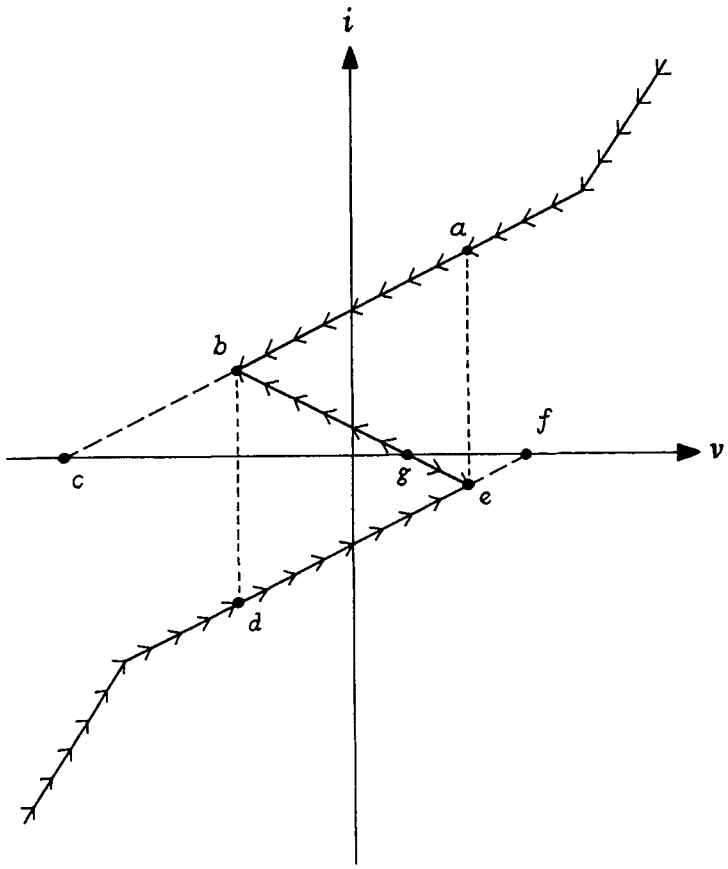


Figure 28. Dynamic route of the oscillator for fixed u. The operating point follows the counterclockwise path 'abde'; it moves smoothly from 'a' to 'b' and from 'd' to 'e', but jumps between 'b' and 'd' and from 'e' back to 'a'

Frequency of oscillation. If we assume that the jumps between segments of the characteristic are instantaneous, then the period (and shape) of the capacitor voltage and current wave-forms can be calculated with ease. The period consists of the time taken for the voltage to decrease from 'a' to 'b' and the time to increase from 'd' to 'e'. These are piecewise-linear segments, each with a known resistance R and hence time constant $\tau = RC$.

The time to go from 'a' to 'b' (assuming that the op amps have infinite gain in their linear regions) is given by[12]

$$t_b - t_a = \tau \ln\left(\frac{v_a - v_c}{v_b - v_c}\right)$$

where $v_c = -(G_H E_{sat}^+ + G_u u)/G_v$, $v_a = (G_f/G_i)E_{sat}^-$, $v_b = -(G_f/G_i)E_{sat}^+$ and $\tau = C/G_v$. Thus

$$t_b - t_a = \frac{C}{G_v} \ln\left(\frac{(G_v G_f/G_i)E_{sat}^- + G_H E_{sat}^+ + G_u u}{-(G_v G_f/G_i)\ E_{sat}^+ + G_H E_{sat}^+ + G_u u}\right)$$

Similarly, the time taken to go from 'd' to 'e' is given by

$$t_e - t_d = \tau \ln\left(\frac{v_d - v_f}{v_e - v_f}\right)$$

where $v_f = (G_H E_{sat}^- - G_u u)/G_v$, $v_e = (G_f/G_i)E_{sat}^-$, $v_d = -(G_f/G_i)E_{sat}^+$ and $\tau = C/G_v$. Thus

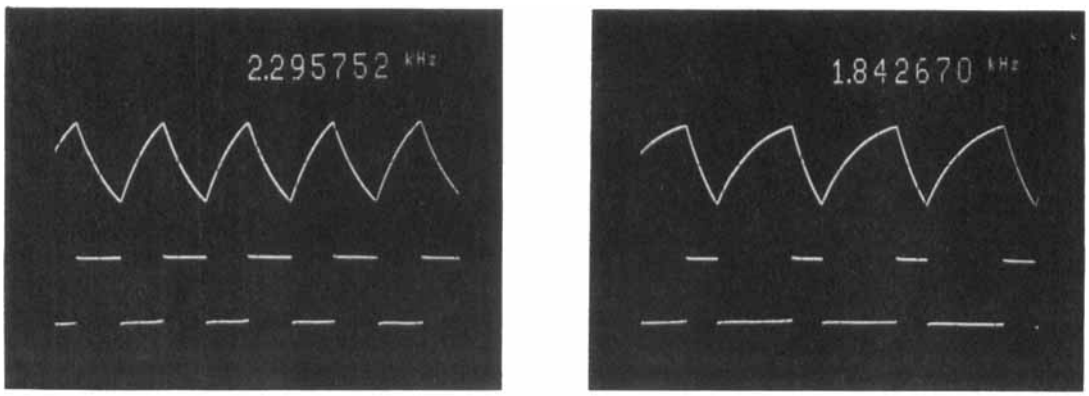
$$t_e - t_d = \frac{C}{G_v} \ln\left(\frac{-(G_v G_f/G_i)E_{sat}^+ - G_H E_{sat}^- + G_u u}{(G_v G_f/G_i)E_{sat}^- - G_H E_{sat}^- + G_u u}\right)$$

The period of oscillation, T, is simply the sum of these two times:

$$T = \frac{C}{G_v} \ln\left[\left(\frac{(G_v G_f/G_i)E_{sat}^- + G_H E_{sat}^+ + G_u u}{-(G_v G_f/G_i)E_{sat}^+ + G_H E_{sat}^- + G_u u}\right)\left(\frac{-(G_v G_f/G_i)E_{sat}^+ - G_H E_{sat}^- + G_u u}{(G_v G_f/G_i)E_{sat}^- - G_H E_{sat}^+ + G_u u}\right)\right]$$

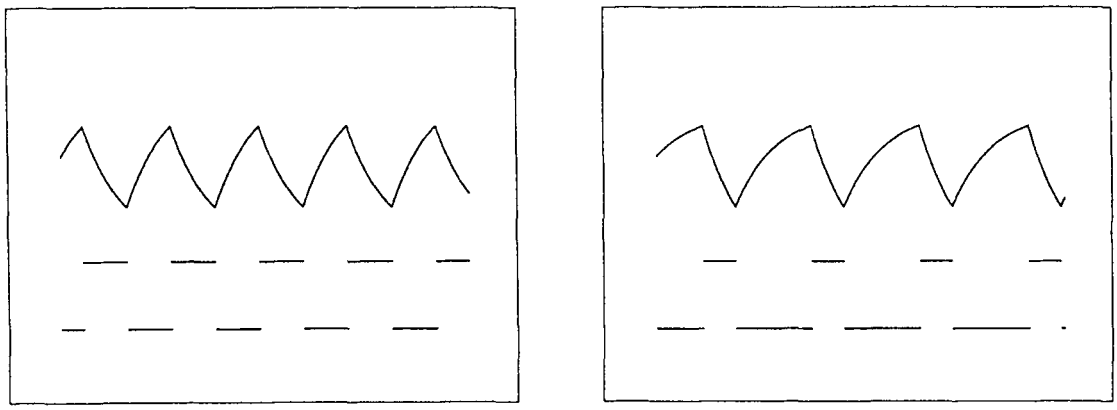
Example. We built the negative resistance neural-type pulse oscillator shown in Figure 24 using the following parameter values: $E_{sat}^+ = E_{sat}^- = 4$ V, $R_f = R_H = R_v = R_u = 20$ kΩ, $R_i = 10$ kΩ and $C = 0{\cdot}01$ μF. The op amp was a TL074[27] with $V_{CC} = 4{\cdot}75$ V and $V_{EE} = -5{\cdot}28$ V. Note that op amp 1 (in Figure 24) remains in the linear region of operation throughout since $v \in [-(G_f/G_i)E_{sat}^-, (G_f/G_i)E_{sat}^+]$; this means that its inverting terminal is indeed a virtual ground. Hence the output of that amplifier is approximately equal to the capacitor voltage; this enables us to measure v directly at the output of op amp 1.

For these component values and with $u = 0$ our analysis predicts an oscillation frequency of 2·275 kHz. Figure 29(a) shows the experimentally measured waveform v with frequency 2·29 kHz. With $u = 1{\cdot}3$ V



(a) (b)

Figure 29. Experimental wave-forms for the neural-type pulse oscillator in Figure 24: the upper wave-form is $v_{in} (\approx v)$; v_{out} is below; (a) $u = 0$; (b) $u = 1{\cdot}3$ V



(a) (b)

Figure 30. Simulated wave-forms for the neural-type pulse oscillator assuming instantaneous jumps 'b' → 'd' and 'e' → 'a': (*a*) $u = 0$; (b) $u = 1{\cdot}3$ V

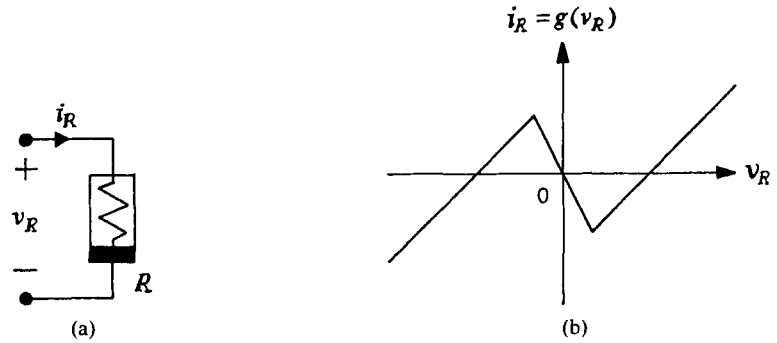
the predicted oscillation frequency is 1·85 kHz; we measured 1·84 kHz (see Figure 29(b)). For comparison we show the wave-forms generated by computer simulation assuming instantaneous jumps (Figures 30(a) and 30(b)).

4.3. Hysteresis resistance: how it occurs

We have seen that the driving point characteristic of a network N_R is the locus of solutions of the equivalent two-terminal resistor connected at the driving point terminals in place of the entire network. This locus consists of all valid voltage and current pairs for the equivalent resistor.

Consider the voltage-controlled resistor R (Figure 31(a)) whose driving point characteristic $i_R = g(v_R)$ is shown in Figure 31(b)). Let us see what happens when we try to measure this curve by placing a current source across the terminals of the resistor (Figure 32(a)). Initially we apply a large negative value of current ($I_s = i_a$) for which there is a unique voltage v_a. This gives us an operating point Q_a on the driving-point characteristic. Now increase I_s smoothly to i_b; the voltage increases smoothly to v_b as the operating point traces out the left segment of the DP characteristic (Figure 32(b)).

If we now increase I_s beyond i_b, the corresponding value of the terminal voltage can only lie on the right segment of the characteristic. Thus, as we move I_s through i_b to i_c, the voltage jumps abruptly from v_b to $v_{b'}$, then continues to increase smoothly to v_c. Decreasing I_s back to i_a enables us to trace out the right segment as far as point Q_d, where v_d jumps abruptly to $v_{d'}$, and we trace out the left segment once more.



(a) (b)

Figure 31. A non-monotone voltage-controlled resistor R with branch voltage v_R and current i_R and (b) its voltage-controlled DP characteristic $i_R = g(v_R)$

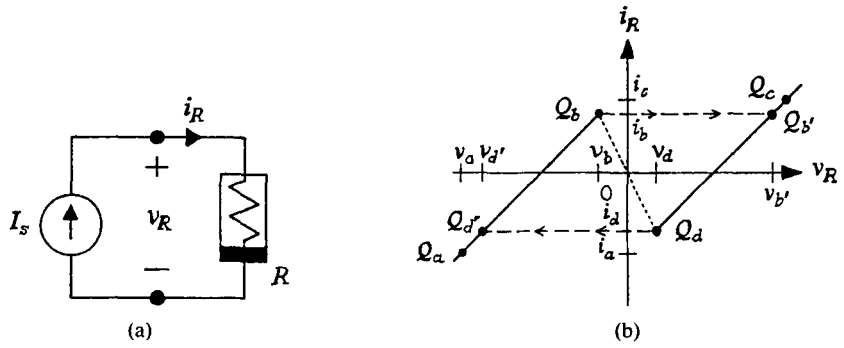


Figure 32. (a) Measuring the DP characteristic by driving R with a current source I_s. (b) DP characteristic, with current forcing, exhibits 'hysteresis'. Increasing I_s from i_a to i_c and decreasing it to i_a once more enables us to trace out just the left and right segments of the three-segment DP characteristic

In this way a non-monotone voltage-controlled resistor[11] can exhibit a 'loop' or discontinuity in its driving point characteristic with jumps in voltage. Such behaviour has prompted the unfortunate classification 'jump-along-v hysteresis resistor'.[2] This 'hysteresis' arises only if we try to measure the DP characteristic of a non-monotone voltage-controlled resistor by forcing with a current source. If we drive with a voltage source, we obtain a continuous curve, since to each value of v corresponds a unique value of i. 'Hysteresis' in the DP characteristic is simply an artifact of the measurement technique. By a similar reasoning it should be clear that driving a non-monotone current controlled resistor with a voltage source produces a 'jump-along-i hysteresis resistor'.[2]

The jump phenomenon. Let us examine the voltage jumps in our test resistor R more carefully. As we increased the current smoothly through i_b, the voltage jumped from v_b to $v_{b'}$ while i remained constant. If the voltage went from v_b to $v_{b'}$ without changing i, then it could not have gone along the DP characteristic (Figure 32(b)) but must have traversed the line segment Q_b–$Q_{b'}$. This path is disallowed because the DP characteristic is the set of all valid terminal voltage and current pairs. So how did v get from v_b to $v_{b'}$?

The answer lies in the fact that our resistor model is incomplete. Whenever we have a non-monotone voltage-controlled resistor, we must add a small parasitic capacitor in parallel with it.[11,20] By duality, a model of a non-monotone current-controlled resistor is incomplete unless it includes a series parasitic inductance.

Let us add the necessary parasitic capacitor and once more examine the voltage-controlled resistor R when driven by a current source. The equivalent circuit is shown in Figure 33. Now the resistor and current source can be combined to form a single voltage-controlled non-linear resistor N_R (Figure 34(a)) whose DP characteristic (shown in Figure 34(b)) is described by

$$i'_R = g(v_R) - I_s = g'(v_R)$$

Note that the effect of I_s is simply to shift the characteristic $g(v_R)$ vertically without affecting its shape (compare Figures 31(b) and 34(b)). The 'jump' mechanism is now exactly as we saw for the Schmitt trigger

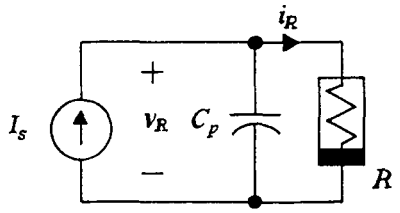


Figure 33. The complete circuit model for Figure 32 includes a parasitic capacitor C_p[11]

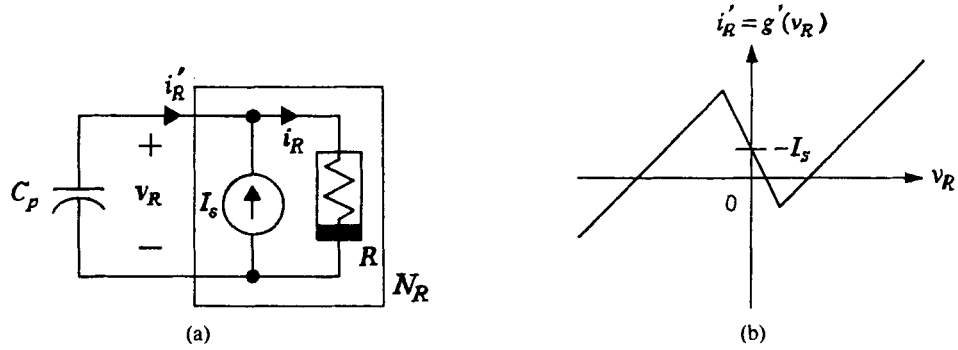


Figure 34. (a) The network of Figure 33 is partitioned into resistive and energy storage subnetworks. The resistive elements are lumped together to form the resistive subnetwork N_R. (b) DP characteristic of N_R for a negative value of I_s

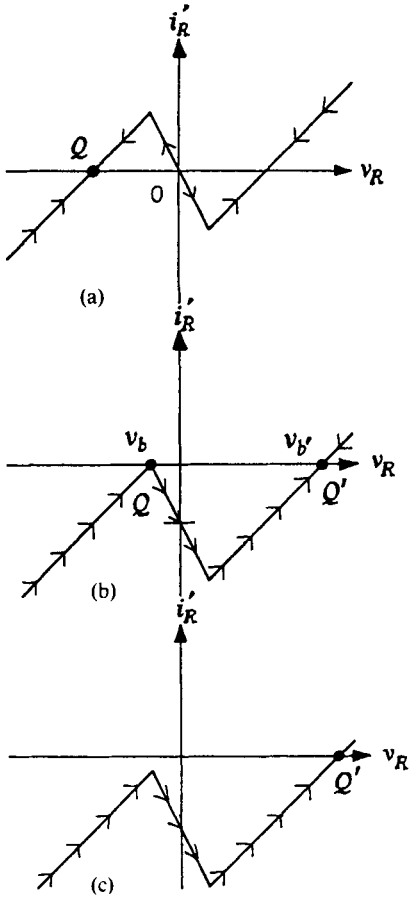


Figure 35. (a) Dynamic route and equilibrium point at Q. (b) As I_s is increased, the characteristic slides downwards until the equilibrium point Q on the left branch becomes unstable at $I_s = i_b$ (where $v_R = v_b$) and the operating point moves to Q′ on the right branch of the DP characteristic. (c) Increasing I_s further causes all initial conditions to converge to the single equilibrium point Q′ on the right branch of the characteristic

circuit. The dynamic route is illustrated in Figure 35(a). As I_s is slowly increased through i_b from below, the equilibrium (operating) point on the left segment of the characteristic becomes unstable at v_b (see Figure 35(b)). The operating point then follows the dynamic route along the DP characteristic to the new stable equilibrium at $v_{b'}$ (see Figure 35(c)). While the voltage is 'jumping', the difference in current between the operating point on the DP characteristic $g'(v_R)$ and i_b is supplied by the capacitor C_p. A dual argument follows for a current-controlled resistor driven by a voltage source.

We are now in a position to derive a complete model for the neural-type pulse oscillator.[10]

State equations. Our original description of the neural-type pulse oscillator circuit was in terms of a capacitor in parallel with a current-controlled resistor. This produced impasse points[25,26] and the jump phenomenon. As a result we could not write state equations to describe the oscillator but were tied to a cumbersome semi-state description. Having seen how the jump phenomenon arises, we can now model it correctly by adding the required parasitic inductance L_p in series with the current-controlled non-linear resistor. The addition of this inductance permits us to write state equations for the circuit in order to analyse it exactly.

The second-order circuit model is shown in Figure 36. Now the state equations for the network are

$$C\frac{dv_C}{dt} = -i_L, \qquad L_p\frac{di_L}{dt} = v_C - h(i_L, u)$$

where $h(i, u)$ is the piecewise-linear function describing the current-controlled negative resistor (see Figure 43 and Appendix I).

The introduction of a small parasitic energy storage element in order to write state equations typically adds a fast new time scale to the circuit which in turn makes the system stiff. Correspondingly, in simulating the network, one must use an implicit integration algorithm (see e.g. Reference 28).

4.4. Unifying the lot

We have seen how an understanding of the jump mechanism which produces hysteretic-type behaviour in driving point and transfer characteristics simplifies the analysis of those circuits which exploit it. This knowledge can also simplify the process of synthesis.

We have identified the neural-type pulse oscillator as a first-order *RC* relaxation oscillator. It was produced by connecting a linear capacitor to a five-segment current-controlled negative resistor, of which only three segments are necessary for oscillation. We can achieve the same functionality with a three-segment characteristic; this requires just one op amp instead of two.[29] In the original circuit, frequency control was effected by applying a DC bias voltage to displace the DP characteristic vertically without changing its shape. In an *ad hoc* manner we can reproduce this behaviour by synthesizing the required DP characteristic with an S-type negative resistance converter in parallel with a current source and then placing a capacitor across its terminals.

Consider the circuit shown in Figure 37 and analysed in Appendix II. It is instructive to study this simple oscillator closely in order to see the connection between transfer and driving point 'hysteresis'.

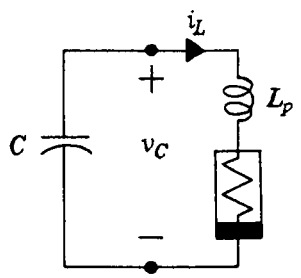


Figure 36. Complete second-order circuit model for the neural-type pulse oscillator of Figure 24. L_p is the parasitic inductance associated with the current-controlled non-linear resistor $v = h(i, u)$

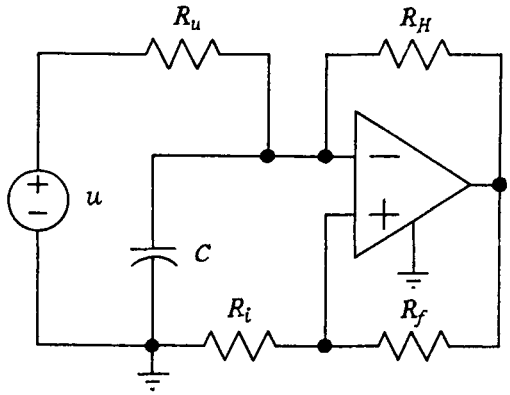


Figure 37. Neural-type pulse oscillator, which is functionally equivalent to that in Figure 24

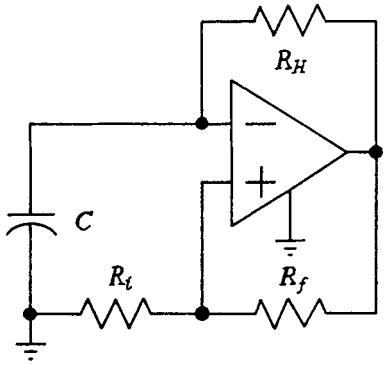


Figure 38. Astable multivibrator obtained by removing the independent voltage source u and resistor R_u from the circuit in Figure 37

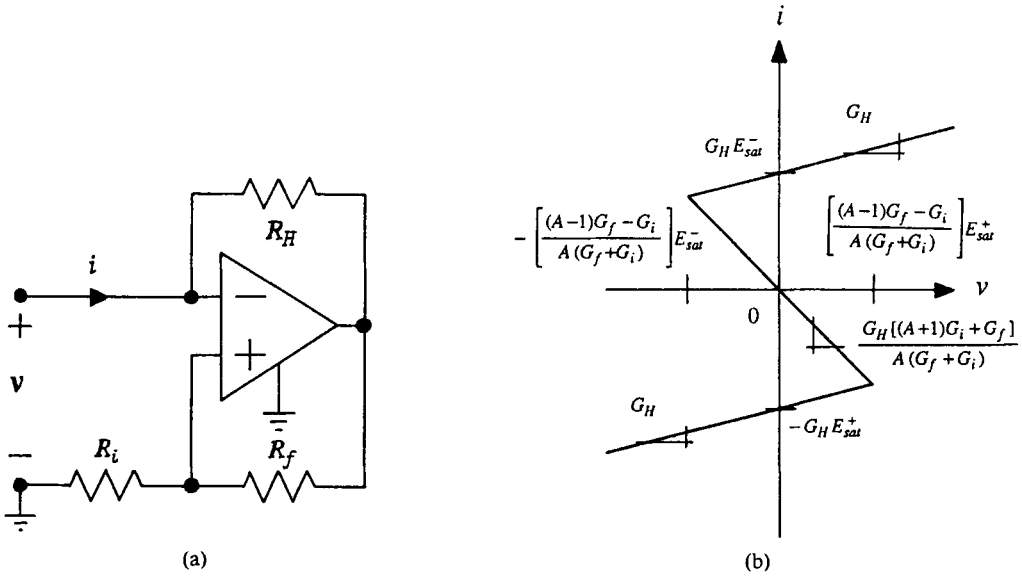


Figure 39. (a) Negative resistance converter obtained by removing the capacitor from Figure 38, and (b) its DP characteristic. See Appendix II for the details of constructing this DP characteristic

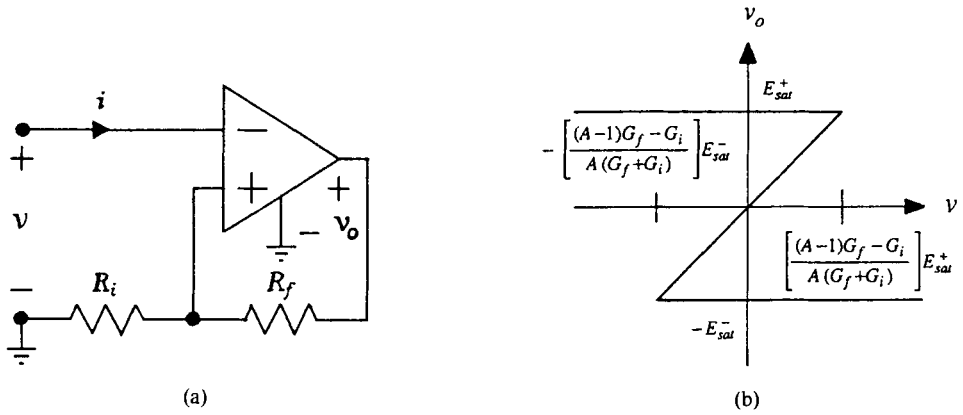


Figure 40. (a) Inverting op amp Schmitt trigger formed by disconnecting the feedback resistor R_H in Figure 38, and (b) its input–output voltage transfer characteristic. See Appendix II for the derivation

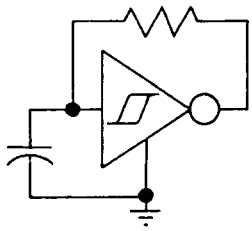


Figure 41. CMOS Schmitt trigger oscillator (from Reference 8)

With the appropriate choice of component values this circuit is exactly equivalent in functionality to the neural-type pulse oscillator. The reader may recognize it as a 'square wave generator with voltage control of pulse width'.[30] If we remove the voltage source u and resistor R_u, what remains is the classic 'free-running symmetrical multivibrator' (Figure 38).[30,31] If we next remove the capacitor from the circuit, we get an S-type negative resistance converter (Figure 39(a)),[11] more recently called an R_H, 'hysteresis resistor'.[2] If we then take away the upper feedback resistor R_H, we obtain a Schmitt trigger once more, this time in the inverting configuration (Figure 40(a)).

We have stripped down an op amp hysteresis oscillator to find a Schmitt trigger within. It is worth noting that CMOS Schmitt trigger oscillators are constructed by reversing this process. A feedback resistor turns an inverting Schmitt trigger into a negative resistor; a capacitor then provides the dynamics to produce oscillation (see Figure 41).

5. CONCLUDING REMARKS

With every non-monotone resistor is intimately associated a parasitic capacitor or inductor. In most situations it is safe to ignore these parasitics in order to reduce the complexity of a network model. So often do we ignore them, however, that omitting parasitics has become the automatic first step in simplifying a model. This leads us to forget how important a role they can play.

A case in point is 'hysteresis' in driving point and transfer characteristics, where it is common practice to use a purely resistive model to try to explain the jumps which one observes in an experiment. The fundamental problem here is that driving point and transfer characteristics are static objects; jumps, on the other hand, are dynamic phenomena. It is therefore futile to try to model the behaviour without resorting to dynamic elements. Nevertheless, we still try to do it, by adding loops, breaks, dots and arrows

to the characteristics. Not only does this lead to incorrect models, misleading intuition, cumbersome semi-state descriptions and wrong answers, but it obscures an otherwise simple mechanism.

In this work we have used elementary circuit theory to explain how parasitic dynamics manifests itself as 'hysteresis'. We have stressed the importance of understanding what is meant by driving point and transfer characteristics. We have chosen two common examples of circuits which exhibit 'hysteresis' in order to illustrate how the concepts of the dynamic route and jump rule can be used to explain experimental observations. By not ignoring critical parasitic elements, the operation of these circuits can be readily understood.

ACKNOWLEDGEMENTS

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APPENDIX I: NEURAL-TYPE PULSE OSCILLATOR (SEE FIGURE 24)

KCL (at terminals 1–1′ in Figure 42)

$$i = G_u(u + v_{d_1}) + G_v(v_{o_1} + v_{d_1}) + G_H(v_{o_2} + v_{d_1}) = G_u u + (G_H + G_u + G_v)v_{d_1} + G_v v_{o_1} + G_H v_{o_2}$$

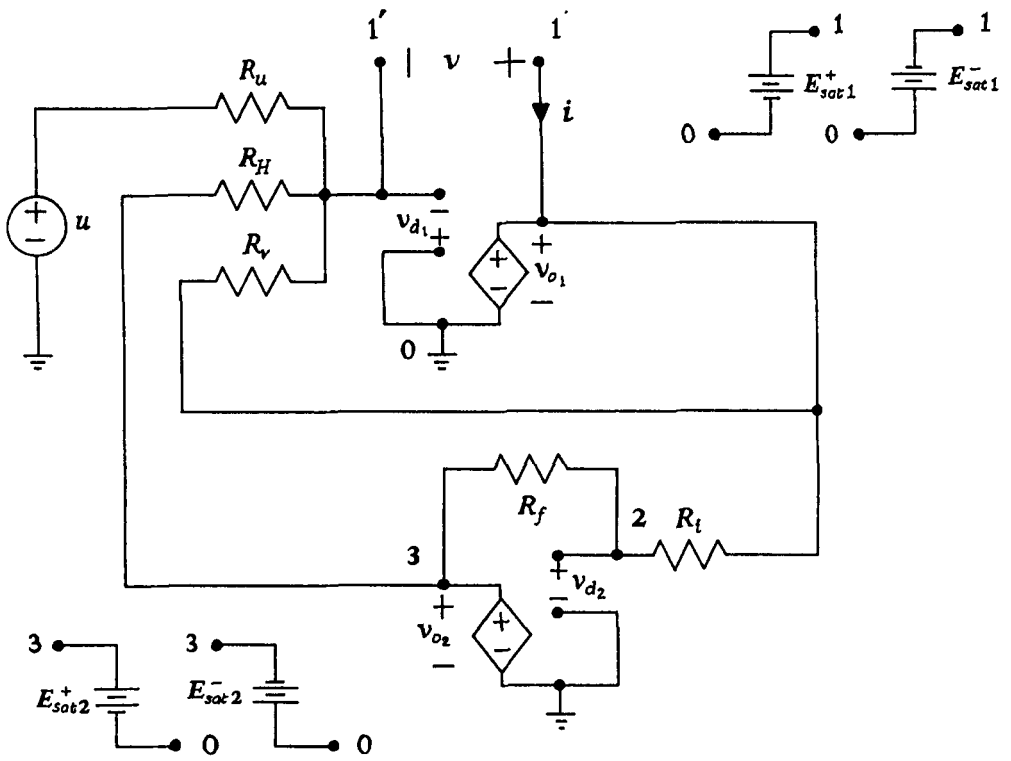

Figure 42. Equivalent circuit for the resistive part N_R of the neural-type pulse oscillator of Figure 24. In each linear region of each op amp we replace the outputs v_{o_1} and v_{o_2} by the appropriate voltage sources

KCL (at node 2 in Figure 42)

$$G_i(v_{o_1} - v_{d_0}) = G_f(v_{d_2} - v_{o_2})$$

KVL (around loop 1–0–1′ in Figure 42)

$$v = v_{d_1} + v_{o_1}$$

Finite gain op amp models (compare with Figure 10)

Op amp	− Sat	Linear	+ Sat
1	$v_{d_1} \leqslant -\dfrac{E_{sat1}^-}{A_1}$	$-\dfrac{E_{sat1}^-}{A_1} \leqslant v_{d_1} \leqslant \dfrac{E_{sat1}^+}{A_1}$	$v_{d_1} \geqslant \dfrac{E_{sat1}^+}{A_1}$
	$v_{o_1} = -E_{sat1}^-$	$v_{o_1} = A_1 v_{d_1}$	$v_{o_1} = E_{sat1}^+$
2	$v_{d_2} \leqslant -\dfrac{E_{sat2}^-}{A_2}$	$-\dfrac{E_{sat2}^-}{A_2} \leqslant v_{d_2} \leqslant \dfrac{E_{sat2}^+}{A_2}$	$v_{d_2} \geqslant \dfrac{E_{sat2}^+}{A_2}$
	$v_{o_2} = -E_{sat2}^-$	$v_{o_2} = A_2 v_{d_2}$	$v_{o_2} = E_{sat2}^+$

Op amp 1 saturated negative ($v_{o_1} = -E_{sat1}^-$)

If op amp 1 is in negative saturation, then

$$v = v_{d_1} - E_{sat1}^-$$

giving

$$v_{d_1} = v + E_{sat1}^-$$

Note that this occurs only if

$$v_{d_1} \leqslant -\frac{E_{sat1}^-}{A_1}$$

Equivalently, op amp 1 is in negative saturation when

$$v \leqslant -\frac{A_1 + 1}{A_1} E_{sat1}^-$$

For the ideal op amp model ($A_1 \to \infty$) we obtain

$$v \leqslant -E_{sat1}^-$$

Op amp 1 saturated negative and op amp 2 saturated negative. When op amps 1 and 2 are both in negative saturation, writing KCL at node 2 gives

$$G_i(-E_{sat1}^- - v_{d_2}) = G_f(v_{d_2} + E_{sat2}^-)$$

yielding

$$v_{d_2} = \frac{-G_i E_{sat1}^- - G_f E_{sat2}^-}{G_i + G_f}$$

Recall that op amp 2 is in negative saturation only if

$$v_{d_2} \leqslant -\frac{E_{sat2}^-}{A_2}$$

Hence op amps 1 and 2 can both be in negative saturation only if

$$v \leqslant -\frac{A_1+1}{A_2} E_{\text{sat1}}^- \quad \text{and} \quad \frac{-G_i E_{\text{sat1}}^- - G_f E_{\text{sat2}}^-}{G_i + G_f} \leqslant -\frac{E_{\text{sat2}}^-}{A_2}$$

For the ideal op amp models ($A_1 \to \infty$, $A_2 \to \infty$) this condition reduces to

$$v \leqslant -E_{\text{sat1}}^- \quad \text{and} \quad \frac{-G_i E_{\text{sat1}}^- - G_f E_{\text{sat2}}^-}{G_i + G_f} \leqslant 0$$

When both op amps are in negative saturation, the current i is given by

$$i = G_u u + (G_H + G_u + G_v) v_{d_1} - G_v E_{\text{sat1}}^- - G_H E_{\text{sat2}}^-$$

Substituting $v_{d_1} = v + E_{\text{sat1}}^-$, we obtain

$$i = G_u u + (G_H + G_u + G_v) v + (G_H + G_u) E_{\text{sat1}}^- - G_H E_{\text{sat2}}^-$$

Op amp 1 saturated negative and op amp 2 linear. If op amp 1 is in negative saturation and op amp 2 is linear, then KCL at node 2 gives

$$G_i(-E_{\text{sat1}}^- - v_{d_2}) = G_f(v_{d_2} - A_2 v_{d_2})$$

yielding

$$v_{d_2} = \frac{G_i E_{\text{sat1}}^-}{(A_2 - 1)G_f - G_i}$$

Now op amp 2 is in its linear region of operation only if

$$-\frac{E_{\text{sat2}}^-}{A_2} \leqslant v_{d_2} \leqslant \frac{E_{\text{sat2}}^+}{A_2}$$

Hence op amp 1 is in negative saturation and op amp 2 is linear only if

$$v \leqslant -\frac{A_1+1}{A_1} E_{\text{sat1}}^- \quad \text{and} \quad -\frac{E_{\text{sat2}}^-}{A_2} \leqslant \frac{G_i E_{\text{sat1}}^-}{(A_2 - 1)G_f - G_i} \leqslant \frac{E_{\text{sat2}}^+}{A_2}$$

For the ideal op amp model this condition reduces to the simpler form

$$v \leqslant -E_{\text{sat1}}^- \quad \text{and} \quad -E_{\text{sat2}}^- \leqslant \frac{G_i}{G_f} E_{\text{sat1}}^- \leqslant E_{\text{sat2}}^+$$

Under these conditions the current is given by

$$i = G_u u + (G_H + G_u + G_v) v_{d_1} - G_v E_{\text{sat1}}^- + A_2 G_H v_{d_2}$$

Substituting for v_{d_2}, we obtain

$$i = G_u u + (G_H + G_u + G_v) v_{d_1} - G_v E_{\text{sat1}}^- + \frac{A_2 G_H G_i}{(A_2 - 1)G_f - G_i} E_{\text{sat1}}^-$$

If we now substitute for v_{d_2}, the current is given by

$$i = G_u u + (G_H + G_u + G_v) v + (G_H + G_u) E_{\text{sat1}}^- + \frac{A_2 G_H G_i}{(A_2 - 1)G_f - G_i} E_{\text{sat1}}^-$$

For the ideal op amp model ($A_1 \to \infty$, $A_2 \to \infty$) this simplifies to

$$i = G_u u + (G_H + G_u + G_v) v + (G_H + G_u) E_{\text{sat1}}^- + \frac{G_H G_i}{G_f} E_{\text{sat1}}^-$$

Op amp 1 saturated negative and op amp 2 saturated positive. When op amp 1 is in negative saturation and op amp 2 is saturated positive, KCL at node 2 gives

$$G_i(-E_{sat1}^- - v_{d_2}) = G_f(v_{d_2} - E_{sat2}^+)$$

giving

$$v_{d_2} = \frac{-G_iE_{sat1}^- + G_fE_{sat2}^+}{G_i + G_f}$$

Now op amp 2 is in positive saturation only if

$$v_{d_2} \geqslant \frac{E_{sat}^+}{A_2}$$

Hence op amp 1 is saturated negative and op amp 2 is in positive saturation only if

$$v \leqslant -\frac{A_1 + 1}{A_1} E_{sat1}^- \quad \text{and} \quad \frac{-G_iE_{sat1}^- + G_fE_{sat2}^+}{G_i + G_f} \geqslant \frac{E_{sat}^+}{A_2}$$

For the ideal op amp model this reduces to the condition

$$v \leqslant -E_{sat1}^- \quad \text{and} \quad \frac{-G_iE_{sat1}^- + G_fE_{sat2}^+}{G_i + G_f} \geqslant 0$$

Using these conditions

$$i = G_u u + (G_H + G_u + G_v)v_{d_1} - G_vE_{sat1}^- + G_HE_{sat2}^+$$

which, after substituting for v_{d_1}, yields

$$i = G_u u + (G_H + G_u + G_v)v + (G_H + G_u)E_{sat1}^- + G_HE_{sat2}^+$$

Op amp 1 linear ($v_{o_1} = Av_{d_1}$)

If op amp 1 is in its linear region of operation, then KVL at terminals 1–1′ gives

$$v = v_{d_1} + A_1v_{d_1}$$

Hence

$$v_{d_1} = \frac{v}{A_1 + 1}$$

Recall that op amp 1 is linear only if

$$-\frac{E_{sat1}^-}{A_1} \leqslant v_{d_1} \leqslant \frac{E_{sat1}^+}{A_1}$$

Equivalently,

$$-\frac{A_1 + 1}{A_1} E_{sat1}^- \leqslant v \leqslant \frac{A_1 + 1}{A_1} E_{sat1}^+$$

For the ideal op amp model we have the simpler constraint

$$-E_{sat1}^- \leqslant v \leqslant E_{sat1}^+$$

Op amp 1 linear and op and amp 2 saturated negative. When op amp 1 is linear and op amp 2 is in negative saturation, KCL at node 2 becomes

$$G_i(A_1v_{d_1} - v_{d_2}) = G_f(v_{d_2} + E_{sat2}^-)$$

This gives

$$v_{d_2} = \frac{A_1 G_i v_{d_1}}{G_f + G_i} - \frac{G_f E_{sat2}^-}{G_f + G_i}$$

Substituting for v_{d_1}, we obtain

$$v_{d_2} = \frac{A_1 G_i v}{(A_1 + 1)(G_f + G_i)} - \frac{G_f E_{sat2}^-}{G_f + G_i}$$

For op amp 2 to be in negative saturation we require that

$$v_{d_2} \leqslant -\frac{E_{sat2}^-}{A_2}$$

Hence op amp 1 is linear and op amp 2 is in negative saturation only if

$$\frac{A_1 G_i v}{(A_1 + 1)(G_f + G_i)} - \frac{G_f E_{sat2}^-}{G_f + G_i} \leqslant -\frac{E_{sat2}^-}{A_2}$$

Equivalently,

$$-\frac{A_1 + 1}{A_1} E_{sat1}^- \leqslant v \leqslant \frac{A_1 + 1}{A_1} E_{sat1}^+ \quad \text{and} \quad v \leqslant \frac{(A_1 + 1)[(A_2 - 1)G_f - G_i]}{A_1 A_2 G_i} E_{sat2}^-$$

For the ideal op amp model

$$-E_{sat1}^- \leqslant v \leqslant E_{sat1}^+ \quad \text{and} \quad v \leqslant \frac{G_f}{G_i} E_{sat2}^-$$

Under these conditions

$$i = G_u u + (G_u + G_H + G_v) v_{d_1} + A_1 G_v v_{d_1} - G_H E_{sat2}^-$$

Grouping terms in v_{d_1}, we obtain

$$i = G_u u + [G_H + G_u + (A_1 + 1)G_v] v_{d_1} - G_H E_{sat2}^-$$

If we now substitute for v_{d_1} in terms of v, this becomes

$$i = G_u u + \left(\frac{G_H + G_u}{A_1 + 1} + G_v\right) v - G_H E_{sat2}^-$$

For the ideal op amp model ($A_1 \to \infty$, $A_2 \to \infty$) we obtain

$$i = G_u + G_v v - G_H E_{sat2}^-$$

Op amp 1 linear and op amp 2 linear. When both op amps are in their linear regions of operation,

$$G_i(A_1 v_{d_1} - v_{d_2}) = G_f(v_{d_2} - A_2 v_{d_2})$$

This yields

$$v_{d_2} = \frac{-A_1 G_i v_{d_1}}{(A_2 - 1)G_f - G_i}$$

which, after substituting for v_{d_1}, becomes

$$v_{d_2} = -\frac{A_1 G_i v}{(A_1 + 1)[(A_2 - 1)G_f - G_i]}$$

Now op amp 2 is linear only if

$$-\frac{E_{sat2}^-}{A_2} \leqslant v_{d_2} \leqslant \frac{E_{sat2}^+}{A_2}$$

Hence both op amps are linear only if

$$-\frac{E_{sat2}^-}{A_2} \leqslant -\frac{A_1 G_i v}{(A_1+1)[(A_2-1)G_f - G_i]} \leqslant \frac{E_{sat2}^+}{A_2}$$

Equivalently,

$$-\frac{A_1+1}{A_1} E_{sat1}^- \leqslant v \leqslant \frac{A_1+1}{A_1} E_{sat1}^+$$

$$\text{and} \quad -\frac{(A_1+1)[(A_2-1)G_f - G_i]}{A_1 A_2 G_i} E_{sat2}^+ \leqslant v \leqslant \frac{(A_1+1)[(A_2-1)G_f - G_i]}{A_1 A_2 G_i} E_{sat2}^-$$

For the ideal op amp this reduces to

$$-E_{sat1}^- \leqslant v \leqslant E_{sat1}^+ \quad \text{and} \quad -\frac{G_f}{G_i} E_{sat2}^+ \leqslant v \leqslant \frac{G_f}{G_i} E_{sat2}^-$$

When both op amps are operating in their linear regimes,

$$i = G_u u + (G_H + G_u + G_v) v_{d_1} + G_v A_1 v_{d_1} + G_H A_2 v_{d_2}$$

We know v_{d_2} in terms of v_{d_1}, so substituting and rearranging gives

$$i = G_u u + \left[G_H + G_u + (A_1+1)G_v - \frac{A_1 A_2 G_H G_i}{(A_2-1)G_f - G_i} \right] v_{d_1}$$

Further, substituting for v_{d_1} yields

$$i = G_u u + \left(\frac{G_H + G_u}{A_1+1} + G_v - \frac{A_1 A_2 G_H G_i}{(A_1+1)[(A_2-1)G_f - G_i]} \right) v$$

For the ideal op amp model ($A_1 \to \infty$, $A_2 \to \infty$) this simplifies to

$$i = G_u u + \left(G_v - \frac{G_H G_i}{G_f} \right) v$$

Op amp 1 linear and op amp 2 saturated positive. When op amp 1 is linear and op amp 2 is in positive saturation, KCL at node 2 becomes

$$G_i(A_1 v_{d_1} - v_{d_2}) = G_f(v_{d_2} - E_{sat2}^+)$$

This gives

$$v_{d_2} = \frac{A_1 G_i v_{d_1}}{G_f + G_i} + \frac{G_f E_{sat2}^+}{G_f + G_i}$$

Substitute for v_{d_1} to obtain

$$v_{d_2} = \frac{A_1 G_i v}{(A_1+1)(G_f + G_i)} + \frac{G_f E_{sat2}^+}{G_f + G_i}$$

Recall that op amp 2 is in positive saturation only if

$$v_{d_2} \geqslant \frac{E_{sat2}^+}{A_2}$$

Thus op amp 1 is linear and op amp 2 is in positive saturation only if

$$\frac{A_1 G_i v}{(A_1+1)(G_f + G_i)} + \frac{G_f E_{sat2}^+}{G_f + G_i} \geqslant \frac{E_{sat2}^+}{A_2}$$

Equivalently,

$$-\frac{A_1+1}{A_1}E_{sat1}^{-} \leqslant v \leqslant \frac{A_1+1}{A_1}E_{sat1}^{+} \quad \text{and} \quad v \geqslant -\frac{(A_1+1)[(A_2-1)G_f-G_i]}{A_1A_2G_i}E_{sat2}^{+}$$

For the ideal op amp this condition arises only if

$$-E_{sat1}^{-} \leqslant v \leqslant E_{sat1}^{+} \quad \text{and} \quad v \geqslant -\frac{G_f}{G_i}E_{sat2}^{+}$$

When op amp 1 is linear and op amp 2 is in positive saturation, then

$$i = G_u u + (G_H + G_u + G_v)v_{d_1} + A_1G_v v_{d_1} + G_H E_{sat2}^{+}$$

giving

$$i = G_u u + [G_H + G_u + (A_1+1)G_v]\,)v_{d_1} + G_H E_{sat2}^{+}$$

Substituting for v_{d_1} yields

$$i = G_u u + \left(\frac{G_H+G_u}{A_1+1} + G_v\right)v + G_H E_{sat2}^{+}$$

For the ideal op amp model ($A_1 \to \infty$, $A_2 \to \infty$) this further reduces to

$$i = G_u u + G_v v + G_H E_{sat2}^{+}$$

Op amp 1 saturated positive ($v_{o_1} = E_{sat1}^{+}$)

When op amp 1 is positive saturation,

$$v = v_{d_1} + E_{sat1}^{+}$$

giving

$$v_{d_1} = v - E_{sat1}^{+}$$

This occurs only if

$$v_{d_1} \geqslant \frac{E_{sat1}^{+}}{A_1}$$

Equivalently,

$$v \geqslant \frac{A_1+1}{A_1}E_{sat1}^{+}$$

For the ideal op amp the condition reduces to

$$v \geqslant E_{sat1}^{+}$$

Op amp 1 saturated positive and op amp 2 saturated negative. When op amp 1 is saturated negative and op amp 2 is saturated positive, KCL at node 2 becomes

$$G_i(E_{sat1}^{+} - v_{d_2}) = G_f(v_{d_2} + E_{sat2}^{-})$$

which gives

$$v_{d_2} = \frac{G_iE_{sat1}^{+} - G_fE_{sat2}^{-}}{G_i + G_f}$$

Recat that op amp 2 is in negative saturation only if

$$v_{d_2} \leqslant -\frac{E_{sat2}^-}{A_2}$$

Hence op amp 1 is in positive saturation and op amp 2 is saturated negative only if

$$v \geqslant \frac{A_1 + 1}{A_1} E_{sat1}^+ \quad \text{and} \quad \frac{G_i E_{sat1}^+ - G_f E_{sat2}^-}{G_i + G_f} \leqslant -\frac{E_{sat2}^-}{A_2}$$

For the ideal op amp model the right-hand side goes to zero and we obtain the simpler conditions

$$v \geqslant E_{sat1}^+ \quad \text{and} \quad \frac{G_i E_{sat1}^+ - G_f E_{sat2}^-}{G_i + G_f} \leqslant 0$$

If op amp 1 is in positive saturation and op amp 2 is in negative saturation, then i is given by

$$i = G_u u + (G_H + G_u + G_v)v_{d_1} + G_v E_{sat1}^+ - G_H E_{sat2}^-$$

With $v_{d_1} = v - E_{sat1}^+$ this gives

$$i = G_u u + (G_H + G_u + G_v)v - (G_H + G_u)E_{sat1}^+ - G_H E_{sat2}^-$$

Op amp 1 saturated positive and op amp 2 linear. When op amp 1 is in positive saturation and op amp 2 is linear, we have that

$$G_i(E_{sat1}^+ - v_{d_2}) = G_f(v_{d_2} - A_2 v_{d_2})$$

Equivalently,

$$v_{d_2} = -\frac{G_i E_{sat1}^+}{(A_2 - 1)G_f - G_i}$$

Now op amp 2 is linear only if

$$-\frac{E_{sat2}^-}{A_2} \leqslant v_{d_2} \leqslant \frac{E_{sat2}^+}{A_2}$$

Hence the amplifiers can be in this state only if

$$v \geqslant \frac{A_1 + 1}{A_1} E_{sat1}^+ \quad \text{and} \quad -\frac{E_{sat2}^-}{A_2} \leqslant -\frac{G_i E_{sat1}^+}{(A_2 - 1)G_f - G_i} \leqslant \frac{E_{sat2}^+}{A_2}$$

For the ideal op amp model these conditions become

$$v \geqslant E_{sat1}^+ \quad \text{and} \quad -E_{sat2}^- \leqslant -\frac{G_i E_{sat1}^+}{G_f} \leqslant E_{sat2}^+$$

Under these conditions

$$i = G_u u + (G_H + G_u + G_v)v_{d_1} + G_v E_{sat1}^+ + G_H A_2 v_{d_2}$$

Substituting for v_{d_2} in terms of v,

$$i = G_u u + (G_H + G_u + G_v)v_{d_1} + G_v E_{sat1}^+ - \frac{A_2 G_H G_i}{(A_2 - 1)G_f - G_i} E_{sat1}^+$$

$$i = G_u u + (G_H + G_u + G_v)v - (G_H + G_u)E_{sat1}^+ - \frac{A_2 G_H G_i}{(A_2 - 1)G_f - G_i} E_{sat1}^+$$

For the ideal op amp model ($A_1 \to \infty$, $A_2 \to \infty$) this reduces to the simpler form

$$i = G_u u + (G_H + G_u + G_v)v - (G_H + G_u)E_{sat1}^+ - \frac{G_H G_i}{G_f} E_{sat1}^+$$

Op amp 1 saturated positive and op amp 2 saturated positive. When both op amps are in positive saturation, we have (from KCL at node 2)

$$G_i(E_{sat1}^+ - v_{d_2}) = G_f(v_{d_2} - E_{sat2}^+)$$

giving

$$v_{d_2} = \frac{G_i E_{sat1}^+ + G_f E_{sat2}^+}{G_i + G_f}$$

Recall that op amp 2 is in positive saturation only if

$$v_{d_2} \geqslant \frac{E_{sat2}^+}{A_2}$$

Thus both op amps are in positive saturation only if

$$v \geqslant \frac{A_1 + 1}{A_1} E_{sat1}^+ \quad \text{and} \quad \frac{G_i E_{sat1}^+ + G_f E_{sat2}^+}{G_i + G_f} \geqslant \frac{E_{sat2}^+}{A_2}$$

For the ideal op amp model these inequalities reduce to

$$v \geqslant E_{sat1}^+ \quad \text{and} \quad \frac{G_i E_{sat1}^+ + G_f E_{sat2}^+}{G_i + G_f} \geqslant 0$$

Under these conditions we obtain

$$i = G_u u + (G_H + G_u + G_v)v_{d_1} + G_v E_{sat1}^+ + G_H E_{sat2}^+$$

Equivalently,

$$i = G_u u + (G_H + G_u + G_v)v - (G_H + G_u)E_{sat1}^+ + G_H E_{sat2}^+$$

Summary (see Figure 43)

Op amp 1	Op amp 2	i
− Sat	− Sat	$G_u u + (G_H + G_u + G_v)v + (G_H + G_u)E_{sat1}^- - G_H E_{sat2}^-$
	Linear	$G_u u + (G_H + G_u + G_v)v + (G_H + G_u)E_{sat1}^- + \frac{A_2 G_H G_i}{(A_2 - 1)G_f - G_i} E_{sat1}^-$
	+ Sat	$G_u u + (G_H + G_u + G_v)v + (G_H + G_u)E_{sat1}^- + G_H E_{sat2}^+$
Linear	− Sat	$G_u u + \left(\frac{G_H + G_u}{A_1 + 1} + G_v\right)v - G_H E_{sat2}^-$
	Linear	$G_u u + \left(\frac{G_H + G_u}{A_1 + 1} + G_v - \frac{A_1 A_2 G_H G_i}{(A_1 + 1)[(A_2 - 1)G_f - G_i]}\right)v$
	+ Sat	$G_u u + \left(\frac{G_H + G_u}{A_1 + 1} + G_v\right)v + G_H E_{sat2}^+$
+ Sat	− Sat	$G_u u + (G_H + G_u + G_v)v - (G_H + G_u)E_{sat1}^+ - G_H E_{sat2}^-$
	Linear	$G_u u + (G_H + G_u + G_v)v - (G_H + G_u)E_{sat1}^+ - \frac{A_2 G_H G_i}{(A_2 - 1)G_f - G_i} E_{sat1}^+$
	+ Sat	$G_u u + (G_H + G_u + G_v)v - (G_H + G_u)E_{sat1}^+ + G_H E_{sat2}^+$

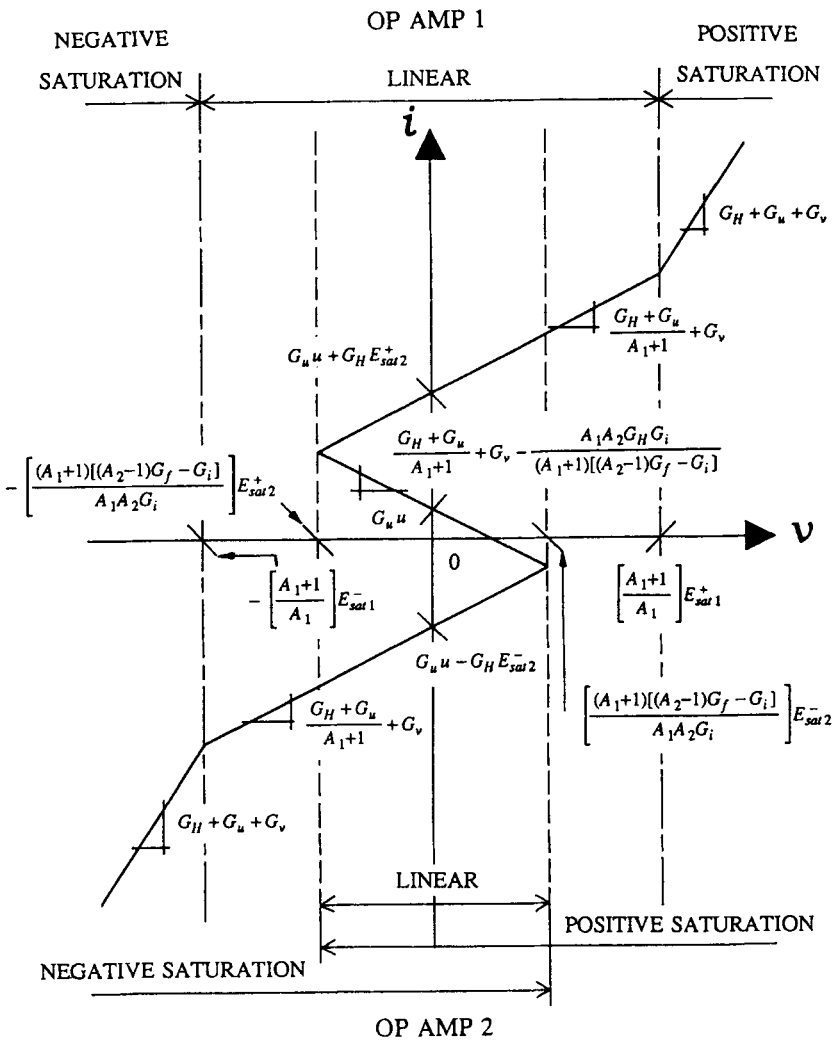

Figure 43. DP characteristic at terminals 1–1′ of the capacitor in the neural-type pulse oscillator (Figure 42)

Example (see Figure 26)

We assume for simplicity that $A_1 \to \infty$ and $A_2 \to \infty$ (this corresponds to the ideal op amp model). The circuit values are $G_f = G_H = G_v = G_u = \frac{1}{20}$ mS and $G_i = \frac{1}{10}$ mS. The saturation levels are ± 4 V.

Op amp 1	Op amp 2	i (mA)	Valid for
− Sat	− Sat	$\frac{1}{20}u + \frac{3}{20}v + \frac{4}{20}$	$v \leqslant -4$ V
Linear	− Sat	$\frac{1}{20}u + \frac{1}{20}v - \frac{4}{20}$	-4 V $\leqslant v \leqslant 2$ V
	Linear	$\frac{1}{20}u - \frac{1}{20}v$	-2 V $\leqslant v \leqslant 2$ V
	+ Sat	$\frac{1}{20}u + \frac{1}{20}v + \frac{4}{20}$	-2 V $\leqslant v \leqslant 4$ V
+ Sat	+ Sat	$\frac{1}{20}u + \frac{3}{20}v - \frac{4}{20}$	$v \geqslant 4$ V

APPENDIX II: MULTIVIBRATOR, NEGATIVE RESISTANCE CONVERTOR, SCHMITT TRIGGER (REFER TO FIGURE 44)

KCL

At node 1

$$i = G_u(v - u) + G_H(v - v_o) = -G_u u + (G_H + G_u)v - G_H v_o$$

At node 2

$$e_2 G_i = (v_o - e_2)G_f, \qquad e_2 = \frac{G_f v_o}{G_f + G_i}$$

KVL

Around loop 0–1–2

$$v + v_d = e_2 = \frac{G_f v_o}{G_f + G_i}$$

Op amp saturated negative ($v_o = -E_{sat}^-$)

This condition exists when

$$v_d \leqslant -\frac{E_{sat}^-}{A}$$

Equivalently (from KVL),

$$-\frac{G_f E_{sat}^-}{G_f + G_i} - v \leqslant -\frac{E_{sat}^-}{A}$$

Thus $v_0 = -E_{sat}^-$ when

$$v \geqslant -\frac{(A-1)G_f - G_i}{A(G_f + G_i)} E_{sat}^-$$

KCL now gives

$$i = -G_u u + (G_H + G_u)v + G_H E_{sat}^-$$

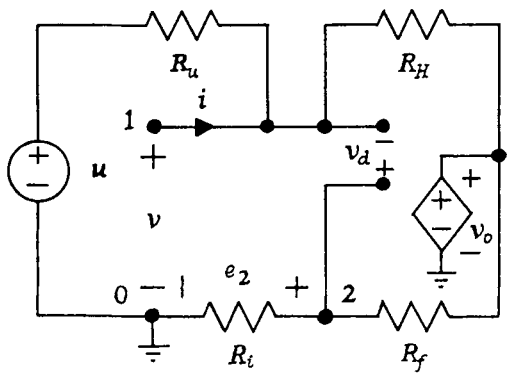

Figure 44. Equivalent circuit for the resistive subnetwork of Figure 37; we use the three-segment PWL finite gain op amp voltage transfer characteristic of Figure 10 to calculate the DP and TC

When $G_u = 0$ (corresponding to a negative resistance convertor—see Figure 39),

$$i = G_H v + G_H E_{sat}^-$$

Op amp linear

In this region

$$v_o = A v_d$$

From KVL we obtain

$$v + v_d = \frac{A G_f v_d}{G_f + G_i}$$

Equivalently,

$$v = \frac{(A-1)G_f - G_i}{G_f + G_i} v_d$$

This gives (see Figure 41)

$$v_o = \frac{A(G_f + G_i)}{(A-1)G_f - G_i} v$$

The linear region is defined by

$$-\frac{E_{sat}^-}{A} \leqslant v_d \leqslant \frac{E_{sat}^+}{A}$$

Equivalently,

$$-\frac{(A-1)G_f - G_i}{A(G_f + G_i)} E_{sat}^- \leqslant v \leqslant \frac{(A-1)G_f - G_i}{A(G_f + G_i)} E_{sat}^+$$

KCL gives

$$i = -G_u u + (G_H + G_u)v - A G_H v_d = -G_u u + \left(G_H + G_u - \frac{A G_H (G_f + G_i)}{(A-1)G_f - G_i}\right) v$$

When $G_u = 0$ (see Figure 39),

$$i = -\frac{G_H[(A+1)G_i + G_f]}{(A-1)G_f - G_i} v$$

Op amp saturated positive ($v_o = E_{sat}^+$)

This condition exists when

$$v_d \geqslant \frac{E_{sat}^+}{A}$$

Equivalently,

$$\frac{G_f E_{sat}^+}{G_f + G_i} - v \geqslant \frac{E_{sat}^-}{A}$$

Thus $v_o = E_{sat}^+$ when

$$v \leqslant \frac{(A-1)G_f - G_i}{A(G_f + G_i)} E_{sat}^+$$

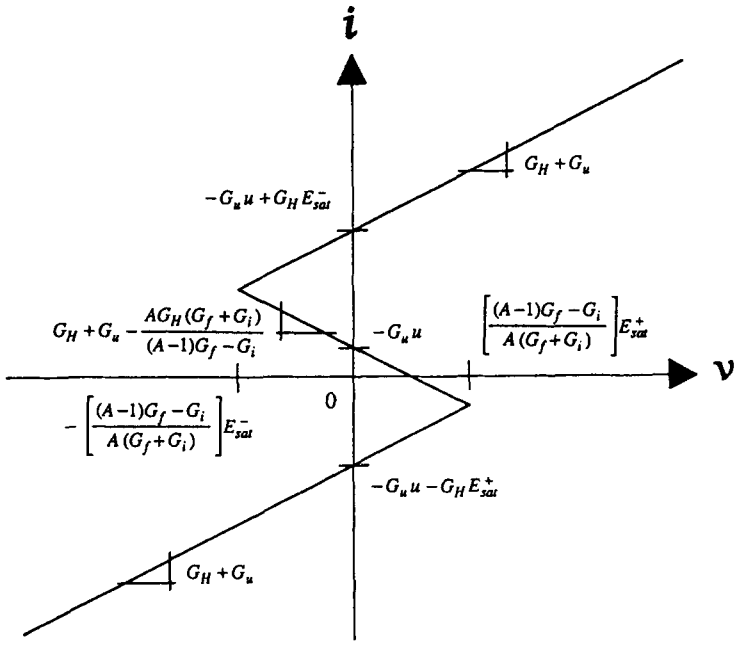

Figure 45. DP characteristic across terminals 1–0 of Figure 44. With the appropriate choice of R_H, R_u, R_f and R_i we can produce a characteristic which is identical to Figure 26 over its central three segments

KCL now gives

$$i = -G_u u + (G_H + G_u)v - G_H E_{sat}^+$$

When $G_u = 0$ (Figure 39),

$$i = G_H v - G_H E_{sat}^+$$

Summary (see Figure 45)

For the special case when $G_u = 0$, see Figure 39(b).

Op amp	v_d	v_o	i
– Sat	$v_d \leqslant -\frac{E_{sat}^-}{A}$	$-E_{sat}^-$	$-G_u u + (G_H + G_u)v + G_H E_{sat}^-$
– Linear	$-\frac{E_{sat}^-}{A} \leqslant v_d \leqslant \frac{E_{sat}^+}{A}$	$\frac{A(G_f + G_i)}{(A-1)G_f - G_i} v$	$-G_u u + \left(G_H + G_u - \frac{AG_H(G_f + G_i)}{(A-1)G_f - G_i}\right)v$
+ Sat	$v_d \geqslant \frac{E_{sat}^-}{A}$	E_{sat}^+	$-G_u u + (G_H + G_u)v - G_H E_{sat}^+$

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