

**IN THE UNITED STATES DISTRICT COURT
FOR THE DISTRICT OF DELAWARE**

PACT XPP SCHWEIZ AG,

Plaintiff

v.

INTEL CORPORATION,

Defendant

Case No. 1:19-cv-01006-JDW

ORDER

AND NOW, this 30th day of September, 2020, for the reasons stated in the accompanying Memorandum, it is **ORDERED** that the Court construes the following claim terms of US Patent Nos. 7,928,763 (“the ’763 patent”); 8,312,301 (the “’301 patent”); 8,471,593 (the “’593 patent”); 8,819,505 (the “’505 patent”); 9,075,605 (the “’605 patent”); 9,170,812 (the “’812 patent”); 9,436,631 (the “’631 patent”); 9,552,047 (the “’047 patent”); 9,250,908 (the “’908 Patent”); 8,301,872 (the “’872 Patent”); and 9,037,807 (the “’807 Patent”) as follows:

<u>Claim Term</u>	<u>Court’s Construction</u>
<i>Contested Terms</i>	
A multi-processor chip, comprising ‘763 Patent, Preamble of claims 1, 31	Not limiting
Programmably/dynamically interconnecting at runtime at least one of data processing cells and memory cells and one or more of the at least one interface unit ‘763 Patent, Claims 1, 31	Variably interconnecting at runtime at least one of data processing cells and memory cells and one or more of the at least one interface unit
Data processing cells, each adapted for sequentially executing ‘763 Patent, Claims 1, 31	Plain and ordinary meaning; no construction necessary

A data processor on a chip comprising '593 Patent, Preamble of claims 1, 16	Limiting as to "data processor"
A plurality of bus segments for each processor of the multiprocessor system '631 Patent, Claim 1	Plain and ordinary meaning; no construction necessary
Instruction dispatch unit . . . configured to dispatch software threads to the array data processor for parallel execution by the parallel processing arithmetic units '812 Patent, Claim 12	Plain and ordinary meaning; no construction required 38 U.S.C. § 112, ¶ 6 does not apply
Preambles '047 Patent, Claims 1, 19	Not limiting
Data processing unit and/or data processing units . . . adapted for sequentially processing data '047 Patent, Claims 1-5, 8, 10, 15, 19, 22, 24 '605 Patent, Claim 1	Sequential data processors that pass results to one or more additional data processing units to perform additional computations
To a minimum '605 Patent, Claim 1	Plain and ordinary meaning; no construction necessary
Data processing element and/or data processing elements adapted for programmably processing sequences '057 Patent, Claim 19	Plain and ordinary meaning; no construction necessary
<i>Agreed-Upon Constructions</i>	
Preamble '605 Patent, Claim 1	Preamble is limiting
Train mission '908 Patent, Claim 4	Transmission
May executed '631 Patent, Claim 1	May be executed
Preambles '872 Patent, Claims 2, 10, 14, 15)	Preambles are not limiting
Preambles '807 Patent, claims 1-6, 24, 26-27, 29, 32, 44, 73-74	Preambles are not limiting

Preamble '812 Patent, claim 12	No construction necessary
Preamble '301 Patent, Claims 6, 8, 12	Preambles are limiting
Preamble '301 Patent, Claim 10	Preamble is not limiting
'505 Patent, Claims 1 and 5	All claimed components must exist on a single, integrated circuit

BY THE COURT:

/s/ Joshua D. Wolson

JOSHUA D. WOLSON, J.
United States District Judge