Intel Corporation, Petitioner
v.
PACT XPP Schweiz AG, Patent Owner

Petitioner's Oral Argument

June 15, 2021

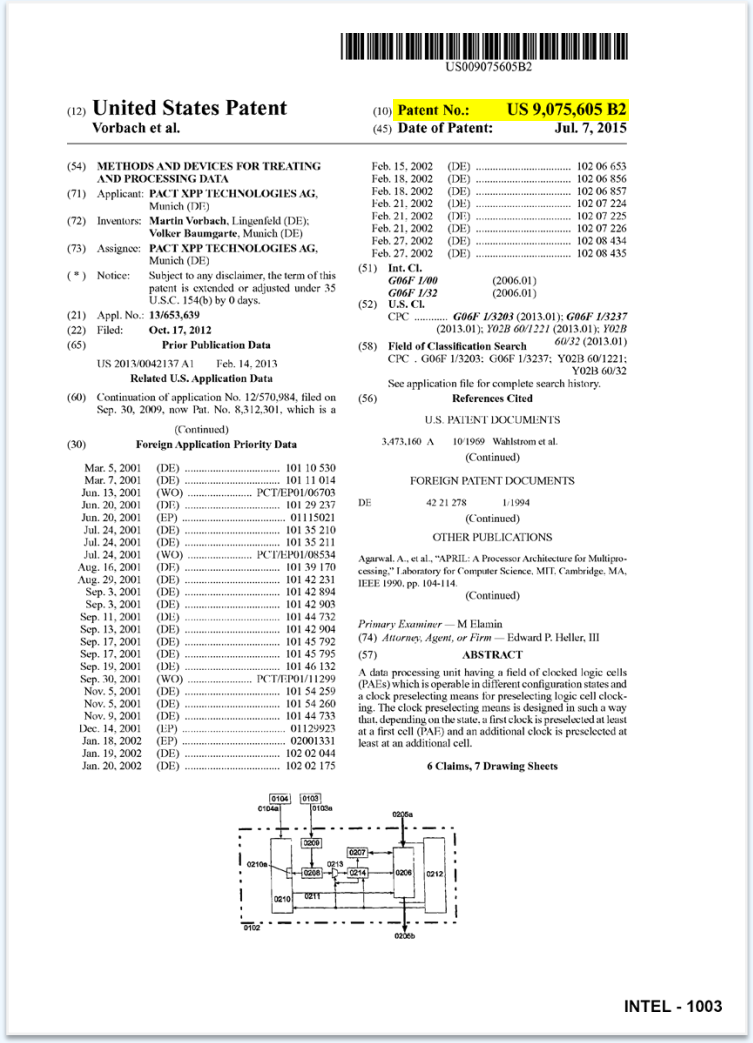
Case No. IPR2020-00541 (Patent 9,075,605)

INTEL - 1056

Challenged ’605 Patent

Case No. IPR2020-00541 (Patent 9,075,605)

Challenged ’605 Patent



US009075605B2

(12) **United States Patent**
Vorbach et al.

(10) **Patent No.: US 9,075,605 B2**
(45) **Date of Patent: Jul. 7, 2015**

(54) **METHODS AND DEVICES FOR TREATING AND PROCESSING DATA**
(71) Applicant: **PACT XPP TECHNOLOGIES AG**, Munich (DE)
(72) Inventors: **Martin Vorbach**, Lingenfeld (DE); **Volker Baumgarte**, Munich (DE)
(73) Assignee: **PACT XPP TECHNOLOGIES AG**, Munich (DE)
(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.
(21) Appl. No.: **13/653,639**
(22) Filed: **Oct. 17, 2012**
(65) **Prior Publication Data**
US 2013/0042137 A1 Feb. 14, 2013
Related U.S. Application Data
(60) Continuation of application No. 12/570,984, filed on Sep. 30, 2009, now Pat. No. 8,312,301, which is a
(Continued)
(30) **Foreign Application Priority Data**

Mar. 5, 2001	(DE)	101 10 530
Mar. 7, 2001	(DE)	101 11 014
Jun. 13, 2001	(WO)	PCT/EP01/06703
Jun. 20, 2001	(DE)	101 29 237
Jun. 20, 2001	(EP)	01115021
Jul. 24, 2001	(DE)	101 35 210
Jul. 24, 2001	(DE)	101 35 211
Jul. 24, 2001	(WO)	PCT/EP01/08534
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Sep. 30, 2001	(WO)	PCT/EP01/11299
Nov. 5, 2001	(DE)	101 54 259
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Nov. 9, 2001	(DE)	101 44 733
Dec. 14, 2001	(EP)	01129923
Jan. 18, 2002	(EP)	02001331
Jan. 19, 2002	(DE)	102 02 044
Jan. 20, 2002	(DE)	102 02 175
Feb. 15, 2002	(DE)	102 06 653
Feb. 18, 2002	(DE)	102 06 856
Feb. 18, 2002	(DE)	102 06 857
Feb. 21, 2002	(DE)	102 07 224
Feb. 21, 2002	(DE)	102 07 225
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Feb. 27, 2002	(DE)	102 08 434
Feb. 27, 2002	(DE)	102 08 435

(51) **Int. Cl.**
G06F 1/00 (2006.01)
G06F 1/32 (2006.01)
(52) **U.S. Cl.**
CPC ***G06F 1/3203*** (2013.01); ***G06F 1/3237*** (2013.01); *Y02B 60/1221* (2013.01); *Y02B 60/32* (2013.01)
(58) **Field of Classification Search**
CPC . G06F 1/3203; G06F 1/3237; Y02B 60/1221; Y02B 60/32
See application file for complete search history.
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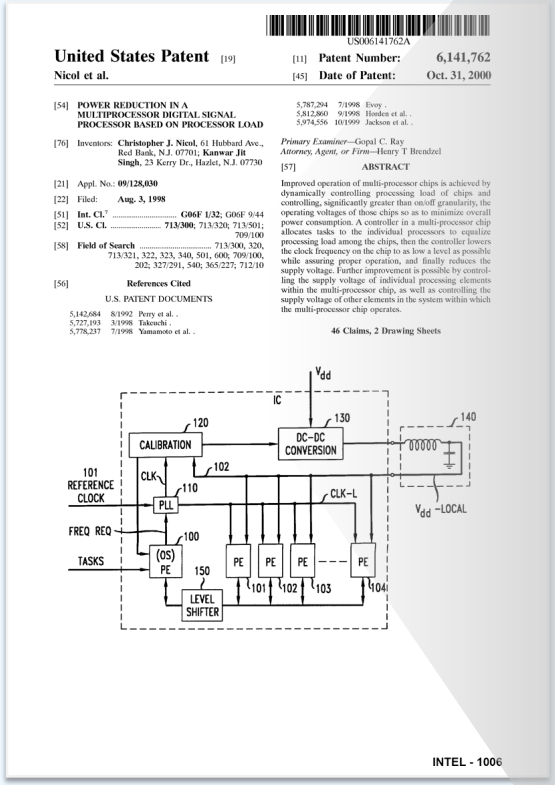
Agarwal, A., et al., “APRIL: A Processor Architecture for Multiprocessing,” Laboratory for Computer Science, MIT, Cambridge, MA, IEEE 1990, pp. 104-114.
(Continued)
Primary Examiner — M Elamin
(74) *Attorney, Agent, or Firm* — Edward P. Heller, III
(57) **ABSTRACT**
A data processing unit having a field of clocked logic cells (PAEs) which is operable in different configuration states and a clock preselecting means for preselecting logic cell clocking. The clock preselecting means is designed in such a way that, depending on the state, a first clock is preselected at least at a first cell (PAE) and an additional clock is preselected at least at an additional cell.
6 Claims, 7 Drawing Sheets

INTEL - 1003

- 6 Challenged Claims
- Prior Art Ground I: Claims 1-6
  - **Nicol** in view of **Kling**
- Prior Art Grounds II and III:
  - No longer at issue because of the District Court’s claim construction

Nicol Overview

Patent Number: 6,141,762



US006141762A

United States Patent [19]
Nicol et al.

[11] **Patent Number: 6,141,762**
[45] **Date of Patent: Oct. 31, 2000**

[54] **POWER REDUCTION IN A MULTIPROCESSOR DIGITAL SIGNAL PROCESSOR BASED ON PROCESSOR LOAD**

[76] Inventors: **Christopher J. Nicol**, 61 Hubbard Ave., Red Bank, N.J. 07701; **Kanwar Jit Singh**, 23 Kerry Dr., Hazlet, N.J. 07730

[21] Appl. No.: **09/128,030**

[22] Filed: **Aug. 3, 1998**

[51] **Int. Cl.**[7] **G06F 1/32**; G06F 9/44

[52] **U.S. Cl.** **713/300**; 713/320; 713/501; 709/100

[58] **Field of Search** 713/300, 320, 713/321, 322, 323, 340, 501, 600; 709/100, 202; 327/291, 540; 365/227; 712/10

[56] **References Cited**

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Primary Examiner—Gopal C. Ray
Attorney, Agent, or Firm—Henry T Brendzel

[57] **ABSTRACT**

Improved operation of multi-processor chips is achieved by dynamically controlling processing load of chips and controlling, significantly greater than on/off granularity, the operating voltages of those chips so as to minimize overall power consumption. A controller in a multi-processor chip allocates tasks to the individual processors to equalize processing load among the chips, then the controller lowers the clock frequency on the chip to as low a level as possible while assuring proper operation, and finally reduces the supply voltage. Further improvement is possible by controlling the supply voltage of individual processing elements within the multi-processor chip, as well as controlling the supply voltage of other elements in the system within which the multi-processor chip operates.

46 Claims, 2 Drawing Sheets

INTEL - 1006

Ex. 1009

POWER REDUCTION IN A MULTIPROCESSOR DIGITAL SIGNAL PROCESSOR BASED ON PROCESSOR LOAD

Inventors: **Christopher J. Nicol**, 61 Hubbard Ave., Red Bank, N.J. 07701; **Kanwar Jit Singh**, 23 Kerry Dr., Hazlet, N.J. 07730

Appl. No.: **09/128,030**

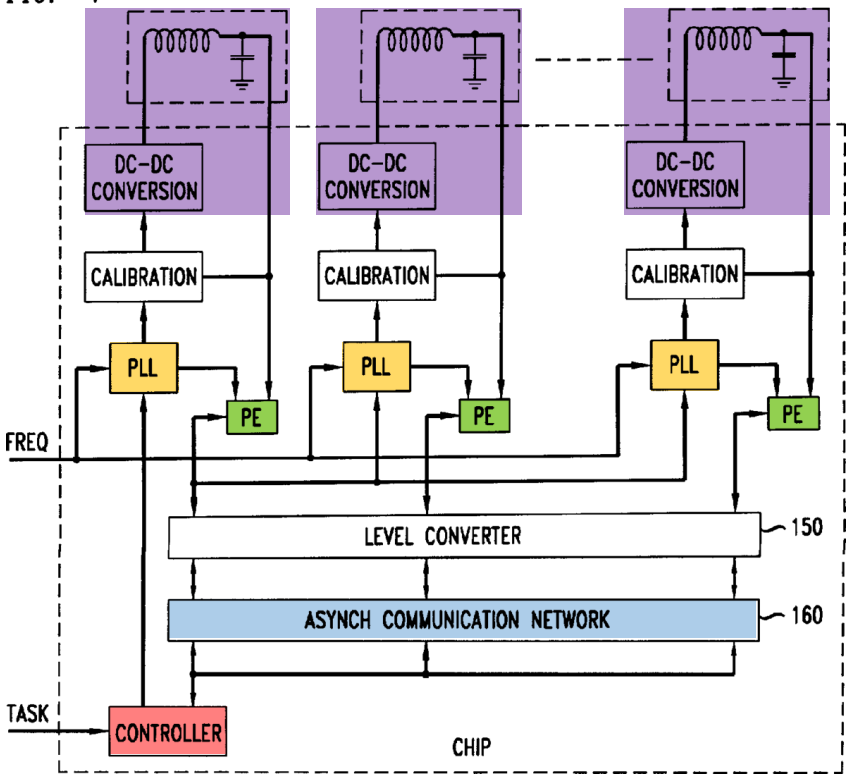
Filed: **Aug. 3, 1998**

[57] **ABSTRACT**

Improved operation of multi-processor chips is achieved by dynamically controlling processing load of chips and controlling, significantly greater than on/off granularity, the operating voltages of those chips so as to minimize overall power consumption. A controller in a multi-processor chip allocates tasks to the individual processors to equalize processing load among the chips, then the controller lowers the clock frequency on the chip to as low a level as possible while assuring proper operation, and finally reduces the supply voltage. Further improvement is possible by controlling the supply voltage of individual processing elements within the multi-processor chip, as well as controlling the supply voltage of other elements in the system within which the multi-processor chip operates.

Ex. 1009, Abstract

FIG. 4



Ex. 1009 at Fig. 4 (annotated); Pet. at 12-13

Pet. at 12-14

Nicol's RTOS

(CPU) and a local cache memory (not shown). A real-time operating system resides in PE **100** and allocates tasks to the other PEs from a mix of many digital signal processing applications. The load of the FIG. **2** system is time varying

Ex. 1009 at 2:53-56

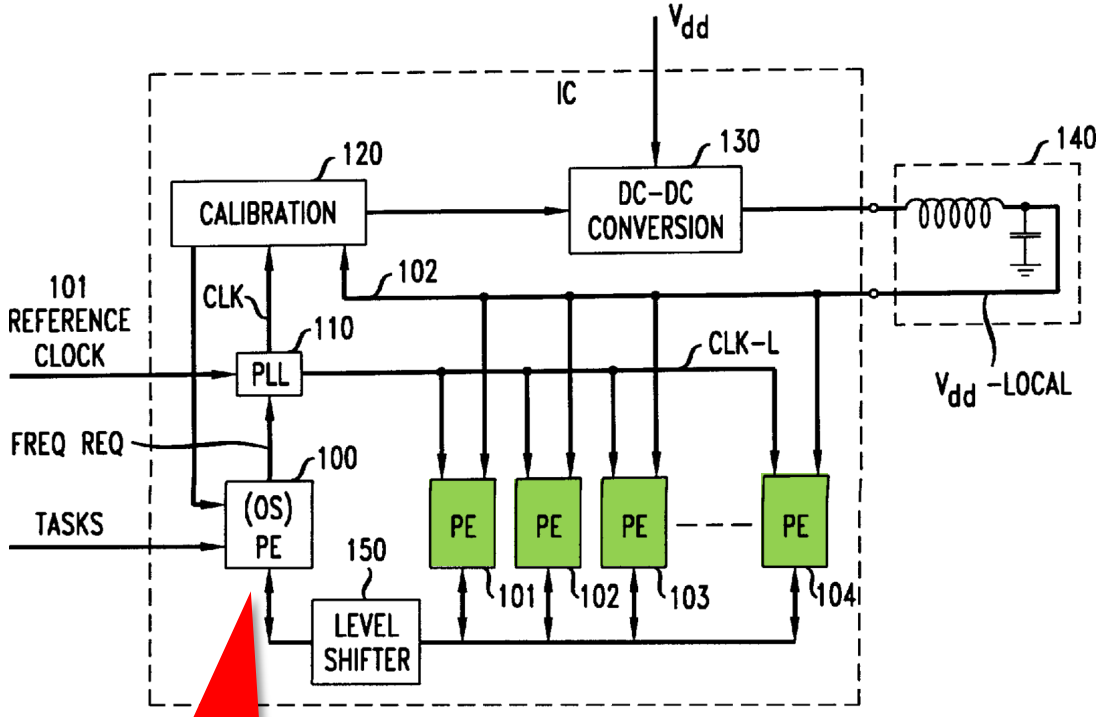
power consumption. A controller in a multi-processor chip allocates tasks to the individual processors to equalize processing load among the chips, then the controller lowers the clock frequency on the chip to as low a level as possible while assuring proper operation, and finally reduces the supply voltage. Further improvement is possible by control-

Ex. 1009 at Abstract

In the FIG. **2** arrangement, in accordance with the principles disclosed herein, the applications that need to be processed are mapped to the N PEs under control of real time operating system (RTOS) executed on PE **100**. If the number of instructions that need to be executed for each task is known and made available to the operating system, a scheduler within the operating system can use this information to determine the best way to allocate the tasks to the available processors in order to balance the computation.

Ex. 1009 at 3:10-18

FIG. 2



RTOS Assigns Tasks And Frequency/Voltage Pair To PEs

Ex. 1009 at Fig. 2

Pet. at 12-14

Nicol's Figure 2 Embodiment

appended claims. For example, in one of the embodiment disclosed above all of the PEs in a multi-processor chip are subjected to a single controlled supply voltage. In another embodiment disclosed above each of the PEs in a multi-processor chip is subjected to its own, individually controlled, supply voltage. It should be realized, however, that a middle ground is also possible; i.e., the PEs of a multi-processor chip can be divided into groups, and each group of PEs can be arranged to operate from its own controlled supply voltage. To cite another example, the FIG.

Ex. 1009 at 6:61-7:3

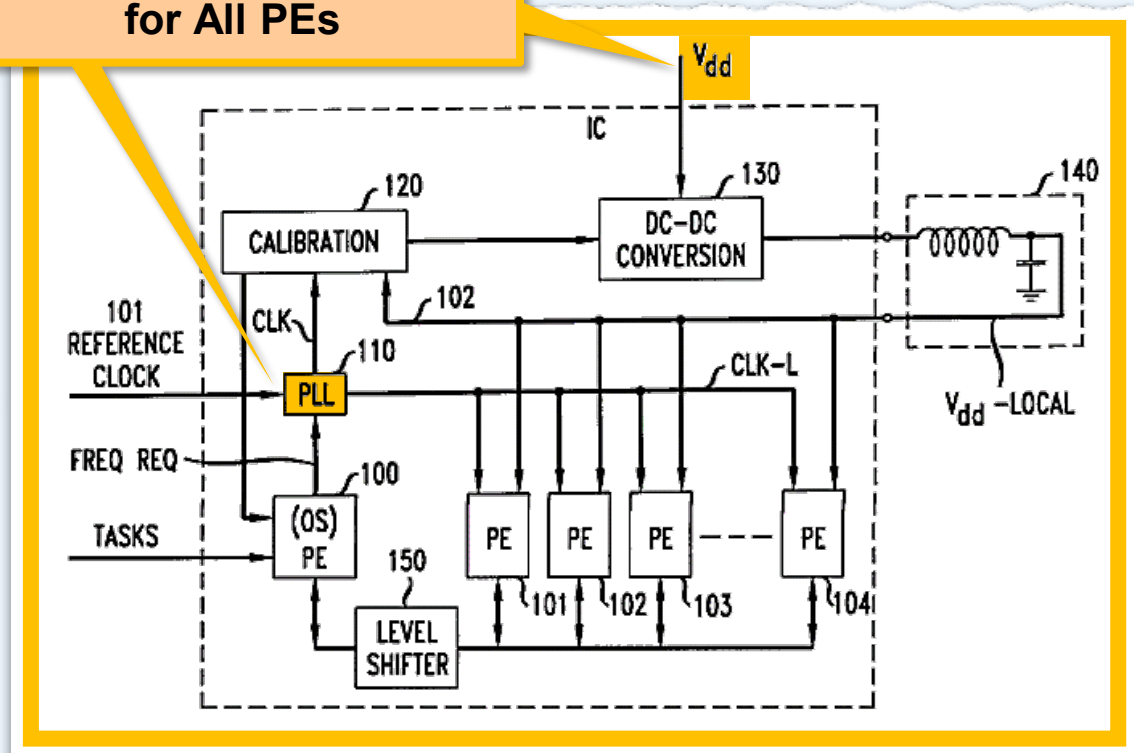
The FIG. **2** system uses the operating system to react to variations in the system load. As more tasks are entered into the "to-do" list, the operating system of PE **100** computes the correct way to balance the additional computational requirements and allocates the tasks to the processors. It then computes the required operating frequency.

Ex. 1009 at 5:24-29

voltage. The benefit of this approach for some applications becomes apparent when it is realized that the chip-wise voltage scaling is most effective when the load of the computation can be evenly distributed across all of the PEs. In some applications, however, one may encounter tasks that cannot be partitioned into concurrent evenly-loaded threads and, therefore, some PE within the multiprocessor would require a higher operating frequency and a higher operating voltage. This would require raising the frequency and voltage of the entire multiprocessor chip.

Ex. 1009 at 5:56-65

Figure 2:
Same Frequency/Voltage for All PEs



Ex. 1009 at Fig. 2 (annotated)

Pet. at 12-14, 25-27

Nicol's Figure 4 Embodiment

A separate power supply for each PE in a chip overcomes this limitation by allowing the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE. The architecture of such an arrangement is shown in FIG. **4**. Each PE in

Ex. 1009 at 5:66-6:3

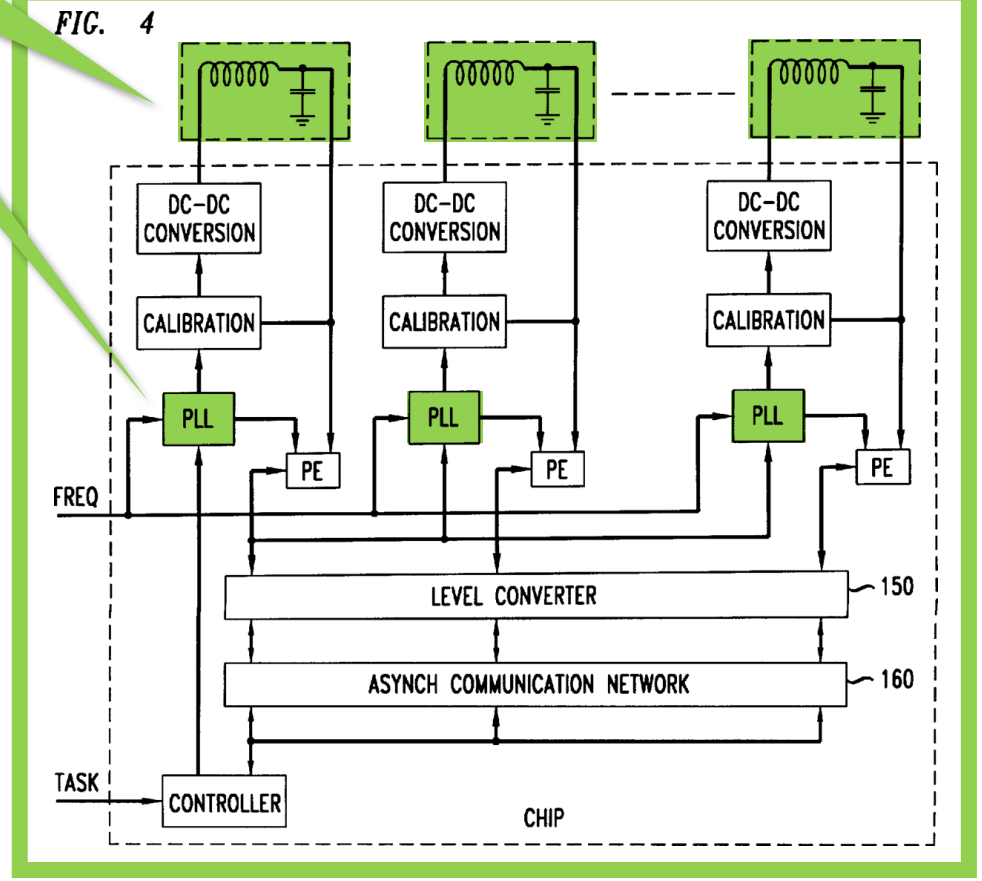
converter circuit like circuits **130** and **140**. It also has a PE **200** that assigns the tasks given to the multi-processor chip of FIG. **4** among the PEs.

Ex. 1009 at 6:11-12

appended claims. For example, in one of the embodiment disclosed above all of the PEs in a multi-processor chip are subjected to a single controlled supply voltage. In another embodiment disclosed above each of the PEs in a multi-processor chip is subjected to its own, individually controlled, supply voltage. It should be realized, however, that a middle ground is also possible; i.e., the PEs of a multi-processor chip can be divided into groups, and each group of PEs can be arranged to operate from its own controlled supply voltage. To cite another example, the FIG.

Ex. 1009 at 6:61-7:3

Figure 4:
Ability To Independently Set Frequency/Voltage for Each PE



Ex. 1009 at Fig. 4

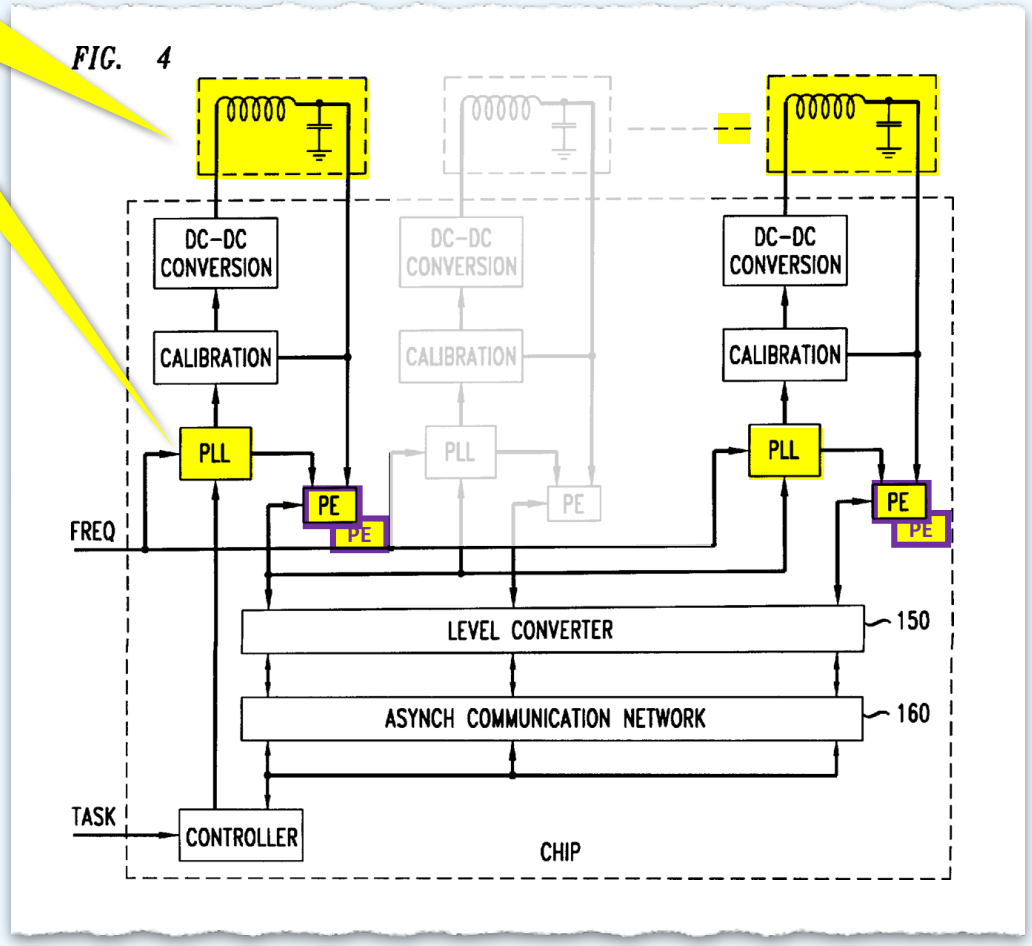
Pet. at 12-14, 25-27

Nicol's Middle Ground Embodiment

Middle Ground:
Ability To Independently Set Frequency/Voltage for Groups of PEs

appended claims. For example, in one of the embodiment disclosed above all of the PEs in a multi-processor chip are subjected to a single controlled supply voltage. In another embodiment disclosed above each of the PEs in a multi-processor chip is subjected to its own, individually controlled, supply voltage. It should be realized, however, that a middle ground is also possible; i.e., the PEs of a multi-processor chip can be divided into groups, and each group of PEs can be arranged to operate from its own controlled supply voltage. To cite another example, the FIG.

Ex. 1009 at 6:61-7:3



Ex. 1009 at Fig. 4 (annotated)

Pet. at 12-14, 25-27

Dr. Mangione-Smith

Q. So in the middle ground embodiment there are circumstances where one PE's frequency will be set by the controller to be -- will be set by the controller based on the load of another PE; fair?

A. I do think that in this hypothetical situation we were just talking about, whether it's a Figure 2 system in isolation or sort of this middle ground that combines elements of Figure 2 with Figure 4, the Figure 2 components, PE 1 and 2, will operate -- will be configured to operate at a clock speed that satisfies the requirements of whichever one is most heavily loaded.

Ex. 1051 at 65:12-25 (objection omitted)

Reply at 7-8

PACT Arguments Against 605

TABLE OF CONTENTS

POR at i-iii

The ’605 Patent – Claim 1

Claim 1

1. A method for operating a multiprocessor system comprising a plurality of data processing cells, each of the plurality of data processing units (a) including at least one Arithmetic Logic Unit (ALU) and a register unit and (b) being adapted for sequentially processing data, the method comprising:

the multiprocessor system setting a clock frequency, of at least a part of the multiprocessor system to a minimum in accordance with a number of pending operations of a first processor;

the multiprocessor system subsequently increasing the clock frequency of the at least the part of the multiprocessor system to a maximum in accordance with a number of pending operations of a second processor; and

the multiprocessor system subsequently reducing the clock frequency of the at least the part of the multiprocessor system in accordance with (a) an operating temperature threshold preventing over-temperature and (b) a hysteresis characteristic.

Ex. 1003 at Claim 1

Nicol Teaches Setting The Clock Frequency To A Minimum Based On The Number Of Pending Operations Of A First PE

the multiprocessor system setting a clock frequency, of at least a part of the multiprocessor system to a minimum in accordance with a number of pending operations of a first processor;

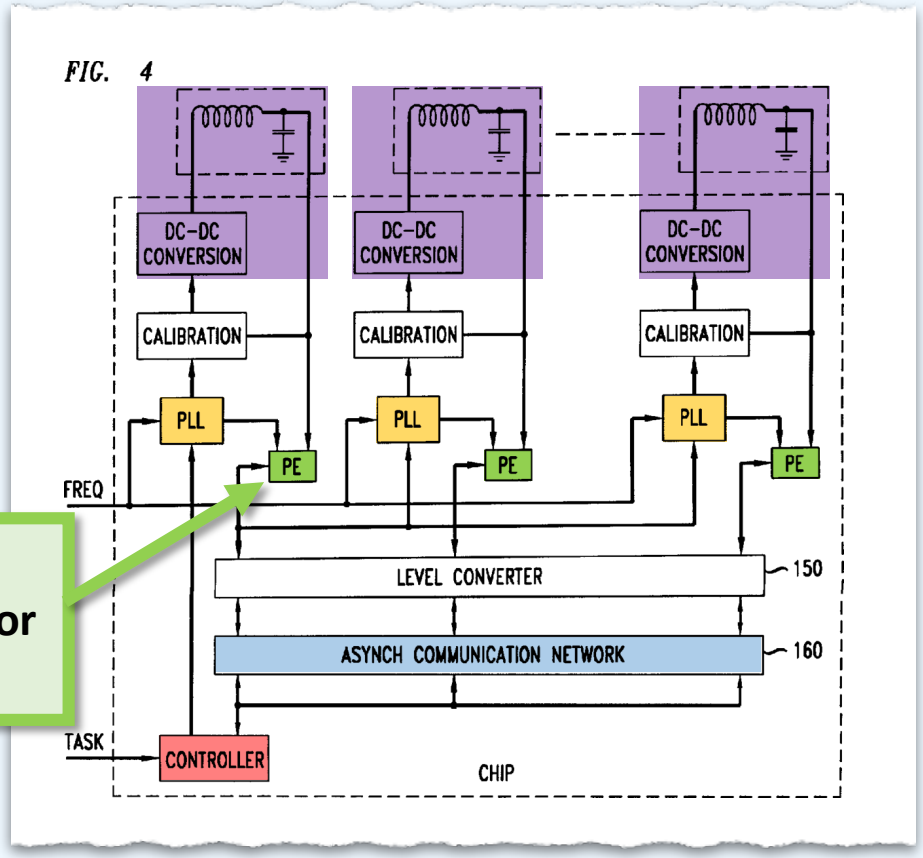
Ex. 1003 at Claim 1

minimize overall power consumption. A controller in a multi-processor chip allocates tasks to the individual processors to equalize processing load among the chips, then the controller lowers the clock frequency on the chip to as low a level as possible while assuring proper operation, and finally reduces the supply voltage. Further improvement is

Ex. 1009 at 2:23-27

A separate power supply for each PE in a chip overcomes this limitation by allowing the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE. The architecture of such an arrangement is shown in FIG. 4. Each PE in

Ex. 1009 at 5:66-6:3



Ex. 1009 at Fig. 4 (annotated)

Pet. at 35-37; Reply at 11-12

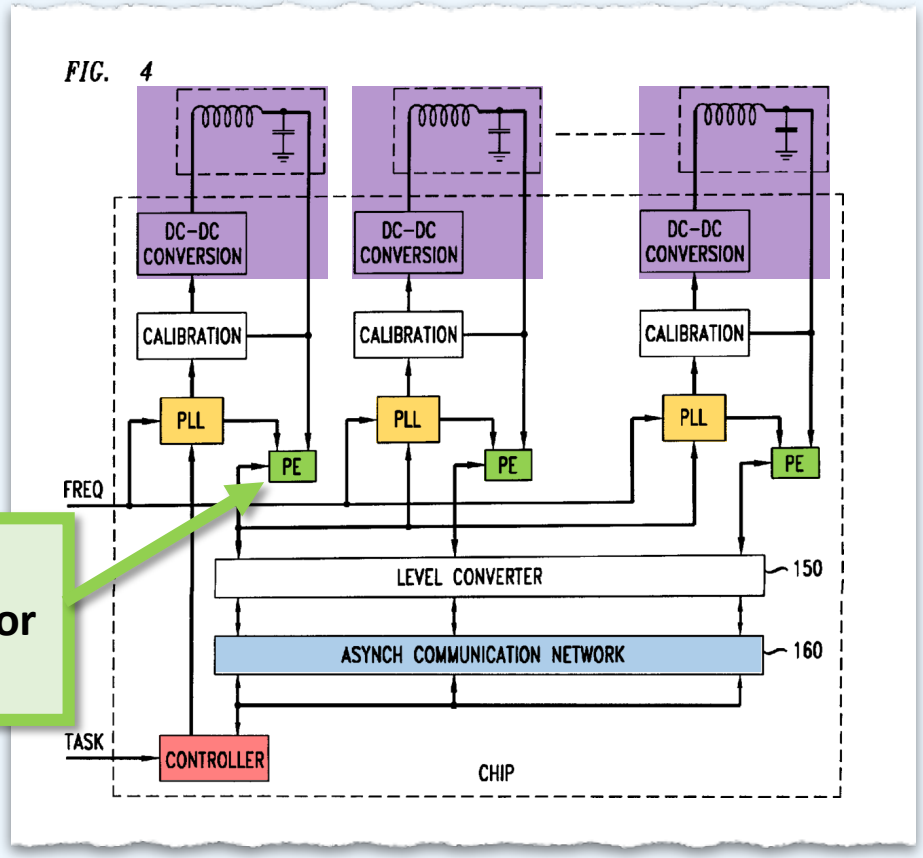
Figure 4 Controller Divides Tasks Among PEs

the multiprocessor system setting a clock frequency, of at least a part of the multiprocessor system to a minimum in accordance with a number of pending operations of a first processor;

Ex. 1003 at Claim 1

sponding lowest supply voltage for each PE. The architecture of such an arrangement is shown in FIG. **4**. Each PE in FIG. **4** needs an independent controller that performs the functions of PE **100** (except it does not divide tasks among PEs). As shown in FIG. **4**, all of the controllers are embodied in a single controller **200**, which may be just another processing element of the integrated circuit that contains the other processing elements. Each processing element also requires a calibration circuit like circuit **120**, and a voltage converter circuit like circuits **130** and **140**. It also has a PE **200** that assigns the tasks given to the multi-processor chip of FIG. **4** among the PEs.

Ex. 1009, 6:2-13



Ex. 1009, Fig. 4 (annotated)

Pet. at 35-37; Reply at 11-12

Nicol Also Teaches Clock Gating PEs

Of course, V_{dd}-local can only be reduced so-far before the circuits start to fail, at which point the operating system employs gated clocking techniques to "shut down" PEs that are not needed. Of course, the fact that supply voltage

Ex. 1009 at 5:42-45

Dr. Mangione-Smith

Q. […] A person of ordinary skill in the art reading Nicol would understand that, when a PE doesn't have a load on it, it should be put into some sort of low-voltage state that will minimize power consumption. Is that fair?

A. I think it's fair to say that in such a situation where there is no task running on a PE, a person would be inclined to put it in such a voltage state as to reduce the power consumption -- that would result in reducing the power consumption as much as they knew how to. Yeah.

Ex. 1051 at 52:5-17

Pet. at 37-38; Reply at 13-14

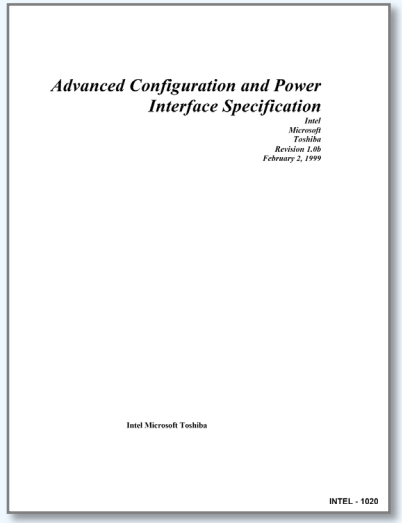
A POSITA Would Understand Reducing To A Minimum In Light of the ACPI Specification

Different types of power and thermal management techniques have been implemented in systems. A simple system includes a sensor that detects for an over-temperature condition and generates an interrupt to cause the computer system to shut down or otherwise go into a low power state (typically by deactivating components) when the over-temperature condition is detected. Another more sophisticated technique is defined by the Advanced Configuration and Power Interface (ACPI) Specification, Rev. 1.0, published on Dec. 22, 1996, that provides an interface between the operating system of a system and hardware devices to implement power and thermal management.

Ex. 1011, 1:6-17

Next, the power management module places (at **126**) the processor **12** into a low activity state (e.g., deep sleep, stop grant, C1, C2, or C3 state). In the deep sleep state, which may be the C3 state defined under the ACPI specification, the external clock BCLK to the processor is disabled so that no activity is performed by the processor except maintenance of the stored data in the processor's internal cache. In the stop grant or C2 state, the processor performs minimal activity, such as snooping for an internal cache line hit to maintain cache coherency. While the processor 12 is in the

Ex. 1011, 12:58-67


Advanced Configuration and Power Interface Specification
Intel
Microsoft
Toshiba
Revision 1.0b
February 2, 1999
Intel Microsoft Toshiba
INTEL - 1020

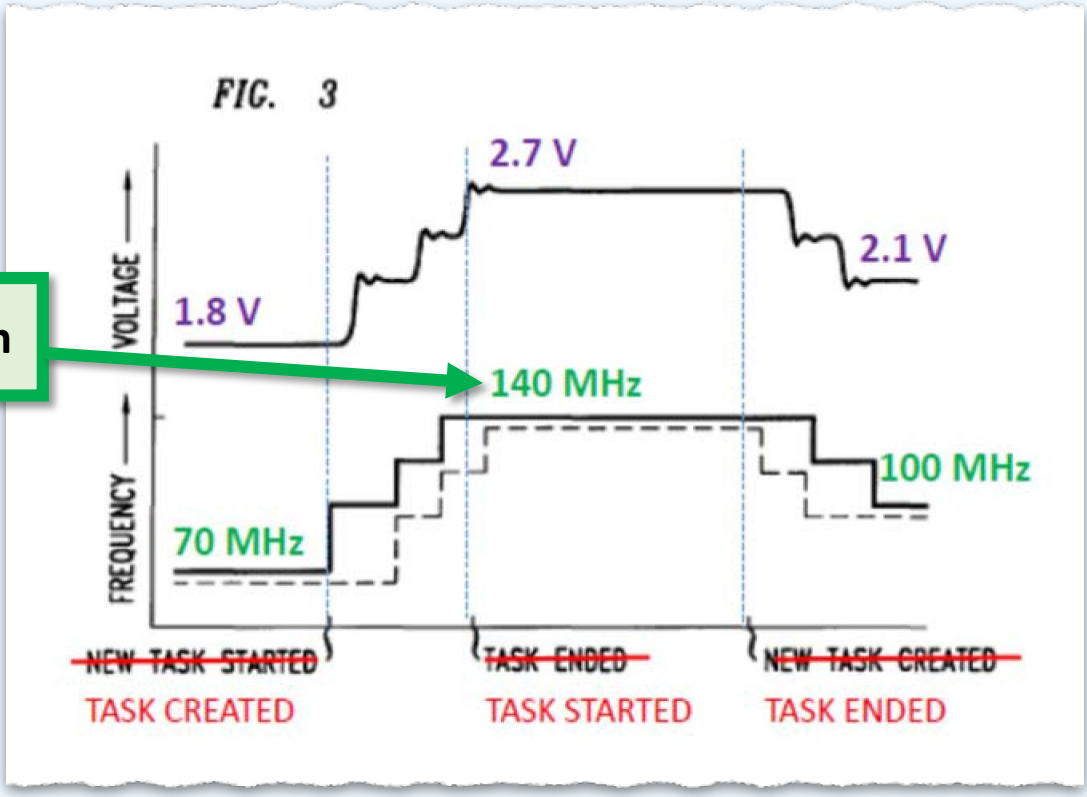
Ex. 1020

Pet. at 38

Nicol Teaches Increasing The Frequency To A Maximum

the multiprocessor system subsequently increasing the clock frequency of the at least the part of the multiprocessor system to a maximum in accordance with a number of pending operations of a second processor; and

Ex. 1003 at Claim 1



Maximum

Ex. 1009, Fig. 4 (annotated)

For a maximally utilized system, all of the available processors ought to be operating at full speed when satisfying the maximum load encountered by the system. At such a time, the power consumption of the multiprocessor chip is at its maximum level. However, as the load requirements are lowered, the system should, advantageously, reduce its power consumption. It may be noted that, typically, com-

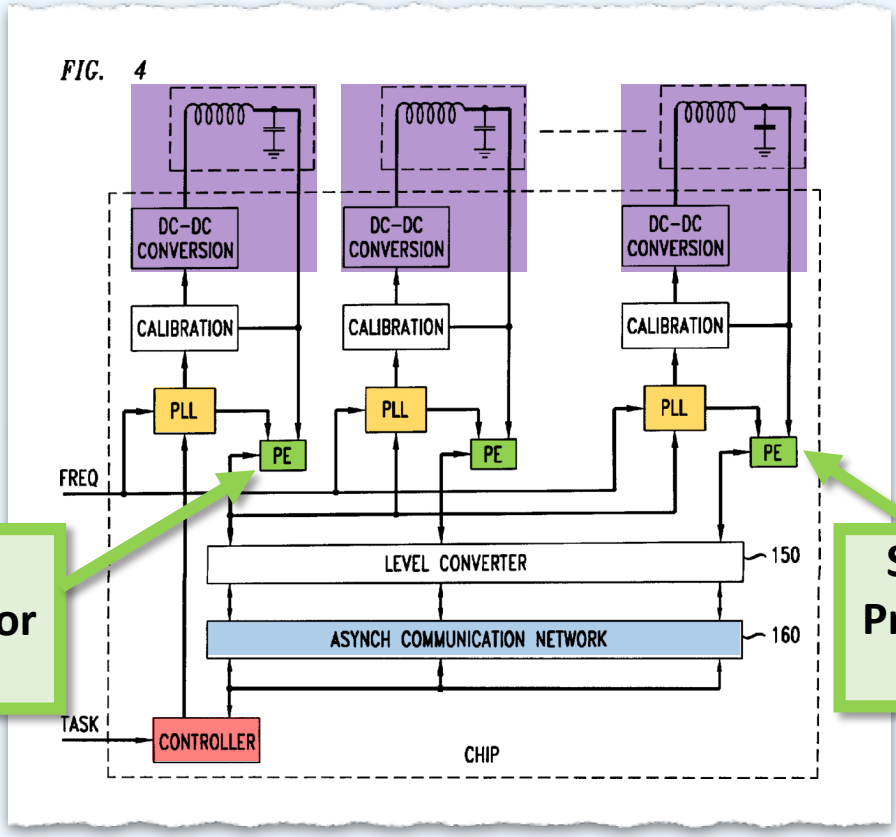
Ex. 1009, 2:65-3:4

Pet. at 39-41

One PE's Load Will Impact Load and Frequency Of Other PEs

The notion of adjusting operating frequency to load and adjusting supply voltage to track the operating frequency can be extended to allow each PE to have its own supply voltage. The benefit of this approach for some applications

Ex. 1009, 5:53-56



Ex. 1009 at Fig. 4 (annotated)

Dr. Mangione-Smith

Q. And so in that circumstance, the decision about -- assigning the task to PE 1 and increasing PE 1's frequency would be influenced by how loaded PE 2 and PE 3 are in our hypothetical; right?

A. It's – it's certainly possible with the load on the other PEs might be taken into account in allocating the tasks -- newly introduced tasks.

Ex. 1051 at 61:16-23

Pet. at 39-41; Reply at 16-17

PO's Expert Agrees That All PEs May Run At The Highest Clock Frequency

Dr. Mangione-Smith

Q. And on the -- now, let's switch to the flip side. There are circumstances in Figure 4 where all of the PEs were running at their absolute maximum frequency; is that right?

A. I think each of the PEs in Figure 4 has -- as they show its own -- their own independent power supply and dynamic voltage. It is hypothetically possible certainly that a particular load situation may cause them all to be running at their highest possible clock frequency and voltage.

Ex. 1051 at 54:2-14 (objections omitted)

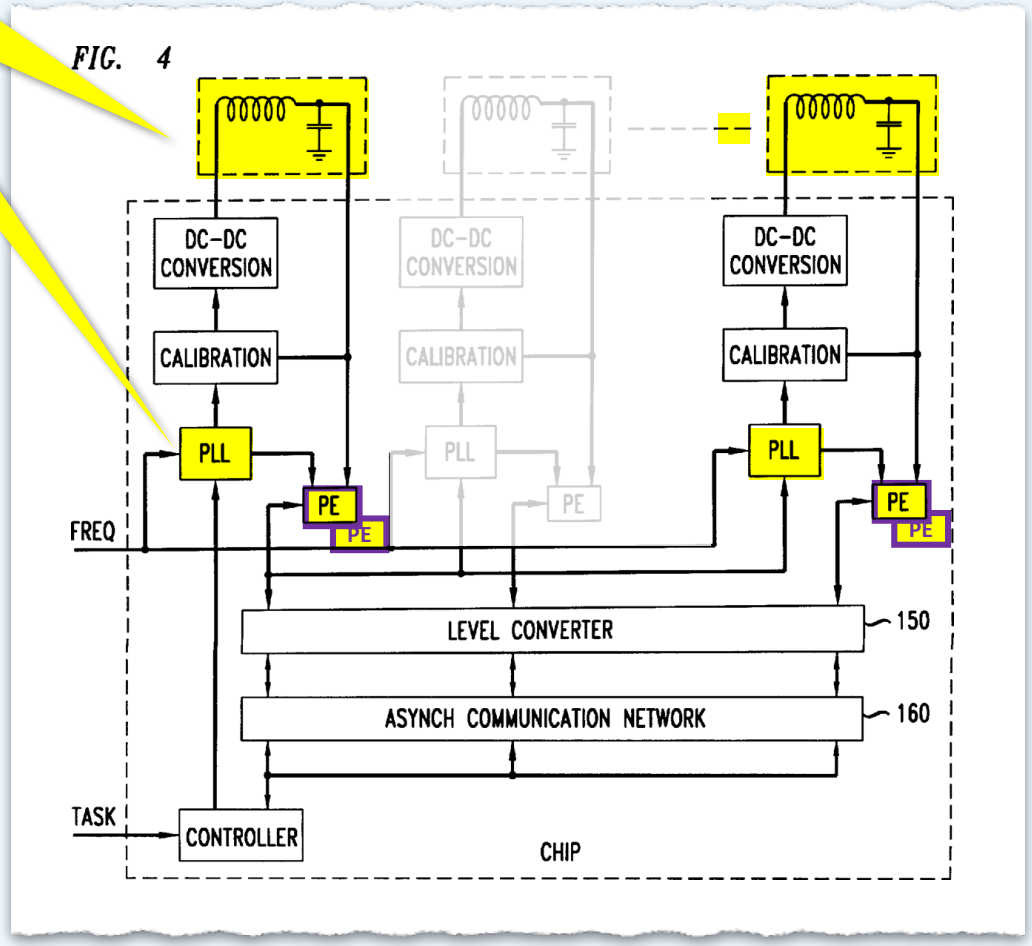
Reply at 19

Nicol Teaches Combining Figure 2 And Figure 4

Middle Ground:
Ability To Independently Set Frequency/Voltage for Groups of PEs

controlled, supply voltage. It should be realized, however, that a middle ground is also possible; i.e., the PEs of a multi-processor chip can be divided into groups, and each group of PEs can be arranged to operate from its own controlled supply voltage. To cite another example, the FIG.

Ex. 1009, 6:66-7:3



Ex. 1009 at Fig. 4 (annotated)

Pet. 39-41; Reply at 16, 18-19

PO's Expert

Dr. Mangione-Smith

Q. So if a PE is not the most heavily loaded PE in the gang, then its frequency will be set based on some other PE's load; right?

A. I think that that is largely consistent with what I said. In a sense that, you know, if there's a PE that is not the most heavily loaded one, its operating state will be set based on whatever the load is of the most heavily loaded PE.

Ex. 1051 at 69:7-16 (objections omitted)

Dr. Mangione-Smith

Q. And just so the record is clear, the situation you were just speaking about occurs in the middle ground embodiment as well as in Figure 2; is that right?

A. Yes. It's my understanding using the scant information that is provided, that what I am calling a gang in the middle ground would operate the same as the -- the system in Figure 2.

Ex. 1051 at 69:18-25

Reply at 19

PO's Expert

Dr. Mangione-Smith

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Ex. 1051 at 69:7-16 (objections omitted)

Reply at 21

Over-Temperature Protection Was Well-Known

the multiprocessor system subsequently reducing the clock frequency of the at least the part of the multiprocessor system in accordance with (a) an operating temperature threshold preventing over-temperature and (b) a hysteresis characteristic.

Ex. 1003 at Claim 1

Nicol

Voltage scaling as a function of temperature has been incorporated into the Intel Pentium product family as a technique to achieve high performance at varying operating temperatures and process corners. It is described in U.S. Pat. No. 5,440,520. The approach uses an on-chip temperature sensor and associated processing circuitry which issues a code to the off-chip power supply to provide a particular supply voltage. The process variation information is hard-

Ex. 1009 at 1:41-48

As indicated above, the operating system can reduce the supply voltage even further by tracking temperature and process variations. For example, when the chip is nominal in its characteristics, then it can be operated along line **20** of FIG. **1**, which calls for only 1.5V supply when operating at 70 MHz.

Ex. 1009 at 4:11-16

Kling

To address the thermal issue, elaborate thermal dissipation systems are often affixed to the processor to help dissipate the heat from the processor to the ambient environment. Some processor packages include a thermal sensor to monitor the temperature of the processor. If the processor temperature exceeds a particular threshold, the processor is placed into low power mode until it cools off. If these precautions are not taken, the processor may destroy itself by its own heat.

Ex. 1010, 1:38-46

Pet. at 42-43

Overview Of Kling

For one embodiment of the present invention, the upper limit is a constant value as shown in FIG. 2A. This constant value may be associated with an approximately maximum power that can be reliably consumed by the computer system from a power outlet into which the system is plugged before the outlet's fuse or circuit breaker trips. This value

Ex. 1010 at 5:20-25

Once the threshold is reached, the power controller sends a throttle signal to one or more ICs of the computer system.

Ex. 1010 at 5:38-40

ICs reduces its power consumption. For example, for one embodiment of the present invention, a processor of the computer system reduces its core frequency while maintaining a consistent bus frequency in response to receiving the throttle signal. For another embodiment, the processor stalls

Ex. 1010 at 2:48-51

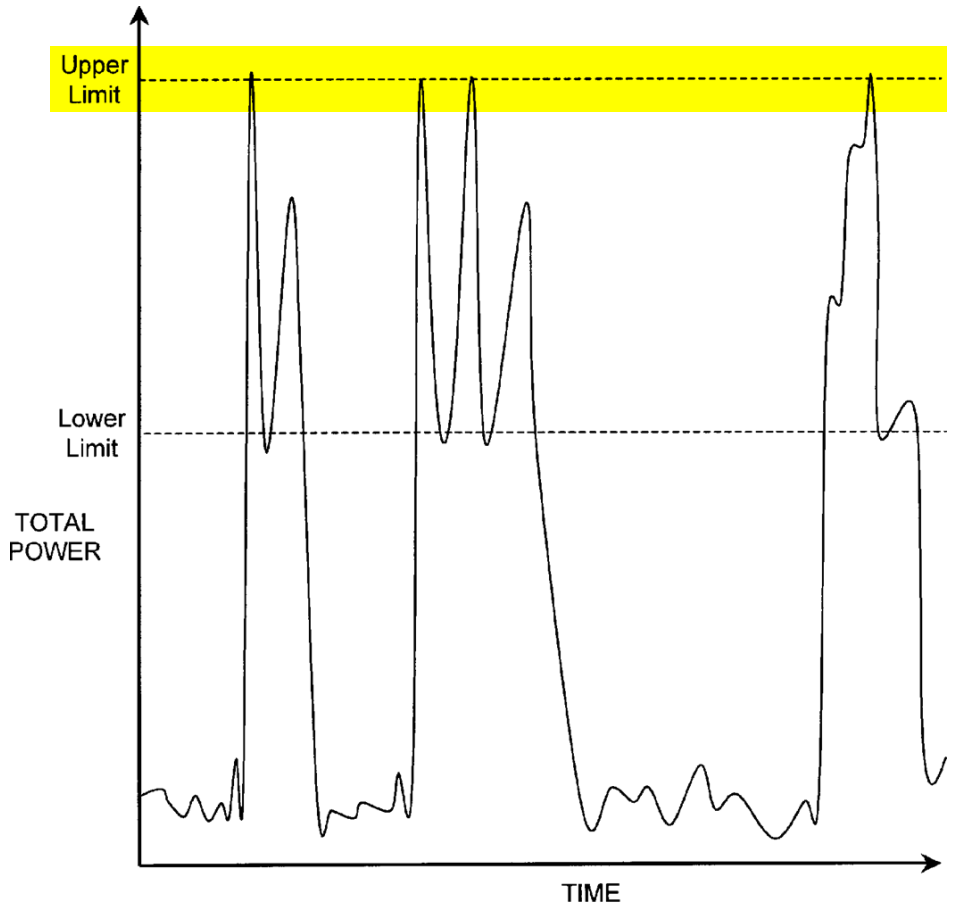


Figure 2A

Ex. 1010 at Figure 2A

Patent Owner's Expert Admits That Temperature Measurement and Temperature Sensors Were Well Known

Dr. Mangione-Smith

Q. [] So putting aside specifically where you would mount the temperature sensor, a person of ordinary skill in the art who was implementing Nicol but was concerned about overheating would at least know of ways that he could do temperature management using a temperature sensor somewhere near his chip; right?

A. Yeah. At least to the extent that the Pentium disclosed it, for example.

Ex. 1051 at 129:23-130:9 (objection omitted)

Reply at 20-21

Patent Owner's Expert Admits Thermal Management Was A Concern

Dr. Mangione-Smith

Q. So I think that at least we can agree, you know, at least in this section, Nicol isn't criticizing or discrediting thermal management as an -- as something that could be done here; is that right?

A. I think in this, the specific context of the discussion in chapter -- I'm sorry, in column 4, which I think is -- yeah, it exists in the context of figure 2. They are saying that thermal management may be a concern that you need to address and that perhaps you can address it somehow with what we are disclosing. I'm sorry, not -- perhaps you could use it in the context of what we are disclosing.

Ex. 1051 at 134:19-135:9 (objection omitted)

Reply at 5

Obvious To Apply Two-Threshold Method From Kling In An Over-Temperature Monitoring System in Nicol

tion. In accordance with this embodiment, the lower threshold may be set to a predetermined value selected to provide hysteresis to reduce the occurrence of power oscillation between the upper and lower thresholds. This lower thresh-

Ex. 1010 at 5:51-54

Dr. Mangione-Smith

Q. [ ]I think what we can agree on as part of what hysteresis is, is as we have talked about in the thermostat example. Using a two-level threshold band such as in a thermostat, that is an example of hysteresis?

A. I think that that's a good example of hysteresis writ large, yes.

Ex. 1051 at 138:2-12

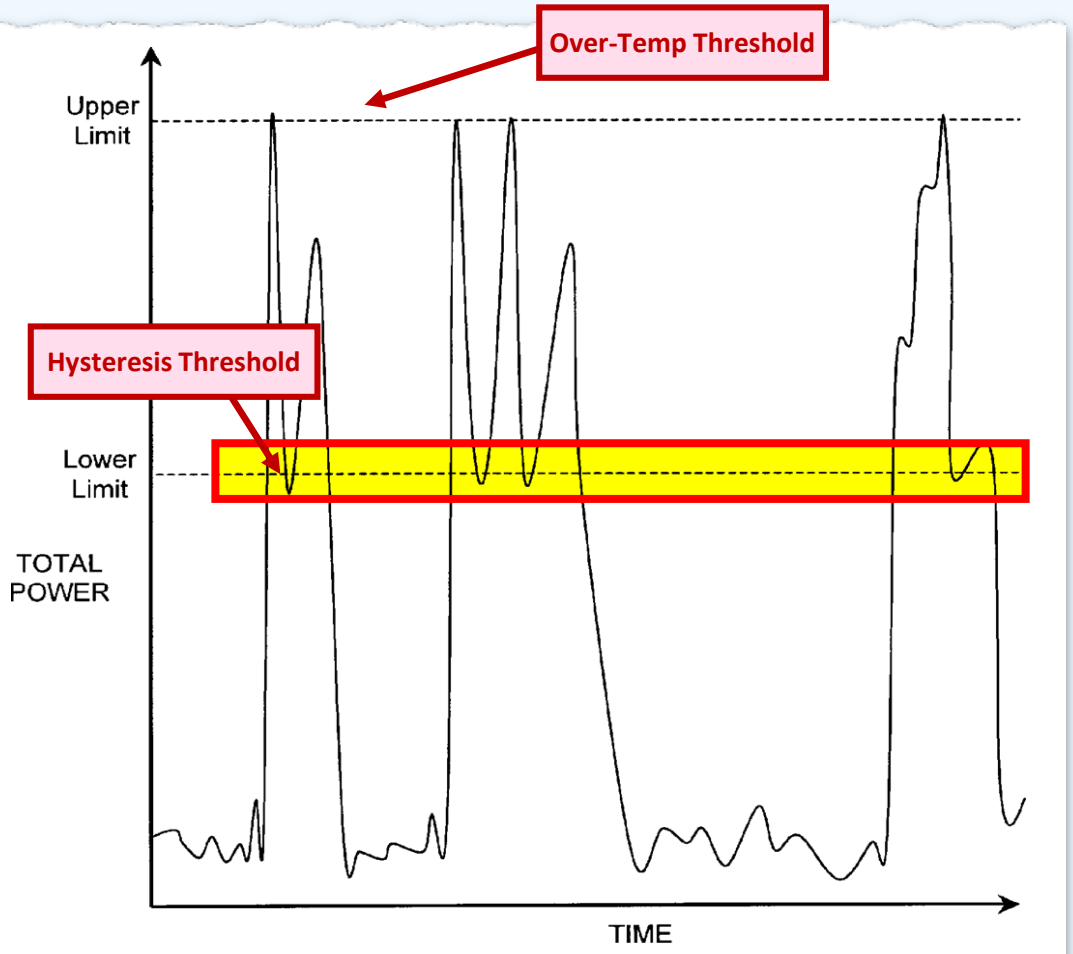


Figure 2A

Ex. 1010 at Figure 2A

Pet. at 44-45; Reply at 22

Obvious To Apply Two-Threshold Method From Kling In An Over-Temperature Monitoring System in Nicol

Thus, in my opinion, a POSITA would have found it obvious to apply the well-known two-threshold method (providing hysteresis) from Kling in implementing an over-temperature monitoring system in Nicol for the same well-known reason—to reduce unwanted oscillations.

Ex. 1001 at par. 192

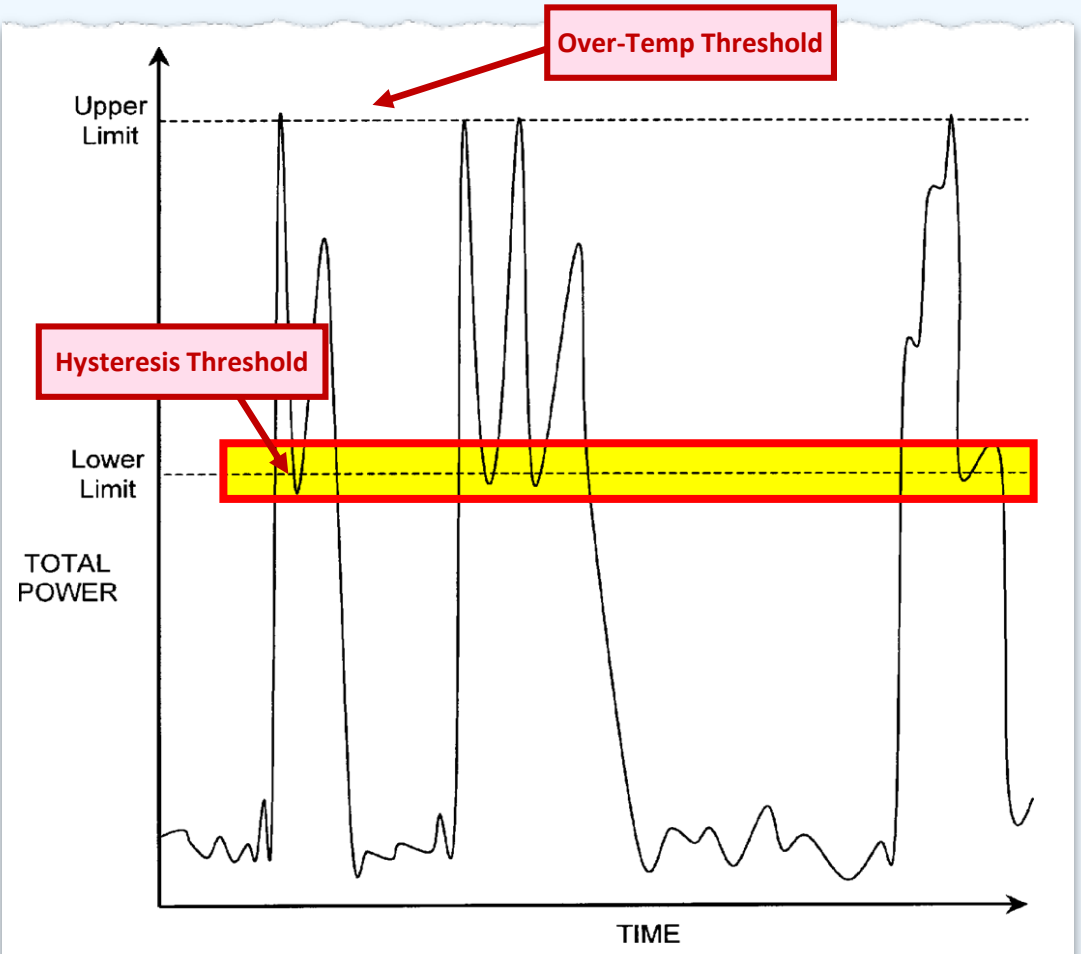


Figure 2A

Ex. 1010 at Figure 2A

Dr. Mangione-Smith

Q. [ ]I think what we can agree on as part of what hysteresis is, is as we have talked about in the thermostat example. Using a two-level threshold band such as in a thermostat, that is an example of hysteresis?

A. I think that that's a good example of hysteresis writ large, yes.

Ex. 1051 at 138:2-12

Pet. at 45; Reply at 21-22

Institution Decision

Patent Owner argues that Petitioner fails to establish that a person having ordinary skill in the art would have been motivated to combine Nicol with Kling. Prelim. Resp. 18–23. We have considered all of Patent Owner's arguments, but are not persuaded by them. For example, Patent Owner argues that the Petition is not supported by record evidence and fails to show that over-temperature control is critical or necessary. *Id.* at 22–23 (citing Pet. 42). The current record contains ample evidence that processors that overheat can and do fail. Ex. Ex. 1001 ¶¶ 50–53, 102; Ex. 1010, 1:25–26, 1:38–47. Indeed, Kling explains that if thermal monitoring is not included "the processor may destroy itself by its own heat." Ex. 1010, 1:42–47. Based on the current record before us, Petitioner's assertions, supported by record evidence, are reasonable and Patent Owner's arguments and evidence currently before us are not persuasive to the contrary.

Institution Decision at 28

Using Hysteresis With Temperature Is A Well-Known Example

PACT Sur-Reply

These admissions raise the question under *ParkerVision, i.e.*, "why a person of ordinary skill in the art would have been motivated to [create conditions] that would result in such [**reduction in clock frequency according to both** an operating temperature threshold and a hysteresis threshold]"? No evidence shows such a motivation.

PO Sur-Reply at 2

605 File History

The patents discloses a clock frequency set in accordance with a hysteresis characteristic (page 28 line 28 through page 29 line 11) where one of ordinary skill in the art would understand that the frequency can be set in accordance with, for instance, a temperature.

Pet. at 9-10

Ex. 1004 at 379

Patent Owner's Expert Admits That Nicol Teaches Sequentially Processing Data

Claim 1

1. A method for operating a multiprocessor system comprising a plurality of data processing cells, each of the plurality of data processing units (a) including at least one Arithmetic Logic Unit (ALU) and a register unit and (b) being adapted for sequentially processing data, the method comprising:

the multiprocessor system setting a clock frequency, of at least a part of the multiprocessor system to a minimum in accordance with a number of pending operations of a first processor;

the multiprocessor system subsequently increasing the clock frequency of the at least the part of the multiprocessor system to a maximum in accordance with a number of pending operations of a second processor; and

the multiprocessor system subsequently reducing the clock frequency of the at least the part of the multiprocessor system in accordance with (a) an operating temperature threshold preventing over-temperature and (b) a hysteresis characteristic.

Ex. 1003 at Claim 1

PACT Construction

passing results onto one or more other data processing units which are subsequently processing data

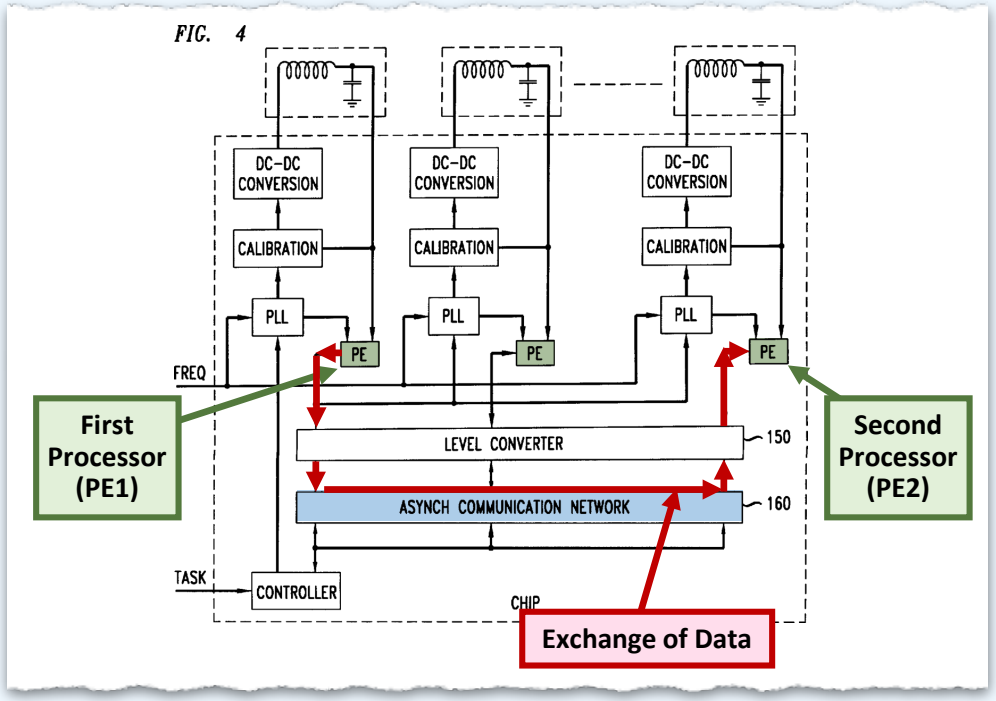
Pet. at 30-34; Reply at 9-10 *Ex. 1016 at 10, 14*

Dr. Mangione-Smith

Q. You're saying that in the instances that Nicol described, so you have to take one task and try to break it up into multiple subtasks to divide across multiple PEs, there's almost always going to have to be communication between those individual PEs about what they're working on; right?

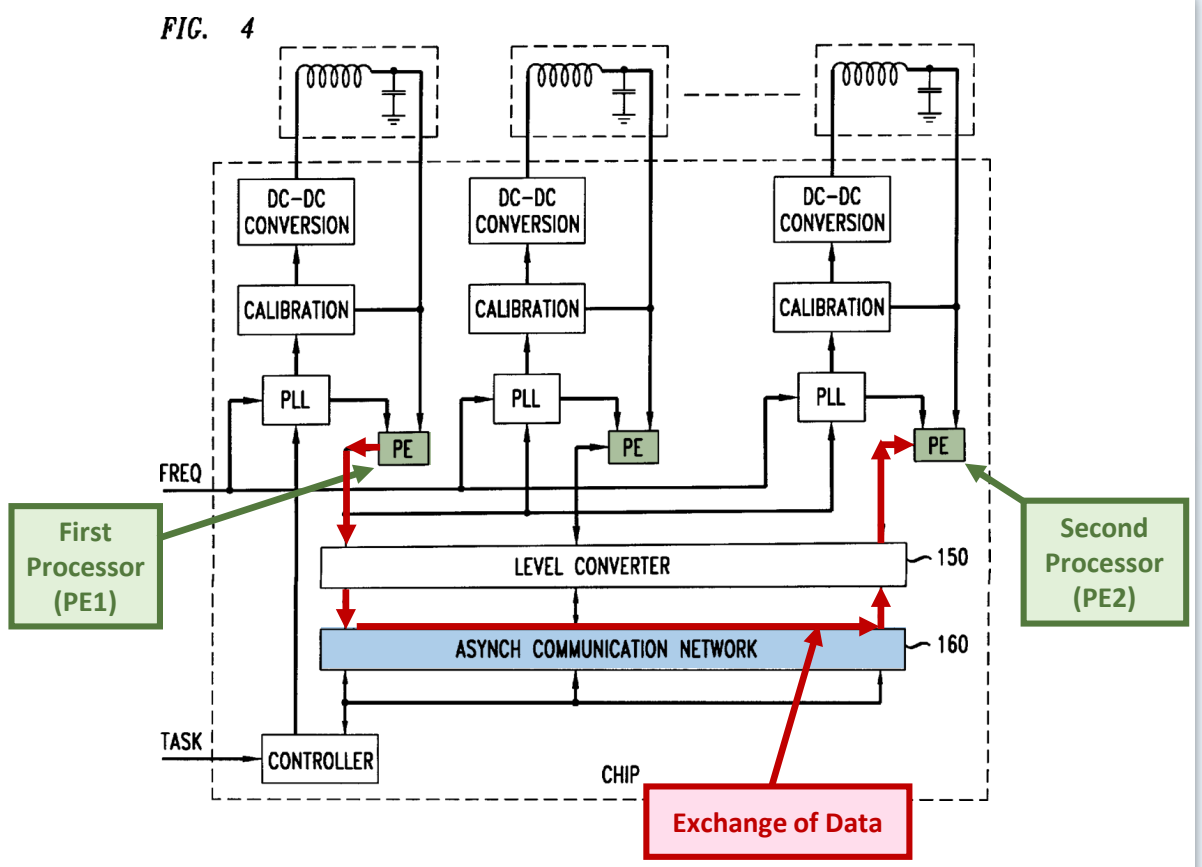
A. Yeah. Only because in general if the two subtasks are completely separate they probably would have been their own separate tasks to begin with. That's my reasoning there. I don't recall -- yeah, so I'll stay with that.

Ex. 1052 at 60:20-61:9 (objections omitted)



Ex. 1009 at Fig. 4 (annotated)

Nicol Teaches Sequentially Processing Data



Ex. 1009, Fig. 4 (annotated)

It may be noted that if the frequencies at which the individual PEs operate differ from one another and from other elements within the system where the multiprocessor chip is employed, there is an issue of synchronization that must be addressed. That is, a synchronization schema must be implemented when there is a need to communicate data between PEs (or with other system elements) that operate at different frequencies. It is possible to arrange the frequencies so that the collection of tasks that are assigned to the multiprocessor is completed at a predetermined time. In such a case, the synchronization problem of the multiprocessor vis-a-vis other elements within the system where the multiprocessor is employed is minimized. However, that leaves the issue of synchronizing the exchange of data among the PEs of a multiprocessor chip.

To effect such synchronization, each PE within the FIG. **4** arrangement is connection to an arrangement comprising elements **150** and **160**. Level converter **150** converts the variable voltage swings of the PEs to a fixed level swing, and network **160** resolves the issue of different clock domains.

Ex. 1009 at 6:14-33

Pet. at 30-32

Kling Teaches Clock Frequency Determined In Part By Processor Voltage

2. The method of claim **1** wherein:
said clock frequency is determined in part by processor voltage.

Ex. 1003 at Claim 2

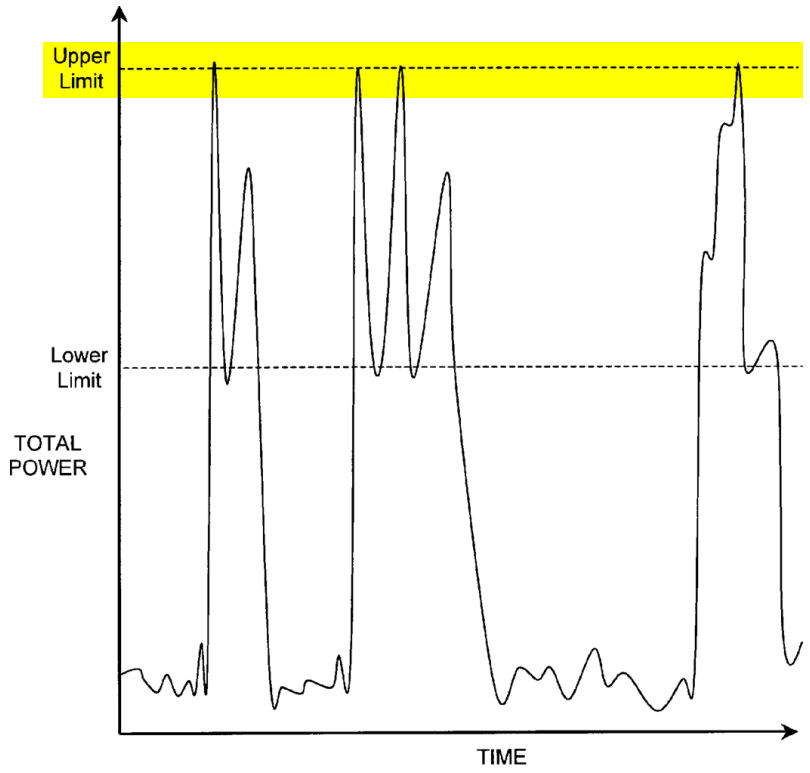


Figure 2A

Once the consumed power, as determined by the power controller, reaches a threshold, a throttle signal is sent to one or more ICs of the computer system by the controller. In response to receiving this throttle signal, one or more of the ICs reduces its power consumption. For example, for one embodiment of the present invention, a processor of the computer system reduces its core frequency while maintaining a consistent bus frequency in response to receiving the throttle signal. For another embodiment, the processor stalls all or a portion of one or more pipelines, or issues no-ops to one or more pipelines, in response to receiving the throttle signal.

Ex. 1010 at 2:43-54

In accordance with an embodiment of the present invention, the power consumed by at least a portion of a computer system is monitored by measuring a parameter that is approximately proportional to the consumed power, such as voltage, current, or the duty cycle of a switching signal in a power supply. These measurements are provided

Ex. 1010 at 2:31-37

Pet. at 46-47, Reply at 22

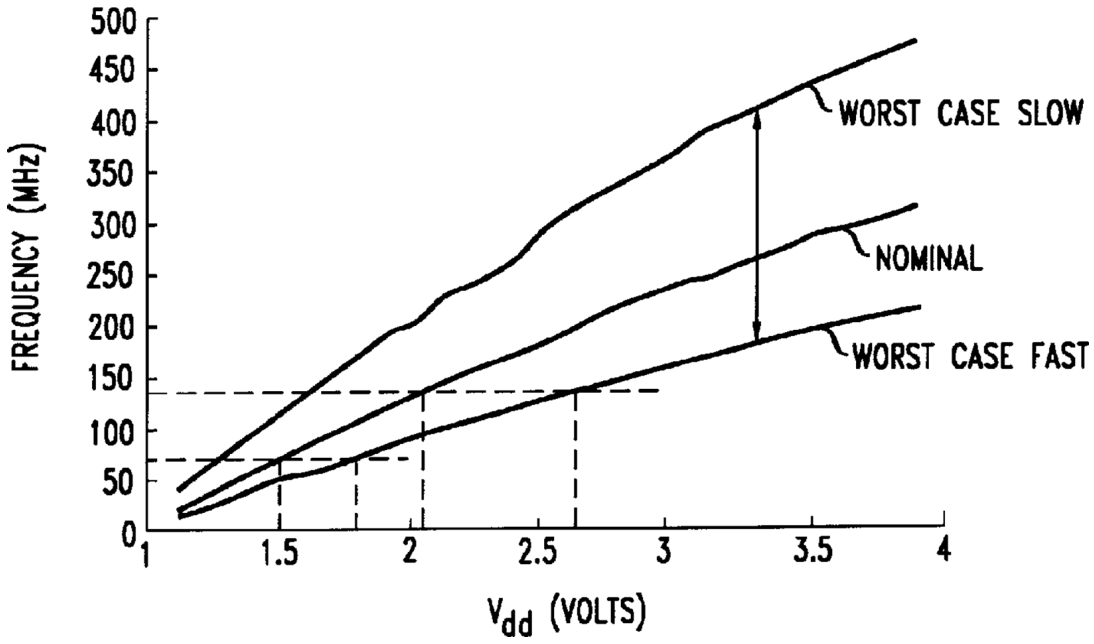
Ex. 1010 at Figure 2A

Nicol Teaches Clock Frequency Determined In Part By Processor Voltage

2. The method of claim 1 wherein:
said clock frequency is determined in part by processor voltage.

Ex. 1003 at Claim 2

FIG. 1



Ex. 1009 at Fig. 1

FIG. 1 illustrates the maximum operating frequency that is achievable with a 0.35 μm technology CMOS chip as a function of supply voltage;

Ex. 1009 at 2:34-36

Pet. at 46; Reply at 22-24

Patent Owner States That Kling Sets A Voltage Limit For Determining Frequency

5:22-25 (emphasis added). With this full context, Kling is properly understood to describe a system that sets its own voltage limit that is reliably below a maximum voltage that can be supplied before an outlet fuse is tripped. Ex. 2024, ¶73. Kling is

POR at 48

be determined, in part, by the available power. Petitioner points to a static upper voltage limit as the available power upon which the clock frequency depends, but if the amount of available power is static and doesn't change, it cannot determine all of these frequencies, which can vary during operation. Pet., 47; Ex. 2024, ¶74.

POR at 49

Patent Owner's Expert Agrees That Kling Discloses Upper Limit Of Maximum Power

3. The method of claim 1 wherein:
said clock frequency is determined in part by available power.

Ex. 1003 at Claim 3

For one embodiment of the present invention, the upper limit is a constant value as shown in FIG. 2A. This constant value may be associated with an approximately maximum power that can be reliably consumed by the computer system from a power outlet into which the system is plugged before the outlet's fuse or circuit breaker trips. This value

Ex. 1010 at 5:20-25

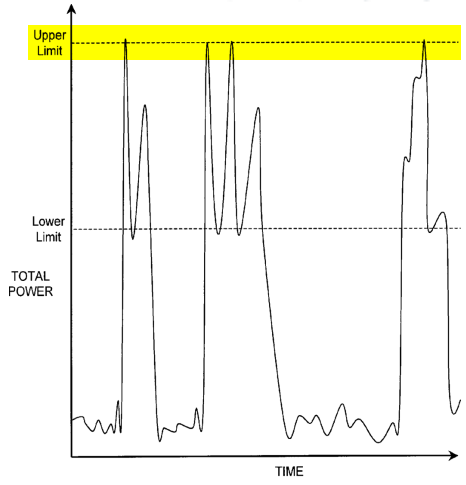


Figure 2A

Ex. 1010 at Figure 2A

Dr. Mangione-Smith

Q. And -- and that upper threshold that is being set there is really sort of saying "this is the maximum available power that I – that's available for you to use"; is that right?

A. Yes. That's how I interpret it.

Q. And then it makes decisions based on what the clock frequency should be based on that available power?

A. It makes decisions based in part on -- yes, what that upper limit is.

Ex. 1051 at 150:3-13 (objections omitted)

Pet. at 47, Reply at 24-25

No Dispute That Kling's Upper And Lower Frequency Thresholds Are Set By A User Setting

4. The method of claim **1** wherein:
said clock frequency is determined in part by a user setting.

Ex. 1003 at Claim 4

system, typically the processors. The upper threshold set in the power controller is shown as the upper limit line in the graph of FIG. **2A**. This threshold may be permanently set within the power controller or may be modifiable by the system designer or system user via software or hardware control.

Ex. 1010 at 5:14-19

Dr. Mangione-Smith

Q. There you go. Okay. So -- so the-- in the Kling reference, the upper and lower threshold may -- may both be set by a user setting; right?

A. That's my understanding from what they disclosed. Yes.

Ex. 1051 at 152:17-22

Reply at 25

No Dispute That Kling Determines Clock Frequency Both By Available Power and A User Setting

5. The method of claim **1** wherein:
said clock frequency is determined in part by available power and a user setting.

Ex. 1003 at Claim 5

Kling Claim 12

12. The method of claim **11**, further comprising determining if the calculation reaches a threshold that is predetermined to be a user-defined value associated with the power delivery specification of the outlet into which the computer system is plugged.

Ex. 1010 at Claim 12

Dr. Mangione-Smith

Q. And in particular to a user defined value associated with that wall socket's available power in claim 12?

A. Well, they certainly do disclose that at least in claim 12. I don't recall if they do it elsewhere in the specification.

Ex. 1051 at 156:2-8 (objections omitted)

Reply at 26

Nicol Discloses A Local Cache Memory That Stores Pending Instructions

6. The method of claim 1 wherein:
said number of pending operations is determined at by the fill level of one or more buffers.

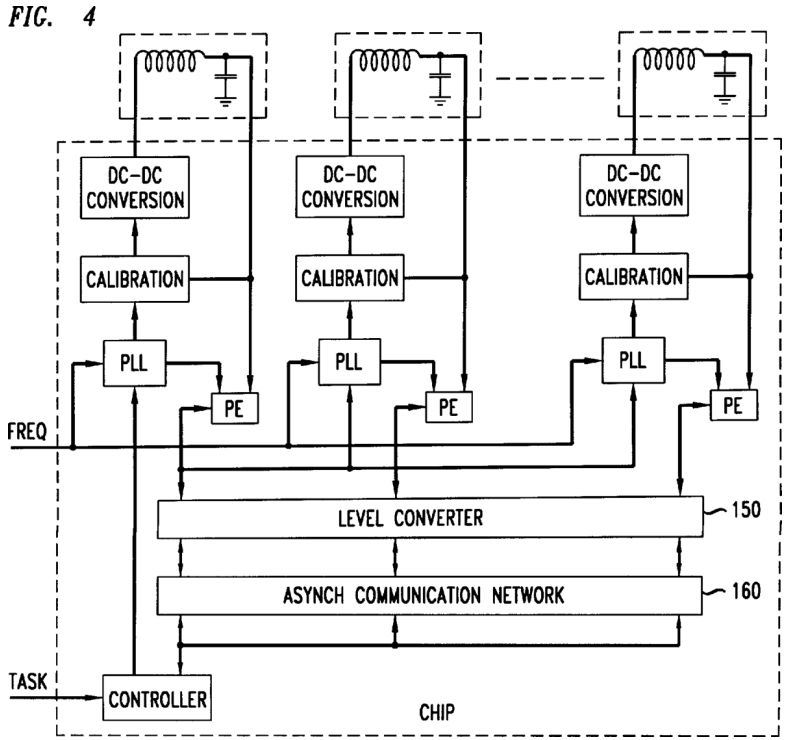
Ex. 1003 at Claim 6

FIG. 2 depicts a block diagram of a multi-processor chip. It contains processing elements (PEs) **100**, **101**, **102**, **103**, . . . **104**, and each PE contains a central processing unit (CPU) and a local cache memory (not shown). A real-time

Ex. 1009 at 2:50-53

time operating system (RTOS) executed on PE **100**. If the number of instructions that need to be executed for each task is known and made available to the operating system, a scheduler within the operating system can use this information to determine the best way to allocate the tasks to the available processors in order to balance the computation.

Ex. 1009 at 3:13-18



Ex. 1009 at Fig. 4

Pet at 51-52, Reply at 26-27

Patent Owner Statements To Examiner

Applicant respectfully traverses. First applicant believes that the examiners rejection is to the use of "load" in the claims. The specification discloses a clock frequency set in accordance with a processor load (page 14 line 23 through page 15 line 9) where one of ordinary skill in the art would understand that the fill level of a data buffer representative of the number of waiting operations or processor load.

Ex. 1004 at 376-77

Pet at 51-52, Reply at 26-27

Nicol And Kling

Nicol

US006141762A

United States Patent [19]
Nicol et al.

[11] **Patent Number: 6,141,762**
[45] **Date of Patent: Oct. 31, 2000**

[54] **POWER REDUCTION IN A MULTIPROCESSOR DIGITAL SIGNAL PROCESSOR BASED ON PROCESSOR LOAD**

[76] Inventors: **Christopher J. Nicol**, 61 Hubbard Ave., Red Bank, N.J. 07701; **Kanwar Jit Singh**, 23 Kerry Dr., Hazlet, N.J. 07730

[21] Appl. No.: **09/128,030**

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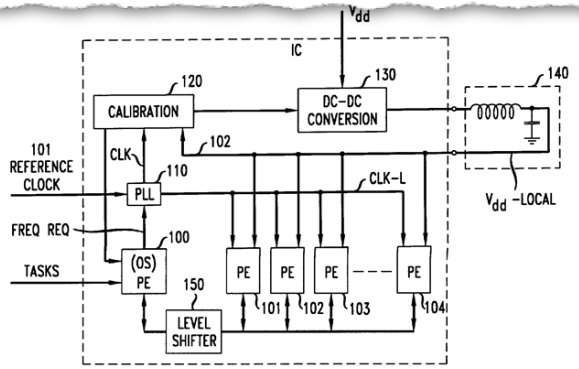
Primary Examiner—Gopal C. Ray
Attorney, Agent, or Firm—Henry T Brendzel

[57] **ABSTRACT**

Improved operation of multi-processor chips is achieved by dynamically controlling processing load of chips and

POWER REDUCTION IN A MULTIPROCESSOR DIGITAL SIGNAL PROCESSOR BASED ON PROCESSOR LOAD



INTEL - 1006

Ex. 1009

Kling

US006367023B2

(12) **United States Patent**
Kling et al.

(10) **Patent No.: US 6,367,023 B2**
(45) **Date of Patent: Apr. 2, 2002**

(54) **METHOD AND APPARATUS OF MEASURING CURRENT, VOLTAGE, OR DUTY CYCLE OF A POWER SUPPLY TO MANAGE POWER CONSUMPTION IN A COMPUTER SYSTEM**

(75) Inventors: **Ralph M. Kling**, Sunnyvale; **Edward T. Grochowski**, San Jose, both of CA

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METHOD AND APPARATUS OF MEASURING CURRENT, VOLTAGE, OR DUTY CYCLE OF A POWER SUPPLY TO MANAGE POWER CONSUMPTION IN A COMPUTER SYSTEM

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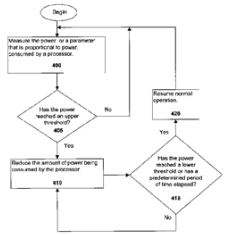
threshold, and if so, the controller sends a throttle signal. A system and method such as this may be found useful to reduce the risk of a computer system blowing a fuse or tripping a circuit breaker.

23 Claims, 9 Drawing Sheets

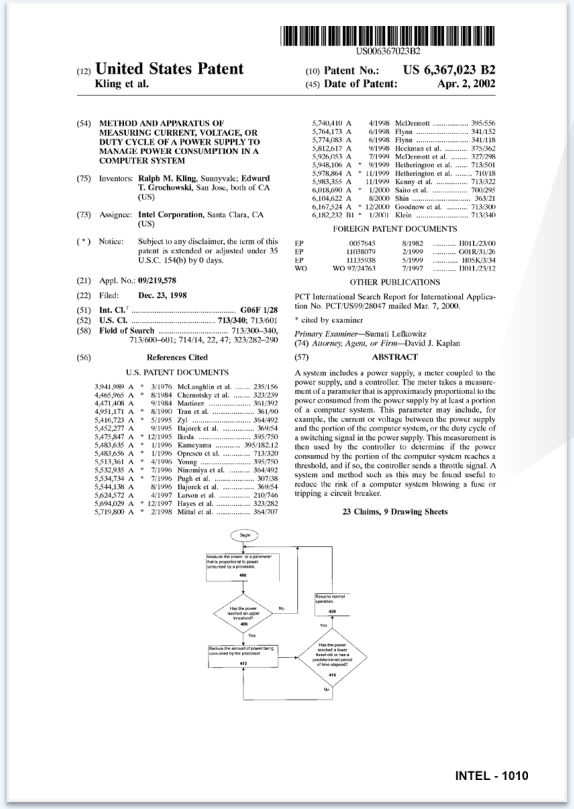


INTEL - 1010

Ex. 1010

Overview Of Kling

Patent No.: US 6,367,023 B2



US006367023B2

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(75) Inventors: **Ralph M. Kling**, Sunnyvale; **Edward T. Grochowski**, San Jose, both of CA (US)

(73) Assignee: **Intel Corporation**, Santa Clara, CA (US)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/219,578**

(22) Filed: **Dec. 23, 1998**

(51) **Int. Cl.**[7] **G06F 1/28**

(52) **U.S. Cl.** **713/340**; 713/601

(58) **Field of Search** 713/300-340, 713/600-601; 714/14, 22, 47; 323/282-290

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Primary Examiner—Sumati Lefkowitz
(74) *Attorney, Agent, or Firm*—David J. Kaplan

(57) **ABSTRACT**

A system includes a power supply, a meter coupled to the power supply, and a controller. The meter takes a measurement of a parameter that is approximately proportional to the power consumed from the power supply by at least a portion of a computer system. This parameter may include, for example, the current or voltage between the power supply and the portion of the computer system, or the duty cycle of a switching signal in the power supply. This measurement is then used by the controller to determine if the power consumed by the portion of the computer system reaches a threshold, and if so, the controller sends a throttle signal. A system and method such as this may be found useful to reduce the risk of a computer system blowing a fuse or tripping a circuit breaker.

23 Claims, 9 Drawing Sheets

INTEL - 1010

Ex. 1010

A system includes a power supply, a meter coupled to the power supply, and a controller. The meter takes a measurement of a parameter that is approximately proportional to the power consumed from the power supply by at least a portion of a computer system. This parameter may include, for example, the current or voltage between the power supply and the portion of the computer system, or the duty cycle of a switching signal in the power supply. This measurement is then used by the controller to determine if the power consumed by the portion of the computer system reaches a threshold, and if so, the controller sends a throttle signal. A system and method such as this may be found useful to reduce the risk of a computer system blowing a fuse or tripping a circuit breaker.

Ex. 1010 at Abstract

FIG. 1 is a multiprocessor computer system formed in accordance with an embodiment of the present invention. Primary bridge **110** is coupled to processors **100** and **101** via a system bus. Bridge **110** is used to couple the processors to main memory **115** and to couple the processors to peripheral components **120** and **130** via a peripheral bus. Secondary bridge **125** couples external memory **140** and video terminal **145** to the peripheral bus.

Ex. 1010 at 2:65-3:5

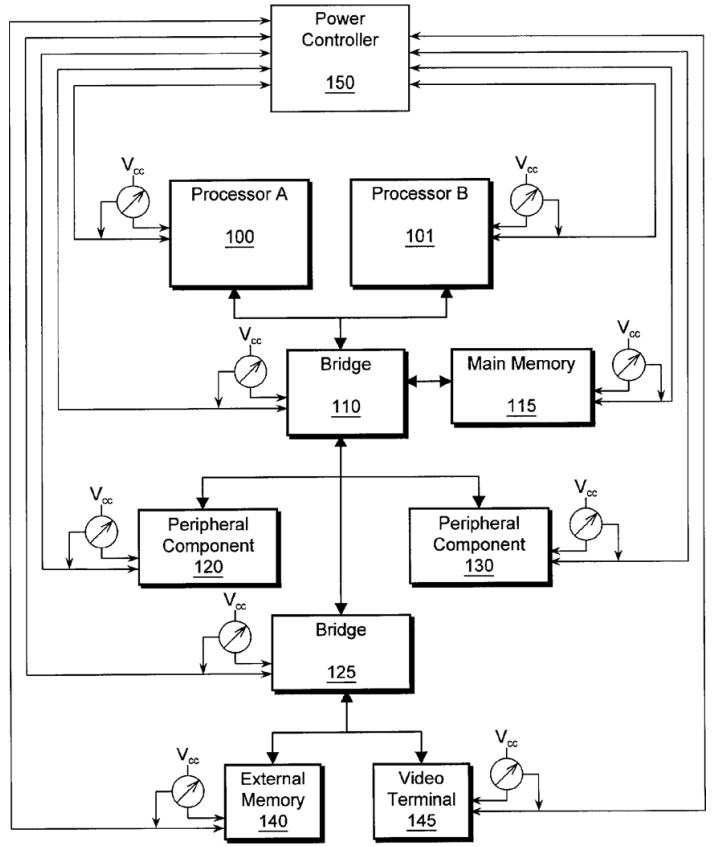


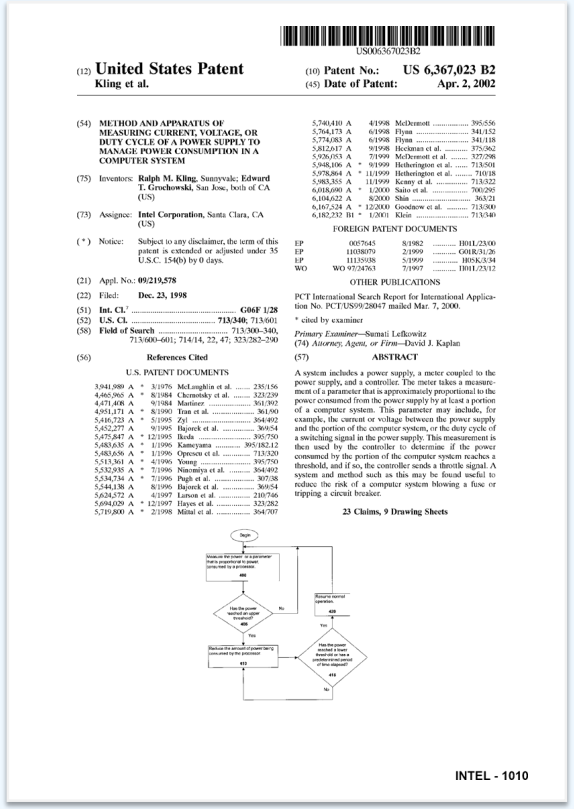
Figure 1

Ex. 1010 at Fig. 1

Pet. at 16-18

Overview Of Kling

Patent No.: US 6,367,023 B2



US006367023B2

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Kling et al.

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(45) **Date of Patent: Apr. 2, 2002**

(54) **METHOD AND APPARATUS OF MEASURING CURRENT, VOLTAGE, OR DUTY CYCLE OF A POWER SUPPLY TO MANAGE POWER CONSUMPTION IN A COMPUTER SYSTEM**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

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(51) **Int. Cl.**[7] **G06F 1/28**

(52) **U.S. Cl.** **713/340**; 713/601

(58) **Field of Search** 713/300-340, 713/600-601; 714/14, 22, 47; 323/283-290

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(57) **ABSTRACT**

A system includes a power supply, a meter coupled to the power supply, and a controller. The meter takes a measurement of a parameter that is approximately proportional to the power consumed from the power supply by at least a portion of a computer system. This parameter may include, for example, the current or voltage between the power supply and the portion of the computer system, or the duty cycle of a switching signal in the power supply. This measurement is then used by the controller to determine if the power consumed by the portion of the computer system reaches a threshold, and if so, the controller sends a throttle signal. A system and method such as this may be found useful to reduce the risk of a computer system blowing a fuse or tripping a circuit breaker.

23 Claims, 9 Drawing Sheets

INTEL - 1010

Ex. 1010

the computer system. If the total power consumed reaches a threshold, or if the total of a value that is proportional to the total power consumed reaches a threshold, controller **150** sends a throttle signal to one or more ICs of the computer system. In response to receiving a throttle signal, an IC reduces its power consumption. Note that for simplicity, as used henceforth, the term "power" includes either actual power or a value, such as current, voltage, duty cycle, or other measurement, that is proportional to power.

The ICs that receive the throttle signal and, in turn, reduce their power consumption, may be selected by power controller **150** of FIG. **1** in any of a number of different ways.

Ex. 1010 at 4:50-5:8

or more ICs of the computer system by the controller. In response to receiving this throttle signal, one or more of the ICs reduces its power consumption. For example, for one embodiment of the present invention, a processor of the computer system reduces its core frequency while maintaining a consistent bus frequency in response to receiving the throttle signal. For another embodiment, the processor stalls

Ex. 1010 at 2:45-51

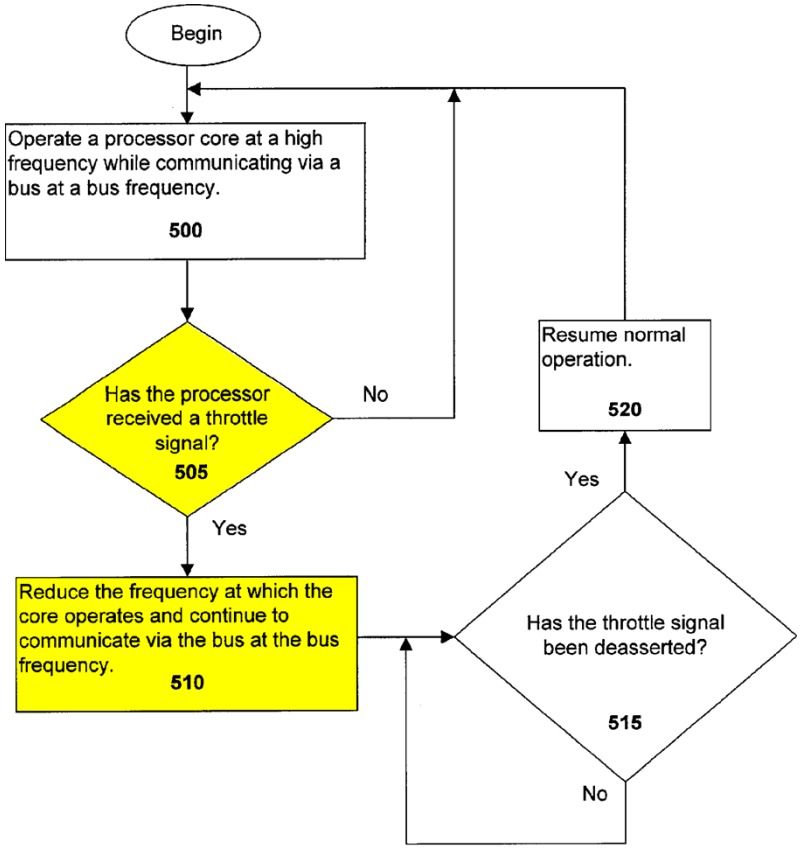


Figure 5

Ex. 1009, Fig. 5 (annotated)

Pet. at 16-18

Overview Of Kling

For one embodiment of the present invention, the upper limit is a constant value as shown in FIG. 2A. This constant value may be associated with an approximately maximum power that can be reliably consumed by the computer system from a power outlet into which the system is plugged before the outlet's fuse or circuit breaker trips. This value

Ex. 1010 at 5:20-25

Once the threshold is reached, the power controller sends a throttle signal to one or more ICs of the computer system.

Ex. 1010 at 5:38-40

ICs reduces its power consumption. For example, for one embodiment of the present invention, a processor of the computer system reduces its core frequency while maintaining a consistent bus frequency in response to receiving the throttle signal. For another embodiment, the processor stalls

Ex. 1010 at 2:48-51

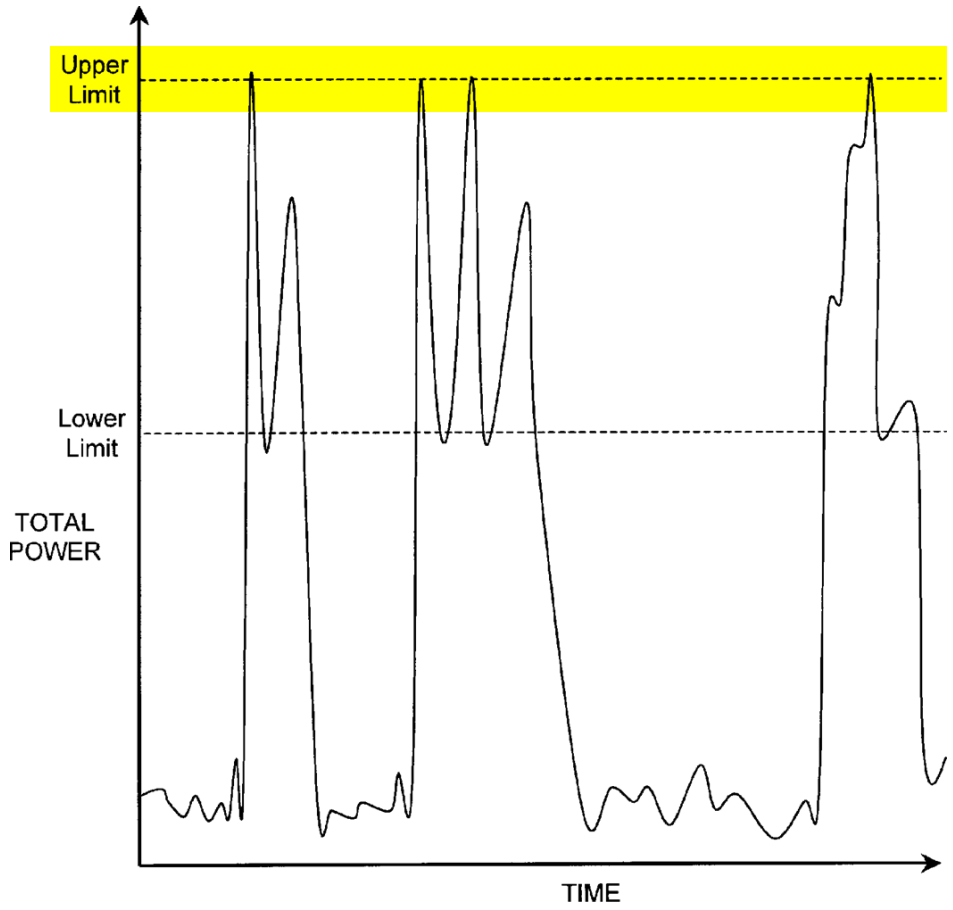


Figure 2A

Ex. 1010 at Figure 2A

Pet. at 16-18, 25, 44, 48

POSITA Would Have Been Motivated To Combine Nicol And Kling

Nicol

POWER REDUCTION IN A MULTIPROCESSOR DIGITAL SIGNAL PROCESSOR BASED ON PROCESSOR LOAD

Ex. 1009 at Title

Improved performance of multi-processor chips is achieved by dynamically controlling the processing load of chips and controlling, which significantly greater than on/off granularity, the operating voltages of those chips so as to minimize overall power consumption. A controller in a multi-processor chip allocates tasks to the individual processors to equalize processing load among the chips, then the controller lowers the clock frequency on the chip to as low a level as possible while assuring proper operation, and finally reduces the supply voltage. Further improvement is

Ex. 1009 at 2:18-27

Kling

METHOD AND APPARATUS OF MEASURING CURRENT, VOLTAGE, OR DUTY CYCLE OF A POWER SUPPLY TO MANAGE POWER CONSUMPTION IN A COMPUTER SYSTEM

Ex. 1010 atTitle

The present invention relates to computer systems and more particularly to limiting the power consumed in a computer system by throttling the power consumed by an integrated circuit in response to a high power condition.

Ex. 1010 at 1:7-10

Pet. at 23-24

POSITA Would Have Been Motivated To Combine Nicol And Kling

Nicol

In the FIG. **2** arrangement, in accordance with the principles disclosed herein, the applications that need to be processed are mapped to the N PEs under control of real time operating system (RTOS) executed on PE **100**. If the number of instructions that need to be executed for each task is known and made available to the operating system, a scheduler within the operating system can use this information to determine the best way to allocate the tasks to the available processors in order to balance the computation. The intermediate goal, of course, is to maximize the parallelism and to evenly distribute the load presented to the FIG. **2** system among all of the PE's.

Ex. 1009 at 3:9-20

Kling

One or more of the meters of the computer system of FIG. **1** monitor power consumption by measuring a parameter that is approximately proportional to the power consumed by one or more ICs. These measurements are then provided to power controller **150**. For example, a meter may measure power, current, or voltage. Current consumption may be measured magnetically by, for example, hall-effect sensors that measure induction. Alternatively, the voltage drop

Ex. 1010 at 3:50-57

Once the threshold is reached, the power controller sends a throttle signal to one or more ICs of the computer system. When an IC reduces its power consumption in response to the throttle signal, the total power consumption, as calculated by the power controller, is reduced as shown in FIG. **2A**.

For the embodiment of FIG. **2A**, once triggered, the throttle signal is continually asserted until the total power consumption, as calculated by the power controller, reaches the lower threshold indicated by the lower limit line. Once this lower threshold is reached, the throttle signal may be deasserted, and, in response, the IC resumes normal operation. In accordance with this embodiment, the lower threshold may be set to a predetermined value selected to provide hysteresis to reduce the occurrence of power oscillation between the upper and lower thresholds. This lower threshold may be hard wired into the power controller or hard wired into the IC that receives the throttle signal. Alternatively, the lower threshold may be modifiable by a user or automatically adjusted within the computer system to, for example, reduce power oscillation.

Ex. 1010 at 5:39-59

Pet. at 23-25

POSITA Would Have Been Motivated To Combine Nicol And Kling

129. In my opinion, a POSITA would have been motivated to implement this functionality in Nicol's system for over-temperature protection and, more generally, to detect excessive power consumption and reduce it, which is consistent with Nicol's objective of minimizing power consumption. Nicol, 2:18-22. Implementing this added functionality presents no risk, and does not require undue experimentation, has a good likelihood of success, and would yield predictable results because the added functionality is primarily add-on software to Nicol's existing controller software. *Id.*, 3:9-20

Ex. 1001 at ¶ 129

Patent Owner's Response

2024, ¶83. Petitioner makes no attempt to explain how a system combining Nicol and Kling would function, likely due to the fact that managing a plurality of metrics to create an efficient processing system is extremely difficult. *Id*. A POSITA might spend their entire career developing intricate systems for managing processor temperature and clock frequency among a plurality of processors, and Petitioner dismisses it as a mere triviality. *Id*. Besides, if the Board were to accept Petitioner's argument that a POSITA could easily and predictably combine the power management systems of Nicol and Kling's software, requiring a motivation to combine loses all meaning – if these two systems could be combined as a mere triviality, then any software could similarly be combined.

In addition, in addition to Petitioner's failure to address how a combination of Nicol and Kling would actually function, Petitioner ignores any issues that would arise. *Id*. at 84. For example, Nicol and Kling change frequencies for

POR at 55-56

Facebook, Inc. v. Windy City Innovations, LLC,

Windy City argues that the Board's analysis was infected by hindsight and that it did not adequately explain how someone skilled in the art would build the combined Roseman and Rissanen system. [] We find no legal error in these aspects of the Board's obviousness analysis. . . . [T]he fact that it would take some creativity to carry out the combination does not defeat a finding of obviousness. [] The Board also correctly rejected Windy City's argument about the difficulty of physically creating the combination, noting that Facebook was not arguing that Rissanen's database would be bodily incorporated into Roseman's system. [] Regardless, "[t]he test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference."

Facebook, Inc. v. Windy City Innovations, LLC, 973 F.3d 1321, 1343 (Fed. Cir. 2020) (internal citations and quotations omitted)

Reply at 6

Elbrus Int'l Ltd. v. Samsung Elecs. Co.

Second, Elbrus argues that combining Lu with Sukegawa would lead to an inoperable circuit absent significant additional design work. However, it is not necessary that [Sukegawa and Lu] be physically combinable to render [a claim] obvious. That is so because the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference, but rather whether a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention. Therefore, Elbrus's argument that combining Sukegawa and Lu could lead to an unworkable circuit is basically irrelevant.

Elbrus Int'l Ltd. v. Samsung Elecs. Co., 738 F. App'x 694, 698–99 (Fed. Cir. 2018) (internal citations and quotations omitted)

Reply at 6

Petition

Consistent with such gating techniques described in Nicol, a POSITA would have known that Nicol's power management system with dynamic frequency control, would set the clock frequency of processing elements that are not needed (or had a low number of pending operations) to a "minimum." Ex. 1001, ¶169. For example, the well-known industry standard, "the Advanced Configuration and Power Interface (ACPI) Specification" was commonly used and referred to by a POSITA. Ex. 1001, ¶170; Ex. 1020 (ACPI Spec.); *see also* Ex. 1011 (Bhatia), 1:6–17 (explaining "the Advanced Configuration and Power Interface (ACPI) Specification, Rev. 1.0., published on Dec. 22, 1996, that provides an interface between the operating system of a system and hardware devices to implement power and thermal management."). Such a "minimum" clock frequency teaching is discussed in the ACPI Specification, and it was thus well-known in the art to set the clock frequency to a minimum in a low power mode. Ex. 1001, ¶171; Ex. 1011, 12:58–65 ("the C3 state defined under the ACPI specification, [whereby] the external clock BCLK to the processor is disabled so that no activity is performed by the processor ***except maintenance of the stored data in the processor's internal cache***.").

Pet. at 38

Petition

If the measured power reaches the upper limit, the controller sends a "throttle signal" to the processor to instruct it to reduce its clock frequency to reduce power consumption. Ex. 1010, 5:38–40, 2:48–51; Ex. 1001, ¶211. "Once [the] lower threshold is reached, the throttle signal may be deasserted, and, in response, the IC resumes normal operation." *Id.*, 5:48–50. In this system, the clock frequency is determined in part by user settings, *e.g.,* the upper and lower power limits. Ex. 1001 ¶213.

Pet. at 49-50

Kling Patent

Once the consumed power, as determined by the power controller, reaches a threshold, a throttle signal is sent to one or more ICs of the computer system by the controller. In response to receiving this throttle signal, one or more of the ICs reduces its power consumption. For example, for one embodiment of the present invention, a processor of the computer system reduces its core frequency while maintaining a consistent bus frequency in response to receiving the throttle signal. For another embodiment, the processor stalls all or a portion of one or more pipelines, or issues no-ops to one or more pipelines, in response to receiving the throttle signal.

Ex. 1010 at 2:43-54

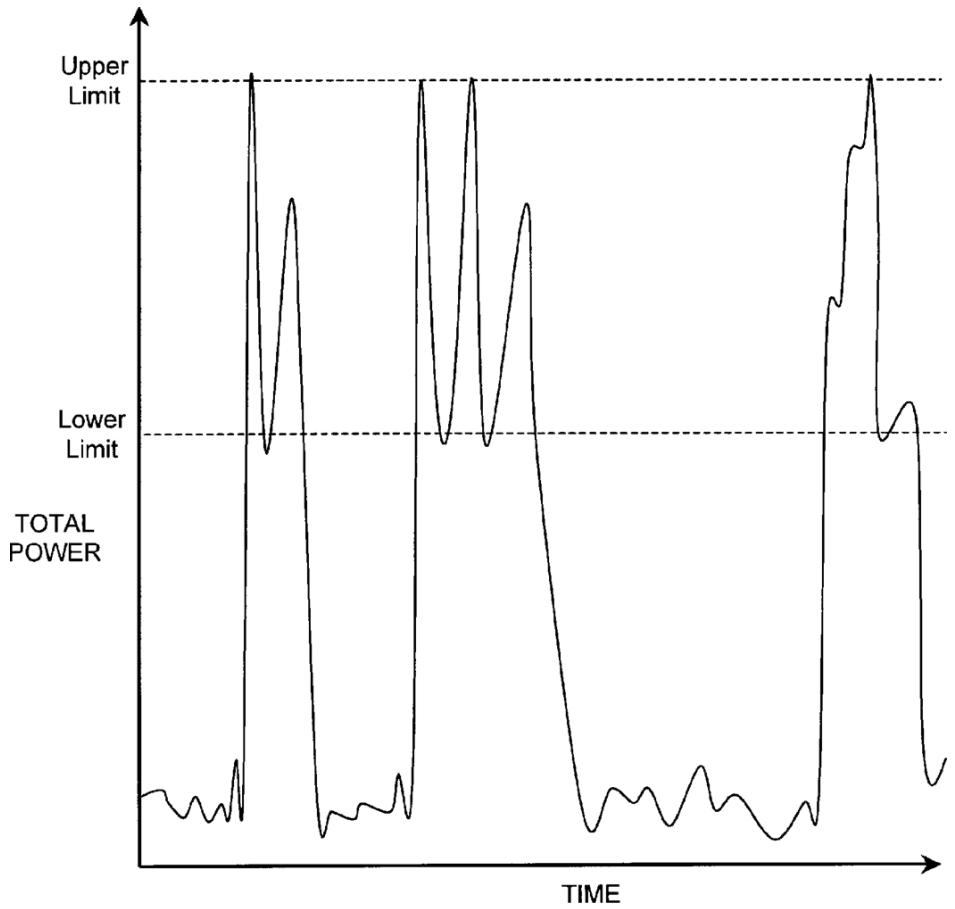


Figure 2A

Ex. 1010 at Figure 2A

Pet. at 16-18, 25, 44, 48

Patent Owner's Expert

Dr. Mangione-Smith

Q. And so isn't that saying that "we'll use a user-defined value that tells us what the total available power is from that outlet"?

A. That may be what they are saying. I -- to be honest with you, I am not sure. I haven't spent the time studying the claim. But there is certainly a user-specified setting for the upper limit, which in some way is intended to be related to the power that they can extract from the wall socket. I -- in some other disclosed usages. I mean, I don't think it always has to be that. It could be that they're – it's simply related to the maximum power that could be consumed by the power supply inside the device, but they certainly do talk about relating it in some circumstances to a wall socket.

Ex. 1051 at 155:8-24

Reply at 26

Nicol Patent

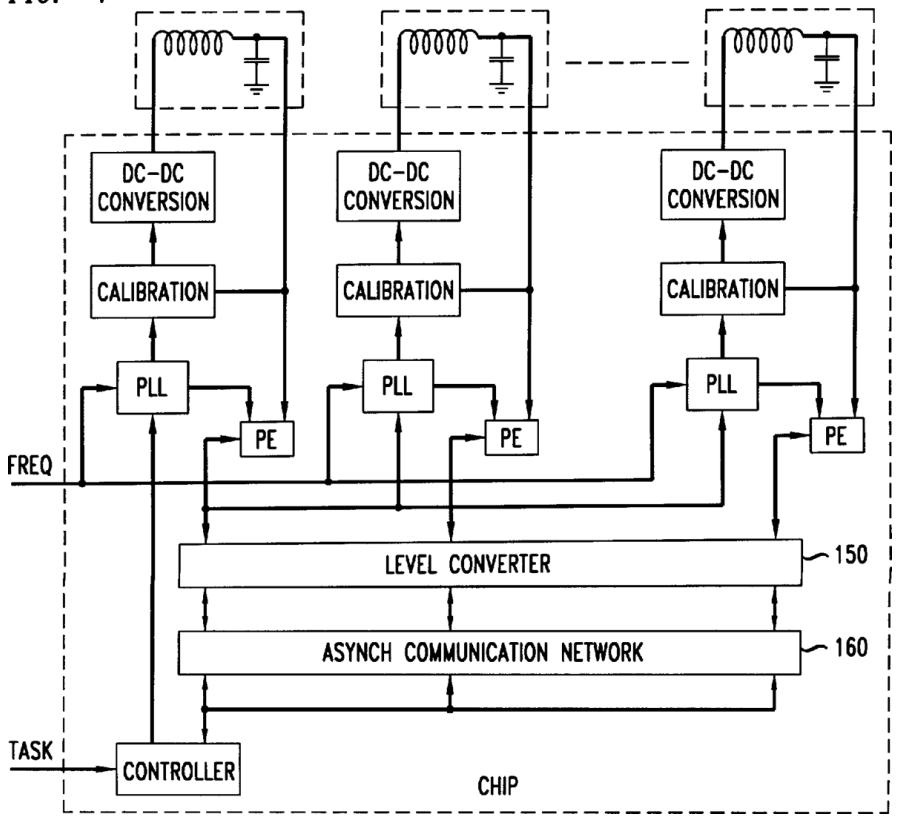
FIG. **2** depicts a block diagram of a multi-processor chip. It contains processing elements (PEs) **100**, **101**, **102**, **103**, . . . **104**, and each PE contains a central processing unit (CPU) and a local cache memory (not shown). A real-time

Ex. 1009 at 2:50-53

time operating system (RTOS) executed on PE **100**. If the number of instructions that need to be executed for each task is known and made available to the operating system, a scheduler within the operating system can use this information to determine the best way to allocate the tasks to the available processors in order to balance the computation.

Ex. 1009 at 3:13-18

FIG. 4



Ex. 1009 at Fig. 4

Pet. at 12-15

Nicol

Voltage scaling as a function of temperature has been incorporated into the Intel Pentium product family as a technique to achieve high performance at varying operating temperatures and process corners. It is described in U.S. Pat. No. 5,440,520. The approach uses an on-chip temperature sensor and associated processing circuitry which issues a code to the off-chip power supply to provide a particular supply voltage. The process variation information is hard-

Ex. 1008 at 1:41-48

As indicated above, the operating system can reduce the supply voltage even further by tracking temperature and process variations. For example, when the chip is nominal in

Ex. 1008 at 4:11-13

Pet. at 42-43; Reply at 20

Ex. 1051

Dr. Mangione-Smith

Q. And -- and you would agree that the -- in Nicol, Nicol's suggestion that however it might be implemented in a mobile computer, as a coprocessor or something like that, the benefits of minimizing power consumption are applicable to mobile computers; right?

A. I -- I would go farther than that and say that the benefits of minimizing power consumption are valuable to a greater or lessor degree in any sort of computing system.

Ex. 1051 at 145:2-12 (objections omitted)

Reply at 13