

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner,

v.

PACT XPP SCHWEIZ AG,
Patent Owner.

IPR2020-00541
Patent 9,075,605 B2

Before SALLY C. MEDLEY, SCOTT C. MOORE, and
CHRISTOPHER L. OGDEN, *Administrative Patent Judges*.

MEDLEY, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
35 U.S.C. § 314

I. INTRODUCTION

Intel Corporation (“Petitioner”) filed a Petition for *inter partes* review of claims 1–6 of U.S. Patent No. 9,075,605 B2 (Ex. 1003, “the ’605 patent”). Paper 2 (“Pet.”). PACT XPP SCHWEIZ AG (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). In accordance with Board authorization, Petitioner filed a Reply to the Preliminary Response (Paper 7, “Pet. Reply”) and Patent Owner filed a Sur-Reply (Paper 9, “Sur-Reply”).

Institution of an *inter partes* review is authorized by statute when “the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.” 35 U.S.C. § 314(a). Upon consideration of the Petition, the Preliminary Response, and the evidence of record, we determine that Petitioner has established a reasonable likelihood of prevailing with respect to the unpatentability of at least one claim of the ’605 patent. Accordingly, for the reasons that follow, we institute an *inter partes* review of claims 1–6 of the ’605 patent.

A. Related Matters

Petitioner and Patent Owner identify, as matters involving or related to the ’605 patent: *PACT XPP Schweiz AG v. Intel Corp.*, Case No. 1:19-cv-1006-UNA (D. Del.) (“District Court Proceeding”); *PACT XPP Schweiz AG v. Intel Corp.*, Civil Action No. 19-267 (D. Del.); *PACT XPP Schweiz AG v. Intel Corp.*, Civil Action No. 19-273 (W.D. Tex.); and *Intel Corp. v. PACT XPP Schweiz AG*, Civil Action No. 19-2241 (N.D. Cal.). Pet. 2 (Mandatory Notices); Paper 3, 1–2.

B. The '605 Patent

The '605 patent describes “optimization of hardware used in data processing,” and more particularly, optimization of power consumption and data processing time in VPU technology (e.g., reconfigurable data processing units, and modules with reconfigurable architecture). Ex. 1003, 1:22–24, 1:32, 2:40–45, 2:56–60. The '605 patent explains that “[t]o determine the clock frequency for a microprocessor based on the state is known,” but “proble[m]s arise in the overall speed with which certain applications are carried out.” *Id.* at 2:30–35. The '605 patent aims to optimize power consumption and data processing time in a VPU (data processing unit) by assigning an appropriate clock to logic cells in a plurality of clocked logic cells (PAEs), based on configuration states of the logic cells. *Id.* at code (57), 2:45–60. For example, a clock preselecting unit in a VPU preselects logic cell clocking such that, “depending on the state, a first clock is preselected at least at a first cell (PAE) and an additional clock is preselected at least at an additional cell.” *Id.* at code (57). The '605 patent’s VPU may include PAEs clockable at different rates in a reconfigurable module, and may also include

multiple buses in parallel whose speed is clocked differently, i.e., a bus which is clocked particularly high for providing a high-performance connection, parallel to a bus which is clocked lower for providing a power-saving connection. The connection c[l]ocked high may be used when longer signal paths have to be compensated, or when PAEs, positioned close together, operate at a high frequency and therefore also have to exchange data at a high frequency in order to provide a good transmission here over short distances in which the latency plays a minor role at best. . . . [A] number of PAEs, positioned together locally and combined in a group, operate at a high frequency and possibly also sequentially and . . . local and correspondingly short bus

systems are clocked high corresponding to the data processing rate of the group, while the bus systems, inputting the operands and outputting the results, have slower clock and data transmission rates. For the purpose of optimizing the power consumption, it would be alternatively possible to implement slow clocking and to supply data at a high speed, e.g., when a large quantity of inflowing data may be processed with only a minor operational effort, thus at low clock rates.

Id. at 8:34–59. Clock frequencies in a VPU may be set in various ways: (i) based on a logic field sleeping mode in which “only one or a plurality of cells are activated, if necessary, on a very low level, i.e., very slow clocking”; (ii) based on “a hysteresis characteristic . . . [for] determining the clock rates, when a temperature-sensitive change of the clock frequencies is to be performed”; and (iii) based on “one or a series of a plurality of different arithmetic and/or logical operations . . . which, at least in part, require a different number of clock cycles.” *Id.* at 3:30–42, 4:55–60, 6:40–55, 13:50–53.

In one example, illustrated in Figures 3a and 3b reproduced below, a field of reconfigurable logic units 0102 (PAEs) are operated at frequencies dependent on the number of operations required for processing a data packet. *Id.* at 6:40–55, 12:31–13:7. Customized clocking of the logic units optimizes a power consumption ratio and the power usage at a constant data throughput through the cells. *Id.* at 6:48–51, 12:55–57.

0301		
0102a I/O	0102d +	0102g loop+
0102b n.c.	0102e -	0102h /
0102c n.c.	0102f *	0102i +

Fig. 3a

+	-	*	loop 16	/	+	I/O
clk	clk	2 clk	16 clk	32 clk	clk	
32	32	16	2	1	32	
8 Mhz	8 Mhz	16 Mhz	128 Mhz	256 Mhz	8 Mhz	8 Mhz
4	4	8	64	128	4	2
1	1	32	16	32	1	1

Fig. 3b

Figure 3a shows a 3×3 field of cells/logic units 0102 that are configurable and reconfigurable independently from one another in a VPU, and Figure 3b illustrates a table indicating numbers of clock cycles and clock rates for the cells of Figure 3a. *Id.* at 11:6–8, 12:31–35.

Figure 3a shows a field of reconfigurable logic units/cells 0102 configured such that (i) a first cell 0102a is used for analyzing an input/output signal, (ii) cells 0102b, 0102c are presently not needed (denoted as not configured, n.c.), and (iii) cells 0102d through 0102i together form a group which executes a complex arithmetic operation including an addition (in cell 0102d), a subtraction (in cell 0102e), a multiplication (in cell 0102f), a loop executing a multiple addition (in cell 0102g), a division (in cell 0102h), and an addition (in cell 0102i). *Id.* at 12:35–45. Cells 0102d through 0102i are grouped in a group 0301 such that data is sequentially and pipeline-like processed by the cells. *Id.* at 12:45–48.

As indicated in the second table row in Figure 3b, the operations in cells 0102a–0102i are executed in different numbers of clock cycles. *Id.* at 12:49–51. For example, an addition or subtraction may be executed in one clock cycle (clk), a multiplication in two clock cycles (2 clk), a division (in

cell 0102h) requires 32 clock cycles (32 clk), and a loop (in cell 0102g) requires 16 clock cycles (16 clk). *Id.* at 12:50–60. Thus, the cell in which the division takes place is operated at the highest clock. *Id.* at 12:57–60. The fourth table row in Figure 3b indicates the cells' clock rates resulting from a central clock of 256 MHz. *Id.* at 13:5–7. Further, if the VPU is operated in an application where the voltage may drop, the entire frequency may be reduced such that all cells are subsequently clocked slower by one half, so that division cell 0102h runs at only 128 MHz, while cell 0102d is clocked at 4 MHz. *Id.* at 13:8–20. If the processor's temperature rises significantly, heat generation in the logic cells may be reduced by an additional clock rate reduction, as indicated in the last table row in Figure 3b. *Id.* at 13:20–28.

C. Illustrative Claim

Petitioner challenges claims 1–6 of the '605 patent. Claim 1 is an independent claim, and claims 2–6 depend therefrom. Claim 1 is reproduced below, which includes changes made per a Certificate of Correction.

1. A method for operating a multiprocessor system comprising a plurality of data processing units, each of the plurality of data processing units (a) including at least one Arithmetic Logic Unit (ALU) and a register unit and (b) being adapted for sequentially processing data, the method comprising:
 - the multiprocessor system setting a clock frequency, of at least a part of the multiprocessor system to a minimum in accordance with a number of pending operations of a first processor;
 - the multiprocessor system subsequently increasing the clock frequency of the at least the part of the multiprocessor system to a maximum in accordance with a number of pending operations of a second processor; and

the multiprocessor system subsequently reducing the clock frequency of the at least the part of the multiprocessor system in accordance with (a) an operating temperature threshold preventing over-temperature and (b) a hysteresis characteristic.

Ex. 1003, 15:6–16:5, Certificate of Correction.

D. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–6 are unpatentable based on the following grounds (Pet. 5):

Claim(s) Challenged	35 U.S.C §	Reference(s)/Basis
1–6	103(a) ¹	Nicol, ² Kling ³
1–6	103(a)	Nicol, Kling, DeHon ⁴
1–6	103(a)	Nicol, Kling, DeHon, Bhatia ⁵

II. DISCUSSION

A. 35 U.S.C. § 315(a)(1)

Section 315(a)(1) provides that “[a]n inter partes review may not be instituted if, before the date on which the petition for such a review is filed, the petitioner or real party in interest filed a civil action challenging the validity of a claim of the patent.”

¹ The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended 35 U.S.C. §§ 102 and 103. Because the ’605 patent has an effective filing date before the effective date of the applicable AIA amendments, we refer to the pre-AIA versions of 35 U.S.C. §§ 102 and 103.

² U.S. Pat. No. 6,141,762, issued Oct. 31, 2000 (Ex. 1009, “Nicol”).

³ U.S. Pat. No. 6,367,023 B2, issued Apr. 2, 2002 (Ex. 1010, “Kling”).

⁴ U.S. Pat. No. 6,052,773, issued Apr. 18, 2000 (Ex. 1012, “DeHon”).

⁵ U.S. Pat. No. 6,535,798 B1, issued Mar. 18, 2003 (Ex. 1011, “Bhatia”).

Patent Owner contends this case is barred under Section 315(a) because Petitioner “sought a declaratory judgment alleging ‘Intel has not infringed and does not infringe, either directly or indirectly, any valid and enforceable claim of the ’605 Patent.’” Prelim. Resp. 30 (citing Ex. 2010 ¶ 102). Patent Owner contends “because Intel asserted that it did not infringe ‘any valid’ claims of the ’605 patent, it expressly challenged the validity of the patent and put it at issue.” *Id.* Petitioner responds that its only cause of action in the cited declaratory judgment complaint was for a “Declaration of Noninfringement,” not a challenge to the validity of the ’605 patent, and that the Board recently rejected the same argument raised by a patent owner involving the same language in a different declaratory judgment complaint. Pet. Reply 3–4 (citing *Intel Corp. v. Tela Innovations, Inc.*, IPR2019-01228, Paper 19 at 15 (PTAB Jan. 30, 2020) (“*Intel v. Tela*”)). In its Sur-Reply, Patent Owner counters that “the label that [a party] has chosen to describe its claim is not determinative,” as “a court looks to ‘the quality of [a pleading’s] substance rather than according to its form or label.’” PO Sur-Reply 4 (quoting *Totes-Isotoner Corp. v. United States*, 594 F.3d 1346, 1355 n.6 (Fed. Cir. 2010)). Here, according to Patent Owner, by alleging in its declaratory judgment action that it “does not infringe any ‘valid’ patent,” “Intel was asking the Judge to rule on validity and the Judge understood that.” *Id.* at 3–4 (citing Ex. 2016). Patent Owner contends that this is because, in a case management order, “the Northern District of California stated that ‘Intel also contends that one or more claims-in-suit are invalid.’” *Id.* at 4 (quoting Ex. 2016).

We agree with Petitioner that 35 U.S.C. § 315(a) does not bar institution under the present circumstances, which, as Petitioner argues, are identical in relevant aspects to those presented in *Intel v. Tela*. We disagree

with Patent Owner’s contention that we should interpret Intel’s allegation that it “does not infringe . . . any valid and enforceable claim of the ’605 Patent” as anything more than an allegation of non-infringement. Ex. 2010 ¶ 102. Nor do we understand the District Court for the Northern District of California to have taken a different view in the co-pending litigation. In full context, the court’s case management order cited by Patent Owner as supporting its contention states that “[i]t shall not be an excuse to deny or delay discovery on the ground that Intel also contends that one or more claims-in-suit are invalid.” Ex. 2016, 1–2. Thus, notwithstanding Patent Owner’s quotation of only a part of that sentence, we find that the court did not affirmatively hold that Petitioner “contends that one or more claims-in-suit are invalid,” but appears to have been stating only that discovery would not be delayed or denied if Petitioner were, for example, to amend its declaratory judgment complaint to add a claim for invalidity.

B. Discretionary Denial under 35 U.S.C. § 314(a)

Institution of *inter partes* review is discretionary. *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1367 (Fed. Cir. 2016) (“[T]he [Office] is permitted, but never compelled, to institute an [*inter partes* review] proceeding.”); 35 U.S.C. § 314(a) (“The Director may not authorize an *inter partes* review to be instituted unless the Director determines that the information presented in the petition filed under section 311 and any response filed under section 313 shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition.”).

Patent Owner contends we should exercise our discretion to deny institution under 35 U.S.C. § 314(a) because a jury trial is currently

scheduled for September 20, 2021 in the co-pending district court litigation. Prelim. Resp. 2, 27–28 (citing *VIZIO, Inc. v. Polaris PowerLED Technologies, LLC*, IPR2020-00043, Paper 30 at 6–12 (May 4, 2020) (denying institution in view of advanced stage of related litigation, investment of time and resources, and overlapping issues); *NHK Spring Co. v. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8 (Sept. 12, 2018) (precedential) (denying institution in view of advanced stage of related litigation)).

We disagree with Patent Owner’s contentions that discretionary denial would be appropriate in this case. As Petitioner points out, the Board has identified a non-exclusive list of factors “relat[ing] to whether efficiency, fairness, and the merits” favor discretionary denial in view of parallel district court litigation. Pet. Reply 4 (citing *Apple Inc. v. Fintiv, Inc.*, IPR2020-00019, Paper 11 at 6 (PTAB Mar. 20, 2020) (precedential) (“*Fintiv*”)).

Those factors include:

1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
2. proximity of the court’s trial date to the Board’s projected statutory deadline for a final written decision;
3. investment in the parallel proceeding by the court and the parties;
4. overlap between issues raised in the petition and in the parallel proceeding;
5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
6. other circumstances that impact the Board’s exercise of discretion, including the merits.

Fintiv at 5–6. In evaluating the factors, we take a holistic view of whether efficiency and integrity of the patent system are best served by denying or

instituting review. *Id.* at 6. We agree with Petitioner that the factors on balance do not favor discretionary denial. Although no single factor is dispositive, the fact that the district court trial is set for after the projected deadline for the Board to issue its Final Written Decision under 35 U.S.C. § 316(a)(11), within one year of institution, weighs heavily against discretionary denial. Patent Owner's arguments regarding *VIZIO* and *NHK Spring* are not persuasive. In both the *VIZIO* and *NHK Spring* cases, the trial date preceded the Board's projected Final Written Decision due date. Accordingly, this proceeding is distinguished from the cases argued by Patent Owner.

Of the remaining factors, the fifth factor alone weighs in favor of discretionary denial, though not sufficiently to tip the balance in our holistic review of all of the *Fintiv* factors. Regarding the first factor, there is no evidence in the record with regard to whether the court is likely to stay the co-pending litigation following institution of an *inter partes* review in this case; the third factor is neutral in view of the parties' respective arguments that documents have been exchanged in the co-pending litigation but that discovery is still ongoing.

The fourth factor likewise is neutral in view of the merely partial overlap between the issues raised here and in the co-pending proceeding. Petitioner contends, and Patent Owner does not dispute, that Petitioner does not assert Nicol and DeHon in the related litigation. Reply 6; Sur-Reply 6 (acknowledging Petitioner's list of non-overlapping references in the Reply). Nicol is relied on by Petitioner in this *inter partes* review for all of the challenged claims 1–6. Pet. 5.

For the above reasons, we decline to exercise our discretion to deny institution under § 314(a).⁶

C. Claim Construction

In this *inter partes* review, claims are construed using the same claim construction standard that would be used to construe the claims in a civil action under 35 U.S.C. § 282(b). 37 C.F.R. § 42.100(b) (2019). The claim construction standard includes construing claims in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent. *See id.*; *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005) (en banc).

Here, Petitioner notes a parallel District Court Proceeding in which Petitioner and Patent Owner have proposed constructions for the following terms: “data processing unit,” “data processing unit . . . adapted for sequentially processing data,” and “to a minimum” recited in claim 1. Pet. 10–11. Petitioner argues that “the Board does not need to construe any claim term for purposes of evaluating the prior art in this Petition” because the Petition’s grounds cover all proposed constructions (in the District Court Proceeding), whereby “Ground I explains the unpatentability of the claims under *Patent Owner’s* proposed construction, Ground II explains the unpatentability of the claims under *Petitioner’s* proposed construction, and

⁶ Patent Owner’s argument in the Sur-Reply that Patent Owner was not properly served under 37 C.F.R. § 42.105(a) is untimely, and thus not considered, as Patent Owner did not raise this argument in the Preliminary Response. Although we need not consider Patent Owner’s untimely service argument here, we note that substantially the same argument was raised by Patent Owner and rejected by the Board in IPR2020-00518, Paper 12, 7–11.

Ground III explains the unpatentability of the claims under either party's constructions." *Id.* Patent Owner does not propose a construction for any claim term. *See generally* Prelim. Resp.

For purposes of this Decision, we need not expressly construe any claim terms. *See Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that "only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy"); *see also Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs.* in the context of an *inter partes* review).

D. Principles of Law

A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including: (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art;⁷ and (4) when in evidence, objective

⁷ Relying on the testimony of Dr. Carl Sechen, Petitioner offers an assessment as to the level of ordinary skill in the art and the general knowledge of a person of ordinary skill (POSITA) at the time of the '605 patent. Pet. 10 (citing Ex. 1001 ¶¶ 83–85). For example, Dr. Sechen states that a POSITA "would have been a person with at least a Master's degree in Electrical or Computer Engineering (or equivalent), and three years of experience with processor design." Ex. 1001 ¶¶ 83–85. Patent Owner does not propose an alternative assessment. *See generally* Prelim. Resp. To the

indicia of obviousness or nonobviousness. *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

E. Asserted Obviousness of Claims 1–6 over Nicol and Kling

Petitioner contends claims 1–6 are unpatentable under 35 U.S.C. § 103(a) as obvious over Nicol and Kling. Pet. 5, 23–52. In support of its showing, Petitioner relies upon the declaration of Dr. Carl Sechen. *Id.* (citing Ex. 1001).

1. Nicol

Nicol describes technology for power reduction in a multiprocessor digital signal processor based on processor load, by dynamically controlling the processing load of chips and controlling the operating voltages of those chips so as to minimize overall power consumption. Ex. 1009, 2:18–31, code (54). Nicol discloses a controller in a multi-processor chip “allocat[ing] tasks to the individual processors to equalize processing load among the chips,” “lower[ing] the clock frequency on the chip to as low a level as possible while assuring proper operation,” and “reduc[ing] the supply voltage.” *Id.* at 2:22–31.

Nicol’s Figure 2, reproduced below, illustrates a multi-processor chip with supply voltage control. *Id.* at 2:37–40.

extent necessary, and for purposes of this Decision, we accept the assessment offered by Petitioner as it is consistent with the ’605 patent and the asserted prior art.

FIG. 2

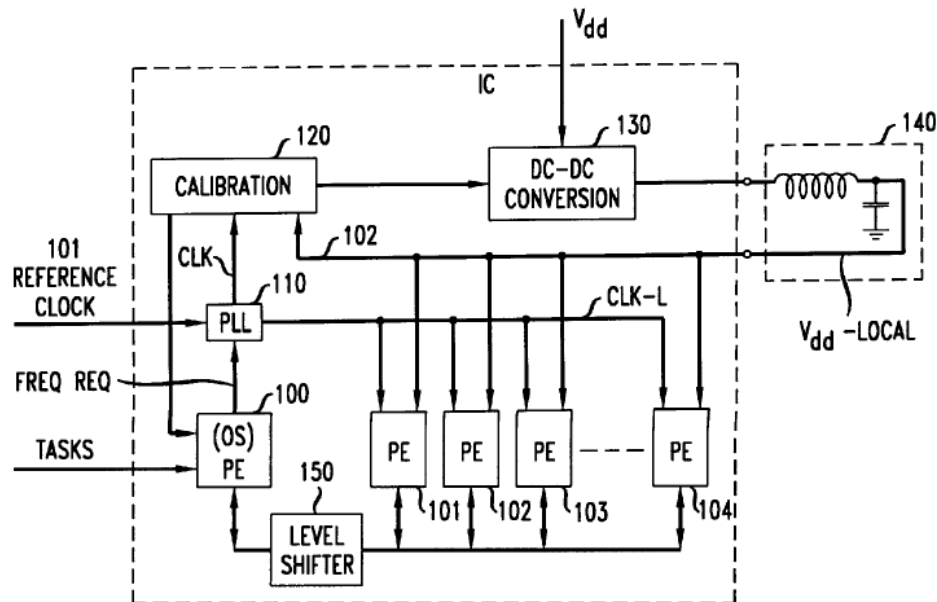


Figure 2 is a block diagram of a multi-processor chip with supply voltage control. *Id.* at 2:37–40.

The multi-processor chip in Figure 2 contains processing elements (PEs) 100, 101, 102, 103, . . . 104, each PE containing a central processing unit (CPU) and a local cache memory. *Id.* at 2:50–53. A real-time operating system resides in PE 100 and allocates tasks to the other PEs. *Id.* at 2:54–55. Applications that need to be processed are mapped to N PEs under control of a real time operating system (RTOS) executed on PE 100. *Id.* at 3:9–13. PEs' processing load is controlled to minimize overall power consumption as follows:

When an application that is running on the FIG. 2 system is subdivided into N concurrent task streams . . . each of the PEs become lightly loaded. This allows the clock frequency of the PEs to be reduced, and if the task division can be carried out perfectly, then the clock frequency of the FIG. 2 system can be reduced by a factor of N. Reducing the frequency, as indicated above, allows reducing the necessary supply voltage, and reducing the supply voltage reduces the system's power

consumption (quadratically). To illustrate, if a given application that is executed on 1 PE requires operating the PE at 140 MHz, it is known from FIG. 1 that the PE can be operated at approximately a 2.7V supply. When the application is divided into two concurrent tasks and assigned to two PEs that are designed to operate at 140 MHz from a 2.7V supply, then the PEs can be operated at 70 MHz and at a supply voltage of 1.8V.

Id. at 3:22–42. In Figure 2, a programmable-frequency clock is generated using a multiplied input reference clock (line 101) via a phase lock loop frequency synthesizer circuit 110. *Id.* at 4:17–22. Two clocks are generated by PLL 110, a Clk clock, and a Clk-L that is 1 frequency step lower than Clk when Clk is being increased. *Id.* at 4:23–26. Clk-L is applied to the PEs, while Clk is applied to calibration circuit 120, which generates a supply voltage command applied to dc–dc converter 130 followed by L–C circuit 140, to cause the converter/L–C circuit combination to create a supply voltage V_{dd} -local that is applied to all PEs. *Id.* at 4:28–37. Figure 3, reproduced below, illustrates the relationship between voltage control clock Clk, the clock Clk-L applied to the PEs, and the V_{dd} -local supply voltage applied to the PEs.⁸ *Id.* at 2:40–44.

⁸ Petitioner asserts that Nicol’s Figure 3 includes labelling errors that Petitioner corrects. *See* Pet. 14–15.

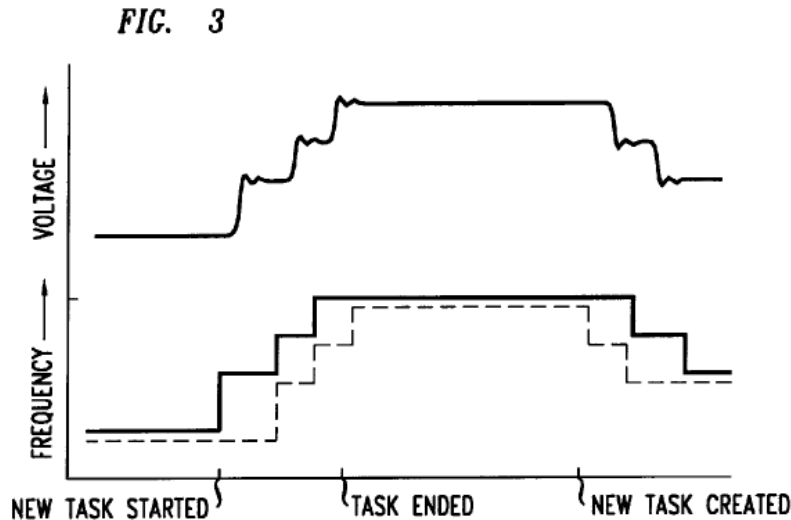


Figure 3 illustrates the relationship between voltage control clock Clk, the clock Clk-L applied to the PEs, and the V_{dd} -local supply voltage applied to the PEs. *Id.* at 2:40–44.

Nicol's Figure 3 illustrates timing associated with increasing Clk, Clk-L, and V_{dd} -local when a new task is created and the load on the multiprocessor is increased, and timing associated with decreasing Clk, Clk-L and V_{dd} -local when the load on the multiprocessor is decreased. *Id.* at 4:54–58. In particular, Figure 3 shows the system operating at 70 MHz from a 1.8V supply when the load is increased in three steps to 140 MHz. *Id.* at 4:58–60. When the 2.7V supply is stable, as shown by the supply voltage plot, the new task is enabled for execution. *Id.* at 4:60–62. Sometime thereafter, a task completes, which reduces the load on the multiprocessor and permits lowering the clock frequency to 100 MHz and lowering the supply voltage to 2.1V. *Id.* at 4:62–67.

Figure 4, reproduced below, illustrates a multi-processor chip with supply voltage control individual to each of the PEs. *Id.* at 2:44–47.

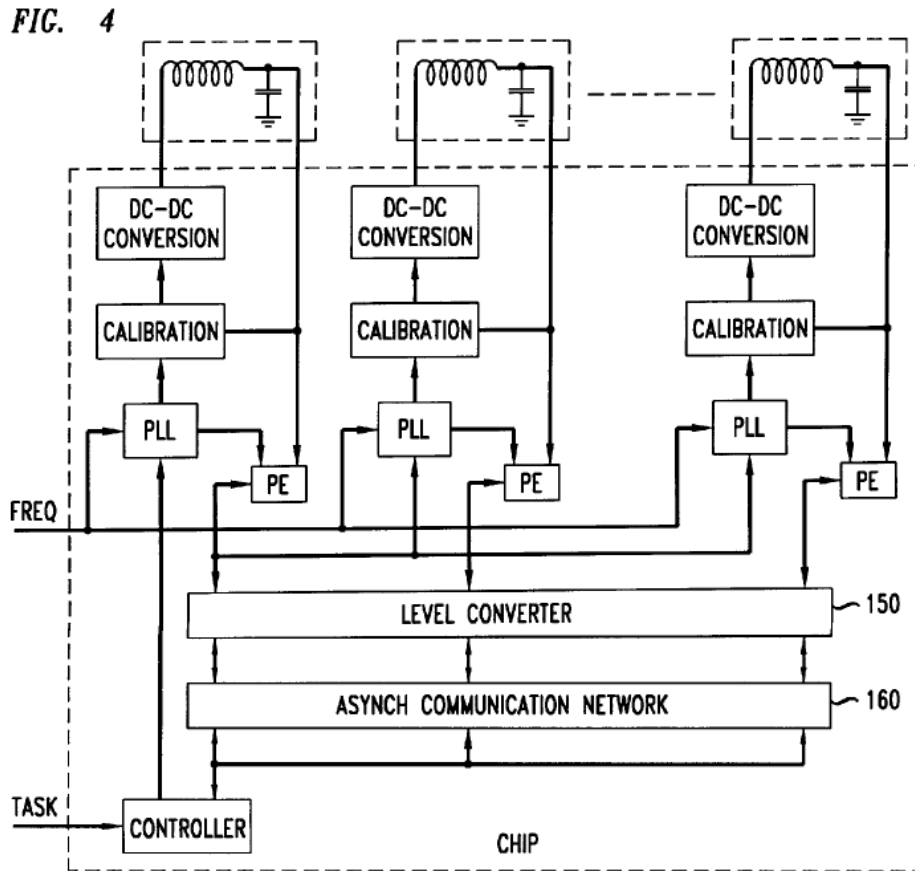


Figure 4 illustrates a multi-processor chip with supply voltage control individual to each of the PEs. *Id.* at 2:44–47.

A separate power supply provided for each PE in Figure 4 allows the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE. *Id.* at 5:55–6:2.

2. Kling

Kling describes a method and apparatus for measuring current, voltage, or duty cycle of a power supply to manage power consumption in a computer system. Ex. 1010, Title, Abstract. Figure 1 of Kling, reproduced below, illustrates a multiprocessor computer system with managed power consumption. *Id.* at 1:65–67, 2:65–67.

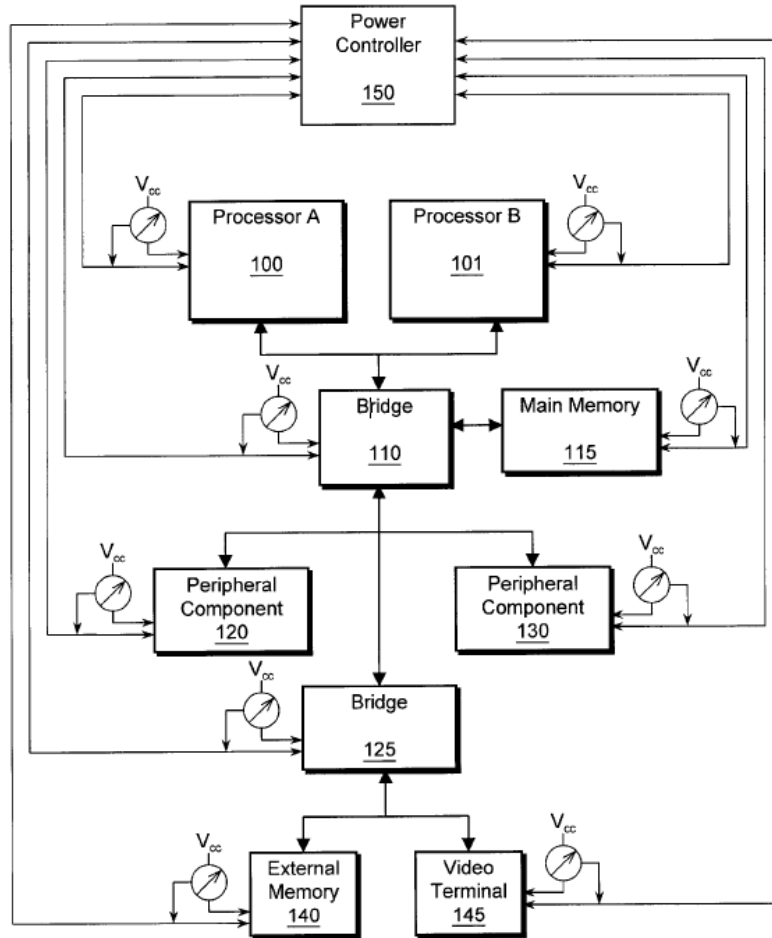


Figure 1

Figure 1 illustrates a multiprocessor computer system with managed power consumption. *Id.* at 1:65–67, 2:65–67.

In the multiprocessor computer system shown in Figure 1, a primary bridge 110 is coupled to processors 100 and 101 via a system bus. *Id.* at 2:65–3:5. Each device in the computer system in Figure 1 receives power from a power supply V_{cc} , the power being monitored by a meter. *Id.* at 3:20–23. A power controller 150, coupled to each device and to each meter, gathers measurements from devices in a portion of the computer system and calculates the total power consumed by that portion of the computer system. *Id.* at 3:22–39. If the total power consumed reaches a threshold, power

controller 150 sends a throttle signal to one or more ICs (integrated circuits) of the computer system, and, in response to receiving the throttle signal, the ICs reduce their power consumption. *Id.* at 4:42–67. Figure 5 of Kling, reproduced below, is a flow chart illustrating a method of reducing power consumption of a processor. *Id.* at 2:14–15.

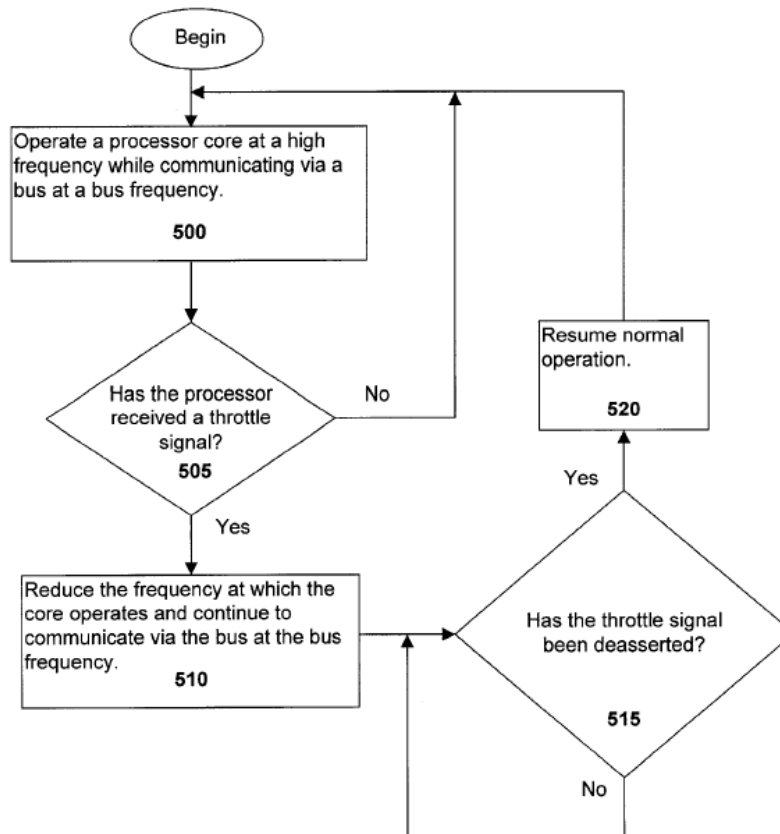


Figure 5

Figure 5 is a flow chart illustrating a method of reducing power consumption of a processor. *Id.* at 2:14–15.

At step 500 in Figure 5, a processor core is operated at a high core frequency while the processor communicates with other ICs of the computer system via a bus operating at a bus frequency. *Id.* at 8:1–5. Next, at step

505, it is determined if the processor has received a throttle signal, and (i) if the processor has not received a throttle signal, normal operation of the processor at the high core frequency continues, but (ii) if the processor has received the throttle signal, then the core frequency of the processor is reduced (step 510). *Id.* at 8:5–15. Next, step 515 determines if the throttle signal to the processor has been deasserted. *Id.* at 8:18–19. The frequency is maintained at the reduced value until the throttle signal is deasserted. *Id.* at 8:20–22. Once the throttle signal is deasserted (step 515), the processor resumes normal operation at the high core frequency (step 520), and the method proceeds back to step 500. *Id.* at 8:22–24.

3. Discussion

Claim 1 recites “[a] method for operating a multiprocessor system comprising a plurality of data processing units, each of the plurality of data processing units (a) including at least one Arithmetic Logic Unit (ALU) and a register unit and (b) being adapted for sequentially processing data.”

Petitioner contends that Nicol discloses a single-chip multiprocessor system that includes a plurality of processing elements (PEs). Pet. 25–29 (citing Ex. 1009, 2:50–53, 3:10–20, 3:66–4:5, 5:66–6:13, 6:27–33, 6:67–7:3, Fig. 4; Ex. 1001 ¶¶ 130, 139, 141). Petitioner further contends that a skilled artisan would have understood that each of Nicol’s PEs (data processing unit) would have included at least one ALU and a register unit. *Id.* at 29–30. In particular, Petitioner argues that Nicol describes that each PE contains a central processing unit (CPU) and a local cache memory, and that a person having ordinary skill in the art would have understood that a PE having a CPU and cache would have included ALU(s) and registers. *Id.* (citing Ex. 1009, 2:50–53; Ex. 1001 ¶ 145; Ex. 1022, 33, Fig. 1.17). Petitioner

contends that under Patent Owner’s proffered District Court Proceeding claim construction of the term “sequentially processing data” to mean “passing results onto one or more other data processing units which are subsequently processing data,” Nicol renders obvious that each of the PEs are adapted for sequentially processing data. *Id.* at 30–35 (citing Ex. 1009, 2:55–56, 6:26–28, 6:14–21, Fig. 4; Ex. 1001 ¶¶ 148, 150–152, 155–158; Ex. 1014, 37, 45, Fig. 1; Ex. 1016, 11, 17; Ex. 1022, 159 (Fig. 3.14), 290, 491–493; Ex. 1026, 10:56–67, Fig. 4).

Claim 1 further recites “the multiprocessor system setting a clock frequency, of at least a part of the multiprocessor system to a minimum in accordance with a number of pending operations of a first processor.” Petitioner contends that the controller of the multiprocessor system sets a clock frequency to a minimum according to a number of pending operations (instructions) of each of the PEs, including the number of pending operations of PE1 (the first processor). *Id.* at 35 (citing Ex. 1009, Fig. 4; Ex. 1001 ¶¶ 161–162). Petitioner further contends that Nicol describes that the controller allocates tasks to the individual processors (including PE1) to equalize processing load among the PEs and then lowers the clock frequency on the chip to as low a level as possible while assuring proper operation. *Id.* at 36 (citing Ex. 1009, 2:23–27). According to Petitioner, Nicol also describes that the controller takes into account the number of pending operations (instructions) of each PE (including PE1) in its determination of processing load and task allocation. *Id.* at 36–37 (citing Ex. 1009, 3:13–18; Ex. 1001 ¶ 165). Petitioner further contends that Nicol Figure 3 illustrates setting the clock frequency of the multi-processor system to a minimum (70 MHz) when the PEs (including PE1) have a light load and also describes setting the clock frequency to zero if none of the PEs are needed. *Id.* at 37–

38 (citing Ex. 1009, 3:31–33, 4:54–62, 5:23–28, 5:42–44, Fig. 3; Ex. 1001 ¶¶ 166, 168). Petitioner also contends that a person having ordinary skill in the art would have known that Nicol’s system would set the clock frequency of processing elements that are not needed to a minimum. *Id.* at 38–39 (citing Ex. 1011, 1:6–17, 12:58–65; Ex. 1020; Ex. 1001 ¶¶ 169–172).

Patent Owner argues that Petitioner fails to show that Nicol discloses or renders obvious the above limitation. Prelim. Resp. 13–17. We have considered Patent Owner’s arguments, but are not persuaded by them. In essence, Patent Owner faults individual passages in Nicol for not describing the disputed limitation, while not discussing other relevant disclosures cited in the Petition. For example, Patent Owner argues that Petitioner fails to show that the clock frequency reduction is in accordance with a number of pending operations of a first processor, because Nicol describes load balancing based on the load across all of the PEs, not based on the load of any single processor. *Id.* at 14 (citing Ex. 1009, 2:23–27). Patent Owner, however, does not address Nicol Figure 4, also relied on in the Petition, which shows PEs that are “independently program[ed] [to] the lowest operating frequency and corresponding lowest supply voltage for each PE.” Ex. 1009, 5:66–6:13; *see also* Ex. 1001 ¶ 95.

Patent Owner’s arguments also fail to address, for example, the Petition and Dr. Sechen’s testimony (cited at Pet. 37–38) that Nicol’s description that “the operating system employs gated clocking techniques to ‘shut down’ PEs that are not needed,” means setting the clock frequency to zero if none of the PEs are needed because all tasks have been completed and there are no new tasks or pending operations for any PE. Ex. 1001 ¶ 168 (citing Ex. 1009, 5:42–44). Based on the current record before us, Petitioner’s assertions with respect to the above claim limitation, supported

by record evidence, are reasonable and Patent Owner's arguments and evidence currently before us are not persuasive to the contrary.

Claim 1 further recites "the multiprocessor system subsequently increasing the clock frequency of the at least the part of the multiprocessor system to a maximum in accordance with a number of pending operations of a second processor." Petitioner contends that Nicol describes a controller that adjusts the clock frequency of the system according to pending operations of each of the PEs. Pet. 39 (citing Ex. 1009, 2:23–27, 3:13–18, Fig. 4). Petitioner further contends that Nicol describes the controller taking into account the number of pending instructions for each PE, including a second processor, because it sets the clock frequency based on identifying the processing requirement of "the most heavily loaded PE." *Id.* at 40 (citing Ex. 1009, 3:66–4:5; Ex. 1001 ¶ 176). Petitioner contends that Nicol Figure 3 (annotated in the Petition) illustrates the multiprocessor system increasing the clock frequency to 140 MHz (maximum clock frequency) prior to execution of a high load. *Id.* at 40–41 (citing Ex. 1009, 3:31–33, 4:54–62, 5:23–28, Fig. 3; Ex. 1001 ¶ 177). Petitioner further contends that Nicol describes each chip having a maximum frequency that the chip can support and that for a maximally utilized system, all of the available processors would operate at full speed (maximum frequency) when satisfying the maximum load encountered by the system. *Id.* at 41 (citing Ex. 1009, 2:65–3:4, 3:63–64; Ex. 1001 ¶ 178).

Patent Owner argues that Petitioner fails to show that Nicol discloses or renders obvious the above limitation. Prelim. Resp. 7–13. We have considered Patent Owner's arguments, but are not persuaded by them. Patent Owner argues that none of the passages in Nicol cited in the Petition

regarding Figure 3 mentions either a maximum frequency or a number of pending operations of a second processor. *Id.* at 9–11.

Nicol Figure 3, annotated in the Petition (Pet. 41), is reproduced below.⁹

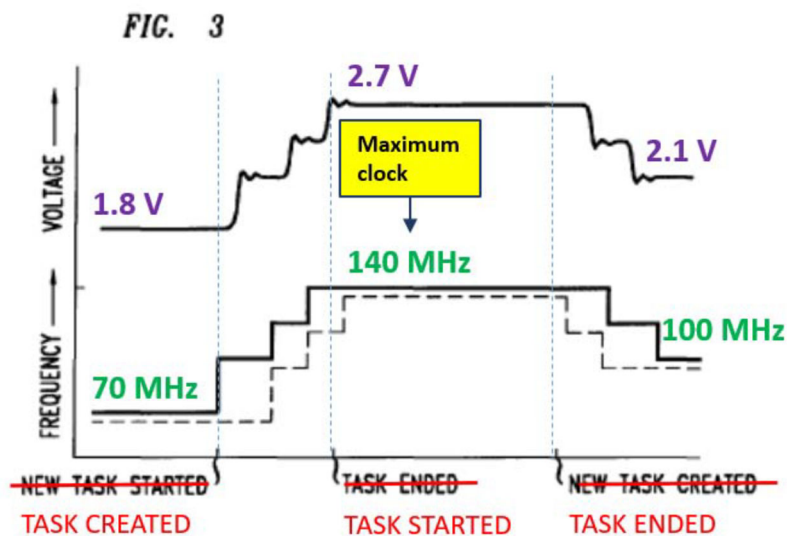


Figure 3 illustrates the relationship between voltage control clock Clk, the clock Clk-L applied to the PEs, and the V_{dd} -local supply voltage applied to the PEs. *Id.* at 2:40–44.

Nicol describes increasing Clk, Clk-L, and V_{dd} -local “when a new task is created and the load on the multiprocessor is thus increased, and the timing associated with decreasing Clk, Clk-L and V_{dd} -local when the load on the multiprocessor is decreased.” Ex. 1009, 4: 54–62. Petitioner, relying on the testimony of Dr. Sechen, contends that Nicol’s 140 MHz of Figure 3 is a maximum clock frequency. Pet. 41 (citing Ex. 1001 ¶ 177; Ex. 1009, 3:31–33, 4:54–62, 5:23–28). Based on the current record before us, we determine

⁹ Petitioner has annotated and “corrected” Nicol Figure 3 because the “sequence of task creation, task start and task end in the original Figure 3 is wrong and has been corrected in red.” Pet. 15 n.5 (citing Ex. 1001 ¶¶ 97–98; Ex. 1009, 4:58–66). Patent Owner does not contest Petitioner’s annotated and “corrected” Figure 3. *See generally* Prelim. Resp.

that Petitioner's contentions are reasonable. Nicol describes that each of the PEs is designed to operate at 140 MHz, which we understand to be the maximum operating frequency of the PE, as Nicol does not describe operating a single PE above 140 MHz. *See, e.g.*, Ex. 1009, 3:54–65. At this stage of the proceeding, we are not persuaded by Patent Owner's arguments that none of the passages cited in the Petition mentions a maximum frequency, because Patent Owner does not squarely address Dr. Sechen's testimony that Nicol's described 140 MHz is a maximum clock frequency.

Patent Owner also argues that the cited passages describing Figure 3 do not mention the number of pending operations. Prelim. Resp. 10. Nicol describes when a new task is created the load on the multiprocessor is increased. Ex. 1009, 4:54–62. Nicol further describes that the Figure 2 system “uses the operating system to react to variations in the system load” and computes a way to balance the additional computational requirements and allocates the tasks to the processors and then computes the required operating frequency. *Id.* at 5:23–28. Nicol Figures 2 and 3 are related. Ex. 1009, 2:40–43. Nicol additionally describes that the clock frequency of the microprocessor is adjusted to “insure that the most heavily loaded PE carries out its assigned tasks within the required completion time.” *Id.* at 3:66–4:5. Based on the record before us, a person having ordinary skill in the art would have understood that in connection with Nicol Figure 3, Nicol's system adjusts the frequency of the multiprocessor system to the “maximum frequency” of 140Mhz in accordance with, for example, the most heavily loaded¹⁰ PE. Ex. 1001 ¶¶ 176–177. Based on the current record before us,

¹⁰ During prosecution of the '605 patent, Patent Owner represented that “a number of operations pending[] . . . is equivalent to the processor load.” Ex. 1004, 377.

Petitioner's assertions, supported by record evidence, are reasonable and Patent Owner's arguments and evidence currently before us are not persuasive to the contrary.

Claim 1 further recites "the multiprocessor system subsequently reducing the clock frequency of the at least the part of the multiprocessor system in accordance with (a) an operating temperature threshold preventing over-temperature and (b) a hysteresis characteristic." Petitioner contends that Nicol in combination with Kling meets this limitation. For example, Petitioner contends Kling describes that processing systems must be able to rapidly detect and mitigate over-temperature situations, and that if a processor temperature exceeds a particular threshold, the processor is placed into low power mode until it cools off. Pet. 41–42 (citing Ex. 1010, 1:38–46). Petitioner contends that a person having ordinary skill in the art would have found it obvious to detect over-temperature in Nicol's multiprocessor system (which itself describes on-chip temperature sensors for tracking temperature) by comparing the system's measured temperatures against a threshold temperature. *Id.* at 42–43 (citing Ex. 1009, 4:11–13; Ex. 1010, 1:43–45; Ex. 1011, 1:6–12; Ex. 1001 ¶¶ 183, 185–186). Petitioner further contends that Kling describes that once an over-temperature is detected, the chip is placed into low power mode, and that a person having ordinary skill in the art would have known that placing Nicol's system in a low power mode would have required reducing the clock frequency to reduce power consumption. *Id.* at 43 (citing Ex. 1009, 1:26–28; Ex. 1010, 1:44–45; Ex. 1001 ¶¶ 187–188). Petitioner also contends that Kling describes the use of hysteresis to improve robustness and reduce the occurrence of power oscillation and that it would have been obvious to a person having ordinary

skill in the art to include Kling's hysteresis teaching to Nicol's system. *Id.* at 44–45 (citing Ex. 1010, 5:50–58; Ex. 1001 ¶¶ 189–190, 192).

Petitioner argues a person of ordinary skill in the art would have been motivated and found it obvious to combine the teachings of Nicol and Kling. Pet. 23–25, 42–45. For example, Petitioner contends that a person having ordinary skill in the art would have been motivated to combine Kling's over-temperature protection to Nicol's multiprocessor system because it was known that over-temperature protection was critical for high-performance multiprocessor systems. *Id.* at 24, 42 (citing Ex. 1001 ¶ 127; Ex. 1009, 2:18–22, 3:9–20; Ex. 1010, 1:38–46; Ex. 1001 ¶¶ 127, 129, 182).

Patent Owner argues that Petitioner fails to establish that a person having ordinary skill in the art would have been motivated to combine Nicol with Kling. Prelim. Resp. 18–23. We have considered all of Patent Owner's arguments, but are not persuaded by them. For example, Patent Owner argues that the Petition is not supported by record evidence and fails to show that over-temperature control is critical or necessary. *Id.* at 22–23 (citing Pet. 42). The current record contains ample evidence that processors that overheat can and do fail. Ex. Ex. 1001 ¶¶ 50–53, 102; Ex. 1010, 1:25–26, 1:38–47. Indeed, Kling explains that if thermal monitoring is not included “the processor may destroy itself by its own heat.” Ex. 1010, 1:42–47. Based on the current record before us, Petitioner's assertions, supported by record evidence, are reasonable and Patent Owner's arguments and evidence currently before us are not persuasive to the contrary.

We also have reviewed Petitioner's showings for dependent claims 2–6. Pet. 45–52. Patent Owner does not contest those claims separately. *See* Prelim. Resp. 7. We conclude that, based on the totality of the arguments and evidence currently in the record, Petitioner has sufficiently shown for

purposes of institution, that Nicol and Kling teach or suggest each limitation of claims 1–6, and that a person of ordinary skill in the art would have had reason to combine the references in the manner Petitioner proposes. *See* Pet. 23–52. Accordingly, we determine the information presented shows a reasonable likelihood that Petitioner would prevail in establishing that at least one of the challenged claims 1–6 would have been obvious over Nicol and Kling.

F. Asserted Obviousness of Claims 1–6 over Nicol, Kling, and DeHon

Petitioner contends claims 1–6 are unpatentable under 35 U.S.C. § 103(a) as obvious over Nicol, Kling, and DeHon. Pet. 5, 52–63. In support of its showing, Petitioner relies upon the declaration of Dr. Carl Sechen. *Id.* (citing Ex. 1001).

1. DeHon

DeHon describes DPGA (dynamically programmable gate array)-coupled microprocessors. Ex. 1012, Title, Abstract. A microprocessor described by DeHon includes a fixed logic processor to perform logic calculations, and a programmable gate array enabling application-specific configurations. *Id.* at 2:10–15. The gate array is configurable to adapt to the time-changing demands of the microprocessor and provide the functionality required to best serve those demands. *Id.* at 2:15–24.

Figure 1 of DeHon, reproduced below, illustrates co-location of a configurable array 100 with a fixed logic processor core cell 10 on a single semiconductor chip. *Id.* at 3:55–58.

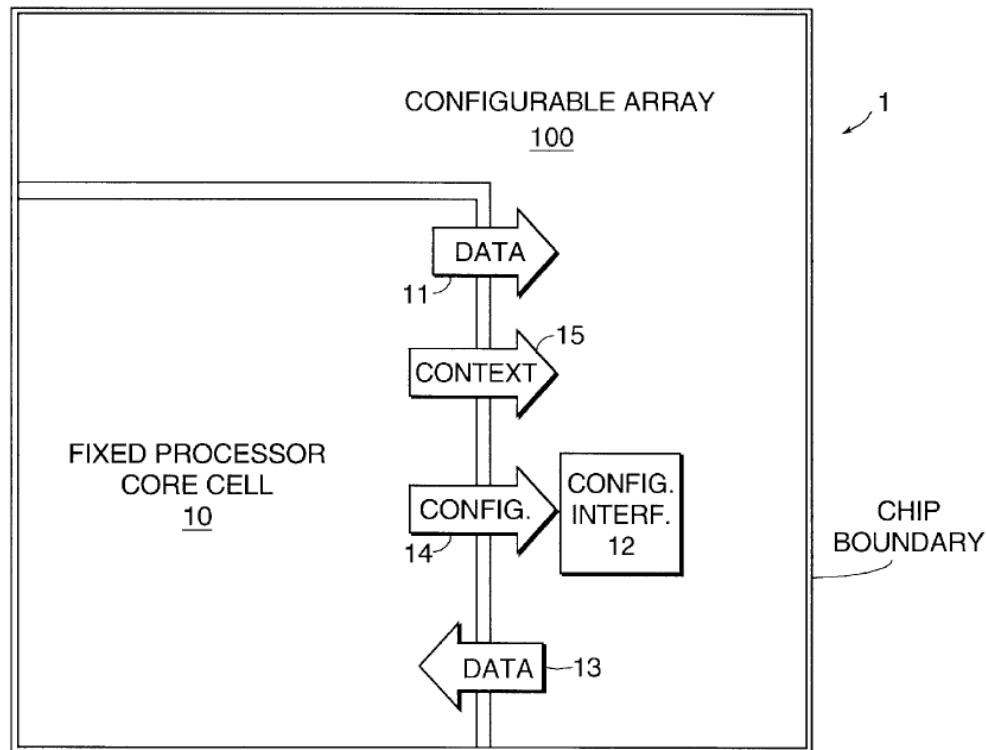


FIG. 1

Figure 1 is a block diagram showing the co-location of a configurable array 100 with a fixed logic processor core cell 10 on a single semiconductor chip. *Id.* at 3:55–58.

Figure 1 of DeHon illustrates a configurable logic-coupled processor 1 including a fixed processor core cell 10 and a configurable array 100 located on the same silicon die or chip. *Id.* at 5:34–39. Processor core cell 10 may be a complex instruction set (CISC) or reduced instruction set (RISC) architecture, includes an arithmetic logic unit (ALU), and may also include a fixed processing unit (FPU), register files (RF), instruction caches, and data caches. *Id.* at 5:39–44. The combination of processor cell 10 and configurable array 100 on the same silicon die enables high bandwidth communications with a low latency interface. *Id.* at 6:19–22. Integration of processor core cell 10 with reconfigurable array 100 also decreases

reconfiguration overhead. *Id.* at 6:30–33. Implementation of this DPGA architecture also facilitates multi-tasking by assigning each task to a different context of array 100. *Id.* at 6:44–46.

In operation, configurable array 100 initially receives configuration programming 14 at power-up, or under application program control from processor cell 10. *Id.* at 5:44–47. Once the proper configuration has been programmed into array 100, processor cell 10 feeds input data 11 to and receives data output 13 from configurable array 100. *Id.* at 5:49–53. Control instructions 15, which may initiate array reconfigurations to finish computations or switch between multi-tasking or multi-threading functions, are also transmitted from processor cell 10 to configurable array 100. *Id.* at 5:53–58. Configurable array 100 is employed by processor core cell 10 as a programmable function unit (PFU) for application-specific acceleration. *Id.* at 5:59–61. For example, the operating system and various applications specialize the configurable array to serve as a co-processor for compute-intensive functions such as compression, encryption, signal processing, or protocol processing. *Id.* at 5:61–67. Alternatively, a separate configurator can be implemented either on- or off-chip, to provide the configuration programming to array 100. *Id.* at 6:4–6. For example, during the initial execution of an application program, configurable array 100 can dynamically manipulate incoming data to processor cell 10; later, configurable array 100 can be configured as a math co-processor to perform ALU operations, or Fast-Fourier transform (FFT) operations. *Id.* at 6:7–18.

2. Discussion

For this challenge, Petitioner argues that to the extent claim 1 requires that the data processing units are reconfigurable, DeHon meets such

requirement. Pet. 53. Specifically, Petitioner contends that DeHon shows in Figure 1 a microprocessor with a fixed core 10 connected to a reconfigurable array 100. *Id.* at 59 (citing Ex. 1012, Fig. 1, 2:25–27, claim 19; Ex. 1001 ¶ 248). Petitioner further contends that DeHon’s reconfigurable processors in Nicol’s microprocessor system can be configured as “sequential data processors where the data results from one processor are fed to another, for each processor to perform a separate computation.” *Id.* at 59–61 (citing Ex. 1009, 2:55–56, 6:26–33, Fig. 4; Ex. 1012, Fig. 1; Ex. 1013, 9; Ex. 1001 ¶¶ 251–253; Ex. 1014, 37, 45, Fig. 1).

Petitioner also contends that to the extent the claim 1 term “to a minimum” requires the preservation of memory contents, a person having ordinary skill in the art, based on Nicol’s disclosure regarding power management, would have consulted the Advanced Configuration and Power Interface (ACPI) Specification, which teaches a lower power mode. *Id.* at 62–63 (citing Ex. 1009, 5:42–45, 5:66–6:2, 6:26–33; Ex. 1001 ¶¶ 259, 261–262; Ex. 1020; Ex. 1011, 1:6–7, 12:58–65). Patent Owner’s arguments with respect to whether Petitioner has shown that the cited prior art meets the claim limitations are the same with respect to the first challenge above. *See* Prelim. Resp. 1, 7, 13, 17. For reasons stated above, and at this juncture of the proceeding, we are not persuaded by such arguments.

Petitioner further provides reasons with rational underpinnings to combine the system of Nicol and Kling with DeHon. *Id.* at 53–58. For example, Petitioner contends that Nicol describes that its multiprocessor system is intended for use in a variety of digital signal processing applications. *Id.* at 54 (citing Ex. 1009, 2:53–56). Petitioner additionally contends that a person having ordinary skill in the art would have been motivated to consult and apply DeHon, “because DeHon teaches an

‘inventive microprocessor [that] can serve as the principle *building block for a wide range of applications* including personal computers, embedded systems, application-specific computers, and general and special-purpose multiprocessors’” *Id.* (citing Ex. 1012, 2:18–24; Ex. 1001 ¶ 232).

Petitioner also contends that a person having ordinary skill in the art would have been motivated to apply DeHon’s teachings of a flexible, reconfigurable, microprocessor chip, as PEs in Nicol’s system to improve application acceleration. *Id.* (citing Ex. 1012, code (57); Ex. 1001 ¶ 233).

We are not persuaded by Patent Owner’s attorney arguments that Nicol fails to suggest the use of reconfigurable processors or application acceleration (Prelim. Resp. 23–24), because such arguments are conclusory and not based on the perspective of what a person having ordinary skill in the art at the time of the invention would have known. Petitioner contends, with supporting evidence, that Nicol describes that its multiprocessor system is intended for use in a variety of digital signal processing applications and that a person having ordinary skill in the art would have been motivated to utilize reconfigurable processors, such as DeHon’s, in Nicol’s system to improve application acceleration. Pet. 54 (citing Ex. 1009, 2:53–56; Ex. 1012, 2:18–24, code (57); Ex. 1001 ¶¶ 232–233). We further disagree that Dr. Sechen’s testimony is conclusory. Prelim. Resp. 24. Dr. Sechen’s testimony is replete with citations to record evidence. Lastly, Patent Owner’s arguments regarding DeHon’s failure to mention frequency are not persuasive. Prelim. Resp. 24–25. DeHon’s processors include clocks. *See, e.g.,* Ex. 1012, 8:11–37. Based on the current record before us, Petitioner’s assertions, supported by record evidence, are reasonable and Patent Owner’s arguments and evidence currently before us are not persuasive to the contrary.

Petitioner's showing for dependent claims 2–6 is the same as Petitioner's showing with respect to its first challenge for claims 2–6. Pet. 53. Patent Owner does not contest those claims separately. *See* Prelim. Resp. 7. We conclude that, based on the totality of the arguments and evidence currently in the record, Petitioner has sufficiently shown for purposes of institution, that Nicol, Kling, and DeHon teach or suggest each limitation of claims 1–6, and that a person of ordinary skill in the art would have had reason to combine the references in the manner Petitioner proposes. *See* Pet. 52–63. Accordingly, we determine the information presented shows a reasonable likelihood that Petitioner would prevail in establishing that at least one of the challenged claims 1–6 would have been obvious over Nicol, Kling, and DeHon.

G. Asserted Obviousness of Claims 1–6 over Nicol, Kling, DeHon, and Bhatia

Petitioner contends claims 1–6 are unpatentable under 35 U.S.C. § 103(a) as obvious over Nicol, Kling, DeHon, and Bhatia. Pet. 5, 63–66. In support of its showing, Petitioner relies upon the declaration of Dr. Carl Sechen. *Id.* (citing Ex. 1001).

1. Bhatia

Bhatia describes thermal management in a system by “a thermal management controller adapted to vary . . . [a system's] component between performance states including a lower performance state when the controller detects a first condition, the controller adapted to throttle the [component's] clock while the component is in the lower performance state.” Ex. 1011, 1:52–59, Title, Abstract. The system's component may be a general or special-purpose processor such as a microprocessor, microcontroller,

application-specific integrated circuit (ASIC), programmable gate array (PGA), peripheral device controller, or other types of devices. *Id.* at 2:30–36. A performance state may be characterized by component core and bus clock speeds, and component supply voltage levels. *Id.* at 2:37–40. In an HP (high performance) state, a processor's (or other component's) core clock frequency and voltage level may be at one setting, while in an LP (low performance) state, the processor's core clock frequency and voltage level may be at a lower setting. *Id.* at 2:45–51. The thermal management operation is designed to increase the amount of time the processor is operating in the HP state. *Id.* at 2:49–51.

Figure 6 of Bhatia, reproduced below, illustrates a graph of power dissipation levels and temperatures in a computing system during thermal management. *Id.* at 2:2–5. Figure 6 illustrates power dissipation P_y as a processor is throttled from the LP state. *Id.* at 9:41–45.

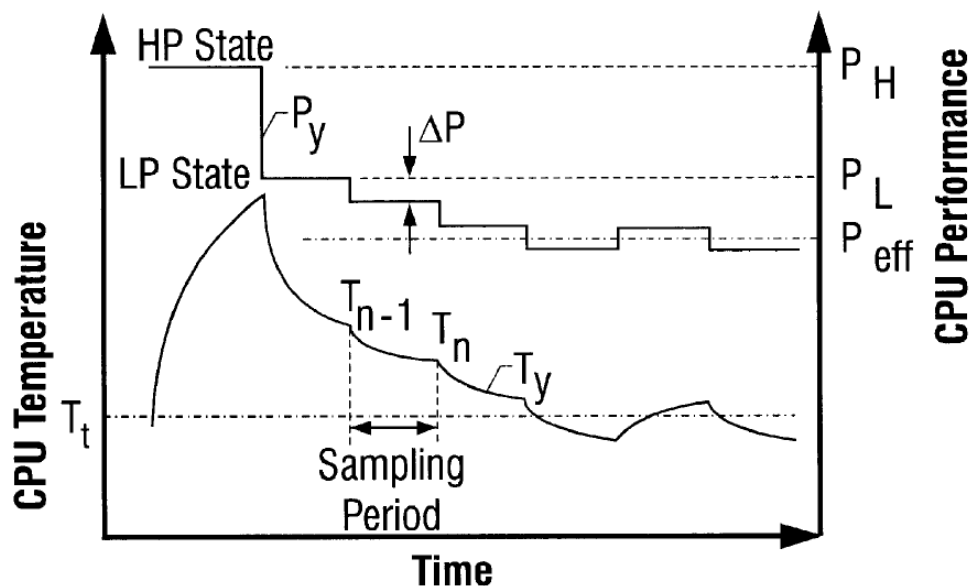


FIG. 6

Figure 6 of Bhatia illustrates a graph of power dissipation levels and temperatures in a computing system during thermal management.
Id. at 2:2–5.

Bhatia also describes a power management module to control performance state transitions. *Id.* at 12:26–30. Figure 8 of Bhatia, reproduced below, is a flow diagram of operations performed by a power management module. *Id.* at 2:9–10.

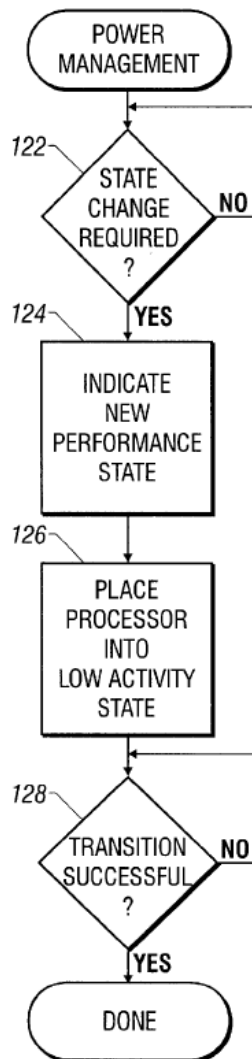


FIG. 8

Figure 8 of Bhatia is a flow diagram of a power management module controlling state transitions. *Id.* at 2:9–10.

The power management module determines (at step 122 in Figure 8 reproduced above) if a performance state change is required in response to a received event/thermal event, and then indicates (at step 124) the new performance state the processor is to transition to. *Id.* at 12:32–40. The new performance state may be indicated by writing a predefined value to a control register that may be programmed under the ACPI (Advanced Configuration and Power Interface) Specification. *Id.* at 12:40–46. Next, the power management module places (at step 126) the processor into a low activity state (e.g., a C1 state under the ACPI Specification, a deep sleep state or C3 state under the ACPI Specification or a stop grant state or C2 state under the ACPI Specification). *Id.* at 12:58–67. In the deep sleep state, which may be the C3 state defined under the ACPI Specification, the external clock BCLK to the processor is disabled so that no activity is performed by the processor except maintenance of the stored data in the processor's internal cache. *Id.* In the stop grant or C2 state, the processor performs minimal activity, such as snooping for an internal cache line hit to maintain cache coherency. *Id.* While the processor is in the low activity state, the performance mode of the processor may be changed by changing the core processor clock frequency and adjusting the core voltage level. *Id.* at 12:67–13:4.

2. Discussion

For this challenge, Petitioner contends that to the extent the claim 1 term “to a minimum” requires the preservation of memory contents, Bhatia explicitly describes this requirement. Pet. 64–65 (citing Ex. 1011, 12:61–64;

Ex. 1001 ¶¶ 269–271). In particular, Petitioner contends that Bhatia describes the “ACPI’s C3-state,” which is a low power mode setting where the processor clock is disabled and the processor does not perform any activity except maintenance of cache memory contents. *Id.* Patent Owner’s arguments with respect to whether Petitioner has shown that the cited prior art meets the claim limitations are the same with respect to the first challenge above. *See* Prelim. Resp. 1, 7, 13, 17. For reasons stated above, and at this juncture of the proceeding, we are not persuaded by such arguments.

Petitioner further provides reasons to combine Nicol, Kling, DeHon, and Bhatia. Pet. 65–66. For example, Petitioner contends that it would have been obvious to a person having ordinary skill in the art to implement Bhatia’s low activity state teachings in Nicol’s system as additional means to minimize power consumption. *Id.* (citing Ex. 1011, 1:6–7, 21:58–64; Ex. 1001 ¶¶ 272–274). We have considered Patent Owner’s arguments that there is no reason to combine the references. Prelim. Resp. 26–27. We are not persuaded by these arguments. At this juncture of the proceeding, the evidence suggests that a person having ordinary skill in the art would have looked to Bhatia for details on how to minimize power consumption, which is a stated goal of Nicol.

Petitioner’s showing for dependent claims 2–6 is the same as Petitioner’s first challenge showing for claims 2–6. Pet. 64. Patent Owner does not contest those claims separately. *See* Prelim. Resp. 7. We conclude that, based on the totality of the arguments and evidence currently in the record, Petitioner has sufficiently shown for purposes of institution, that Nicol, Kling, DeHon, and Bhatia teach or suggest each limitation of claims 1–6, and that a person of ordinary skill in the art would have had reason to

combine the references in the manner Petitioner proposes. *See* Pet. 63–66. Accordingly, we determine the information presented shows a reasonable likelihood that Petitioner would prevail in establishing that at least one of the challenged claims 1–6 would have been obvious over Nicol, Kling, DeHon, and Bhatia.

III. CONCLUSION

For the foregoing reasons, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing at least one of claims 1–6 of the '605 patent is unpatentable under 35 U.S.C. § 103(a).

IV. ORDER

Accordingly, it is:

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 1–6 of the '605 patent on the grounds set forth in the Petition; and

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial; the trial will commence on the entry date of this decision.

IPR2020-00541
Patent 9,075,605 B2

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