UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION
Petitioner

v.

PACT XPP SCHWEIZ AG
Patent Owner

Case IPR2020-00541
U.S. Patent No. 9,075,605

PATENT OWNER'S RESPONSE PURSUANT TO 37 C.F.R. § 42.120

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Intel Corporation's ("Petitioner") Petition (Paper 1, "Pet.") proffers three invalidity grounds for U.S. Patent No. 9,075,605 ("'605 patent") (Ex. 1003):

(1) Claims 1-6 are allegedly obvious over U.S. Patent No. 6,141,762 ("Nicol") (Ex. 1009) in view of U.S. Patent No. 6,367,023 ("Kling") (Ex. 1010);

(2) Claims 1-6 are allegedly obvious over Nicol in view of Kling and in view of U.S. Patent No. 6,052,773 ("DeHon") (Ex. 1012);

(3) Claims 1-6 are allegedly obvious over Nicol in view of Kling and DeHon and in further view of U.S. Patent No. 6,535,798 ("Bhatia") (Ex. 1011);

On September 9, 2020, the Board instituted review, but stated the decision is "based on the totality of the arguments and evidence currently in the record . . . for purposes of institution." Paper 11 ("Institution Decision") at 38. "There is a significant difference between a petitioner's burden to establish a 'reasonable likelihood of success' at institution, and actually proving invalidity by a preponderance of the evidence at trial." *Trivascular, Inc. v. Samuels*, 812 F.3d 1056, 1068 (Fed. Cir. 2016). Patent Owner Pact XPP Schweiz AG ("PO") provides new evidence and arguments demonstrating Petitioner has not met its burden.

I. INTRODUCTION

In Ground I, Petitioner argues claims 1-6 is obvious in view Nicol in combination with Kling under Patent Owner's construction. This argument fails for several reasons.

In regard to claim 1, Nicol in view of Kling does not disclose "setting a clock frequency, of at least a part of the multiprocessor system to a minimum." For this limitation, Petitioner improperly points to features from different embodiments (Figure 2 and Figure 4) in Nicol without explaining how they are interchangeable or how they fit together into a single system. As discussed below in details, a POSITA would not be motivated to combine the Figure 2 and Figure 4 embodiments of Nicol. Even assuming these embodiments could be combined for argument purposes, the combination does not show "in accordance with number of pending operations of a first processor." Petitioner points to an arbitrary "PE" in the annotated Figure 4 as the First Processor (PE1), but does not show that the clock frequency is set based on the number of pending operations of PE1. In addition, Petitioner misreads the "gated clock" as the "minimum frequency." The gated clock is caused by low voltage, not set according to the number of pending operations of any processor. Under this Ground, Petitioner also improperly relies on ACPI that is not disclosed in either prior art references, as well as Bhatia that is not part of the ground. Last but the not least, Petitioner misinterpret the term

"minimum" to mean either the 70 MHz disclosed in Figure 3 of Nicol, the clock gating with a frequency of zero, or the ACPI C3 state. As discussed below, these three disclosures are described for different purposes, and a POSITA would not be motivated to combine them.

In regard to claim 2, Petitioner has not shown that Nicol in view of Kling renders obvious the "clock frequency [being] determined in part by processor voltage." As discussed below, a POSITA would have understood that Nicol's clock frequency is jointly determined by the processing load and the required completion time. Specifically, Nicol's clock frequency is minimized to the value necessary to finish the tasks within the required completion time. A POSITA would have understood that the clock frequency in Nicol is not determined by voltage. Kling fails to disclose a measurement of the "processor voltage," because the voltage measured in Kling is not the processor voltage, but is the voltage drop between the power supply and the processor. Even assuming Kling's throttling is based on the "processor voltage," a POSITA would not have a motivation to combine Kling with Nicol, because Nicol already minimized the power consumption based on processing load and required completion time. A further reduction of clock frequency based on supply voltage would cause the tasks to not finish on time impacting performance, and Intel fails to provide a reasonable expectation of success in combining the references.

In regard to claim 3, Petitioner has not shown that Nicol in view of Kling discloses "said clock frequency is determined in part by available power." Petitioner's argument fails for three reasons: (1) Petitioner misrepresents what is disclosed by the reference. Kling is not limited by available power; it is limited by a self-imposed safety measure, such as fuse or circuit breaker trips; (2) Petitioner has not shown that Kling's frequency is dependent on an available power within the context of a changing clock frequency in claim 1, from which claim 3 is dependent; (3) Petitioner's claim that Kling's maximum power limitation is "simple add-on software" that could have been readily implemented with "an appropriately placed resistor" is simply false.

In regard to claim 4, Petitioner has not carried its burden to show that Nicol in view of Kling renders obvious that "said clock frequency is determined in part by a user setting." For a user setting, Petitioner refers to Kling lower threshold which Kling describes as being modifiable by a user. Pet., 49. However, the frequency does not depend on a lower threshold. The frequency depends on either the upper threshold, which causes throttling, or normal operating conditions which sets a high core frequency.

In regard to claim 5, it requires that a clock frequency depend on both available power and a user setting. For the reasons set forth above, Petitioner fails to show this element. In addition, Petitioner also argues that the upper limit in

Kling Figure 2 is available power, and the lower limit in Figure 2 is a user setting. Pet. at 47-50. However, even assuming this is true, at no point does Kling's clock frequency depend on both an available power and a user input under Petitioner's own analysis.

In regard to claim 6, Petitioner fails to establish that "said number of pending operations is determined at by the fill level of one or more buffers." Petitioner points to Nicol's disclosure of "the number of instructions" and the existence of an "instruction queue." Pet. at 51. However, as discussed in detail below, a POSITA would not have concluded that the existence of an "instruction queue" means the number of instructions or pending operations is "determined by" the fill level. A POSITA would not have understood that processor loads or number of pending operations are necessarily determined through the buffer fill level.

Last but not the least, Petitioner has not carried its burden to show that POSITA would combine Nicol and Kling. Petitioner's alleged motivations to combine amount to a suggestion that Nicol and Kling manage aspects of a computer system and it would be beneficial to combine the aspects that they manage. However, mere benefit without any showing of actual motivation is plainly insufficient to suggest a POSITA would combine these reference. Petitioner also ignores any issues the combination would arise. In fact, the

disclosure of Kling dissuade a POSITA from using a thermal sensor as proposed by Petitioner to avoid the inaccuracies and slow response time.

Under Ground II, Petitioner asserts that claims 1–6 are obvious in view of Nicol in combination with Kling and DeHon under Petitioner's constructions. Petitioner relies on DeHon for at least the reconfigurable aspect of the claims. However, a POSITA would have understood that the proposed combination would substantially increase the overhead implicit in communication between the PEs and substantially increase reconfiguration overhead. A POSITA would not have a motivation to make such combination or a reasonable expectation of success.

Under Ground III, Petitioner proposes to combine Nicol, Kling and Dehon with Bhatia for the reason that Bhatia describes the ACPI's C3-state, a low power mode setting that satisfies the "to a minimum" limitation under Petitioner's construction. Pet. at 64. However, this attempt fails because Petitioner merely points to benefit without showing any actual motivation. Petitioner makes no attempt to explain how a system combining Nicol and Bhatia would actually function, and ignores the issues that would arise. As such, none of the Grounds in the Petition renders the claims obvious.

II. OVERVIEW OF THE '605 PATENT

The '605 patent is directed to systems and methods for separately setting the clock frequencies of different hardware modules within an integrated circuit.

The ’605 patent also discloses specific ways to assign clock frequencies to different modules in order to improve power management and increase the operating efficiency. Specifically, the ’605 patent discloses changing the clock frequencies of portions of the multi-core system in a particular way to take advantage of the processing power of certain cores and in the meantime increase power efficiency. For example, clock frequencies of groups of processors that sequentially process data shown in Fig. 4 may be changed to achieve improved power efficiency, where the frequency change of the one group of processors may depend on the pending operations of another group of processors:

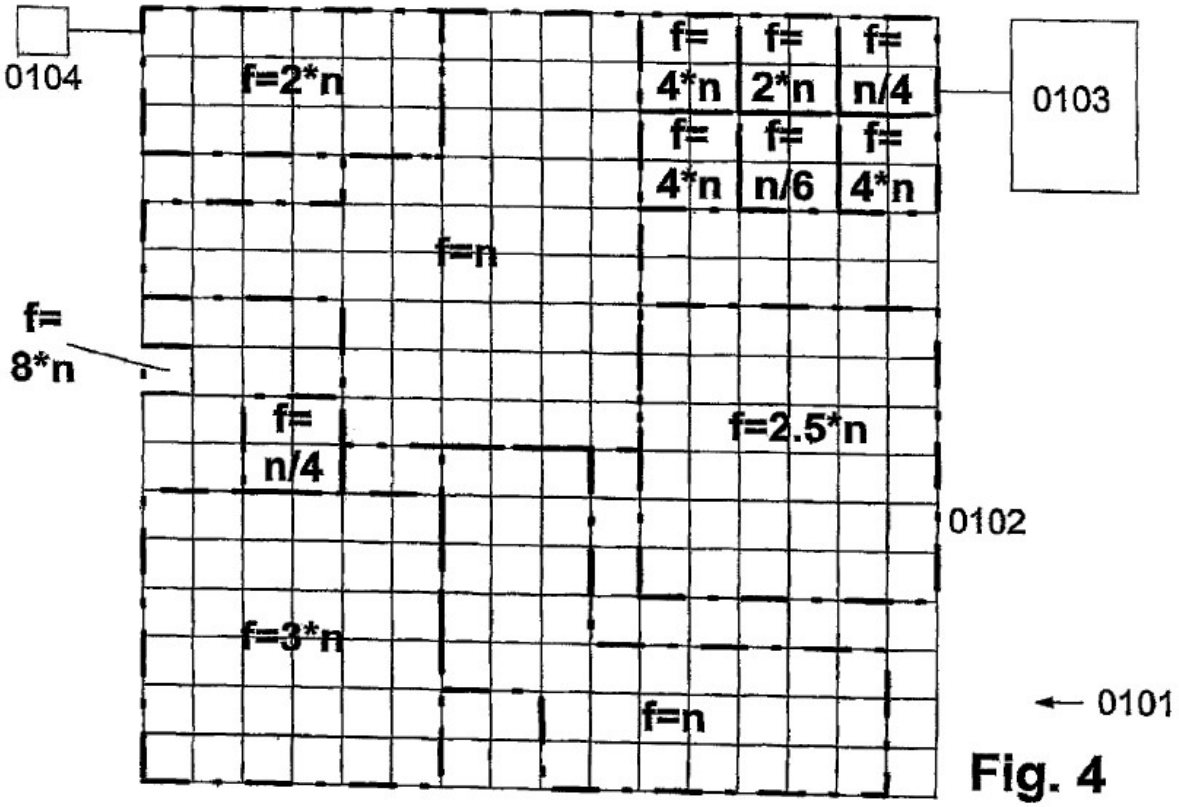


Fig. 4

III. CLAIM CONSTRUCTION

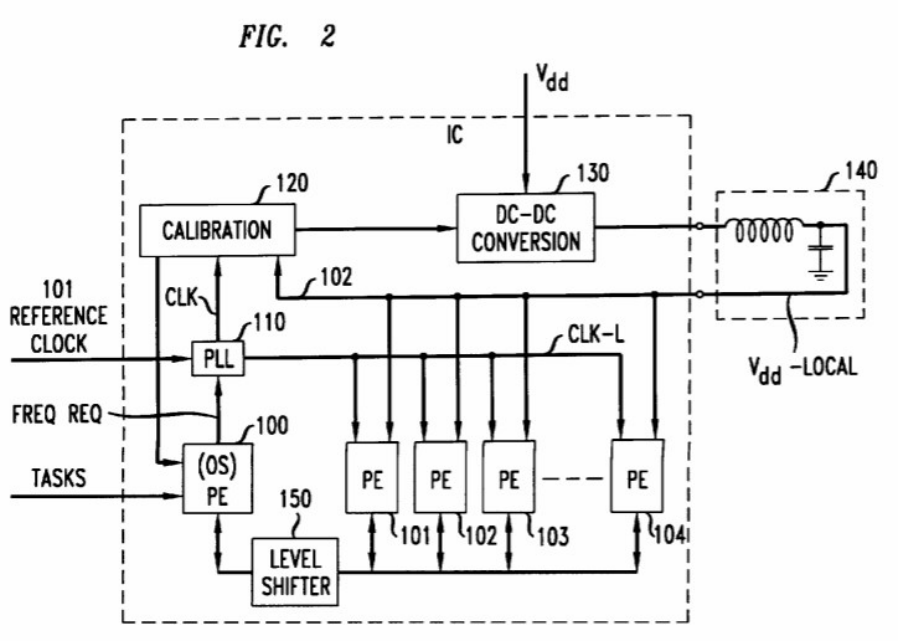
Claim terms "shall be construed using the same claim construction standard that would be used to construe the claim in a civil action under 35 U.S.C. § 282(b)." 37 C.F.R. § 42.100(b) (2018); *Phillips v. AWH Corp*., 415 F.3d 1303 (Fed. Cir. 2005) (en banc). The Petition identifies the phrases "data processing unit" and/or "data processing unit . . . adapted for sequentially processing data" and "to a minimum" as the disputed claim terms in *PACT XPP Schweiz AG v. Intel Corp.*, Case No. 1:19-cv-1006-JDW (D. Del.). Pet., 11. The terms are no longer disputed in that matter. The Court has determined that "data processing unit"

and/or "data processing unit . . . adapted for sequentially processing data" shall be construed to mean "[s]equential data processors that pass results to one or more additional data processing units to perform additional computations" and the term "to a minimum" requires no construction and is understood according to its "[p]lain and ordinary meaning." Ex. 2025, 17, 19, 20.

IV. OVERVIEW OF THE ASSERTED PRIOR ART

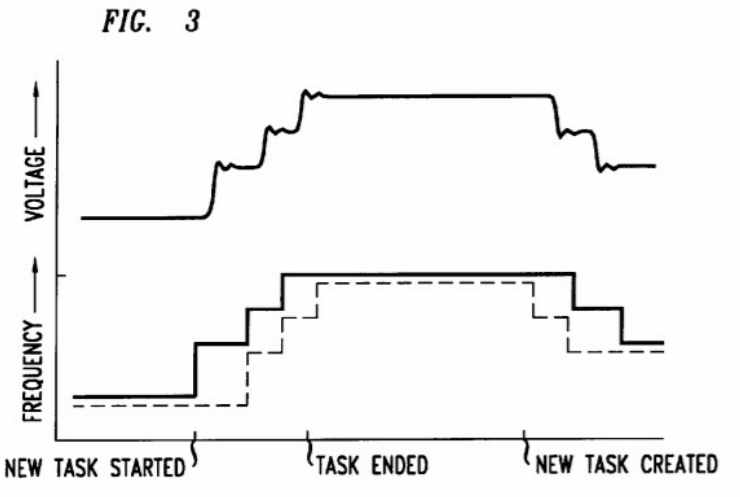
Overview of Nicol

Nicol is directed to methods for reducing power consumption of a multi-processor chip system. Ex. 1008, Abstract; 1:5-7. Specifically, Nicol describes a system that controls the voltage applied to an array of processors and the processing load assigned to each processor. *Id*. at 2:18-22. Nicol describes two different embodiments, one shown in Figure 2 and another shown in Figure 4. For the Figure 2 embodiment, all of the processors (or "processing elements") run at the same clock frequency. For this embodiment, a controller "allocates tasks to the individual processors to equalize processing load among the chips." *Id*. at 2:24. This function is performed using a scheme such as the one shown in Figure 2, which depicts "a block diagram of a multi-processor chip with supply voltage control" (*Id*. at 2:37-38) and is reproduced below:



PE 100, upon which the operating system ("OS") is run, "ascertain[s] the required completion time, divide[s] the collection of tasks as evenly as possible (in terms of needed processing time), consider[s] the PE with the tasks that require the most time to carry out, and adjust[s] the clock frequency to [e]nsure that the most heavily loaded PE carries out its assigned tasks within the required completion time." *Id*. at 3:67–4:5. After determining a clock frequency to ensure all the tasks will be completed in time, PE 100 adjusts the clock frequency by increasing the voltage in a stepped manner as shown in Fig. 3, reproduced below. *Id*. at 5:29-32. Upon completion of the first collection of tasks, a new collection of tasks is created and divided among the processors. The frequency is then gradually increased or decreased, in the same stepped manner, from the frequency set for the first

collection of tasks, to a new frequency that will ensure the most heavily loaded PE for the second set of tasks completes its assigned task in time. *Id.* at 4:54–5:2.



Nicol also discusses a separate embodiment where "each PE [has] its own supply voltage." *Id*. at 5:55-56; Ex. 2027, 19:19-21. Nicol describes the need for this embodiment: "In some applications, however, one may encounter tasks that cannot be partitioned into concurrent evenly-loaded threads" Ex. 1009, 5:60-61; Ex. 2027, 33:4-7, 33:13-16. This embodiment, depicted in Figure 4, has "[a] separate power supply for each PE in a chip" and an "operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE." *Id*. at 5:66-6:2. Because the frequency for each PE can be set independently, the lowest operating frequency for each PE can be determined based on the load on that PE. Because each PE's frequency and voltage is set independently, "[e]ach PE in Fig. 4 needs an independent controller

that performs the functions of PE 100 (except it does not divide tasks among PEs)." In Fig. 4, "all of the controllers are embodied in a single controller 200, which may be just another processing element of the integrated circuit that contains the other processing elements." *Id*. at 6:6-9. In the Figure 4 embodiment, because "the frequencies at which the individual PEs operate differ from one another and from other elements within the system where the multiprocessor chip is employed, there is an issue of synchronization that must be addressed." *Id*. at 6:14-18. "To effect such synchronization, each PE within the Fig. 4 arrangement is connection to an arrangement comprising elements 150 and 160. Level converter 150 converts the variable voltage swings of the PEs to a fixed level swing, and network 160 resolves the issue of different clock domains." *Id*. at 6:29-33. Nicol's Figure 2 embodiment does not include a network 160 because it does not have synchronization issues, since all of the PEs in Figure 2 embodiment operate at the same frequency.

Overview of Kling

Kling is directed to "limiting the power consumed in a computer system by throttling the power consumed by an integrated circuit in response to a high power condition." Ex. 1010, 1:8-10. Specifically, Kling describes a method shown in Figure 4, reproduced below, whereby the power consumed by a processor is continually measured. *Id*. at 7:41-47. When the a power consumed exceeds a

threshold, a throttle signal is sent to one or more integrated circuit of a computer system to reduce power consumption. *Id*. at 2:43-47. The threshold is set at a value that is less than a power level that would trip a fuse or circuit breaker of a power outlet from which the computer system draws power.

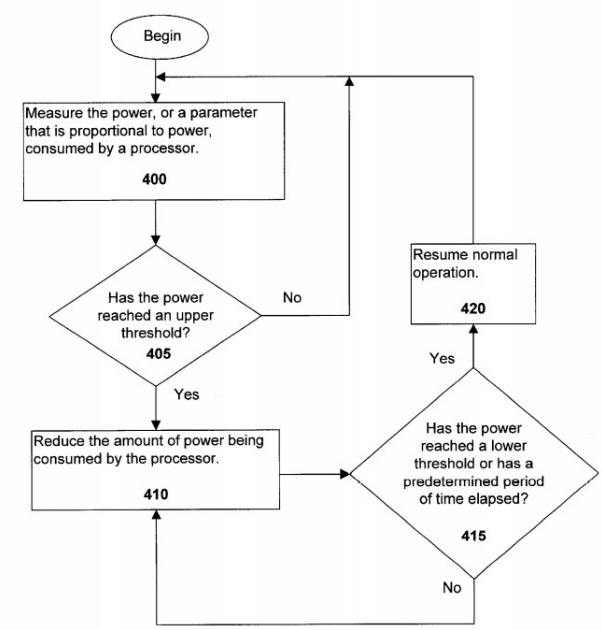


Figure 4

As shown in Figure 2B, power is decreased when an upper limit is reached. In addition, there is shown a lower limit. The lower limit acts to de-assert the throttle signal causing the integrated circuit to resume normal operations. *Id*. at 5:45-51. As a result, when activated, Kling's ICs will oscillate between the upper limit and lower limit and maintain a high processing power while avoiding tripping the circuit of a wall outlet. 5:31-37.

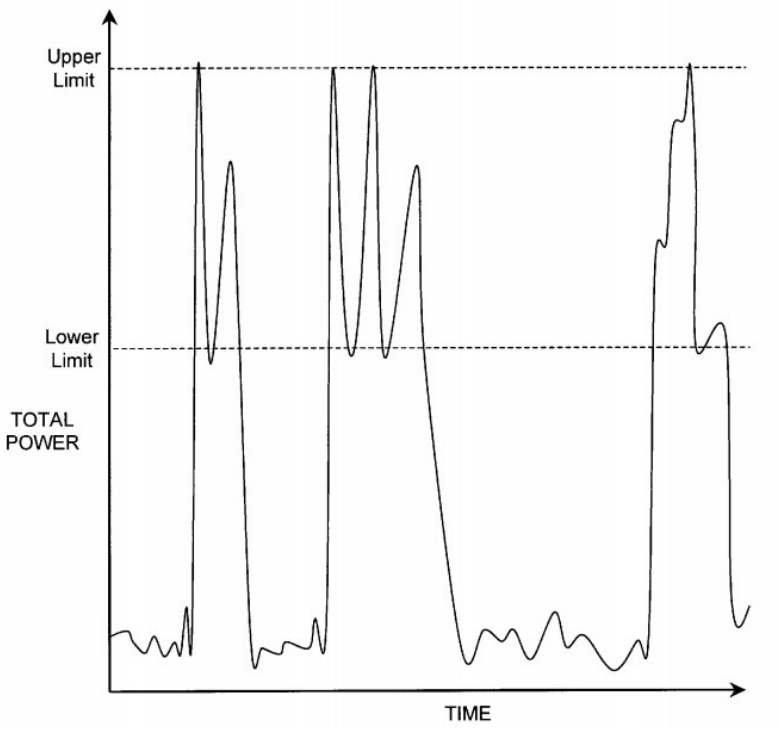


Figure 2A

In addition, Kling abandoned the indirect way of measuring power consumption through a thermal sensor, so that "temperature measurement inaccuracies related to poor positioning of thermal sensors in proximity to the processor are avoided." Ex. 1010, 2:56-58. By not using a thermal sensor, "the response time between detecting a high power condition and reducing the power consumption of the computer system is greatly improved over the use of thermal sensors to detect the high power condition." *Id.*, 2:58-62.

Overview of DeHon

DeHon is directed to a processor that includes a "gate array . . . configurable to adapt to the particular time-changing demands," which allows such processors

to "operate at speeds only achievable if the device were specifically designed for the applications." Ex. 1010 at 2:14-18.

Overview of Bhatia

Bhatia is directed to a thermal management method that monitors a temperature of a computer and changes a clock frequency of a processor according to the monitored temperature. Ex. 1009, Abstract. Specifically, Bhatia describes a process, shown in reproduced Figure 3 below, by which a computer's processor is transitioned between a high performance state and a low performance state based on a determination of whether a temperature sample ("T_n") of a thermal zone within computer exceeds a temperature threshold ("T_t"). *Id*. at 2:38-44; 3:1-3:10; 3:32-46; 7:20-45. The processor clock frequency and voltage are higher in the high performance state than the processor clock frequency and voltage in the low performance state. *Id*. at 2:36-44.

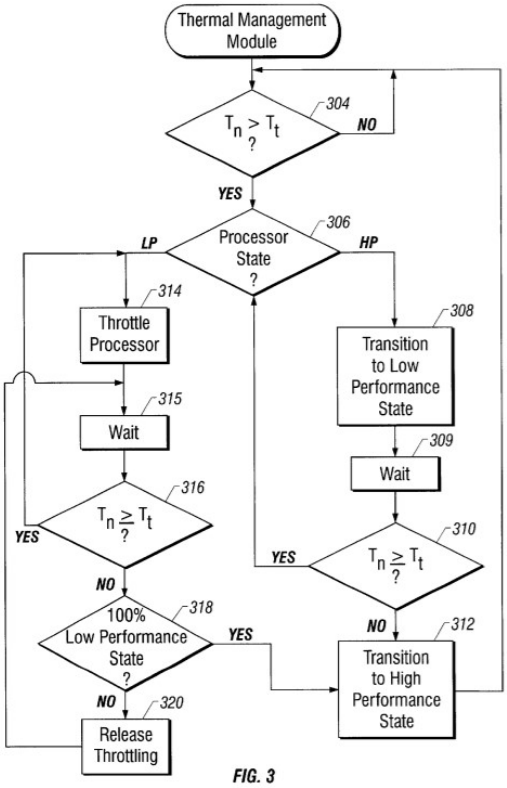


FIG. 3

Bhatia's system aims to improve on existing thermal management systems for computers by maintaining system performance at a high rate through active management of clock frequencies according to temperature measurements. *Id*. at 1:6-49. As an aside to this main purpose, Bhatia also briefly suggests that transitions between high and low performance states may also be effectuated in response to an "environmental change" such as "docking or undocking of the computer system 10 and the coupling or discoupling of the external source port 58 to an external power source." *Id*. at 12:5-12:19. These events are unrelated to temperature, but Bhatia suggests that a user may nonetheless configure a processor to trigger a switch between performance states. *Id*. Bhatia does not specify

whether or how these other triggers would be incorporated into Bhatia's thermal management system.

V. LACK OF MOTIVATION TO COMBINE THE ASSERTED PRIOR ART

Lack of Motivation to Combine the Different Embodiments in Nicol

The chip depicted in Figure 2 of Nicol and the chip in Figure 4 of Nicol are distinct embodiments with different modes of operation. Ex. 2024, ¶37. For the Figure 2 embodiment, Nicol describes a circuit which has only one voltage supply because all of the PEs are designed to operate at the same clock frequency. *Id*. Nicol describes how to balance the load "as evenly as possible" because the purpose is to find the allocation of tasks that will allow operation of the entire chip at the lowest clock frequency. *Id*. In this case, it does not make sense to allocate more tasks to one PE as that would force running that PE, and hence the entire chip, at a higher frequency in order to finish within the required completion time. *Id*. In contrast, for Figure 4 Nicol describes that "in some applications, however, one may encounter tasks that cannot be partitioned into concurrent evenly-loaded threads, and therefore, some PE within the multiprocessor would require a higher operating frequency and a higher operating voltage." Ex. 1009 5:60-61. Ex. 2027, 33:4-16. This is the motivation Nicol provides in describing the Figure 4 embodiment, where each PE has its own voltage supply, so that each PE can be operated at its own lowest operating frequency. Ex. 2024, ¶37 In this scenario,

there is no longer a need to allocate tasks as evenly as possible; indeed, Nicol's stated motivation is premised on this, and Nicol states this explicitly. *See* Ex. 1009 (Nicol) at 6:3-6 ("Each PE in Fig. 4 needs an independent controller that performs the functions of PE 100 (except it does not divide tasks among PEs)"). In this scenario, there is no longer a need to set the frequency based on the most heavily loaded PE. Ex. 2024, ¶37. Instead, each PE can be set independently, and a lowest operating frequency can be determined based on its own load. *Id*. Because of this, the Figure 4 embodiment cannot simply be combined with Figure 2 embodiment without modification. *Id*. Certainly, the disclosure about the most heavily loaded PE that Petitioner relies on is not applicable for the Figure 4 embodiment. *Id*. The features in Figures 2 and 4 are not interchangeable as Figure 2 and Figure 4 deal with different scenarios (when tasks can and cannot be evenly divided, and when frequencies for PEs cannot and can be set independently), and Petitioner has not described at all how they should be combined. *Id*. Petitioner simply treats Figure 4 and Figure 2 as if the various features are interchangeable and a POSITA would be motivated to combine these different embodiments. *Id*. This is counter to IPR case law. *See, e.g., Abiomed, Inc. and Abiomed R&D, Inc. v. Maquet Cardiovascular, LLC*, IPR2017-01204 and IPR2017-01205 (rejecting petition for failure to establish interchangeability of features of different embodiments and failure to

provide sufficient rationale to combine the teachings of those different embodiments).

VI. STANDARD OF REVIEW

"There is a significant difference between a petitioner's burden to establish a 'reasonable likelihood of success' at institution, and actually proving invalidity by a preponderance of the evidence at trial." *Trivascular,* 812 F.3d at 1068. Because, at the institution phase, the "Board is considering the matter preliminarily [and] without the benefit of a full record," "the Board is not bound by any findings made in its Institution Decision." *Id*. Findings made during trial are rendered "under a qualitatively different standard" than is used at institution. *Id*.; *see also Samsung Elecs. Co., Ltd. v. Infobridge Pte. Ltd.*, IPR2017-00100 (Paper 30), slip. op., 15 (PTAB Apr. 23, 2018).

VII. ORDINARY SKILL IN THE ART AT THE TIME OF THE CLAIMED INVENTION

Petitioner's expert, Professor Sechen, opined that a person of ordination skill in the art ("POSITA") " would have been a person with at least a Master's degree in Electrical or Computer Engineering (or equivalent), and three years of experience with processor design." Ex. 1001 (Sechen Decl.) ¶85. Patent Owner adopts this definition of a POSITA for its arguments herein.

VIII. GROUND I: PETITIONER FAILS TO PROVE NICOL IN VIEW OF KLING RENDERS CLAIMS 1-6 OBVIOUS

Nicol in view of Kling fails to disclose the features of independent claim 1. Nicol in view of Kling additionally fails to disclose the features of at least dependent claims 2-6. Ex. 2024, ¶38.

A. PETITIONER HAS NOT CARRIED ITS BURDEN TO SHOW THAT NICOL IN VIEW OF KLING RENDERS OBVIOUS INDEPENDENT CLAIM 1

Nicol, upon which Petitioner relies, fails to disclose "being adapted for sequentially processing data," "setting a clock frequency, of at least a part of the multiprocessor system to a minimum," "increasing the clock frequency of the at least the part of the multiprocessor system to a maximum in accordance with a number of pending operations of a second processor," "reducing the clock frequency of the at least the part of the multiprocessor system in accordance with . . . an operating temperature threshold preventing over-temperature," and "reducing the clock frequency of the at least the part of the multiprocessor system in accordance with . . . a hysteresis characteristic." as recited in claim 1. Ex. 2024, ¶39.

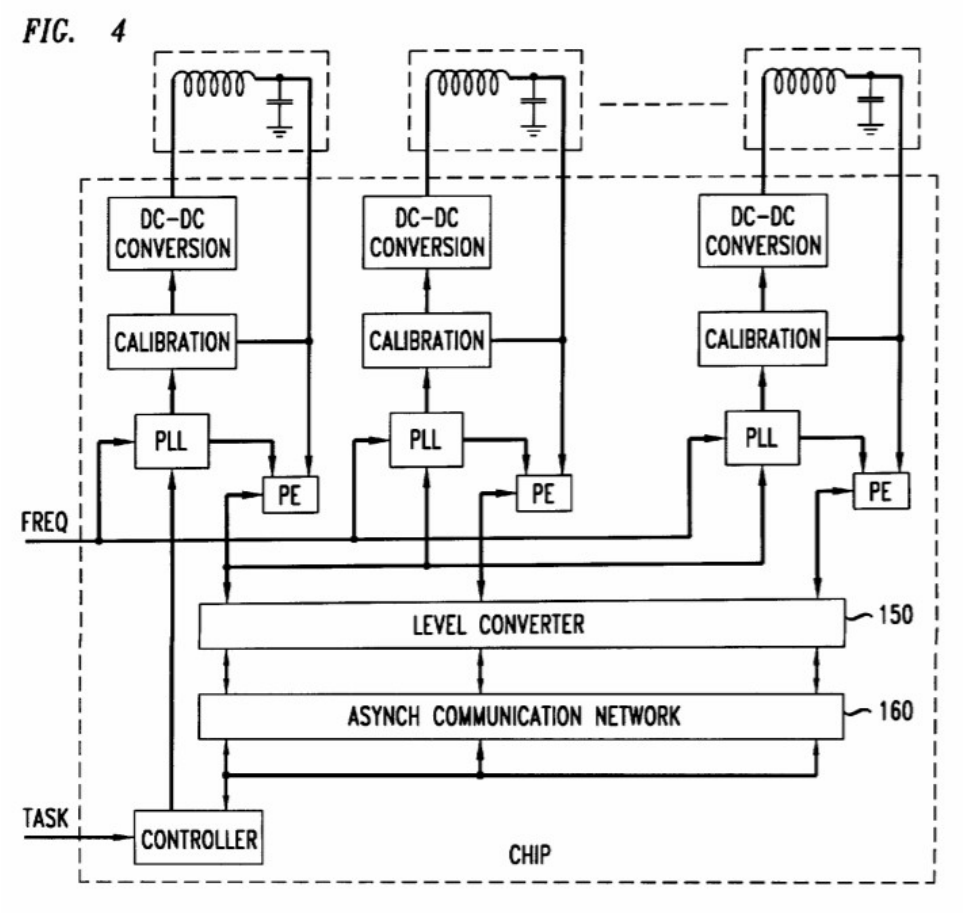
(a) Petitioner has not Carried its Burden to Show That Nicol in view of Kling discloses "being adapted for sequentially processing data"

Petitioner argues that a POSITA would understand Nicol's inclusion of an asynchronous communication network ("ACN") to teach sequentially processing

data based on Petitioner's three step analysis. Pet., 31; Ex. 2024, ¶40. Petitioner argues (a) ACN would not have been necessary if Nicol's PEs were not configured to pass results of their tasks to other processors, *id*. at 31-32; (b) systems designed to handle digital signal processing ("DSP") applications **typically** involve a pipeline process whereby PEs pass data from one to the next in a sequence, *id*. at 33; and (c) Nicol's system **could be** configured like a systolic architecture, *id*. at 34-35. Beyond Petitioner's admission that its analysis rests on mere possibilities (which do not support the contention that a POSITA would assume an ACN implies programmable processing sequences), each step of Petitioner's analysis is flawed. Ex. 2024, ¶40.

(i) Petitioner's Evidence Does Not Show that a POSITA Would Understand an ACN to Imply Passing of Data or Instructions Between Processors

As shown below, Nicol's Fig. 4 includes a level converter and asynchronous communication network connecting a controller and the PEs:



Ex. 2024, ¶41. The level converter and ACN are used to effect synchronization required because the PEs operate at different voltages and frequencies. Ex. 1008, 6:29-33; Ex. 2024, ¶41. The level converter (also known as a level shifter or level translator) receives data signals from each of the PEs, which are supplied with different amounts of power from the various DC-DC converters, and converts the signals to signals with a common power level. Ex. 1009, 6:31-32 (" Level converter 150 converts the variable Voltage Swings of the PES to a fixed level Swing"); Ex. 2024, ¶41. The level converter then transmits the modified data signals to the ACN which is configured to receive and coordinate data from the

individual PEs which output data at different times. Ex. 1009, 6:33 ("[N]etwork 160 resolves the issue of different clock domains."); Ex. 2024, ¶41. The PEs in Fig. 4 operate at different clock frequencies. Ex. 1009, 6:14-17; . The ACN is needed to receive data from the PEs at different times, coordinate the data as part of the same set of tasks, and pass the coordinated data along to the controller. *Id*. The use of the ACN does not necessitate communication across the PEs, much less imply that sequential data pEx. 2024, ¶41rocessing is performed. *Id*. Petitioner insists to the contrary. Pet., 31-32. However, Petitioner's Expert's conclusion based on Nicol is unfounded. Petitioner concludes, quoting Nicol, that "the asynchronous communication network is provided, *solely*, in the situation where there is 'a need to communicate data between PEs (or with other system elements).'" *Id*. (emphasis original). The passage from Nicol in appropriate context, states only that "a synchronization schema must be implemented when there is a need to communicate data between PEs." Ex. 1009, 6:19–21. Nicol describes a situation when a synchronization schema is needed ("when there is a need to communicate data between PEs"), not that the use of a synchronization schema necessarily implies that data is being communicated between PEs. Ex. 2024, ¶41.

Nonetheless, Petitioner refers to the coprocessor configuration described in Ex. 1010, Hayes, John, Computer Architecture and Organization (third edition),

McGraw-Hill International Edition: Computer Science Series (1998) ("Hayes Textbook") to argue that the ACN necessarily implies communication between PEs. Pet., 34; Ex. 2024, ¶42. The comparison is unfounded for two reasons. Ex. 2024, ¶42

First, Nicol and Hayes Textbook describe two distinct systems. Ex. 2024, ¶43. Nicol describes a multi-processor system where "each PE contains a central processing unit (CPU) and a local cache memory." Ex. 1009, 2:51-53; Ex. 2024, ¶43. Hayes Textbook, on the other hand, describes a processor and floating point coprocessor configuration within a single CPU. Ex. 1022, Fig. 3.14; Ex. 2024, ¶43. Additionally, unlike the processors in Nicol, Hayes Textbook's coprocessor is a "specialized instruction execution unit" that does not include its own cache memory. Ex. 1022 at 159; Ex. 2024, ¶43. The coprocessor is designed only to execute specific floating point operations which are sent directly by the microprocessor, which fetches and decodes instructions and transfers only the command portions to the coprocessor. *Id*. Accordingly, Hayes Textbook's coprocessor configuration is not analogous to Nicol's multi-processor system, and a POSITA would not look to Hayes Textbook to understand Nicol's can.

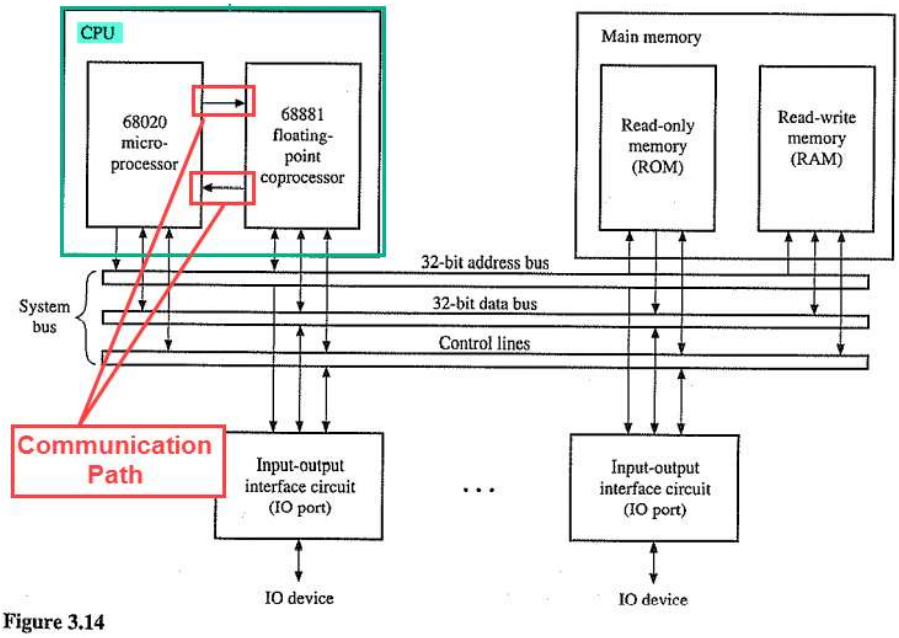


Figure 3.14

Second, even if a POSITA were to consider Hayes Textbook, the disclosure Petitioner points to does not show that an ACN implies data communication between processors. Ex. 2024, ¶44. Petitioner suggests that the microprocessor and coprocessor of Hayes Textbook's would communicate along the 32-bit data bus shown in Fig. 3.14. Pet., 32. However, Fig. 3.14 indicates that the microprocessor and coprocessor communicate directly within the CPU, and a POSITA would not expect processors within a CPU to communicate over an external system bus. Ex. 2024, ¶44. Because the microprocessor and co-processor communicate directly and are unlikely to communicate across the bus, a POSITA would not assume that a bus connected to multiple processors (as in Nicol) implies it is used by the processors to share data between them. *Id*

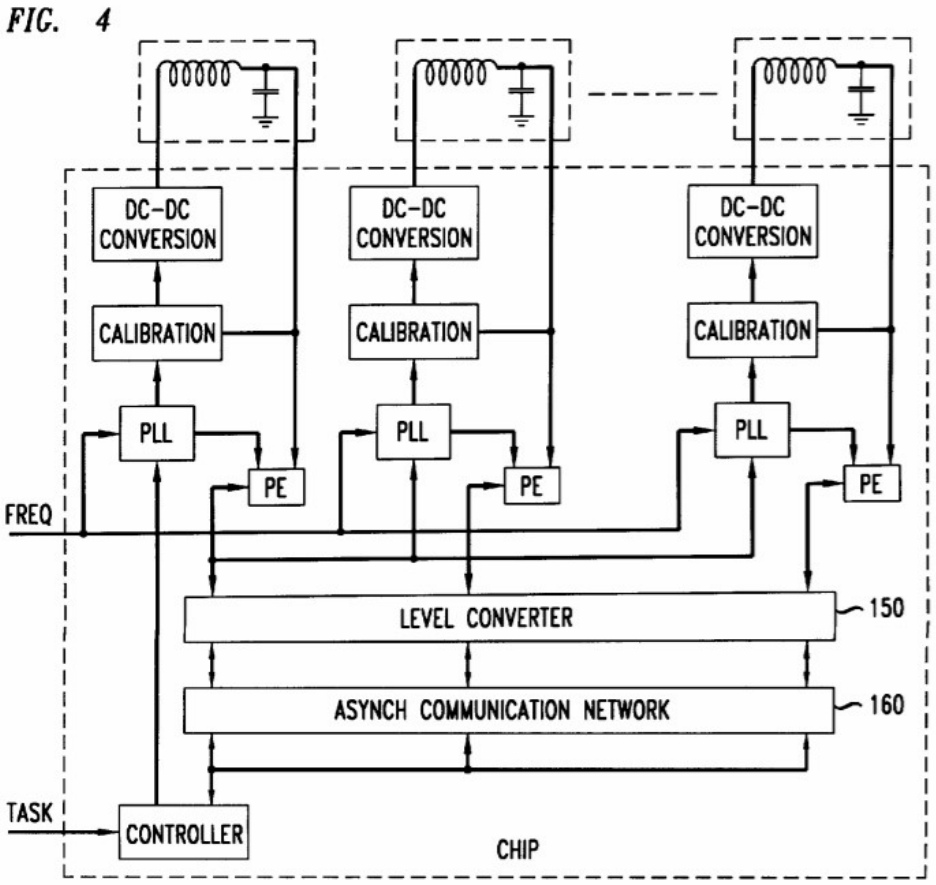
(ii) Nicol's Digital Signal Processing does not Require a Pipeline Process with PEs Passing Data in a Sequence

Petitioner seems to argue that because Nicol performs digital signal processing and digital signal processing is allegedly typically performed using a chain of processors, Nicol must be performed in the same manner as, for example, Exhibit 1026 ("Williams"). Pet., 33; Ex. 2024, ¶45. First, it is inaccurate to say that digital signal processing is "typically" performed using a chain of processors – there are a multitude of architectures for performing digital signal processing. Ex. 2024, ¶45. Next, Nicol does not suggest that it would process data according to the configuration shown in Williams. Williams is directed to graphics processing. *Id*.; *see , e.g.,* Ex. 1026, Abstract. Graphics processing is not a form of digital signal processing. Nicol provides no indication that it is designed to perform graphics processing. Ex. 2024, ¶45. Williams' system includes a pixel operations unit, a rasterization unit, a per fragment operations unit, and a frame buffer. Ex.1026, 10:56–11:19; Ex. 2024, ¶45. Nicol does not mention any of these elements, the functions of any of these elements, or even the concept of graphics processing. Ex. 2024, ¶45. Accordingly, a POSITA would not read Nicol to disclose a specific configuration that is designed to perform a specific type of processing that Nicol never mentions. *Id*.

(iii) A POSITA Would not Modify Nicol's Multiprocessor System to Operate as a Systolic Architecture.

Petitioner argues that a POSITA would have known that the PEs in Nicol's multiprocessors system could be configured to operate as a systolic architecture. Pet., 34-35. This is incorrect. Ex. 2024, ¶46. A POSITA would understand that Nicol would not and could not be operated as a systolic architecture. *Id*.

Systolic architecture refers to a chain of processors hardwired in series. *Id*. at ¶47. It has a very narrow set of applications and requires complicated analysis and planning before data is transmitted to the systolic architecture. *Id*. It could not be used in Nicol's architecture which, as shown below in reproduced Fig. 4, includes processors connected in parallel. *Id*. Moreover, Petitioner's Expert argues that in a systolic array, "[d]ata words flow *synchronously*." Ex. 1001, ¶159; Ex. 2027, 44:14-45:18. Petitioner and Petitioner's expert offer no explanation as to how an asynchronous system, such as Nicol's Fig. 4, could be combined (much less why a POSITA would be motivated to combine them) or whether and how it would work in an asynchronous manner, which is how Nicol describes its ACN.



(b) **Nicol in view of Kling does not disclose "setting a clock frequency, of at least a part of the multiprocessor system to a minimum"**

(i) **Petitioner Mixes Embodiments Without Justification**

Petitioner improperly points to features from different embodiments in Nicol without explaining how they are interchangeable or how they fit together into a single system. Ex. 2024, ¶48. Petitioner starts by showing an annotated picture of Figure 4, but throughout the text points to passages that describe the Figure 2

embodiment. *Id*. Petitioner needs to rely on Figure 4 for other limitations of claim 1. As described in Section V. above, a POSITA would not be motivated to combine the Figure 2 and Figure 4 embodiments of Nicol. *Id*.

For example, Petitioner points to a disclosure from Nicol that the controller "allocates tasks to the individual processors to equalize processing load among the chips, then the controller lowers the clock frequency on the chip to as low a level as possible while assuring proper operation, and finally reduces the supply voltage." Ex. 1009, at 2:23-27. The equalizing of processor load describes the process followed in the context of Figure 2, where the entire chip (all of the processing elements) is set to the same frequency. Ex. 2024, ¶49. That is the motivation for equalizing the processing load, so that no PE takes (significantly) longer to complete its tasks. *Id*. This is a different scenario from Figure 4, where "the operating system [can] independently program the lowest operating frequency and corresponding lowest supply voltage for each PE." Ex. 1009 (Nicol) at 5:67-6:2; Ex. 2027, 19:19-21; Ex. 2024, ¶49.

Petitioner then relies on disclosure from Nicol that states: "If the number of instructions that need to be executed for each task is known and made available to the operating system, a scheduler within the operating system can use this information to determine the best way to allocate the tasks to the available processors in order to balance the computation." Ex. 1009, 3:13-18. Petitioner

omits the very next sentence which states: "The intermediate goal, of course, is to maximize the parallelism and to evenly distribute the load presented to the Fig. 2 system among all of the PE's." *Id*. at 3:19-20. Again, this describes the Figure 2 embodiment where the load is distributed as evenly as possible. Ex. 2024, ¶50. This is exactly opposite to the situation that Figure 4 embodiment addresses: "In some applications, however, one may encounter tasks that cannot be partitioned into concurrent evenly-loaded threads" Ex. 1009, 5:60-61; Ex. 2027, 33:4-7, 33:13-16. Thus, not only does Petitioner attempt to point to two separate embodiments in Nicol without providing any motivation to combine or explain how they may fit together – these two embodiments are not intended to be combined as they use different modes of operation to address different scenarios. Ex. 2024, ¶50.

(ii) **Petitioner Does Not Show "in accordance with number of pending operations of a first processor"**

Petitioner points to an arbitrary "PE" in the annotated Figure 4 as the First Processor (PE1), but does not show that the clock frequency is set based on the number of pending operations of PE1. Ex. 2024, ¶51. For Figure 4, Nicol describes that "[a] separate power supply for each PE in a chip overcomes this limitation by allowing the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE… Each

PE in Fig. 4 needs an independent controller that performs the functions of PE 100 (except it does not divide tasks among PEs)." Ex. 1009 (Nicol) at 5:66-6:6. That is, rather than using the technique described for figure 2 (divide the tasks among the PEs as evenly as possible), each PE can set its own operating frequency independently and the controller does NOT divide the tasks among the PEs. Ex. 2024, ¶51. Thus, PE1 does not set the frequency of the system, but only its own operating frequency. *Id*.

(iii) **Petitioner Misinterprets Gated Clock Disclosure**

Petitioner also points to a gated clock disclosure where certain clock frequencies are set to zero, and claims it is additional disclosure of the minimum frequency required by this claim limitation, but Petitioner misreads Nicol. Ex. 2024, ¶52. Petitioner points to the disclosure "the operating system employs gated clocking techniques to 'shut down' PEs that are not needed," (Ex. 1009, 5:42-44) and simply assumes without considering the context that this is done in accordance with the number of pending operations. Ex. 2024, ¶52. But read in context, this is not what Nicol describes. *Id*. The fuller passage is below:

> Of course, V_{dd}-local can only be reduced so-far before the circuits start to fail, at which point the operating system employs gated clocking techniques to 'shut down' PEs that are not needed.

Ex. 1009, 5:41-44. Nicol is here describing the need to shut down certain circuits because they fail due to low voltage. This passage does not describe how clock frequencies are set according to the number of pending operations (of any processor). Ex. 2024, ¶52. This is not a disclosure of "a minimum in accordance with a number of pending operations of a first processor" as required by the claim. *Id*.

(iv) **ACPI is Not Disclosed in Either Nicol or Kling, and Bhatia and ACPI Are Not Part of the Ground**

Petitioner further relies on states disclosed in the Advanced Configuration and Power Interface (ACPI) Specification for this limitation. But ACPI is mentioned in neither Nicol or Kling. Ex. 2024, ¶53. Instead, Petitioner and its expert Dr. Sechen simply assert in conclusory fashion that ACPI "was commonly used and referred to by a POSITA" (Pet., 38; Ex. 1001, ¶ 170) without any explanation. Ex. 2024, ¶53. In order to overcome the fact that neither of the references, Nicol or Kling, that are part of the ground mention ACPI, Petitioner introduces Bhatia (Ex. 1011) and the ACPI Specification itself (Ex. 1020). But neither of these are part of the ground, nor does Petitioner provide a motivation to combine these references with Nicol or Kling. Ex. 2024, ¶53. Petitioner cannot use this method to combine a third or fourth reference and avoid establishing a motivation to combine. Furthermore, Petitioner asserts that a POSITA would

know to use a particular low power mode C3 without any explanation other than that it preserves memory contents. But Nicol and Kling do not use preservation of memory contents to determine the clock frequency. Ex. 2024, ¶53. Indeed, if this is the reason a POSITA would look to the C3 state, this runs counter to the claim itself. *Id*. The claim requires that the clock frequency is set in accordance with a number of pending operations of a first processor. *Id*. The claim does not state that the preservation of memory contents is a consideration in setting the clock frequency. *Id*. Petitioner never ties the C3 state to the number of pending operations of a first processor, and only mentions a vague reference to low-power mode. *Id*.

(v) **Inconsistent interpretation of "minimum" is fatal to the motivation to combine.**

For this limitation, Petitioner points to three separate examples of a "minimum": 70 MHz disclosed in Figure 3 of Nicol, clock gating with a frequency of zero, and the ACPI C3 state. Ex. 2024, ¶54. As discussed above, these three disclosures are described for different purposes, and a POSITA would not be motivated to combine them. *Id*. But further, Petitioner provides no motivation why a POSITA would look to use multiple different modes of operation with different minimum frequencies in a single combined embodiment. *Id*. In fact, the plain meaning of the word "minimum" is to take the lowest, and a POSITA would not

try to combine these three different disclosures if the purpose were to try to find a minimum, and instead focus on using the lowest one if power savings were the motivation. Petitioner is the one with the burden of proof. *Id*. Disclosing three different "minima" does not improve the motivation to combine the different references or disclosures, and in fact makes it worse as it highlights and contrasts the different purposes of each. *Id*.

(c) Petitioner has not Carried its Burden to Show That Nicol in view of Kling discloses "increasing the clock frequency of the at least the part of the multiprocessor system to a maximum in accordance with a number of pending operations of a second processor"

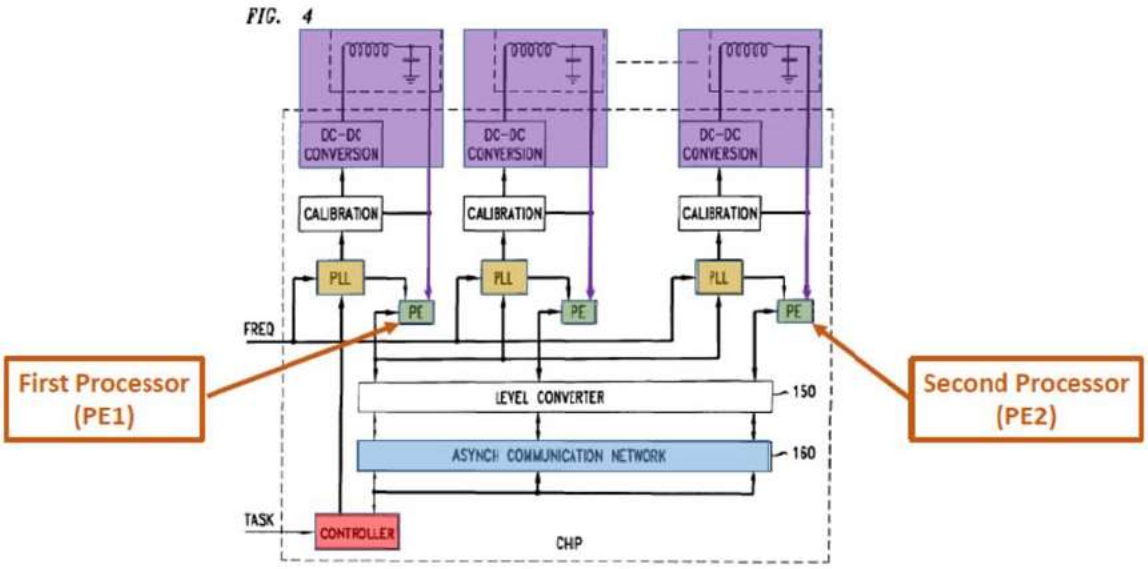
(i) Petitioner Mixes Embodiments Without Justification

As with the limitation immediately above, Petitioner mixes embodiments by citing to an annotated version of Figure 4 while quoting portions of Nicol describing the Figure 2 embodiment. Ex. 2024, ¶55. Petitioner's showing on this limitation therefore fails for the same reasons discussed above in Section V. *Id*.

(ii) Petitioner Fails to Establish a "second processor" and that a clock frequency is set "in accordance with number of pending operations of a second processor"

This limitation requires "increasing the clock frequency of the at least ***the*** part of the multiprocessor system to a maximum," where "the" part of the

multiprocessor system must be the same part of the multiprocessor system that was identified for the previous limitation, which describes "a part of the multiprocessor system." Ex. 2024, ¶56. Petitioner identifies specific PE's for the first processor and the second processor in its annotated Figure 4:



Petition at 60; Ex. 2024, ¶56.

Nicol's Figure 4 embodiment has "[a] separate power supply for each PE…allowing the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE." Nicol at 5:66-6:2. Thus, each PE's operating frequency is set independently based on its own load. PE1's operating frequency is set according to PE1's load, PE2's operating frequency is set according to PE2's load, etc. Ex. 2024, ¶57. In the Figure 4 embodiment, the clock frequency is not set according to what Petitioner describes

("Specifically the controller takes into account the number of pending instructions for each PE – including PE1 ("first processor") and PE2 ("second processor") – because it sets the clock frequency based on identifying the processing requirement of 'the most heavily loaded PE.'" (Pet, 40; Ex. 1001, ¶176)). As described in Section V., the reference to "most heavily loaded PE" occurs in the context of the Figure 2 embodiment, which is not applicable here for Figure 4. Ex. 2024, ¶57.

For the previous limitation, Petitioner pointed to PE1 as the "first processor" and thus "***a*** part of the multiprocessor system" referred to PE1 (the only part of the system whose frequency is determined by the load on PE1), while here Petitioner points to PE2 as the "second processor," whose load only determines the frequency of PE2, which must map to "***the*** part of the multiprocessor system." Id. at ¶58. If Petitioner is asserting that PE2 is "***the*** part of the multiprocessor system," it is different from "***a*** part of the multiprocessor system" from the previous limitation, and thus Petitioner has failed to show how this limitation is met by the disclosures of Nicol. *Id*. Alternatively, if Petitioner is asserting that "***the*** part of the multiprocessor system" is PE1, the clock frequency of PE1 is not determined "in accordance with the number of pending operations of a second processor (PE2)." *Id*.

(iii) **Petitioner has Failed to Establish "in accordance with number of pending operations**

of a second processor" for this limitation in any embodiment

Even if we were to assume that the Figure 2 disclosure in Nicol is applicable for the Figure 4 embodiment which Petitioner identifies in its annotated figure, Petitioner has still failed to identify the clock frequency is set "in accordance with the number of pending operations of a second processor." Id. at ¶59. Petitioner (and its expert) states that "it [the controller] sets the clock frequency based on identifying the processing requirement of 'the most heavily loaded PE.'" (Pet., 40; Ex. 1001, ¶176). This is the same way clock frequency was determined for PE1, as Petitioner also pointed to disclosures describing Figure 2, where the system attempted to "equalize processing load among the chips." Ex. 2024, ¶59. Petitioner has presented no reason why the description of the same technique for determining clock frequency in the Figure 2 embodiment of Nicol would consider a different PE, when the disclosure of Nicol is clear that the "most heavily loaded PE" is used to set the clock frequency in that embodiment. Id. Therefore, Nicol does not disclose setting a clock frequency in accordance with the number of pending operations of a second processor – in the Figure 2 embodiment, the clock frequency always relies on the load of the most heavily loaded PE. *Id*.

(iv) Nicol Does Not Teach Setting Both PEs to 140 MHz

Petitioner identifies 140 MHz in its annotated Figure 3 of Nicol as the maximum frequency, and suggests "the clock frequency of the PEs" is set to this value in Nicol. Petitioner cites to 3:31-33 as support for this, but a closer look at Nicol suggests this misreads Nicol. Ex. 2024, ¶60. Nicol describes an example where "a given application that is executed on 1 PE requires operating the PE at 140 MHz" (Nicol at 3:31-33). Nicol further suggests that "the application is divided into two concurrent tasks and assigned to two PEs that are designed to operate at 140 MHz from a 2.7 V supply, then the PEs can be operated at 70 MHz and at a supply voltage of 1.8 V." (Nicol at 3:34-37). Nicol explains: "It should be understood that in the above example, when two PEs are employed and their operating frequency can be reduced to 70 MHz, the indicated reduction presumes that it is desired to perform the given tasks as if there was a single PE that operates at 140 MHz." (Ex. 1009, 3:43-47). That is, Nicol teaches dividing the task so that it runs on two separate PEs each running at 70 MHz. Ex. 2024, ¶60. Nicol does not teach running both PEs at 140 MHz, and suggests instead running at lower frequencies to save power. Petitioner's suggestion that the system is set to 140 MHz for all of the PEs in the system is not what Nicol teaches. *Id*. Petitioner's expert agrees that Nicol does not suggest setting both PEs to 140 MHz in this

example. *See* Sechen Depo at 16:14-17:11. Petitioner provides no explanation how the example described in Nicol with respect to Figure 2 supports setting all PE's of the system to 140 MHz in Figure 3 "in accordance with the number of pending operations of a second processor." Ex. 2024, ¶60.

(v) Nicol's Purpose is to Reduce Power

Petitioner points to Nicol's disclosure of "[f]or a maximally utilized system, all of the available processors ought to be operating at full speed when satisfying the maximum load encountered by the system." Ex. 1001, 2:65-67). Nicol goes on to say that "typically, computers spend 99% of their time waiting for a user to press a key. Ex. 1009, 3:4-7. This presents a great opportunity to drastically reduce the average power consumption." Id.; Ex. 2024, ¶61. Indeed, Nicol's title is "Power Reduction" and the abstract discusses "minimiz[ing] overall power consumption" and the summary of the invention also suggests "minimiz[ing] overall power consumption." Ex. 1009, 2:22). Petitioner also characterizes Nicol in such a way, describing Nicol as "directed to reducing power consumption of a multiprocessor system or chip." Pet., 11; Ex. 1001,¶91). In other words, Nicol's teaching is about how to avoid running the system at full speed as much as possible, and its descriptions focus on how to avoid running the system at the maximum frequency. Ex. 2024, ¶61. Petitioner's expert has characterized Nicol as

follows in a declaration in an *inter partes* review for the '047 patent which shares the same specification and for which Petitioner has asserted the identical reference Nicol: "Nicol generally discloses power minimization of a multiprocessor DSP chip." IPR2020-00539, Sechen '047 Decl. (Ex. 1001) at ¶215. Therefore, Nicol does not suggest running the system at a maximum frequency, and instead describes the maximal load as a possibility to avoid. Ex. 2024, ¶61. In addition, Nicol never connects this maximal load to the number of pending operations of PE2 that Petitioner identified. *Id*. Petitioner never connects this disclosure in Nicol to the embodiments in Figure 2 (which teaches away from using 2 PEs at 140 MHz) or Figure 4, where each PE is set according to its own load. *Id*.

(d) **Petitioner has not Carried its Burden to Show That Nicol in view of Kling discloses "reducing the clock frequency of the at least the part of the multiprocessor system in accordance with . . . an operating temperature threshold preventing over-temperature"**

Petitioner admits that Nicol does not discuss over-temperature. Pet., 24. Petitioner therefore relies entirely on Kling. For at least the reason discussed in section VIII.G., Petitioner fails to provide sufficient motivation to suggest Nicol and Kling can be combined, and thus fail to establish Nicol and Kling teach this element. Ex. 2024, ¶62. In addition, Nicol discusses voltage scaling based on temperature variations, but not clock frequency changes. *Id*. A reduction in clock

frequency due to temperature would prevent tasks from being completed on time. *Id*.

(e) **Petitioner has not Carried its Burden to Show That Nicol in view of Kling discloses "reducing the clock frequency of the at least the part of the multiprocessor system in accordance with . . . a hysteresis characteristic"**

Petitioner relies entirely on Kling to teach this claim element and only on a single passage at that: "In accordance with this embodiment, the lower threshold may be set to a predetermined value selected to provide hysteresis to reduce the occurrence of power oscillation between the upper and lower thresholds." Pet., 44 *quoting* Ex. 1010, 5:51-54. Petitioner argues that "a POSITA would have found it obvious to apply the well-known two threshold method (providing hysteresis) from Kling to implement an over-temperature monitoring system in Nicol . . . to reduce unwanted oscillations, and thus to improve the reliability and performance of Nicol's power management system." *Id*. at 45.

Once again, Petitioner confuses benefit and motivation, relying on hindsight rather than focusing on what a POSITA would have been motivated to do at the time of the invention. Ex. 2024, ¶64. Kling describes that hysteresis could be used to reduce power oscillation. Ex. 1010,54-59. It provides no explanation as to how hysteresis would be implemented (power limits do not constitute a particular form of hysteresis – they are merely input conditions to a hysteretic system) or how it

could be implemented in alternative systems such as Nicol. Nicol, for its part, makes no mention of hysteresis and provides no insight as to how the undescribed hysteresis method from Kling could be introduced. Ex. 2024, ¶64 Accordingly, Petitioner relies improperly on benefit alone. *Id*.

Nonetheless, Petitioner argues, based on Kling's single mention of the term hysteresis and Ex. 1021 (Kennedy, M. & Chua, L., Hysteresis in Electronic Circuits: A Circuit Theorist's Perspective, International Journal of Circuit Theory and Applications, Vol. 19, (1991)("Kennedy")) that Kling's undescribed implementation of hysteresis was so well known that a POSITA would be motivated to add it to Nicol to reduce unwanted oscillation. This argument fails for three reasons: (1) Petitioner does not point to any unwanted oscillation in Nicol or a need to reduce such unwanted oscillation through hysteresis;[1] (2) a single mention of hysteresis in Kling is insufficient to show that the undescribed implementation of hysteresis was so well known; and (3) Petitioner interprets Kennedy to suggest that hysteresis was "'indispensable' and commonly used 'in noisy environments and to guard against false triggers,'" Pet., 44, but Kennedy makes no such claim. Ex. 2024, ¶65. The first two reasons are self-explanatory. *Id*.

[1] In a related matter, IPR2020-00539, Petitioner makes arguments that could potentially be applied to suggest Nicol includes unwanted oscillation, but those arguments are made using a different combination of references, using different terminology, and for distinct claim element. Patent Owner assumes that any such argument is inapplicable herein, or Petitioner would have raised it. Patent Owner cannot be expected to respond to arguments Petitioner has not made.

With respect to the third, Petitioner quotes Kennedy out of context. Kennedy does not state that hysteresis is indispensable in noisy environments; Kennedy recites "[hysteresis] elements have become indispensable building blocks ***in a variety of noise rejection and oscillator circuits***." Ex. 1021, 471 (emphasis added); Ex. 2024, ¶65. That is, when using certain noise rejection and oscillator circuits, hysteresis elements are indispensable. Ex. 2024, ¶65. Not for a full system such as Nicol. *Id*. Not for all circuits. *Id*. Not for all types of noise rejection and oscillator circuits. *Id*. Hysteresis is only indispensable for certain noise rejection and oscillator circuits. *Id*. Petitioner points to neither a noise rejection nor an oscillator circuit in Kling and Nicol. *Id*. Indeed, neither reference discusses specific circuit level architecture. *Id*. Accordingly, it is inaccurate, based on Kennedy, to say that hysteresis was indispensable in all systems that include unwanted noise (which is every system), and there is no evidence that hysteresis would be indispensable in Nicol. *Id*. Indeed, Nicol describes an alternative method for dealing with noise. Ex. 1009, 5:29-31 ("[T]he frequency is gradually programmed into the system . . . [to] prevent[] excessive noise."); Ex. 2024, ¶65.

B. Petitioner has not Carried its Burden to Show That Nicol in view of Kling Renders Obvious Dependent Claim 2

Petitioner has not shown that Nicol in view of Kling renders obvious the "clock frequency [being] determined in part by processor voltage." Ex. 2024, ¶66.

Petitioner does not argue that Nicol alone discloses this element. In Nicol, the clock frequency is determined by the processing load and the completion time, not by the voltage. Ex. 2024, ¶67. As stated in the Abstract, "[the] controller in [Nicol's] multi-processor chip allocates tasks to the individual processors to **equalize processing load** among the chips, **then** the controller **lowers the clock frequency on the chip to as low a level as possible while assuring proper operation**, and **finally reduces the supply voltage**." Ex. 1009, Abstract (emphasis added). Specifically, "the operating system of PE 100 needs to **ascertain the required completion time**, divide the collection of tasks as evenly as possible (in terms of needed processing time), consider the PE with the tasks that require the most time to carry out, and **adjust the clock frequency to insure that the most heavily loaded PE carries out its assigned tasks within the required completion time**." Ex. 1009, 3:66-4:5. A POSITA would have understood that Nicol's clock frequency is jointly determined by the processing load and the required completion time. Ex. 2024, ¶67. Specifically, Nicol's clock frequency is minimized to the value necessary to finish the tasks within the required completion time. *Id*. A POSITA would have understood that the clock frequency in Nicol is not determined by voltage. *Id.*.

Intel relies on Kling for this element. *See* Pet., 46. Kling is about sending throttle signals "if the power consumed by the portion of the computer system

reaches a threshold." Ex. 1010, Abstract. The power is measured by a meter, "tak[ing] a measurement of a parameter that is approximately proportional to the power consumed from the power supply by at least a portion of a computer system. This parameter may include, for example, the current or **voltage between the power supply and the portion of the computer system**, or the duty cycle of a switching signal in the power supply." *Id*. (emphasis added). Petitioner alleges that the voltage measured in Kling discloses the claimed "processor voltage." See Pet. at 46 ("'a parameter that is approximately proportional to the consumed power, ***such as voltage*** . . .' is tracked. Ex. 1010, 2:31–37. . . . "[C]urrent consumed by a processor is tracked by measuring 'a voltage across a resistor' of the processor as would have been well-known in the art." Ex. 1010, 3:57–59; Ex. 1001 ¶195.).

Petitioner alleges that "current consumed by a processor is tracked by measuring '**a voltage across a resistor' of the processor** as would have been well-known in the art." Pet., 46 (emphasis added). The underlined statement is incorrect, because the referenced "resistor" is not part of the processor. Ex. 2024, ¶69. A POSITA would have understood that the voltage measured in Kling is not the processor voltage, but is the voltage drop between the power supply and the processor. *Id*. For example, the Abstract quoted above explicitly identified the measured voltage being the "voltage between the power supply and

the portion of the computer system." Ex. 1010, Abstract; Ex. 2024, ¶69. Claim 23 of Kling says: "the parameter includes a voltage across a **resistor between the power supply and the portion of the computer system**." And claim 16 explains that the "portion of the computer system" is the component that consumes power. A POSITA would have understood that the voltage measured in Kling is the voltage drop between the power source and the load (*e.g.,* a processor). *Id*. Such voltage drop is not processor voltage because processor voltage is the voltage between the load (*e.g.,* a processor) and the ground. *Id*. Therefore, a POSITA would have understood that Kling fails to disclose a measurement of the "processor voltage" and Kling's throttling is not based on the "processor voltage." [*Id*.

Even assuming Kling's throttling is based on the "processor voltage," a POSITA would not have a motivation to combine Kling with Nicol. Id. at 70. Nicol already minimized the power consumption based on processing load and required completion time. Ex. 1009, Abstract ("by dynamically controlling processing load of chips and controlling . . . the operating voltages of those chips, [Nicol] minimize[s] overall power consumption."); 3:66-67 ("the operating system of PE 100 needs to ascertain the required completion time"). A POSITA would have understood that a further reduction of clock frequency based on supply voltage would cause the tasks to not finish on time, impacting performance, and

would not have a reasonable expectation of success in combining Kling with Nicol. Ex. 2024, ¶70.

Thus, Petitioner fails to establish by the preponderance of the evidence that Nicol in view of Kling renders this claim obvious. Ex. 2024, ¶71.

C. Petitioner has not Carried its Burden to Show That Nicol in view of Kling Renders Obvious Dependent Claim 3

Petitioner has not shown that Nicol in view of Kling discloses "said clock frequency is determined in part by available power." Petitioner relies on Kling for this element. *Id*. at ¶72. Petitioner quotes Kling as disclosing "the upper limit is a constant value … associated with an approximately maximum power that can be reliably consumed by the computer system." Pet., 48. Petitioner argues that "[a] POSITA would have understood that this functionality can be readily implemented in Nicol's system with reasonable expectation of success" because "[t]he functionality involves relatively simple add-on software to Nicol's more complex task scheduler software residing in the controller, and relies on well-known measurement techniques, such as measuring a voltage across an appropriately placed resistor, and would have yielded predictable results." Petitioner's argument fails for three reasons: (1) Petitioner misrepresents what is disclosed by omitting not just the context of this quote, but the remaining portion of the sentence, which undercuts Petitioner's claims; (2) Petitioner has not shown that Kling's frequency

is dependent on an available power within the context of a changing clock frequency in claim 1, from which claim 3 is dependent; (3) Petitioner's claim that Kling's maximum power limitation is "simple add-on software" that could have been readily implemented with "an appropriately placed resistor" is false. Ex. 2024, ¶72.

(a) **Petitioner Misrepresents Kling**

The sentence from Kling, on which Petitioner relies, recites "the upper limit is a constant value … associated with an approximately maximum power that can be reliably consumed by the computer system ***from a power outlet into which the system is plugged before the outlet's fuse or circuit breaker trips***." Ex. 1010, 5:22-25 (emphasis added). With this full context, Kling is properly understood to describe a system that sets its own voltage limit that is reliably below a maximum voltage that can be supplied before an outlet fuse is tripped. Ex. 2024, ¶73. Kling is not limited by available power; it is limited by a self-imposed safety measure. *Id*.

(b) **Petitioner has Not Shown that the Clock Frequency is Determined in Part on Available Power**

Independent claim 1, from which claim 3 depends, describes a dynamically changing clock frequency that requires an initial setting of a clock frequency, subsequently increasing the clock frequency to a maximum frequency in accordance with a number of pending operations of a second processor, and reducing the clock frequency in accordance with an operating temperature

threshold and hysteresis characteristic. Claim 3 specifies that this frequency must be determined, in part, by the available power. Petitioner points to a static upper voltage limit as the available power upon which the clock frequency depends, but if the amount of available power is static and doesn't change, it cannot determine all of these frequencies, which can vary during operation. Pet., 47; Ex. 2024, ¶74.

(c) Incorporating Kling's upper power limit would not be a simple matter as Petitioner asserts

The idea that a POSITA would easily incorporate the invention of Kling into Nicol via simple add-on software is untrue. Ex. 2024, ¶75. Balancing upper limits with Nicol's power management system would have been a complex task in which a POSITA would have to balance the power needs of individual processors to accomplish tasks within a designated time along with temperature considerations which is also an element of the claim. *Id*. A POSITA may spend their entire career developing such a system that responds appropriately and efficiently balance these considerations. *Id*.

D. Petitioner has not Carried its Burden to Show That Nicol in view of Kling Renders Obvious Dependent Claim 4

Dependent claim 4 recites "said clock frequency is determined in part by a user setting." For a user setting, Petitioner refers to Kling lower threshold which Kling describes as being modifiable by a user. Pet., 49. However, the frequency does not depend on a lower threshold. Ex. 2024, ¶76. The frequency depends on

either the upper threshold, which causes throttling, or normal operating conditions which sets a high core frequency. *Id*.; Ex. 1010, 10:10-13 ("If the processor does not receive the throttle signal (or receives a de asserted throttle signal), normal operation of the processor at the high core frequency continues"). The lower threshold determines only whether the frequency ceases to depend on the upper threshold. Ex. 1010, 8:43-45 ("The pipeline continues to be stalled at step 610 until the power has reached a lower threshold . . . ."); Ex. 2024, ¶76. Accordingly, assuming for argument's sake that the lower threshold can fairly be characterized as a user setting, Petitioner has failed to show that the frequency is dependent upon it. Ex. 2024, ¶76.

E. Petitioner has not Carried its Burden to Show That Nicol in view of Kling Renders Obvious Dependent Claim 5

Petitioner has failed to show that Nicol and Kling disclose the elements of claim 5 for at least the reasons discuss in Sections VIII.C. and VIII.D. Ex. 2024, ¶77. In addition, Claim 5 requires that a clock frequency depend on both available power and a user setting. *Id*. Petitioner's arguments with respect to each of these elements fails to detail a situation in which a clock frequency is dependent on both these elements – according to Petitioner's analysis, the clock frequency depends on available power OR a user setting. *Id*.

Petitioner argues, with reference to annotated Figure 2A (reproduced below), that the upper limit is available power, Pet., 47-48, and the lower limit is a user setting, *id*. at 49-50. Petitioner's expert explains that "if the measured power reaches the upper limit, the controller sends a 'throttle signal' to the processor to instruct it to reduce its clock frequency to reduce power consumption." Ex. 1001, ¶211. Petitioner's expert further quotes Kling as reciting ""[o]nce [the] lower threshold is reached, the throttle signal may be deasserted, and, in response, the IC resumes normal operation." *Id*. at 212; Ex. 1010, 5:48-50. Under Petitioner's expert's analysis of Kling, the clock frequency is either (1) throttled according to the upper limit or (2) not throttled and determined according to normal operational techniques if the upper limit has not been reached, or if the lower limit has been reached. Ex. 2024, ¶78. At no point does the clock frequency depend on both the upper and lower limits. *Id*. Accordingly, at no point does Kling's clock frequency depend on both an available power and a user input under Petitioner's own analysis. *Id*.

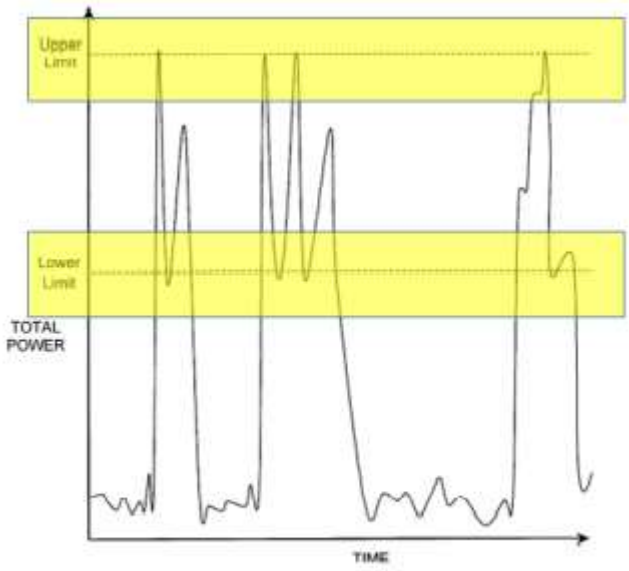


Figure 2A

F. Petitioner has not Carried its Burden to Show That Nicol in view of Kling Renders Obvious Dependent Claim 6 ([SL])

Petitioner relies on Nicol alone for this element. It points to Nicol's disclosure of "the number of instructions" and the existence of an "instruction queue." Pet. at 51. However, a POSITA would not have concluded that this disclosure means the number of instructions or pending operations is "determined by" the fill level. Ex. 2024, ¶79. As admitted by Petitioner, there are many ways to determine the number of pending operations, such as "by taking an average of recent workload and assuming the average represents the near-term workload." Pet. at 51-52; *see also* Ex. 2024, ¶79. Nicol simply does not disclose any particular way to determine the number of instructions. Ex. 2024, ¶79.

Petitioner points to the file history of the '605 patent, alleging that Patent Owner admitted that "the fill level of a data buffer [is] representative of the

number of waiting operations or processor load." Pet. at 51. However, this statement does not render the claim obvious. Ex. 2024, ¶80. It was made in a context of written support rejection. *Id*. Specifically, Patent Owner explained to the Examiner that the patent specification discloses "a clock frequency set in accordance with a processor load" because it discloses "the clock frequency may . . be determined from the filling level of the particular data buffers" and a POSITA would have known that the filling level of the data buffers indicates the processor load. Ex. 1004 at 377. However, this does not mean the reverse is true. Ex. 2024, ¶80. A POSITA would not have understood that processor loads or number of pending operations are necessarily determined through the buffer fill level. Ex. 2024, ¶80.

Petitioner also points to Cline and Hong to show that inspecting the fill level of buffers was well known. However, it provides no analysis as to a POSITA's motivation to apply such knowledge to Nicol and any expectation of success of such application. Ex. 2024, ¶81. Cline and Hong proves no more than inspecting the buffer fill level was independently known in the prior art. *Id*. However, an invention "composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art." *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). Rather, Petitioner must demonstrate "both 'that a skilled artisan would have been motivated to

combine the teachings of the prior art references to achieve the claimed invention, and that the skilled artisan would have had a reasonable expectation of success in doing so.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–68 (Fed. Cir. 2016) (citation omitted). Petitioner fails to do so, and thus, fails to establish by a preponderance of evidence that claim 6 is obvious in view of Nicol. Ex. 2024, ¶81.

G. Petitioner has not Carried its Burden to Show That POSITA Would Combine Nicol and Kling

Petitioner proposes three potential motivations to combine Nicol and Kling: (1) Nicol and Kling are directed to thermal and power management aspects that are allegedly critical and ubiquitous in processor-based systems, Pet., 23; (2) Nicol and Kling involve multiprocessor systems, software-managed power supplies for each processor, and immaterial differences between software such that a POSITA would find it obvious to introduce Kling's functionality into Nicol's controller OS, *id*. at 23-24; and (3) Nicol is concerned with power consumption, and over-temperature protection is allegedly critical for a multiprocessor system, and a POSITA seeking to improve Nicol allegedly would have incorporated the benefits of Kling to help with over-temperature protection, *id.* at 24-25. Together, these alleged motivations to combine amount to a suggestion that Nicol and Kling manage aspects of a computer system and it would be beneficial to combine the aspects that they

manage. Ex. 2024, ¶82. Mere benefit without any showing of actual motivation is plainly insufficient to suggest a POSITA would combine these reference. *Id*. Indeed, the reliance on benefit evidences application of impermissible hindsight bias. *Polaris Industries, Inc. v. Arctic Cat, Inc*, 882 F3d 1056, 1068 (Fed. Cir 2018) ("[S]ubjective preferences . . . invite[] the distortion caused by hindsight bias into the fold. . . . We have observed that the prejudice of hindsight bias often overlooks that the genius of invention is often a combination of known elements which in hindsight seems preordained." (internal citations omitted)).

In an attempt to legitimize its reliance only on the benefit of combinations, Petitioner alleges, supported only by parroting language of its expert, that a "POSITA would have found it obvious to program Nicol's controller to handle the additional software functionalities discussed in Kling," and "[i]mplementing this added functionality would not require undue experimentation, has a reasonable expectation of success, and would yield predictable results because the added functionality is primarily add-on software." Pet., 24-25. This claim is untrue. Ex. 2024, ¶83. Petitioner makes no attempt to explain how a system combining Nicol and Kling would function, likely due to the fact that managing a plurality of metrics to create an efficient processing system is extremely difficult. *Id*. A POSITA might spend their entire career developing intricate systems for managing processor temperature and clock frequency among a plurality of processors, and

Petitioner dismisses it as a mere triviality. *Id*. Besides, if the Board were to accept Petitioner's argument that a POSITA could easily and predictably combine the power management systems of Nicol and Kling's software, requiring a motivation to combine loses all meaning – if these two systems could be combined as a mere triviality, then any software could similarly be combined.

In addition, in addition to Petitioner's failure to address how a combination of Nicol and Kling would actually function, Petitioner ignores any issues that would arise. *Id*. at 84. For example, Nicol and Kling change frequencies for substantially different reasons. Petitioner's expert recognizes that "Kling teaches a controller … to adjust clock frequency of the processors . . . based on sensor measurements," Ex. 1001, ¶123, whereas "Nicol teaches that the controller allocates tasks to the individual processors . . . so that it can equalize the processing load among the PEs, . . . and then the controller lowers the clock frequency on the chip to as low a level as possible" *id*. at ¶164. Petitioner ignores any prioritization issues that would arise from these two different methods for changing frequency. Ex. 2024, ¶84. It is difficult to implement them both simultaneously, and there is no discussion in Nicol or Kling to suggest that they could be implemented as seamlessly and simply as Petitioner argues. *Id*.

In fact, the disclosure of Kling would dissuade a POSITA from using a thermal sensor as proposed by Petitioner. Id. at ¶85. As analyzed above, Kling

abandoned the indirect way of measuring power consumption through a thermal sensor, so that "temperature measurement inaccuracies related to poor positioning of thermal sensors in proximity to the processor are avoided." Ex. 1010, 2:56-58. By not using a thermal sensor, "the response time between detecting a high power condition and reducing the power consumption of the computer system is greatly improved over the use of thermal sensors to detect the high power condition." *Id.*, 2:58-62. Nevertheless, Petitioner argues that "Kling discusses conventional techniques to address those issues. In particular, to address critical overtemperature, a thermal sensor is typically used to monitor the temperature of a processor." Pet. at 16. However, given Kling's disclosure, a POSITA would not have a motivation to combine the traditional thermal sensor with Nicol because of the stated inaccuracies and slow response time caused by the thermal sensor. Ex. 2024, ¶85.

IX. GROUND II: PETITIONER FAILS TO PROVE NICOL IN VIEW OF KLING AND DEHON RENDERS CLAIMS 1-6 OBVIOUS

Petitioner fails to show that Nicol in view of Kling and DeHon renders claims 1-6 obvious at least because Petitioner has not shown that a POSITA would be motivated to combine DeHon with Nicol. Id. at 86.

The DeHon processor includes two components, "fixed processor core cell 10" and "a configurable array 100 on the same silicon die or chip" as shown below:

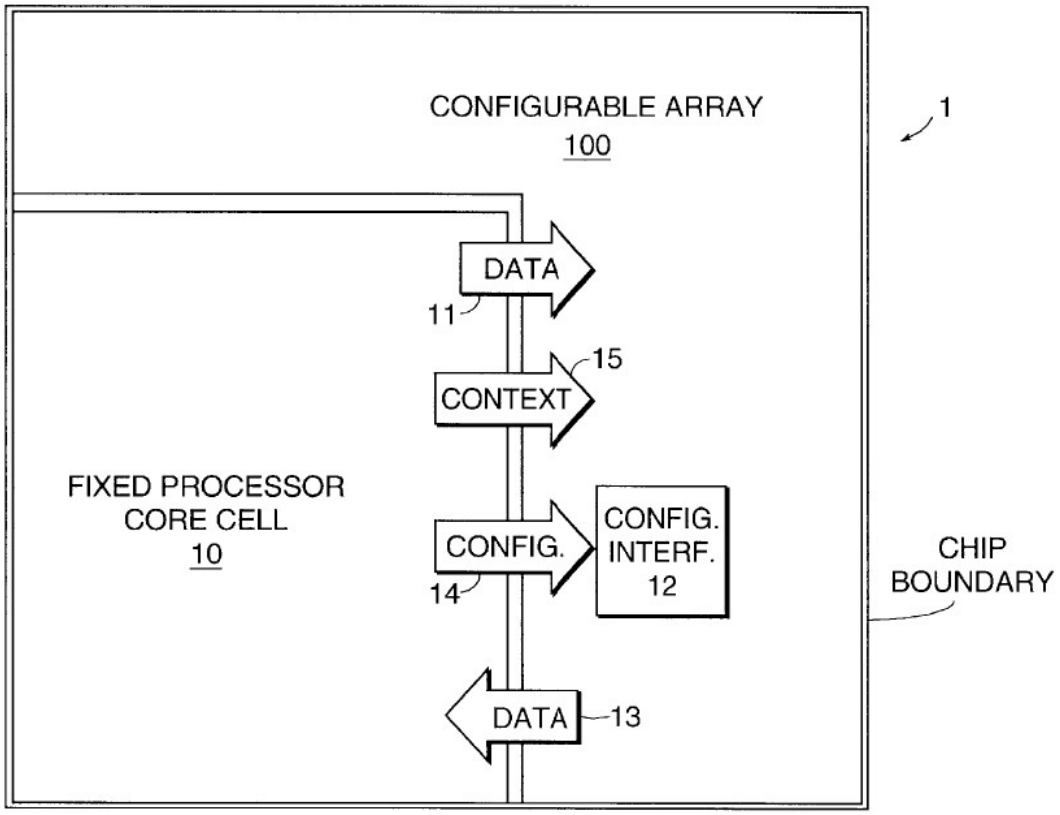


FIG. 1

Ex. 1010, Figure 1, 5:37-39. In order to configure the "configurable array 100," DeHon needs a compiler that "selects the hardware configurations and library routines that best accelerate each application." Ex. 1012, 6:47-65. Ex. 2024, ¶88. In the proposed combination, Petitioner replaces each PE in Nicol with the integrated chip in DeHon so that the combination becomes a multi-chip system.

See Petition at 55-56 ("The figure [] combines Figure 4 of Nicol with Figure 1 of DeHon to illustrate Nicol's multiprocessor system in which the PEs are DeHon's reconfigurable processor **chips**.") (emphasis added). Ex. 2027, 56:1-24. A POSITA would have understood that in this multi-chip system, the controller PE runs the operating system and thus includes the required compiler. Ex. 2024, ¶88. In other words, in the proposed combination, it is the controller PE that would configure the DeHon "configurable array 100" on separate chips. Ex. 2024, ¶88.

A POSITA would have understood that this proposed combination violates a key requirement of DeHon. *Id*. at ¶89. DeHon states that integrating all components on one die is a key feature:

> The combination of the processor cell 10 and the configurable array 100 on the same silicon die is **a key feature** of the invention enabling high bandwidth communications with a low latency interface. **When the configurable array is merely attached to a host processor as an external peripheral, the high overhead implicit in communication with the configurable engine located on a different chip limits the avenues for acceleration and prevents close cooperation**. The low bandwidth similarly makes communication expensive and limits the throughput achievable with the reconfigurable array.

Ex. 1012, 6:19-29. A POSITA would have understood that the combination proposed by Petition is equivalent to "the configurable array [being] merely attached to a host processor as an external peripheral," where the controller PE becomes the host processor that configures the configurable array on separate

chips. Ex. 2024, ¶89. This would substantially increase the overhead implicit in communication between the controller PE and the DeHon processors on different chips. *Id*.. In addition, DeHon states that "the integration of the processor core cell 10 and the reconfigurable array 100 also decreases reconfiguration overhead. As a mere peripheral, the reconfiguration time for the array must be amortized over a large amount of processing to justify the array's reconfiguration." Ex. 1012, 6:31-35. A POSITA would have understood that using the controller PE to configure the array on different chips as proposed by Petitioner would significantly increase reconfiguration overhead, and Nicol does not disclose the amount of processing that could justify the array's configuration time. Ex. 2024, ¶89. Thus, a POSITA would not have a motivation to use separate DeHon chips in the Nicol system. *Id*. Given the extra overhead introduced in the proposed combination, a POSITA would not have a reasonable expectation of success. *Id*. For example, the reconfiguration overhead and latency created in the proposed combination would substantially increase the complexity for the "Asynchronous Communication Network 160" and would no longer meet the requirement that the "real-time operating system resides in PE 100." *Id*.

Petitioner does not explain why a POSITA would ignore the "**key feature**" of DeHon and apply the DeHon invention in a multi-chip environment. *Id*. at 90. Instead, Petitioner only touches on the motivation to combine at a very high level.

Petitioner's motivation to combine analysis in the present case is almost a verbatim copy of its motivation to combine Nicol and DeHon in its petition in IPR2020-00539. *See* IPR2020-00539, Paper 2 at 73-78. There, the Board summarized the motivation to combine arguments in the Institution Decision. *See* IPR2020-00539, Paper 11 at 34-36. First, Petitioner argues that "Nicol explains that its multiprocessor system is intended for use in a variety of digital signal processing applications," and DeHon teaches that its multiprocessor "can serve as the principle building block for a wide range of applications," so a person of ordinary skill in the art would have chosen DeHon's processor as each of the PEs in Nicol's system. IPR2020-00539, Paper 11 at 34. However, this shows no more than Nicol could potentially be combined with DeHon, which is insufficient. *See Belden Inc. v. Berk-Tek LLC*, 805 F.3d 1064, 1073 (Fed. Cir. 2015) ("[O]bviousness concerns whether a skilled artisan not only **could have made but would have been motivated to make** the combinations or modifications of prior art to arrive at the claimed invention.") (emphasis original).

Second, Petitioner argues that "a person of ordinary skill in the art would have been motivated to use a reconfigurable processor, such as DeHon's, to meet the needs of specific applications." IPR2020-00539, Paper 11 at 34. Specifically, Petitioner also points to some advantages in DeHon, such as "handl[ing] a variety of compute-intensive functions 'such as compression, encryption, signal

processing, or protocol processing'" and "replac[ing] or be[ing] deployed alongside traditional fixed processors." Pet. at 57. However, Petitioner does not provide any specific applications in Nicol that would benefit from DeHon's reconfigurable processor or any needs that Nicol alone cannot meet. Given Nicol is a self-contained complete system, it does not have any need to be modified. Ex. 2024, ¶91. Petitioner's motivation is based on hindsight.

Third, Petitioner argues that "both references 'relate to the same field of invention, optimizing processor systems by dynamically controlling processors.'" Id. However, a POSITA would have understood that the field of processors is very broad. *Id*. at ¶92. This characterization covers very small slow processors such as those used in pagers and extremely high-performance supercomputers. *Id*. The characterization covers the controller for the display in a microwave oven as well as the controller for a reactor core on a nuclear submarine. *Id.* All of these areas attempt to optimize processors systems by dynamically controlling processors. *Id.* They have little if anything in common beyond that shockingly broad characterization. *Id.* A POSITA would be hard-pressed to think of a computer system or computer related patent where that characterization would not apply. This is different from *In re Dance*, where "the references are in the same **narrow** field." 160 F.3d 1339, 1343 (Fed. Cir. 1998).

As noted by the Board, "[Petitioner] did not devote much discussion in its Petition specifically relating to an expectation of success in combining DeHon with Nicol (as modified by Bhatia with respect to Ground 4)." IPR2020-00539, Paper 11 at 35. Given that integrating on one chip is a "key feature of the [DeHon] invention," Petitioner's failure of explanation of a reasonable expectation of success is fatal. Ex. 2024, ¶93.

Thus, Petitioner fails to establish the motivation to combine Nicol and DeHon and a reasonable expectation of success of such combination by the preponderance of the evidence. Ex. 2024, ¶94.

X. GROUND III: PETITIONER FAILS TO PROVE NICOL IN VIEW OF KLING, DEHON, AND BHATIA RENDERS CLAIMS 1-6 OBVIOUS

Petitioner fails to show that claims 1-6 are obvious over Nicol in view of Kilng, DeHon, and Bhatia at least because Petitioner fails to show that POSITA would be motivated to combine Bhatia with Nicol, Kling, and DeHon. Ex. 2024, ¶95.

As discussed above, a POSITA would not be motivated to combine Nicol with Kling or DeHon. A POSITA would also not be inclined to combine Nicol with Bhatia, much less to combine all four reference together. Ex. 2024, ¶96.

Petitioner proposes three potential motivations to combine Bhatia with Nicol, and Kling: (1) Nicol, Kling, and Bhatia are directed to thermal and power

management aspects that are allegedly critical and ubiquitous in processor-based systems, Pet., 65; (2) a POSITA would allegedly be motivated by Bhatia's description of a low activity state to incorporate them into Nicol to achieve further minimization of power consumption, *id.* at 65-66; and (3) A POSITA would have had a reasonable expectation of success in doing so because Bhatia explains that those low activity states were commonly used in the industry, *id*. at 66. Together, these alleged motivations to combine amount to a suggestion that Nicol, Kling, and Bhatia manage aspects of a computer system and it would be beneficial to combine the aspects that they manage. Ex. 2024, ¶97. Petitioner's argument that the activity states were commonly used, and a POSITA would have had a reasonable expectation of success in implementing them, is supported by nothing more than Petitioner's expert's empty conjecture, and also is irrelevant because Petitioner proposes that the combination would result in a benefit but has not pointed to any motivation to combined the references. *Id*. Mere benefit without any showing of actual motivation is plainly insufficient to suggest a POSITA would combine these reference. Indeed, the reliance on benefit evidences application of impermissible hindsight bias. *Polaris Industries, Inc. v. Arctic Cat, Inc*, 882 F3d 1056, 1068 (Fed. Cir 2018) ("[S]ubjective preferences . . . invite[] the distortion caused by hindsight bias into the fold. . . . We have observed that the prejudice of hindsight bias often overlooks that the genius of invention is often a combination of known elements

which in hindsight seems preordained." (internal citations omitted)); Ex. 2024, ¶97.

Furthermore, Petitioner makes no attempt to explain how a system combining Nicol and Bhatia would actually function, likely due to the fact that managing a plurality of metrics to create an efficient processing system is extremely difficult. *Id*. at ¶98 A POSITA might spend their entire career developing intricate systems for managing processor temperature and clock frequency among a plurality of processors, and Petitioner dismisses it as a mere triviality. *Id*.

Lastly, in addition to Petitioner's failure to address how a combination of Nicol and Bhatia would actually function, Petitioner ignores any issues that would arise. Ex. 2024, ¶99. Combining Nicol and Bhatia would frustrate the purpose of each. Nicol is designed to minimize power consumption by **lowering the clock frequency** and therefore the voltage demanded by the processors. *See* Ex. 1009, Abstract; 2:22-27; Ex. 2024, ¶99. Conversely, Bhatia is designed to **maintain** a system operating at a high performance, characterized by **a high frequency** which requires a high voltage, without exceeding over-temperature thresholds. Ex. 1011, 1:47-49; 3:14-23; 6:41-51; Ex. 2022, ¶99.

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CERTIFICATE OF COMPLIANCE

I hereby certify that this paper complies with the type-volume limitation of 37 C.F.R. § 42.24 because it contains 13,496 words, excluding the parts of the paper exempted by 37 C.F.R. § 42.24(b).

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CERTIFICATE OF SERVICE

The undersigned hereby certify that Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, along with all the exhibits were served on December 5, 2020 by filing these documents through the Patent Review Processing System, as well as by e-mailing copies to:

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