

UNITED STATES PATENT AND TRADEMARK OFFICE

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BEFORE THE PATENT TRIAL AND APPEAL BOARD

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INTEL CORPORATION,  
Petitioner,

v.

PACT XPP SCHWEIZ AG,  
Patent Owner.

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IPR2020-00541  
Patent 9,075,605 B2

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Before SALLY C. MEDLEY, SCOTT C. MOORE, and  
CHRISTOPHER L. OGDEN, *Administrative Patent Judges*.

MEDLEY, *Administrative Patent Judge*.

JUDGMENT  
Final Written Decision  
Determining All Challenged Claims Unpatentable  
*35 U.S.C. § 318(a)*

## I. INTRODUCTION

Intel Corporation (“Petitioner”) filed a Petition for *inter partes* review of claims 1–6 of U.S. Patent No. 9,075,605 B2 (Ex. 1003, “the ’605 patent”). Paper 2 (“Pet.”). PACT XPP SCHWEIZ AG (“Patent Owner”) filed a Preliminary Response. Paper 6 (“Prelim. Resp.”). In accordance with Board authorization, Petitioner filed a Reply to the Preliminary Response (Paper 7) and Patent Owner filed a Sur-reply (Paper 9). Upon review of these papers, we instituted *inter partes* review, pursuant to 35 U.S.C. § 314, as to claims 1–6 based on the challenges set forth in the Petition. Paper 11 (“Decision to Institute” or “Dec.”).

Subsequent to institution, Patent Owner filed a Patent Owner Response (Paper 20, “PO Resp.”), Petitioner filed a Reply to Patent Owner’s Response (Paper 27, “Pet. Reply”), and Patent Owner filed a Sur-reply (Paper 31, “Sur-reply”). On June 15, 2021, we held an oral hearing. A transcript of the hearing is of record. Paper 35 (“Tr.”).

For the reasons that follow, we conclude that Petitioner has proven by a preponderance of the evidence that claims 1–6 of the ’605 patent are unpatentable.

### *A. Related Matters*

The parties identify several district court proceedings involving, or relating to, the ’605 patent, including PACT XPP Schweix AG v. Intel Corp., No. 1:19-cv-1006-JDW (D. Del) (“District Court Action”). Pet. 2 (Mandatory Notices); Paper 3, 1–2, Papers 22, 23, 29.

### *B. The ’605 Patent*

The ’605 patent describes “optimization of hardware used in data processing,” and more particularly, optimization of power consumption and

data processing time in VPU technology (e.g., reconfigurable data processing units, and modules with reconfigurable architecture). Ex. 1003, 1:22–24, 1:32, 2:40–45, 2:56–60. The '605 patent explains that “[t]o determine the clock frequency for a microprocessor based on the state is known,” but “proble[m]s arise in the overall speed with which certain applications are carried out.” *Id.* at 2:30–35. The '605 patent aims to optimize power consumption and data processing time in a VPU (data processing unit) by assigning an appropriate clock to logic cells in a plurality of clocked logic cells (Processing Array Elements (PAEs)), based on configuration states of the logic cells. *Id.* at code (57), 2:45–60. For example, a clock preselecting unit in a VPU preselects logic cell clocking such that, “depending on the state, a first clock is preselected at least at a first cell (PAE) and an additional clock is preselected at least at an additional cell.” *Id.* at code (57). The '605 patent's VPU may include PAEs clockable at different rates in a reconfigurable module, and may also include

multiple buses in parallel whose speed is clocked differently, i.e., a bus which is clocked particularly high for providing a high-performance connection, parallel to a bus which is clocked lower for providing a power-saving connection. The connection c[l]ocked high may be used when longer signal paths have to be compensated, or when PAEs, positioned close together, operate at a high frequency and therefore also have to exchange data at a high frequency in order to provide a good transmission here over short distances in which the latency plays a minor role at best. . . . [A] number of PAEs, positioned together locally and combined in a group, operate at a high frequency and possibly also sequentially and . . . local and correspondingly short bus systems are clocked high corresponding to the data processing rate of the group, while the bus systems, inputting the operands and outputting the results, have slower clock and data transmission rates. For the purpose of optimizing the power consumption, it would be alternatively possible to implement

slow clocking and to supply data at a high speed, e.g., when a large quantity of inflowing data may be processed with only a minor operational effort, thus at low clock rates.

*Id.* at 8:34–59. Clock frequencies in a VPU may be set in various ways: (i) based on a logic field sleeping mode in which “only one or a plurality of cells are activated, if necessary, on a very low level, i.e., very slow clocking”; (ii) based on “a hysteresis characteristic . . . [for] determining the clock rates, when a temperature-sensitive change of the clock frequencies is to be performed”; and (iii) based on “one or a series of a plurality of different arithmetic and/or logical operations . . . which, at least in part, require a different number of clock cycles.” *Id.* at 3:30–42, 4:55–60, 6:40–55, 13:50–53.

In one example, illustrated in Figures 3a and 3b reproduced below, a field of reconfigurable logic units 0102 (PAEs) are operated at frequencies dependent on the number of operations required for processing a data packet. *Id.* at 6:40–55, 12:31–13:7. Customized clocking of the logic units optimizes a power consumption ratio and the power usage at a constant data throughput through the cells. *Id.* at 6:48–51, 12:55–57.

0301

0102a I/O	0102d +	0102g loop+
0102b n.c.	0102e -	0102h /
0102c n.c.	0102f *	0102i +

**Fig. 3a**

+	-	*	loop 16	/	+	
clk	clk	2 clk	16 clk	32 clk	clk	I/O
32	32	16	2	1	32	
8 Mhz	8 Mhz	16 Mhz	128 Mhz	256 Mhz	8 Mhz	8 Mhz
4	4	8	64	128	4	2
1	1	32	16	32	1	1

**Fig. 3b**

Figure 3a shows a 3×3 field of cells/logic units 0102 that are configurable and reconfigurable independently from one another in a VPU, and Figure 3b illustrates a table indicating numbers of clock cycles (row 2) and clock rates (row 4) for the cells of Figure 3a. *Id.* at 11:6–8, 12:31–35.

In Figure 3a, the depicted field of reconfigurable logic units/cells 0102 is configured such that (i) a first cell 0102a is used for analyzing an input/output signal, (ii) cells 0102b, 0102c are presently not needed (denoted as not configured, n.c.), and (iii) cells 0102d through 0102i together form a group which executes a complex arithmetic operation including an addition (in cell 0102d), a subtraction (in cell 0102e), a multiplication (in cell 0102f), a loop executing a multiple addition (in cell 0102g), a division (in cell 0102h), and an addition (in cell 0102i). *Id.* at 12:35–45. Cells 0102d through 0102i are grouped in a group 0301 such that data is sequentially and pipeline-like processed by the cells. *Id.* at 12:45–48.

As indicated in the second table row in Figure 3b, the operations in cells 0102d–0102e are executed in different numbers of clock cycles. *Id.* at 12:49–51. For example, an addition or subtraction may be executed in one clock cycle (clk), a multiplication in two clock cycles (2 clk), a division (in cell 0102h) requires 32 clock cycles (32 clk), and a loop (in cell 0102g) requires 16 clock cycles (16 clk). *Id.* at 12:50–60. Thus, the cell in which the division takes place is operated at the highest clock. *Id.* at 12:57–60. The fourth table row in Figure 3b indicates the cells' clock rates resulting from a central clock of 256 MHz. *Id.* at 13:5–7. Further, if the VPU is operated in an application where the voltage may drop, the entire frequency may be reduced such that all cells are subsequently clocked slower by one half, so that division cell 0102h runs at only 128 MHz, while cell 0102d is clocked at 4 MHz. *Id.* at 13:8–20. If the processor's temperature rises

significantly, heat generation in the logic cells may be reduced by an additional clock rate reduction, as indicated in the last table row in Figure 3b. *Id.* at 13:20–28.

*C. Illustrative Claim*

Petitioner challenges claims 1–6 of the '605 patent. Claim 1 is an independent claim, and claims 2–6 depend therefrom. Claim 1 is reproduced below, which includes changes made per a Certificate of Correction.

1. A method for operating a multiprocessor system comprising a plurality of data processing units, each of the plurality of data processing units (a) including at least one Arithmetic Logic Unit (ALU) and a register unit and (b) being adapted for sequentially processing data, the method comprising:
  - the multiprocessor system setting a clock frequency, of at least a part of the multiprocessor system to a minimum in accordance with a number of pending operations of a first processor;
  - the multiprocessor system subsequently increasing the clock frequency of the at least the part of the multiprocessor system to a maximum in accordance with a number of pending operations of a second processor; and
  - the multiprocessor system subsequently reducing the clock frequency of the at least the part of the multiprocessor system in accordance with (a) an operating temperature threshold preventing over-temperature and (b) a hysteresis characteristic.

Ex. 1003, 15:6–16:5, Certificate of Correction.

*D. Instituted Grounds of Unpatentability*

We instituted *inter partes* review based on the following grounds of unpatentability under 35 U.S.C. § 103(a)<sup>1</sup> as follows (Dec. 7, 39):<sup>2</sup>

Claims Challenged	35 U.S.C §	Reference(s)/Basis
1–6	103(a)	Nicol, <sup>3</sup> Kling <sup>4</sup>
1–6	103(a)	Nicol, Kling, DeHon <sup>5</sup>
1–6	103(a)	Nicol, Kling, DeHon, Bhatia <sup>6</sup>

II. DISCUSSION

*A. Principles of Law*

To prevail in its challenges to Patent Owner’s claims, Petitioner must demonstrate by a preponderance of the evidence that the claims are unpatentable. 35 U.S.C. § 316(e); 37 C.F.R. § 42.1(d) (2019). A patent claim is unpatentable under 35 U.S.C. § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains.

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<sup>1</sup> The Leahy-Smith America Invents Act, Pub. L. No. 112-29, 125 Stat. 284 (2011) (“AIA”), amended several provisions of 35 U.S.C., including § 103. Because the ’605 patent has an effective filing date before the effective date of the applicable AIA amendments, we refer to the pre-AIA version of 35 U.S.C. § 103. Petitioner asserts, and Patent Owner does not dispute, that each relied upon reference is prior art under the pre-AIA version. Pet. 4; *see generally* PO Resp.

<sup>2</sup> As explained below, “Petitioner hereby withdraws Grounds II and III.” Pet. Reply 27. As such, this Decision only addresses Ground I.

<sup>3</sup> U.S. Pat. No. 6,141,762, issued Oct. 31, 2000 (Ex. 1009, “Nicol”).

<sup>4</sup> U.S. Pat. No. 6,367,023 B2, issued Apr. 2, 2002 (Ex. 1010, “Kling”).

<sup>5</sup> U.S. Pat. No. 6,052,773, issued Apr. 18, 2000 (Ex. 1012, “DeHon”).

<sup>6</sup> U.S. Pat. No. 6,535,798 B1, issued Mar. 18, 2003 (Ex. 1011, “Bhatia”).

*KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of ordinary skill in the art; and (4) when in evidence, objective evidence of nonobviousness.<sup>7</sup> *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966).

*B. Level of Ordinary Skill*

In determining the level of ordinary skill in the art, various factors may be considered, including the “type of problems encountered in the art; prior art solutions to those problems; rapidity with which innovations are made; sophistication of the technology; and educational level of active workers in the field.” *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995) (citation omitted). Petitioner relies on the declaration testimony of Dr. Carl Sechen, who testifies that a person having ordinary skill in the art “would have been a person with at least a Master’s degree in Electrical or Computer Engineering (or equivalent), and three years of experience with processor design.” Pet. 10 (citing Ex. 1001 ¶¶ 83–85). Patent Owner adopts Petitioner’s definition of a person having ordinary skill in the art. PO Resp. 19.

We accept the assessment offered by Petitioner and adopted by Patent Owner as it is consistent with the ’605 patent and the asserted prior art. We further note that the prior art of record in the instant proceeding reflects the appropriate level of ordinary skill in the art. *Cf. Okajima v. Bourdeau*, 261 F.3d 1350, 1354–55 (Fed. Cir. 2001) (holding the Board may omit specific

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<sup>7</sup> Patent Owner does not present any objective evidence of nonobviousness as to the challenged claims.



findings as to the level of ordinary skill in the art “where the prior art itself reflects an appropriate level and a need for testimony is not shown”).

### *C. Claim Construction*

In an *inter partes* review for a petition filed on or after November 13, 2018, “[claims] of a patent . . . shall be construed using the same claim construction standard that would be used to construe the [claims] in a civil action under 35 U.S.C. § 282(b), including construing the [claims] in accordance with the ordinary and customary meaning of such claims as understood by one of ordinary skill in the art and the prosecution history pertaining to the patent.” *See* 37 C.F.R. § 42.100(b) (2019); *see also Phillips v. AWH Corp.*, 415 F.3d 1303, 1312–14 (Fed. Cir. 2005) (en banc).

As explained more fully below, we adopt the District Court’s claim construction for “each of the plurality of data processing units . . . adapted for sequentially processing data.” For purposes of this Decision, we otherwise need not expressly construe any claim terms. *See Vivid Techs., Inc. v. Am. Sci. & Eng’g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999) (holding that “only those terms need be construed that are in controversy, and only to the extent necessary to resolve the controversy”); *see also Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co. Matal*, 868 F.3d 1013, 1017 (Fed. Cir. 2017) (citing *Vivid Techs.* in the context of an *inter partes* review).

### *D. Asserted Obviousness of Claims 1–6 over Nicol and Kling*

#### *1. Nicol*

Nicol describes technology for power reduction in a multiprocessor digital signal processor based on processor load, by dynamically controlling the processing load of chips and controlling the operating voltages of those

chips so as to minimize overall power consumption. Ex. 1009, 2:18–31, code (54). Nicol discloses a controller in a multi-processor chip “allocat[ing] tasks to the individual processors to equalize processing load among the chips,” “lower[ing] the clock frequency on the chip to as low a level as possible while assuring proper operation,” and “reduc[ing] the supply voltage.” *Id.* at 2:22–31.

Nicol’s Figure 2, reproduced below, illustrates a multi-processor chip with supply voltage control. *Id.* at 2:37–40.

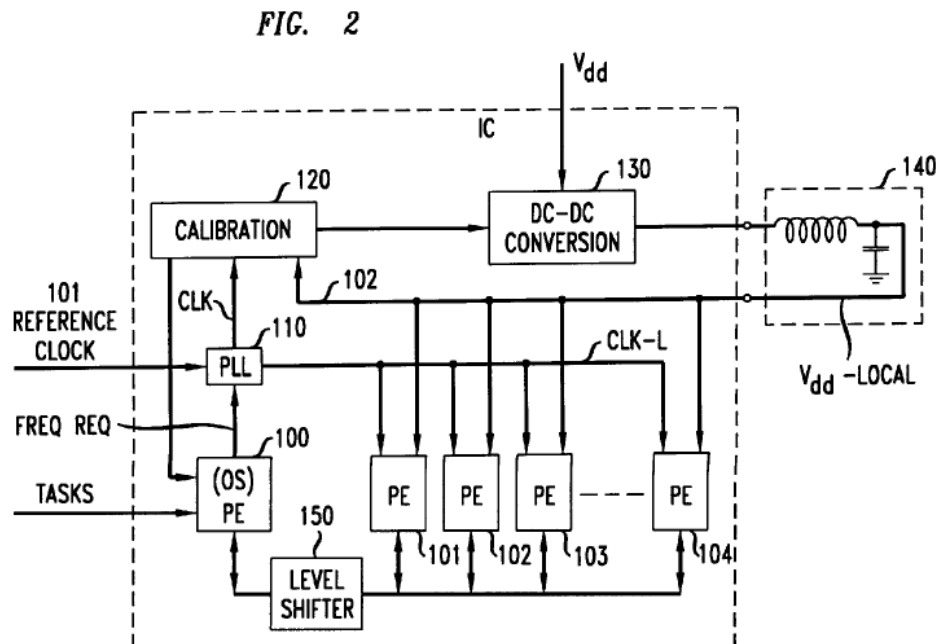


Figure 2 is a block diagram of a multi-processor chip with supply voltage control. *Id.* at 2:37–40.

The multi-processor chip in Figure 2 contains processing elements (PEs) 100, 101, 102, 103, . . . 104, each PE containing a central processing unit (CPU) and a local cache memory. *Id.* at 2:50–53. A real-time operating system resides in PE 100 and allocates tasks to the other PEs. *Id.* at 2:54–55. Applications that need to be processed are mapped to N PEs under control of a real time operating system (RTOS) executed on PE 100. *Id.* at

3:9–13. The processing load of the PEs is controlled to minimize overall power consumption as follows:

When an application that is running on the FIG. 2 system is subdivided into N concurrent task streams . . . each of the PEs become lightly loaded. This allows the clock frequency of the PEs to be reduced, and if the task division can be carried out perfectly, then the clock frequency of the FIG. 2 system can be reduced by a factor of N. Reducing the frequency, as indicated above, allows reducing the necessary supply voltage, and reducing the supply voltage reduces the system's power consumption (quadratically). To illustrate, if a given application that is executed on 1 PE requires operating the PE at 140 MHz, it is known from FIG. 1 that the PE can be operated at approximately a 2.7V supply. When the application is divided into two concurrent tasks and assigned to two PEs that are designed to operate at 140 MHz from a 2.7V supply, then the PEs can be operated at 70 MHz and at a supply voltage of 1.8V.

*Id.* at 3:22–42. In Figure 2, a programmable-frequency clock is generated using a multiplied input reference clock (line 101) via a phase lock loop frequency synthesizer circuit 110. *Id.* at 4:17–22. Two clocks are generated by PLL 110, a Clk clock, and a Clk-L that is 1 frequency step lower than Clk when Clk is being increased. *Id.* at 4:23–26. Clk-L is applied to the PEs, while Clk is applied to calibration circuit 120, which generates a supply voltage command applied to dc–dc converter 130 followed by L–C circuit 140, to cause the converter/L–C circuit combination to create a supply voltage  $V_{dd}$ -local that is applied to all PEs. *Id.* at 4:28–37. Figure 3, reproduced below, illustrates the relationship between voltage control clock Clk, the clock Clk-L applied to the PEs, and the  $V_{dd}$ -local supply voltage applied to the PEs.<sup>8</sup> *Id.* at 2:40–44.

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<sup>8</sup> Petitioner asserts, and Patent Owner does not dispute, that Nicol's Figure 3 includes labelling errors that Petitioner corrects. *See* Pet. 14–15.

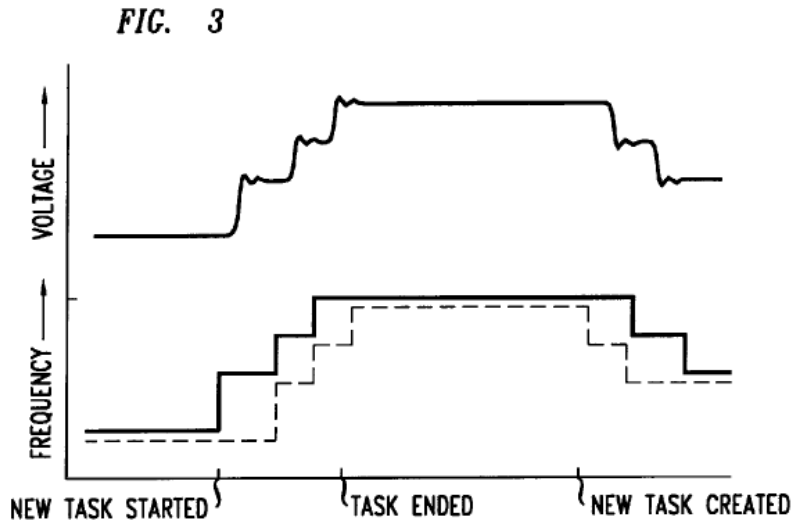


Figure 3 illustrates the relationship between voltage control clock Clk, the clock Clk-L applied to the PEs, and the  $V_{dd}$ -local supply voltage applied to the PEs. *Id.* at 2:40–44.

Nicol's Figure 3 illustrates timing associated with increasing Clk, Clk-L, and  $V_{dd}$ -local when a new task is created and the load on the multiprocessor is increased, and timing associated with decreasing Clk, Clk-L and  $V_{dd}$ -local when the load on the multiprocessor is decreased. *Id.* at 4:54–58. In particular, Figure 3 shows the system operating at 70 MHz from a 1.8V supply when the load is increased in three steps to 140 MHz. *Id.* at 4:58–60. When the 2.7V supply is stable, as shown by the supply voltage plot, the new task is enabled for execution. *Id.* at 4:60–62. Sometime thereafter, a task completes, which reduces the load on the multiprocessor and permits lowering the clock frequency to 100 MHz and lowering the supply voltage to 2.1V. *Id.* at 4:62–67.

Figure 4, reproduced below, illustrates a multi-processor chip with supply voltage control individual to each of the PEs. *Id.* at 2:44–47.

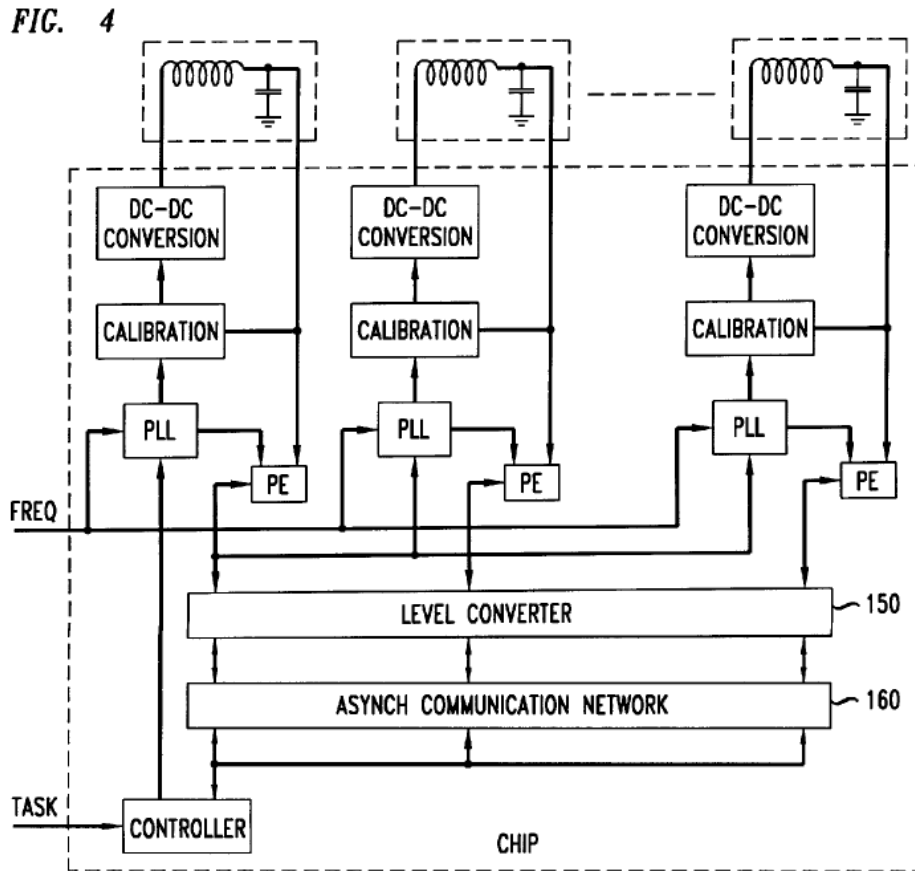
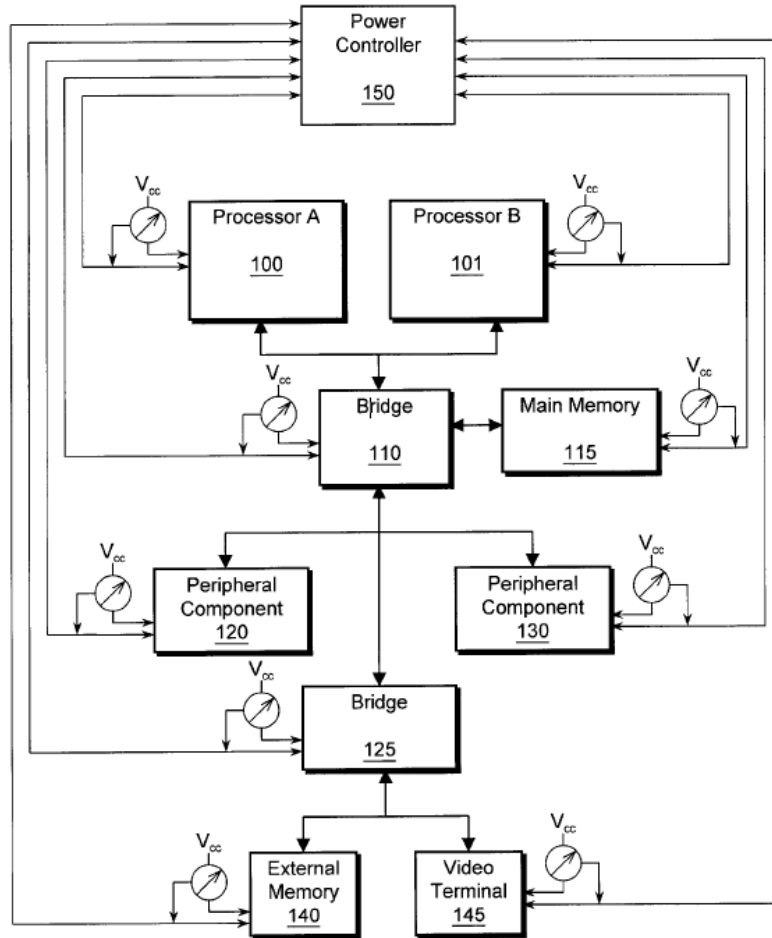


Figure 4 illustrates a multi-processor chip with supply voltage control individual to each of the PEs. *Id.* at 2:44–47.

A separate power supply provided for each PE in Figure 4 allows the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE. *Id.* at 5:55–6:2.

## 2. *Kling*

Kling describes a method and apparatus for measuring current, voltage, or duty cycle of a power supply to manage power consumption in a computer system. Ex. 1010, Title, Abstract. Figure 1 of Kling, reproduced below, illustrates a multiprocessor computer system with managed power consumption. *Id.* at 1:65–67, 2:65–67.

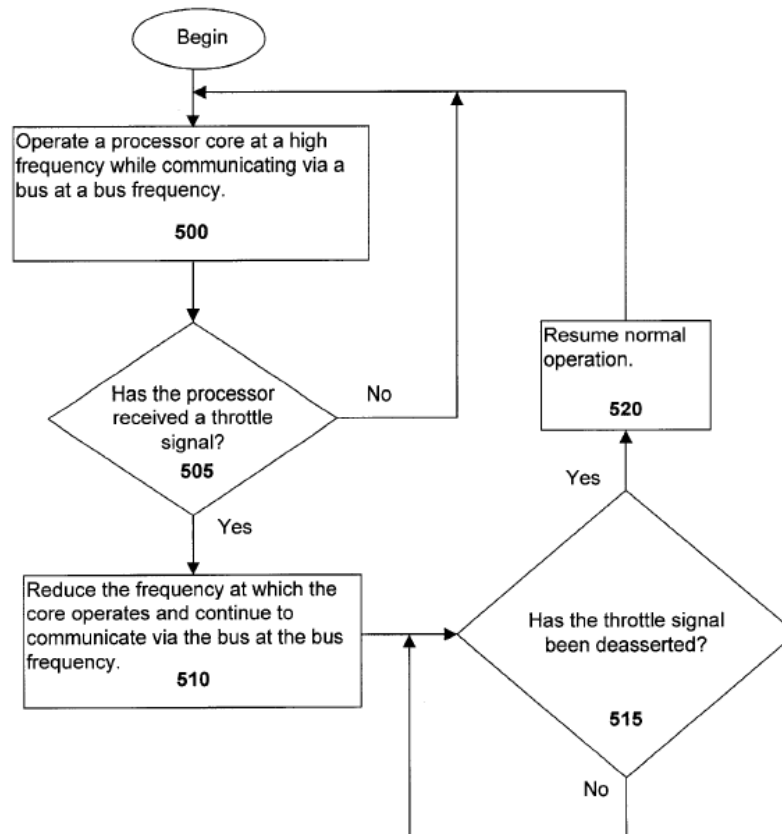


**Figure 1**

Figure 1 illustrates a multiprocessor computer system with managed power consumption. *Id.* at 1:65–67, 2:65–67.

In the multiprocessor computer system shown in Figure 1, a primary bridge 110 is coupled to processors 100 and 101 via a system bus. *Id.* at 2:65–3:5. Each device in the computer system in Figure 1 receives power from a power supply  $V_{cc}$ , the power being monitored by a meter. *Id.* at 3:20–23. A power controller 150, coupled to each device and to each meter, gathers measurements from devices in a portion of the computer system and calculates the total power consumed by that portion of the computer system. *Id.* at 3:22–39. If the total power consumed reaches a threshold, power

controller 150 sends a throttle signal to one or more ICs (integrated circuits) of the computer system, and, in response to receiving the throttle signal, the ICs reduce their power consumption. *Id.* at 4:42–67. Figure 5 of Kling, reproduced below, is a flow chart illustrating a method of reducing power consumption of a processor. *Id.* at 2:14–15.



**Figure 5**

Figure 5 is a flow chart illustrating a method of reducing power consumption of a processor. *Id.* at 2:14–15.

At step 500 in Figure 5, a processor core is operated at a high core frequency while the processor communicates with other ICs of the computer system via a bus operating at a bus frequency. *Id.* at 8:1–5. Next, at step

505, it is determined if the processor has received a throttle signal, and (i) if the processor has not received a throttle signal, normal operation of the processor at the high core frequency continues, but (ii) if the processor has received the throttle signal, then the core frequency of the processor is reduced (step 510). *Id.* at 8:5–15. Next, step 515 determines if the throttle signal to the processor has been deasserted. *Id.* at 8:18–19. The frequency is maintained at the reduced value until the throttle signal is deasserted. *Id.* at 8:20–22. Once the throttle signal is deasserted (step 515), the processor resumes normal operation at the high core frequency (step 520), and the method proceeds back to step 500. *Id.* at 8:22–24.

### 3. Discussion

Petitioner contends that claims 1–6 are unpatentable under 35 U.S.C. § 103(a) as obvious over Nicol and Kling. Pet. 5, 23–52. In support of its showing, Petitioner relies upon the declaration of Dr. Carl Sechen. *Id.* (citing Ex. 1001). Patent Owner relies upon the declaration of Dr. William Henry Mangione-Smith (Ex. 2024). Patent Owner argues that several limitations of the claims are not taught by the prior art and that it would not have been obvious to combine (1) the various embodiments of Nicol and (2) Nicol and Kling.

First, we focus on the terms of claim 1. Then, we evaluate Petitioner's reasons to combine Nicol and Kling, and Patent Owner's arguments to that end for claim 1. Next, we address the remaining claims 2–6 and the arguments presented for those claims. For the reasons that follow, we conclude that Petitioner has met its burden of proving by a preponderance of the evidence that each of the challenged claims would have been obvious in view of the asserted prior art.



*a. Claim 1: “a method for operating a multiprocessor system comprising . . . ” (preamble)<sup>9</sup>*

Claim 1 recites “[a] method for operating a multiprocessor system comprising a plurality of data processing units, each of the plurality of data processing units (a) including at least one Arithmetic Logic Unit (ALU) and a register unit and (b) being adapted for sequentially processing data.”

Petitioner contends, and we agree, that Nicol discloses a method of operating a single-chip multiprocessor system that includes a plurality of processing elements (PEs). Pet. 25–29 (citing Ex. 1009, 2:50–53, 3:10–20, 3:66–4:5, 5:66–6:13, 6:27–33, 6:67–7:3, Fig. 4; Ex. 1001 ¶¶ 130, 139, 141). We also agree with Petitioner’s contention that an ordinarily skilled artisan would have understood that each of Nicol’s PEs (data processing unit) would have included at least one ALU and a register unit. *Id.* at 29–30. In particular, Petitioner shows sufficiently that Nicol describes that each PE contains a central processing unit (CPU) and a local cache memory, and that a person having ordinary skill in the art would have understood that a PE having a CPU and cache would have included ALU(s) and registers. *Id.* (citing Ex. 1009, 2:50–53; Ex. 1001 ¶ 145; Ex. 1022, 33, Fig. 1.17). Patent Owner does not dispute Petitioner’s showing with respect to these elements of the preamble. *See generally* PO Resp.

The preamble further recites that “each of the plurality of data processing units . . . being adapted for sequentially processing data.” In the Petition, Petitioner contends that under Patent Owner’s proffered District Court Proceeding claim construction of the term “sequentially processing

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<sup>9</sup> The parties contend that the preamble is limiting. Pet. 25–35; PO Resp. 8–9, 20–28. For purposes of this Decision, we assume without deciding that the preamble is limiting.

data” to mean “passing results onto one or more other data processing units which are subsequently processing data,” Nicol renders obvious that each of the PEs are adapted for sequentially processing data. *Id.* at 30–35.

Subsequent to the Decision to Institute, the District Court determined that the phrase “each of the plurality of data processing units . . . adapted for sequentially processing data” means “[s]equential data processors that pass results to one or more additional data processing units to perform additional computations.” Ex. 2026, 17, 19. The parties appear to agree with that construction. PO Resp. 8–9; Pet. Reply 8, 27. Petitioner’s showing in the Petition is consistent with the District Court’s construction, because the construction is similar to Patent Owner’s proffered construction and neither party indicates that there is a substantive difference between Patent Owner’s proffered construction and the District Court’s construction for purposes of deciding the issues in this proceeding. Pet. 30–32; PO Resp. 8–9; Pet. Reply 8, 27. Accordingly, for purposes of this Decision, we adopt the District Court’s claim construction for “each of the plurality of data processing units . . . adapted for sequentially processing data.”

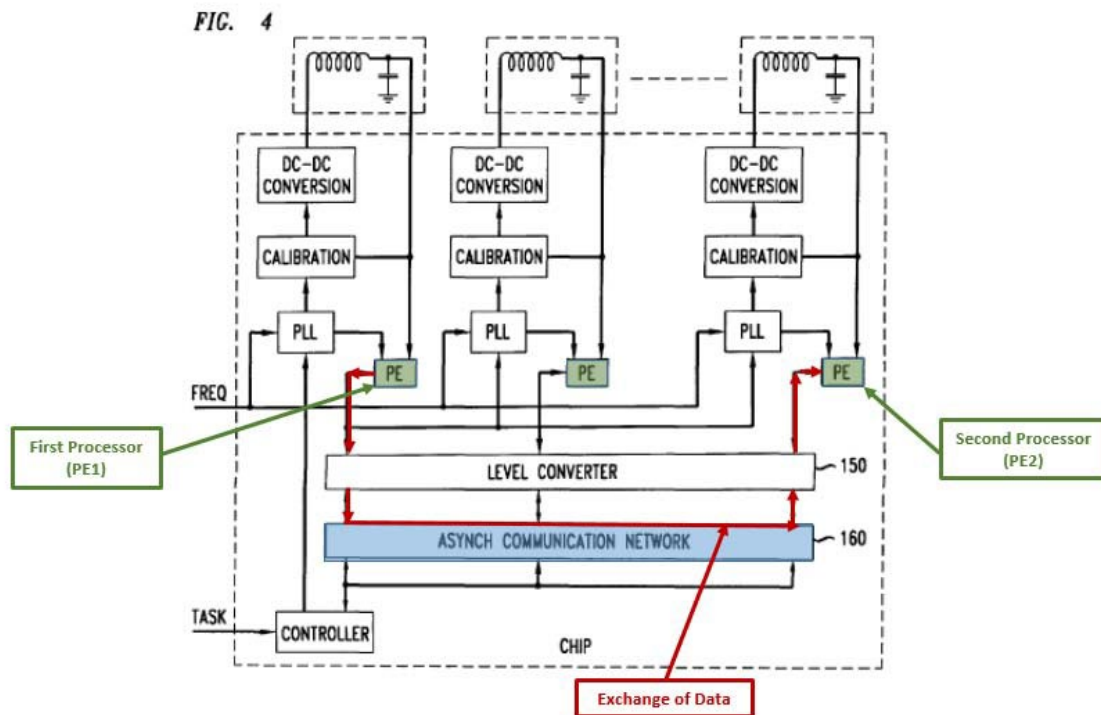
In the Petition, Petitioner “provides three independent reasons for why a POSITA<sup>10</sup> would understand Nicol to disclose, or at least render obvious, ‘being adapted for sequentially processing data.’” Pet. Reply 8 (citing Pet. 30–35). For purposes of this Decision, we focus our analysis on Petitioner’s first reason, as do the parties. Pet. 30–32; Pet. Reply 8–10 (discussing only the first reason discussed at pages 30 to 32 of the Petition); Sur-reply 15–16.

Petitioner argues, referencing Nicol annotated Figure 4, that “Nicol teaches the need for ‘*synchronizing the exchange of data*’ among the PEs

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<sup>10</sup> A person of ordinary skill in the art.

[green] of a multiprocessor chip' through an 'asynch[ronous] communication network' 160 (highlighted in blue in Figure 4)." Pet. 30–31 (citing Ex. 1009, 6:26–28, 6:14–18, Fig. 4). Figure 4 of Nicol, as annotated in the Petition, is reproduced below. *Id.* at 31.



Petitioner argues that annotated Figure 4 shows “the passing of data (red) from PE1 (green) through the asynchronous communication network (blue) to PE2 (green) for further processing.” *Id.* at 31 (citing Ex. 1001 ¶ 148). Petitioner further contends, and it is not disputed (PO Resp. 22), that “[a]synchronous communication networks were well-known in the art.” *Id.* (citing Ex. 1001 ¶ 150 (citing Ex. 1022, 491–493)). Petitioner further contends that a “POSITA would have understood that, in Nicol’s system, the asynchronous communication network is provided, *solely*, in the situation where there is ‘*a need to communicate data between PEs (or with other system elements)*.’” *Id.* at 31–32 (citing Ex. 1009, 6:19–21; Ex. 1001

¶ 150). Petitioner asserts that “Nicol’s multiprocessor system is arranged with an asynchronous communication network (160 blue) specifically for the purpose of ‘passing results onto one or more other data processing units which are subsequently processing data.’” *Id.* at 32 (citing Ex. 1016, 11, 17; Ex. 1001 ¶¶ 151–152; Ex. 1022, 159, Fig. 3.14)).

Patent Owner argues that the “ACN<sup>11</sup> is needed to receive data from the PEs at different times, coordinate the data as part of the same set of tasks, and pass the coordinated data along to the controller” and that “[t]he use of the ACN does not necessitate communication across the PEs, much less imply that sequential data [sic] processing is performed.” PO Resp. 23 (citing Ex. 2024 ¶ 41). Patent Owner further argues that “Nicol describes a situation when a synchronization schema is needed (‘when there is a need to communicate data between PEs’), not that the use of a synchronization schema necessarily implies that data is being communicated between PEs.” *Id.*

We agree with Petitioner that a POSITA would have understood that Nicol discloses PEs to be “adapted for sequentially processing data.” Pet. Reply 8. Nicol describes that tasks are assigned among PEs. Ex. 1009, 6:11–13. Nicol also describes that when the PEs’ operating frequencies differ from one another, “there is an issue of synchronization that must be addressed.” Ex. 1009, 6:14–18. Nicol further describes that a synchronization schema “must be implemented when there is *a need to communicate data between PEs . . . that operate at different frequencies.*” *Id.* at 6:18–21. Nicol recognizes that the frequencies may be arranged such that the “collection of tasks that are assigned to the multiprocessor is

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<sup>11</sup> Asynchronous communication network.

completed at a predetermined time,” but there remains “the issue of synchronizing *the exchange of data among the PEs* of a multiprocessor chip.” *Id.* at 6:21–28. “To effect such synchronization, each PE within the FIG. 4 arrangement is connection [sic] to an arrangement comprising elements 150 and 160” where element “160 resolves the issue of different clock domains.” *Id.* at 6:29–33.

We find that a POSITA would have understood such descriptions in Nicol to mean that data is passed from one PE through the asynchronous communication network to another PE (e.g., one PE passes results to another PE) as seen above in Petitioner’s annotated Figure 4. Pet. 30–31.

Petitioner’s explanation that Nicol’s description is captured in annotated Figure 4, which shows “the passing of data (red) from PE1 (green) through the asynchronous communication network (blue) to PE2 (green) for further processing,” is supported by record evidence. *Id.* at 31. This is so because Nicol describes “the need to communicate data between PEs” and “synchronizing the exchange of data among the PEs” by using the asynchronous communication network. Ex. 1009, 6:14–33; Ex. 1001 ¶ 148.

We disagree with Patent Owner that Nicol’s asynchronous communication network does not allow PE-to-PE communication, but only communication between the individual PEs and the controller. PO Resp. 23 (citing Ex. 2024 ¶ 41). Patent Owner’s declarant, Dr. Mangione-Smith, testifies that “[t]he ACN is needed to receive data from the PEs at different times, coordinate the data as part of the same set of tasks, and pass the coordinated data along to the controller” and that “[t]he use of the ACN does not necessitate communication across the PEs, much less imply that sequential data processing is performed.” Ex. 2024 ¶ 41 (citing Ex. 1009, 6:14–17). We do not give much weight to Dr. Mangione-Smith’s testimony

in that regard, because these assertions are not supported by record evidence. The portion of Nicol that Dr. Mangione-Smith relies on explains that “if the frequencies at which the individual PEs operate differ from one another and from other elements within the system where the multiprocessor chip is employed, there is an issue of synchronization that must be addressed.” Ex. 1009, 6:14–17. Dr. Mangione-Smith fails to explain sufficiently how that Nicol description would have led a POSITA to the conclusion that Nicol’s asynchronous communication network does not allow PE-to-PE communication, but only communication between the individual PEs and the controller. Indeed, such a conclusion appears to be contradictory to Nicol’s disclosures of the “need to communicate data between PEs,” and “synchronizing the exchange of data among the PEs” by using the asynchronous communication network. Ex. 1009, 6:14–33.

Moreover, we agree with Petitioner that during cross-examination, Dr. Mangione-Smith acknowledged that Nicol’s PEs do communicate with each other. Pet. Reply 9–10 (citing Ex. 1052, 60:18–61:9, 95:11–15, 107:14–108:1). Patent Owner appears to agree that Dr. Mangione-Smith acknowledged that Nicol’s PEs do communicate, but argues that such communication does not always imply “passing results for sequential processing,” because such communication “could just be ‘know[ing] [whether] the other task [finished]’ or ‘fir[ing] off’ other tasks.” Sur-reply 15 (citing Ex. 1052, 95:3–6, 96:1–3). Patent Owner fails to explain why a PE communicating to another PE that a task is finished so that the receiving PE then fires off other tasks does not meet the claim construction set forth by the District Court (“pass[ing] results to one or more additional data processing units to perform additional computations”). We determine that such communication meets the agreed upon construction of the disputed

phrase.

In addition, Nicol does not describe its PEs as simply communicating. Rather, Nicol explicitly describes *communicating data* between PEs and *synchronizing the exchange of data* among the PEs. Ex. 1009, 6:14–33. We agree with Petitioner that such descriptions would have led a POSITA to understand that Nicol’s PEs pass data (results) to one or more PEs for further processing. Pet. 30–32.

Lastly, Dr. Mangione-Smith agreed that Nicol describes taking a task and breaking it up into multiple subtasks to divide across multiple PEs, resulting in communication between the PEs. Ex. 1052, 60:20–61:3. He further testified that when you have a task and break it up among PEs that there would be “*dependence* between them, so there will almost always be some communication.” *Id.* at 60:11–15. Accordingly, Dr. Mangione-Smith appears to concede that Nicol meets the disputed limitation, because breaking up tasks into subtasks and dividing those subtasks between PEs results in “dependence between them” and, thus, communication between the PEs as claimed (passing results to perform additional computations). Pet. Reply 9–10.<sup>12</sup>

*b. Claim 1: “the multiprocessor system setting a clock frequency, of at least a part of the multiprocessor system to*

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<sup>12</sup> We disagree with Patent Owner that Dr. Mangione-Smith was referring to a hypothetical and not Nicol. Sur-reply 15–16. The question posed to Dr. Mangione-Smith was framed with respect to Nicol. Ex. 1052, 60:20–61:3. In any event, this testimony is only further evidence that the disputed limitation is met. The record evidence discussed above without this portion of Dr. Mangione-Smith’s statement (Ex. 1052, 60:20–61:3) is sufficient for us to determine that a POSITA would have understood such descriptions in Nicol to mean that data is passed from one PE through the asynchronous communication network to another PE (e.g., one PE passes results to another PE).

*a minimum in accordance with a number of pending operations of a first processor”*

Petitioner provides three alternative ways that Nicol teaches the above limitation. Pet. 35–39. For purposes of this Decision, we focus on the first two ways. First, Petitioner contends, and we agree, that Nicol’s controller of the multiprocessor system sets a clock frequency to a minimum according to a number of pending operations (instructions) of each of the PEs, including the number of pending operations of PE1 (the first processor). *Id.* at 35 (citing Ex. 1009, Fig. 4; Ex. 1001 ¶¶ 161–162). In particular, Petitioner asserts, and we find, that Nicol describes that the controller allocates tasks to the individual processors (PEs) including a first processor (labeled PE1 in the Petition) to equalize processing load among the PEs and then lowers the clock frequency on the chip to as low a level as possible while assuring proper operation. *Id.* at 36 (citing Ex. 1009, 2:23–27). According to Petitioner, Nicol describes, and we agree, that the controller takes into account the number of pending operations (instructions) of each PE (including PE1) in its determination of processing load and task allocation. *Id.* at 36–37 (citing Ex. 1009, 3:13–18; Ex. 1001 ¶ 165). Petitioner further contends, and we agree, that Nicol Figure 3 illustrates setting the clock frequency of the multi-processor system to a minimum (70 MHz) when the PEs (including PE1) have a light load. *Id.* at 37 (citing Ex. 1009, 3:31–33, 4:54–62, 5:23–28, Fig. 3; Ex. 1001 ¶ 166).

As a second way that Nicol meets the limitation, Petitioner argues, and we agree, that Nicol describes “setting the clock frequency to zero if none of the PEs are needed because all tasks have been completed and there are no new tasks or pending operations for any PE.” *Id.* at 37–38 (citing Ex. 1009, 5:42–44; Ex. 1001 ¶ 168).



Patent Owner argues that Petitioner fails to show that Nicol discloses or renders obvious the above limitation and that Petitioner improperly combines Nicol’s Figure 2 and Figure 4 embodiments. PO Resp. 17–19, 28–34. First, Patent Owner argues that Petitioner “improperly points to features from different embodiments in Nicol without explaining how they are interchangeable or how they fit together into a single system.” *Id.* at 28 (citing Ex. 2024 ¶ 48); *see also id.* at 18. Patent Owner further argues that Petitioner points to Figure 4, but relies on passages that describe the Figure 2 embodiment. *Id.* at 28–29. Patent Owner argues that the Figure 2 descriptions outline a “different scenario from Figure 4, where ‘the operating system [can] independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.’” *Id.* at 29 (citing Ex. 1009, 5:67–6:2; Ex. 2027, 19:19–21; Ex. 2024 ¶ 49); *id.* at 17–18. Patent Owner contends that “the Figure 2 embodiment where the load is distributed evenly as possible” is “exactly opposite to the situation that Figure 4 embodiment addresses.” *Id.* at 30 (citing Ex. 1009, 5:60–61; Ex. 2027, 33:4–7, 33:13–16).

Patent Owner’s arguments focus too narrowly on the individual embodiments shown and described in Nicol Figures 2 and 4, and do not adequately address Petitioner’s showings, which rely on Nicol as a whole. Pet. 25–29, 35–38, 40. For example, the Petition relies on an *annotated* Figure 4 to show and label different PEs (PE1 and PE2) for purposes of showing the claimed “a first processor” and “a second processor.” Pet. 36, 40. Notably, Petitioner does not rely on the passages related to Figure 4 that Patent Owner points to in arguing that Petitioner improperly mixes and matches embodiments, *e.g.*, Exhibit 1009, 5:60–61, 5:67–6:2. Pet. 35–41. Furthermore, the Petition makes clear that Figure 3, which Petitioner

primarily relies on to show setting of the clock frequency for the *annotated Figure 4 system* illustrates how the claim limitations are met. *Id.* Patent Owner’s incompatibility arguments are based on glossing over the teachings of Figure 3 altogether, while rigidly focusing only on certain descriptions of Figures 2 and 4. PO Resp. 17–19, 28–30. Indeed, Dr. Mangione-Smith’s testimony regarding the incompatibility of Nicol’s Figure 2 and Figure 4 embodiments does not mention Nicol Figure 3 at all. Ex. 2024 ¶¶ 37, 48–51. With this in mind, we address Patent Owner’s incompatibility arguments.

We agree with Petitioner that an emphasis in Nicol is “Nicol’s real-time operating system (‘RTOS’) software, which cuts across all embodiments.” Pet. Reply 7 (citing Ex. 1009, 2:18–27, 6:27–33). We also agree with Petitioner that Nicol describes a controller (containing the RTOS software) that allocates tasks among PEs and controls their frequency and voltage settings, “regardless of the number and types of PEs, and regardless how PEs are connected to DC-DC converters (which supply their voltages under RTOS control) and PLLs (which supply their clock frequencies under RTOS control).” Pet. Reply (citing Pet. 12–16; Ex. 1009, 2:18–27, 6:27–33; Ex. 1055 ¶ 13).

We have considered Patent Owner’s argument and Dr. Mangione-Smith’s testimony that a POSITA would not have considered the descriptions with respect to Figure 2 to be applicable to Figure 4, but disagree with the argument and find the testimony of Dr. Sechen to be more persuasive than that of Dr. Mangione-Smith. Ex. 2024 ¶ 48; Ex. 1055 ¶¶ 13–14. Nicol does describe that in the Figure 4 embodiment, “the operating system [can] independently program the lowest operating frequency and corresponding lowest supply voltage for each PE.” Ex. 1009, 5:67–6:2. Nicol, however, also describes that when each PE has its own

supply voltage, like that shown in Figure 4, “chip-wise voltage scaling is most effective when the load of the computation can be evenly distributed across all of the PEs.” *Id.* at 5:53–59. We agree with Petitioner that a POSITA would have understood such description to mean that “the PEs operate in unison exactly as in the Figure 2 embodiment.” Pet. Reply 7, 11. Nicol also describes a “middle ground” where “the PEs of a multi-processor chip can be divided into groups, and each group of PEs can be arranged to operate from its own controlled supply voltage.” *Id.* at 6:61–7:3. Thus, Nicol is not as rigid in its teachings as Patent Owner asserts.

Dr. Mangione-Smith’s testimony that the Figure 2 and Figure 4 embodiments are not combinable or that the respective “designs are diametrically opposed” is entitled to little weight, because it narrowly focuses on certain passages in Nicol, while failing to take into consideration other passages in Nicol discussed above. Ex. 2024 ¶¶ 37, 48. Moreover, as Petitioner points out (Pet. Reply 7–8 (citing Ex. 1051, 60:4–7, 65:12–25)), during cross-examination, Dr. Mangione-Smith testified that Nicol’s “middle ground” is a combination of Nicol’s Figure 2 and Figure 4 embodiments, undermining his original testimony that the Figure 2 and Figure 4 embodiments are not combinable or that the respective “designs are diametrically opposed.” Ex. 2024 ¶¶ 37, 48.

We also agree with Petitioner, and it is not disputed, that a POSITA would have understood that Figure 3, which Petitioner relies on in the Petition to illustrate the disputed limitation, applies to both systems of Figure 2 and Figure 4. Pet. Reply 11 (citing Pet. 37–38; Ex. 1009, 4:54–66). As explained in the Petition, Figure 3 shows the initial 70 MHz frequency setting is at a minimum when the PEs, including PE1 (of annotated Figure 4), have a light load. Pet. 36–37 (citing Ex. 1009, 2:23–27, 3:13–18, 3:31–

33, 4:54–62, 5:23–28).<sup>13</sup> In the case where the PEs of Figure 4 operate with the same voltage and frequency applied to all PEs to achieve “chip-wise scaling,” “the initial 70 MHz frequency setting is the minimum frequency needed to handle the tasks at hand by the PEs, which takes into account the number of pending operations of the PE identified in the Petition as the ‘first processor’ (PE1).” Pet. Reply 12 (citing Pet. 36–37; Ex. 1009, 2:23–27 (“the controller lowers the clock frequency on the chip to *as low a level as possible* while assuring proper operation”); 3:13–18 (the controller “determine[s] the best way to allocate the tasks to the available processors” by taking into account “*the number of instructions* that need to be executed for each task”); Ex. 1055 ¶ 21). For the above reasons, we determine that Petitioner has demonstrated sufficiently that its first showing with respect to the teachings of Nicol meets the disputed limitation.<sup>14</sup>

Next, we address Patent Owner’s arguments regarding Petitioner’s second showing (Pet. 37–38) as to how the disputed limitation is met. PO Resp. 31–32. Patent Owner argues that “Petitioner points to the disclosure ‘the operating system employs gated clocking techniques to ‘shut down’ PEs

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<sup>13</sup> As noted above, Patent Owner and Dr. Mangione-Smith fail to discuss Figure 3 at all in making the Figure 2 and Figure 4 incompatibility arguments. PO Resp. 17–19, 28–30; Ex. 2024, ¶¶ 37, 48–51.

<sup>14</sup> Patent Owner’s argument that “PE1 does not set the frequency of the system, but only its own frequency” is not particularly relevant to Petitioner’s showing (Pet. 36–37), because Patent Owner’s arguments are based on the assumption that Figure 4 is solely directed to the case where the operating system independently programs the lowest operating frequency and corresponding lowest supply voltage for each PE. PO Resp. 30–31 (citing Ex. 1009, 5:66–6:6; Ex. 2024 ¶ 51). As explained above, Nicol also states that the Figure 4 system can operate with the same voltage and frequency applied to all PEs to achieve “chip-wise scaling.” Ex. 1009, 5:53–59.

that are not needed,’ (Ex. 1009, 5:42–44) and simply assumes without considering the context that this is done in accordance with the number of pending operations.” PO Resp. 31 (citing Ex. 2024 ¶ 52). Patent Owner further argues that Nicol describes the need to shut down certain circuits because they fail due to low voltage, not that clock frequencies are set according to the number of pending operations of any processor. *Id.* at 32 (citing Ex. 2024 ¶ 52).

Petitioner responds that “PO and its expert incorrectly contend that clock-gating” is “used in Nicol to avoid circuit failure” and “misrepresent Nicol’s teaching.” Pet. Reply 14. Petitioner argues that the quote from Nicol that “ $V_{dd}$ -local can only be reduced so-far before the circuits start to fail” means “that PEs are designed to operate over a certain  $V_{dd}$  range and cannot operate below a minimum design voltage.” *Id.* (citing Ex. 1009, 5:42–45, Figure 1; Ex. 1055 ¶ 23). Petitioner argues that “when a PE is idling, reducing its  $V_{dd}$  supply voltage below its minimum voltage to save power is not appropriate as the circuit would fail and, instead, the PE should be clock-gated and its voltage maintained at minimum voltage or higher.” *Id.* (citing Ex. 1055 ¶ 23). Lastly, Petitioner argues that clock gating was commonly used in computer systems to temporarily shut down circuits that are not needed to save power. *Id.* (citing Pet. 38; Ex. 1055 ¶ 22; Ex. 101, 1:30–46).

We give substantial weight to Dr. Sechen’s testimony that Nicol’s description of employing gated clocking techniques to “shut down” PEs that are not needed means setting “the clock frequency of some or all PEs to zero (‘clock gating’) when those PEs are not needed, *e.g.*, because the number of pending operations for those PEs is zero (*i.e.*, no load).” Ex. 1055 ¶ 22 (citing Ex. 1010, 1:30–46 for the proposition “that clock gating was

commonly used in computer systems to temporarily shut down circuits that are not needed to save power”); Ex. 1009 ¶¶ 168–169. We further give substantial weight to Dr. Sechen’s testimony that a person having ordinary skill in the art would have understood Nicol’s description at column 5, lines 42 to 45, to teach that a “PE should be clock-gated and its voltage maintained at the minimum voltage or higher when the PE is not needed (no pending operations)” and that a “controller would not reduce its  $V_{dd}$  supply voltage below its minimum voltage to save power because the circuit would fail.” Ex. 1055 ¶ 23. We do not give substantial weight to Dr. Mangione-Smith’s testimony that Nicol is describing “the need to shut down certain circuits because they fail due to low voltage.” Ex. 2024 ¶ 52. Nicol does not describe shutting down circuits to avoid circuit failure. Rather, in totality, the passage contains the important disclosure that gated clocking techniques are used “to ‘shut down’ PEs *that are not needed.*” Ex. 1009, 5:42–45 (emphasis added). Dr. Mangione-Smith fails to explain why a POSITA would have understood Nicol to teach shutting down circuits to avoid circuit failure instead of shutting down PEs that are not needed. Dr. Sechen’s responsive Reply testimony is unrebutted<sup>15</sup> and consistent with record evidence that clock gating was commonly used in computer systems to temporarily shut down circuits that are not needed to save power. Ex. 1010, 1:30–46. For the above reasons, we determine that Petitioner has demonstrated by a preponderance of the evidence that its second alternative

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<sup>15</sup> In the Sur-reply Patent Owner does not address the merits of Dr. Sechen’s testimony.

showing with respect to the teachings of Nicol meets the disputed limitation.<sup>16,17</sup>

*c. Claim 1: “the multiprocessor system subsequently increasing the clock frequency of the at least the part of the multiprocessor system to a maximum in accordance with a number of pending operations of a second processor”*

For the above limitation, Petitioner contends that Nicol describes a controller that adjusts the clock frequency of the system according to pending operations of each of the PEs. Pet. 39 (citing Ex. 1009, 2:23–27, 3:13–18, Fig. 4). Petitioner further contends that Nicol describes the controller taking into account the number of pending instructions for each PE, including a second processor, because it sets the clock frequency based on identifying the processing requirement of “the most heavily loaded PE.” *Id.* at 40 (citing Ex. 1009, 3:66–4:5; Ex. 1001 ¶ 176). Petitioner contends that Nicol Figure 3 (annotated in the Petition) illustrates the multiprocessor system increasing the clock frequency to 140 MHz (maximum clock frequency) prior to execution of a high load. *Id.* at 40–41 (citing Ex. 1009, 3:31–33, 4:54–62, 5:23–28, Fig. 3; Ex. 1001 ¶ 177). Petitioner further contends that Nicol describes each chip having a maximum frequency that the chip can support and that for a maximally utilized system, all of the

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<sup>16</sup> Patent Owner’s argument that “Petitioner is attempting to offer a new ground, and it should not be considered” (Sur-reply 21) is moot, as that argument pertains to Petitioner’s third alternative showing (Pet. 38–39), which is not included in this Decision.

<sup>17</sup> Petitioner presents three separate, alternative ways in which Nicol meets the disputed limitation (Pet. 35–39), two of which we discuss in this Decision. Patent Owner’s argument regarding combining the three different ways set forth in the Petition is not relevant to this Decision, because Petitioner does not combine the three alternative ways together into a single embodiment as Patent Owner suggests. PO Resp. 33–34; Pet. Reply 13 n.4.

available processors would operate at full speed (maximum frequency) when satisfying the maximum load encountered by the system. *Id.* at 41 (citing Ex. 1009, 2:65–3:4, 3:63–64; Ex. 1001 ¶ 178).

Patent Owner argues that Petitioner fails to show that Nicol discloses or renders obvious the above limitation. PO Resp. 34–40. Patent Owner repeats its arguments regarding Petitioner improperly mixing descriptions from Nicol related to Figure 2 and Figure 4 embodiments (*id.* at 34), which we have addressed and our analysis applies here as well. In addition, Patent Owner argues that in the Figure 4 embodiment, where each PE’s operating frequency is set independently based on its own load, “Petitioner has failed to show how this limitation is met by the disclosures of Nicol.” *Id.* at 34–36 (citing Ex. 2024 ¶¶ 56–58). Again, Patent Owner’s arguments are based on the notion that “the Figure 2 embodiment, . . . is not applicable here for Figure 4.” *Id.* at 36 (citing Ex. 2024 ¶ 57). As explained above, we determine that the Figure 2 embodiment and the descriptions of that embodiment are applicable to the Figure 4 embodiment. In particular, we agree with Petitioner that “PO erroneously contends that the controller in Figure 4 can only rigidly set the clock frequency of each PE according to its own workload.” Pet. Reply 17. Patent Owner ignores Nicol’s teaching that “[w]hen tasks can be evenly divided, the controller adjusts their frequency and supply voltage in unison (‘chip-wise’ scaling), taking into account all of the PE workloads.” *Id.* (citing Ex. 1009, 5:56–59).

Next, Patent Owner argues that even assuming “that the Figure 2 disclosure in Nicol is applicable for the Figure 4 embodiment,” Petitioner has failed to show that the clock frequency is increased to a maximum in accordance with a number of pending operations of a second processor. PO Resp. 37 (citing Ex. 2024 ¶ 59). Patent Owner further argues that Nicol



does not teach setting both PEs to 140 MHz or running the system at maximum frequency. *Id.* at 38–40 (citing Ex. 2024 ¶¶ 60–61).

We agree with Petitioner that the Petition shows how Nicol’s “controller sets the maximum clock frequency of PE1, taking into account the workload (*e.g.*, number of pending operations) of all PEs, including the PE mapped to the claimed second processor (PE2).” Pet. Reply 17 (citing Pet. 39–40). For instance, the Petition explains that “Nicol Figure 3 illustrates the multiprocessor system increasing the clock frequency of the PEs [including PE1] of the multiprocessor system from 70 MHz (minimum clock frequency) to 140 MHz (maximum clock frequency) prior to the execution of a high load, *i.e.*, involving a number of pending operations for the PEs [including PE2].” Pet. 40–41 (citing Ex. 1001 ¶ 177; Ex. 1009, 3:31–33, 4:54–62, 5:23–28). We further agree with Petitioner that a POSITA would have understood that Nicol teaches or suggests the scenario where the “most heavily loaded” processor can be both PE1 and PE2 contrary to Patent Owner’s assertions. Pet. Reply 18–19 (citing Ex. 1055 ¶¶ 29–30).

As Dr. Sechen explains, “both PE1 and PE2 can be the ‘most heavily loaded’ when the tasks are evenly divided among available PEs. Those available PEs (which includes PE1 and PE2) would be equally loaded, both the ‘most heavily loaded’ compared, for example to clock-gated PEs with no load.” Ex. 1055 ¶ 29. Dr. Sechen further testifies, and we find, that Nicol describes embodiments where all PEs of the chip (Figure 2) or the PEs within a group (middle ground) share the same DC-DC converter and PLL (Ex. 1009, 6:66–7:3). *Id.* ¶ 30. Dr. Sechen further testifies, and we find, that in such a case, all PEs on the chip (Figure 2), or PEs within the same group (middle ground) operate in unison, with the same clock frequency and

supply voltage applied to the PEs. *Id.* (citing Ex. 1009, 3:9–42). He further explains, and we agree, that the 70MHz in Figure 3 represents the frequency common to the PEs, determined based on the workload of the most heavily loaded PE (e.g., PE1) at some point prior to the new task creation. *Id.* (citing Ex. 1009, 4:54–60, Figure 3). He further testifies, and we agree, that, “subsequently, Nicol’s Figure 3 also illustrates a maximum frequency of 140MHz (common to all PEs or the group of PEs) that is determined based on the workload of the most heavily loaded PE (‘PE2’), taking into account the additional workload due to the ‘new task.’” *Id.* (citing Ex. 1009, 3:66–4:6). His explanation is consistent with Petitioner’s showing in the Petition. Pet. 39–41 (citing Ex. 1001 ¶¶ 176–178). And as pointed out by Petitioner, Dr. Mangione-Smith testified that in the middle ground embodiment “if there’s a PE that is not the most heavily loaded one, *its operating state will be set based on whatever the load is of the most heavily loaded PE.*” Ex. 1051, 69:13–16 (emphasis added). Such testimony undermines Patent Owner’s argument that “Petitioner does not explain why a POSITA would operate PE1 or PE2 at the maximum frequency rather than a lower frequency when there are clock-gated PEs with no load.” Sur-reply 22.

We also disagree with Patent Owner that Nicol teaches away from running PEs at a maximum frequency of 140 MHz. PO Resp. 39–40; Sur-reply 22 (“Petitioner does not explain why a POSITA would operate PE1 or PE2 at the maximum frequency rather than a lower frequency when there are clock-gated PEs with no load”). Nicol expressly describes otherwise. In particular, Nicol states that “[f]or a maximally utilized system, all of the available processors ought to be operating at full speed when satisfying the maximum load encountered by the system.” Ex. 1009, 2:65–3:4. Petitioner explained this in its Petition. Pet. 41 (citing Ex. 1009, 2:65–3:4, 3:63–64;

Ex. 1001 ¶ 178). And even Dr. Mangione-Smith admitted that “a particular load situation may cause them [PEs] all to be running at their highest possible clock frequency and voltage.” Ex. 1051, 54:2–14. Patent Owner fails to direct us to anything in Nicol that “discredits or criticizes running PEs at their maximum frequency.” Pet. Reply 20. A POSITA would have understood that Nicol contemplates such a maximum frequency scenario. Ex. 1001 ¶ 178; Ex. 1055 ¶ 31.

Patent Owner makes several arguments that it is prejudiced by the “late” introduction of “new arguments” Petitioner has made with respect to the above limitation. Sur-reply 21–22. In particular, Patent Owner argues that Petitioner’s explanation of Nicol’s description relating to “chip-wise” scaling with respect to Figure 4 “is new.” *Id.* at 22. We disagree that Patent Owner was prejudiced or denied due process.

First, petitioners are not prohibited from relying on new evidence and arguments in a reply, if the evidence and arguments are responsive to arguments made in a patent owner response. *See* 37 C.F.R. 42.23(b); Consolidated Trial Practice Guide (“Consolidated Practice Guide”)<sup>18</sup> at 73; *Hulu, LLC. v. Sound View Innovations, LLC*, IPR2018-01039, Paper 29 at 15 (PTAB Dec. 20, 2019) (precedential) (“For example, if the patent owner challenges a reference’s status as a printed publication, a petitioner may submit a supporting declaration with its reply to further support its argument that a reference qualifies as a printed publication”). Here, we determine that Petitioner’s arguments and accompanying evidence (*e.g.*, Ex. 1055) in connection with the Petitioner Reply are responsive to Patent Owner’s arguments.

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<sup>18</sup> Available at <https://www.uspto.gov/TrialPracticeGuideConsolidated>.

Specifically, an underlying theme of Patent Owner's Response and Dr. Mangione-Smith's testimony is that a POSITA would not have considered the descriptions with respect to Figure 2 to be applicable to Figure 4. PO Resp. 17–19, 28–30, 34–36; Ex. 2024 ¶¶ 37, 48, 55, 57, 58. In response, Petitioner provides a detailed explanation as to how Nicol's embodiments share common functionality and that such a narrow view of the teachings of Nicol proposed by Patent Owner is improper. Pet. Reply 6–8, 10–12, 16–17; Ex. 1055. This explanation includes showing how Nicol describes “chip-wise” scaling that applies to the Figure 4 embodiment. Pet. Reply 17. And this explanation is not inconsistent with what was presented in the Petition. In other words, and as explained above, the Petition relies on an *annotated* Figure 4 to show and label different PEs (PE1 and PE2) for purposes of showing the claimed “a first processor” and “a second processor.” Pet. 36, 40. The Petition, however, does not rely on the passages related to Figure 4 where the tasks are not evenly divided, as Patent Owner asserts (Sur-reply 21), *e.g.*, Exhibit 1009, 5:60–61, 5:67–6:2. Pet. 35–41.

Moreover, we disagree with Patent Owner that Petitioner's arguments with respect to its Reply are improper, or should have been made in connection with the Petition. Petitioner could not have anticipated that Patent Owner would present such a narrow reading of Nicol. Moreover, Patent Owner could have cross-examined Dr. Sechen after his Reply declaration had been submitted into the record. Paper 12, 4 (“5.”). There is no transcript in the record of any deposition taken of Dr. Sechen after his reply declaration was made. Nor did Patent Owner request to submit new testimony in support of its Sur-reply. For these reasons, we determine that Patent Owner has not been prejudiced or denied due process, and that we

may consider the reply arguments and Dr. Sechen's reply testimony in support of the arguments.

*d. Claim 1: "the multiprocessor system subsequently reducing the clock frequency of the at least the part of the multiprocessor system in accordance with (a) an operating temperature threshold preventing over-temperature and (b) a hysteresis characteristic"*

Petitioner contends that Nicol in combination with Kling meets the above limitation. For example, Petitioner contends, and we agree, that Kling describes that processing systems must be able to rapidly detect and mitigate over-temperature situations, and that if a processor temperature exceeds a particular threshold, the processor is placed into low power mode until it cools off. Pet. 41–42 (citing Ex. 1010, 1:38–46).

Petitioner further contends that a person having ordinary skill in the art would have found it obvious to detect over-temperature in Nicol's multiprocessor system (which itself describes on-chip temperature sensors for tracking temperature) by comparing the system's measured temperatures against a threshold temperature. *Id.* at 42–43 (citing Ex. 1009, 4:11–13; Ex. 1010, 1:43–45; Ex. 1011, 1:6–12; Ex. 1001 ¶¶ 183, 185–186). Petitioner further contends, and we agree, that Kling describes that once an over-temperature is detected, the chip is placed into low power mode, and that a person having ordinary skill in the art would have known that placing Nicol's system in a low power mode would have required reducing the clock frequency to reduce power consumption. *Id.* at 43 (citing Ex. 1009, 1:26–28; Ex. 1010, 1:44–45; Ex. 1001 ¶¶ 187–188). Petitioner also contends, and we agree, that Kling describes the use of hysteresis to improve robustness and reduce the occurrence of power oscillation and that it would have been obvious to a person having ordinary skill in the art to include Kling's

hysteresis teaching to Nicol’s system. *Id.* at 44–45 (citing Ex. 1010, 5:50–58; Ex. 1001 ¶¶ 189–190, 192).

Patent Owner argues that Petitioner “relies entirely on Kling” to teach “over-temperature” and that “Nicol discusses voltage scaling based on temperature variations, but not clock frequency changes.” PO Resp. 40 (citing Ex. 2024 ¶ 62). Petitioner does not rely solely on the teachings of Kling to meet the disputed limitation as Patent Owner asserts. Pet. 41–43. As such, Patent Owner’s arguments fail to rebut Petitioner’s showing that Nicol in view of Kling teaches reducing clock frequency of “the at least the part of the multiprocessor system in accordance with (a) an operating temperature threshold preventing over-temperature.” *Id.*

Kling describes that “[i]f the processor temperature exceeds a particular threshold, *the processor is placed into low power mode until it cools off*. If these precautions are not taken, the processor may destroy itself by its own heat.” Pet. 41–42 (citing Ex. 1010, 1:38–46). We agree with Petitioner that a POSITA would have understood Kling’s description to mean comparing a system’s measured temperatures against a temperature threshold, which meets “an operating temperature threshold preventing over-temperature.” *Id.* at 42 (citing Ex. 1001 ¶ 183; Ex. 1010, 1:43–45; Ex. 1011, 1:6–12). Patent Owner does not contend otherwise. PO Resp. 40–41.

We further agree with Petitioner that the combined teachings of Nicol and Kling results in “reducing the clock frequency” of Nicol’s PEs once an over-temperature is detected. *Id.* at 43 (citing Ex. 1009, 1:26–28; Ex. 1010, 1:44–45, 2:43–52; Ex. 1001 ¶¶ 186–188). We disagree with Patent Owner that “[a] reduction in clock frequency due to temperature would prevent tasks from being completed on time.” *Id.* at 40–41 (citing Ex. 2024 ¶ 62). Dr. Mangione-Smith testifies that “Nicol discusses voltage scaling based on

temperature variations, but not clock frequency changes. Therefore, it is my opinion that a POSITA would understand Nicol to teach away from reducing a clock frequency due to temperature because doing so would prevent Nicol from completing tasks on time.” Ex. 2024 ¶ 62. Dr. Mangione-Smith’s testimony is not particularly relevant, because the disputed claim language is directed to “preventing over-temperature,” not merely sensing temperature in general. Moreover, neither Patent Owner nor Dr. Mangione-Smith points to record evidence to show that a reduction in clock frequency due to an *over-temperature* would prevent tasks from being completed on time.<sup>19</sup> As Petitioner points out, during cross-examination, Dr. Mangione-Smith testified that a person of ordinary skill in the art would have understood how to manage temperature in Nicol’s multiprocessor system. *See* Pet. Reply 20–21 (citing Ex. 1052, 129:23–130:9 (Patent Owner’s expert agreeing that a person of ordinary skill in the art would have known of ways to use a temperature sensor in implementing Nicol “[a]t least to the extent that the Pentium disclosed it, for example”)).

Next, Patent Owner argues that “Kling describes that hysteresis could be used to reduce power oscillation” but “provides no explanation as to how hysteresis would be implemented . . . or how it could be implemented in alternative systems such as Nicol.” PO Resp. 41–42 (Ex. 2024 ¶ 64). Patent Owner argues that (1) Petitioner does not point to any unwanted oscillation in Nicol or a need to reduce unwanted oscillation through hysteresis; (2) a single mention of hysteresis in Kling is insufficient to show that

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<sup>19</sup> This argument relates to Patent Owner’s argument that a POSITA would not have been motivated to combine the teachings of Nicol and Kling because doing so would prevent the combined system from working efficiently. *See, e.g.*, PO Resp. 55–57. We address the arguments below.

implementation of hysteresis was well known; and (3) Petitioner interprets Kennedy to suggest that hysteresis was indispensable and commonly used in noisy environments and to guard against false triggers, but Kennedy makes no such claim. PO Resp. 42 (Ex. 2024 ¶ 65).

The Petition does not rely solely on a “single mention of the term hysteresis” in Kling to meet the disputed limitation of reducing the clock frequency “in accordance with (a) an operating temperature threshold preventing over-temperature and (b) a hysteresis characteristic.” PO Resp. 41–42. The Petition explains that the use of hysteresis to avoid false triggers was well known in the art, and does not rely only on Kling to show that hysteresis was used to avoid excessive switching or unnecessary oscillations. Pet. 44 (citing Ex. 1010, 5:50–58; Ex. 1001 ¶ 190; Ex. 1021, 471); Pet. Reply 21 (citing Ex. 1055 ¶ 37). Importantly, Patent Owner does not present rebuttal evidence that Kling does not teach hysteresis, but only argues that Kling has a “single mention of the term hysteresis.” PO Resp. 41. The ’605 patent also only contains a single mention of the term hysteresis. Ex. 1003, 13:50–53. There is no explanation in the ’605 patent explaining what hysteresis is or how it works. We agree with Petitioner that a reasonable reading of the ’605 patent on hysteresis was not necessary, because at the time of the invention a POSITA would have known what hysteresis was and how it worked. Pet. Reply 21 (citing Ex. 1055 ¶ 36). We agree with Petitioner, and it is not disputed that a hysteresis characteristic “is commonly implemented by comparing the same signal against two thresholds, as shown in Kling Figure 2A.” Pet. 44 (citing Ex. 1010, 5:51–54). We further agree with, and give substantial weight to Dr. Sechen’s testimony, that it would have been obvious to apply the well-known two-threshold method (providing hysteresis) from Kling in implementing an over-temperature



monitoring system in Nicol to reduce unwanted oscillations. Ex. 1001 ¶ 192; *see also* Ex. 1055 ¶ 37 (explaining that like a thermostat control system, “an over-temperature protection system requires the use of hysteresis to avoid constantly switching between a normal operation mode . . . and an over-temperature protection mode”).

For all the above reasons, we determine that Petitioner has sufficiently demonstrated that Nicol combined with Kling meets the disputed limitation.

*e. Claim 1: Motivation and Rationale to Combine*

Petitioner argues a person of ordinary skill in the art would have been motivated and found it obvious to combine the teachings of Nicol and Kling. Pet. 23–25, 42–45. For example, Petitioner contends, and we agree, that a POSITA would have been motivated to combine Kling’s over-temperature protection to Nicol’s multiprocessor system because it was known that over-temperature protection was critical for high-performance multiprocessor systems. *Id.* at 24, 42 (citing Ex. 1001 ¶ 127; Ex. 1009, 2:18–22, 3:9–20; Ex. 1010, 1:38–46; Ex. 1001 ¶¶ 127, 129, 182). Petitioner further contends, and we agree, that a POSITA would have been motivated to use temperature measurements to improve voltage scaling (taught in Nicol) and for over-temperature protection (taught in Kling). *Id.* at 42–43 (citing Ex. 1001 ¶ 186).

Patent Owner first argues that “[m]ere benefit without any showing of actual motivation is plainly insufficient to suggest a POSITA would combine these reference[s].” PO Resp. 54–55 (citing Ex. 2024 ¶ 82). We are not persuaded by this conclusory argument, because “[i]f a person of ordinary skill in the art can implement a predictable variation, and would see the benefit of doing so, § 103 likely bars its patentability.” *KSR Int’l Co. v.*

*Teleflex Inc.*, 550 U.S. 398, 401 (2007). In any event, Petitioner explains that a POSITA would have been motivated to combine Kling’s over-temperature protection to Nicol’s multiprocessor system because it was known that over-temperature protection was critical for high-performance multiprocessor systems. Pet. 24, 42 (citing Ex. 1001 ¶ 127; Ex. 1009, 2:18–22, 3:9–20; Ex. 1010, 1:38–46; Ex. 1001 ¶¶ 127, 129, 182). We find, and it is not disputed, that over-temperature protection was critical for high-performance multiprocessor systems. Ex. 1010, 1:42–47 (explaining that if thermal monitoring is not included “the processor may destroy itself by its own heat”). Nicol describes that temperature tracking would be desirable in its power management system (*see, e.g.*, Ex. 1009, 4:11–13 (explaining that “the operating system can reduce the supply voltage even further by tracking temperature and process variations”). Nicol, however, does not specifically provide details, and we give substantial weight to Dr. Sechen’s testimony that a POSITA would have been motivated to consult Kling and implement Kling’s over-temperature protection, which was known to be “critical for high-performance systems.” Ex. 1001 ¶ 127.

Next, Patent Owner argues that “Petitioner makes no attempt to explain how a system combining Nicol and Kling would function, likely due to the fact that managing a plurality of metrics to create an efficient processing system is extremely difficult.” PO Resp. 55–56 (citing Ex. 2024 ¶ 83). Patent Owner further argues that because Petitioner fails “to address how a combination of Nicol and Kling would actually function, Petitioner ignores any issues that would arise” such as “prioritization issues that would arise from these two different methods for changing frequency” which would be “difficult to implement them both simultaneously.” *Id.* at 56 (citing Ex. 2024 ¶ 84). In support of Patent Owner’s arguments, Dr.

Mangione-Smith testifies that there are prioritization issues that would arise from the different methods of Kling and Nicol for changing frequency and that it “is difficult to implement them both simultaneously.” Ex. 2024 ¶ 84. Dr. Mangione-Smith’s testimony is conclusory, because he does not explain what kind of prioritization issues would arise from the “two different methods for changing frequency.”

We agree with Petitioner that it is not disputed that both Nicol and Kling teach “a power management system in which a controller dynamically adjusts clock frequencies of PEs.” Pet. Reply 3 (citing PO Resp. 56; Ex. 1051, 157:13–18). We further agree with Petitioner that there are no prioritization issues because Kling’s over-temperature protection is a critical safety mode of operation, whereby the controller “puts the brakes on (‘throttles’) the processors to avoid catastrophic meltdown due to over-heating.” *Id.* (citing Pet. 16–18; Ex. 1010, 2:45–51, 4:50–5:8; Ex. 1055 ¶ 8). This “emergency braking” does not interfere with Nicol’s normal mode of operation as long as there is no risk of device failure due to over-heating. *Id.* Patent Owner’s attorney arguments in the Sur-reply simply overlook this or mischaracterize Petitioner’s reply arguments. Sur-reply 5–14.

For example, Patent Owner argues for the first time in the Sur-reply that “[r]egarding the hysteresis-based reduction, Petition[er] alleges that it is triggered by the upper power consumption threshold in Kling’s Figure 2A.” Sur-reply 6 (citing Pet. Reply 21). Not so. There is no “hysteresis-based reduction” limitation in claim 1. Rather, claim 1 requires reducing frequency in accordance with an operating temperature threshold preventing over-temperature and a hysteresis characteristic. The claim does not preclude reducing frequency based on an over-temperature threshold, taking into account a hysteresis characteristic as Patent Owner appears to contend.

Petitioner makes clear that Figure 2A from Kling is illustrative of how a hysteresis characteristic would have been applied in implementing an over-temperature monitoring system in Nicol to reduce unwanted oscillations. Pet. 44–45; Pet. Reply 21–22; Ex. 1001 ¶¶ 190–192; *see also* Ex. 1055 ¶ 37 (explaining that like a thermostat control system, “an over-temperature protection system requires the use of hysteresis to avoid constantly switching between a normal operation mode . . . and an over-temperature protection mode”); Ex. 1051, 138:2–12 (Dr. Mangione-Smith acknowledging that a two-level threshold band such as in a thermostat is a good example of hysteresis). Thus, Patent Owner’s new arguments (Sur-reply 7–8) that a POSITA “would [not] have been motivated to [further raise the power consumption when the processor already has unsafe hot spots so] that would result in [reaching the upper threshold to trigger a hysteresis reduction]” are based on a misunderstanding of Petitioner’s showing by bodily incorporating Kling into Nicol (*see, e.g.*, Sur-reply 12) without considering what the combined teachings of Nicol and Kling would have suggested to a person having ordinary skill in the art. *See In re Keller*, 642 F.2d 413, 425 (Fed. Cir. 1981).

We also are not persuaded by Patent Owner’s argument that it would be too difficult to combine the teachings of Nicol and Kling into a system, because “managing a plurality of metrics to create an efficient processing system is extremely difficult.” PO Resp. 55–56 (citing Ex. 2024 ¶ 83). Dr. Mangione-Smith fails to explain why it would be “extremely difficult” to combine the teachings of Nicol and Kling, only that it would be. Ex. 2024 ¶ 83. Such conclusory testimony is entitled to little weight. Moreover, record evidence describes otherwise. Kling describes that computer processor designers are continually striving to increase the

operating speed of processors, but as processor speed increases, power consumed by the processor increases as well, leading to thermal dissipation problems and decreased battery life. Ex. 1010, 1:19–29. Kling continues, by describing that:

Processor and computer system designers have developed numerous methods to deal with these issues. For example, processor designers implement specialized circuit design techniques that reduce power consumption. In addition, modern computer systems are designed to shut down portions of the system that are not needed during a particular period of time. Both of these techniques conserve power and help extend battery life.

To address the thermal issue, elaborate thermal dissipation systems are often affixed to the processor to help dissipate the heat from the processor to the ambient environment. Some processor packages include a thermal sensor to monitor the temperature of the processor. If the processor temperature exceeds a particular threshold, the processor is placed into lower power mode until it cools off. If these precautions are not taken, the processor may destroy itself by its own heat.

Ex. 1010, 1:30–46. We agree with Petitioner that the above description supports a finding that normal power management modes of operation *along with* over-temperature protection were “routinely implemented together in computer systems.” Pet. Reply 4 (citing Pet. 23–25; Ex. 1055 ¶ 9; Ex. 1010, 1:30–46). In addition, as explained above, during cross-examination, Dr. Mangione-Smith testified that a person of ordinary skill in the art would have understood how to manage temperature in Nicol’s multiprocessor system. *See* Pet. Reply 20–21 (citing Ex. 1052, 129:23–130:9 (Patent Owner’s expert agreeing that a person of ordinary skill in the art would have known of ways to use a temperature sensor in implementing Nicol “[a]t least to the extent that the Pentium disclosed it, for example”)).

Lastly, Patent Owner argues that “Kling would dissuade a POSITA from using a thermal sensor as proposed by Petitioner.” PO Resp. 56–57 (Ex. 2024 ¶ 85; Ex. 1010, 2:56–62). The Petition relies on Nicol’s existing temperature measurements used in Nicol for voltage scaling and proposes also using the same for over-temperature detection. Pet. 43 (citing Ex. 1001 ¶ 186). We agree with Petitioner that it would have been obvious to use Nicol’s existing temperature sensors to also detect over-temperature conditions. *Id.*; Pet. Reply (citing Pet. 43; Ex. 1055 ¶¶ 10–11; Ex. 1010, 1:38–46). This is especially so, given that Kling recognizes and specifically describes systems with normal power management modes of operation (like Nicol) *along with* over-temperature protection. Ex. 1010, 1:30–46.

Kling does describe an embodiment in which power consumption is directly monitored to avoid temperature measurement inaccuracies, which Kling describes as an “improvement over the use of thermal sensors to detect the high power condition.” *Id.* at 2:55–62. Patent Owner, however, does not explain how such a description of directly monitoring power consumption over using thermal sensors *to detect a high power condition* would have discouraged a POSITA from using thermal sensors to detect an *over-temperature condition*. Dr. Mangione-Smith fails to explain why Kling’s discussion regarding thermal sensors for detecting high power conditions is relevant to using thermal sensors for detecting an “over-temperature condition.” Ex. 2024 ¶ 85. Accordingly, we give little weight to Dr. Mangione-Smith’s testimony that “Kling would dissuade a POSITA from using a thermal sensor.” *Id.* Rather, we agree with Petitioner that a POSITA would have understood that Kling does not teach eliminating conventional temperature sensors for detecting an over-temperature thermal event. Pet. Reply 5 (citing Ex. 1055 ¶¶ 10–11).

*f. Dependent Claims 2–6*

*Claim 2*

Claim 2 depends from claim 1 and recites “wherein: said clock frequency is determined in part by processor voltage.” Petitioner contends that “a POSITA would have found it obvious to add Kling’s power reduction based on measured power (‘PRBMP’) functionality to Nicol’s system.” Pet. 45–46 (citing Petition Section XI.A.1). In particular, Petitioner contends that “a POSITA seeking to improve Nicol would have been motivated to consult Kling, which discusses well-known techniques of providing over-temperature protection, as well as additional improvements” such as detecting excessive power consumption to throttle back processors to reduce power consumption. Pet. 24–25. Petitioner further argues that a POSITA would have been motivated to implement measuring for excessive power consumption “and to reduce it, which is consistent with Nicol’s objective of minimizing power consumption.” *Id.* at 25 (citing Ex. 1001 ¶ 129).

Petitioner contends, and we agree, that Kling describes an implementation of PRBMP where a parameter that is approximately proportional to the consumed power, such as voltage, is tracked. *Id.* at 46 (citing Ex. 1010, 2:31–37). Petitioner further asserts, and we agree, that Kling describes an implementation of PRBMP where current consumed by a processor is tracked by measuring a voltage across a resistor of the processor. *Id.* (citing Ex. 1010, 3:57–59; Ex. 1001 ¶ 195). Petitioner argues, and we agree, that if the voltage exceeds a threshold, the controller sends a throttle signal to the processor to reduce its clock frequency, which reduces power consumption. *Id.* (citing Ex. 1010, 2:48–51; Ex. 1001 ¶ 196). Lastly, Petitioner contends, and we agree, that Kling discloses the design incentive of reducing a clock frequency based in part on a voltage in a processor, and

“a POSITA would have understood that PRBMP can also be implemented in Nicol’s system with a reasonable expectation of success to yield predictable results.” *Id.* (citing Ex. 1001 ¶ 197).

Patent Owner argues that a POSITA would have understood that the voltage measured in Kling is not the processor voltage (*e.g.*, the voltage between the processor (load) and ground), but is instead the voltage drop between the power supply and the processor. PO Resp. 45–46 (citing Ex. 2024 ¶ 69; Ex. 1010, code (57), Claims 16, 23). We disagree.

Kling describes measuring power consumed by at least a portion of a computer system. Ex. 1010, 2:31–35. “The portion of the computer system that is monitored may include one or more processors.” *Id.* at 2:37–38. Kling also describes that the power consumed by at least a portion of a computer system, such as the processors, is monitored by “measuring a parameter that is approximately proportional to the consumed power, *such as voltage.*” *Id.* at 2:31–35; *see also id.* at 4:54–58 (“the term ‘power’ includes either actual power or a value, such as current, voltage, duty cycle, or other measurement, that is proportional to power”). Kling further describes reducing the clock frequency when the power consumed by a processor reaches a threshold. *Id.* at 2:42–50.

We agree with Petitioner that such descriptions would have led a POSITA to understand that “Kling undisputedly teaches reducing clock frequency based on the power consumed by a processor; *the frequency reduction is based in part on processor voltage* because the power consumed by a processor is the product of its voltage and current ( $P = V \times I$ ), as was well-known in the art.” Pet. Reply 23 (citing Ex. 1055 ¶¶ 41–42). For all of these reasons, we find that Kling teaches a “clock frequency [that] is determined in part by processor voltage.”



Next, Patent Owner argues that “even assuming Kling’s throttling is based on the ‘processor voltage,’ a POSITA would not have a motivation to combine Kling with Nicol” because “Nicol already minimized the power consumption based on processing load and required completion time.” PO Resp. 46 (Ex. 2024 ¶ 70; Ex. 1009, code (57), 3:66–67). Patent Owner argues that a POSITA would have understood that a further reduction of clock frequency based on supply voltage would cause tasks not to finish on time, and, therefore, a POSITA would not have a reasonable expectation of success in combining Kling with Nicol. *Id.* at 46–47 (citing Ex. 2024 ¶¶ 70–71). Patent Owner also argues that “even if Kling’s power limit can be represented by a voltage limit, such voltage does not determine the clock frequency because the voltage limit would not be reached.” Sur-reply 17. Patent Owner’s arguments are misplaced. The Petition does not propose adding Kling to Nicol’s system to further reduce clock frequency based on supply voltage, as Patent Owner asserts. Rather, Petitioner proposes adding Kling’s functionality of power reduction based *on measured power* (‘PRBMP’) to Nicol’s system as an additional feature (detecting excessive power consumption to throttle back processors to reduce power consumption). Pet. 23–25 (cited at *id.* 45–46). We determine that a POSITA would have been motivated to implement Kling’s PRBMP functionality to detect excessive power consumption and reduce it, which is consistent with Nicol’s objective of minimizing power consumption. *Id.*; Ex. 1001 ¶ 129.

### *Claim 3*

Claim 3 depends from claim 1 and recites “wherein: said clock frequency is determined in part by available power.” Referencing its showing for claim 2, and the section of the Petition on combining Nicol and

Kling, Petitioner contends that “a POSITA would have found it obvious to add Kling’s power control functionality to Nicol’s system.” Pet. 47 (citing Petition Section XI.A.1, XI.A.3; Ex. 1001 ¶ 199).

Petitioner further asserts, and we agree, that Kling teaches measuring the power (based on the current or voltage across a resistor) of a processor and comparing the measured power against an upper limit threshold. *Id.* (citing Ex. 1010, Fig. 2A; Ex. 1001 ¶ 200). Petitioner contends that if the measured power reaches the upper limit, the controller sends a throttle signal so the processor to reduce clock frequency to reduce power consumption. *Id.* at 48 (citing Ex. 1010, 5:38–40, 2:48–51). Petitioner contends that adding Kling’s functionality “involves relatively simple add-on software to Nicol’s more complex task scheduler software residing in the controller.” *Id.* (citing Ex. 1001 ¶¶ 205–206).

Patent Owner argues that “Kling is not limited by available power” but “is limited by a self-imposed safety measure.” PO Resp. 48 (citing Ex. 2024 ¶ 73). Petitioner responds that such an argument is “inapposite” as Kling clearly teaches “an available power limit that, when exceeded, would trigger frequency reduction.” Pet. Reply (citing Pet. 49; Ex. 1055 ¶ 46). We agree with Petitioner. In particular, Kling describes the upper threshold of the power controller is set to an upper limit and is a constant value. Ex. 1010, 5:14–21. The constant value “may be associated with an *approximately maximum power that can be reliably consumed by the computer system* from a power outlet into which the system is plugged before the outlet’s fuse or circuit breaker trips.” *Id.* at 5:21–25. We find that the maximum power that can be reliably consumed to be “available power,” no matter from where that power comes, *e.g.*, an outlet that contains fuses or circuit breaker. Dr. Mangione-Smith does not explain why the

source of the power matters or why a source of power that is limited is still not “available power.” Ex. 2024 ¶ 73. Moreover, we agree with Petitioner that Dr. Mangione-Smith acknowledged that “Kling teaches reducing frequency when an available power limit is reached.” Pet. Reply 24–25 (citing Ex. 1051, 149:12–150:2).

Patent Owner further argues that claim 1 “describes a dynamically changing clock frequency,” and that the same frequency recited in claim 3 must be determined, in part, by the available power. PO Resp. 48–49. Patent Owner additionally argues that “Petitioner points to a static upper voltage limit as the available power upon which the clock frequency depends, but if the amount of available power is static and doesn’t change, it cannot determine all of these frequencies, which can vary during operation. *Id.* at 49 (citing Pet. 47; Ex. 2024 ¶ 74). Patent Owner’s argument is not commensurate in scope with what is claimed, and we agree with Petitioner that claim 3 does not require determining “all” frequencies based on available power. Pet. Reply 25; Sur-reply 18. Moreover, we are not persuaded by Patent Owner’s argument that it would be too difficult to combine the teachings of Nicol and Kling into a system for similar reasons we have addressed above with respect to claims 1 and 2. Again, Petitioner proposes adding Kling’s power reduction based *on measured power* (‘PRBMP’) functionality to Nicol’s system as an additional feature (detecting excessive power consumption to throttle back processors to reduce power consumption). Pet. 23–25 (cited at *id.* 45–46). We determine that a POSITA would have been motivated to implement Kling’s PRBMP functionality to detect excessive power consumption and reduce it, which is consistent with Nicol’s objective of minimizing power consumption. *Id.*; Ex. 1001 ¶ 129.

*Claim 4*

Claim 4 depends from claim 1 and recites “wherein: said clock frequency is determined in part by a user setting.” Referencing its showing for claims 2, 3, and the section of the Petition on combining Nicol and Kling, Petitioner contends that “a POSITA would have found it obvious to add Kling’s power control functionality to Nicol’s system.” Pet. 48 (citing Petition Section XI.A.1, XI.A.3, XI.A.4; Ex. 1001 ¶ 208). Petitioner contends, and we agree, that Kling teaches measuring power of a processor and comparing the measured power against “an ‘upper limit’ threshold as well as a ‘lower limit’ threshold.” *Id.* (citing Ex. 1010, Fig. 2A). Petitioner contends, and we agree, that “[t]he thresholds are user settings.” *Id.* (citing Ex. 1010, 5:57–59). Petitioner further contends, and we agree, that if the measured power reaches the upper limit, the controller sends a throttle signal to the processor to instruct it to reduce its clock frequency to reduce power consumption.” *Id.* at 50 (citing Ex. 1010, 5:38–40, 2:48–51; Ex. 1001 ¶ 211). Petitioner asserts that in the system, “the clock frequency is determined in part by user settings, *e.g.*, the upper and lower power limits.” *Id.* (citing Ex. 1001 ¶ 213).

Patent Owner argues that Petitioner only refers to Kling’s lower threshold as being modifiable by a user, but “the frequency does not depend on a lower threshold” only an “upper threshold, which causes throttling, or normal operating conditions which sets a high core frequency.” PO Resp. 49–50 (citing Pet. 49; Ex. 2024 ¶ 76; Ex. 1010, 8:43–45, 10:10–13). We agree with Petitioner, however, that the Petition asserts that Kling describes that *both* the upper limit threshold and lower limit threshold are user settings (“[t]he thresholds [upper limit threshold and lower limit threshold] are user

settings”). Pet. 49.<sup>20</sup> Indeed, Kling describes that the upper threshold “may be modifiable by the system designer or system user.” Ex. 1010, 5:16–19. And as pointed out by Petitioner, Dr. Mangione-Smith acknowledged that both Kling’s upper and lower threshold may both be set by a user setting. Pet. Reply 25 (citing Ex. 1051, 152:17–22).

*Claim 5*

Claim 5 depends from claim 1 and recites “wherein: said clock frequency is determined in part by available power and a user setting.” Petitioner, referring back to its showings for claims 3 and 4, argues that Nicol in combination with Kling meets the claim 5 limitation. Pet. 50 (citing XI.A.4, XI.A.5; Ex. 1001 ¶¶ 215–216).

Patent Owner references the arguments Patent Owner made for claims 3 and 4 and states that for at least the same reasons, Petitioner has failed to show that Nicol and Kling disclose the elements of claim 5. PO Resp. 50 (citing Ex. 2024 ¶ 77). As explained above, we are not persuaded by Patent Owner’s arguments regarding claims 3 and 4. Next, Patent Owner argues that “Petitioner’s arguments with respect to each of these elements [available power and a user setting] fail[] to detail a situation in which a clock frequency is dependent on both these elements” because “according to Petitioner’s analysis, the clock frequency depends on available power OR a user setting.” *Id.* We disagree that Petitioner’s analysis depends on showing available power or a user setting. Rather, we understand the Petition to assert that Kling teaches both in its system. Pet. 50. We agree with Petitioner that “Kling teaches reducing clock frequency when an available

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<sup>20</sup> We disagree with Patent Owner that this is a new argument, because Petitioner all along contended that Kling describes user settings for both the upper and lower limit thresholds. Sur-reply 22.

power limit is reached, *and* the limit is determined by user settings.” Pet. Reply 26 (citing Pet. 49–50; Ex. 1010, 2:31–51, 5:16–19; Ex. 1055 ¶¶ 51–53).

*Claim 6*

Claim 6 depends from claim 1 and recites “wherein: said number of pending operations is determined at by the fill level of one or more buffers.” Petitioner contends that “Nicol renders obvious this claim element.” Pet. 51 (citing Ex. 1001 ¶ 217). Petitioner contends, and we agree, that Nicol teaches estimating processing loads based on the number of instructions of each of the “to do” tasks to be allocated to the PEs. *Id.* (citing Ex. 1009, 3:13–18). Petitioner contends that a “POSITA would have understood that the instructions that need to be executed are stored in an instruction queue or buffer, and that the fill level of the buffer corresponds to the number of instructions.” *Id.* (citing Ex. 1001 ¶ 219; Ex. 1022, 155, Fig. 3.11). Petitioner asserts that “during prosecution of the ’605 patent” the applicant stated that “one of ordinary skill in the art would understand that ***the fill level of a data buffer [is] representative of the number of waiting operations or processor load.***” *Id.* (citing Ex. 1004, 377). Petitioner contends that a POSITA would have known that Nicol detects the number of pending operations of the PEs by inspecting the fill level of buffers and that it was further known that the number of pending operations could be determined by monitoring queues, such as the fill level of buffers that feed work to the processors. *Id.* at 51–52 (citing Ex. 1001 ¶¶ 222–223; Ex. 1017, 1704; Ex. 1018, 4:57–60).

Patent Owner argues that Petitioner has failed to account sufficiently for how the number of instructions of pending operations is determined by the fill level and that “Nicol simply does not disclose any particular way to

determine the number of instructions.” PO Resp. 52 (citing Ex. 2024 ¶ 79). Patent Owner further argues that a “POSITA would not have understood that processor loads or number of pending operations are necessarily determined through the buffer fill level.” *Id.* at 53 (citing Ex. 2024 ¶ 80). Patent Owner contends that although Petitioner relies on Cline and Hong to show that inspecting the fill level of buffers was well known, “Ppetitioner provides no analysis as to a POSITA’s motivation to apply such knowledge to Nicol and any expectation of success of such application.” *Id.* (citing Ex. 2024 ¶ 81).

Patent Owner’s arguments are unavailing. First, Petitioner does not rely on Nicol alone to teach the disputed claim limitation. Rather, Petitioner relies on Nicol *in light of the POSITA’s knowledge* at the time of the invention. Pet. 51–52. It is not disputed that Nicol describes the number of instructions waiting to be executed (“number of pending operations”). Ex. 2024 ¶ 79; Ex. 1009, 3:13–18. It also is not disputed that a POSITA knew how to determine the number of pending operations by monitoring buffer fill levels. Ex. 1018, 54:57–60; Ex. 1017, 1704; Ex. 2024 ¶ 81. We determine that it would have been obvious to determine the number of instructions (“pending operations”) by monitoring the fill level of one or more buffers as claimed. Ex. 1001 ¶¶ 222–223

In the Sur-reply, Patent Owner argues that the “number of instructions” or pending operations in Nicol cannot determine the “number of pending operations of each individual processor.” Sur-reply 20. Claim 6 does not recite the number of pending operations “of each individual processor.” Accordingly, Patent Owner’s argument is not commensurate in scope to what is claimed. Moreover, as pointed out by Petitioner, during prosecution of the involved patent, applicant stated that “one of ordinary skill in the art would understand that *the fill level of a data buffer [is]*

*representative of the number of waiting operations or processor load.”*

Ex. 1004, 377. Thus, we do not agree that the pending operations or instructions are not for the individual processors.

*E. Remaining Grounds Challenging Claims 1–6*

Petitioner has withdrawn the remaining challenges in the Petition. Pet. Reply 27 (“Petitioner hereby withdraws Grounds II and III); Sur-reply 1 (“Petitioner withdrew Grounds II and III . . . . Corresponding arguments should not be considered”). Accordingly, we need not and do not consider the remaining challenges.

III. CONCLUSION<sup>21</sup>

For the foregoing reasons, we determine that Petitioner has shown by a preponderance of the evidence that claims 1–6 of the ’605 patent are unpatentable, as summarized in the following table:

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<sup>21</sup> Should Patent Owner wish to pursue amendment of the challenged claims in a reissue or reexamination proceeding subsequent to the issuance of this Decision, we draw Patent Owner’s attention to the April 2019 *Notice Regarding Options for Amendments by Patent Owner Through Reissue or Reexamination During a Pending AIA Trial Proceeding*. See 84 Fed. Reg. 16654 (Apr. 22, 2019). If Patent Owner chooses to file a reissue application or a request for reexamination of the challenged patent, we remind Patent Owner of its continuing obligation to notify the Board of any such related matters in updated mandatory notices. See 37 C.F.R. § 42.8(a)(3), (b)(2).



<b>Claims</b>	<b>35 U.S.C. §</b>	<b>Reference(s) /Basis</b>	<b>Claims Shown Unpatentable</b>	<b>Claims Not Shown Unpatentable</b>
1–6	103(a) <sup>22</sup>	Nicol, Kling	1–6	
1–6	103(a)	Nicol, Kling, DeHon	Challenge withdrawn	
1–6	103(a)	Nicol, Kling, DeHon, Bhatia	Challenge withdrawn	
<b>Overall Outcome</b>			1–6	

#### IV. ORDER

Accordingly, it is:

ORDERED that claims 1–6 of the '605 patent have been shown to be unpatentable; and

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the Decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

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<sup>22</sup> As explained immediately above, we need not and do not decide whether Petitioner has shown by a preponderance of the evidence that claims 1–6 also would have been obvious based on the remaining grounds not addressed in this Decision.

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