UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

INTEL CORPORATION,
Petitioner

v.

PACT XPP SCHWEIZ AG,
Patent Owner

Case IPR2020-00541
U.S. Patent No. 9,075,605

PATENT OWNER'S PRELIMINARY RESPONSE PURSUANT TO 35 U.S.C. § 313 AND 37 C.F.R. § 42.107

TABLE OF CONTENTS

Page

TABLE OF AUTHORITIES

Page

Cases

Statutory Authorities

Rules and Regulations

Additional Authorities

EXHIBIT LIST

Exhibit No.	Description
2001	Certified translation of Commercial Register showing the change of name of Scientia Sol Mentis AG to PACT XPP Schweiz AG
2002	Excerpts of the complaint in *PACT XPP Schweiz AG v. Intel Corporation*, No. 19-cv-267 (D. Del.).
2003	Proof of service of *PACT XPP Schweiz AG v. Intel Corporation*, No. 19-cv-267 (D. Del.).
2004	Notice of dismissal of *PACT XPP Schweiz AG v. Intel Corporation*, No. 19-cv-267 (D. Del.).
2005	The Scheduling Order in *PACT XPP Schweiz AG v. Intel Corporation*, No. 19-cv-1006 (D. Del.).
2006	Order Extending Time
2007	Docket summary of *PACT XPP Schweiz AG v. Intel Corporation*, No. 19-cv-1006 (D. Del.).
2008	PACT's Letter Regarding Claim Narrowing and Swapping
2009	Excerpts of Petitioner's invalidity contentions in the District Court case
2010	Petitioner's complaint in *Intel Corporation v. PACT XPP Schweiz AG*, No. 19-cv-2241 (N.D. Cal. April 25, 2019)

I. INTRODUCTION

Petitioner fails to establish a reasonable likelihood that two separate limitations of claim 1 are found or rendered obvious in the prior art, which dooms the petition on all of the challenged claims. As Petitioner relies on Nicol as its primary reference, and Nicol is included on all 3 asserted grounds, Petitioner's failure on these two limitations also dooms all of the asserted grounds.

First, Petitioner fails fundamentally on showing setting a clock frequency to a maximum, and mistakenly cites disclosures in Nicol establishing a lower bound on the clock frequency. The disclosure Petitioner relies on in Nicol "adjust[s] the clock frequency to insure that the most heavily loaded PE carries out its assigned task within the required completion time." But this describes a lower bound, as clock frequencies higher than this will also allow the most heavily loaded PE to carry out its assigned task within the required completion time (in fact, the task would be finished faster at higher frequencies). Because of this alone, all grounds on all claims should be denied.

Petitioner also fails to establish a motivation to combine the prior art references it relies on, including Nicol, Kling, DeHon and Bhatia, which all deal with different aspects of processor systems. Petitioner's overbroad descriptions of the technology does not establish a motivation to combine these disparate references,

and Petitioner further fails to show how such a combined system would work or that there is any reasonable expectation of success for the combined system.

The Petition should be denied under 35 U.S.C. § 314(a) because the validity of the '605 patent may be considered in a jury trial before the Board's final decision. In addition, the Petition is barred under 35 U.S.C. §315(a) because Petitioner previously challenged validity in a district court case before the filing of the Petition. *Cisco Systems, Inc. v. Chrimar Systems, Inc.*, Case IPR2018-01511, Paper 11 (Jan. 31, 2019) (Precedential) (denying institution under AIA § 315(a)(1)). As such, the Board should deny institution.

II. OVERVIEW OF THE '605 PATENT

A. The '605 Patent Specification

The '605 patent includes 6 claims, and Petitioner challenges all 6 claims. Only claim 1 is independent and all of claims 2-6 depend on claim 1. Independent claim 1 is reproduced below:

> 1. A method for operating a multiprocessor system comprising a plurality of data processing cells, each of the plurality of data processing units (a) including at least one Arithmetic Logic Unit (ALU) and a register unit and (b) being adapted for sequentially processing data, the method comprising:
> <u>the multiprocessor system setting a clock frequency, of at least a part of the multiprocessor system to a minimum in accordance with a number of pending operations of a first processor</u>;

the multiprocessor system subsequently increasing the clock frequency of the at least the part of the multiprocessor system to a maximum in accordance with a number of pending operations of a second processor; and

the multiprocessor system subsequently reducing the clock frequency of the at least the part of the multiprocessor system in accordance with (a) an operating temperature threshold preventing over-temperature and (b) a hysteresis characteristic.

Ex. 1003 ('605 patent) claim 1 (emphasis added for claim elements discussed in this response).

III. OVERVIEW OF THE ASSERTED PRIOR ART

Petitioner relies on four separate references, as summarized below.

A. Nicol (U.S. Patent No. 6,141,762)

Nicol (U.S. Patent No. 6,141,762) is entitled "Power Reduction in a Multiprocessor Digital Signal Processor Based on Processor Load," was filed August 3, 1998 and issued on October 31, 2000. Nicol describes a "[i]mproved operation of multi-processor chips," using a technique where "[a] controller in a multi-processor chip allocates tasks to the individual processors to equalize processing load among the chips, then the controller lowers the clock frequency on the chip to as low a level as possible." Ex. 1009 (Nicol) at 2:22-26.

In Figure 2, Nicol discloses an embodiment ("Figure 2 embodiment") with multiple processing entities (PEs) powered by one voltage supply V_{dd}-local, and

driven by one reference clock 101. In this case, Nicol manages power consumption by equalizing the processing load among the chips first, and then afterwards, lowers the clock frequency as low as possible. The idea behind the strategy of equalizing load first is to prevent a bottleneck where one processor may take longer than the other processors. *See, e.g.,* Ex. 1009 (Nicol) at 3:18-20 ("The intermediate goal, of course, is to maximize the parallelism and to evenly distribute the load presented to the Fig. 2 system among all of the PE's."). This strategy makes sense when all of the processors are controlled by a common power supply and operated at a common frequency.

In Figure 4, Nicol discloses a separate embodiment with multiple PEs, each powered by its own voltage supply. Nicol describes this embodiment as useful when tasks cannot be divided into evenly loaded threads. *See, e.g.,* Ex. 1009 (Nicol) at 5:60-6:3 ("In some applications, however, one may encounter tasks that cannot be partitioned into concurrent evenly-loaded threads and, therefore, some PE within the multiprocessor would require a higher operating frequency and a higher operating voltage… A separate power supply for each PE in a chip overcomes this limitation by allowing the operating system to independently program the lowest operating frequency and corresponding lowest supply voltage for each PE. The architecture for such an arrangement is shown in Fig. 4.").

B. Kling (U.S. Patent No. 6,367,023)

Kling (U.S. Patent No. 6,367,023) describes a system to manage power consumed in a computer system by measuring electrical parameters, such as voltage, current or duty cycle of a power supply and determining if power consumption has reached a threshold. Kling does not discuss load balancing or setting clock frequencies of different processors to different values.

C. DeHon (U.S. Patent 6,052,773)

DeHon (U.S. Patent No. 6,052,773) describes a programmable gate array which enables application-specific configurations. DeHon does not describe power management through clock frequency adjustments.

D. Bhatia (U.S. Patent No. 6,535,798)

Bhatia (U.S. Patent No. 6,535,798) describes a thermal management system based on two levels, HP (high performance) and LP (low performance). The system manages power by switching between the two levels based on temperature measurements. Bhatia does not describe load or task balancing.

IV. OVERVIEW OF THE INVALIDITY THEORIES IN THE PETITION

Petitioner's invalidity theories include three grounds. Ground I relies on Nicol in combination with Kling and Petitioner alleges that claims 1-6 are invalid under Ground I. Petitioner relies on Kling because Nicol does not teach an over-temperature threshold or temperature sensors. Under Ground II, Petitioner adds

DeHon to address Petitioner's claim construction that "data processing unit" and/or "data processing unit … adapted for sequentially processing data" means "reconfigurable and sequential data processors where the data results from one processor are fed to another, for each processor to perform a separate computation," and alleges that claims 1-6 are obvious in view of Nicol in combination with Kling and DeHon under Petitioner's claim constructions. Petitioner only addresses the limitations "and (b) being adapted for sequentially processing data, the method comprising" and "the multiprocessor system setting a clock frequency, of at least a part of the multiprocessor system to a minimum in accordance with a number of pending operations of a first processor;" under Ground II, and relies on the assertions under Ground I for the others. Under Ground III, Petitioner adds Bhatia to address Petitioner's claim construction of "to a minimum" and alleges that claims 1-6 are obvious in view of Nicol in combination with Kling, DeHon and Bhatia under Petitioner's claim constructions. Petitioner only addresses the limitation "the multiprocessor system setting a clock frequency, of at least a part of the multiprocessor system to a minimum in accordance with a number of pending operations of a first processor;" under Ground III, and states that the "only difference" as compared with Ground II is the explicit combination with Bhatia. Petitioner relies on the assertions under Ground I for the other limitations.

Because Petitioner fails to establish the disclosure of certain elements in claim 1, all of Petitioner's grounds fail.

V. THE PETITION FAILS TO DEMONSTRATE A REASONABLE LIKELIHOOD THAT ANY CLAIM IS INVALID BASED ON NICOL IN VIEW OF KLING (GROUND I)

The Petition should be denied and no review instituted. The '605 patent includes only one challenged independent claims: Claim 1. Petitioner fails to demonstrate a reasonable likelihood that this claim is invalid for at least the following reasons. Since all of the dependent claims 2-6 depend on Claim 1, Petitioner also fails to demonstrate a reasonable likelihood that claims 2-6 are invalid for the same reasons.

A. Petitioner Fails To Show Any Disclosure Of "the multiprocessor system subsequently increasing the clock frequency of the at least the part of the multiprocessor system to a maximum in accordance with a number of pending operations of a second processor" (Claim 1)

Petitioner fails to show this limitation is disclosed or rendered obvious as the Petition relies on a disclosure in Nicol that sets a ***lower bound*** for the clock frequency, which cannot be a "maximum" clock frequency as required by this claim limitation. This is a fundamental and fatal error which dooms all claims and grounds in the Petition, as this limitation appears in independent claim 1, and Nicol is the only reference relied upon by Petitioner for this limitation, across all grounds. For this reason alone, the Petition should be denied.

Specifically, Petitioner points to 3:66-4:5, which discloses that Nicol "needs to ascertain the required completion time [of the tasks], divide the collection of tasks as evenly as possible (in terms of needed processing time), consider the PE with the tasks that require the most time to carry out, and adjust the clock frequency [common to all PEs] to insure that the most heavily loaded PE carries out its assigned task within the required completion time."). Petitioner relies on this passage to attempt to show that "the controller takes into account the number of pending instructions for each PE – including PE1 ('first processor') and PE2 ('second processor') – because it sets the frequency based on identifying the processing requirement of 'the most heavily loaded PE.'" Pet. at 40.

But the frequency referenced here, set to insure that the most heavily loaded PE carries out its assigned task within the required completion time, ***is not a maximum frequency***. The requirement that the most heavily loaded PE must carry out its task within a set time period in fact determines ***a lower bound for the frequency*** that must be used for that PE. If that PE ran at a higher frequency and finished earlier, that would still meet the requirement of completing the assigned tasks within the required completion time. The disclosure in Nicol Petitioner points to does not demonstrate or render obvious the limitation in the '605 patent, which requires increasing the clock frequency to a maximum in accordance with the number of pending operations of a second processor. In fact, in the sentence that

immediately follows this cited passage, Nicol states: "Once the frequency is thus determined, a ***minimum*** supply voltage can be determined." Ex. 1009 (Nicol) at 4:5-6 (emphasis added). This is further support that what is referenced here in Nicol is a minimum, ***not a maximum***, as higher supply voltages are needed for higher frequencies, and lower supply voltages can be used for lower frequencies. Disclosure of a minimum frequency does not render obvious a maximum frequency as the reasons for running a processor at a minimum frequency (*e.g.,* to save power) are different for running a processor at a maximum frequency (*e.g.,* to maximize performance).

Petitioner next points to Figure 3, and describes a sequence of "increasing the clock frequency of the PEs of the multiprocessor system from 70 MHz (minimum clock frequency) to 140 MHz (maximum clock frequency) prior to the execution of a high load" (Pet. at 40-41) and cites to 3:31-33, 4:54-62 and 5:23-28 of Ex. 1009 (Nicol). However, none of these passages in Nicol describes a maximum frequency in accordance with the number of pending operations of a second processor. The disclosure at 3:31-33 reads:

> To illustrate, if a given application that is executed on 1 PE requires operating the PE at 140 MHz, it is known from FIG. 1 that the PE can be operated at approximately a 2.7V supply.

Ex. 1009 (Nicol) at 3:31-33. This passage simply describes the required voltage for the power supply to operate the PE at 140 MHz and does not mention either a maximum frequency or a number of pending operations.

The next cited passage at 4:54-62 reads:

> FIG. 3 demonstrates the timing associated with increasing Clk, Clk-L and Vdd -local when a new task is created and the load on the multiprocessor is thus increased, and the timing associated with decreasing Clk, Clk-L and Vdd -local when the load on the multiprocessor is decreased. Specifically, it shows the system operating at 70 MHz from a 1.8V supply when the load is increased in three steps to 140 MHz. When the 2.7V supply is stable, as shown by the supply voltage plot, the new task is enabled for execution.

Ex. 1009 (Nicol) at 4:54-62. This passage describes Figure 3, which illustrates the timing and steps used to increase the clock frequency and voltage supply when a new task is created, which increases the load. Nothing here describes a maximum frequency, and nothing here mentions the number of pending operations. The passage simply says the creation of a new task will increase the load.

The next cited passage at 5:23-28 reads:

> The FIG. 2 system uses the operating system to react to variations in the system load. As more tasks are entered into the "to-do" list, the operating system of PE 100 computes the correct way to balance the additional computational requirements and allocates the tasks to the processors. It then computes the required operating frequency.

Ex. 1009 (Nicol) at 5:23-28. This portion describes how the operating system can react to variations in system load, and describes how the system balances

computational requirements and allocates tasks among the processors. The reallocation of tasks and balancing computational requirements does not result in a change in frequency. It is only after the balancing and allocation is done (note the use of the word "then") that a required operating frequency is computed. Furthermore, the disclosed "required operating frequency" is a minimum frequency (as described above, a higher frequency would still allow completion within the required time), not a maximum, so this passage also does not disclose setting clock frequency to a maximum.

Lastly, Petitioner points to two citations where the word "maximum" or "maximally" is used in Nicol, but these are separate passages from those cited above and not tied to the number of pending operations. The first citation is part of a sentence which reads in full:

> Thus, in a sense it is the expected completion time for the collection of assigned tasks that is controlling, and the reduction of frequency from the maximum that the chip can support may be controlled by the division of tasks that may be accomplished.

Ex. 1009 (Nicol) at 3:61-65. The Petition only quotes the portion: "maximum that the chip can support." The disclosure in Nicol is again talking about the expected completion time that controls the clock frequency, which is a similar idea to that described above, and represents a lower bound for the frequency. Furthermore, the language which is not quoted in the Petition makes clear that in fact there is a

reduction in frequency from the maximum that the chip can support, which makes clear that the setting of the frequency is in fact not the maximum that Petitioner points to. Furthermore, the phrase itself "maximum that the chip can support" suggests on its face that this maximum is not determined in accordance with a number of pending operations, but based on limitations of the chip. Indeed, Nicol states: "a requirement for when the tasks are to be finished might not be related might not be related to the highest operating frequency of the chip." Ex. 1009 (Nicol) at 3:51-53.

The other quoted disclosure is:

> For a maximally utilized system, all of the available processors ought to be operating at full speed when satisfying the maximum load encountered by the system. At such a time, the power consumption of the multiprocessor chip is at its maximum level. However, as the load requirements are lowered, the system should, advantageously, reduce its power consumption.

Ex. 1009 (Nicol) at 2:65-3:4. The context of this statement is that it appears at the beginning of the Detailed Description and serves as an introduction only. There is no connection of this statement with the rest of the embodiments disclosed and relied upon by the Petitioner. This is a general statement about running all available processors at full speed when a maximally utilized system encounters maximum load, but not about how the system in Nicol functions. In fact, the last sentence in this passage suggests that one should not run the system at this maximum level. And

the next few sentences following this excerpt make clear that the advantages of Nicol are gained by not running in this maximal state. *See, e.g.,* Ex. 1009 (Nicol) at 3:4-9 ("It may be noted that, typically, computers spend 99% of their time waiting for a user to press a key. This presents a great opportunity to drastically reduce the average power consumption. The specific approach by which the system 'scales back' its performance can greatly impact the realizable power savings."). Lastly, the claim requires a maximum in accordance with "the number of pending operations of a second processor," which is not disclosed or suggested here, since the statement quoted here is about the system as a whole.

Petitioner's failure to establish a reasonable likelihood that this limitation is disclosed or rendered obvious alone is enough to deny the Petition, as this limitation appears in independent claim 1 and therefore impacts all claims 1-6, including dependent claims 2-6. Since Petitioner's showing relates to Nicol, which is part of all asserted grounds, this also affects all grounds in the Petition. Petitioner's failure to establish a reasonable likelihood on this limitation alone is sufficient grounds, by itself, to deny the entire Petition.

B. Petitioner Fails To Show Any Disclosure Of "the multiprocessor system setting a clock frequency of at least a part of the multiprocessor system to a minimum in accordance with a number of pending operations of a first processor" (Claim 1)

Petitioner points to 2:23-27 and annotates the quote as follows:

> Nicol explains that the controller "allocates tasks to the individual processors [PEs, including PE1] to equalize processing load among the [PEs, including PE1], then the controller lowers the clock frequency on the chip to as low a level as possible while assuring proper operation, and finally reduces the supply voltage." Ex. 1009, 2:23-27.

Pet. at 36. Petitioner uses square brackets in two places with identical content, but in two separate ways. The first square bracket is Petitioner's interpretation of the term "individual processors," but the second square bracket actually replaces a missing word from the quote, "chips." Petitioner provides no explanation why it equates both "individual processors" and "chips" to "PEs, including PE1." Changing the words of the cited reference without explanation, especially when different words are being interpreted, does not demonstrate why the reference Nicol discloses or renders obvious this claim interpretation.

Second, this passage discloses a 2-step process, and Petitioner fails to show that the clock frequency reduction is in accordance with a number of pending operations of a first processor. The first step here is load balancing which is based on the load across all of the PEs, and not based on the load on any single processor. The purpose is to equalize the load across all PEs. It is only in the second step that the clock frequency is then lowered. The additional citation in the Petition to Nicol at 3:13-18 makes clear that the number of instructions is used in the first step of allocating tasks. A fuller excerpt of this excerpt from Nicol is provided below:

> If the number of instructions that need to be executed for each task is known and made available to the operating system, a scheduler within the operating system can use this information to determine the best way to allocate the tasks to the available processors in order to balance the computation. The intermediate goal, of course, is to maximize the parallelism and to evenly distribute the load presented to the FIG. 2 system among all of the PE's.

Ex. 1009 (Nicol) at 3:13-21. This passage makes clear that the number of instructions is used in the step of allocating tasks among the available processors. This step is to achieve load balancing, and to try to evenly distribute the load in the Fig. 2 system. This passage does not even mention changing the clock frequency. Petitioner has failed to show how the clock frequency is related to the number of instructions.

Petitioner next points to Figure 3 as support for setting the clock frequency of the multi-processor to a minimum, and cites to 3:31-33, 4:54-62 and 5:23-28 of Nicol for support. These are the same citations Petitioner uses for the other limitation "the multiprocessor system subsequently increasing the clock frequency … to a maximum." But none of these show setting the clock frequency to a minimum in accordance with a number of pending operations of a first processor. Figure 3, as annotated by the Petitioner, simply shows increase and decrease of frequency and voltage per task, not based on the number of pending operations.

The disclosure at 3:31-33 reads:

> To illustrate, if a given application that is executed on 1 PE requires operating the PE at 140 MHz, it is known from FIG. 1 that the PE can be operated at approximately a 2.7V supply.

Ex. 1009 (Nicol) at 3:31-33. This passage simply describes the required voltage for the power supply to operate the PE at 140 MHz and does not mention either a minimum frequency or a number of pending operations.

The passage at 4:54-62 reads:

> FIG. 3 demonstrates the timing associated with increasing Clk, Clk-L and Vdd -local when a new task is created and the load on the multiprocessor is thus increased, and the timing associated with decreasing Clk, Clk-L and Vdd -local when the load on the multiprocessor is decreased. Specifically, it shows the system operating at 70 MHz from a 1.8V supply when the load is increased in three steps to 140 MHz. When the 2.7V supply is stable, as shown by the supply voltage plot, the new task is enabled for execution.

Ex. 1009 (Nicol) at 4:54-62. This passage describes Figure 3, which illustrates the timing and steps used to increase the clock frequency and voltage supply when a new task is created, which increases the load. Nothing here describes a maximum frequency, and nothing here mentions the number of pending operations. The passage simply says the creation of a new task will increase the load.

The passage at 5:23-28 reads:

> The FIG. 2 system uses the operating system to react to variations in the system load. As more tasks are entered into the "to-do" list, the operating system of PE 100 computes the correct way to balance the additional computational requirements and allocates the tasks to the processors. It then computes the required operating frequency.

Ex. 1009 (Nicol) at 5:23-28. This portion describes how the operating system can react to variations in system load, and describes how the system balances computational requirements and allocates tasks among the processors. Petitioner has failed to show how the reallocation of tasks and balancing computational requirements results in a change in frequency. As with the first passage described above in this section (Nicol at 2:23-27), this describes only the first step of load balancing and not an adjustment of the clock frequency.

Under Grounds II and III, Petitioner references the Advanced Configuration and Power Interface (ACPI) industry specification and Bhatia to address Petitioner's claim construction of "to a minimum," but nothing in those sections addresses the issues with Nicol raised above.

Petitioner's failure to establish a reasonable likelihood that this limitation is disclosed or rendered obvious alone is enough to deny the Petition, as this limitation appears in independent claim 1 and therefore impacts all claims 1-6, including dependent claims 2-6. Since Petitioner's showing relates to Nicol, which is part of all asserted grounds, this also affects all grounds in the Petition. Petitioner's failure to establish a reasonable likelihood on this limitation alone is sufficient grounds, by itself, to deny the entire Petition.

VI. PETITIONER FAILS TO ESTABLISH A MOTIVATION TO COMBINE NICOL, KLING, DEHON AND BHATIA

Petitioner fails to establish a motivation to combine any of the 4 disparate references asserted in the 3 grounds in the Petition. Because the 4 references describe different aspects of technology, Petitioner is forced to rely on broad characterizations of the references in order to find commonalities. Such an approach fails to establish a motivation to combine the prior art in the way claimed by the '605. *See Johns Manville Corp. v. Knauf Insulation, Inc.*, Case IPR2018-00827, Paper 9 at 10 (Oct. 16, 2018) (Informative) ("a broad characterization of [prior art references] as both falling within the same alleged field . . . without more, is not enough for [Petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness conclusion.") (citing *Securus Techs., Inc. v. Global Tel*Link Corp.*, 701 F. App'x 971, 977 (Fed. Cir. 2017)). Furthermore, Petitioner describes the proposed combined system in high level terms, without adequately addressing the differences between the systems and how they would be integrated, and why such an integrated system would work. Without such details, Petitioner fails to establish a reasonable expectation of success by combining these references.

A. Petitioner Fails To Establish That A POSITA Would Be Motivated to Combine Nicol With Kling

Petitioner sets forth three reasons a POSITA would have been motivated to combine Nicol with Kling. None of these establish that "a person of ordinary skill

in the art would have been motivated to combine the prior art in the way claimed by the … patent claims at issue and had a reasonable expectation of success in doing so." *Personal Web Techs. v. Apple, Inc.*, 848 F.3d 987, 991 (Fed. Cir. 2017).

First, Petitioner states both Nicol and Kling are directed to "interrelated thermal and power management aspects that are critical and ubiquitous in processor-based systems." Petition at 23. Petitioner offers no explanation of this statement, and only cites the title of Nicol, and one sentence in Kling broadly discussing computer systems and power consumption. Petitioner also cites a third reference Bhatia, with no explanation how the one sentence in Bhatia, which broadly mentions power and thermal management techniques, is relevant to a motivation to combine Nicol with Kling. Such broad generalizations describing Nicol and Kling and such broad characterizations of the field do not motivate a POSITA to combine Nicol and Kling. *See Johns Manville Corp. v. Knauf Insulation, Inc.*, Case IPR2018-00827, Paper 9 at 10 (Oct. 16, 2018) (Informative) ("a broad characterization of [prior art references] as both falling within the same alleged field . . . without more, is not enough for [Petitioner] to meet its burden of presenting a sufficient rationale to support an obviousness conclusion.") (citing *Securus Techs., Inc. v. Global Tel*Link Corp.*, 701 F. App'x 971, 977 (Fed. Cir. 2017)). Nothing in these statements discuss Nicol or Kling, and the broad characterizations of how Nicol and Kling overlap in subject matter would apply to a large number of other references and provide no

motivation why a POSITA would combine these two references, as opposed to any other references in the broadly described subject area. As described earlier, Nicol is focused on managing power consumption through load balancing, while Kling focuses on managing power management through monitoring of electrical parameters. These are different approaches.

Second, Petitioner further claims both describe "the same flexible and distributed multiprocessor architecture in which processors have their own power supplies and in which software residing in a controller is programmed to selectively control the power consumption of each processor, notably by dynamically adjusting the processor's clock frequency during operation." *Id*. But Petitioner has not shown in what way Nicol and Kling use the same architecture. Petitioner makes no attempt to compare any of the figures in Nicol and Kling and explain why they depict the same architecture. Petitioner points out they both have power supplies, and frequency management and multiple processors, which are susceptible to the same criticisms mentioned above. Petitioner proposes that Nicol's controller can be programmed with Kling's software functionalities, but other than a conclusory statement saying it would yield predictable results, offers no explanation how it could be done. Nicol describes a hardware-based system and Petitioner does not explain why controller software in Kling can simply be used in Nicol, as Petitioner admits that Kling's software uses different sensor inputs. Petitioner only states a

conclusion that the software differences are not material without explanation. Petitioner has failed "to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does." *KSR Intern. Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007). Petitioner has not established that a person of ordinary skill would have a reasonable expectation of success in combining Nicol and Kling.

Third, Petitioner admits that Nicol does not discuss over-temperature protection, which in fact argues against combining it with Kling. Petitioner argues that Nicol's focus on minimizing power consumption would lead a POSITA to be motivated to consult Kling for over-temperature protection, but a broad desire to minimize power consumption does not provide a reason why a POSITA would look to Kling to combine with Nicol. Furthermore, Nicol's disclosure of monitoring temperature is for an entirely different purpose. Nicol states that "[s]ince the two critical path copies within element 120 experience the same variations in temperature as do PEs 101-104, the V_{dd}-local supply voltage appropriately tracks the temperature variations as well as the different operating frequency specifications." Ex. 1009 (Nicol) at 5:18-22. Petitioner misreads this statement to assert that Nicol includes an on-chip temperature sensor. In fact, Nicol states that there are two critical paths which are close enough so that they experience the same variations in temperature – the temperature tracking is not performed by an explicit on-chip

sensor. Nicol's concern with temperature variation is not for over-temperature, but for tracking temperature variations to ensure voltages and frequencies are modified appropriately. And the reason is that the system in Nicol is focused on power reduction based on processor load, as its title states. Petitioner has pointed to nothing in Nicol that suggests over-temperature is a concern that it was attempting to address. Petitioner states that a POSITA would have been motivated to implement Kling's system to detect power consumption and reduce it, but the citation to Ex. 1009 (Nicol) 2:18-22 only discusses managing processing load and operating voltages to minimize power consumption. Nothing other than Petitioner's statements suggests Nicol should be combined with Kling's over-temperature system.

Petitioner further argues that "a POSITA would have found it obvious, ***and in fact necessary,*** to include over-temperature control in the multiprocessor system of Nicol." (emphasis in original) Petition at 42. This is again a bare conclusion which is not supported by the actual disclosures. In order for over-temperature control to be ***necessary***, Petitioner must show that systems without such over-temperature control would fail or cease to be useful. But Petitioner has failed to point to evidence to show this. Nicol does not even mention over-temperature. Furthermore, Kling itself states: "Some processor packages include a thermal sensor to monitor the temperature of the processor." Ex. 1010 (Kling) at 1:42-43. This statement leaves open that some processor packages would not include a thermal sensor. If such a

sensor were necessary, and a standard part of all processor packages, it is unlikely Kling would have qualified this statement in this way.

B. Petitioner Fails To Establish That A POSITA Would Be Motivated to Combine Nicol With Kling and DeHon

Petitioner states that it "adds the DeHon reference to satisfy Petitioner's claim construction requiring that the data processing unit be reconfigurable." Petition at 53. But Nicol does not describe reconfigurable processors at all, which Petitioner does not dispute. And DeHon does not describe clock frequency management. There is no reason in the references themselves that Nicol and DeHon should be combined in the way that Petitioner proposes.

Petitioner relies on a disclosure in Nicol which states "A real-time operating system resides in PE 100 and allocates tasks to the other PEs from a mix of many digital signal processing applications." Ex. 1009 (Nicol) at 2:53-56. But this is a general and broad statement about the variety of tasks that can be handled by the system in Nicol. Nothing here suggests the use of reconfigurable processors. Petitioner then points to a statement in DeHon that it teaches an "inventive microprocessor [that] can serve as the principle building block for a wide range of applications including personal computers, embedded systems, application-specific computer, and general and special-purpose multiprocessors." Ex. 1012 (DeHon) at 2:18-24. But the simple mention of a wide variety of applications is too general an

overlap, and doesn't suggest that reconfigurable processors should be introduced into Nicol. These alleged motivations suffer from the same flaws of the overbroad generalized descriptions of Nicol and Kling. Petitioner further states that "adding a reconfigurable processor would improve application acceleration in Nicol's system." Petition at 54. But Nicol does not talk about application acceleration; its focus is on power management and load balancing. The reason Petitioner provides is entirely post hoc and the only support cited is a conclusory statement by Petitioner's expert, which simply repeats the citations in the petition followed by a conclusion.

Petitioner proposes that the PEs in Nicol could be replaced by DeHon's reconfigurable processor chips. But Petitioner fails to explain and provides no details how such a system would work. Petitioner only cites general statements that Nicol mentions about extending to other system arrangements. Petition at 56-57. Nicol is about load balancing and clock frequency management. DeHon does not even mention frequency. Petitioner does not address how Nicol would manage frequency using DeHon's reconfigurable processors. Petitioner does not establish that there is any reasonable expectation of success in combining Nicol and DeHon.

Petitioner then relies on certain statements in DeHon relating to "programmable gate array" and "application-specific configurations." But as discussed above, applicability to a wide variety of functions or applications is simply

a overbroad description of one feature that is not unique or even the focus of Nicol. Petitioner further points to a citation from DeHon about integration of DeHon's programmable function units (PFUs) with fixed processing units (FPUs). Petition at 57, citing Ex. 1012 (DeHon) at 7:20-25. But this is not the integration that is at issue in the combination of DeHon with Nicol, since Petitioner proposes to replace the PEs of Nicol altogether. As noted above, the issue for the proposed combination is there is no disclosure how the clock frequency in DeHon's processors, which is not discussed at all in DeHon, should be integrated with Nicol, which is about using load balancing to manage clock frequency.

Lastly, Petitioner characterizes that Nicol and DeHon are both in the "same field" of dynamically controlling processors. But this is not a same field, but rather a trait that is only common at a high level. Petitioner points to DeHon dynamically reconfiguring a programmable array, while Nicol's controller allocates tasks. This argument suffers from the same failures mentioned above about overbroad general statements about the field. Taking two references whose commonality is broadly applicable does not lead a POSITA to conclude they can combine these references and obtain predictable results, for many of the same reasons raised above.

C. Petitioner Fails To Establish That A POSITA Would Be Motivated to Combine Nicol With Kling, DeHon and Bhatia

Petitioner argues that a "POSITA would have been motivated to consult Bhatia because Nicol, Kling and Bhatia are all directed to interrelated thermal and power management aspects that are critical and ubiquitous in processor-based systems." Petition at 65. But this is the exact same, overbroad justification used for motivation to combine Nicol with Kling, and fails for the same reasons discussed above. Furthermore, this just serves to illustrate the problem with this logic – this broad description likely encompasses dozens if not hundreds of references, and thus could be used to provide a motivation to combine any of them. Motivation to combine requires a showing that "a skilled artisan would have been motivated to combine the teachings of the prior art references to achieve the claimed invention", and is not a broad pass to allow any references within a broadly defined field to be combined. *Johns Manville Corp. v. Knauf Insulation, Inc.*, Case IPR2018-00827, Paper 9 at 9-14 (Oct. 16, 2018) (Informative) (citing *Intelligent Bio-Sys., Inc. v. Illumina Cambridge Ltd.*, 821 F.3d 1359, 1367–1368 (Fed. Cir. 2016) and *Securus Techs., Inc. v. Global Tel*Link Corp.*, 701 F. App'x 971, 977 (Fed. Cir. 2017)).

Petitioner further argues that it is the lack of detailed description of the Advanced Configuration and Power Interface (ACPI) industry standard specification in Nicol and Kling that provides a motivation to combine with Bhatia.

But Nicol, for example, is not about sleep states, but about reduction in frequency by managing load. The lack of description of ACPI in Nicol is not a motivation to combine Nicol with Bhatia.

VII. THE PETITION SHOULD BE DENIED FOR ADDITIONAL REASONS

A. The Petition Should Be Denied Because of the Co-pending District Court Case

The Board should exercise its discretion and deny the Petition in view of the late stage of the parallel District Court case. *See VIZIO, Inc. v. Polaris PowerLED Technologies, LLC*, Case IPR2020-00043, Paper 30 at 6-12 (May 4, 2020) (denying institution based on the Board statutory discretion because of "(1) the advanced stage of the [] District Court proceeding; (2) the investment of time and resources by the District Court and the parties in the [] District Court proceeding; (3) overlap in the invalidity theories that Petitioner is pursuing here and in the [] District Court proceeding; and (4) overlap in the claims challenged in the [] District Court proceeding"); *see also NHK Spring Co., Ltd. v. Intri-Plex Techs., Inc.*, Case IPR2018-00752, Paper 8 (Sept. 12, 2018) (denying institution because of co-pending district court proceeding).

1. *The Advanced Stage of the Parallel District Court Proceedings and Significant Investment of Time and Resources by the Parties and District Court Counsels Weighs Against Institution.*

Petitioner waited until the last minute to file the present Petition.[1] As a result, the District Court case is in an advanced stage and the parties have invested significant time and resources in the parallel proceedings. The parties exchanged infringement contentions and invalidity contentions in October and November of 2019. Ex. 2005 at 5-7. Claim Construction briefing has been complete, and the *Markman* hearing was held on June 10, 2020. *Id*. at 7. The deadline for substantial completion of document discovery is currently scheduled for June 26, 2020. Ex. 2006. And the Pre-trial Conference is scheduled for September 3, 2021, followed by a five-day jury trial beginning on September 20, 2021. Ex. 2005 at 10.

[1] On February 7, 2019, Patent Owner filed the first patent infringement case asserting the patent at issue against Petitioner and the complaint was served on February 8, 2019. Ex. 2002 at 60; Ex. 2003. Even though the case was later dismissed (Ex. 2004), it still started the clock for the one-year bar. *See Click-to-Call Techs., LP v. Ingenio, Inc.*, 899 F.3d 1321, 1330 (Fed. Cir. 2018). The one year anniversary of the service of the district court complaint falls on a Saturday, February 8, 2020. Thus, the one year bar date is the following Monday, February 10, 2020.

The institution decision for this Petition will likely be issued three months after the filing of this Preliminary Response, on September 15, 2020, followed by a written decision approximately one-year later on September 15, 2021. *See* 35 U.S.C. §§ 314(b), 316(a). In other words, the written decision will come down on the eve of the Pre-trial conference—after the parties have completed, for instance, fact and expert discovery, expert reports, and motions for summary judgment.

Both the parties and the District Court have invested substantial time and resources in the Delaware District Court proceeding over the past year, exemplified by submission of arguments and evidence, and rulings by the court. Ex. 2007 (docket showing Motions to Compel and Discovery Order (Dkts. 53, 55, 62), Order to Extend Time (Dkt. 79), Motion to Compel (Dkt. 81), Motion to Compel (Dkt. 83), Joint Claim Construction Brief (Dkt. 90), Markman Hearing (Minute Entry on June 10, 2020), Motion for Leave to File Amended Answer to Add Inequitable Conduct Defense (Dkt. 103)). Petitioner's late filing, therefore, will require the Board and the District Court to substantially duplicate efforts and lead to wasted resources.

2. *Similar Invalidity Theories and Claims are at Issue in the Parallel District Court Proceeding*

The overlap between the District Court proceedings also counsels against institution. Here, all of the claims challenged in the Petition are also at issue in the district court. *Compare* Ex. 2008 (PACT's Letter Regarding Claim Narrowing and

Swapping) *with* Petition at 1 ("Petitioner Intel Corporation . . . respectfully requests *inter partes* review ('IPR') of claims 1–6 ('the Challenged Claims') of U.S. Patent No. 9,075,605").

The parallel District Court case also involves overlapping prior art. *See* Ex. 2009 at 75-76 (alleging challenged claims are invalid based on Bhatia and Kling). Accordingly, the invalidity theories in the parallel District Court proceedings substantially overlap with those in the Petition.

B. The Petition Is Barred by Intel's Declaratory Judgement Case Challenging Validity

On April 25, 2019, Petitioner filed a declaratory judgment action against Patent Owner. Ex. 2010. In Count IX of the Complaint, Intel sought a declaratory judgment alleging "Intel has not infringed and does not infringe, either directly or indirectly, any valid and enforceable claim of the '605 Patent" *Id*. ¶ 102 (emphasis added). Thus, despite the language used, Intel directly challenged the validity of the '605 patent. Here, because Intel asserted that it did not infringe "any valid" claims of the '605 patent, it expressly challenged the validity of the patent and put it at issue. Thus, the Petition is barred by 35 U.S.C. §315(a) ("An *inter partes* review may not be instituted if, before the date on which the petition for such a review is filed, the petitioner or real party in interest filed a civil action challenging the validity of a claim of the patent."); *see also Cisco Systems, Inc. v. Chrimar Systems, Inc.*, Case

IPR2018-01511, Paper 11 (Jan. 31, 2019) (Precedential) (denying institution under AIA § 315(a)(1)).

VIII. CONCLUSION

In view of the foregoing, Patent Owner respectfully requests that this Petition for *Inter Partes* Review of the '605 patent be denied.

Date: June 15, 2020

Respectfully submitted,

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CERTIFICATE OF COMPLIANCE

The undersigned attorney certifies that this Preliminary Response complies with the applicable type-volume limitations of 37 C.F.R. § 42.24(b)(1). Exclusive of the portions exempted by 37 C.F.R. § 42.24(a)(1), this Preliminary Response contains 7,192 words as counted by Microsoft Word.

Date: June 15, 2020

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CERTIFICATE OF SERVICE

The undersigned hereby certify that Patent Owner's Preliminary Response Pursuant to 37 C.F.R. § 42.107, along with all the exhibits were served on June 15, 2020 by filing these documents through the Patent Review Processing System, as well as by e-mailing copies to:

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