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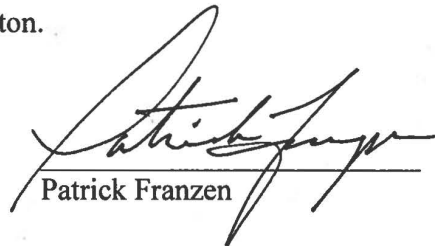
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## ***Charge-Coupled Devices and Solid State Optical Sensors IV***

**Morley M. Blouke**  
*Chair/Editor*

**7–8 February 1994**  
**San Jose, California**

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## **SESSION 1**

### **New Sensor Technologies**

## The CIVIS Sensor : A Flexible Smart Imager with Programmable Resolution

N. Ricquier, I. Debusschere, B. Dierickx, A. Alaerts, J. Vlummens, C. Claeys

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### ABSTRACT

For time critical industrial machine vision applications, a dedicated imager has been developed. The camera can be programmed to operate in several resolutions. This is done by binning the signal charges of neighbouring pixels on the sensor plane itself. Additionally the readout window was made programmable and an electronic shutter function was implemented. This square 256\*256 imager was fabricated in a standard 1.5  $\mu\text{m}$  CMOS technology. The readout occurs in two phases. After transferring in parallel a row of charges to 256 charge sensitive amplifiers, these signals are coupled to a single output amplifier. By controlling the sequence of addresses and reset pulses of the amplifiers, charges of different pixels are accumulated. This way multiple resolutions can be programmed. The imager is operated at data rates upto 10 MHz providing about 125 full images per second. At lower resolution, even higher frame rates are obtained. The signal to noise ratio is about 35 dB. This paper reports on the fixed pattern noise, response, speed and smear behaviour of this imager.

### 1. INTRODUCTION

Present machine vision systems typically use CCD based cameras as input device. In this paper an alternative image sensor is presented which was specifically developed for use in industrial machine vision applications. Our work has to be situated as a part of the effort that was undertaken within the framework of the CIVIS project<sup>†</sup> to optimize a computer vision system as a whole. A description of the entire system architecture can be found in reference<sup>1</sup>. It was recognized that for a broad scope of applications ranging from target recognition to detailed inspection, image processing systems could benefit from the ability to acquire data only from a specific region of interest and this with a variable resolution.

A first system fulfilling some of the demands just mentioned, consists of a classical CCD imager, commercially available at affordable prices, in combination with a frame buffer. This solution offers region of interest viewing, by accessing only the useful data available in the frame store. Moreover, when necessary, also a programmable resolution can be provided in a dedicated CCD design by binning charges of neighbouring pixels and reading out the accumulated signal. This type of solution however does not exploit all the possibilities of sensor design because it still suffers from the large bandwidth necessary between sensor and frame store. This drawback caused by the inherently serial data flow in CCD architectures, makes it necessary to read out all the image data, even useless ones. As a consequence scene information can only be updated at a fixed frame rate.

The sensor described here, makes it possible to acquire information of the scene in a flexible way and at a relatively high speed. The latter is especially true when combining the windowing feature with the possibility of a reduced resolution. This is a valuable asset because speed is important in a lot of industrial applications. For instance, when the image acquisition rate is increased in inspection tasks or when tracking can be performed faster in assembly tasks, the production volume can be increased accordingly. A CMOS technology was chosen because it offers the selective addressability together with the possibility of further cointegration of processing electronics on the same chip.

The development of this sensor has to be seen in the context of a burgeoning field of research, exploring smart image sensor architectures. During the last decade several researchers have been investigating this type of imager architectures. Different ways have been followed. While some people explored the processing capabilities of CCDs and related structures<sup>2-6</sup>, others regained their interest in simple CMOS photodiodes and started to build more and more complicated structures around them. CMOS architectures have been realised with 'intelligent' operations at the pixel

<sup>†</sup>CIVIS : Computer Integrated Vision System, ESPRIT II project nr 5194, cofunded by the Commission of the European Union



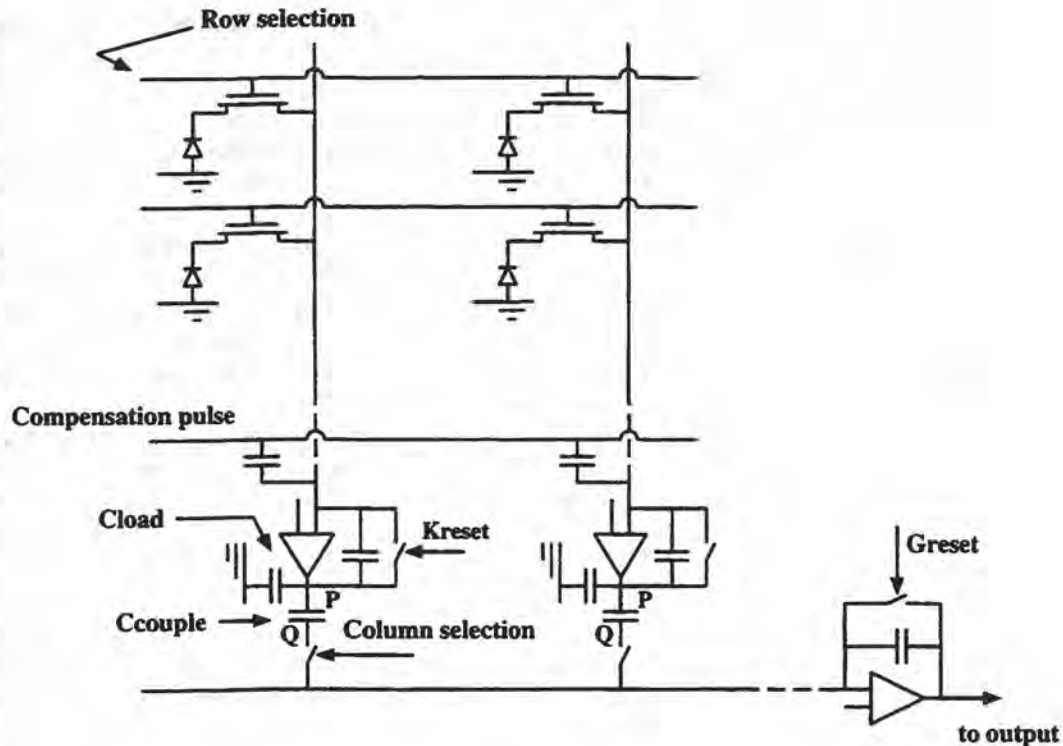


Figure 1: Schematic representation of the sensor architecture

site itself, imitating human visual functions using analog CMOS structures<sup>7,8</sup> or realising more classical operators, based on a combination of analog and digital processing<sup>9</sup>. In other CMOS sensors, processing capacity was integrated at the edges of the photodiode array exploiting the possibility to access a whole row of data at once<sup>10,11</sup>. Our work is closely related to this research, emphasizing the development of a multi-purpose flexible sensor architecture that can be used as a module in further sensor systems on a single chip. In this sense this imager belongs to a class of X-Y addressable imager architectures exhibiting properties especially useful for industrial imaging applications<sup>12,13</sup>.

## 2. SENSOR CONCEPT

To realise the acquisition of image data only in specific regions of interest, an X-Y addressable architecture was selected. Based on X-Y addresses and control pulses generated by an external driving unit, two decoders drive one particular row selection and column selection signal. These signals can be found in figure 1 which shows a schematic representation of the sensor architecture. It represents more in detail the pixel structure and the different read out stages of the pixel charges. A pixel consists of a photodiode and a switch.

The readout of the charge packets that are accumulated during the integration time, proceeds as follows. After selecting one particular row of pixels, these charges are converted simultaneously to a voltage at the output of the different charge sensitive amplifiers located at the end of the column readout lines. The output nodes of these amplifiers couple capacitively to the nodes marked as Q, resulting in the propagation of the voltage variation from point P to Q. During an initialisation phase these nodes Q were all brought to the same starting voltage, namely the virtual ground of the output amplifier. Based on the column selection signals these nodes Q are again discharged to their starting value, at the same time creating a voltage variation at the output amplifier proportional to the charges at that column. Every column selection is followed by a reset pulse on the Greset switch bringing back the output amplifier into its initial state. After that, an other charge packet can be received. After reading out a particular row of pixels, the Kreset switch is closed causing the integration capacitor to discharge. As already mentioned above,

during this initialisation cycle between two row readouts, also points Q are brought at the input voltage (virtual ground) of the output amplifier.

In every part of this read out scheme, charge packets and capacitive couplings are used between the column amplifiers and the output. Hence, theoretically the output signal is expected not to show any non-uniformities related to offset voltages of these column amplifiers. This differential operating mode is therefore a substantial advantage.

By using the Kreset switches and the Greset switch in an appropriate way, it is possible to accumulate charge packets of different pixels or of different column amplifiers on the integration capacitors according to different patterns. So by controlling the clocking scheme, the resolution of the imager can be altered and it is even possible to create rectangular pixel patterns with a resolution varying across the rows. For instance, when one wants to half the resolution by adding the charges of the pixels in 2 by 2 neighbourhoods, the readout operation proceeds as follows. After the selection of two successive rows at a rate of 2.5 MHz an additional 2 to 3  $\mu\text{s}$  is necessary for the outputs of the column amplifiers to become stable. After this wait cycle the different column signals are selected at a rate of 10 MHz with an intermediate (during the off-time of the column selection) Greset pulse every two pixels. In order to limit the complexity of the timing controller (realised in an off-chip driving unit) only timing configurations of some very common patterns are provided : apart from the normal resolution (1\*1) also the addition of pixel charges in 2\*2, 4\*4 and 8\*8 neighbourhoods was foreseen.

The ability to create different types of pixel patterns has an important consequence for the dimensions of the integration capacitors at the amplifiers. When the resolution is reduced by a factor K the frame rate increases in an almost proportional way. This results in charge levels in the pixels that are K times lower than in the case of the 1\*1 resolution. Due to the fact that K of these charge packets are summed at the input of a column amplifier, the order of magnitude of the charge that is put on these integration capacitors is approximately equal in all 4 operation modes. This ensures that at a given illumination level, the resolution of the sensor can be changed on the fly, while still respecting the limited voltage range in which the charge sensitive amplifiers have a linear behaviour. At the output stage however, several capacitors had to be provided. These capacitors are switched on according to the resolution at hand.

An electronic shutter function is implemented as follows. Shortening of the integration time is done by initializing a particular row of pixels during the horizontal blanking time. For instance, when an integration time about half the frame time is required, the row that will be read out a half frame later has to be selected. Prolonging the integration time is obvious and realised by suspending the readout phase, in this way also lowering the frame rate.

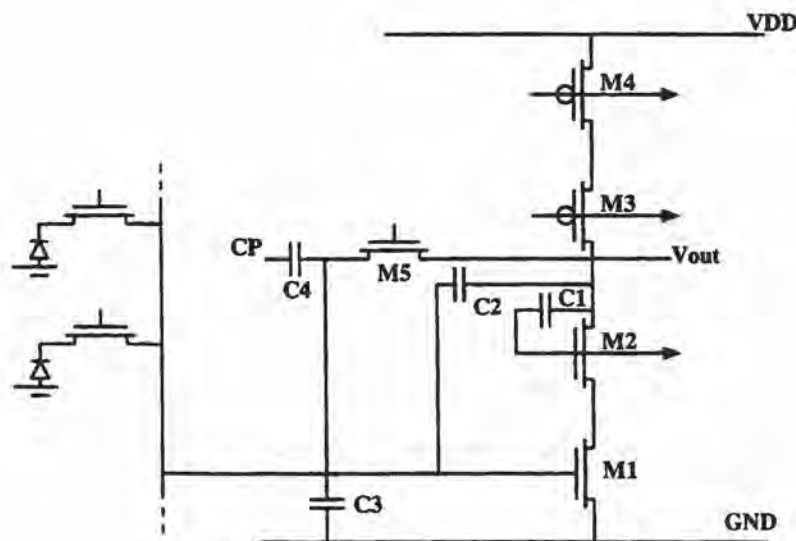


Figure 2: Transistor scheme of the column amplifier



It was already mentioned above that the addressing speeds in X and Y direction are asymmetrical. This is due to the geometrical restrictions on the column amplifiers. A transistor scheme of these charge sensitive amplifiers can be seen in figure 2. When transistor M2 and M3 are omitted, this scheme represents an inverting amplifier in its most simple form. However, to realise a good virtual ground at the input node of the amplifier, cascode transistors M2 and M3 were added (voltage variations at the output take place without any noticeable voltage variations at the input node). To obtain a fast response, the gain-bandwidth product of the amplifier has to be maximized. To this end, the transconductance of the input transistor has to be made as high as possible. The limit is the maximal value that can be tolerated for the channel width versus channel length ratio, given the available area. As a consequence, the settling time of these column amplifiers is in the order of 2 to 3  $\mu\text{s}$ , while the output amplifier based on a similar structure can operate at speeds upto 10 MHz.

The limited bandwidth of the column amplifiers causes a major problem in the design of this sensor. When reading out the signals present at the nodes Q (see figure 1) a capacitive coupling occurs to the output nodes of the amplifiers bringing them out of equilibrium. For this reason additional capacitors,  $C_{load}$ , were added at nodes P, reducing a pure capacitive coupling into a voltage division. As a consequence when a switch closes, immediately a voltage variation is felt at the output that is proportional to the amount of charge that was situated on the couple capacitor. Following this sudden voltage drop, the output voltage tends to a stable value with the time constant of about 3  $\mu\text{s}$ . Waiting for all signals to become stable is unacceptable because the column addressing must be done at speeds upto 10 MHz. However, as was already mentioned above, the instantaneous voltage drop is also proportional to the amount of signal charge. Therefore it was decided to read out the output signal associated with this sudden voltage drop.

When increasing the capacitance of  $C_{load}$ , the instantaneous voltage drop at the output amplifier becomes larger (because the voltage dip at the output of the column amplifier is smaller). So one would like to take a relatively high capacitance value at point P and an, in comparison, smaller value for the couple capacitor. However, what really counts is the total number of charges that are transferred to the output stage and this amount is also proportional to the value of the couple capacitor. Taking into account the limited space available at the pitch of the column amplifiers, it was decided to take a couple capacitor of about 40 fF and an additional output capacitor at point P of about 30 fF.

Finally, a last signal present on figure 1 has to be explained : the compensation pulse. The shape of this pulse corresponds to the inverse of the reset signal and can be tuned in such a way that it guarantees that the reset voltage at the output of the amplifiers is at the onset of the region in which the response is linear. Indeed, when the reset signal would be the only one that is applied, the associated clockfeedthrough and the redistribution of the charges coming from the reset transistor would cause a considerable decrease in output swing.

### 3. Practical realisation

The pixel array consists of 256 by 256 square pixels arranged on a pixel pitch of 19  $\mu\text{m}$  and realised in a 1.5  $\mu\text{m}$  n-well CMOS technology. The pixel pitch is not limited by the pixel structure itself, but by the minimal width of the column amplifier. The fill factor of the pixel is approximately 55%. The technology used offers two metal layers and two poly layers. The second poly layer was exclusively used for the realisation of compact, linear capacitors (0.5 fF/ $\mu\text{m}^2$ ) : the integration capacitors at the output amplifier, the couple capacitors  $C_{couple}$  and the load capacitors  $C_{load}$  (see figure 1). As to these last two types of capacitors it is essential to minimize geometrical aberrations and misalignment because of the consequences for the uniformity of the response at the output. Therefore approximately square shapes were chosen.

The integration capacitors on the contrary were realised using the overlap of metall and poly1 which represents a capacitance of about 0.05 fF/ $\mu\text{m}^2$ . The reason for the choice of this type of capacitor is that, because of sensitivity, the capacitance value may not be too large (3fF as a whole), but on the other hand geometrically it may not be too small for reproducibility reasons.

A last type of capacitors that is present in the circuit are the compensation capacitors at the inputs of the column



amplifiers and the output amplifier. They are formed by a poly electrode that is completely covering a patch of the active area. In this way this type of capacitor has exactly the same behaviour as the gate capacitor of the reset transistor which charge it has to compensate for.

#### 4. Results

A general impression of the image quality can be seen in figure 3. This figure illustrates the four resolutions that are supported by the driving unit : 256 by 256 pixels, 128 by 128, 64 by 64 and 32 by 32. These four images are formed on the sensor plane itself without any external calibration. In what follows different sensor characteristics will be described. All measurements mentioned were performed using light at a wavelength of 550 nm.

##### 4.1. Response

Figure 4 shows the average value of the image in relation to the (homogeneous) illumination level. This curve clearly shows a good linear characteristic while saturating at illumination levels of about  $15 \mu\text{W}/\text{cm}^2$ . The total dynamic range in this measurement was approximately 400 mV. This measurement was performed given a  $1 \times 1$  resolution and a speed of about 125 full images per second. At a lower speed of about 34 full images per second the dynamic range is about 750 mV.

##### 4.2. Behaviour under high illumination conditions

When increasing the illumination more and more, a smear effect can be seen on columns that contain highly illuminated parts. These columns turn completely white. The cause of this effect is found in the presence of parasitic diffusions at the selection transistors in the pixels. The actual photodiode is realised as an enlarged source diffusion of the selection transistor. The drain diffusion, although ten times smaller and completely covered with metal, also collects photon induced charges and is continuously influencing the readout line. Taking into account that there are 256 of these parasitic photodiodes simultaneously collecting charges on the column readout line, this effect is not negligible. An estimation of this effect can be made quickly. The integration time on such a parasitic diode is  $1/256$  of the integration time on the diodes of the pixels itself (in normal integration mode). Due to the fact that 256 parasitic diodes are influencing simultaneously the readout line and that the area of a parasitic diode is about  $1/10$  of the area of a pixel diode, this would mean that one out of ten charges accumulated on a column amplifier would be contributed by parasitic effects. This problem was reduced by putting a metal<sup>2</sup> shielding on top these parasitic diodes. Measurements have shown that with a spot illumination exceeding five times the dynamic range, this smear effect becomes prominent. The spot size covered 30 pixels of the particular column.

##### 4.3. Dark current

The dark current level can be characterised as follows : it takes about 13 seconds to obtain an output signal equivalent with the dynamic range. This measurement was done at  $21^\circ\text{C}$ .

##### 4.4. Fixed pattern noise

The non-uniformity in response is mainly related to the column amplifier structures. This non-uniformity was measured for several uniform illumination levels. This way an idea was formed of what is usually called photoreponse non-uniformity (PRNU). Figure 5 shows the mean value of the output signal (in ADC values) on the different columns for several illumination levels. The illumination levels are expressed in  $\mu\text{W}/\text{cm}^2$ . A maximal PRNU can be observed of 15% of the total dynamic range. A regular pattern in the X dimension appears corresponding to the variations of the bits of the column address. This is an indication that the PRNU is not only caused by the sensor architecture but also by the generation of the address clocking signals. Probably, the non-equilibrium condition in which the read out operation is done, is influencing this PRNU.





Figure 3: Resolution changes on the sensor plane

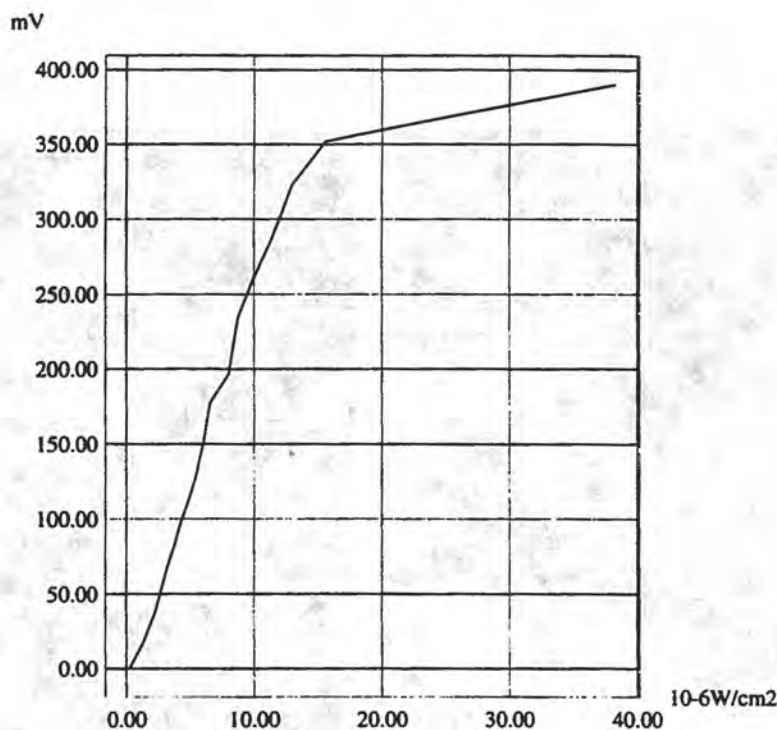


Figure 4: Response of the imager

#### 4.5. Temporal noise

This type of noise manifests itself as variations of the output signal of one particular pixel. Using a frame grabber setup 1024 samples were acquired of the same pixels at the maximal speed of 125 frames per second. By calculating on these timesequences the standard deviation around the average, a value for the RMS value of the temporal noise of the imager can be derived in real operating conditions.

This operation was done for all 4 resolutions, resulting in values from 30dB to 35 dB. The best results were obtained for the 2\*2 resolution. The reason for this lies in the availability of an optimal capacitance value at the output amplifier. To obtain the same signal to noise ratio for the 1\*1 resolution, the parasitic capacitance always present at the output amplifier should be further reduced.

The spectral distribution of the noise corresponds to white noise. The absence of 1/f-noise for the lower frequencies can be explained by the differential operation of the charge amplifiers.

Good agreement of the measurements with hand calculations was found. The dominant noise sources are related to the column amplifiers. A value of about 600 equivalent noise electrons was calculated, given a total dynamic range of about 40000 electrons.

#### 4.6. Speed

The maximal frame rate still offering an acceptable image quality is about 125 full images per second. The whole system is operated from a 20 MHz master clock, offering a maximal data rate of 10 MHz in the 1\*1 resolution. In that case a horizontal blanking time of 5  $\mu\text{s}$  is respected, consisting of an initialising cycle, a row selection cycle and an additional settling time. In the higher resolutions, given the same maximal clock frequency, respectively 195, 355 and 540 full images per second can be acquired. The frame rate does not increase proportionally because the



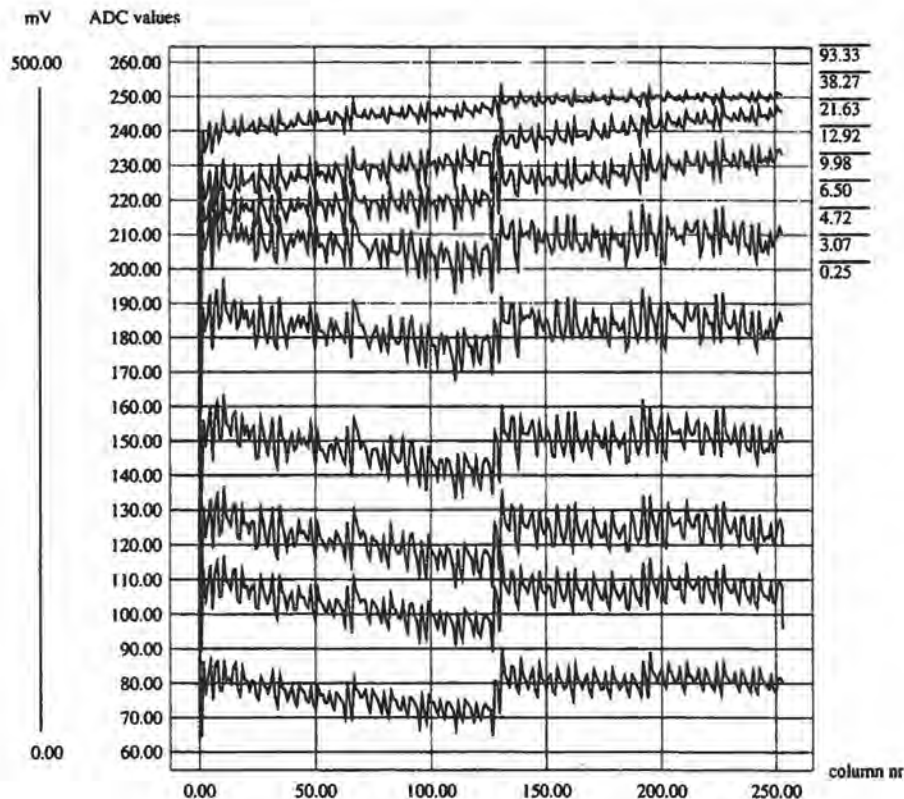


Figure 5: non uniformity in the row direction

horizontal blanking time strongly increases due to the larger initialisation and selection cycles.

## 5. Conclusions

A dedicated image sensor for time critical industrial applications was presented. It consists of a 256\*256 X-Y addressable photodiode array integrated together with a readout structure that allows the addition of charges of different pixels. The sensor was realised in a 1.5  $\mu\text{m}$  standard CMOS technology. Apart from the windowing feature and the possibility to change the resolution, also an electronic shutter function was realised. The frame rate ranges from 125 full images per second up to 540 full images per second in the lowest resolution mode. Compared to CCD imagers the S/N is quite bad, but for the intended industrial applications it is sufficient.

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