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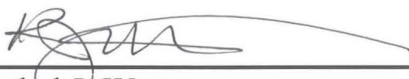
an excerpt of pages 115 to 124 of that volume, showing the article entitled *800-thousand-pixel color CMOS sensor for consumer still cameras* (1997). Based on this information, the date stamp on the volume's cover page indicates *800-thousand-pixel color CMOS sensor for consumer still cameras* (1997) was received by the University of Wisconsin-Madison Libraries on June 6, 1997.

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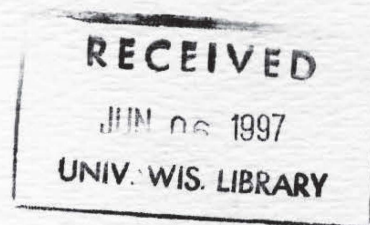
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## ***Solid State Sensor Arrays: Development and Applications***

**Morley M. Blouke**  
*Chair/Editor*

**10–11 February 1997**  
**San Jose, California**

*Sponsored by*  
IS&T—The Society for Imaging Science and Technology  
SPIE—The International Society for Optical Engineering



**Volume 3019**



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# An 800K-Pixel Color CMOS Sensor For Consumer Still Cameras.

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## ABSTRACT

An 800k-pixel Active Pixel device has been developed for use in a Digital Still Camera application. A mode of operation has been developed to cancel the problems of Fixed Pattern Noise (FPN) and dark current inherent to this type of CMOS imaging array. A time multiplexed read-out mechanism allows the device to operate at 5 Mpix/s and still settle to within 0.1%. The device, with a full well of approximately 100K electrons, is capable of delivering a S/N of 66dB, and a sensitivity of approximately 50mV/lux at 50ms exposure. The sensor is covered with a color mosaic to allow an accurate recovery of a color image. This sensor makes new in-roads for CMOS imaging into areas traditionally occupied by CCD's

**Keywords:** CMOS sensors, Active Pixels, Image Sensors, Digital Still Cameras

## 1.0 INTRODUCTION

We report on the development and performance of an 800k-pixel Active Pixel Sensor (APS) for a new generation of Digital Still Cameras (DSC). The operation of the device takes advantage of other system components found in a typical DSC application (Figure 1), in order to cancel threshold offsets and dark current FPN inherent to Active Pixel arrays that are fabricated on standard digital CMOS processes. This provides a cost effective final solution. In a DSC there is usually a Frame store available, it is sufficient to know that a 12-bit deep frame store is available off the sensor as a normal part of the camera function (in a still camera the image is digitised and stored in this buffer prior to compression for long term storage). We use this buffer as a cache store for several image operations.

## 2.0 PIXEL ARCHITECTURE

The active pixel which lies at the heart of the image sensor is shown in Figure 2. It comprises 3 transistors; M1 which forms the top section of a NMOS source follower stage, M2 - the access transistor for reading the pixel and M3 the reset transistor. This simple pixel type is chosen for low read noise, compact layout and good spectral response. The inherent problem with a photodiode pixel type, namely reset noise, is overcome by an appropriate operating scheme, that uses the possibility of a non-destructive read to cancel the effective reset voltage.

The reset/integrate/read cycle of the pixel starts with the reset transistor M3 turned on, so that the pixel voltage,  $V_{pix}$ , is reset to  $V_{RT}$ . When the control line for M3,  $Rst[n]$  goes low the photodiode starts to discharge the pixel capacitance. Near the end of the required exposure period, the read transistor, M2, is turned on by  $Rd[n]$  going high. This connects a current source at the bottom of the pixel columns to the output of transistor M1 forming an NMOS source follower. The output line,  $Vx[m]$  will settle to a roughly a NMOS threshold voltage below  $V_{pix}$ . The integration time of the pixel ends when  $Rd[n]$  goes low. Finally,  $Rst[n]$  goes high to return the pixel into reset, to prevent any problems caused by the pixel blooming when not in use. Instead of toggling the  $Rst[n]$  line from 5V to 0V when going from reset to integration, it is possible to put the reset line to a voltage ' $V_{bloom}$ ' that is chosen to be between  $V_{RT}$  and  $V_{T(NMOS)}$ , so as not to introduce Fixed Pattern Noise in white areas of the image.

The pixel is laid out to be 10.8um square using a 0.8um double-metal, single-polysilicon, industry standard, CMOS process.

Company Information: [WWW.vvl.co.uk](http://WWW.vvl.co.uk)



### 3.0 SENSOR ARCHITECTURE

The sensor chip architecture (Figure 3) includes conventional shift-register based access by row and column. However, column output is via a multiplexed, buffered tree which has been optimised to achieve sample settling to better than 0.1% at a pixel read-out rate of 5 Msps.

Each tree path, and of course the pixel itself, contains a random but fixed offset, which is also cancelled as part of the general operating scheme.

The image sensor comprises an 804 by 1014 array of active pixels (photodiode plus the top section of a NMOS source follower stage - Figure 3) feeding into a row of column PMOS source followers at the top of the photodiode array. These columns are then in turn multiplexed on to 4 output channels, and finally onto the AVO output.

Exposure is controlled by a reset shift register with pixel read-out controlled by the read and horizontal shift registers. The resetting and reading of the pixel is performed on a line to line basis, i.e. the row of column amplifiers read a whole line of pixel voltages in parallel. The length of the pulse, FI, propagating up this register sets the exposure time for a line of pixels. The pulse, FR, propagating down the read vertical shift register, decides which line is to be read.

The columns are read out by the LS pulse propagating along the Horizontal Shift Register. To avoid bandwidth limitations within the output stage causing crosstalk problems between the colours in a colour pixelated sensor the horizontal shift register either reads out the odd columns and then the even columns, Shuffling the data. This can be later unshuffled in the picture processing.

At the top of the array are the current sources which combine with the M1 transistor in the pixel to form the pixel source follower. Also at the top of each column is a sample and hold stage and a PMOS source follower to drive the output stage. The purpose of the sample/hold stage is to allow all the pixels within a line to have the same exposure, as the outputs of a row pixels are sampled in parallel.

The columns are read-out via 4 column output channels. Each channel is multiplexed out onto the AVO pin, via an AC-coupling stage. This is used to restore the DC content. There is an onboard 5-bit DAC that can be used to adjust one or other of the clamping voltages in order to put the video into the input window of the ADC. It should be noted that the video is 'inverted', i.e. Black is higher than White. There is an AVOREf pin to provide a pseudo-differential output, by providing a 'mimic'ed output stage of an internal reference of black. This can be used to track any output chain variations and to set-up the sampling ADC range.

In keeping with the attributes of a CMOS sensor, the device integrates a number of peripheral circuit functions, including a low-noise op-amp based output buffer designed to ensure glue-free interfacing to an industry-standard A/D converter. (Figure 4)

### 4.0 COLORIZATION

A four-color pixel arrangement based on the primary colors (RGB) has been used. This provides high color fidelity with low color aliasing; an objective which is especially relevant for still photography. The 4 colours are Red, Green, Blue and Teal (a mixture of Blue/Green).

### 5.0 DEVICE OPERATION

Although the read-out path is intrinsically low noise, there are several offset noise sources that need to be cancelled if we are to achieve net image noise in the range of -60dB to -70dB, as required for high quality still image reproduction. In simple terms the imager is read twice; one image is taken in the dark and forms a reference, and the other image is exposed. The array is not reset between the two images. The two images are differenced and the result is the 'clean' image. There are many different ways to operate the device to give this result, Figure 5 shows a sequence of 1 reset, and 3 reads that leads to cancellation of Reset Noise, Array offsets, and dark current FPN.

The 3 reads are:-

- (A) The reference image, which contains the Array threshold FPN and the KTC reset noise.
- (B) The exposed image, which contains the reference image, the signal and the dark current FPN.
- (C) The dark image, which contains the exposed image, and another dark current FPN (4x the value).

By simple calculations the signal can be extracted from these sources of FPN and noise, leaving behind a residual noise.

$$\text{difference image} = \text{exposed} - \text{reference} = B - A$$

$$\text{Dark corrected image} = \text{difference} - (\text{dark} - \text{exposed})/4 = (B - A) - (C - B)/4$$

A summary of the principle mechanisms of FPN and Reset Noise is given below.

### 5.1 Reset Noise

The photodiode has capacitance and because it is switched when reset it is subject to KTC noise, as the same Photodiode reset noise is present in both reference and exposed images it is therefore cancelled in the difference image.

### 5.2 Transistor Threshold Offsets

The path from photodiode to output contains a total of 3 source follower buffers (including the one in the pixel), and a final op-amp buffer, each with a threshold related offset. As these are static they are also cancelled in the difference image. This cancellation can be imperfect due to flicker noise over the period between the two reads. We have measured this effect, and account for it in the cumulative noise analysis below.

### 5.3 Dark Current

Dark current fixed pattern noise is estimated by repeating the entire image capture process but with a closed mechanical shutter. To reduce noise added through this process it can be beneficial to extend the exposure time for dark image by some factor (4x is used in this paper)

## 6.0 Residual Noise

With successful operation of the above scheme all fixed pattern sources are cancelled and the residual sources are:-

#### (i) Flicker noise in the output chain

The major contributors are the M1 transistor of the pixel, which is a very small NMOS device (Flicker noise being inversely proportional to area), and in the Output buffer which contains several transistors.

#### (ii) Thermal noise in the output chain

Thermal noise is related to bandwidth, the Output Buffer and external amplifier have been respectfully chosen to limit their bandwidths to 30MHz, keeping their noise contributions down

#### (iii) A/D quantisation noise

The quantisation noise is calculated from the theoretical limit, of a perfectly linear ADC. It is related to the number of bits of resolution. The noise of the system is calculated for both 10bit and 12bit ADC's. Note that a 'real' ADC will be worse than the theoretical limit.

(iv) Dark current shot noise

The dark current noise contribution are calculated as the Square root of the mean dark current. The mean dark current was calculated at 25C and will double for approximately every 8C. The noise contribution of the 'dark' image is greatly reduced by dividing it's contribution by 4.

### 6.1 Noise Analysis

Note that these noise figures represent the net performance of the total camera system, in normal operating mode not just read noise of the sensor alone. All figures are rms electrons, referred to photodiode.

	Reference Image (A)	Differenced Image (B-A)	Dark-Current Compensated Image (B-A)-(C-B)/4
Array/Read-out Offsets	7000	#	-
Reset Noise	52		
Average Dark Current Fixed Pattern (200msec)	-	360	*
Dark Current Shot Noise	-	19	21
Thermal Noise	12	17	18
Flicker Noise	-	6	6
10/12- bit A/D Quantisation	28/7	40/10	41/10
Total Camera Noise (10/12) bit			50/30
Theoretical S/N (10/12) bit			66dB/71dB

# Values here are present, but cancelled in image difference operation.

\* Values here are present, but are cancelled by taking the difference

### 7.0 Measured Data and Status

The device has been fabricated (Figure 6) and is 100% functional, producing color still images of very high quality. Characterisation measurements confirm that the performance is close to the noise data given, with S/N figures of 62dB and 66dB respectively for the 10-bit and 12-bit systems. The Quantum efficiency and spectral response are in line with published results for similar photodiode structures. a summary of the performances are given below



## 8.0 Summary of Sensor Characteristics

Technology	0.8um CMOS
Array Size	1014 x 804
Pixel Size	10.8um x 10.8um
Fill Factor	26%
Saturated Signal	100k electrons
Sensitivity	10uV/electron
Responsivity - Black/White with IR Filter	200mV/lux at 50mS exposure
Responsivity - Average Color with IR Filter	50mV/lux at 50mS exposure
Dark Signal	15mV/S at 25C
Non-Linearity	<3% across Full Scale
S/N of the 10 Bit system	62 dB
S/N of the 12 Bit system	66 dB
Sensor Power Supply	5 V
Sensor Power Consumption	120 mW
Pixel rate for 0.1% settling	5 MSPS
Maximum Pixel rate	10 MSPS

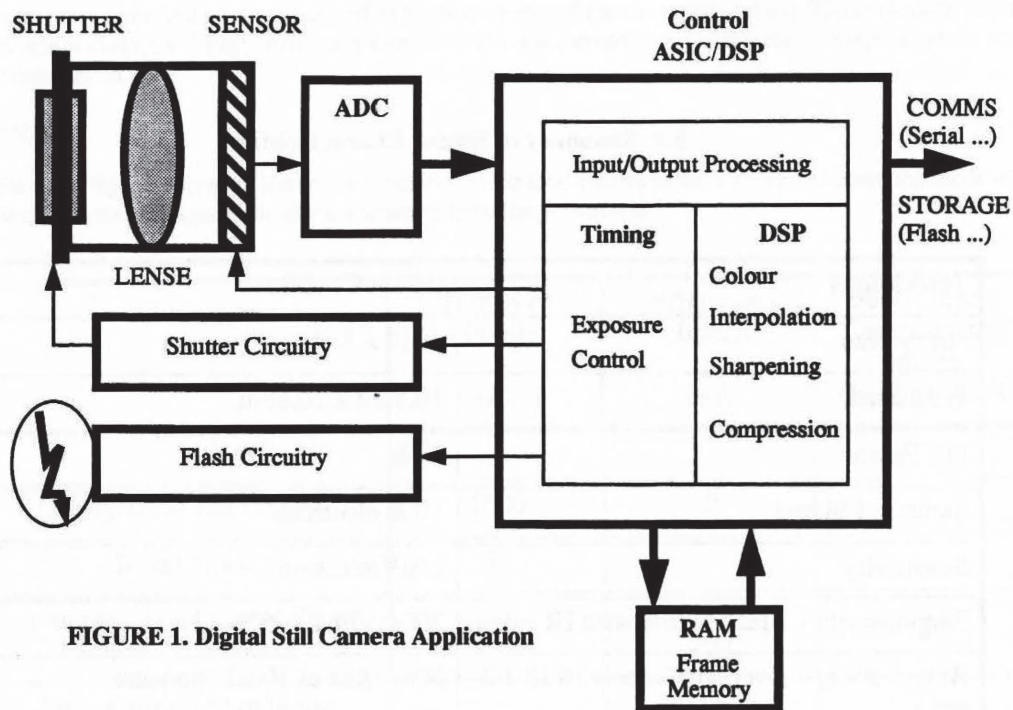


FIGURE 1. Digital Still Camera Application

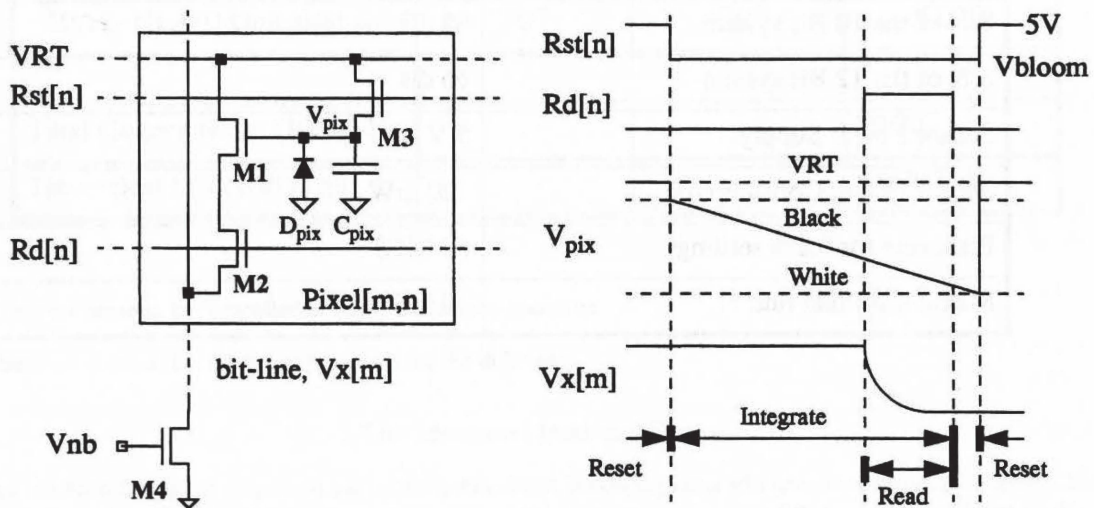


FIGURE 2. An Active Pixel.

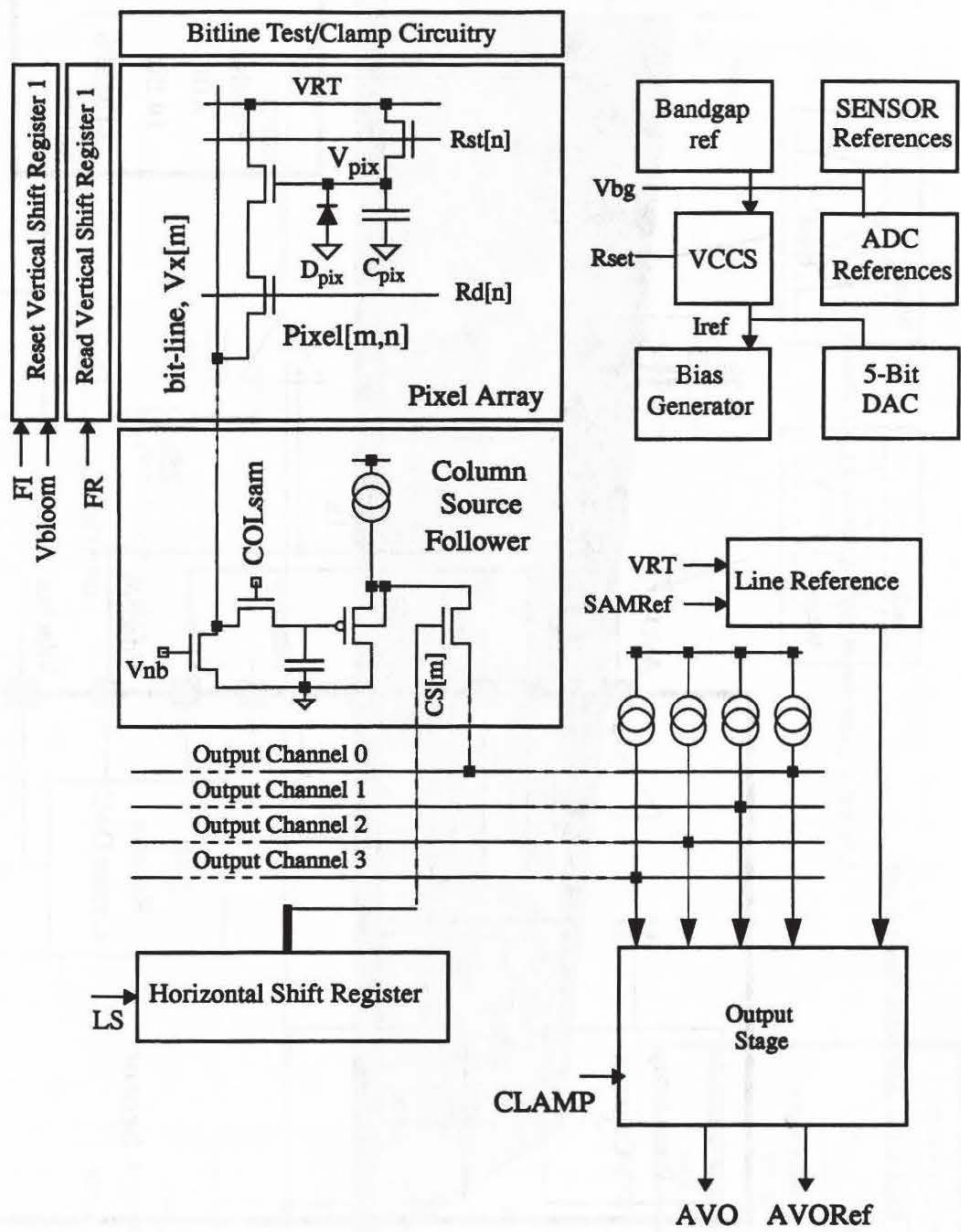
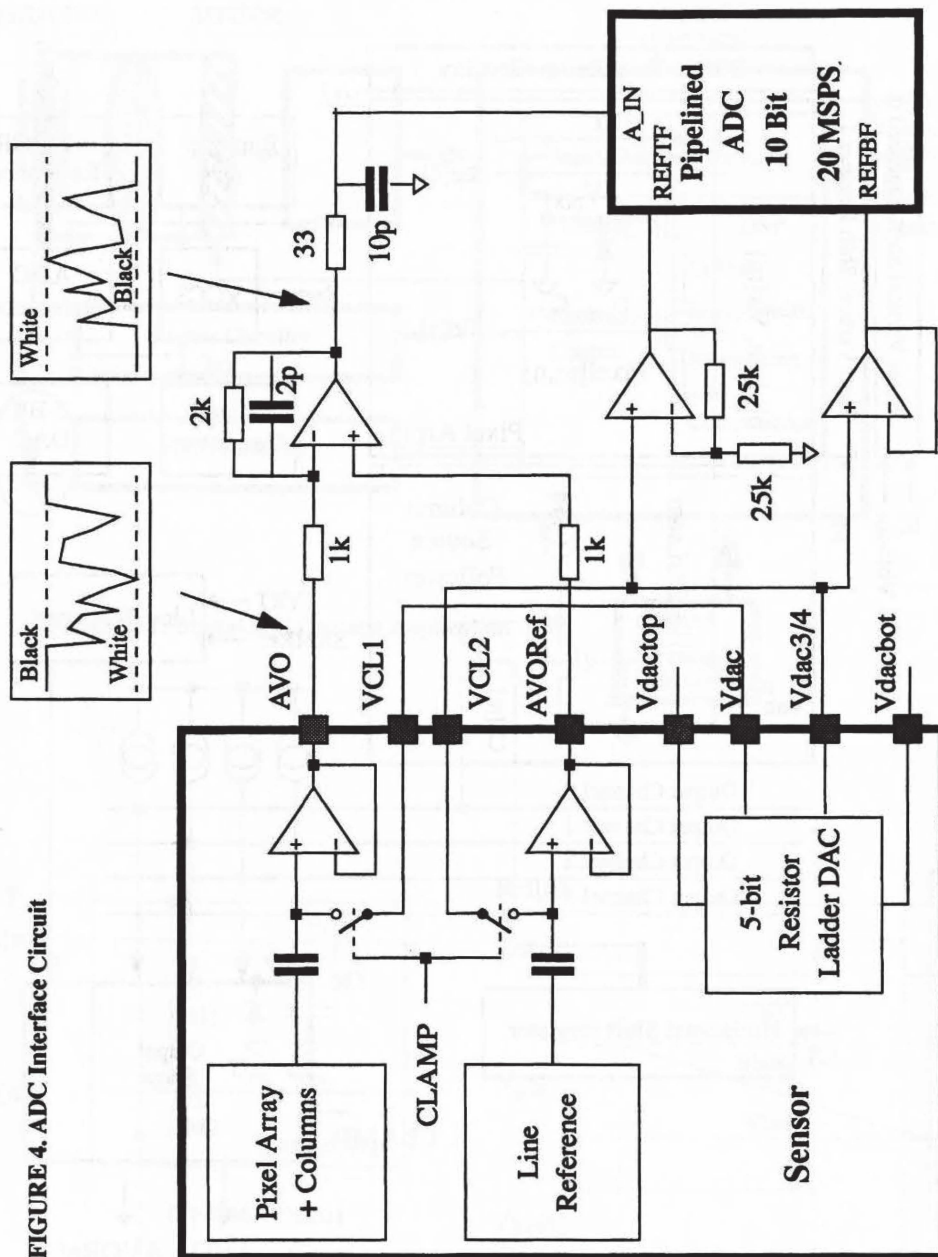


FIGURE 3. Sensor Architecture.



FIGURE 4. ADC Interface Circuit



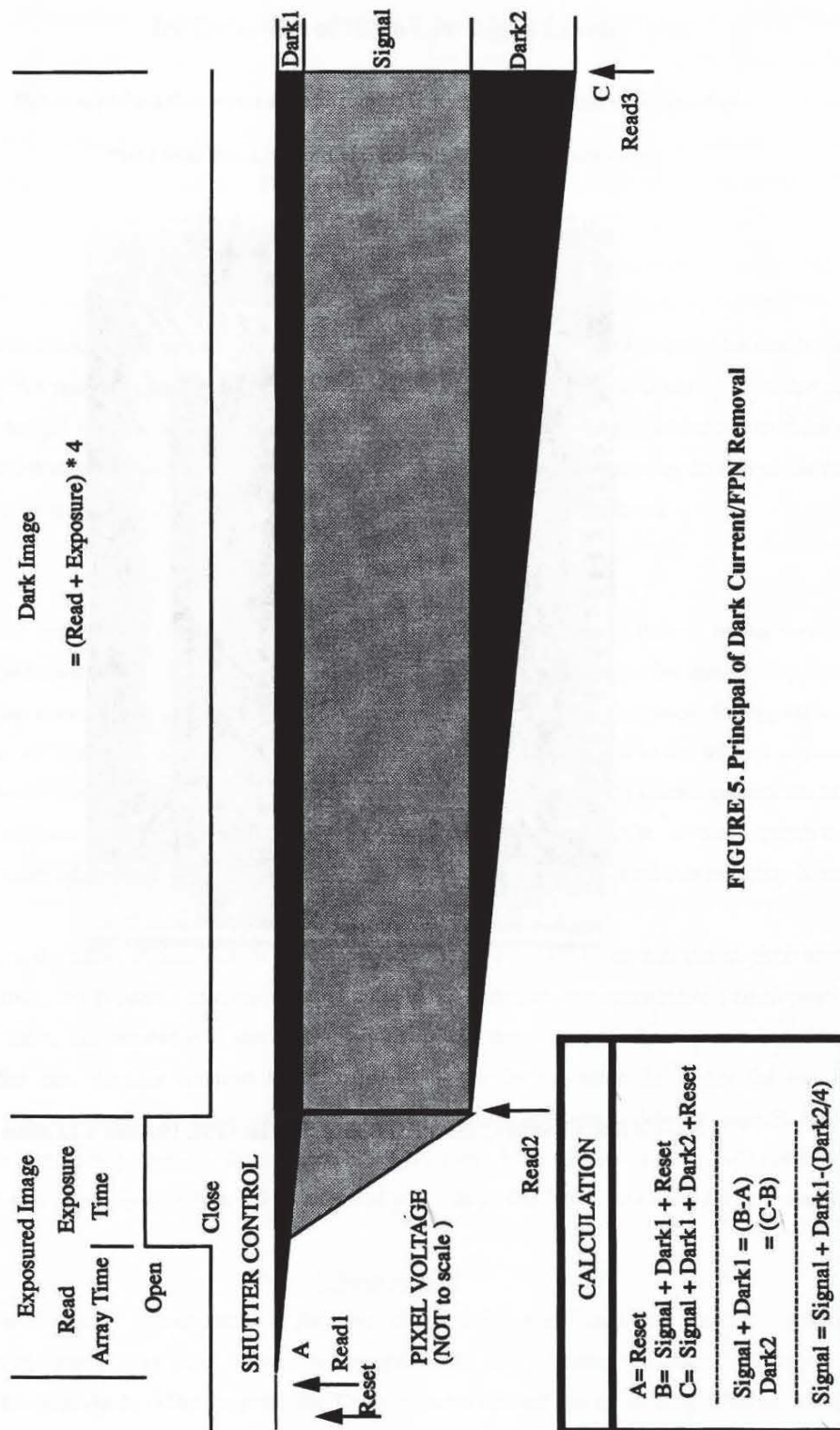
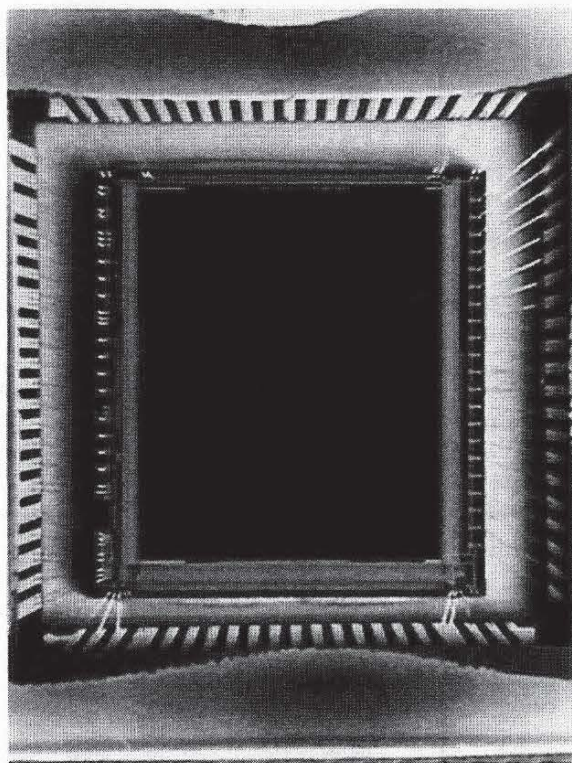


FIGURE 5. Principal of Dark Current/FPN Removal



**FIGURE 6. VV6800 CHIP PHOTOMICROGRAPH, 10.8mm x 12.3mm**