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PTO/SB/05 (4/96)
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UTILITY PATENT APPLICATION TRANSMITTAL <small>(Only for new nonprovisional applications under 37 C.F.R. § 1.53(b))</small>	Attorney Docket No. <u>E97.13 CIP7</u>
	First Inventor or Application Identifier <u>Edwin L. Adair, et al</u>
	Title <u>Hand-held Computers Incorporating Reduced Area Imaging Devices</u>
	Express Mail Label No. <u>EL547144479US</u>

APPLICATION ELEMENTS <small>See MPEP chapter 600 concerning utility patent application contents.</small>		ADDRESS TO: Assistant Commissioner for Patents Box Patent Application Washington, DC 20231	
1. <input checked="" type="checkbox"/> * Fee Transmittal Form (e.g., PTO/SB/17) <small>(Submit an original and a duplicate for fee processing)</small>	5. <input type="checkbox"/> Microfiche Computer Program (Appendix)	ACCOMPANYING APPLICATION PARTS 7. <input type="checkbox"/> Assignment Papers (cover, sheet & document(s)) 8. <input type="checkbox"/> 37 C.F.R. § 3.73(b) Statement <input type="checkbox"/> Power of Attorney <small>(when there is an assignee)</small> 9. <input type="checkbox"/> English Translation Document (if applicable) 10. <input type="checkbox"/> Information Disclosure Statement (IDS)/PTO-1449 <input type="checkbox"/> Copies of IDS Citations 11. <input type="checkbox"/> Preliminary Amendment 12. <input checked="" type="checkbox"/> Return Receipt Postcard (MPEP 503) <small>(Should be specifically itemized)</small> 13. <input checked="" type="checkbox"/> * Small Entity Statement filed in prior application, Status still proper and desired <input type="checkbox"/> <small>(PTO/SB/09-12)</small> 14. <input type="checkbox"/> Certified Copy of Priority Document(s) <small>(if foreign priority is claimed)</small> 15. <input checked="" type="checkbox"/> Other: Declaration Accompanying Petition Under 37 CFR 1.102 Petition to Make Special Under 37 CFR 1.102	
2. <input checked="" type="checkbox"/> Specification [Total Pages <u>32</u>] <small>(preferred arrangement set forth below)</small> - Descriptive title of the Invention - Cross References to Related Applications - Statement Regarding Fed sponsored R & D - Reference to Microfiche Appendix - Background of the Invention - Brief Summary of the Invention - Brief Description of the Drawings (if filed) - Detailed Description - Claim(s) - Abstract of the Disclosure	6. Nucleotide and/or Amino Acid Sequence Submission <small>(if applicable, all necessary)</small> a. <input type="checkbox"/> Computer Readable Copy b. <input type="checkbox"/> Paper Copy (identical to computer copy) c. <input type="checkbox"/> Statement verifying identity of above copies		
3. <input checked="" type="checkbox"/> Drawing(s) (35 U.S.C. 113) [Total Sheets <u>12</u>]			
4. Oath or Declaration [Total Pages <u>3</u>] a. <input checked="" type="checkbox"/> Newly executed (original or copy) b. <input type="checkbox"/> Copy from a prior application (37 C.F.R. § 1.63(d)) <small>(for continuation/divisional with Box 16 completed)</small> i. <input type="checkbox"/> DELETION OF INVENTOR(S) <small>Signed statement attached deleting inventor(s) named in the prior application, see 37 C.F.R. §§ 1.63(d)(2) and 1.33(b).</small>			
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16. If a CONTINUING APPLICATION, check appropriate box, and supply the requisite information below and in a preliminary amendment: <input type="checkbox"/> Continuation <input type="checkbox"/> Divisional <input checked="" type="checkbox"/> Continuation-in-part (CIP) of prior application No: <u>09 / 496,312</u> <small>Prior application Information: Examiner _____ Group / Art Unit: <u>2713</u></small> For CONTINUATION or DIVISIONAL APPS only: The entire disclosure of the prior application, from which an oath or declaration is supplied under Box 4b, is considered a part of the disclosure of the accompanying continuation or divisional application and is hereby incorporated by reference. The incorporation can only be relied upon when a portion has been inadvertently omitted from the submitted application parts.			
17. CORRESPONDENCE ADDRESS <input type="checkbox"/> Customer Number or Bar Code Label <u>[REDACTED]</u> or <input checked="" type="checkbox"/> Correspondence address below <small>(Insert Customer No. or Attach bar code label here)</small>			
Name <u>Brent P. Johnson</u>			
Address <u>Fields & Johnson, P.C.</u>			
<u>8480 East Orchard Road</u>			
<u>Suite 5600</u>			
City <u>Englewood</u>	State <u>CO</u>	Zip Code <u>80111</u>	
Country <u>U.S.A.</u>	Telephone <u>303-689-9100</u>	Fax <u>303-689-9250</u>	

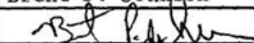
Name (Print/Type) <u>Brent P. Johnson</u>	Registration No. (Attorney/Agent) <u>38,031</u>
Signature <u>[Signature]</u>	Date <u>8/15/00</u>

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FEE TRANSMITTAL		Complete if Known	
for FY 2000		Application Number	
Patent fees are subject to annual revision. Small Entity payments <u>must</u> be supported by a small entity statement, otherwise large entity fees must be paid. See Forms PTO/SB/09-12. See 37 C.F.R. §§ 1.27 and 1.28.		Filing Date	
TOTAL AMOUNT OF PAYMENT (\$) 1,230.00		First Named Inventor	Edwin L. Adair, et al.
		Examiner Name	
		Group / Art Unit	
		Attorney Docket No.	F97.13 CIP7

METHOD OF PAYMENT (check one)	FEE CALCULATION (continued)																																																																																																																								
<p>1. <input checked="" type="checkbox"/> The Commissioner is hereby authorized to charge indicated fees and credit any overpayments to:</p> <p>Deposit Account Number: 06-0778</p> <p>Deposit Account Name: Fields & Johnson, P.C.</p> <p><input checked="" type="checkbox"/> Charge Any Additional Fee Required Under 37 CFR §§ 1.16 and 1.17</p> <p>2. <input checked="" type="checkbox"/> Payment Enclosed: <input checked="" type="checkbox"/> Check <input type="checkbox"/> Money Order <input type="checkbox"/> Other</p>	<p>3. ADDITIONAL FEES</p> <table border="1" style="width: 100%; border-collapse: collapse; font-size: x-small;"> <thead> <tr> <th>Large Entity Fee Code (\$)</th> <th>Small Entity Fee Code (\$)</th> <th>Fee Description</th> <th>Fee Paid</th> </tr> </thead> <tbody> <tr><td>105 130</td><td>205 65</td><td>Surcharge - late filing fee or oath</td><td></td></tr> <tr><td>127 50</td><td>227 25</td><td>Surcharge - late provisional filing fee or cover sheet</td><td></td></tr> <tr><td>139 130</td><td>139 130</td><td>Non-English specification</td><td></td></tr> <tr><td>147 2,520</td><td>147 2,520</td><td>For filing a request for reexamination</td><td></td></tr> <tr><td>112 920*</td><td>112 920*</td><td>Requesting publication of SIR prior to Examiner action</td><td></td></tr> <tr><td>113 1,840*</td><td>113 1,840*</td><td>Requesting publication of SIR after Examiner action</td><td></td></tr> <tr><td>115 110</td><td>215 55</td><td>Extension for reply within first month</td><td></td></tr> <tr><td>116 380</td><td>216 190</td><td>Extension for reply within second month</td><td></td></tr> <tr><td>117 870</td><td>217 435</td><td>Extension for reply within third month</td><td></td></tr> <tr><td>118 1,360</td><td>218 680</td><td>Extension for reply within fourth month</td><td></td></tr> <tr><td>128 1,850</td><td>228 925</td><td>Extension for reply within fifth month</td><td></td></tr> <tr><td>119 300</td><td>219 150</td><td>Notice of Appeal</td><td></td></tr> <tr><td>120 300</td><td>220 150</td><td>Filing a brief in support of an appeal</td><td></td></tr> <tr><td>121 260</td><td>221 130</td><td>Request for oral hearing</td><td></td></tr> <tr><td>138 1,510</td><td>138 1,510</td><td>Petition to institute a public use proceeding</td><td></td></tr> <tr><td>140 110</td><td>240 55</td><td>Petition to revive - unavoidable</td><td></td></tr> <tr><td>141 1,210</td><td>241 605</td><td>Petition to revive - unintentional</td><td></td></tr> <tr><td>142 1,210</td><td>242 605</td><td>Utility issue fee (or reissue)</td><td></td></tr> <tr><td>143 430</td><td>243 215</td><td>Design issue fee</td><td></td></tr> <tr><td>144 580</td><td>244 290</td><td>Plant issue fee</td><td></td></tr> <tr><td>122 130</td><td>122 130</td><td>Petitions to the Commissioner</td><td></td></tr> <tr><td>123 50</td><td>123 50</td><td>Petitions related to provisional applications</td><td></td></tr> <tr><td>126 240</td><td>126 240</td><td>Submission of Information Disclosure Stmt</td><td></td></tr> <tr><td>581 40</td><td>581 40</td><td>Recording each patent assignment per property (times number of properties)</td><td></td></tr> <tr><td>146 690</td><td>246 345</td><td>Filing a submission after final rejection (37 CFR § 1.129(a))</td><td></td></tr> <tr><td>149 690</td><td>249 345</td><td>For each additional invention to be examined (37 CFR § 1.129(b))</td><td></td></tr> <tr><td colspan="3">Other fee (specify) _____</td><td></td></tr> <tr><td colspan="3">Other fee (specify) _____</td><td></td></tr> <tr> <td colspan="2" style="text-align: right;">SUBTOTAL (3) (\$)</td> <td colspan="2" style="text-align: center;">0</td> </tr> </tbody> </table>	Large Entity Fee Code (\$)	Small Entity Fee Code (\$)	Fee Description	Fee Paid	105 130	205 65	Surcharge - late filing fee or oath		127 50	227 25	Surcharge - late provisional filing fee or cover sheet		139 130	139 130	Non-English specification		147 2,520	147 2,520	For filing a request for reexamination		112 920*	112 920*	Requesting publication of SIR prior to Examiner action		113 1,840*	113 1,840*	Requesting publication of SIR after Examiner action		115 110	215 55	Extension for reply within first month		116 380	216 190	Extension for reply within second month		117 870	217 435	Extension for reply within third month		118 1,360	218 680	Extension for reply within fourth month		128 1,850	228 925	Extension for reply within fifth month		119 300	219 150	Notice of Appeal		120 300	220 150	Filing a brief in support of an appeal		121 260	221 130	Request for oral hearing		138 1,510	138 1,510	Petition to institute a public use proceeding		140 110	240 55	Petition to revive - unavoidable		141 1,210	241 605	Petition to revive - unintentional		142 1,210	242 605	Utility issue fee (or reissue)		143 430	243 215	Design issue fee		144 580	244 290	Plant issue fee		122 130	122 130	Petitions to the Commissioner		123 50	123 50	Petitions related to provisional applications		126 240	126 240	Submission of Information Disclosure Stmt		581 40	581 40	Recording each patent assignment per property (times number of properties)		146 690	246 345	Filing a submission after final rejection (37 CFR § 1.129(a))		149 690	249 345	For each additional invention to be examined (37 CFR § 1.129(b))		Other fee (specify) _____				Other fee (specify) _____				SUBTOTAL (3) (\$)		0	
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SUBMITTED BY		Complete (if applicable)	
Name (Print/Type)	Brent P. Johnson	Registration No. (Attorney/Agent)	38,031
Signature		Telephone	303-689-9100
		Date	8/15/00

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re the Continuation-in-Part)
Application of)
)
Edwin L. Adair, Jeffrey L. Adair,)
Randall S. Adair)
)
Parent Application:)
Serial No.: 09/496,312)
Filed: February 1, 2000;)
)
For: "Hand-held Computers)
Incorporating Reduced Area)
Imaging Devices")

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Assistant Commissioner for Patents
Washington, DC 20231

Sir:

"EXPRESS MAIL" mailing label number EL547144479US

Date of Deposit: 8/15/00

I hereby certify that the following:

- Specification - 32 pages
- Twelve (12) formal drawing sheets
- Utility Patent Application Transmittal
- Fee transmittal (1 original and 1 copy)
- Declaration and Power of Attorney
- Small Entity Statement - Independent Inventors
- Declaration Accompanying Petition Under 37 CFR 1.102
- Petition to Make Special Under 37 CFR 1.102
- Check for \$ 1,230.00
- Return postcard

are being deposited with the United States Postal Service "Express Mail
Post Office to Addressee" service under 37 CFR 1.10 on the date indicated

Katherine L. Goncalves
8480 East Orchard Road, Suite 5600
Englewood, CO 80111
(303) 689-9100

Date: 8/15/00

**HAND-HELD COMPUTERS INCORPORATING
REDUCED AREA IMAGING DEVICES**

This application is a continuation-in-part of U.S. Serial No.
09/496,312, filed February 1, 2000, and entitled "Reduced Area Imaging
5 Devices", which is a continuation application of U.S. Serial No.
09/175,685, filed October 20, 1998 and entitled "Reduced Area Imaging
Devices", now U.S. Patent No. 6,043,839, which is a continuation-in-part
of U.S. Serial No. 08/944,322, filed October 6, 1997 and entitled "Reduced
Area Imaging Devices Incorporated Within Surgical Instruments", now
10 U.S. Patent No. 5,929,901.

Technical Field

This invention relates to solid state image sensors and associated
electronics, and more particularly, to solid state image sensors which are
configured to be of a minimum size and used within miniature computer
15 systems known as palm top computers, personal digital assistants (PDA),
or hand-held computers/organizers.

Background Art

The three most common solid state image sensors include charged
coupled devices (CCD), charge injection devices (CID) and photo diode
20 arrays. In the mid-1980s, complementary metal oxide semiconductors
(CMOS) were developed for industrial use. CMOS imaging devices offer
improved functionality and simplified system interfacing. Furthermore,
many CMOS imagers can be manufactured at a fraction of the cost of other
solid state imaging technologies.

25 The CCD device is still the preferred type of imager used in
scientific applications. Only recently have CMOS-type devices been
improved such that the quality of imaging compares to that of CCD

2

devices. However, there are enormous drawbacks with CCD devices. Two major drawbacks are that CCD device have immense power requirements, and the amount of processing circuitry required for a CCD imager always requires the use of a remote processing circuitry module which can process the image signal produced by the CCD imager. Also, because of the type of chip architecture used with CCD devices, on-chip processing is impossible. Therefore, even timing and control circuitry must be remoted from the CCD imager plane. Therefore, CCD technology is the antithesis of "camera on a chip" technology discussed below.

One particular advance in CMOS technology has been in the active pixel-type CMOS imagers which consist of randomly accessible pixels with an amplifier at each pixel site. One advantage of active pixel-type imagers is that the amplifier placement results in lower noise levels. Another major advantage is that these CMOS imagers can be mass produced on standard semiconductor production lines. One particularly notable advance in the area of CMOS imagers including active pixel-type arrays is the CMOS imager described in U.S. Patent No. 5,471,515 to Fossum, et al. This CMOS imager can incorporate a number of other different electronic controls that are usually found on multiple circuit boards of much larger size. For example, timing circuits, and special functions such as zoom and anti-jitter controls can be placed on the same circuit board containing the CMOS pixel array without significantly increasing the overall size of the host circuit board. Furthermore, this particular CMOS imager requires 100 times less power than a CCD-type imager. In short, the CMOS imager disclosed in Fossum, et al. has enabled the development of a "camera on a chip."

Passive pixel-type CMOS imagers have also been improved so that they too can be used in an imaging device which qualifies as a "camera on a chip." In short, the major difference between passive and active CMOS pixel arrays is that a passive pixel-type imager does not perform signal amplification at each pixel site. One example of a manufacturer which has developed a passive pixel array with performance nearly equal to known active pixel devices and compatible with the read out circuitry disclosed in the U.S. Patent No. 5,471,515 is VLSI Vision, Ltd., 1190 Saratoga Avenue, Suite 180, San Jose, California 95129. A further description of this passive pixel device may be found in co-pending application, Serial No. 08/976,976, entitled "Reduced Area Imaging Devices Incorporated Within Surgical Instruments," now U.S. Patent No. 5,986,693, and is hereby incorporated by reference.

In addition to the active pixel-type CMOS imager which is disclosed in U.S. Patent No. 5,471,515, there have been developments in the industry for other solid state imagers which have resulted in the ability to have a "camera on a chip." For example, Suni Microsystems, Inc. of Mountain View, California, has developed a CCD/CMOS hybrid which combines the high quality image processing of CCDs with standard CMOS circuitry construction. In short, Suni Microsystems, Inc. has modified the standard CMOS and CCD manufacturing processes to create a hybrid process providing CCD components with their own substrate which is separate from the P well and N well substrates used by the CMOS components. Accordingly, the CCD and CMOS components of the hybrid may reside on different regions of the same chip or wafer. Additionally, this hybrid is able to run on a low power source (5 volts) which is normally not possible on standard CCD imagers which require 10 to 30 volt power supplies. A

brief explanation of this CCD/CMOS hybrid can be found in the article entitled "Startup Suni Bets on Integrated Process" found in *Electronic News*, January 20, 1997 issue. This reference is hereby incorporated by reference for purposes of explaining this particular type of imaging processor.

Another example of a recent development in solid state imaging is the development of a CMOS imaging sensor which is able to achieve analog to digital conversion on each of the pixels within the pixel array. This type of improved CMOS imager includes transistors at every pixel to provide digital instead of analog output that enable the delivery of decoders and sense amplifiers much like standard memory chips. With this new technology, it may, therefore, be possible to manufacture a true digital "camera on a chip." This CMOS imager has been developed by a Stanford University joint project and is headed by Professor Abbas el-Gamal.

A second approach to creating a CMOS-based digital imaging device includes the use of an over-sample converter at each pixel with a one bit comparator placed at the edge of the pixel array instead of performing all of the analog to digital functions on the pixel. This new design technology has been called MOSAD (multiplexed over sample analog to digital) conversion. The result of this new process is low power usage, along with the capability to achieve enhanced dynamic range, possibly up to 20 bits. This process has been developed by Amain Electronics of Simi Valley, California. A brief description of both of the processes developed by Stanford University and Amain Electronics can be found in an article entitled "A/D Conversion Revolution for CMOS Sensor?," September 1998 issue of *Advanced Imaging*. This article is also

hereby incorporated by reference for purposes of explaining these particular types of imaging processors.

Yet another example of a recent development with respect to solid state imaging is an imaging device developed by ShellCase, of Jerusalem, Israel. In an article entitled "A CSP Optoelectronic Package for Imaging and Light Detection Applications" (A. Badihi), ShellCase introduces a die-sized, ultrathin optoelectronic package which is completely packaged at the wafer level using semiconductor processing. In short, ShellCase provides a chip scale package (CSP) process for accepting digital image sensors which may be used, for example, in miniature cameras. The die-sized, ultrathin package is produced through a wafer level process which utilizes optically clear materials and completely encases the imager die. This packaging method, ideally suited for optoelectronic devices, results in superior optical performance and form factor not available by traditional image sensors. This article is also incorporated by reference for purposes of explaining ShellCase's chip scale package process.

Yet another example of a recent development with respect to solid state imaging is shown in U.S. Patent No. 6,020,581 entitled "Solid State CMOS Imager Using Silicon on Insulator or Bulk Silicon." This patent discloses an image sensor incorporating a plurality of detector cells arranged in an array wherein each detector cell as a MOSFET with a floating body and operable as a lateral bipolar transistor to amplify charge collected by the floating body. This invention overcomes problems of insufficient charge being collected in detector cells formed on silicon on insulator (SOI) substrates due to silicon thickness and will also work in bulk silicon embodiments.

The above-mentioned developments in solid state imaging technology have shown that "camera on a chip" devices will continue to be enhanced not only in terms of the quality of imaging which may be achieved, but also in the specific construction of the devices which may be manufactured by new breakthrough processes.

Although the "camera on a chip" concept is one which has great merit for application in many industrial areas, a need still exists for a reduced area imaging device which can be used in even the smallest type of industrial application. Recently, devices known as palm top computers, PDA(s), or hand-held computers have become very popular items. Essentially, these PDAs are miniature computers, small enough to be held in the hand, which have various software programs available to a user including word processing, e-mail, and organization software for addresses/phone books, etc.

One example of a U.S. patent disclosing a type of a PDA includes U.S. Patent No. 5,900,875. This patent is incorporated herein by reference for purposes of illustrating an example of a PDA including basic functionality for such a device. In a recent article entitled "Palm, Inc. Gets Ready for New Hands" appearing in the *Wallstreet Journal*, a number of soon to be commercially available PDAs are disclosed. One such device disclosed in this article is known as the "Hand Spring Visor Deluxe." This device will soon be available which allows a user to accommodate pagers, MP3 players, still digital cameras and other devices.

It is one general object of this invention to provide a video system in combination with a standard PDA enabling a user to take video images by a very small camera module incorporated within the PDA, view the video images taken on a video viewscreen incorporated within the PDA, and to

have the capability to store , download the video images, and send the video images electronically through a communications network.

Another object of this invention is to provide a PDA with the ability to not only transmit video images taken by the camera module, but also to
5 receive video images sent from a remote location via the communications network, and to view such received video images on the video view screen of the PDA. Accordingly, the invention is ideally suited for video teleconferencing.

It is another object of this invention to provide a reduced area
10 imaging device incorporated within a PDA which takes advantage of "camera on a chip" technology, but to rearrange the video processing circuitry in a selective stacked relationship so that the camera module has a minimum profile.

It is yet another object of this invention to provide imaging
15 capability for a PDA wherein the video camera used is of such small size that it can be stored in the PDA when not in use. The camera module is attached to the PDA by a retractable cord which enables the imaging device to be used to image anything at which the camera module is pointed by the user without having to also move the PDA away from the view of the user.

20 In all applications, to include use of the imaging device of this invention with a PDA, "camera on a chip" technology can be improved with respect to reducing its profile area, and incorporating such a reduced area imaging device within a PDA such that minimal size and weight is added to the PDA, and further that the imaging device can be used to image
25 selected targets by the user.

Disclosure of the Invention

In accordance with the present invention, reduced area imaging devices are provided in combination with a hand-held computer or PDA. The term "imaging device" as used herein describes the imaging elements and processing circuitry which is used to produce a video signal which may be accepted by both a standard video device such as a television or video monitor accompanying a personal computer, and a small LCD screen which is incorporated within the PDA. The term "image sensor" as used herein describes the components of a solid state imaging device which captures images and stores them within the structure of each of the pixels in the array of pixels found in the imaging device. As further discussed below, the timing and control circuits can be placed either on the same planar structure as the pixel array, in which case the image sensor can also be defined as an integrated circuit, or the timing and control circuitry can be placed remote from the pixel array. The terms "video signal" or "image signal" as used herein, and unless otherwise more specifically defined, refer to an image which at some point during its processing by the imaging device, is found in the form of electrons which have been placed in a specific format or domain. The term "processing circuitry" as used herein refers to the electronic components within the imaging device which receive the image signal from the image sensor and ultimately place the image signal in a usable format. The terms "timing and control circuits" or "timing and control circuitry" as used herein refer to the electronic components which control the release of the image signal from the pixel array.

In a first arrangement, the image sensor, with or without the timing and control circuitry, may be placed at the distal tip of a very small camera

module which is attached by a cable or cord to the PDA, while the remaining processing circuitry may be placed within the housing of the PDA.

In a second arrangement, the image sensor and the processing
5 circuitry may all be placed in a stacked arrangement of miniature circuit boards or planar circuit structures and positioned at the distal tip of the camera module. In this second arrangement, the pixel array of the image sensor may be placed by itself on its own circuit board while the timing and control circuitry and processing circuitry are placed on one or more other
10 circuit boards, or the circuitry for timing and control may be placed with the pixel array on one circuit board, while the remaining processing circuitry can be placed on one or more of the other circuit boards.

In yet another alternative arrangement, the pixel array, timing and control circuits, and some of the processing circuitry can be placed near the
15 distal end of the camera module on two or more circuit boards with the remaining part of the processing circuitry being placed in the housing of the PDA.

For the arrangement or configuration of the imaging device which calls for the array of pixels and the timing and control circuitry to be placed
20 on the same circuit board, only one conductor is required in order to transmit the image signal to the video processing circuitry. When the timing and control circuits are incorporated onto other circuit boards, a plurality of connections are required in order to connect the timing and control circuitry to the pixel array, and then the one conductor is also
25 required to transmit the image signal back to the video processing circuitry.

As mentioned above, the invention disclosed herein can be considered an improvement to a PDA wherein the improvement comprises

a video system. The video system would include the video view screen or monitor attached to the PDA, the camera module, as well as supporting video processing circuitry for the imaging device. In yet another aspect, the invention disclosed herein can also be considered an improvement to a PDA wherein the improvement comprises a novel imaging device, preferably of CMOS construction. For this improvement comprising the imaging device, the imaging device includes the array of pixels, and the supporting video processing circuitry for providing a video ready signal.

This video ready signal may be formatted by the video processing circuitry for viewing on a NTSC/PAL compatible device such as television, or for viewing on a VGA compatible device such as a monitor of a personal computer. Of course, the video ready signal is formatted for viewing the video images on the video view screen incorporated within the PDA.

In yet another aspect, the invention disclosed herein can also be considered an improvement to a PDA wherein the improvement comprises a combination of a video system, and wireless telephone communication means for transmitting and receiving both audio and video signals. In this aspect, the invention has functionality for transmitting and receiving audio and video signals via the communications network. One example of a U.S. patent disclosing wireless remote communications between a personal computer and a PDA or miniature hand held computer is U.S. Patent No. 6,034,621. This patent is hereby incorporated by reference in its entirety for purposes of disclosing means by which data can be exchanged between the hand held computer and a personal computer, to include video and audio signals. The specific example in this patent which readily lends itself to the communication network incorporated within this invention is found

at Figure 4 of this '621 patent. The discussion further below outlines this particular communication network.

In yet another aspect, the invention disclosed herein can also be considered an improvement to a PDA wherein the improvement comprises a video system, and a standard wireless telephone communication means for transmitting and receiving audio signals. In this aspect, the PDA simply includes a standard wireless/cellular phone connected externally on the PDA which enables the user to conduct well-known wireless/ telephone communications. This wireless/cellular communication means can be in addition to the wireless telephone communication means for transmitting and receiving both audio and video signals discussed immediately above with respect to the U.S. Patent No. 6,034,621.

Another example of a U.S. patent disclosing basic mobile phone technology including a discussion of basic phone circuitry is U.S. Patent No. 6,018,670. This patent is hereby incorporated by reference in its entirety for purposes of disclosing standard or basic mobile phone technology and supporting circuitry.

Accordingly, the invention disclosed herein has utility with respect to an overall combination of elements, as well as various sub-combination of elements.

Brief Description of the Drawings

Figure 1 is an enlarged fragmentary partially exploded perspective view of the distal end of the camera module which is used in conjunction with the PDA, specifically illustrating the arrangement of the image sensor with respect to the other elements of the camera module;

Figure 1a is an enlarged exploded perspective view illustrating another configuration of the image sensor wherein video processing circuitry is placed behind and in longitudinal alignment with the image sensor;

5 Figure 2 is a perspective view of the PDA incorporating the reduced area imaging device of this invention;

Figure 3 illustrates the PDA of Figure 2 wherein the camera module is in the retracted position;

10 Figure 4 is an overall schematic diagram of the functional electronic components which make up both the PDA and the reduced area imaging device wherein communications are achieved by wireless/cellular technology for video teleconferencing via the world wide web which is well-known as a global communications network;

15 Figure 5 is a schematic diagram illustrating an example communications network which can be used for data transfer of text, audio, and visual signals between the PDA and a personal computer which is in communication with the world wide web;

Figure 6a is a perspective view of the PDA in combination with an externally attached wireless/cellular phone;

20 Figure 6b is another perspective view of the combination of Figure 6a illustrating the combination opened to expose the PDA;

Figure 7 is a more detailed schematic diagram of the functional electronic components which make up the imaging device;

25 Figure 7a is an enlarged schematic diagram of a circuit board/planar structure which may include the array of pixels and the timing and control circuitry;

Figure 7b is an enlarged schematic diagram of a video processing board/planar structure having placed thereon the processing circuitry which processes the pre-video signal generated by the array of pixels and which converts the pre-video signal to a post-video signal which may be accepted
5 by an NTSC/PAL compatible video device; and

Figures 8a-8e are schematic diagrams that illustrate an example of specific circuitry which may be used to make the video processing circuitry of the imaging device.

Best Mode for Carrying Out the Invention

10 In accordance with the invention, as shown in Figure 1, a camera module 10 is provided which incorporates a reduced area imaging device 11. As further discussed below, the elements of the imaging device 11 may all be found near one location, or the elements may be separated from one another and interconnected by the appropriate wired connections. The
15 array of pixels making up the image sensor captures images and stores them in the form of electrical energy by conversion of light photons to electrons. This conversion takes place by the photo diodes in each pixel which communicate with one or more capacitors which store the electrons. Specifically, the camera module 10 includes an outer tube/sheath 14 which
20 houses the components of the imaging device. The camera module is shown as being cylindrical in shape having a window 16 sealed at the distal end of the camera module. A retractable cable 12 extends from the proximal end of the camera module 10. A shielded cable 21 is used to house the conductors which communicate with the imaging device 11. The
25 shielded cable 21 is then housed within the retractable cable 12. A lens group 18 is positioned at the distal end of the camera module to enable an

image to be appropriately conditioned prior to the image impinging upon the imaging device 11. Also shown is a focusing ring 20 which enables the lens group 18 to be displaced distally or proximally to best focus an image on the imaging device 11.

5 Now referring to Figures 2 and 3, a PDA 22 is shown which incorporates the camera module 10. In basic terms, the PDA 22 is a miniature hand-held computer incorporating a video system enabling video to be taken by the camera module, and viewed on the video view screen 26, as well as enabling images to be stored and downloaded on a miniature
10 computer disc (not shown) used with the PDA. Also discussed further below is the ability to transmit and receive audio and video signals.

Beginning first with a description of the basic components of the PDA 22, it includes a housing 24 which hold the components of the PDA and the video system. Cable 12 is housed within the housing 24 when in
15 the retracted position. A spring biased spool (not shown) or some other known retracting device is mounted within the housing 24 enabling the cable 12 to be extended or retracted. A plurality of controls are provided enabling the user to manipulate the functions of the PDA. These are shown as buttons 34 on the housing 24. The video view screen 26 is used for
20 displaying video images taken by the camera module 10, or for viewing incoming video signals received from a remote location. A command screen 28 is provided which allows a user to select programs with a stylus (not shown). A video capture button 30 is provided which allows a user to capture a still video image taken by the camera module 10. A video store
25 button 32 is also provided which enables a captured video image to be stored within the digital memory of the PDA, as further discussed below. An opening or cavity 35 is provided which allows the camera module 10 to

be stored, along with cable 12 within the housing 24. As shown in Figure 3, the camera module 10 is in the stored or retracted position. The antenna 36 allows for enhanced transmission and reception of incoming or transmitted/outgoing audio and video signals. A video select switch 37 is provided enabling a user to view either video images taken by the camera module 10, or for viewing incoming video images. The video view screen 26 may be a liquid crystal display (LCD) type, or any other well-known display device of high resolution which has low power requirements, and has minimum size requirements as well.

An example of a manufacture of such a miniature LCD monitor includes DISPLAYTECH of Longmont, Colorado. DISPLAYTECH manufactures a miniature reflective display that consists of ferroelectric liquid crystal (FLC) applied to a CMOS integrated circuit. The reflective display is a VGA display panel having low voltage digital operation, low power requirements, and full color operation. One of their specific products includes the LightCaster™ VGA Display Panel, Model LDP-0307-MV1. This is but one example of an LCD monitor which is available and usable within the invention herein described.

A camera on/off switch 66 is provided enabling the user to turn the video system on or off. Also shown in Figures 2 and 3 is a speaker 76 and a microphone 78 which are used for sending and receiving audio signals in the conventional manner as with a wireless/cellular telephone. A further description of speaker 76 and microphone 78 is found below.

Referring back to Figures 1 and 1a, the imaging device 11 includes an image sensor 40. Figure 1 illustrates that the image sensor 40 can be a planar and square shaped member, or alternatively, planar and circular shaped to better fit within outer tube 14. In the configuration of the

16

imaging device in Figures 1 and 1a, there are only three conductors which are necessary for providing power to the image sensor 40, and for transmitting an image from the image sensor 40 back to the processing circuitry found within the phone housing 24. Specifically, there is a power conductor 44, a grounding conductor 46, and an image signal conductor 48, each of which are hardwired to the image sensor 40. Thus, shielded cable 21 may simply be a three conductor, 50 ohm type cable.

~~Image sensor 40 can be as small as 1 mm in its largest dimension~~

However, a more preferable size for most PDA applications would be between 4 mm to 8 mm in the image sensor's largest dimension (height or width). The image signal transmitted from the image sensor 40 through conductor 48 is also herein referred to as a pre-video signal. Once the pre-video signal has been transmitted from image sensor 40 by means of conductor 48, it is received by video processing board 50, as shown in Figure 6b. Video processing board 50 then carries out all the necessary conditioning of the pre-video signal and places it in a form, also referred to herein as a video ready signal, so that it may be viewed directly on a remote video device such as a television or standard computer video monitor. In order for the pre-video signal to be viewed on the video view screen/monitor 26, the pre-video signal is further conditioned by a digital signal processor 72, as further discussed below. The video signal produced by the video processing board 50 can be viewed by an NTSC/PAL compatible video device (such as a television) which connects to the PDA through a remote jack. This video signal produced by board 50 can be further defined as a post-video signal.

Figure 1 illustrates an arrangement wherein the image sensor 40 is placed by itself adjacent the distal end of the camera module 10.

Alternatively, some or all of the video processing circuitry may be placed in adjacent circuit boards directly behind the image sensor 40.

Accordingly, 1a illustrates video processor board 50 aligned directly behind the image sensor 40. A plurality of pin connectors 52 can be used
5 to interconnect image sensor 40 to video processor board 50. Depending upon the specific configuration of image sensor 40, pin connectors 52 may be provided for structural support only, and/or to provide a means by which image signals are transmitted between image sensor 40 and board 50.

Additionally, digital signal processor 72 could also be placed behind image
10 sensor 40 and behind video processing board 50. Accordingly, the image sensor, and all supporting video processing circuitry could be placed at the distal end of the camera module 10. However, because of the ample space within housing 24, it may be preferable to place at least some of the video processing circuitry within housing 24. In the case of Figure 1a, the
15 conductor 49 represents the conductor which may carry the post-video signal for direct connection with a remote video device 60 such as a television or computer monitor. As also discussed further below, placement of the digital signal processor 72 at the distal tip of the camera module behind the video processing board 50 would also enable yet
20 another conductor (not shown) to connect directly to the video monitor 26 for transmitting a video signal to the video monitor 26.

Again referring to Figures 1 and 1a, the area which is occupied by image sensor 40 may be defined as the profile area of the imaging device and which determines its critical dimensions. If it is desired to place video
25 processing circuitry adjacent the image sensor 40 at the distal end of the camera module 10, such circuitry must be able to be placed on one or more circuit boards which are longitudinally aligned with image sensor 40 along

longitudinal axis XX. If it is not important to limit the size of the profile area, then any circuitry placed behind image sensor 40 can be aligned in an offset manner, or may simply be larger than the profile area of image sensor 40. In the configuration shown in Figure 1a, it is desirable that elements 40 and 50 be approximately the same size so that they may uniformly fit within the distal end of outer tube 14.

Now referring to Figure 4, a further explanation is provided of the basic electronic components of the PDA 22. The PDA 22 of this invention includes functionality normally found in multiple devices. Specifically, the PDA 22 includes the computing capability of a PDA, a mobile/wireless phone, communication means for connection to a computer network such as the worldwide web, and a video system. The PDA 22 may be separated into two major groups, namely, a video and communication system 61, and a computer processing and memory unit 82. Both of these are discussed in further detail below.

As shown in Figure 4, a conventional lithium ion battery 62 is provided which communicates with power supply board 64. Power supply board 64 conditions various power outputs to the components of the device, to include power to the video components. In the preferred imaging device of this invention, the power to the imaging device may simply be direct current of between about 1.5 to 12 volts, depending upon the power requirements of the imaging device. A camera on/off switch 66 must be set to the "on" position in order to activate the camera module 10. The video processor board 50 then transfers power to supplies the camera module 10, and also receives the analog pre-video signal back from the camera module, as further discussed below. After processing of the pre-video signal at the video processor board 50, the video signal is video ready,

meaning that it may then be directly viewed on a remote compatible video device 60, such as a television or computer monitor. A video port 54 can be provided on the housing 24 enabling a user to take a standard video jack (not shown) and interconnect the PDA with the video port of the remote video device. The video format for such remote video devices includes NTSC/PAL and VGA; thus, the video signal processed by video processor board 50 creates the video ready signals for use with these remote video devices. For purposes of viewing images on the monitor 26, the pre-video signal is further processed into a digital format within video processor board 50, preferably an 8 bit component video signal format that is commonly referred to as "YUV 4:2:2." This video format easily lends itself to video compression. This 8 bit digital video signal is then sent to the digital signal processor 72 which performs two functions relevant to the video signal. The digital signal processor 72 further converts the signal into a format that is compatible with the driver circuitry of the video monitor 26. Secondly, the digital signal processor 72 compresses the YUV signal using a common video compression format, preferably JPEG. The JPEG encoded video signal is then mixed with the audio signal created by microphone 78 and amplifier 74, and the resulting high frequency carrier signal may then be passed onto the transceiver/amplifier section 70 for transmission. It is to be understood that the transceiver/amplifier 70 is intended for communication with well-known wide area wireless communication networks. It is also contemplated within the spirit and scope of this invention that the PDA 22 be capable of communication with computer networks to include the worldwide web. Accordingly, the invention is well adapted for conducting video teleconferencing which is normally conducted with desktop computers and supplemental video

equipment. The transceiver/amplifier section also modulates the carrier signal prior to transmission. Depending upon the position of video switch 37, the video signal from digital signal processor 72 is either sent to the monitor 26, or is sent to the transceiver/amplifier section 70 for transmission. As also shown, the antenna 36 is used for enhancement of reception and transmission of transmitted and received carrier signals.

The transceiver/amplifier section 70 also serves as a receiver which receives an incoming carrier signal. This incoming signal is then demodulated within section 70, the video and audio components of the incoming signal are separated, and then these separated signals are then sent to the digital signal processor 72 which performs video decompression. Then, the decompressed video signal is sent to the monitor 26 for viewing (if the video switch 37 is placed in that selected mode). The decompressed audio signal is sent to the amplifier 74, and then to the speaker 76.

Figure 4 shows the transceiver/amplifier section 70 as being a cellular digital packet data system (CDPD) type transceiver. This particular transceiver/amplifier 70 could be the same as that disclosed in the U.S. Patent No. 6,034,621. A cellular digital packet system is a wireless standard providing two-way, 19.2 kbps packet data transmission over existing cellular telephone channels.

The video switch 37 may simply be a momentary, spring loaded, push button-type switch. When the video switch 37 is not depressed, incoming video, which is received via the antenna 36, is processed as discussed above in the transceiver/amplifier section 70 and digital signal processor 72, and then sent to the monitor 26. When the video switch 37 is depressed and held, the video signal produced from the camera module 10

is processed as discussed above, and ultimately sent to the monitor 26 for viewing by the user. An operator can cycle the switch 37 between the two positions in order to selectively choose whether to view incoming or outgoing video.

5 Figure 5 illustrates a communications network which can be used by the invention. A communications network of this type is disclosed in the U.S. Patent No. 6,034,621, and is discussed specifically therein at Figures 3 and 4 of that patent. Figure 5 illustrates a CDPD base station 182 with a remote computer 188 utilizing a direct connection to the CDPD base station
10 182 via a modem 186 with a dial-up connection to the public switch telephone network (PSTN) 184. The CDPD base station 182 includes an antenna 181. The remote computer 188 can be a personal computer, a server, or any other well-known stand-alone computer.

Referring back to Figure 4, the computer processing and memory
15 unit 82 which allows the PDA 22 to achieve basic word processing, etc., includes a microprocessor 83, RAM 84, ROM 86, and digital storage 88. Digital storage 88 is provided for storing the formatted images taken by the camera module 10. The RAM 84, microprocessor 83, and ROM 86 are conventional or standard components as found in existing PDAs. An
20 input/output bus 89 is provided which allows video signals to be stored or otherwise manipulated within the computer processing and memory unit 82. Accordingly, video taken by camera module 10 can be downloaded to digital storage 88. Also, existing image data stored in digital storage 88 could be viewed on video monitor 26.

25 Figures 6a and 6b illustrate another combination of the invention wherein the PDA 22 is simply combined with an externally mounted cellular telephone 190. The cellular phone 190 is a commercially available

cellular/wireless telephone. As shown, the telephone includes the standard keypad 194, visual display 196, and antennae 198. The phone 190 is secured to the PDA 22 as by mounting means 192, which is shown in the preferred embodiment as a piano-type hinge. Thus, the PDA is altered very simply by providing means by which a cellular telephone can be attached to the PDA. This enables the user to hold both the PDA and cellular telephone in one hand while manipulating the PDA or phone 190 as desired with the other hand. All of the telephone circuitry for phone 190 is housed within the phone itself, and there is no circuitry within the PDA which is used within the phone 190.

The actual size of the phone 190 is smaller than the PDA 22. However, in order to create a uniform edged combination, the phone 190 is housed in a larger housing 200 which essentially matches the dimensions of housing 24. Additionally, a peripheral flange could be provided on the inner surface of housing 200 which comes into contact with housing 24 in the closed position of Figure 6a which would prevent inadvertent activation of the control buttons on the PDA 22.

Figure 7 is a schematic diagram illustrating one way in which the imaging device 11 may be constructed. As illustrated, the image sensor 40 may include the timing and control circuits on the same planar structure. Power is supplied to image sensor 40 by power supply board 64. The connection between image sensor 40 and board 64 may simply be a cable having two conductors therein, one for ground and another for transmitting the desired voltage. These are illustrated as conductors 44 and 46. The output from image sensor 40 in the form of the pre-video signal is input to video processor board 50 by means of the conductor 48. In the configuration of Figure 7, conductor 48 may simply be a 50 ohm

conductor. Power and ground also are supplied to video processing board 50 by conductors 44 and 46 from power supply board 52. The output signal from the video processor board 50 is in the form of the post-video signal and which may be carried by conductor 49 which can also be a 50 ohm conductor.

Although Figure 7 illustrates the image sensor and the timing and control circuits being placed on the same circuit board or planar structure, it is possible to separate the timing and control circuits from the pixel array and place the timing and control circuits onto video processing board 50.

10 The advantage in placing the timing and control circuits on the same planar structure as the image sensor is that only three connections are required between image sensor 40 and the rest of the imaging device, namely, conductors 44, 46 and 48. Additionally, placing the timing and control circuits on the same planar structure with the pixel array results in the pre-

15 video signal having less noise. Furthermore, the addition of the timing and control circuits to the same planar structure carrying the image sensor only adds a negligible amount of size to one dimension of the planar structure. If the pixel array is to be the only element on the planar structure, then additional connections must be made between the planar structure and the

20 video processing board 50 in order to transmit the clock signals and other control signals to the pixel array. For example, a ribbon-type cable (not shown) or a plurality of 50 ohm coaxial cables (not shown) must be used in order to control the downloading of information from the pixel array. Each of these additional connections would be hard wired between the boards.

25 Figure 7a is a more detailed schematic diagram of image sensor 40 which contains an array of pixels 90 and the timing and control circuits 92. One example of a pixel array 90 which can be used within the invention is

similar to that which is disclosed in U.S. Patent No. 5,471,515 to Fossum, et al., said patent being incorporated by reference herein. More specifically, Figure 3 of Fossum, et al. illustrates the circuitry which makes up each pixel in the array of pixels 90. The array of pixels 90 as described in Fossum, et al. is an active pixel group with intra-pixel charged transfer. The image sensor made by the array of pixels is formed as a monolithic complementary metal oxide semiconductor (CMOS) integrated circuit which may be manufactured in an industry standard complementary metal oxide semiconductor process. The integrated circuit includes a focal plane array of pixel cells, each one of the cells including a photo gate overlying the substrate for accumulating the photo generated charges. In broader terms, as well understood by those skilled in the art, an image impinges upon the array of pixels, the image being in the form of photons which strike the photo diodes in the array of pixels. The photo diodes or photo detectors convert the photons into electrical energy or electrons which are stored in capacitors found in each pixel circuit. Each pixel circuit has its own amplifier which is controlled by the timing and control circuitry discussed below. The information or electrons stored in the capacitors is unloaded in the desired sequence and at a desired frequency, and then sent to the video processing board 50 for further processing.

Although the active pixel array disclosed in U.S. Patent No. 5,471,515 is mentioned herein, it will be understood that the hybrid CCD/CMOS described above, or any other solid state imaging device may be used wherein timing and control circuits can be placed either on the same circuit board or planar structure with the pixel array, or may be separated and placed remotely. Furthermore, it will be clearly understood that the invention claimed herein is not specifically limited to an image

sensor as disclosed in the U.S. Patent No. 5,471,515, but encompasses any image sensor which may be configured for use in conjunction with the other processing circuitry which makes up the imaging device of this invention.

5 To summarize the different options available in terms of arrangement of the components of the imaging device 11, the array of pixels 90 of the image sensor 40 may be placed alone on a first plane, or the timing and control circuitry 92 may be placed with the array of pixels 90 on the first plane. If the timing and control circuitry 92 is not placed
10 with the array of pixels 90 on the first plane, the timing and control circuitry 92 may be placed by itself on a second plane, or the timing and control circuitry 92 may be placed on a second plane with some or all of the processing circuitry from video processing board 50. The video processing board 50 itself may be placed on one or more planes on
15 corresponding circuit boards containing video processing circuitry. Figure 1a illustrates a single video processor board 50 located directly behind image sensor 40; however, it shall be understood that additional circuit boards containing additional circuitry may be placed behind the image sensor 40 and behind the video processing board 50. Some or all of the
20 video processing circuitry may be placed within the camera module 10 near the distal end thereof adjacent the image sensor 40. Video processing circuitry which is not placed within the distal end of the camera module 10 may be placed within the housing 24 of the PDA. If video processing circuitry is placed near the distal end of the camera module 10, it is
25 preferable to arrange the video processing circuitry in a stacked relationship behind the image sensor 40. Additionally, it is preferable to place the processing circuitry in a parallel arrangement with respect to

image sensor 40 and to center such video processing circuitry along axis X-X in order to minimize the size of camera module 10.

The timing and control circuits 92 are used to control the release of the image information or image signal stored in the pixel array. In the
5 image sensor of Fossum, et al., the pixels are arranged in a plurality of rows and columns. The image information from each of the pixels is first consolidated in a row by row fashion, and is then downloaded from one or more columns which contain the consolidated information from the rows. As shown in Figure 7a, the control of information consolidated from the
10 rows is achieved by latches 94, counter 96, and decoder 98. The operation of the latches, counter and decoder is similar to the operation of similar control circuitry found in other imaging devices. That is, a latch is a means of controlling the flow of electrons from each individual addressed pixel in the array of pixels. When a latch 94 is enabled, it will allow the transfer of
15 electrons to the decoder 98. The counter 96 is programmed to count a discrete amount of information based upon a clock input from the timing and control circuits 92. When the counter 96 has reached its set point or overflows, the image information is allowed to pass through the latches 94 and be sent to the decoder 98 which places the consolidated information in
20 a serial format. Once the decoder 98 has decoded the information and placed it in the serial format, then the row driver 100 accounts for the serial information from each row and enables each row to be downloaded by the column or columns. In short, the latches 94 will initially allow the information stored in each pixel to be accessed. The counter 96 then
25 controls the amount of information flow based upon a desired time sequence. Once the counter has reached its set point, the decoder 98 then knows to take the information and place it in the serial format. The whole

process is repeated, based upon the timing sequence that is programmed. When the row driver 100 has accounted for each of the rows, the row driver reads out each of the rows at the desired video rate.

The information released from the column or columns is also
5 controlled by a series of latches 102, a counter 104 and a decoder 106. As with the information from the rows, the column information is also placed in a serial format which may then be sent to the video processing board 50. This serial format of column information is the pre-video signal carried by conductor 48. The column signal conditioner 108 places the column serial
10 information in a manageable format in the form of desired voltage levels. In other words, the column signal conditioner 108 only accepts desired voltages from the downloaded column(s).

The clock input to the timing and control circuits 92 may simply be a quartz crystal timer. This clock input is divided into many other
15 frequencies for use by the various counters. The run input to the timing and control circuit 92 may simply be an on/off control. The default input can allow one to input the pre-video signal to a video processor board which may run at a frequency of other than 30 hertz. The data input controls functions such as zoom. At least for a CMOS type active pixel
20 array which can be accessed in a random manner, features such as zoom are easily manipulated by addressing only those pixels which locate a desired area of interest by the user.

A further discussion of the timing and control circuitry which may be used in conjunction with an active pixel array is disclosed in U.S. Patent
25 No. 5,471,515 and is also described in an article entitled "Active Pixel Image Sensor Integrated With Readout Circuits" appearing in *NASA Tech*

Briefs, October 1996, pp. 38 and 39. This particular article is also incorporated by reference.

Once image sensor 40 has created the pre-video signal, it is sent to the video processing board 50 for further processing. At board 50, as
5 shown in Figure 6b, the pre-video signal is passed through a series of filters. One common filter arrangement may include two low pass filters 114 and 116, and a band pass filter 112. The band pass filter only passes low frequency components of the signal. Once these low frequency components pass, they are then sent to detector 120 and white balance
10 circuit 124, the white balance circuit distinguishing between the colors of red and blue. The white balance circuit helps the imaging device set its normal, which is white. The portion of the signal passing through low pass filter 114 then travels through gain control 118 which reduces the magnitude or amplitude of this portion to a manageable level. The output
15 from gain control 118 is then fed back to the white balance circuit 124. The portion of the signal traveling through filter 116 is placed through the processor 122. In the processor 122, the portion of the signal carrying the luminance or non-chroma is separated and sent to the Y chroma mixer 132. Any chroma portion of the signal is held in processor 122.

20 Referring to the output of the white balance circuit 124, this chroma portion of the signal is sent to a delay line 126 where the signal is then further reduced by switch 128. The output of switch 128 is sent through a balanced modulator 130 and also to the Y chroma mixer 132 where the processed chroma portion of the signal is mixed with the processed non-
25 chroma portion. Finally, the output from the Y chroma mixer 132 is sent to the NTSC/PAL encoder 134, commonly known in the art as a "composite" encoder. The composite frequencies are added to the signal leaving the Y

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chroma mixer 132 in encoder 134 to produce the post-video signal which may be accepted by a television. Additionally, the signal from Y chroma mixer 132 is sent to the digital signal processor 72 so that images can be viewed on monitor 26.

5 In addition to the functions described above that are achieved by the digital signal processor 72, the processor 72 can also provide additional digital enhancements. Specifically, digital enhancement can sharpen or otherwise clarify the edges of an image viewed on a video screen which might normally be somewhat distorted. Additionally, selected background
10 or foreground images may be removed thus only leaving the desired group of images.

 In addition to digital enhancement, the digital signal processor 72 can include other circuitry which may further condition the signal received from board 50 so that it may be viewed in a desired format other than
15 NTSC/PAL. One common encoder which can be used would be an RGB encoder. An RGB encoder separates the signal into the three primary colors (red, green and blue). A SVHS encoder (super video home system) encoder could also be added to processor 72. This type of encoder splits or separates the luminance portion of the signal and the chroma portion of the
20 signal. Some observers believe that a more clear signal is input to the video device by such a separation, which in turn results in a more clear video image viewed on the video device. Another example of an encoder which could be added to processor 72 includes a VGA compatible encoder, which enables the video signal to be viewed on a standard VGA monitor
25 which is common to many computer monitors.

 One difference between the arrangement of image sensor 40 and the outputs found in Figure 3 of the Fossum, et al. patent is that in lieu of

providing two analog outputs [namely, VS out (signal) and VR out (reset)], the reset function takes place in the timing and control circuitry 92. Accordingly, the pre-video signal only requires one conductor 48.

Figures 8a-8e illustrate in more detail one example of circuitry which may be used in the video processing board 50 in order to produce a post-video signal which may be directly accepted by a NTSC/PAL compatible video device such as a television. The circuitry disclosed in Figures 8a-8e is very similar to circuitry which is found in a miniature quarter-inch Panasonic camera, Model KS-162. It will be understood by those skilled in the art that the particular arrangement of elements found in Figures 8a-8e are only exemplary of the type of video processing circuitry which may be incorporated in order to take the pre-video signal and condition it to be received by a desired video device.

As shown in Figure 8a, 5 volt power is provided along with a ground by conductors 44 and 46 to board 50. The pre-video signal carried by conductor 48 is buffered at buffer 137 and then is transferred to amplifying group 138. Amplifying group 138 amplifies the signal to a usable level as well as achieving impedance matching for the remaining circuitry.

The next major element is the automatic gain control 140 shown in Figure 8b. Automatic gain control 140 automatically controls the signal from amplifying group 138 to an acceptable level and also adds other characteristics to the signal as discussed below. More specifically, automatic gain control 140 conditions the signal based upon inputs from a 12 channel digital to analog converter 141. Converter 141 retrieves stored information from EEPROM (electrically erasable programmable read only memory) 143. EEPROM 143 is a non-volatile memory element which may

store user information, for example, settings for color, tint, balance and the like. Thus, automatic gain control 140 changes the texture or visual characteristics based upon user inputs. Housing 24 could also include buttons for controlling the image viewed on monitor 26 such as a gain control 140. The signal leaving the automatic gain control 140 is an analog signal until being converted by analog to digital converter 142.

Digital signal processor 144 of Figure 8c further processes the converted signal into a serial type digital signal. One function of the microprocessor 146 is to control the manner in which digital signal processor 144 sorts the digital signals emanating from converter 142. Microprocessor 146 also controls analog to digital converter 142 in terms of when it is activated, when it accepts data, when to release data, and the rate at which data should be released. Microprocessor 146 may also control other functions of the imaging device such as white balance. The microprocessor 146 may selectively receive the information stored in the EEPROM 143 and carry out its various commands to further control the other elements within the circuitry.

After the signal is processed by digital signal processor 144, the signal is sent to digital encoder 148 illustrated in Figure 8d. Some of the more important functions of digital encoder 148 are to encode the digital signal with synchronization, modulated chroma, blanking, horizontal drive, and the other components necessary so that the signal may be placed in a condition for reception by a video device such as a television monitor. As also illustrated in Figure 8d, once the signal has passed through digital encoder 148, the signal is reconverted into an analog signal through digital to analog converter 150.

This reconverted analog signal is then buffered at buffers 151 and then sent to amplifier group 152 of Figure 8e which amplifies the signal so that it is readily accepted by a desired video device. Specifically, as shown in Figure 8e, one SVHS outlet is provided at 160, and two composite or
5 NTSC outlets are provided at 162 and 164, respectively.

From the foregoing, it is apparent that an entire imaging device may be incorporated within the distal tip of the camera module, or may have some elements of the imaging device being placed in the housing of the PDA. Based upon the type of image sensor used, the profile area of the
10 imaging device may be made small enough to be placed into a camera module which has a very small diameter.

This invention has been described in detail with reference to particular embodiments thereof, but it will be understood that various other modifications can be effected within the spirit and scope of this invention.

CLAIMS**What is claimed is:**

1. In a PDA having capability to transmit data between a personal computer connected to a global communications network, the improvement comprising:

5 a video system integral with said PDA for receiving and transmitting video images, and for viewing said video images, said video system comprising;

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10 a camera module housing an image sensor therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of CMOS pixels for timing and control of said array of CMOS pixels, said image sensor producing a pre-video signal, a first circuit board lying in a second plane and electrically coupled to said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired
15 video format;

a video view screen attached to said PDA for viewing said video images, said video view screen communicating with said first circuit board, and displaying video images processed by said first circuit board.

2. A device, as claimed in claim 1, wherein:

said first circuit board is placed adjacent said image sensor within said camera module.

3. A device, as claimed in claim 1, wherein:

said first circuit board is remote from said image sensor and placed within a housing of said PDA.

4. A device, as claimed in claim 1, wherein:
said image sensor defines a profile area in said first plane,
and said first circuit board is positioned in longitudinal alignment with said image sensor such that said first circuit board does not extend substantially
5 beyond said profile area.

5. A device, as claimed in claim 1, further including:
a second circuit board electrically coupled with said first circuit board and said image sensor for further processing said pre-video signal, said second board being placed adjacent said first circuit board
5 within said camera module.

6. A device, as claimed in claim 1, wherein:
said first and second planes are offset from and substantially parallel to one another.

7. A device, as claimed in claim 5, wherein:
said second circuit board lies in a third plane which is offset from and extends substantially parallel to said first and second planes.

8. A device, as claimed in claim 5, wherein:
said second circuit board includes means for digital signal processing enabling the pre-video signal conditioned by said first circuit board to be viewed by said video view screen.

9. A device, as claimed in claim 1, wherein:
said first circuit board converts said pre-video signal to a
post-video signal for direct reception by a remote video device, said post-
video signal being of a format selected from the group consisting of a
5 NTSC/PAL video signal and a VGA video signal.
10. A device, as claimed in claim 1, wherein:
said array of CMOS pixels includes an array of passive
CMOS pixels, wherein individual passive CMOS pixels of said array of
passive CMOS pixels each include a photo diode for producing
5 photoelectrically generated signals, and an access transistor communicating
with said photo diode to control the release of photoelectrically generated
signals.
11. A device, as claimed in claim 1, wherein:
individual pixels within said array of CMOS pixels each
include an amplifier.
12. A device, as claimed in claim 1, further including:
a retractable cable interconnecting said camera module to
said PDA, said retractable cable enabling said camera module to be pulled
away from said PDA for selective taking of images by said camera module,
5 and allowing said camera module to be stored within said PDA by
retracting said cable and securing said camera module within said PDA.
13. A device, as claimed in claim 1, wherein:

said PDA includes a text screen mounted therein for viewing text which is manipulated by a user.

14. A device as claimed in claim 1, further including:
a wireless telephone attached to said PDA.

15. A device, as claimed in claim 1, further including:
a remote video device electrically coupled to said video system for further viewing said video images.

16. A device, as claimed in claim 15, wherein:
said remote video device is selected from the group consisting of a television and a computer monitor.

17. In a PDA having capability to transmit data between a computer connected to a global communications network, the PDA having a housing, and a video view screen for viewing the data which includes video signals, the improvement comprising:

5 a camera module for taking video images, said camera module communicating with circuitry within said PDA enabling viewing on said video view screen and enabling video signals to be transmitted from said camera module to said computer, said camera module including an image sensor housed therein, said image sensor lying in a first plane and
10 including an array of CMOS pixels for receiving images thereon, said image sensor further including circuitry means on said first plane and coupled to said array of said CMOS pixels for timing and control of said array of CMOS pixels, said image sensor producing a pre-video signal, a

first circuit board electrically connected to said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired video format.

18. A device, as claimed in claim 17, wherein:

said first circuit board is placed adjacent said image sensor within said camera module.

19. A device, as claimed in claim 17, wherein:

said first circuit board is placed within said housing of said PDA.

20. A device, as claimed in claim 17, wherein:

said image sensor defines a profile area in said first plane, and said first circuit board is positioned in longitudinal alignment with said image sensor such that said first circuit board does not extend substantially beyond said profile area.

21. A device, as claimed in claim 17, further including:

a second circuit board electrically coupled with said first circuit board and said image sensor for further processing said pre-video signal, said second board being placed adjacent said first circuit board within said camera module.

22. A device, as claimed in claim 17, wherein:

said first and second planes are offset from and substantially parallel to one another.

23. A device, as claimed in claim 17, wherein:
said second circuit board lies in a third plane which is offset
from and extends substantially parallel to said first and second planes.

24. A device, as claimed in claim 17, wherein:
said second circuit board includes means for digital signal
processing enabling the pre-video signal conditioned by said first circuit
board to be viewed by said video view screen.

25. A device, as claimed in claim 17, wherein:
said first circuit board converts said pre-video signal to a post
video signal for direct reception by a remote video device, said post-video
signal being of a format selected from the group consisting of a NTSC/PAL
5 video signal and a VGA video signal.

26. A device, as claimed in claim 17, wherein:
said array of CMOS pixels includes an array of passive
CMOS pixels, wherein individual passive CMOS pixels of said array of
passive CMOS pixels each include a photo diode for producing
5 photoelectrically generated signals, and an access transistor communicating
with said photo diode to control the release of photoelectrically generated
signals.

27. A device, as claimed in claim 17, wherein:
individual pixels within said array of CMOS pixels each
include an amplifier.

28. A device, as claimed in claim 17, further including:
a retractable cable interconnecting said camera module to
said PDA, said retractable cable enabling said camera module to be pulled
away from said PDA for selective taking of images by said camera module,
5 and allowing said camera module to be stored within said PDA by
retracting said cable and securing said camera module within said PDA.

29. A device, as claimed in claim 17, wherein:
said PDA includes a command screen mounted therein for
executing commands directed by a user.

30. A device as claimed in claim 17, further including:
a wireless telephone attached to said PDA.

31. A device, as claimed in claim 17, further including:
a remote video device electrically coupled to said PDA for
further viewing said video images.

32. A device, as claimed in Claim 31, wherein:
said remote video device is selected from the group
consisting of a television and a computer monitor.

33. A PDA having capability for receiving and transmitting video
and audio images between the PDA and a personal computer connected to
a global communications network, said PDA comprising:
an image sensor lying in a first plane, and an array of CMOS
5 pixels for receiving images thereon, said image sensor further including

circuitry means on said first plane and coupled to said array of CMOS pixels for timing and control of said array of CMOS pixels, said image sensor producing a pre-video signal;

10 a first circuit board electrically communicating with said image sensor, said first circuit board including circuitry means for converting said pre-video signal to a desired video format;

a camera module housing said image sensor;

15 a transceiver/amplifier section electrically coupled to said first circuit board for transmitting, receiving, and amplifying video and audio signals;

20 a digital signal processor electrically coupled to said first circuit board and said transceiver/amplifier section, said digital signal processor further conditioning said pre-video signal which is first conditioned by said first circuit board, and also for conditioning video and audio signals from said transceiver/amplifier section;

a microphone electrically communicating with said digital signal processor for recording and receiving audio signals;

a speaker electrically communicating with said digital signal processor for broadcasting audio signals;

25 a video view screen attached to said PDA, said video view screen for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section;

30 a video switch communicating with said first circuit board and said digital signal processor for switching video images to be viewed on said video view screen; and

a power supply mounted to said PDA for providing power thereto.

34. A device, as claimed in claim 33, wherein:
said first circuit board is placed adjacent said image sensor within said camera module.

35. A device, as claimed in claim 33, wherein:
said first circuit board is remote from said image sensor and placed within a housing of said PDA.

36. A device, as claimed in claim 33, wherein:
said image sensor defines a profile area in said first plane, and said first circuit board is positioned in longitudinal alignment with said image sensor such that said first circuit board does not extend substantially
5 beyond said profile area.

37. A device, as claimed in claim 33, further including:
a second circuit board electrically coupled with said first circuit board and said image sensor for further processing said pre-video signal, said second board being placed adjacent said first circuit board.

38. A device, as claimed in claim 33, wherein:
said first and second planes are offset from and substantially parallel to one another.

39. A device, as claimed in claim 37, wherein:

said second circuit board lies in a third plane which is offset from and extends substantially parallel to said first and second planes.

40. A device, as claimed in claim 37, wherein:

said second circuit board includes means for digital signal processing enabling the pre-video signal conditioned by said first circuit board to be viewed by said video view screen.

41. A device, as claimed in claim 33, wherein:

said first circuit board converts said pre-video signal to a post-video signal for direct reception by a remote video device, said post-video signal being of a format selected from the group consisting of a

5 NTSC/PAL video signal and a VGA video signal.

42. A device, as claimed in claim 33, wherein:

said array of CMOS pixels includes an array of passive CMOS pixels, wherein individual passive CMOS pixels of said array of passive CMOS pixels each include a photo diode for producing

5 photoelectrically generated signals, and an access transistor communicating with said photo diode to control the release of photoelectrically generated signals.

43. A device, as claimed in claim 33, wherein:

individual pixels within said array of CMOS pixels each include an amplifier.

44. A device, as claimed in claim 33, further including:

a retractable cable interconnecting said imaging device to
 said PDA, said retractable cable enabling said imaging device to be pulled
 away from said PDA for selective taking of images by said imaging device,
 5 and allowing said imaging device to be stored within said PDA by
 retracting said cable and securing said camera module within said PDA.

45. A device, as claimed in claim 33, wherein:
 said PDA includes a text screen mounted therein for viewing
 text which is manipulated buy a user.

46. A device as claimed in claim 33, further including:
 a wireless telephone attached to said PDA.

47. A device, as claimed in claim 33, further including:
 a remote video device electrically coupled to said video
 system for further viewing said video image.

48. A device, as claimed in claim 47, wherein:
 said remote video device is selected from the group
 consisting of a television and a computer monitor.

49. In a PDA having capability to transmit data between a
 personal computer connected to a global communications network, the
 improvement comprising:
 a video system integral with said PDA for receiving and
 5 transmitting video images, and for viewing said images, said video system
 comprising:

a camera module housing an image sensor therein,
 said image sensor lying in a first plane and including an array of CMOS
 pixels for receiving images thereon, said image sensor producing a pre-
 video signal, a first circuit board lying in a second plane and electrically
 coupled to said image sensor, said first circuit board including circuitry
 means for timing and control of said array of CMOS pixels and circuitry
 means for processing and converting said pre-video signal to a desired
 video format; and

a video view screen attached to said PDA for viewing
 said video images, said video view screen communicating with said first
 circuit board.

50. A device, as claimed in claim 49, wherein:

said first circuit board is placed adjacent to said image sensor
 and within said camera module.

51. A device, as claimed in claim 49, wherein:

said first circuit board is remote from said image sensor and
 placed within a housing of said PDA.

52. In a PDA having capability to transmit data between a
 personal computer connected to a global communications network, the
 improvement comprising:

a video system integral with said PDA for receiving and
 transmitting video images, and for viewing said images, said video system
 comprising:

a camera module housing an image sensor therein, said image
 sensor lying in a first plane and including an array of CMOS pixels for
 receiving images thereon, circuitry means electrically coupled to said array
 of CMOS pixels for timing and control of said array of CMOS pixels, said
 10 circuitry means for timing and control being placed remote from said array
 of CMOS pixels on a second plane, said image sensor producing a pre-
 video signal, a first circuit board lying in a third plane and electrically
 coupled to said image sensor, said first circuit board including circuitry
 15 means for processing and converting said pre-video signal to a desired
 video format; and

a video view screen attached to said PDA for viewing said
 video images, said video view screen communicating with said first circuit
 board, and displaying video images processed by said first circuit board.

53. A device, as claimed in claim 52, wherein:

said circuitry means for timing and control is placed adjacent
 to said image sensor in said camera module.

54. A device, as claimed in claim 52, wherein:

said circuitry means for timing and control is placed within a
 housing of the PDA.

55. In a PDA having capability to transmit data between a
 personal computer connected to a global communications network, the
 PDA including a video view screen for viewing video images, the
 improvement comprising:

5 a camera module for taking video images, said camera
 module communicating with circuitry within said PDA enabling viewing
 on said video view screen and enabling video signals to be transmitted
 from said camera module to the personal computer, said camera module
 including an image sensor housed therein, said image sensor lying in a first
 10 plane and including an array of CMOS pixels for receiving images thereon,
 said image sensor producing a pre-video signal, a first circuit board lying in
 a second plane and electrically connected to said image sensor, said first
 circuit board including circuitry means for timing and control of said array
 of CMOS pixels and circuitry means for processing and converting said
 15 pre-video signal to a desired video format.

56. A device, as claimed in claim 55, wherein:

said first circuit board is placed adjacent said image sensor
 within said camera module.

57. A device, as claimed in claim 55, wherein:

said first circuit board is placed within a housing of said
 PDA.

58. In a PDA having capability to transmit data between a
 personal computer connected to a global communications network, the
 PDA including a video view screen for viewing the video images, the
 improvement comprising:

5 a camera module for taking video images, said camera
 module communicating with circuitry within said PDA enabling viewing of
 said video images on said PDA and enabling video signals to be

transmitted from said camera module to the personal computer, said camera module including an image sensor housed therein, said image sensor lying in a first plane and including an array of CMOS pixels for receiving images thereon, said image sensor further including circuitry means electrically coupled to said array of said CMOS pixels for timing and control of said array of CMOS pixels, said circuitry means for timing and control placed remote from said array of CMOS pixels on a second plane, said image sensor producing a pre-video signal, a first circuit board electrically connected to said image sensor and lying in a third plane, said first circuit board including circuitry means for processing and converting said pre-video signal to a desired video format.

59. A device, as claimed in claim 58, wherein:

said circuitry means for timing and control is placed adjacent to said image sensor in said camera module.

60. A device, as claimed in claim 58, wherein:

said circuitry means for timing and control is placed within a housing of said PDA.

61. A PDA having capability for receiving and transmitting video and audio images between the PDA and a personal computer connected to a global communications network, said PDA comprising:

an image sensor lying in a first plane including an array of CMOS pixels for receiving images thereon, said image sensor producing a pre-video signal,

a first circuit board electrically communicating with said image sensor, said first circuit board including circuitry means for timing and control of said array of CMOS pixels and circuitry means for
10 processing and converting said pre-video signal to a desired video format;
a camera module housing said image sensor;
a transceiver/amplifier section electrically coupled to said first circuit board for transmitting, receiving, and amplifying video and audio signals;
15 a digital signal processor electrically coupled to said first circuit board and said transceiver/amplifier section, said digital signal processor further conditioning said pre-video signal which is first conditioned by said first circuit board, and also for conditioning video and audio signals from said transceiver/amplifier section;
20 a microphone electrically communicating with said digital signal processor for recording and receiving audio signals;
a speaker electrically communicating with said digital signal processor for broadcasting audio signals;
a video view screen attached to said PDA, said video view
25 screen for selectively displaying images from said imaging device, and for selectively displaying video images received by said transceiver/amplifier section;
a video switch communicating with said first circuit board and said digital signal processor for switching video images to be viewed
30 on said video view screen; and
a power supply mounted to said PDA for providing power thereto.

62. A device, as claimed in claim 61, wherein:

said first circuit board is placed adjacent to said image sensor and within said camera module.

63. A device, as claimed in claim 61, wherein:

said first circuit board is remote from said image sensor, and placed within a housing of said PDA.

64. A PDA having capability for receiving and transmitting video and audio images between the PDA and a personal computer connected to a global communications network, said PDA comprising:

an image sensor lying in a first plane, and an array of CMOS
5 pixels for receiving images thereon, said image sensor further including circuitry means electrically coupled to said array of CMOS pixels for timing and control of said array of CMOS pixels, said circuitry means for timing and control being placed remote from said array of CMOS pixels on a second plane, said image sensor producing a pre-video signal;

10 a first circuit board electrically coupled with said image sensor and lying in a third plane, said first circuit board including circuitry means for processing and converting said pre-video signal to a desired video format;

a camera module housing said image sensor;
15 a transceiver/amplifier section electrically coupled to said first circuit board for transmitting, receiving, and amplifying video and audio signals;

a digital signal processor electrically coupled to said first circuit board and said transceiver/amplifier section, said digital signal

20 processor further conditioning said pre-video signal which is first
conditioned by said first circuit board, and also for conditioning video and
audio signals from said transceiver/amplifier section;

a microphone electrically communicating with said digital
signal processor for recording and receiving audio signals;

25 a speaker electrically communicating with said digital signal
processor for broadcasting audio signals;

a video view screen attached to said PDA, said video view
screen for selectively displaying images from said imaging device, and for
selectively displaying video images received by said transceiver/amplifier
30 section;

a video switch communicating with said first circuit board
and said digital signal processor for switching video images to be viewed
on said video view screen; and

35 a power supply mounted to said PDA for providing power
thereto.

65. A device, as claimed in claim 64, wherein:

said circuitry means for timing and control is placed adjacent
to said image sensor in said camera module.

66. A device, as claimed in claim 65, wherein:

said circuitry means for timing and control is placed within a
housing of said PDA.

67. In a method for conducting video conferencing communications through connection with a global communications network, the improvement comprising the steps of:

providing a camera module having an image sensor housed
5 therein;

providing a cable for interconnecting the camera module to
the PDA;

displacing the camera module away from the PDA;

pointing the camera module at a targeted object; and

10 taking video images of the targeted object by the camera module for viewing on the PDA, and for transmission of the video images to the global communications network.

68. A method, as claimed in claim 67, further comprising the steps of:

selectively extending and selectively retracting the cable,
enabling the camera module to be pointed in a desired direction toward the
5 targeted object.

69. A method, as claimed in claim 67, wherein:

said image sensor includes a CMOS pixel array.

70. In a PDA having capability for data exchange between a personal computer connected to a global communications network, the improvement comprising:

a camera module housing an image sensor therein, said
5 camera module for producing video images of a targeted object;

means for interconnecting said camera module to said PDA,
 said means for interconnecting enabling said camera module to be
 selectively displaced at a location remote from said PDA; and
 a video view screen attached to said PDA for selectively
 viewing video images taken by said camera module, and for selectively
 viewing incoming video images received from the personal computer
 connected to the global communications network.

71. A device, as claimed in claim 70, wherein:

said PDA includes a housing, and an opening for receiving
 said camera module so as to place said camera module in a stored position.

72. In a PDA having a housing and a video view screen for
 viewing video images, the improvement comprising:

a camera module housing an image sensor therein, said
 camera module for producing video images of a targeted object; and

means for interconnecting said camera module to said PDA,
 said means for interconnecting enabling said camera module to be
 selectively displaced at a location remote from said PDA.

73. A device, as claimed in claim 72, wherein:

said PDA includes an opening in said housing for receiving
 said camera module so as to place said camera module in a stored position.

74. In a PDA, the improvement comprising:

a camera module housing an image sensor therein;

circuitry means coupled to said image sensor for timing and control of said image sensor;

5 circuitry means for processing images taken by said image sensor to create video signals of a desired video format;

means for interconnecting said camera module to a housing of said PDA, said means for interconnecting enabling said camera module to be selectively displaced from said housing by the user for pointing the
10 camera module at a targeted object.

75. A device, as claimed in claim 74, wherein:

said PDA includes an opening in said housing for receiving said camera module so as to place said camera module in a stored position.

ABSTRACT

A reduced area imaging device is provided for use with a miniature hand-held computer referred to in the industry as a PDA. In one configuration of the imaging device, the image sensor is placed remote from the remaining image processing circuitry. In a second configuration, all of the image processing circuitry to include the image sensor is placed in a stacked fashion near the same location. In the first configuration, the entire imaging device can be placed at the distal end of a camera module. In a second configuration, the image sensor is remote from the remaining image processing circuitry wherein available space within the PDA is used to house the remaining circuitry. In any of the embodiments, the image sensor may be placed alone on a first circuit board, or timing and control circuits may be included on the first circuit board containing the image sensor. One or more video processing boards can be stacked in a longitudinal fashion with respect to the first board, or the video processing boards may be placed within the housing of the communication device. The PDA includes a miniature LCD-type video view screen which is capable of viewing not only the images taken by the camera module, but also can show incoming video images received from a personal computer connected to a global communications network. The camera module is of such small size that it can be easily stored within the housing of the PDA, and may be attached thereto as by a small retractable cable.

Please type a plus sign (+) inside this box → ☐

**DECLARATION FOR UTILITY OR
DESIGN PATENT APPLICATION**
(37 CFR 1.63)

Attorney Docket Number: F97.13 CIP7First Named Inventor: Edwin L. Adair, et al.**COMPLETE IF KNOWN**

☒ Declaration Submitted with Initial Filing
☐ Declaration Submitted after Initial Filing (surcharge [37 CFR 1.16(e)] required)

Application Number: _____

Filing Date: _____

Group Art Unit: _____

Examiner Name: _____

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled _____
"Hand-held Computers Incorporating Reduced Area Imaging Devices" the specification of which

☒ is attached hereto

OR

☐ was filed on (MM/DD/YY) _____ as United States Application Number or PCT International Application Number _____ as was amended on (MM/DD/YY) _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or Inventor's certificate, or 365(a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or Inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

Priority Not Claimed
Certified Copy Attached ?
Yes No

(Number)	(Country)	(Foreign Filing Date)	<input checked="" type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>
(Number)	(Country)	(Day/Month/Year Filed)	<input type="checkbox"/>	<input type="checkbox"/>	<input type="checkbox"/>

☐ Additional foreign application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached.

I hereby claim the benefit under 35 U.S.C. 119(e) of the United States provisional application(s) listed below.

(Application Number)	(Filing Date)	<input type="checkbox"/> Additional provisional application numbers are listed on supplemental priority data sheet PTO/SB/02B attached hereto.
(Application Number)	(Filing Date)	

I hereby claim the benefit under 35 U.S.C. §120 of any United States application(s), or §365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 C.F.R. 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application.

<u>09/496,312</u>	<u>2/1/00</u>	
U.S. Parent Application or PCT Parent Number	Parent Filing Date	Parent Patent Number (if applicable)
<u>U.S. Parent Application or PCT Parent Number</u>	<u>Parent Filing Date</u>	<u>Parent Patent Number (if applicable)</u>

☐ Additional U.S. or PCT International application numbers are listed on a supplemental priority data sheet PTO/SB/02B attached.

As named inventor, I hereby appoint the following practitioner(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: ☒ Registered Practitioner(s) name/registration number listed below

Name	Registration Number
<u>Gary D. Fields</u>	<u>19,604</u>
<u>Brent P. Johnson</u>	<u>38,031</u>

☐ Additional registered practitioner(s) named on Supplemental Registered Practitioner Information sheet PTO/SB/02C attached hereto.

Direct all correspondence to: Fields & Johnson, P.C.
8480 East Orchard Road, Suite 5600, Englewood, CO 80111
Country: U.S.A. Telephone: (303) 689-9100 Fax: (303) 689-9250

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under 18 U.S.C. 1001 and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Name of Sole or First Inventor ☐ A petition has been filed for this unsigned inventor
Given Name (first and middle [if any]) Edwin L. Family Name or Surname Adair

Inventor's signature Edwin L. Adair Date 11 Aug 2010
Residence 317 Paragon Way Citizenship U.S.A.
Post Office Address 317 Paragon Way
City, State, Zip, Country Castle Pines Village, CO 80104

Full name of second joint inventor, if any (given name, family name) Jeffrey L. Adair

Second Inventor's signature Jeffrey L. Adair Date 8-11-10
Residence 1861 East Redfox Place Citizenship U.S.A.
Post Office Address 1861 East Redfox Place
City, State, Zip, Country Highlands Ranch, CO 80126

☒ Additional inventors are being named on the _____ supplemental Additional Inventor(s) sheet(s) PTO/SB/02A attached hereto.

DECLARATION FOR PATENT APPLICATION

Attorney Docket No.: F97.13 CIP5

Full name of third joint inventor, if any (given name, family name) Randall S. Adair

Third Inventor's signature Randall S. Adair Date 8/11/00

Residence 3082 South Flamingo Way Citizenship U.S.A.

Post Office Address 3082 South Flamingo Way

City, State, Zip, Country Denver, CO 80222

[Page 3 of 3]

Applicant, Patentee or Identifier Edwin L. Adair, et al. Attorney's
 Application or Patent No.: _____ Docket No.: F97.13CIP7

Filed or Issued: _____

Title "Hand-held Computers Incorporating Reduced Area Imaging Devices"

**STATEMENT CLAIMING SMALL ENTITY
 STATUS (37 CFR 1.9(f) AND 1.27(b)) - INDEPENDENT INVENTOR**

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9(c) for purposes of paying reduced fees under Section 41(a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention described in:

- ☒ the specification filed herewith with titled as listed above.
☐ the application identified above.
☐ the patent identified above.

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who would not qualify as an independent inventor under 37 CFR 1.9(c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9(d) or a nonprofit organization under 37 CFR 1.9(e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey or license any rights in the invention is listed below:

- ☒ no such person, concern or organization.
☐ each such person, concern or organization is listed below.

Separate statements are required from each named person, concern or organization having rights to the invention stating their status as small entities. (37 CFR 1.27)

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate (37 CFR 1.28(b)).

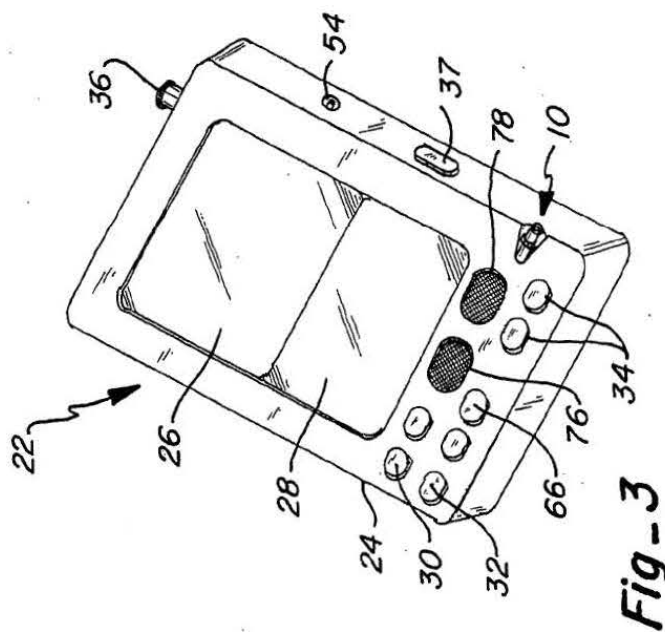
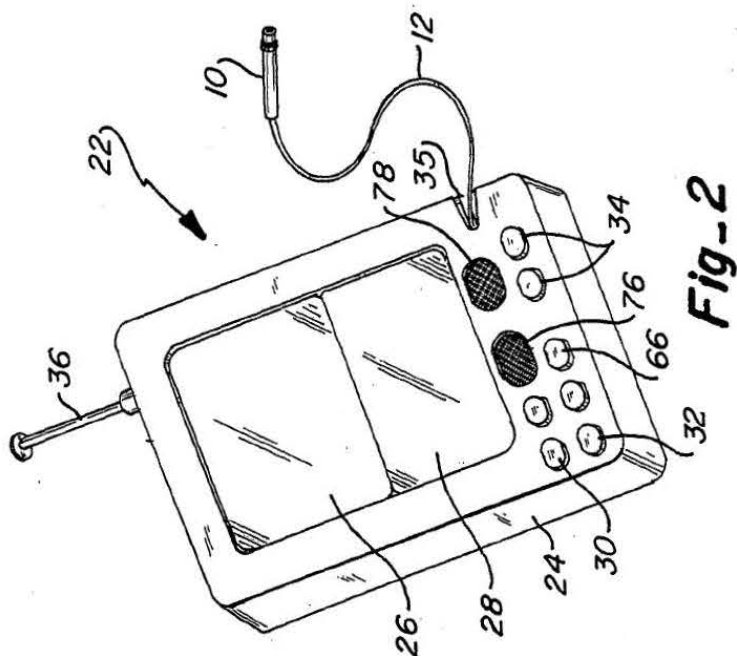
I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

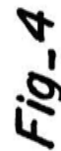
<u>Edwin L. Adair</u>	<u>Jeffrey L. Adair</u>	<u>Randall S. Adair</u>
NAME OF INVENTOR:	NAME OF INVENTOR:	NAME OF INVENTOR:
<u>Edwin L. Adair</u>	<u>Jeff L. Adair</u>	<u>Randall S. Adair</u>
Signature of Inventor:	Signature of Inventor:	Signature of Inventor:
<u>11 August 2000</u>	<u>8-11-00</u>	<u>8/11/00</u>
Date:	Date:	Date:



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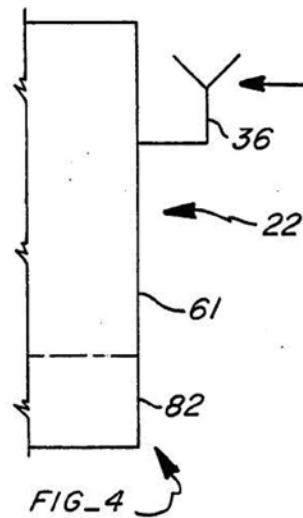
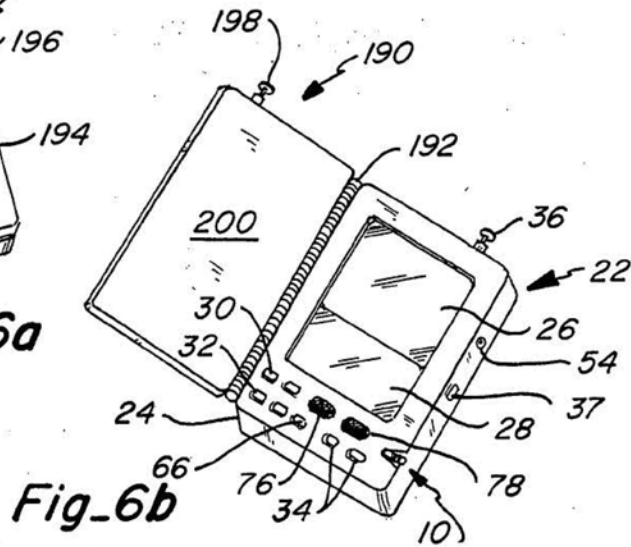
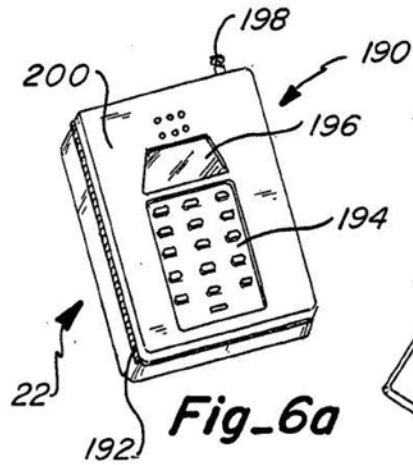
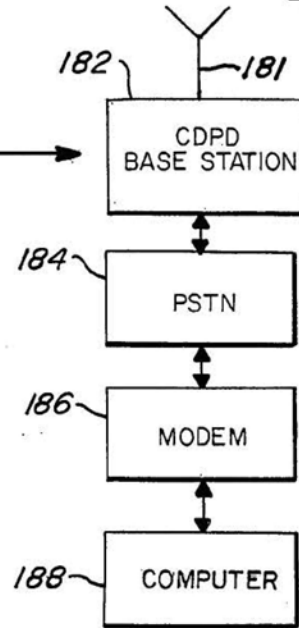
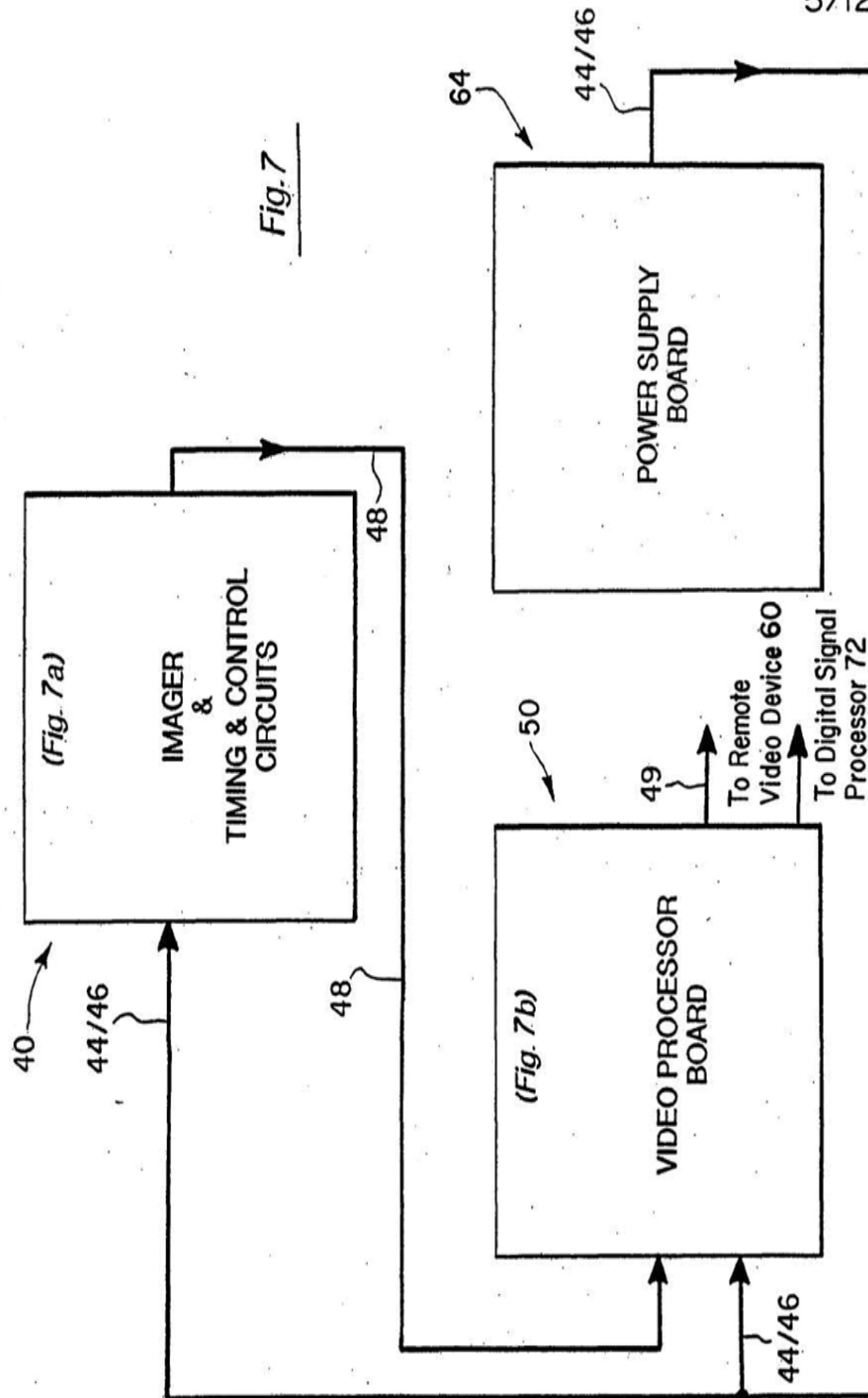
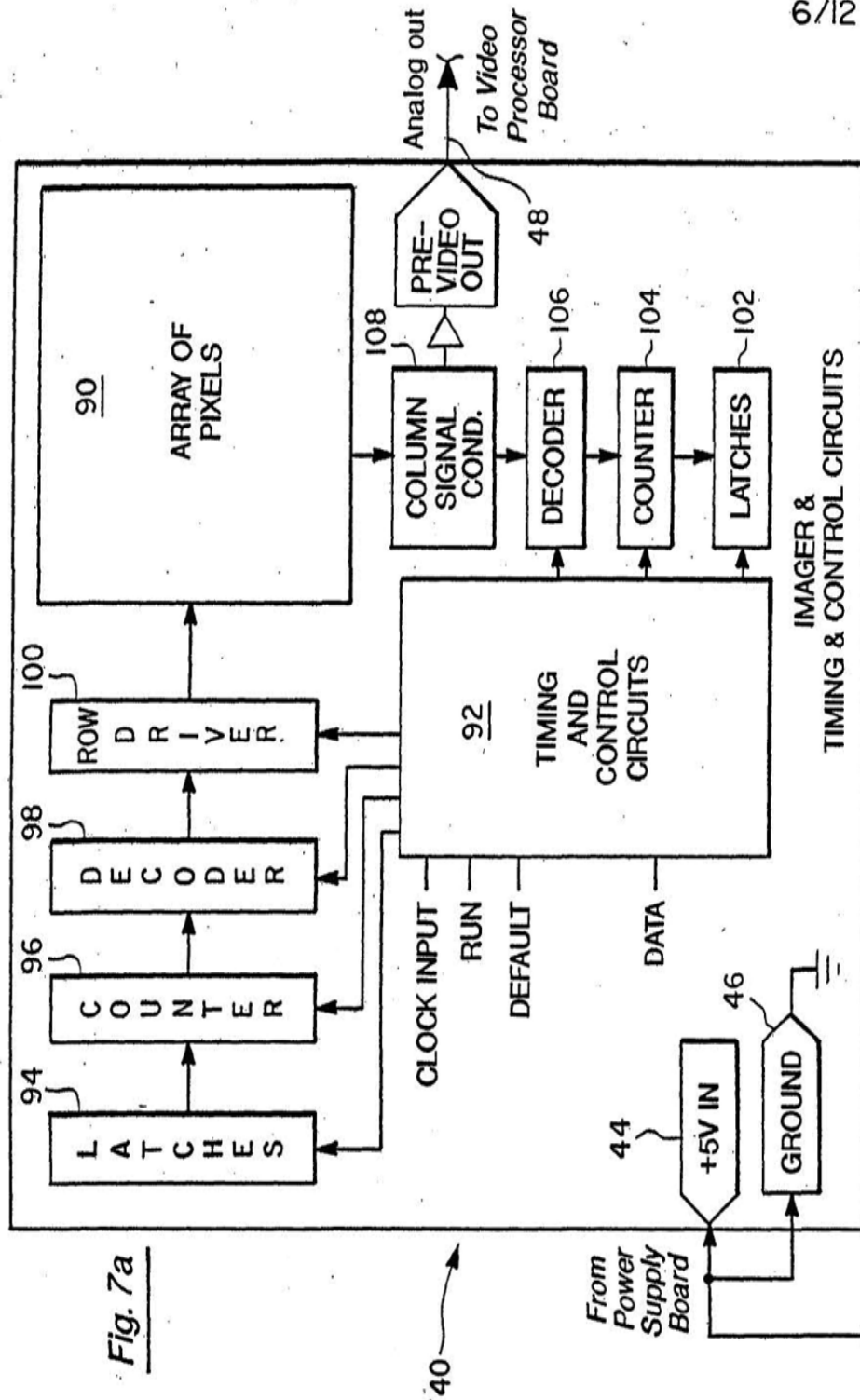


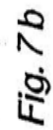
Fig-5





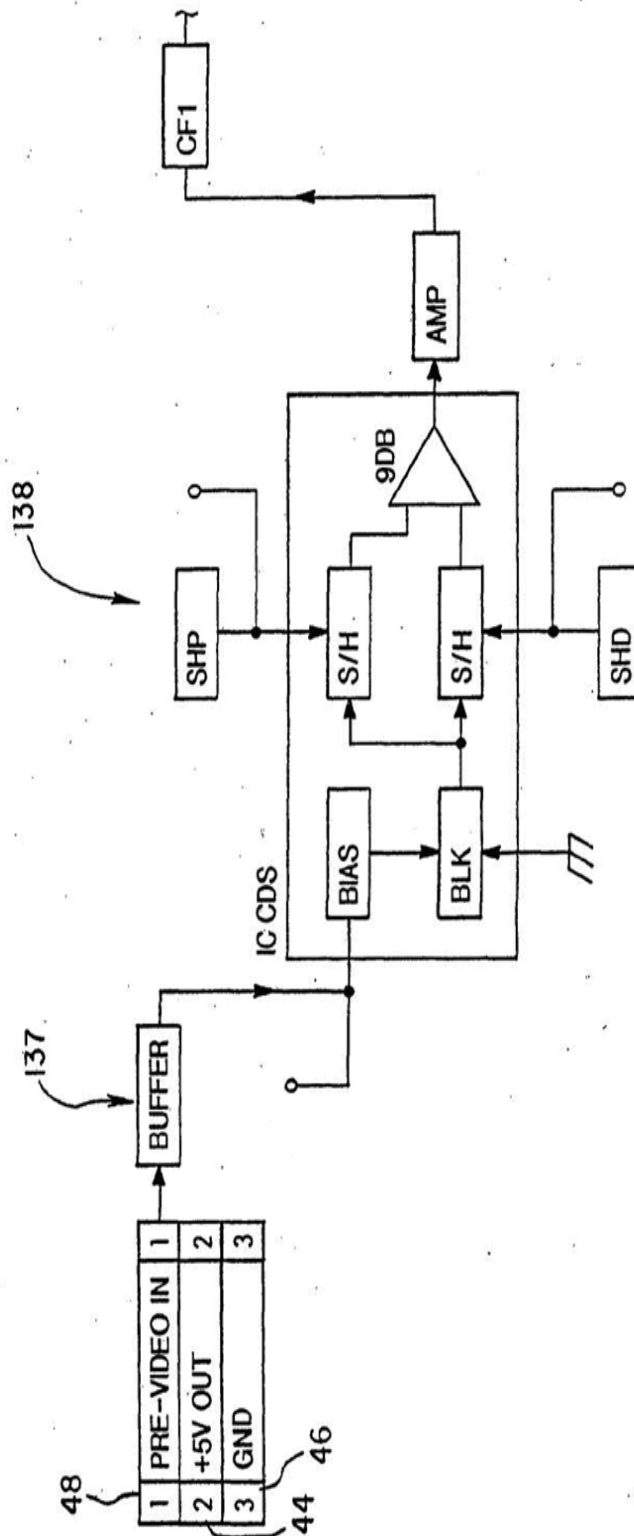
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Fig. 8a



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Fig. 8b

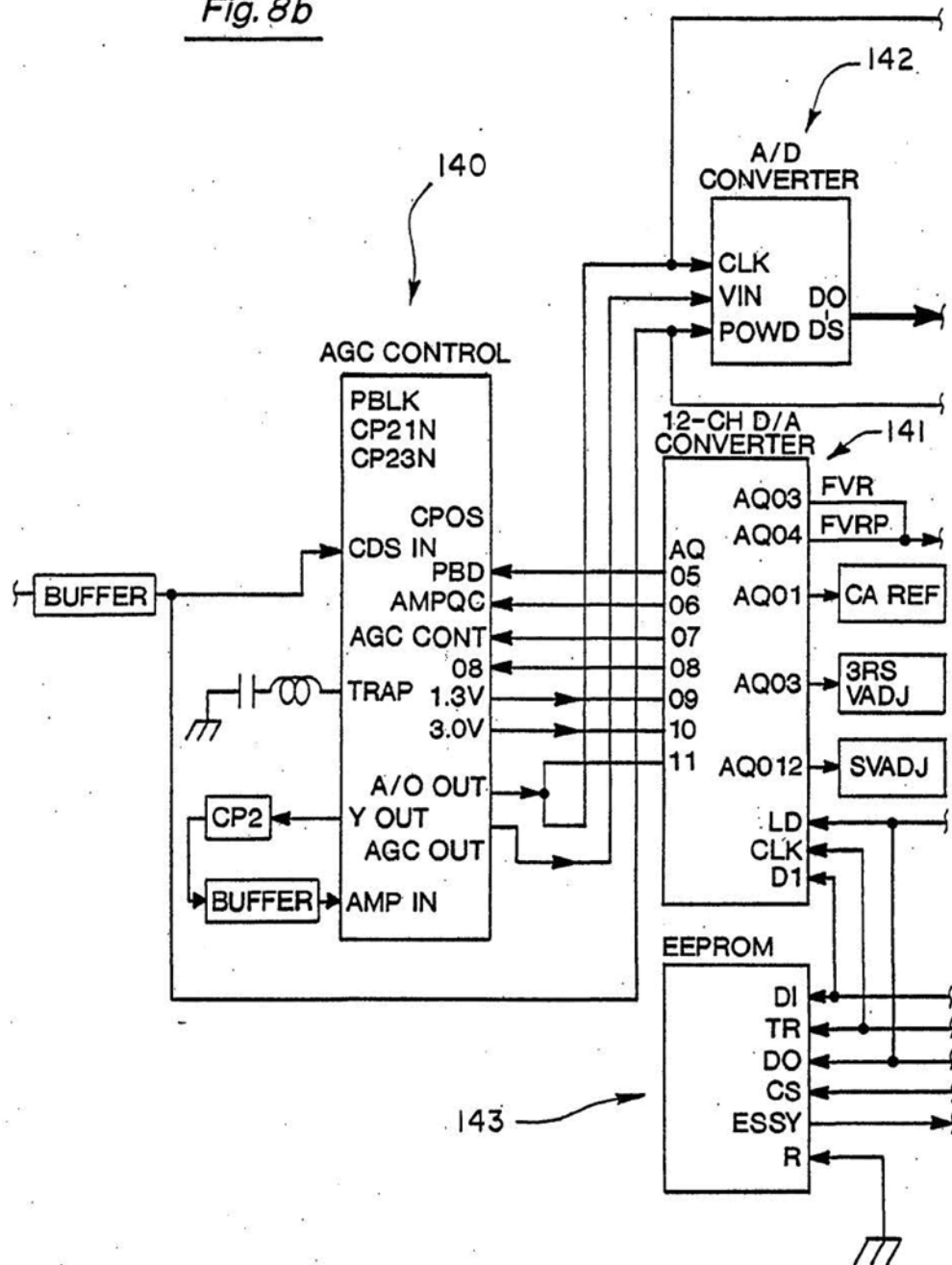
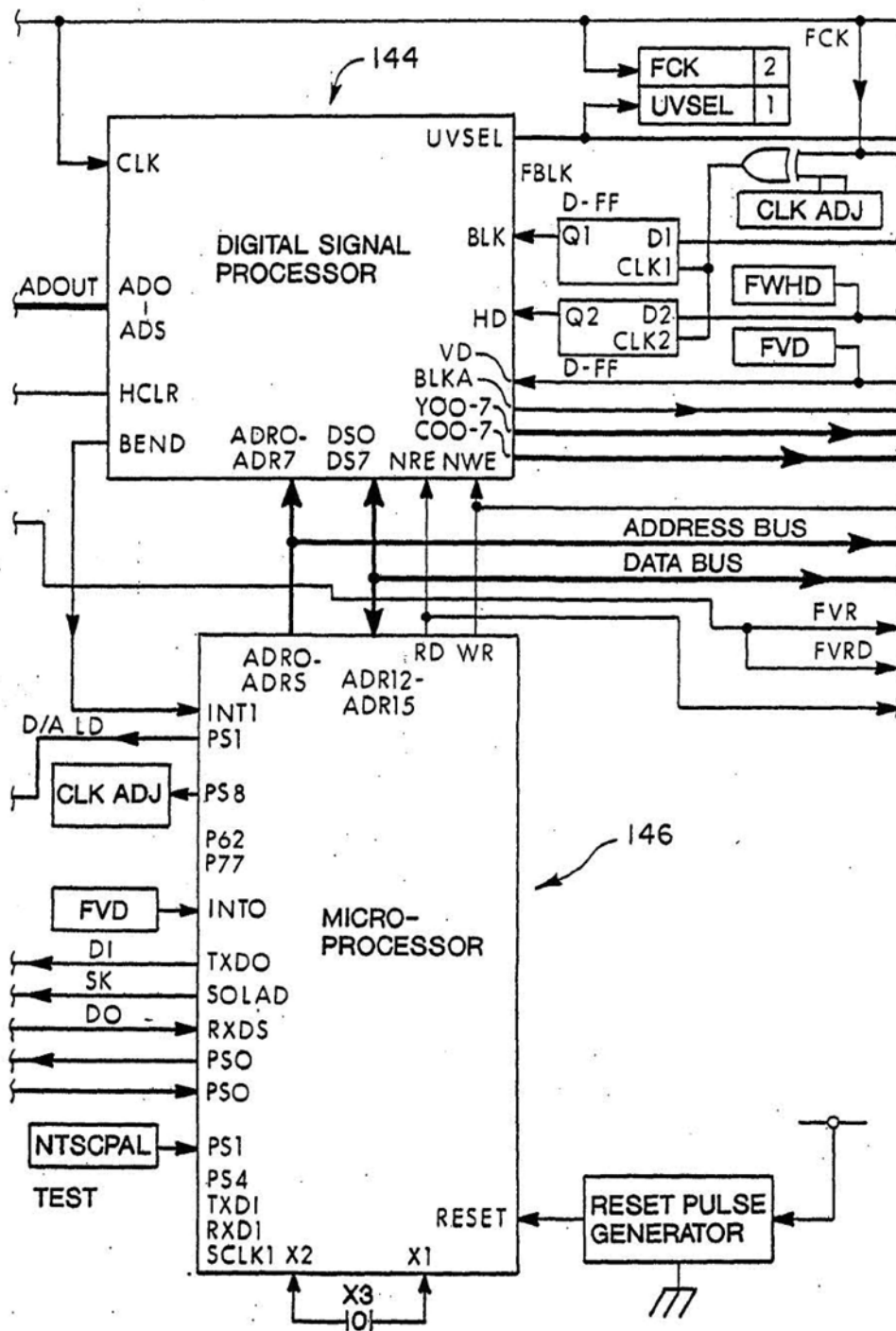
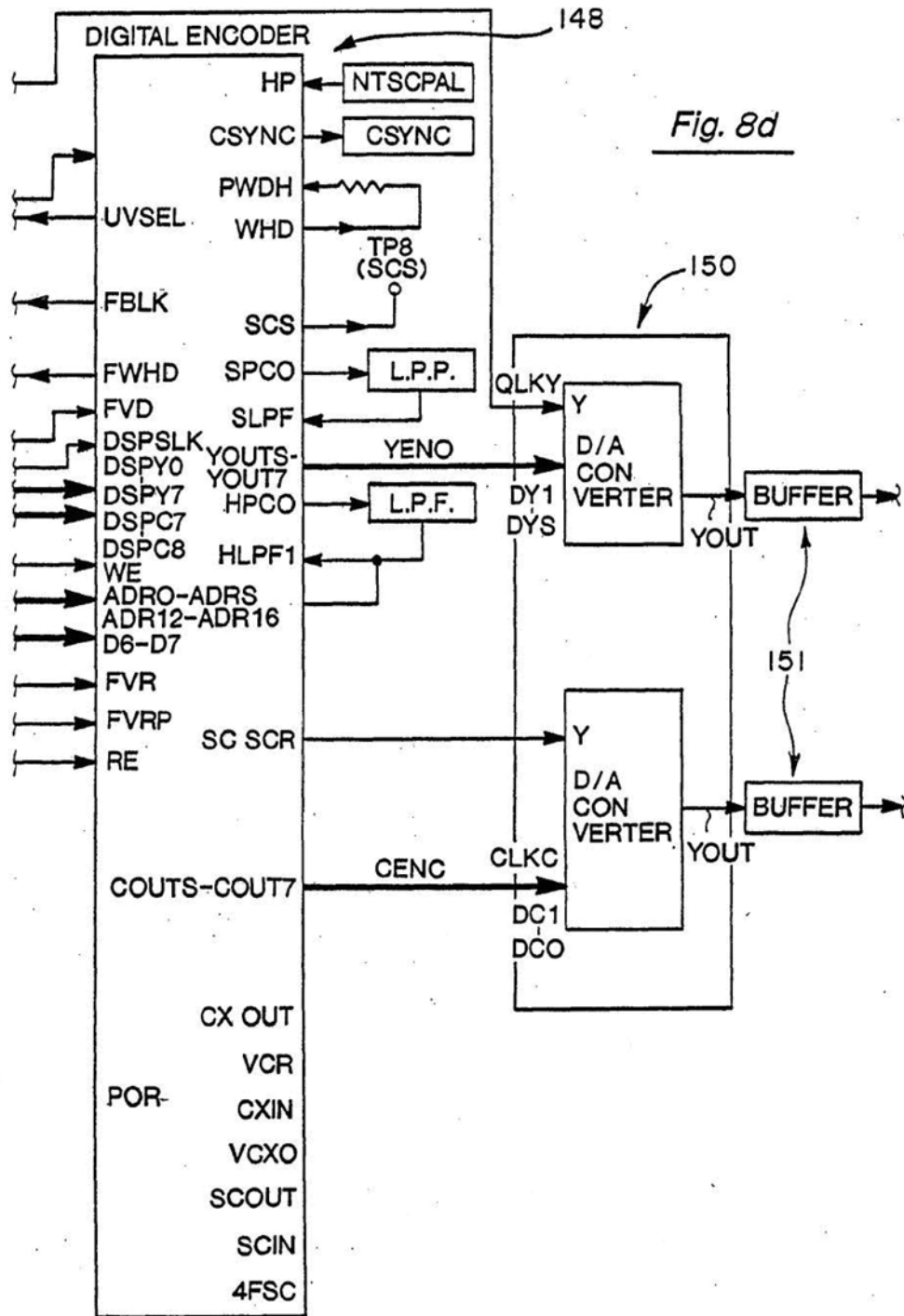


Fig. 8c

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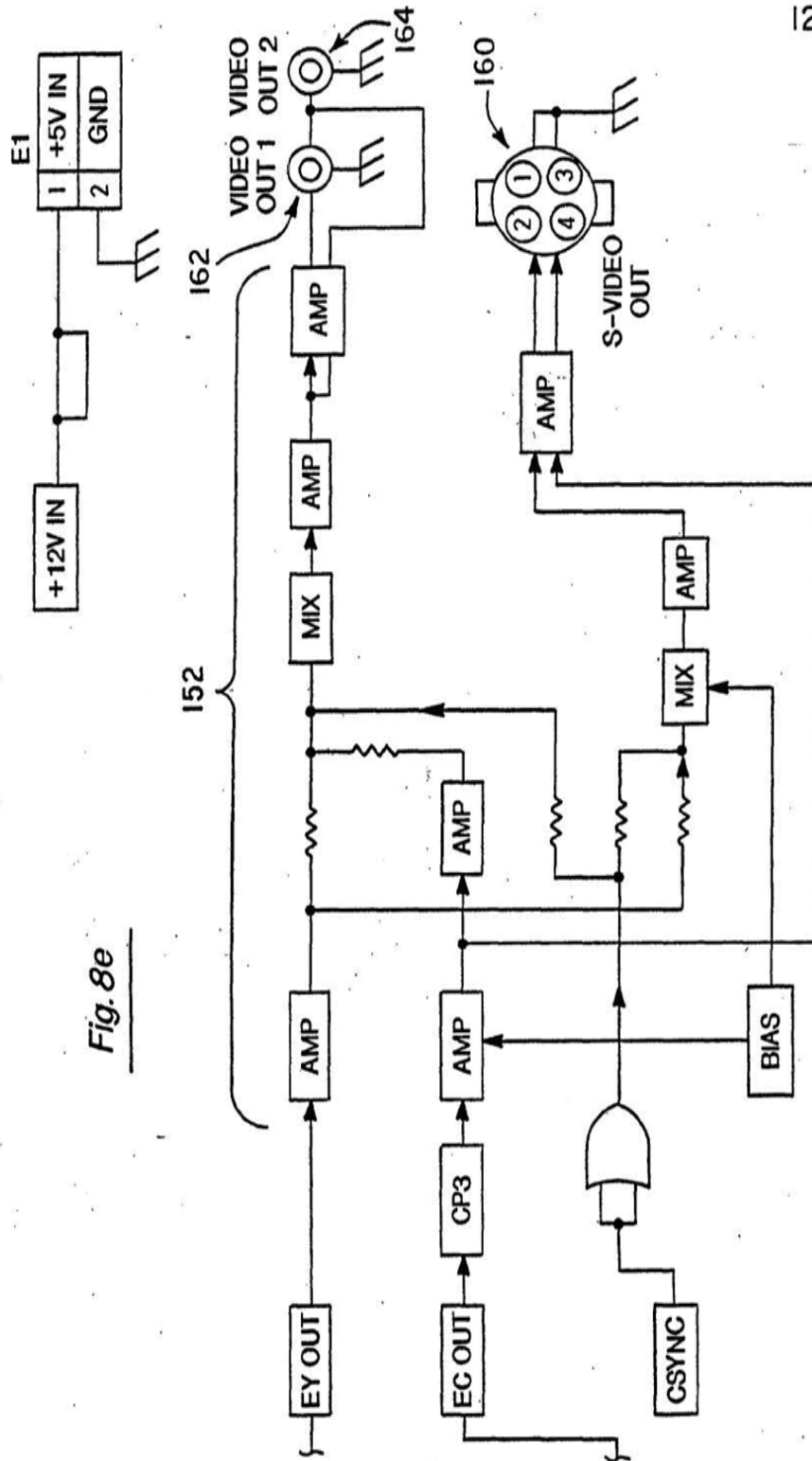


Fig. 8e