UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE

PATENT TRIAL AND APPEAL BOARD

SMIC, AMERICAS,

Petitioner

v.

INNOVATIVE FOUNDRY TECHNOLOGIES LLC

Patent Owner

U.S. Patent No. 6,580,122
Original Issue Date: June 17, 2003
Title: TRANSISTOR DEVICE HAVING AN ENHANCED WIDTH DIMENSION AND A METHOD OF MAKING SAME

Case No. IPR2020-01003

PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,580,122 PURSUANT TO 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42

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LISTING OF EXHIBITS

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Exhibit 1002	Declaration of Dr. Sayfe Kiaei ("**Kiaei**")
Exhibit 1003	Korean Laid-Open Patent Application No. KR1998-074469 (with associated certified English translation and translator's declaration) ("**Yun**")
Exhibit 1004	U.S. Patent No. 5,859,466 ("**Wada**")
Exhibit 1005	U.S. Patent No. 6,009,023 ("**Lu**")
Exhibit 1006	U.S. Patent No. 5,960,297 ("**Saki**")
Exhibit 1007	U.S. Patent No. 6,429,062 ("**Rubin**")
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Exhibit 1013	Excerpt from Chapter 4 of Sedra & Smith, *Microelectronic Circuits*, 5th Ed. (2004)
Exhibit 1014	R. K. Pancholy, *Gate Protection for CMOS/SOS*, 15th Int'l Reliability Physics Symposium, pp. 132-37 (1977)
Exhibit 1015	A. Chatterjee et al., *A Shallow Trench Isolation Study for 0.25/0.18 μm CMOS Technologies and Beyond*, Symposium on VLSI Technology Digest of Technical Papers, pp. 156-57 (1996)
Exhibit 1016	A. C. Ipri, *Sub-Micron Polysilicon Gate CMOS/SOS Technology*, 1978 International Electron Devices Meeting, pp.

	46-49 (1978)
Exhibit 1017	K. Ahmed et al., *Transistor Wars*, IEEE Spectrum, Vol. 48, No. 11, pp. 50-66 (2011)
Exhibit 1018	S. Aur et al., *Circuit Hot Electron Effect Simulation*, International Electron Devices Meeting, pp. 498-501 (1987)
Exhibit 1019	W. K. Henson et al., *Analysis of Leakage Currents and Impact on Off-State Power Consumption for CMOS Technology in the 100-nm Regime*, IEEE Transactions on Electron Devices, Vol. 47, No. 7, pp. 1393-1400 (2000)

1. INTRODUCTION

Pursuant to 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42, Petitioner SMIC, AMERICAS ("**SMIC**" or "**Petitioner**") respectfully requests *inter partes* review ("**IPR**") of claims 1-3, 5-14, 16-25, and 27-34 ("**Challenged Claims**") of U.S. Patent No. 6,580,122 (the "**'122 patent**") to Derick J. Wristers et al. The '122 patent was filed March 20, 2001 and issued June 17, 2003. According to U.S. Patent and Trademark Office ("**USPTO**") assignment records, the '122 patent is currently assigned to Innovative Foundry Technologies LLC ("**IFT**" or "**Patent Owner**"). There is more than a reasonable likelihood that Petitioner will prevail with respect to at least one Challenged Claim.

None of the prior art on which this Petition is based was cited or discussed during prosecution of the '122 patent.

Petitioner requests that the PTAB institute trial and find the Challenged Claims unpatentable for the reasons set forth in this Petition.

2. 37 C.F.R. § 42.8(B): MANDATORY NOTICES

2.1. 37 C.F.R. § 42.8(b)(1): Notice of Real-Parties-in-Interest

Petitioner SMIC and the following entities are real parties-in-interest:

Semiconductor Manufacturing International Corporation[1]; Semiconductor Manufacturing International (Shanghai) Corporation; Semiconductor Manufacturing International (Beijing) Corporation; Semiconductor Manufacturing International (Tianjin) Corporation; Semiconductor Manufacturing International (BVI) Corporation; Semiconductor Manufacturing International (Shenzhen) Corporation; Semiconductor Manufacturing North China (Beijing) Corporation; Semiconductor Manufacturing South China Corporation; Cypress Semiconductor Corporation; Broadcom Corporation; and Broadcom Incorporated. No other parties exercised or could have exercised control over this Petition; no other parties funded or directed this Petition. *See* Office Patent Trial Practice Guide, 77 Fed. Reg. 48759-60.

2.2. 37 C.F.R. § 42.8(b)(2): Notice of Related Matters

To the best knowledge of Petitioner, the '122 patent has been involved in the following litigations and matters:

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[1] Petitioner identifies Semiconductor Manufacturing International Corporation ("**SMIC Cayman**") as a real party in interest only because it is a named defendant in the co-pending litigation. SMIC Cayman itself, however, does not manufacture, use, sell, offer to sell, or import into the United States any products accused in the litigation.

Case Name	Filed
SMIC Americas et al. v. Innovative Foundry Technologies LLC, Case No. 3:20-cv-02256 (N.D. Cal.)	April 2, 2020
Innovative Foundry Technologies LLC v. Semiconductor Manufacturing International Corporation et al., Case No. 6:19-cv-00719 (W.D. Tex.)	Dec. 20, 2019

2.3. 37 C.F.R. § 42.8(b)(3) and (4): Notice of Counsel and Service Information

Lead Counsel: Alex V. Chachkes (Reg. No. 41,663)

Backup Counsel: Yufeng Ma (Reg. No. 56,975)

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Petitioner submits a Power of Attorney with this Petition. Please address all correspondence to lead counsel. Petitioner consents to service by email at the email addresses listed above.

2.4. Fee for *Inter Partes* Review

The USPTO is authorized to charge the filing fee and any other fees incurred by Petitioner to the deposit account of Orrick, Herrington, & Sutcliffe LLP: 15-0665.

3. REQUIREMENTS FOR *INTER PARTES* REVIEW

This Petition meets and complies with all requirements under 37 C.F.R. § 42.104 for *inter partes* review.

3.1. 37 C.F.R. § 42.104(a): Grounds for Standing

Petitioner certifies that the '122 patent is available for *inter partes* review and that Petitioner is not barred or estopped from requesting *inter partes* review challenging the patent claims on the grounds identified in this petition. Petitioner also certifies that this Petition for *Inter Partes* Review is timely filed under 35 U.S.C. § 315(b).

3.2. 37 C.F.R. § 42.104(b): Identification of Challenge

Pursuant to 37 C.F.R. § 42.104(b), Petitioner requests that the PTAB invalidate the Challenged Claims of the '122 Patent.

3.2.1 37 C.F.R. § 42.104(b)(1): Challenged Claims

Petitioner challenges claims 1-3, 5-14, 16-25, and 27-34 of the '122 patent.

3.2.2 37 C.F.R. § 42.104(b)(2): The Prior Art and Statutory Grounds

The application for the ’122 patent was filed on March 20, 2001 and does not claim priority to an earlier-filed application. This Petition therefore treats **March 20, 2001** as the priority date for the ’122 patent (the “**Priority Date**”).

The prior art references relied upon herein are:

Patent/Publication	Priority Date	Publication Date	Prior Art	Ex. No.
Korean Laid-Open Patent Application No. KR1998-074469 (“**Yun**”)[2]	Mar. 25, 1997	Nov. 5, 1998	102(b)	1003
U.S. Patent No. 5,859,466 (“**Wada**”)	June 6, 1996	Jan. 12, 1999	102(b)	1004
U.S. Patent No. 6,009,023 (“**Lu**”)	May 26, 1998	Dec. 28, 1999	102(b)	1005
U.S. Patent No. 5,960,297 (“**Saki**”)	July 2, 1997	Sept. 28, 1999	102(b)	1006

Below are the specific (pre-AIA) statutory grounds on which the claims are challenged:

Ground #1: Claims 1-2 and 11-12 are anticipated by Yun under 35 U.S.C. § 102.

[2] Since Yun published in Korean, a certified English translation and a declaration attesting to the accuracy of the translation have been appended to Exhibit 1003. All citations to Yun in this Petition refer to the translation.

Ground #2: Claims 3, 23-25 and 33-34 are obvious under 35 U.S.C. § 103 over Yun.

Ground #3: Claims 5 and 27 are obvious under 35 U.S.C. § 103 over Yun in view of Wada.

Ground #4: Claims 6-10, 13-14, 17-22 and 28-32 are obvious under 35 U.S.C. § 103 over Yun in view of Lu.

Ground #5: Claim 16 is obvious under 35 U.S.C. § 103 over Yun in view of Wada and Lu.

Ground #6: Claims 1-3, 6, 11-14, 21-25, 28 and 33-34 are obvious under 35 U.S.C. § 103 over Saki.

Ground #7: Claims 5, 16, and 27 are obvious under 35 U.S.C. § 103 over Saki in view of Wada.

Ground #8: Claims 7-10, 17-20 and 29-32 are obvious under 35 U.S.C. § 103 over Saki in view of Lu.

Again, none of the references on which these grounds are based was cited or discussed by the Examiner during prosecution of the ’122 patent.

3.2.3 Level of Ordinary Skill in the Art

A person of ordinary skill in the art (“**POSITA**”) with respect to the technology described in the ’122 patent would have had at least a Bachelor of Science degree in electrical engineering, physics, chemistry, chemical engineering,

material science, or a closely related field and at least 3 years of experience in semiconductor process, design, or fabrication. Kiaei, ¶38. An individual with an advanced degree in a relevant field would require less experience in semiconductor devices. *Id.*

This POSITA would have been familiar with the general structure of semiconductor devices, the fabrication process, isolation structures such as shallow trench isolation (STI), gate insulation layers, implant regions, and methods to improve the performance of semiconductor devices and CMOS integrated circuits. Kiaei, ¶39.

3.2.4 37 C.F.R. § 42.104(b)(5): Evidence Supporting Challenge

The Declaration of Dr. Sayfe Kiaei (Ex. 1002) ("**Kiaei**") and other supporting evidence in the Exhibit List are filed herewith. Dr. Kiaei's background and qualifications, and the information provided to him, are discussed in Ex. 1002.

4. INSTITUTION SHOULD BE GRANTED

Petitioner has established a reasonable likelihood of success on the merits and all other requirements for IPR have been met. The PTAB should institute IPR.

Petitioner's prior art references were never considered during prosecution. Thus, no ground presented here was considered by the Examiner. In fact, the Examiner applied only a single prior art reference during prosecution, in response to which the Applicant filed a Rule 131 Declaration to "swear behind" the

reference in lieu of addressing the merits of the Examiner's rejection. *See* Section 5.3, *infra*. The Examiner quickly thereafter allowed the claims without any discussion of prior art. *Id.*

The '122 patent is involved in co-pending district court proceedings between the parties. On December 20, 2019, Patent Owner initiated an action stylized as *Innovative Foundry Technologies LLC v. Semiconductor Manufacturing International Corporation et al.*, Case No. 6:19-cv-00719 (W.D. Tex.) ("**Texas Action**"). Petitioner is ***not*** a named defendant in the Texas Action; rather, Patent Owner has named related entities of Petitioner as well as four other entities as defendants in the Texas Action: Broadcom Incorporated, Broadcom Corporation, Cypress Semiconductor Corporation and DISH Networks Corporation. And on April 2, 2020, Petitioner filed a declaratory judgment action stylized as *SMIC Americas et al. v. Innovative Foundry Technologies LLC*, Case No. 3:20-cv-02256 (N.D. Cal.).

Application of the factors in *Apple Inc. v. Fintiv, Inc.*, Case No. IPR2020-00019, Paper No. 11 (Mar. 20, 2020) weigh ***against*** discretionary denial.

First, the district court proceedings are currently in its early stages. Patent Owner filed its complaint in the Texas Action less than six months ago. Moreover, the escalating pandemic adds uncertainty in the timing of the proceedings. Relevant to the second factor, a trial date has not yet been set and announcement of

a trial date is not expected soon.[3]

Second, preliminary infringement contentions were served just two months ago on April 1, 2020, and preliminary invalidity contentions were served on May 27, 2020, shortly before the filing of this Petition. Petitioner has been diligent in expeditiously preparing and filing this Petition. Further, the prior art in this Petition and the Texas Action do not overlap completely. For example, the Lu reference—which Petitioner relies on in multiple Grounds included in this Petition—is not identified in the preliminary invalidity contentions served in the Texas Action. A *Markman* hearing has been scheduled for September 18, 2020; even assuming, despite the pandemic, the *Markman* hearing occurs as scheduled, it is unclear whether the Court will have issued its claim construction order by the institution deadline.

Third, the grounds asserted in this Petition are strong. The Petition clearly demonstrates that the ’122 patent is directed to “nothing new” when considering the state of the art in the 1990s and 1980s, many years before the ’122 patent’s filing date (*see* Section 5.1, *infra*). Moreover, the Petition provides a detailed

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[3] The Scheduling Order in the Texas Action indicates that, *at the earliest*, trial could begin on September 17, 2021, one year after the *Markman* hearing (as currently scheduled).

analysis as to why the Challenged Claims are unpatentable and presents multiple grounds of invalidity for each Challenged Claim.

The factors above weigh strongly against discretionary denial and outweigh any counterargument that the remaining factors weigh towards denial. Accordingly, IPR should be instituted.

Because institution is approximately six months away, Petitioner requests the opportunity to update its analysis of these factors if the facts change. Petitioner will contact the Board should that need arise.

5. THERE EXISTS A REASONABLE LIKELIHOOD THAT THE CHALLENGED CLAIMS ARE UNPATENTABLE

5.1. Technology Background

As explained in more detail in Dr. Kiaei's Declaration, the below section introduces some basic concepts related to the technology at issue that were well known in the art.

5.1.1 Introduction to Transistors and MOSFET Technology

The '122 patent relates to transistors such as a Metal Oxide Semiconductor Field-Effect Transistor ("**MOSFET**"). MOSFETs are the most common transistors used in integrated circuits, because, among other things, of their relative ease of fabrication, lower cost, and lower power consumption. Kiaei, ¶44. MOSFETs can be either *N-type* (also known as an "**NMOS**" or "**N-channel**" transistor) or *P-type* ("**PMOS**" or "**P-channel**" transistor). Kiaei, ¶¶44-45

(discussing the properties and operation of NMOS and PMOS transistors). A complementary metal–oxide–semiconductor (CMOS) circuit refers to an integrated circuit having both NMOS and PMOS transistors formed on the same substrate. Kiaei, ¶¶44-45 (discussing CMOS circuits).

An example of a prior art transistor is depicted below, which is Fig. 1 of the '122 patent.

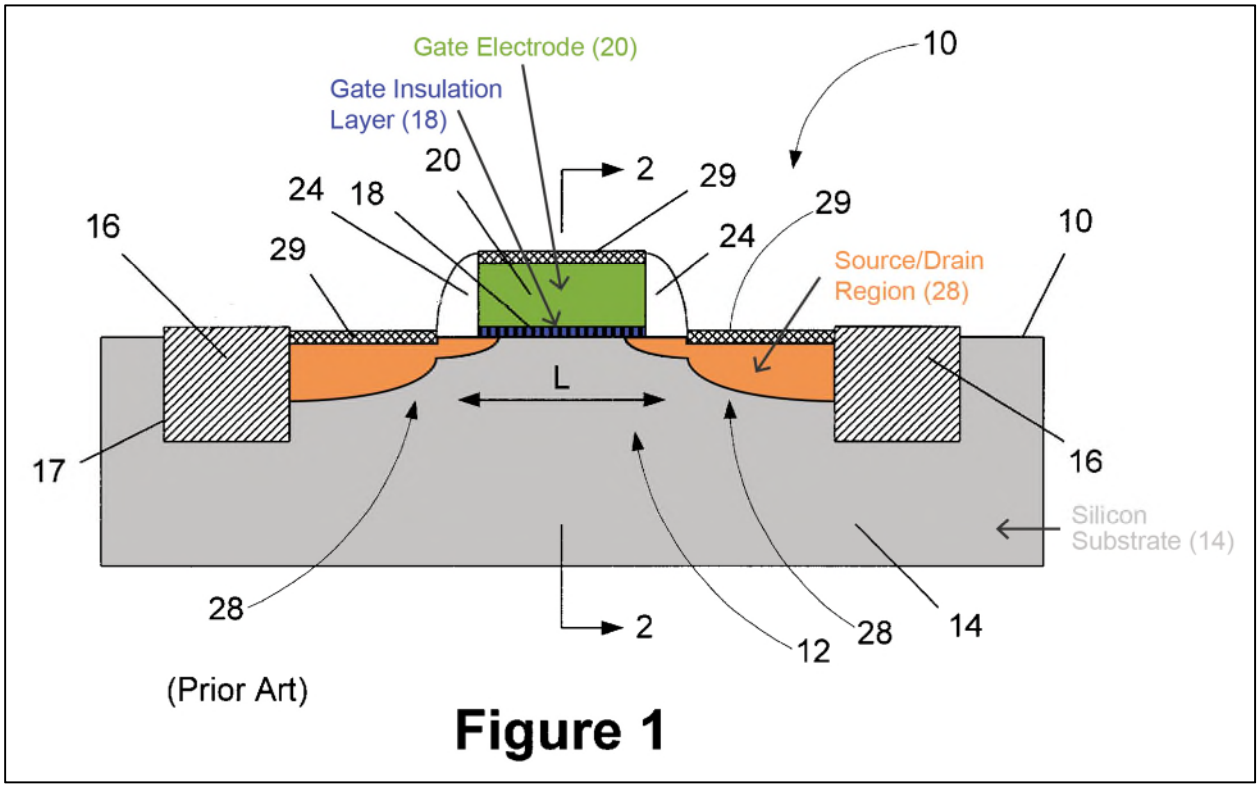


Figure 1

Specifically, a transistor (element 10) is formed in and on a silicon substrate (element 14) and has four terminals: a gate electrode (element 20) that is isolated from the substrate (element 14) by a gate insulation layer (element 18), and source

and drain regions (element 28) formed in the substrate (which can be regarded as the fourth terminal) on each side of the gate. Kiaei, ¶¶46-47.

When a voltage is applied to the gate terminal, a conducting channel is formed in the substrate that allows current to flow between the source and drain. Kiaei, ¶48. Increasing the voltage will cause the channel resistance to decrease further, causing an increase in the drain current through the channel. Kiaei, ¶49.

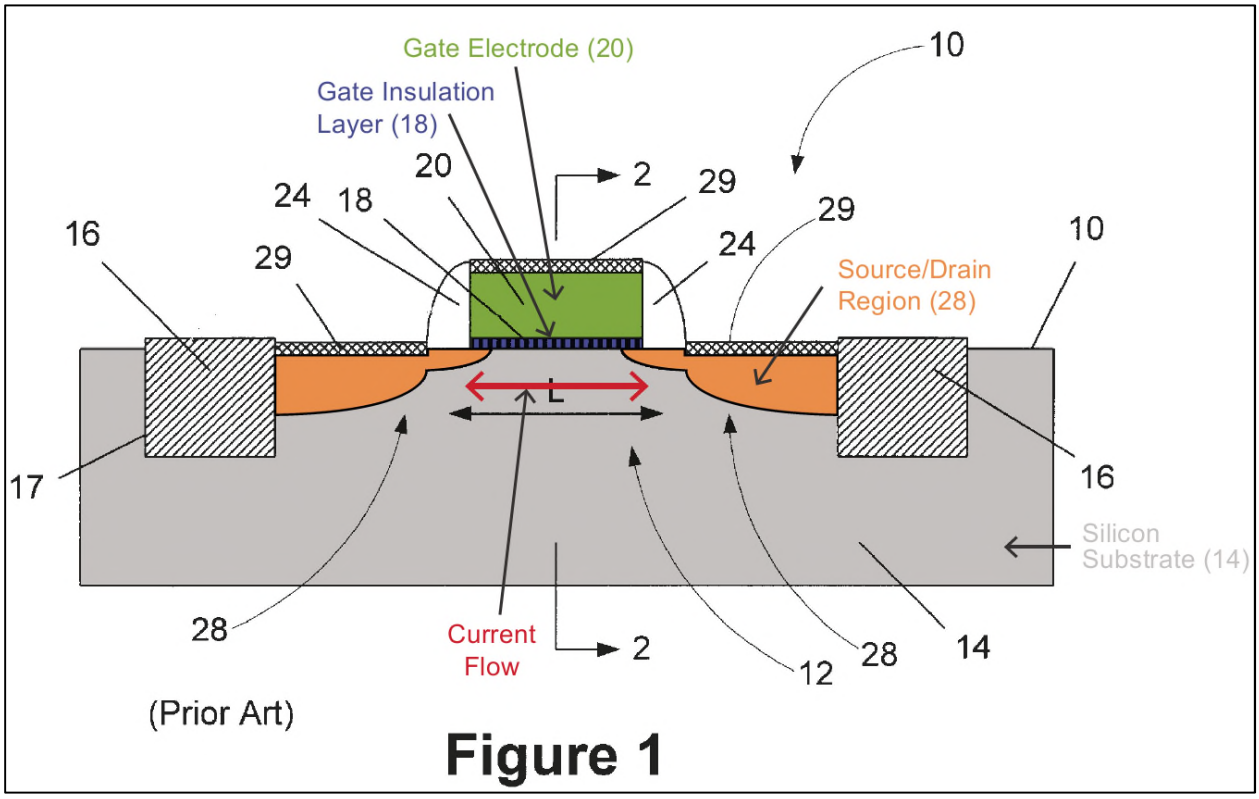


Figure 1

The source and drain are doped areas (active regions) that are the sources for particles (e.g., electrons or holes) to flow into and out of the channel. Kiaei, ¶49. The channel region is lightly doped with a dopant type that is opposite to that of the source and drain. *Id.*

The transistor gate refers to two basic components: (1) a *gate insulation layer* (also known as a "gate oxide"), and (2) a *gate electrode*. Kiaei, ¶50. The gate electrode is a conductor, often formed of polysilicon, to connect the gate input voltage to the transistor gate. *Id.* And the gate oxide isolates the gate from the substrate so that there is no current flow from the gate to the conducting channel. *Id.* The gate oxide is typically formed of silicon dioxide (SiO_2). *Id.* (discussing same and citing technical literature on this topic); *see, e.g.*, Ex. 1007 (Rubin), 1:23-25 ("The conduction is along a 'channel' that is spaced from the gate by a silicon dioxide layer, referred to as a 'gate oxide.'"); Ex. 1008 (Tao), 1:28-32 ("a substrate is typically formed with an oxide layer, such as silicon dioxide. This oxide layer may function as a gate oxide to the active devices formed on the substrate.").

The transistor operation involves the application of an input voltage to the gate electrode, which creates an electric field in the channel region. Kiaei, ¶51. The electric field can be varied to modulate the conductance of the channel region. *Id.*

5.1.2 The Need for Improved Transistor Performance

The dimensions of transistors fabricated on integrated circuits have continually shrunk over time. Kiaei, ¶52. Packing a larger number of transistors into a smaller area, however, has resulted in lower transistor performance, due to decreased *drive current*. *Id.* Drive current is a measure of current flow across the

channel region of a transistor under the gate and between the source and drain regions. Kiaei, ¶¶52-53.

Transistor performance can be increased by increasing the drive current. Kiaei, ¶¶52-53. As relevant here, the drain to source drive current ("$\boldsymbol{I_{DS}}$") of a transistor is proportional to its width ("***W***") and inversely proportional to the length ("***L***"). Kiaei, ¶53. This relationship is illustrated by the following equation:

$$I_{DS} = K' \frac{W}{L} (V_{GS} - V_{TH})^2$$

Kiaei, ¶53. Thus, increasing ***W*** or reducing ***L*** will increase the transistor's drive current. Kiaei, ¶54. Increasing ***W*** or reducing ***L***, however, affects other transistor properties and may cause an undesirable increase in the "off-state leakage current." Kiaei, ¶54. This refers to current flow between the drain and source when the transistor is *not* in an operating state (e.g., for an NMOS transistor, when the device is in the "subthreshold" or "off-state" and V_{GS} is less than V_{TH}). Kiaei, ¶54. Reducing off-state leakage current is critical to minimizing transistor and integrated circuit power consumption. Kiaei, ¶54.

5.1.3 Forming Isolation Structures in the Substrate Was Well Known in the Art

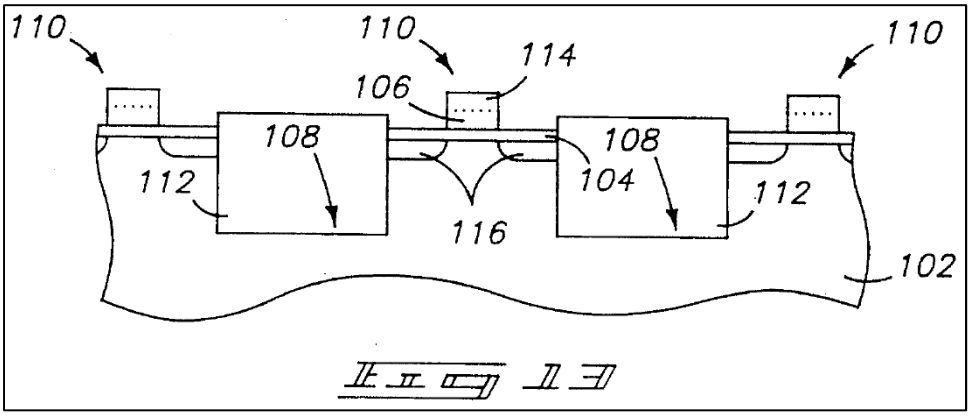
Before the '122 patent was filed in 2001, it was well known in the art to use isolation structures to electrically isolate transistors. Kiaei, ¶55. Sufficient isolation is important to the proper functioning of individual transistors and the

electronic devices that rely on them. *Id.* As an increasing number of transistors were packed into a constantly shrinking area, however, achieving isolation became more challenging. *Id.* For example, as Koike recognized in 1994:

> With the advance of microminiaturization (fine structuring) of integrated circuits, the area allowed for device isolation regions has been increasingly reduced. Thus, these conventional device isolation regions formed by means of LOCOS (Local Oxidation Of Silicon) are becoming difficult to use.

Ex. 1009 (Koike), 1:14-19.

Well known methods of isolation include Shallow Trench Isolation (STI) and Local Oxidation Of Silicon (LOCOS). Kiaei, ¶56. These methods have been utilized since the 1990s and earlier. For example, U.S. Patent No. 5,206,182, filed in 1989, describes "an improved integrated circuit process in which adjacent devices are isolated by a trench" that improves upon prior art trench processes. 1:24-30 and 1:64-66; Kiaei, ¶56. Similarly, U.S. Patent No. 5,177,028 (filed in 1991) describes "a method for isolating field effect transistors using trench isolation techniques" as shown in its Fig. 13 below:



Kiaei, ¶56.

5.2. Description of the Alleged Invention of the '122 Patent

The '122 patent relates generally to a "semiconductor device having an enhanced width dimension." Ex. 1001, 1:10-11; Kiaei, ¶57.

The '122 patent states that the "demand for increased speed has resulted in a continual reduction in the size of semiconductor devices." Ex. 1001, 1:18-20; Kiaei, ¶58. A transistor's speed and overall performance depends on its "drive current," which the '122 patent defines as "the amount of current flowing from the drain region to the source region of the transistor." Ex. 1001, 1:62-66; Kiaei, ¶58. As discussed above and recognized in the prior art, the '122 patent explains that the drive current, in turn, depends on the transistor's channel length ("***L***") and width ("***W***"). Ex. 1001, 2:5-20; Kiaei, ¶58. Specifically, reducing ***L*** or increasing ***W*** results in increased drive current. Ex. 1001, 2:5-20; Kiaei, ¶58.

According to the '122 patent, it is desirable to maximize the drive current without otherwise adversely impacting the transistor's performance, such as

"generating excessive heat or excessive off-state leakage currents." Ex. 1001, 1:66 – 2:4; Kiaei, ¶59. In this regard, the '122 patent notes that off-state leakage current increases *exponentially* as ***L*** decreases; in contrast, the leakage current increases at a lower rate as ***W*** increases. Ex. 1001, 2:5-20; Kiaei, ¶59. "Thus, it would be desirable to have a transistor in which the width dimension of a substrate can be maximized in a given plot space of semiconducting substrate." Ex. 1001, 2:35-38; Kiaei, ¶59.

Figures 3 – 7C depict the semiconductor device contemplated by the '122 patent. Kiaei, ¶60. The figures show the semiconductor device at various stages of the fabrication process. *Id.* Fig. 6B, for example, is a view of the device along the *transistor gate width (**W**) dimension* after the gate electrode has been patterned from a layer of polysilicon. Ex. 1001, 5:33-45; Kiaei, ¶60. And Fig. 7A, which shows the device after the subsequent step of forming source/drain regions, shows the device along the *transistor gate length (**L**) dimension*. Ex. 1001, 5:58-65; Kiaei, ¶60. The annotations of Figs. 7A and 6B provided below illustrate the relevant device elements visible in each view (certain elements may be visible in one view, but not another). Kiaei, ¶¶60-61 (discussing same).

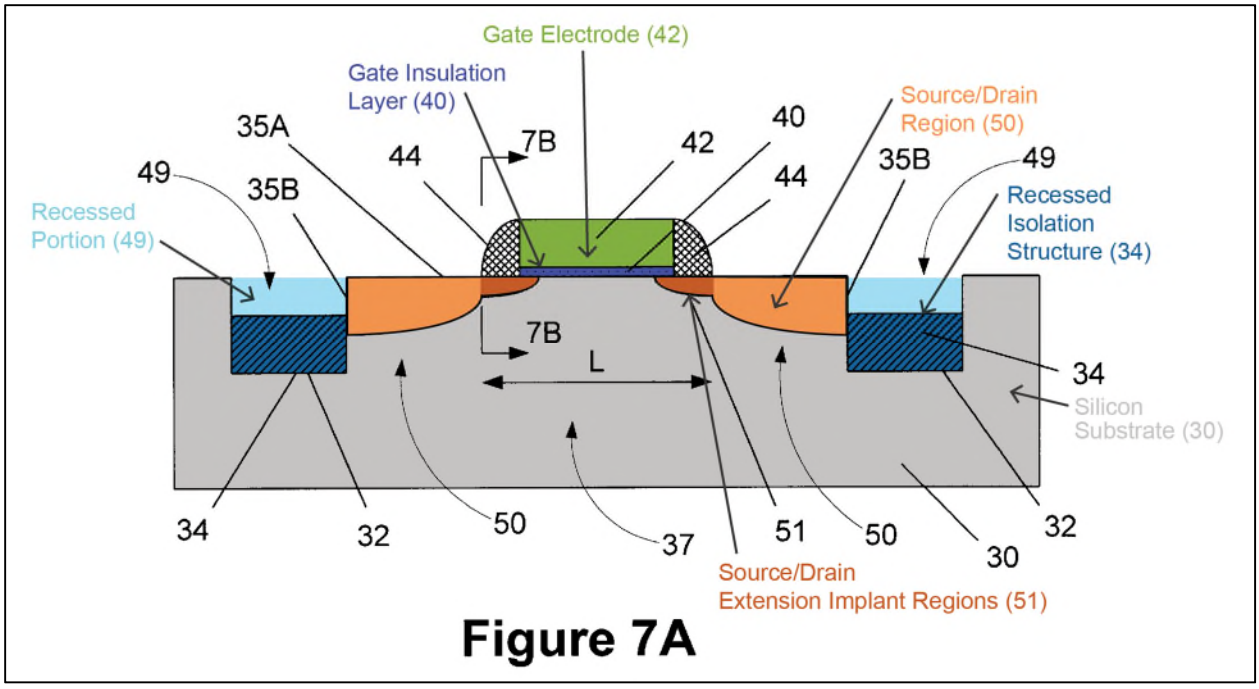


Figure 7A

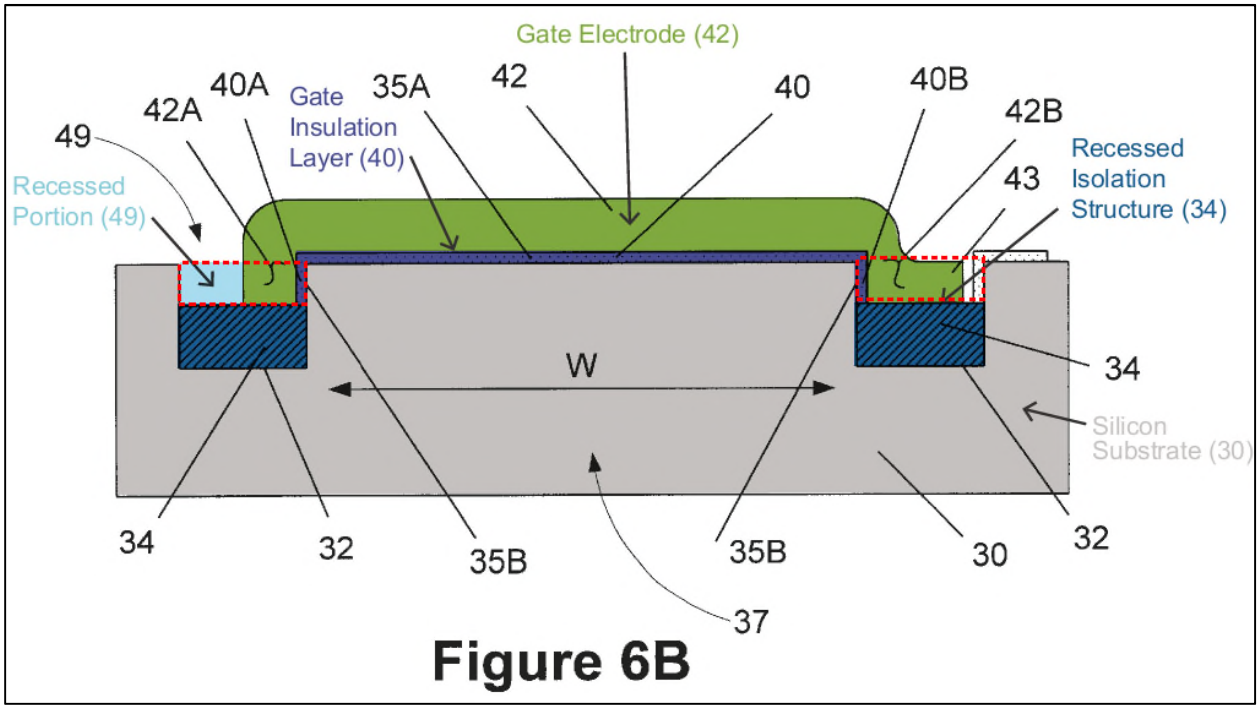


Figure 6B

The transistor includes substrate 30 with gate electrode 42 and gate insulation layer 40 formed on the substrate. Ex. 1001, 6:62 – 7:3; Kiaei, ¶62.

Recessed isolation structure 34,[4] as well as source and drain regions 50, are formed in the substrate. Ex. 1001, 5:58-63; 7:45 – 55; Kiaei, ¶62. Further, recessed isolation structure 34 defines a recessed portion (indicated by element 49) and includes a layer of insulating material in the trench 32. Ex. 1001, 4:21-56; Kiaei, ¶62. The recessed portion includes the full void above the insulating material as indicated by the red dashed lines in annotated Fig. 6B above; Kiaei, ¶62. And as depicted in Fig. 6B, the recessed portion is partially filled in by the gate insulation layer and gate electrode; Kiaei, ¶62.

5.3. Prosecution History of the '122 Patent

The '122 patent was filed on March 20, 2001 and assigned Application No. 09/812,521 ("**'521 application**"). On June 18, 2002, the Examiner issued a two-way restriction that required applicant to select between claims 1-34 ("drawn to a semiconductor device") and 35-55 ("drawn to a method of making a semiconductor device"). Ex. 1012 at 73-76. Applicant selected device claims 1-34. Ex. 1012 at 77-78 (July 2, 2002 Response to Restriction).

The Examiner subsequently issued an Office Action rejecting claims 1-34 as obvious under 35 U.S.C. § 103(a) over JP 2001-036048A to Fukatsu. Ex. 1012 at

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[4] The '122 patent uses the term "recessed isolation material" to refer to the same element 34.

79-83 (Sept. 25, 2002 Office Action). In rejecting the claims, the Examiner reasoned:

> Fukatsu discloses the claimed invention in general, however fails to disclose the particulars of as disclosed in the claims. **Therefore, the examiner takes *official notice* that the gate, gate insulation, isolation material and drain extension region are well known to be used** when making a semiconductor device. **Also, [i]t would have been obvious to one of ordinary skill in the art at the time the invention was made to form the trench to the depth and width and the thickness of the electrode and gate insulation as claimed**, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

Ex. 1012 at 79-83 (Sept. 25, 2002 Office Action).

Notably, Applicant declined to address the Examiner's reasoning or characterization of the claim limitations as being well known in the art and obvious to a POSITA at the time of the application's filing. Applicant instead filed a declaration under 37 C.F.R. § 1.131 to "establish that the Fukatsu patent is not prior art to the present application." Ex. 1012 at 85-89 (Feb. 3, 2003 Response to

Office Action). Applicant's response omitted any discussion of whether the claim limitations were well known in the art and obvious to a POSITA.

One month later, the Examiner issued a Notice of Allowance. Ex. 1012 at 109-111 (March 11, 2003 Notice of Allowance). The Examiner stated only that "the prior art of record fails to disclose" the claim limitations, without providing any details. *Id.* In this regard, the Examiner's reasons for allowance are no different than the Examiner's prior Office Action, in which the Examiner stated "Fukatsu discloses the claimed invention in general, however fails to disclose the particulars of as disclosed in the claims." Ex. 1012 at 79-83 (Sept. 25, 2002 Office Action).

Other than Fukatsu, the Examiner made no reference to any prior art of record.

5.4. Proposed Claim Construction

The PTAB applies the *Phillips* claim construction standard to construe a claim term subject to IPR. *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-19 (Fed. Cir. 2005) (en banc). Under this standard, claim terms are given their ordinary and customary meaning, as would have been understood by a person of ordinary skill in the art at the time of the invention, in light of the language of the claims, the specification, and the prosecution history of record. *See Thorner v. Sony Comput. Entm't Am. LLC*, 669 F.3d 1362, 1365-66 (Fed. Cir. 2012).

Petitioner does not believe that any construction is needed to determine whether to institute, and therefore does not propose any construction. *See, e.g.*, *Netflix, Inc. v. Uniloc 2017 LLC*, Case No. IPR2020-00041, Paper No. 10 at 15 (Mar. 25, 2020) ("our determination whether to institute does not depend on a construction of any claim terms or phrases") (citing *Nidec Motor Corp. v. Zhongshan Broad Ocean Motor Co.*, 868 F.3d 1013, 1017 (Fed. Cir. 2017); *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999)).

Because Petitioner is not yet aware of Patent Owner's claim construction position, Petitioner reserves the right to respond to any such construction in Petitioner's reply brief.

5.5. Invalidity Based on Yun

Yun relates to semiconductor devices and methods for manufacturing them. Like the '122 patent, Yun is directed to increasing the drive current of a transistor by increasing the channel width. Ex. 1003 (Yun), 1-5 and 2-5;[5] Kiaei, ¶66. In particular, Yun describes that:

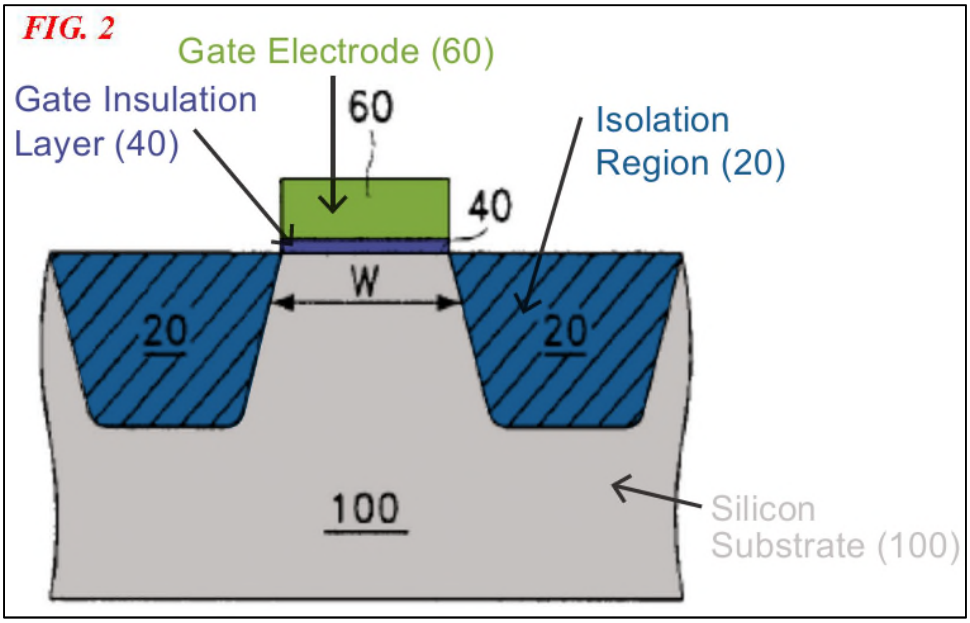
> It is the object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can

[5] All references to Yun are to the certified English translation that begins on page 7 of Exhibit 1003.

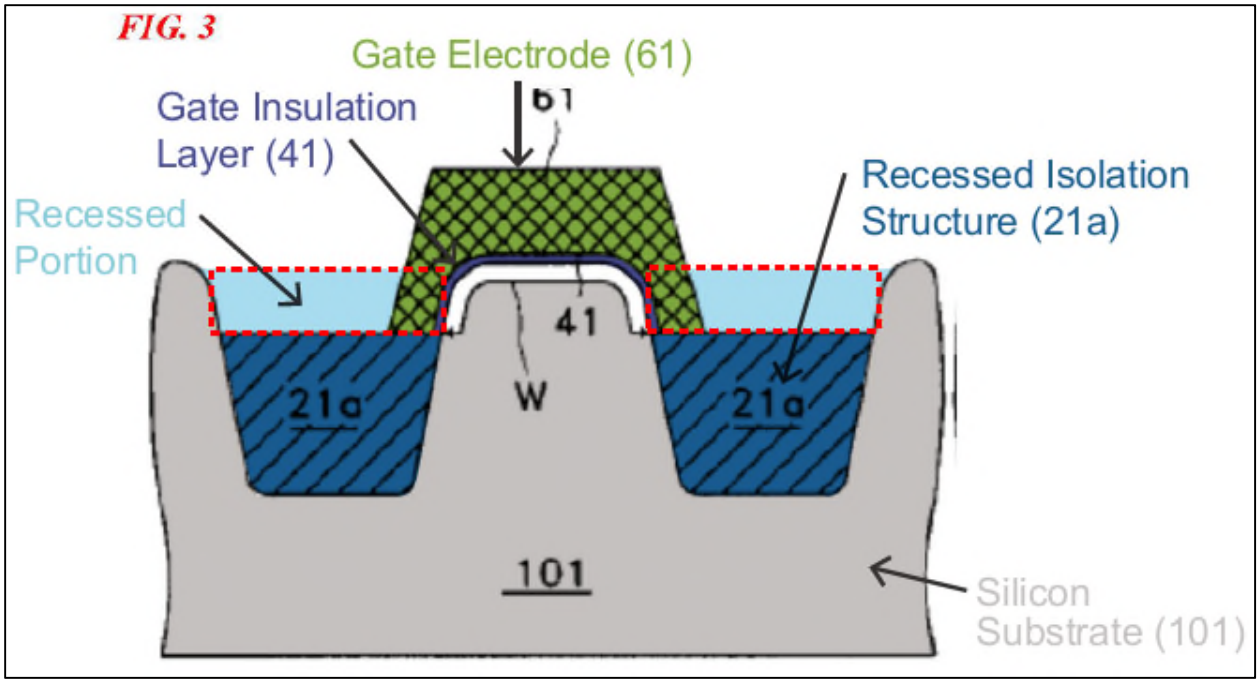
> ***improve the electric current driving capability of a transistor by increasing the channel width*** without increasing the chip area by vertically forming a part of the channel region.

Ex. 1003, 2-5. In short, Yun teaches increasing the effective width of the transistor active area without increasing the chip size. Ex. 1003, 2-5; Kiaei, ¶66.

With respect to Fig. 2 below, Yun discloses a prior art transistor having: (i) "a channel region W directly formed on a silicon substrate 100"; (ii) "an isolation region 20 for isolating the device"; (iii) "a gate oxide film 40 formed on top of channel width W"; and (iv) "gate electrode 60 formed thereon." Ex. 1003, 1-5; Kiaei, ¶66. As Yun explains: "when the channel width W is increased to increase the current-driving amount of a transistor, it immediately results in an increase in the size of the area." Ex. 1003, 1-5. An increase in chip area becomes problematic as more and more transistors are packed into constantly shrinking device sizes. Kiaei, ¶67.



To improve upon the prior art transistor, Yun teaches the transistor depicted in Fig. 3 below. Kiaei, ¶68. Yun's transistor includes: (i) "isolation regions 21a" formed on silicon substrate 101 and with a gate formed between the isolation regions; (ii) "gate oxide film 41" formed "on the area where the silicon substrate is higher by a predetermined height relative to the upper part of the isolation region 21a"; and (iii) "a gate electrode 61" formed "on the upper part thereof." Ex. 1003, 2-5; Kiaei, ¶68.



As Yun explains:

> ***[T]he channel width is raised by a predetermined height relative to the isolation region 21a and for a curve by as much as the height, thereby increasing the channel width***. In doing so, there will not be any change in the chip area.

Ex. 1003, 2-5. By forming the transistor in this way, Yun notes that it is possible "to obtain stable isolation characteristics while increasing the channel width of a transistor by adjusting the depth of the oxide film in the trench." Ex. 1003, 2-5; Kiaei, ¶69. In other words, the channel width can be further increased by extending gate electrode 61 and gate oxide film 41 further into the trench. *Id.* This is accomplished by reducing the depth of the oxide film in the trench. *Id.*

5.5.1 Ground #1: Claims 1-2 and 11-12 Are Anticipated By Yun

5.5.1.1. Claim 1

(i) [1.P] "A transistor, comprising:"

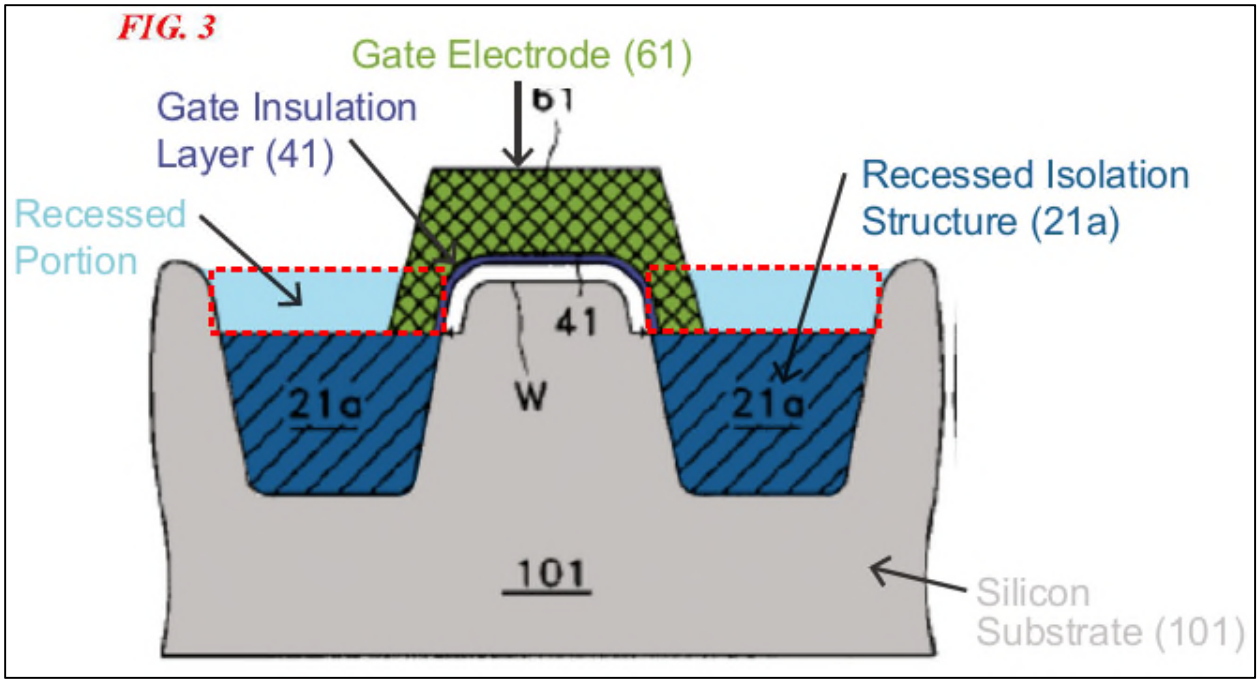
Yun discloses a transistor. *See* Ex. 1003, 1-5 and 2-5; Kiaei, ¶70.

(ii) [1.1] "a semiconducting substrate;"

Yun discloses forming a transistor on substrate 101. Ex. 1003, 2-5; Kiaei, ¶71. Substrate 101 is formed of silicon. Ex. 1003, 2-5; Kiaei, ¶71.

(iii) [1.2] "a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove;"

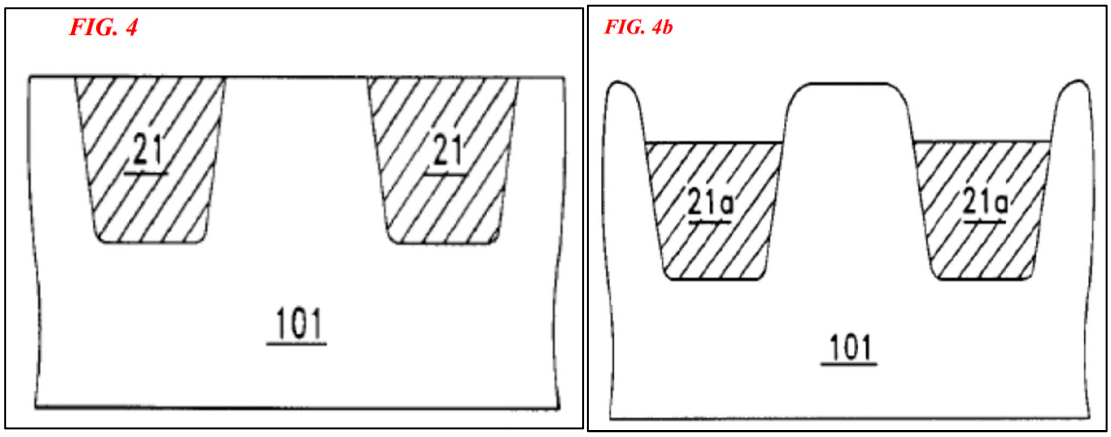
Yun discloses a transistor having isolation regions 21a formed on substrate 101, as depicted in Fig. 3 below. Kiaei, ¶72. Isolation region 21 includes an oxide film—an insulating material—formed inside the trench. *Id.* As can be verified visually, isolation region 21 defines a recess in the region above the oxide film. Ex. 1003, 2-5; Kiaei, ¶72. The recessed portion includes the full void above the insulating material as indicated by the red dashed lines in annotated Fig. 3 below. Kiaei, ¶72. And as shown, the recessed portion is partially filled in by the gate insulation layer and gate electrode. *Id.*



Yun's Figs. 4a and 4b (reproduced below) provide views of the transistor fabrication process and further illustrate the formation of the recessed isolation region. Kiaei, ¶73. Fig. 4a describes forming isolation region 21a using a "conventional trench isolation process." Ex. 1003, 2-5; Kiaei, ¶73. And in Fig. 4b, the oxide film in the trench is etched in order to increase the channel width, thereby forming the recess above. Kiaei, ¶73. As Yun explains:

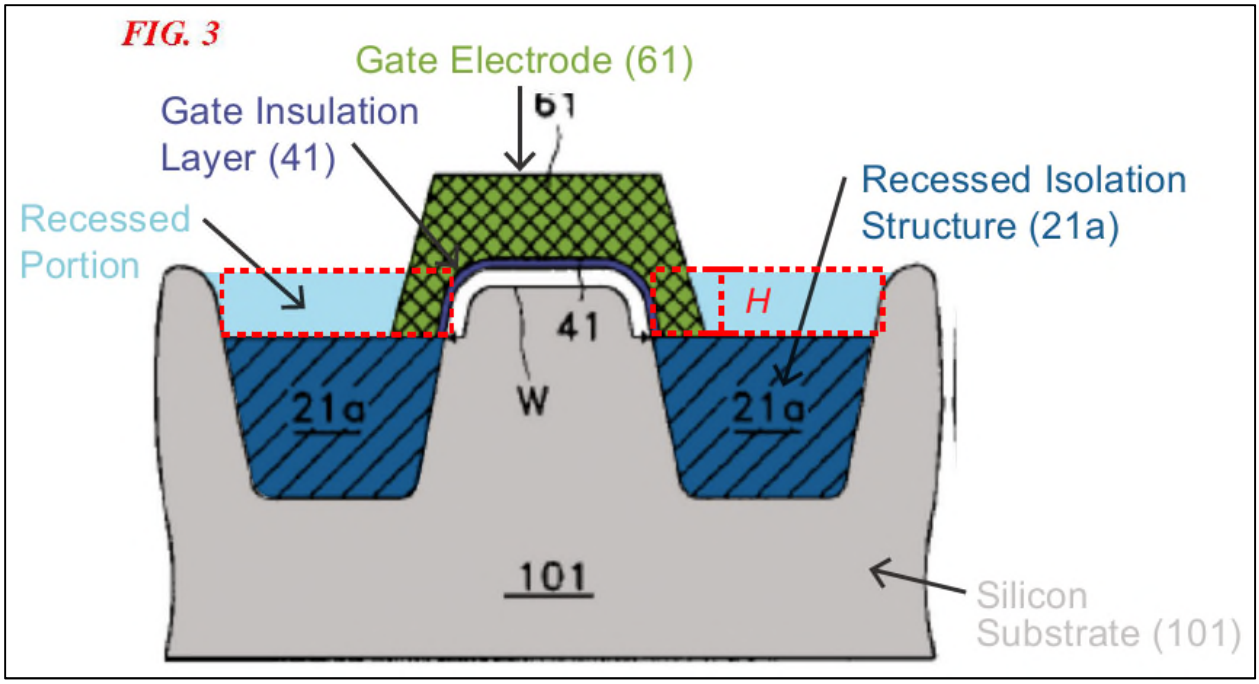
> With reference to FIG. 4b, the oxide film 21a inside the trench isolation in the region desired to increase the channel width is etched by 10nm – 200nm by means of a wet etching process. Also, the sacrificial oxide film is sacrificed by 10nm – 30nm to allow the channel region in the angular part to become a more curved surface, thereby increasing the channel width W.

Ex. 1003, 2-5.



(iv) **[1.3] "a gate electrode and a gate insulation layer formed above said substrate, a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure; and"**

Yun teaches the formation of gate electrode 61 and gate insulation layer above substrate 101. Ex. 1003, 2-5. As can be verified visually with reference to Fig. 3, the end portions of gate electrode 61 and gate insulation layer 41 extend into the recess above the oxide film inside the trench (*see* element 21a). Kiaei, ¶74. As Yun explains, extending gate electrode 61 and gate insulation layer 41 into the trench increases the channel width of the transistor. Ex. 1003, 2-5; Kiaei, ¶74. In particular, the effective width is increased by an amount equal to the height by which gate electrode 61 and gate insulation layer 41 are raised above isolate region 21a, as illustrated by the height of the curve ("***H***") in the figure below. Ex. 1003, 2-5; Kiaei, ¶74.

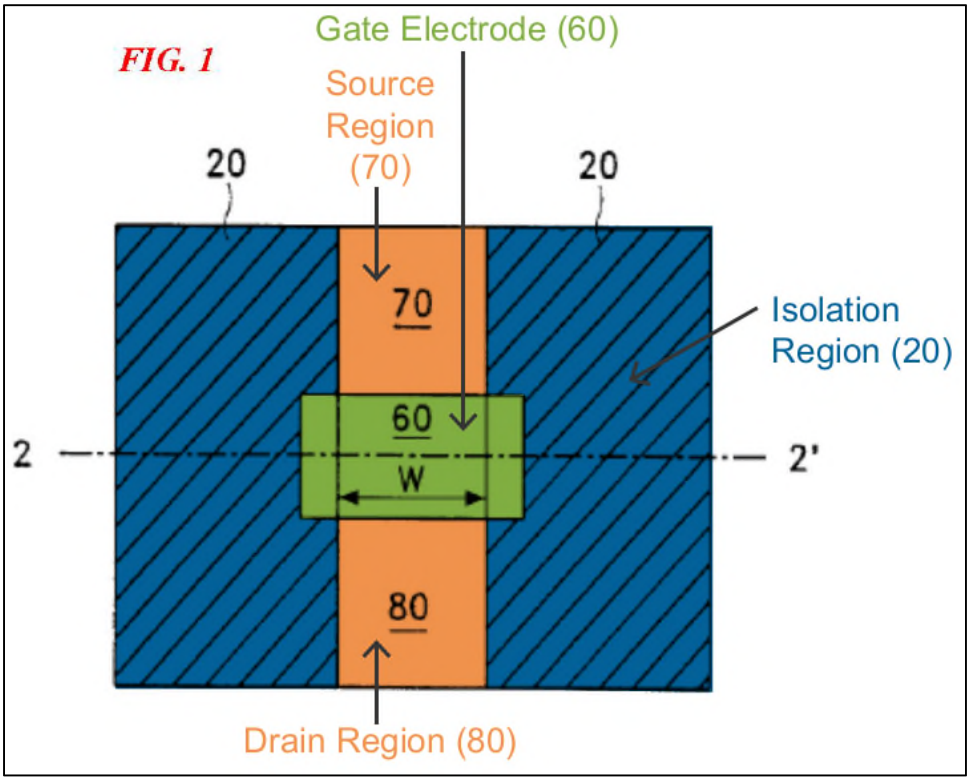


(v) **[1.4] "a source region and a drain region formed in said substrate."**

Yun notes that the completed transistor includes a source region and a drain region formed in the substrate. Kiaei, ¶75. As Yun explains:

> With reference to FIG. 4c, after the process described above is performed, ***a transistor is formed by means of*** a gate oxide 41 formation process and ***a source and drain formation process***.

Ex. 1003, 2-5. Yun describes forming source and drain regions using a "conventional" process (Ex. 1003, 1-5 and 2-5); these regions are formed in substrate 101. Kiaei, ¶76. For example, Yun's Fig. 1 (reproduced below) depicts source 70 and drain 80 formed in the substrate of a prior art transistor fabricated from a conventional process. *Id.*



5.5.1.2. Claim 2

(i) **[2] "The transistor of claim 1, wherein said semiconducting substrate is comprised of silicon"**

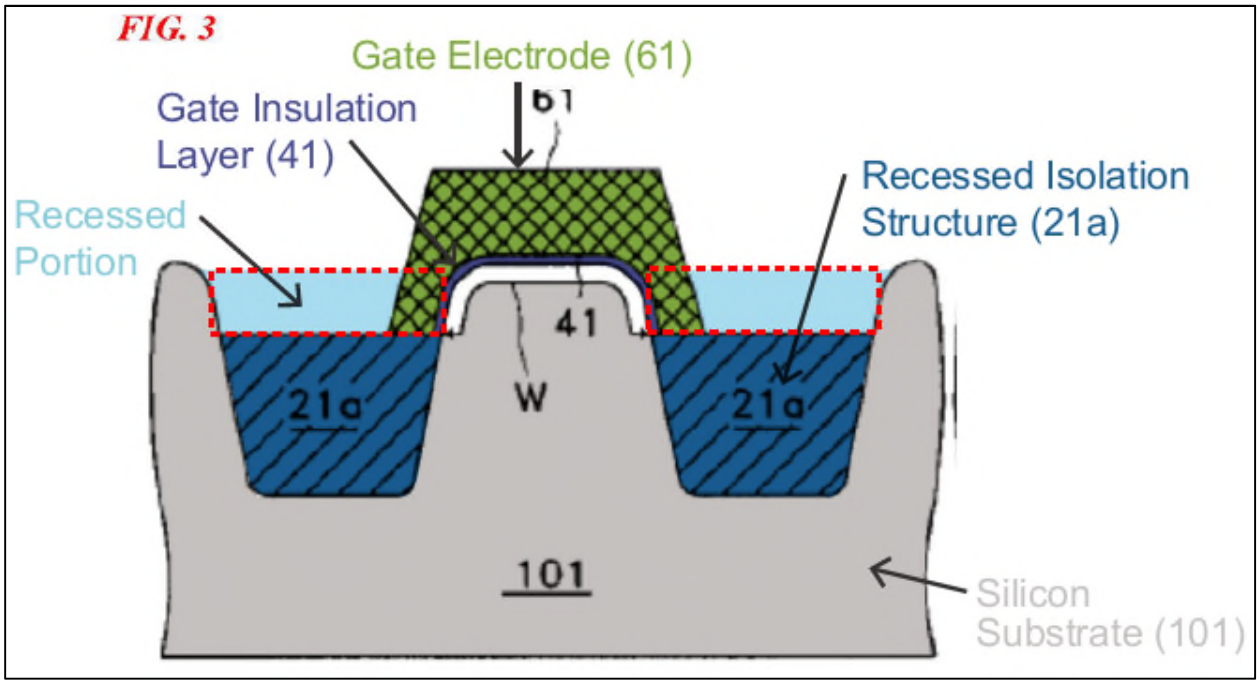
As discussed in Section 5.5.1.1, *supra*, Yun discloses claim 1. Further, Yun discloses forming a transistor on silicon substrate 101. Kiaei, ¶¶78-79.

5.5.1.3. Claim 11

(i) **[11] "The transistor of claim 1, wherein said gate electrode has first and second end portions that extend into said recess"**

As discussed in Section 5.5.1.1, *supra*, Yun discloses claim 1. Further, Yun discloses that gate electrode 61 extends into the recess above the oxide film inside the trench. *See* Section 5.5.1.1(iv); Kiaei, ¶82. Specifically, first and second end

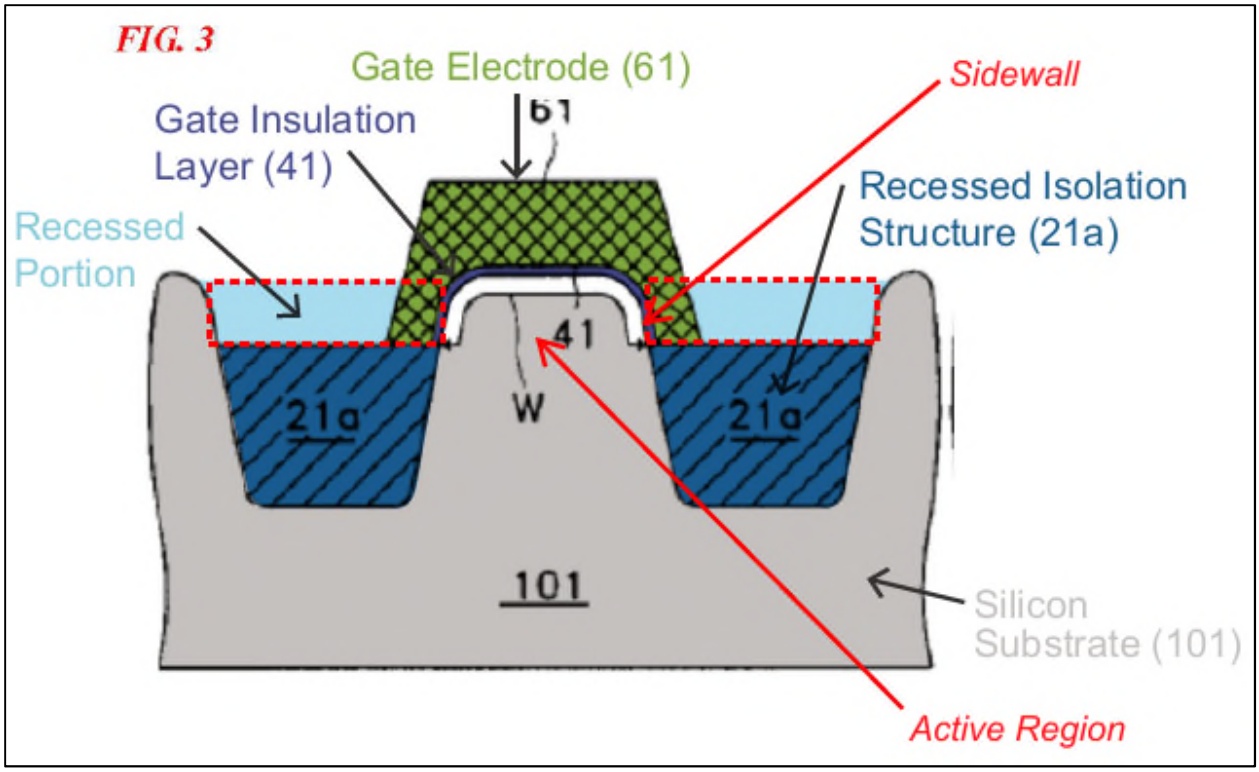
portions of gate electrode 61 extend into the recess, as illustrated by the annotated figure below. Kiaei, ¶82.



5.5.1.4. Claim 12

(i) **[12] "The transistor of claim 11, wherein said first and second end portions extending into said recess are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure"**

As discussed in Sections 5.5.1.3, *supra*, Yun discloses claim 11. Further, as can be verified easily by reference to Yun's Fig. 3 below, the first and second end portions of gate electrode 61 are positioned above a portion of a sidewall of the active region:



Kiaei, ¶¶84-85.

5.5.2 Ground #2: Claims 3, 23-25 and 33-34 Are Obvious Over Yun In Light of the Knowledge of a POSITA

5.5.2.1. Claim 3

(i) **[3] "The transistor of claim 1, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride"**

As discussed in Section 5.5.1.1, *supra*, Yun discloses claim 1. Yun also discloses claim 3 for the reasons provided below. Kiaei, ¶87.

Yun discloses forming a recessed isolation structure (isolation region 21a), which includes an oxide film formed inside the trench. Kiaei, ¶88. An oxide film, in the field of semiconductor fabrication, includes the class of silicon dioxide

(SiO_2) insulators, which is one of the most common CMOS gate insulators used in the art. *Id.* (discussing same and citing technical literature on this topic). Indeed, Tao notes that "a substrate is typically formed with an oxide layer, such as silicon dioxide. This oxide layer may function as a gate oxide to the active devices formed on the substrate." Ex. 1008 (Tao), 1:28-32; Kiaei, ¶88. Further, "oxide" and "oxide film" are well understood in the field of semiconductor fabrication as terms that refer to silicon dioxide. Kiaei, ¶88 (discussing same and citing technical literature on this topic).

Further, a POSITA, reading Yun, would understand Yun's oxide film as being silicon dioxide when considering that Yun uses a ***silicon*** substrate. Kiaei, ¶¶89-90.

5.5.2.2. Claim 23

(i) **[23.P] "A transistor, comprising:"**

See claim [1.P].

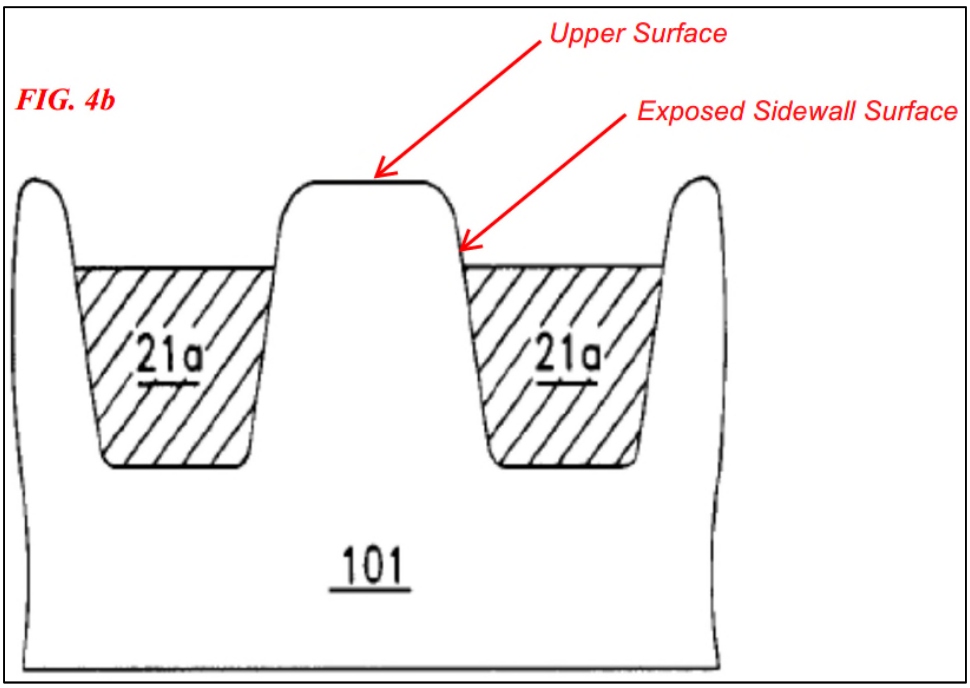
(ii) **[23.1] "a semiconducting substrate;"**

See claim [1.1].

(iii) **[23.2] "a recessed isolation structure defining an active area having an upper surface and an exposed sidewall surface;"**

For the reasons described in Section 5.5.1.1(iii), *supra*, Yun discloses this claim limitation.

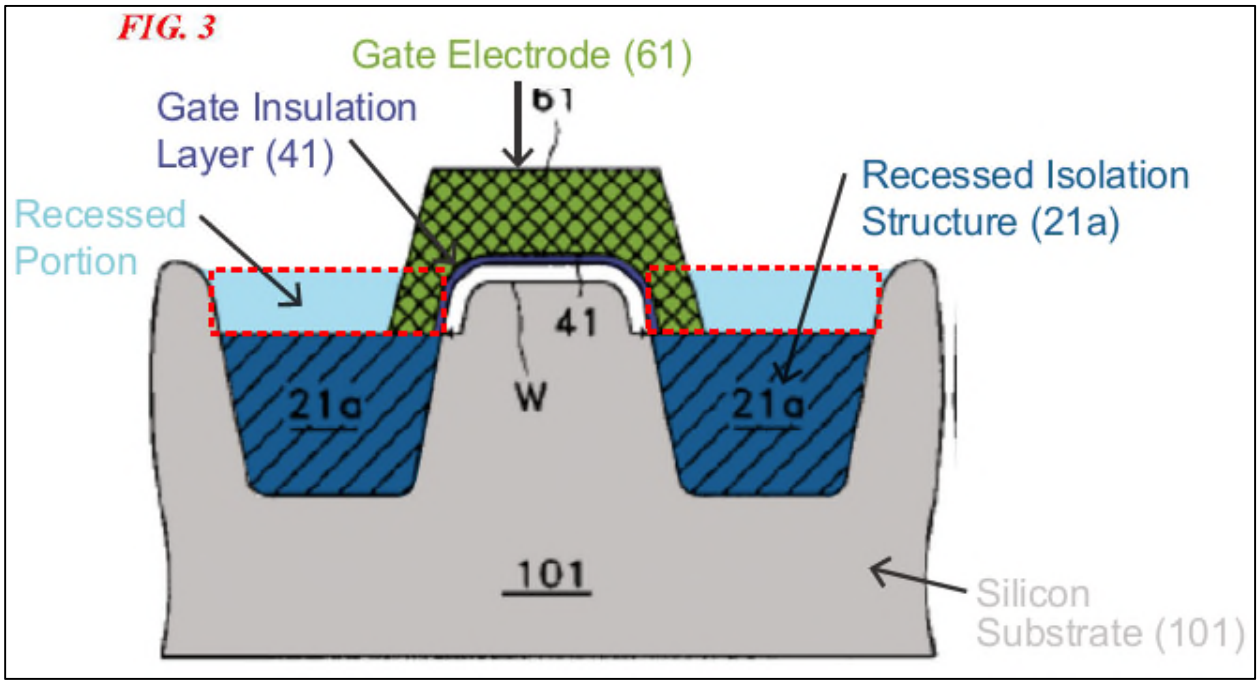
Yun discloses "a process of ***forming a trench isolation region and an active region on a silicon substrate*** by means of a conventional trench isolation process." Ex. 1003, 1-5; Kiaei, ¶94. Specifically, Yun teaches forming isolation regions 21a, which include a recessed portion over a portion filled with an oxide film insulator, as illustrated in annotated Fig. 4b below. Kiaei, ¶94. As shown, isolation regions 21a define an active area having an upper surface and an exposed sidewall surface. *Id.*



(iv) **[23.3] "a gate insulation layer and a gate electrode positioned above a portion of said upper surface and a portion of said exposed sidewall surface of said active area; and"**

For the reasons described in Section 5.5.1.1(iv), *supra*, Yun discloses this claim limitation.

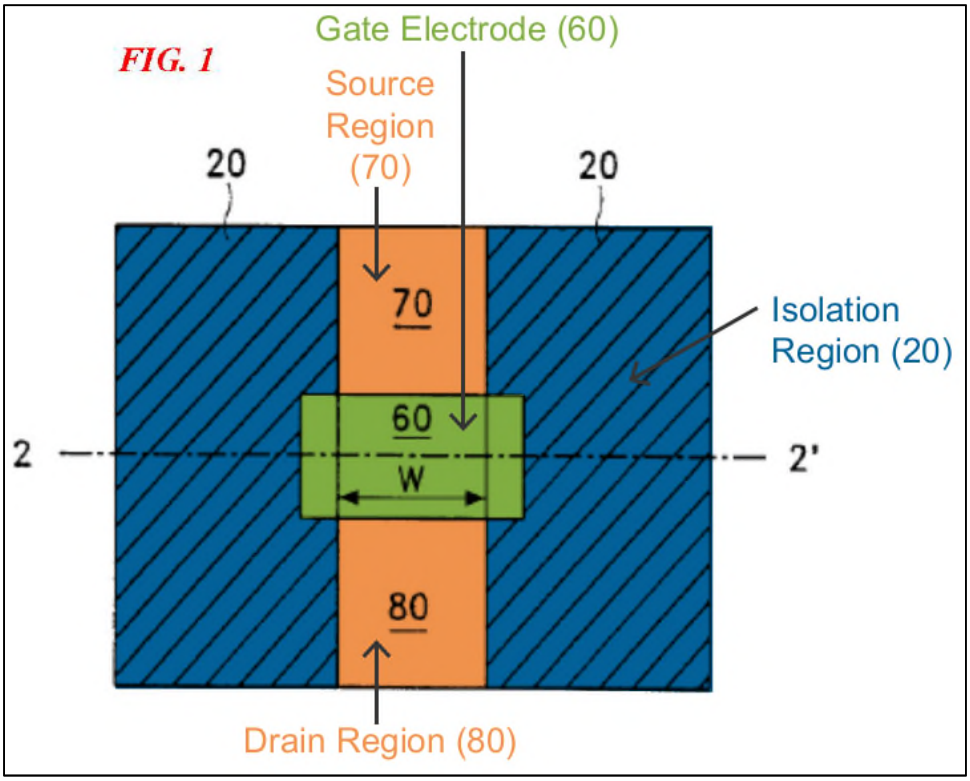
Yun teaches forming gate electrode 61 and gate insulation layer 41 above substrate 101. Kiaei, ¶96. Specifically, Yun discloses that "a ***gate oxide film 41 is formed on the area where the silicon substrate is higher*** by a predetermined height relative to the upper part of the isolation region 21a; and a ***gate electrode 61 is formed on the upper part thereof***." Ex. 1003, 2-5; Kiaei, ¶96. And as can be verified visually from Yun's Fig. 3 below, gate electrode 61 and gate insulation layer 41 are positioned above the upper surface and exposed sidewall surface of the active area. Kiaei, ¶96.



(v) **[23.4] "a source region and a drain region formed in said active area."**

For the reasons described in Section 5.5.1.1(v), *supra*, Yun discloses this claim limitation.

Yun discloses "a process of forming ***conventional*** gate oxide film, gate electrode, ***source, and drain***." Ex. 1003, 1-5; Kiaei, ¶98. As Yun explains: "Here, the width W of the channel formed at the lower part of the gate 60 is formed with the same width as that of the source 70 and the drain 80." Ex. 1003, 1-5. Thus, as can be visualized from Yun's Fig. 1 below, the source and drain regions are formed on either side of the gate electrode and would extend below the upper surface to form a conducting channel for the transistor drive current. Kiaei, ¶98.



A POSITA, reading Yun, would recognize that conventional source and drain regions are formed in the active area over the substrate. Kiaei, ¶99. For example, Fig. 1 of the '122 patent shows an "illustrative ***prior art transistor*** in the transistor length direction" ('122 patent, 3:9-10); as shown in the annotated figure

below, active area 12 includes source/drain regions 28, as indicated by the red dashed lines. Kiaei, ¶99.

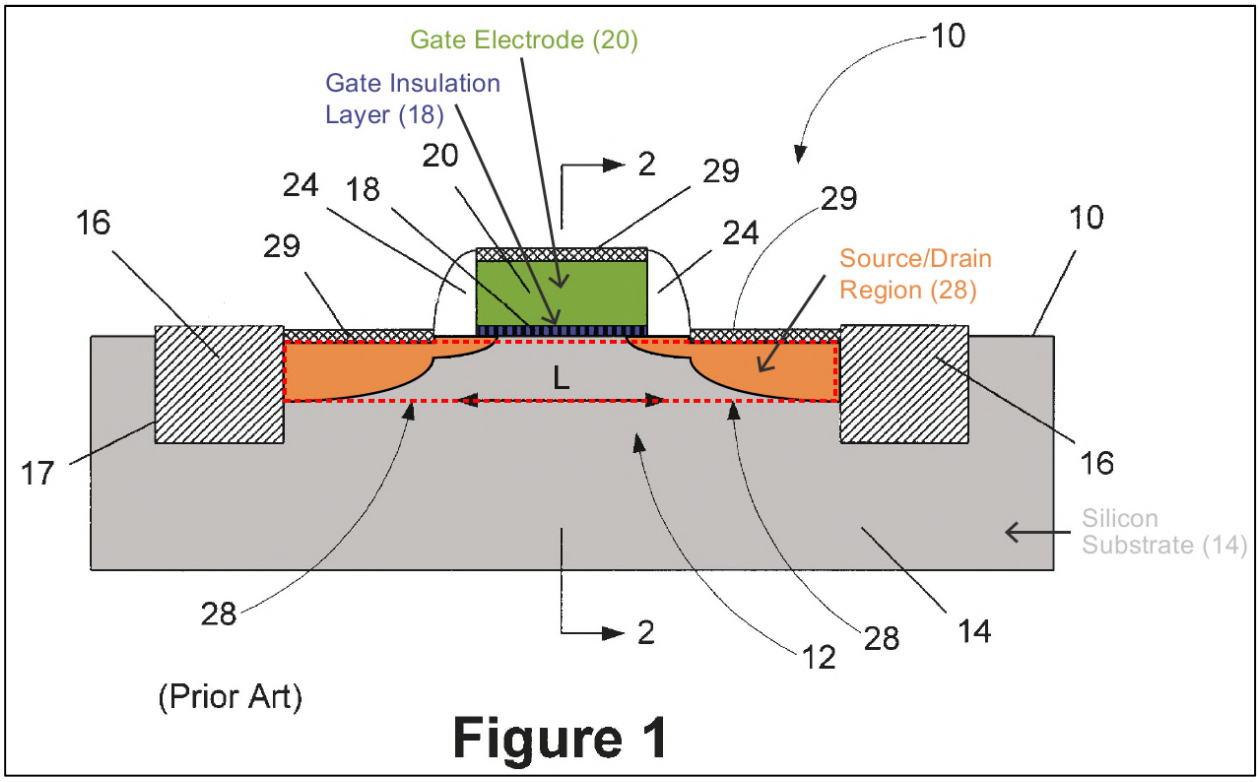


Figure 1

5.5.2.3. Claim 24

(i) **[24] "The transistor of claim 23, wherein said semiconducting substrate is comprised of silicon."**

Claim 24, which depends from claim 23, is identical to claim 2. As discussed in Sections 5.5.1.2 and 5.5.2.2, *supra*, Yun discloses claims 2 and 23, respectively. Thus, Yun further discloses claim 24. Kiaei, ¶¶101-102.

5.5.2.4. Claim 25

(i) **[25] "The transistor of claim 23, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride."**

Claim 25, which depends from claim 23, is identical to claim 3. As discussed in Sections 5.5.2.1 and 5.5.2.2, *supra*, Yun discloses claims 3 and 23, respectively. Thus, Yun further discloses claim 25. Kiaei, ¶¶104-105.

5.5.2.5. Claim 33

(i) **[33] "The transistor of claim 23, wherein said gate electrode has first and second end portions that extend into a recess in said substrate defined by said recessed isolation structure."**

Claim 33, which depends from claim 23, is identical to claim 11. As discussed in Sections 5.5.1.3 and 5.5.2.2, *supra*, Yun discloses claims 11 and 23, respectively. Thus, Yun further discloses claim 33. Kiaei, ¶¶107-108.

5.5.2.6. Claim 34

(i) **[34] "The transistor of claim 33, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure."**

Claim 34, which depends from claim 33, is identical to claim 12. As discussed in Sections 5.5.1.4 and 5.5.2.5, *supra*, Yun discloses claims 12 and 33, respectively. Thus, Yun further discloses claim 34. Kiaei, ¶¶110-111.

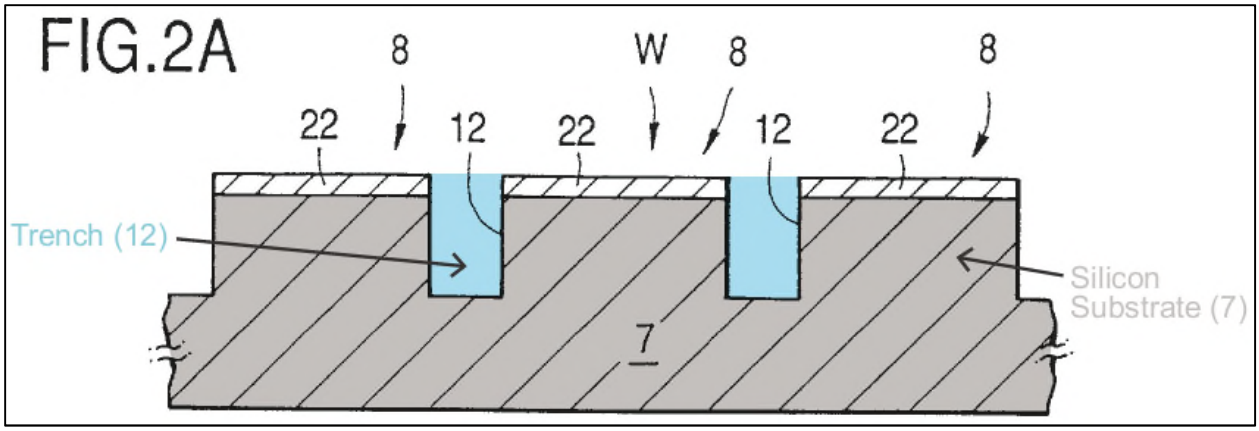
5.5.3 Ground #3: Claims 5 and 27 Are Obvious Over Yun and Wada

5.5.3.1. Wada

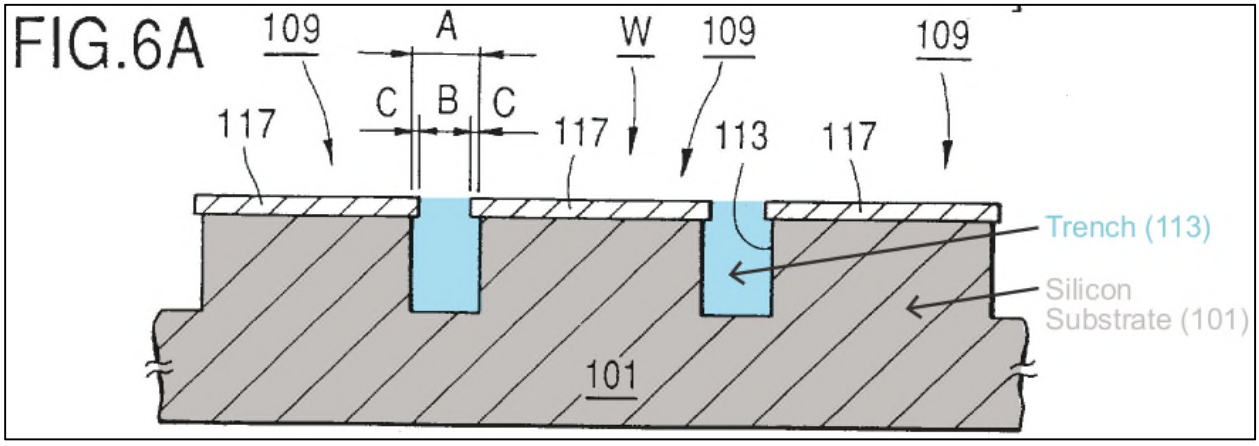
Wada relates to semiconductor devices and is directed to techniques for isolating transistors. Ex. 1004 (Wada), 1:8-12; Kiaei, ¶112. Specifically, Wada improves upon conventional methods of "field-shield device isolation" (FSDI), which includes forming an isolation structure in between two active regions of an integrated circuit to isolate the two devices from each other. Ex. 1004, 1:29-38; Kiaei, ¶112. Wada achieves this by forming the isolation structure in a "trench cavity" having dimensions tailored to the device parameters (e.g., the depth of the trench relates to properties of the source/drain diffusion layers), thereby "substantially" increasing the "effective isolation dimension." Ex. 1004, 2:1-27; Kiaei, ¶112. Because "the area required for the device isolation structure is only

that area required for the width of the trench cavity," Wada explains that "a higher degree of integration density can be achieved in a given area of a substrate." Ex. 1004, 2:28-35; Kiaei, ¶112. As a result, Wada's invention enables "the high degree of integration density required for modern semiconductor devices" and provides a simplified method of fabricating isolation structures. Ex. 1004, 3:22-32; Kiaei, ¶112.

Wada's Figs. 2A-2G and 6A-6G illustrate the successive steps of making the contemplated semiconductor device. Kiaei, ¶113. As relevant here, Fig. 2A, reproduced below, shows the cavities for trenches 12 that are fabricated on silicon substrate 7. Ex. 1004, 4:42-49; Kiaei, ¶113. Specifically, the cavities are formed by "etching through an etching mask of a SiO_2 film 22, for protecting those active regions 8 for fabricating the N-channel MOS transistor but exposing those regions for forming the trenches 12." Ex. 1004, 4:42-49; Kiaei, ¶113. And Wada further explains: "The process of forming the trenches 12 used in this embodiment is a dry etching process using gaseous chlorine to make a cavity measuring 0.5~1.5 μm [5000 to 15000 Å] in depth and 0.2~0.5 μm [2000 to 5000 Å] in width." Ex. 1004, 4:49-52; Kiaei, ¶113.



Wada's Fig. 6A shows a similar structure in connection with another embodiment:



See Ex. 1004, 9:59 – 10:9; Kiaei, ¶114.

Finally, Wada notes with respect to the trench dimensions that:

The dimensions quoted in the embodiments are meant to be examples, and they are not limited to the exact dimensions quoted.

For example, it is permissible to have a range of dimensions such as: the trench widths may range from 80 nm~several mm; the depth of

the trench may be made deeper by up to 10 μm than the depth of the diffusion layers for source and drain . . .

Ex. 1004, 7:54-62 and 13:64 – 14:6; Kiaei, ¶115.

5.5.3.2. Claims 5 and 27

(i) **[5] "The transistor of claim 1, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å" and [27] "The transistor of claim 23 . . ."**

Claims 5 and 27, which respectively depend from claims 1 and 23, are identical. As discussed in Sections 5.5.1.1 and 5.5.2.2, *supra*, Yun discloses claims 1 and 23.

Wada discloses forming trenches 12 having a width ranging from 2000 to 5000 Å and a depth ranging from 5000 to 15000 Å. Ex. 1004, 4:41-51; Kiaei, ¶118. Further, Wada notes that "[t]he dimensions quoted in the embodiments are meant to be examples, and they are not limited to the exact dimensions quoted." Ex. 1004, 7:54-62 and 13:64 – 14:6; Kiaei, ¶118. A POSITA reading Wada would appreciate, for example, that trenches 12 could be formed to a depth that is less than 5000 Å. Kiaei, ¶118.

Thus, Wada discloses claim 5. Kiaei, ¶119.

5.5.3.3. It Would Have Been Obvious to Combine the Teachings of Yun and Wada

As of the '122 patent's filing date, a POSITA would have found it obvious to form the depth and width of Yun's recessed isolation structures to the thickness ranges as taught by Wada, to arrive, with a reasonable expectation of success, at the subject matter of claims 5 and 27. Kiaei, ¶¶120-121.

As an initial matter, both Yun and Wada are directed to improvements to techniques for isolating transistors on the same substrate. Kiaei, ¶122. It was well recognized in the art that isolating transistors on the same substrate from one another, particularly as transistors continued to shrink in size, was critical to transistor and overall device operation. Kiaei, ¶122 (discussing same and citing technical literature on this topic). Further, it was desirable to attain a higher degree of integration, smaller transistor sizes, and minimize overall integrated circuit area, in order to, for example, reduce cost and complexity when manufacturing semiconductor devices at large scale. Kiaei, ¶122 (discussing same and citing Wada, Tao and Rubin).

Wada, for example, improves upon prior art isolation structures in order to enable "a higher degree of integration of circuits in the semiconductor device." Ex. 1004, 1:63-67; Kiaei, ¶123. It achieves this by providing a trench having sufficient depth, reducing the surface area for the isolation structure relative to prior art structures, and simplifying the processing required to form the isolation

structure. Ex. 1004, 5:63 – 6:33; Kiaei, ¶123. Thus, a POSITA reading Yun would have been motivated to combine the teachings of Wada and Yun to achieve a greater degree of isolation, thereby avoiding any adverse effects on transistor performance caused by insufficient isolation and current leakage, while also increasing drive current without increasing the integrated circuit area. Kiaei, ¶123.

Further, Wada describes forming the trench to a depth of approximately 5000 to 15000 Å and a width of approximately 2000 to 5000 Å. Ex. 1004, 4:41-51; Kiaei, ¶124. A POSITA reading Yun would be able to select appropriate parameters for the trench (such as the depth and width) based on the device design and any relevant constraints. Kiaei, ¶124. Yun teaches, for example, "adjusting the depth" of the oxide film inside the trench: oxide film 21a "is etched by 10nm [100 Å] – 200nm [2000 Å] by means of a wet etching process." Ex. 1003, 2-5; Kiaei, ¶124. Thus, a POSITA would have been motivated to form Yun's recessed isolation structures to the thickness ranges as taught by Wada to improve transistor isolation, better protect against potential leakage issues, and increase overall device functioning. Kiaei, ¶124.

Wada and Yun also share a common aim of simplifying transistor design and manufacturing process without increasing the integrated circuit area. Kiaei, ¶125. For example, Wada explains that its improved isolation structure "not only achieves a ***higher density of integration of active devices in a given space of the***

substrate but also ***simplifies the design of interconnection lines***, thereby suggesting a path to production of very large integrated circuits economically in the future." Ex. 1004, Abstract; Kiaei, ¶125. And Yun states: "It is yet another object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can increase the channel width and, at the same time, ***decrease the number of processes while forming an isolation region***." Ex. 1003, 2-5; Kiaei, ¶125.

A POSITA would also have every reason to believe that applying Wada's teachings to the semiconductor device of Yun would succeed. Kiaei, ¶126. Both are in the same field of semiconductor processing and fabrication. *Id.* This similarity in subject matter would not only motivate a POSITA to combine the teachings of Yun and Wada, but would also lead a POSITA to believe that forming a trench isolation structure based on the width and depth ranges as taught by Wada could be successfully applied to Yun's semiconductor device. *Id.*

5.5.4 Ground #4: Claims 6-10, 13-14, 17-22 and 28-32 Are Obvious Over Yun and Lu

5.5.4.1. Lu

Lu relates to semiconductor "fabrication processes that will enhance performance," particularly in the context of dynamic random access memory ("**DRAM**") applications. Ex. 1005 (Lu), 1:6-10; Kiaei, ¶127. To improve transistor performance and reliability, Lu discloses, among other things, forming

transistors having either a "thinner" or "thicker" gate insulation layer. Ex. 1005, 2:33-41. Specifically, Lu discloses forming: (i) a "thinner gate oxide in circuits having a lower voltage" to improve performance, and (ii) a "thicker gate oxide" in circuits subject to a higher voltage to improve reliability. Ex. 1005, 2:33-41; *see also id.* at 3:1-26 (discussing various circuit elements and identifying whether they should be formed using "thinner" or "thicker" gate oxides); Kiaei, ¶127.

Fig. 4f, annotated below, shows the elements of a transistor formed in accordance with Lu's invention. Kiaei, ¶128. The transistor includes polysilicon gate 120 (Ex. 1005, 7:8-13), "thinner" gate oxide 90 and "thicker" gate oxide 110 (7:2-7), and source/drain extension implant regions 140/160 within the source/drain regions 150/170 (7:14-21). Kiaei, ¶128. Further, trench 40 isolates transistors on the substrate. Ex. 1005, 6:54-63; Kiaei, ¶128.

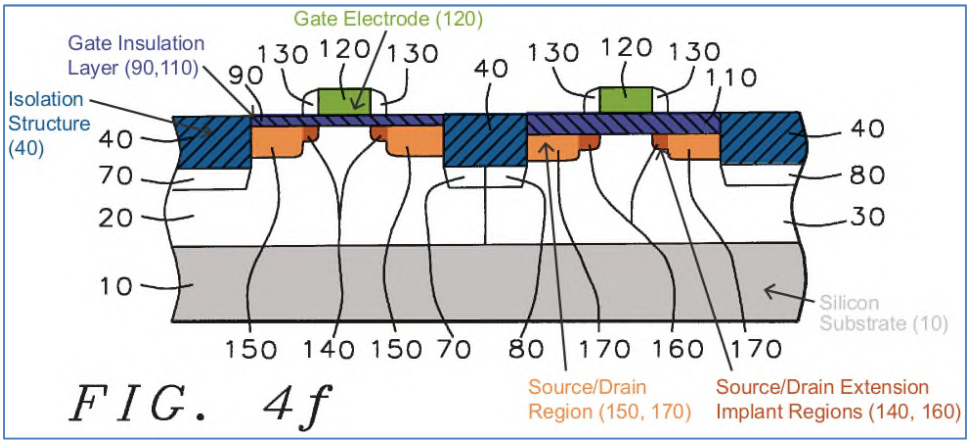


FIG. 4f

Lu discloses that the "thinner" gate oxide 90 has a thickness of 30 to 60 Å, the "thicker" gate oxide 110 has a thickness of 50 to 80 Å, and the polysilicon gate electrode 120 has a thickness of 0.1 to 0.4 μm, which is equivalent to 1000 to 4000

Å. Ex. 1005, 7:2-13; Kiaei, ¶129. With respect to the gate oxide thickness, Lu further explains that:

> The ***thinner gate oxide will provide approximately a 20% improvement in performance parameters*** such as delay over the equivalent circuits fabricated using the thicker gate oxide. ***Placing the thicker gate oxide selectively*** in areas of the DRAM having higher voltages present on the MOS transistors ***will insure [sic] that the MOS transistors meet their reliability requirements***.

Ex. 1005, 7:59-65; Kiaei, ¶129.

5.5.4.2. Claims 13, 14, 21 and 22

Independent claim 13 differs from independent claim 1 in two respects only: (1) claim 13 recites a semiconducting substrate "comprised of silicon," and (2) claim 13 recites a gate electrode "comprised of polysilicon." Kiaei, ¶130. Dependent claims 14, 21 and 22 are identical to dependent claims 3, 11 and 12. As discussed in Sections 5.5.1 and 5.5.2, *supra*, Yun discloses claims 1, 3, 11 and 12.

Yun further discloses a silicon substrate, as required by claim 13. Kiaei, ¶132.

Further, a POSITA would have found it obvious to form Yun's gate electrode from polysilicon, as required by claim 13. Kiaei, ¶133. It has long been common practice in the art to form a gate electrode using layers of polysilicon,

including during the time of Yun and the '122 patent. Kiaei, ¶133 (discussing same and citing technical literature on this topic). Indeed, the '122 patent, in describing prior art transistors, notes that "the gate electrode [] may be comprised of polysilicon." Ex. 1001, 1:50-52; Kiaei, ¶133.

To the extent Patent Owner argues a POSITA would not have found it obvious to form the gate electrode from polysilicon, Lu discloses a polysilicon gate, as discussed in detail in the following Section 5.5.4.3, *infra*.

5.5.4.3. Claims 6 and 28

(i) **[6] "The transistor of claim 1, wherein said gate electrode is comprised of polysilicon" and [28] "The transistor of claim 23 . . ."**

Claims 6 and 28, which respectively depend from claims 1 and 23, are identical. As discussed in Sections 5.5.2 and 5.5.3, *supra*, Yun discloses claims 1 and 23.

Lu discloses forming a polysilicon gate electrode. Kiaei, ¶138. "After the dual gate oxide 90 and 110 is grown, ***the polysilicon gate layer is deposited and gate 120 is formed*** for both NMOS and PMOS by the photolithographic process, as shown in FIG. 4e." Ex. 1005, 7:8-12. Thus, Lu discloses this claim limitation. Kiaei, ¶138.

5.5.4.4. Claims 7, 17 and 29

(i) **[7] "The transistor of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride"; [17] "The transistor of claim 13 . . ."; and [29] "The transistor of claim 23 . . ."**

Claims 7, 17 and 29, which respectively depend from claims 1, 13 and 23, are identical. As discussed in Sections 5.5.1.1, 5.5.2.2 and 5.5.4.2, *supra*, Yun discloses claims 1 and 23, and the combination of Yun and Lu discloses claim 13.

Yun discloses a gate insulation layer formed of an oxide film (see gate oxide 41). Kiaei, ¶141. As discussed in Section 5.5.2.1, *supra,* an oxide film, in the field of semiconductor fabrication, includes the class of silicon dioxide (SiO_2) insulators, one of the most common insulators used in the art. *Id.* Further, a POSITA, reading Yun, would understand Yun's oxide film as being silicon dioxide when considering that Yun uses a ***silicon*** substrate. *Id.*

Further, Lu discloses forming the gate insulation layer from at least one of silicon dioxide and silicon oxynitride. "The gate oxide is formed of silicon oxide, silicon nitride, or silicon oxynitride . . . ." Ex. 1005, 3:39-41; Kiaei, ¶142. Thus, Lu discloses this claim limitation. Kiaei, ¶142.

5.5.4.5. Claims 8, 18 and 30

(i) **[8] "The transistor of claim 1, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å"; [18] "The transistor of claim 13 . . ."; and [30] "The transistor of claim 23 . . ."**

Claims 8, 18 and 30, which respectively depend from claims 1, 13 and 23, are identical. As discussed in Sections 5.5.1.1, 5.5.2.2 and 5.5.4.2, *supra*, Yun discloses claims 1 and 23, and the combination of Yun and Lu discloses claim 13.

Lu discloses that "[t]he thickness of polysilicon gate 120 is from 0.1 [1000 Å] to 0.4 μm [4000 Å] and its deposition temperature is from 550° C. to 750° C." Ex. 1005, 7:11-13; Kiaei, ¶145. Thus, Lu's gate electrode has a thickness that falls within the claimed range. Kiaei, ¶145.

5.5.4.6. Claims 9, 19 and 31

(i) **[9] "The transistor of claim 1, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å."; [19] "The transistor of claim 13 . . ."; and [31] "The transistor of claim 23 . . ."**

Claims 9, 19 and 31, which respectively depend from claims 1, 13 and 23, are identical. As discussed in Sections 5.5.1.1, 5.5.2.2 and 5.5.4.2, *supra*, Yun discloses claims 1 and 23, and the combination of Yun and Lu discloses claim 13.

Lu discloses forming "thinner" and "thicker" gate oxides. Kiaei, ¶148. "***The thickness of thinner gate oxide is from 30 to 60 Ångstroms (preferably 45 Ångstroms)*** and is grown temperature is from 750 to 1000° C." Ex. 1005, 7:2-6.

Thus, Lu's gate insulation layer has a thickness that falls within the claimed range. Kiaei, ¶148.

5.5.4.7. Claims 10, 20 and 32

(i) **[10] "The transistor of claim 1, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region" and [32] "The transistor of claim 23 . . ."**

Claims 10, 20 and 32, which respectively depend from claims 1, 13 and 23, are identical. As discussed in Sections 5.5.1.1, 5.5.2.2 and 5.5.4.2, *supra*, Yun discloses claims 1 and 23, and the combination of Yun and Lu discloses claim 13.

Lu discloses forming source/drain extension regions 140 and 160, and source/drain regions 150 and 170, as shown in annotated Fig. 4f below. Ex. 1005, 7:14-21; Kiaei, ¶151. Like the '122 patent, Lu teaches implanting boron into the source/drain regions of PMOS transistors, and arsenic into the source/drain regions of NMOS transistors. Kiaei, ¶151; *compare* Ex. 1005, 7:22-36 with Ex. 1001, 6:1-6. Further, the structure of Lu's source/drain extension regions 140 and 160, and source/drain regions 150 and 170 mirrors the structure disclosed in the '122 patent, as illustrated below:

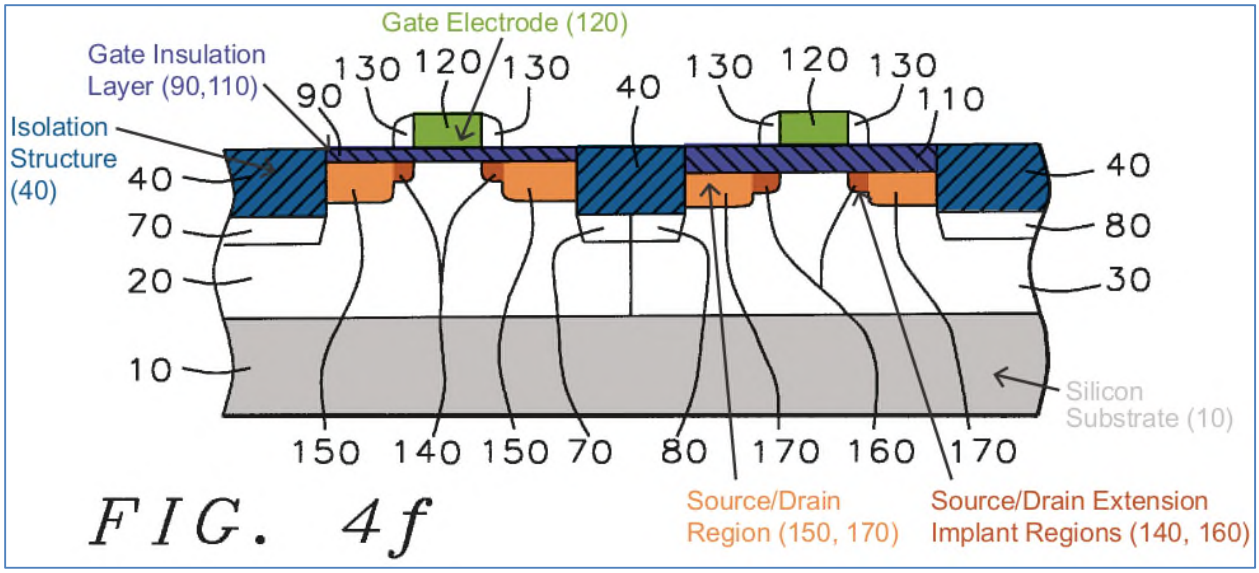


FIG. 4f

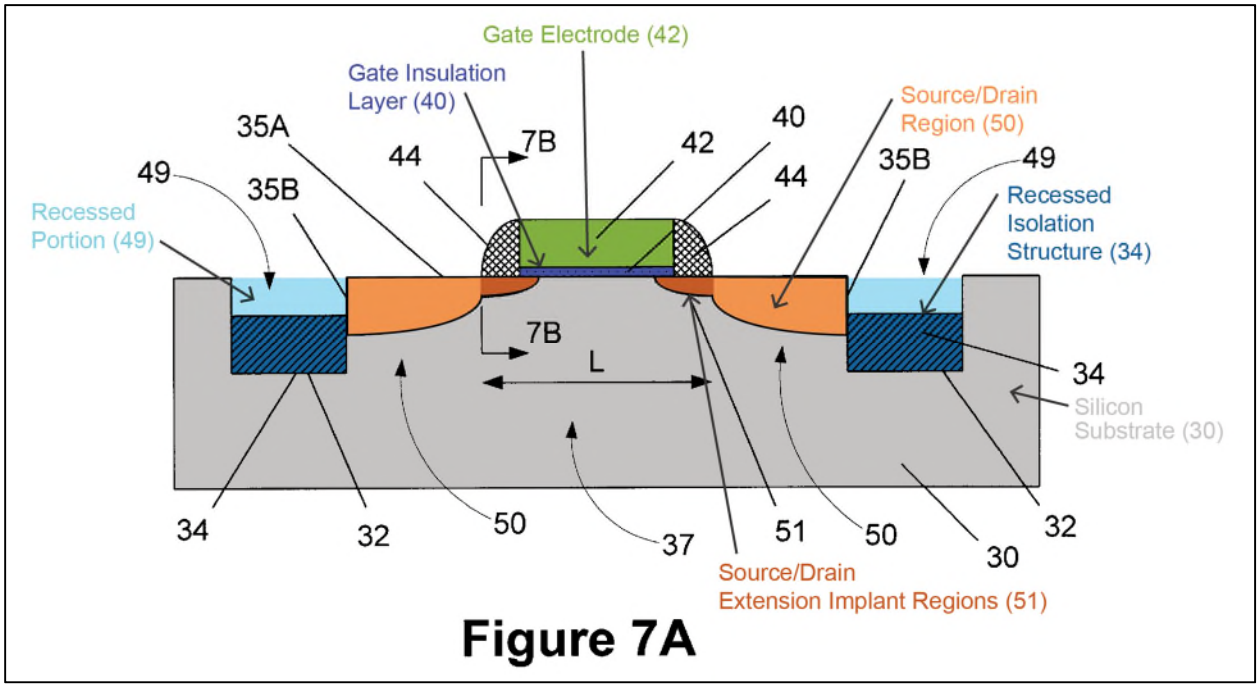


Figure 7A

Kiaei, ¶151. Thus, Lu discloses the subject matter of this claim limitation. *Id.*

5.5.4.8. It Would Have Been Obvious to Combine the Teachings of Yun and Lu

As of the '122 patent's filing date, a POSITA would have found it obvious to combine the teachings of Yun and Lu to arrive, with a reasonable expectation of

success, at the subject matter of claims 6-10, 13-14, 17-22 and 28-32, for the reasons discussed below. Kiaei, ¶¶152-53. Specifically, a POSITA would have been motivated to: (i) form Yun's *gate electrode* from polysilicon (claims 6, 13, 14, 21, 22 and 28) and to the thickness taught in Lu (claims 8, 18 and 30); (ii) form Yun's *gate insulation layer* from silicon dioxide or silicon oxynitride (claims 7, 17 and 29) and to the thickness taught in Lu (claims 9, 19 and 31); and (iii) form, in Yun's transistor, *source/drain extension implant regions* as taught in Lu (claims 10, 20 and 32). Kiaei, ¶¶152-53.

As an initial matter, Yun and Lu are directed to improving upon prior art processes related to semiconductor fabrication and enhancing transistor performance. Kiaei, ¶154. For example, Yun teaches methods for increasing transistor drive current without increasing integrated circuit area, by extending the gate electrode and gate insulation layer into the recessed portion of an isolation structure. *Id.* Similarly, Lu focuses on improving MOS transistor performance in connection with DRAM (memory) applications; Lu specifically describes forming "thinner" or "thicker" gate insulation layers depending on the voltage requirements of the associated DRAM circuitry. *Id.*

The continued trend of shrinking transistor size and thinner transistor elements (e.g., gate electrode and gate oxide) was generally recognized well before the '122 patent's filing date. Kiaei, ¶155 (discussing same and citing Tao). This

trend, however, presented new technical challenges. Kiaei, ¶155 (discussing same and citing Tao). For example, by the time of the '122 patent's filing in 2001, transistor gate length had decreased to less than 100 nm, while off-state leakage current had become increasingly problematic. Kiaei, ¶155 (discussing same and citing technical literature on this topic). Specifically, the thinner gate electrode and gate oxide layers resulted in greater current leakage, made transistor fabrication more difficult, and caused reliability issues with process control. *Id.*

A POSITA reading Yun would have understood Yun's desire to improve semiconductor fabrication techniques to account for devices with smaller feature sizes. Kiaei, ¶156. For example, Yun notes:

> It is the object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can ***improve the electric current driving capability of a transistor by increasing the channel width without increasing the chip area by vertically forming a part of the channel region***.

Ex. 1003, 2-5. With respect to the gate electrode and gate oxide, a POSITA would have appreciated the importance of fabricating devices in a way that achieves reliable and improved transistor performance. Kiaei, ¶157. For example, Lu notes:

> An object of this invention is to provide a DRAM device having ***improved performance of peripheral circuitry by having MOS transistors with a thinner gate oxide in circuits having a lower voltage***. Another object of this invention is to provide a DRAM device having ***improved reliability by having the memory cells and selected peripheral subcircuitry subjected to a higher voltage having thicker gate oxide***.

Ex. 1005, 2:34-41 (*see also id.* at 4:47-52). Thus, a POSITA would have been motivated to apply Lu's process to Yun's "conventional" process of forming the gate electrode and gate oxide to achieve improved transistor performance and reliability. Kiaei, ¶157.

A POSITA further would have recognized that Lu's technique of using lightly-doped drains ("**LDD**")—which addresses the well-known "hot-carrier effect"[6] among other things—would have increased the performance of the transistor taught by Yun. Kiaei, ¶158 (discussing same and citing technical literature on this topic). To reduce the "hot-carrier effect," each source and each

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[6] The "hot-carrier effect" is a phenomenon in which carriers (electrons and holes) are injected inadvertently into certain areas of the device (e.g., the gate oxide), resulting in device degradation and decreased transistor performance. Kiaei, ¶158.

drain can include a lightly-doped extension (LDD region) that separates a respective heavily doped "deep" source/drain region from the channel; the channel then separates the source extension from the drain extension. Kiaei, ¶158 (discussing same). In particular, a POSITA would have been motivated to use Lu's LDD technique to form source/drain extension implant regions within Yun's source/drain regions, because doing so would: (1) separate the heavily-doped source/drain regions from the conducting channel, (2) thereby diminishing the hot-carrier effect, and (3) as a result, minimize off-state current leakage. Kiaei, ¶159. Put another way, forming source/drain extension implant regions would extend the transistor active area and width (***W***) and thereby increase the drive current,[7] an express aim of Yun. Ex. 1003, 2-5 ("It is the object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can improve the electric current driving capability of a transistor by increasing the channel width without increasing the chip area . . ."); Kiaei, ¶159.

A POSITA would also have every reason to believe that applying Lu's teachings to the semiconductor device of Yun would succeed. Kiaei, ¶160. Both are in the same field of semiconductor processing and fabrication. *Id.* And both

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[7] As discussed above, the drive current can be increased by increasing the width (***W***).

are directed to improving semiconductor fabrication methods to realize increased transistor performance. *Id.* These similarities in subject matter would not only motivate a POSITA to combine the teachings of Yun and Lu, but also would lead a POSITA to believe that forming the gate electrode, gate insulation layer, and source/drain extension implant regions in the manner taught by Lu could be successfully applied to Yun. *Id.*

5.5.5 Ground #5: Claim 16 Is Obvious Over Yun in view of Wada and Lu

5.5.5.1. Claim 16

(i) **[16] "The transistor of claim 13, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å."**

Claim 16 depends from independent claim 13 and is identical to dependent claims 5 and 27 (which depend from independent claims 1 and 23, respectively). Yun discloses claims 1 and 23 for the reasons provided in Section 5.5.1.1 and 5.5.2.2, *supra*. And as discussed in Section 5.5.3, *supra*, the combination of Yun and Wada discloses claims 5 and 27.

Claim 1 and claim 13, as discussed above, differ in two minor respects only: (1) claim 13 requires a *silicon* substrate (which Yun discloses), and (2) claim 13 requires a *polysilicon* gate electrode (which Lu discloses). Kiaei, ¶161. For the

reasons provided in Section 5.5.4.2, *supra*, the combination of Yun and Lu discloses claim 13.

Further, a POSITA would have found it obvious to combine the teachings of Yun, Wada and Lu for the reasons provided above in Sections 5.5.3.3 and 5.5.4.8. Kiaei, ¶163. Specifically, Yun, Wada and Lu are in the same field of semiconductor processing and fabrication; each focuses on improving prior art fabrication methods that result in increased transistor performance. *Id.* When considering the overlap and similarity in subject matter between Yun, Wada and Lu, a POSITA would believe that forming the gate electrode from polysilicon (as taught by Lu) and a trench isolation structure based on the width and depth ranges as taught by Wada could be successfully applied to Yun's semiconductor device. *Id.*

Thus, Yun in view of Wada and Lu discloses claim 16. Kiaei, ¶164.

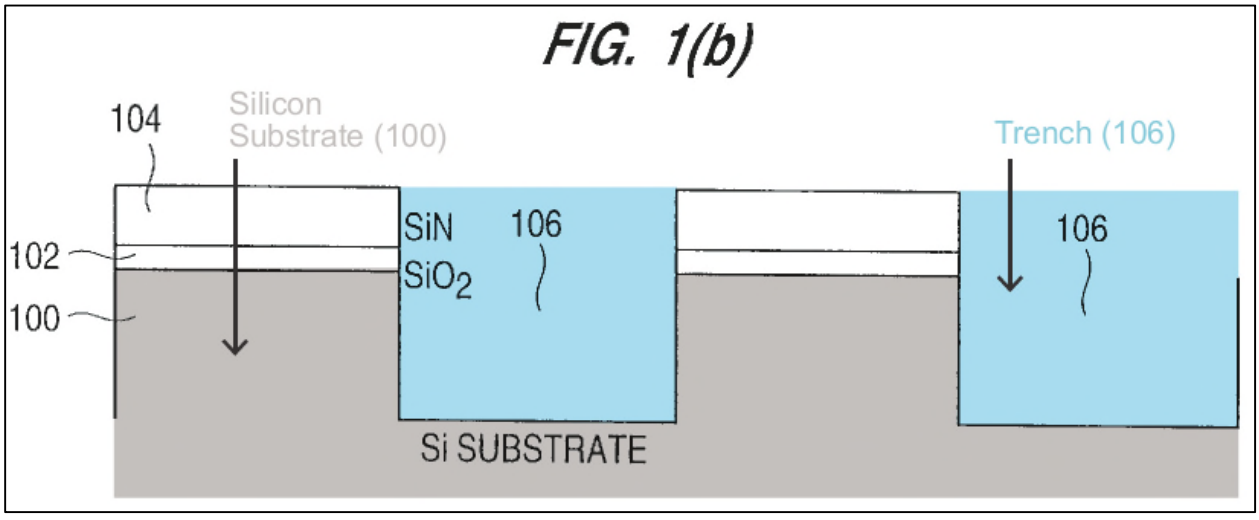
5.6. Invalidity Based on Saki

Saki relates to semiconductor devices and, like the '122 patent, is specifically directed to "an isolation structure for such devices and the methods for forming the isolation structure." Ex. 1006 (Saki), 1:8-12; Kiaei, ¶167. As Saki explains:

> An integrated circuit may be formed by connecting together various elements such as transistors which are formed on a semiconductor

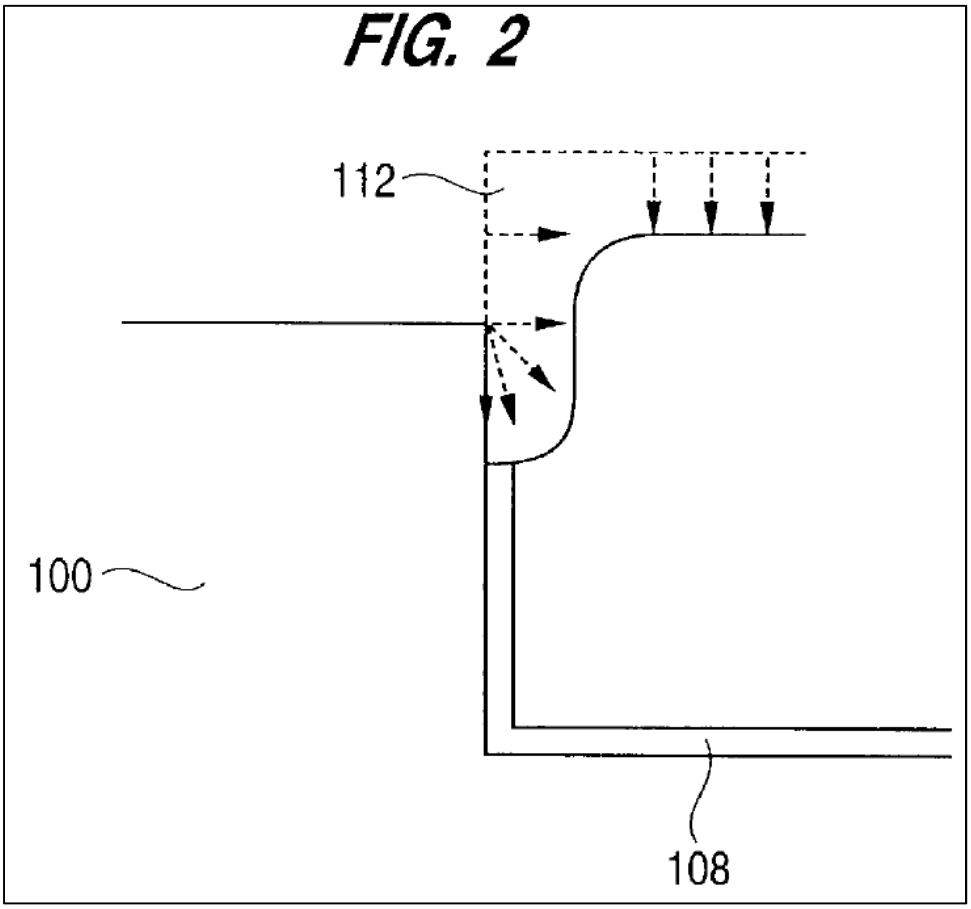
substrate. ***To ensure proper functioning of the integrated circuit, these elements must be electrically isolated from each other***. Such isolation can be achieved using local oxidation of silicon (LOCOS) or shallow trench isolation (STI). ***Shallow trench isolation is particularly advantageous for circuits having a high integration density*** since shallow trench isolation can provide for a relatively planar surface on which subsequent insulating and/or conducting layers may be formed

Ex. 1006, 1:14-24. Saki's Figs. 1(a)-1(f) illustrate a "conventional process" for forming an STI structure; Fig. 1(b), reproduced below, shows trenches 106 formed in silicon substrate 100. Kiaei, ¶168.

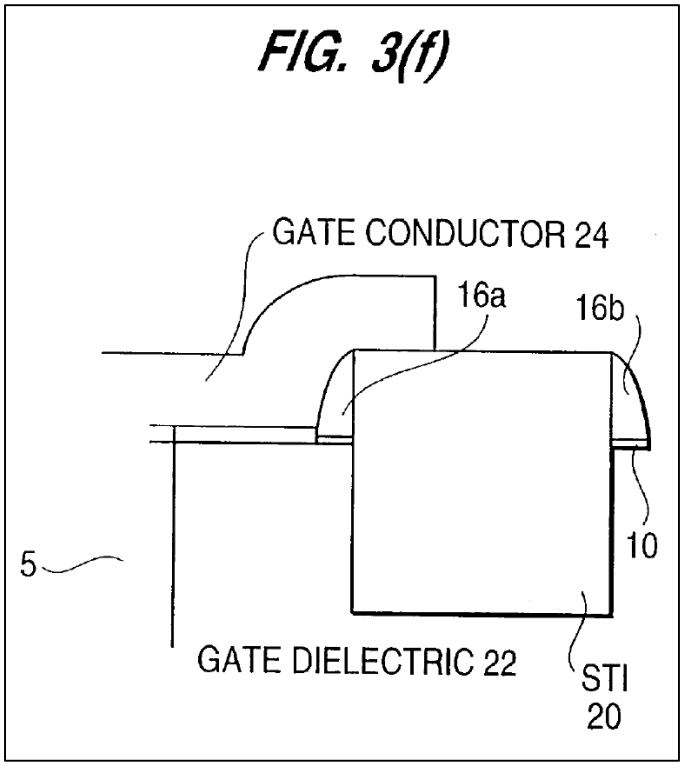


Saki observes that prior art etching processes could result in silicon dioxide being removed (etched away) from the corners of an STI structure, as illustrated in Fig. 2 below. Ex. 1006, 1:43-59; Kiaei, ¶169. This may "result in a lowering of the

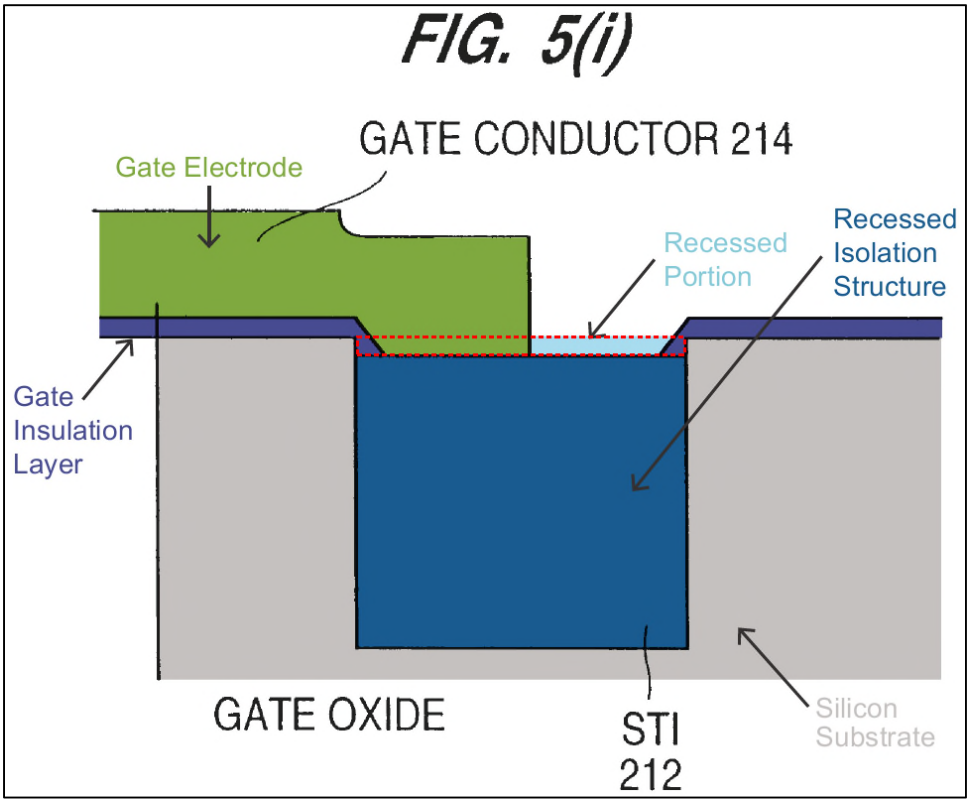
threshold voltage of a transistor formed in the active area defined by the shallow trench isolation structure," which ultimately affects transistor performance. Ex. 1006, 1:54-59; Kiaei, ¶169.



Saki also recognized that prior art processes could lead to formation of a "step" on the gate electrode caused by the difference in level between the surface of the silicon substrate and the insulator, as illustrated in Saki's Fig. 3(f), below. Ex. 1006, 2:42-47; Kiaei, ¶170. As Saki explains, "[t]his can lead to difficulties in the patterning of the gate conductor 24," especially in important applications such as DRAM. Ex. 1006, 2:47-50; Kiaei, ¶170.



Saki's invention improves upon conventional STI in several ways, including by providing "enhanced controllability of the shape of the shallow trench isolation structure." Ex. 1006, 3:14-21; Kiaei, ¶171. Saki's invention is illustrated in Figs. 5(a)-5(i). Kiaei, ¶171. Specifically, a benefit of Saki's method is suppressing "etching of the insulator at the corner of the shallow trench isolation structure." Ex. 1006, 4:61 – 5:7; Kiaei, ¶171. Further, as illustrated in Fig. 5(i) below, the gate conductor and gate insulating layer (oxide) extend into the recess formed by the trench, thereby avoiding the problems of the prior art "step." Ex. 1006, 5:18-27; Kiaei, ¶171.



5.6.1 Ground #6: Claims 1-3, 6, 11-14, 21-25, 28 and 33-34 Are Obvious Over Saki In Light of the Knowledge of a POSITA

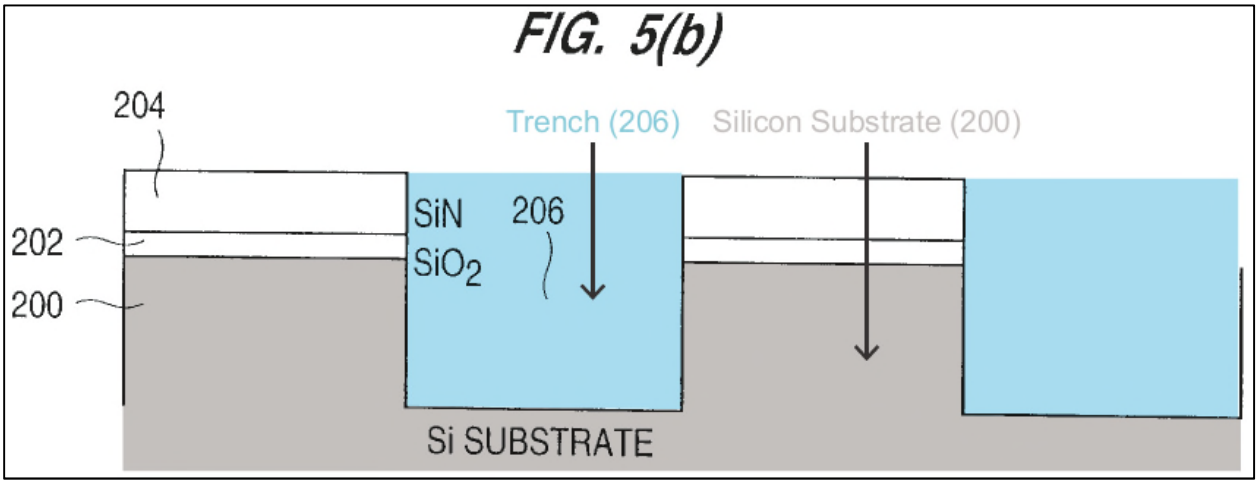
5.6.1.1. Claims 1 and 13

(i) **[1.P] and [13.P] "A transistor, comprising:"**

Saki relates to "semiconductor devices such as semiconductor memory devices," which are made up of transistors. Ex. 1006, 1:8-16; Kiaei, ¶172. Saki specifically relates to isolation structures that are formed in between transistors on a common substrate. Ex. 1006, 1:14-24; Kiaei, ¶172.

(ii) **[1.1] "a semiconducting substrate;" and [13.1] "a semiconducting substrate comprised of silicon;"**

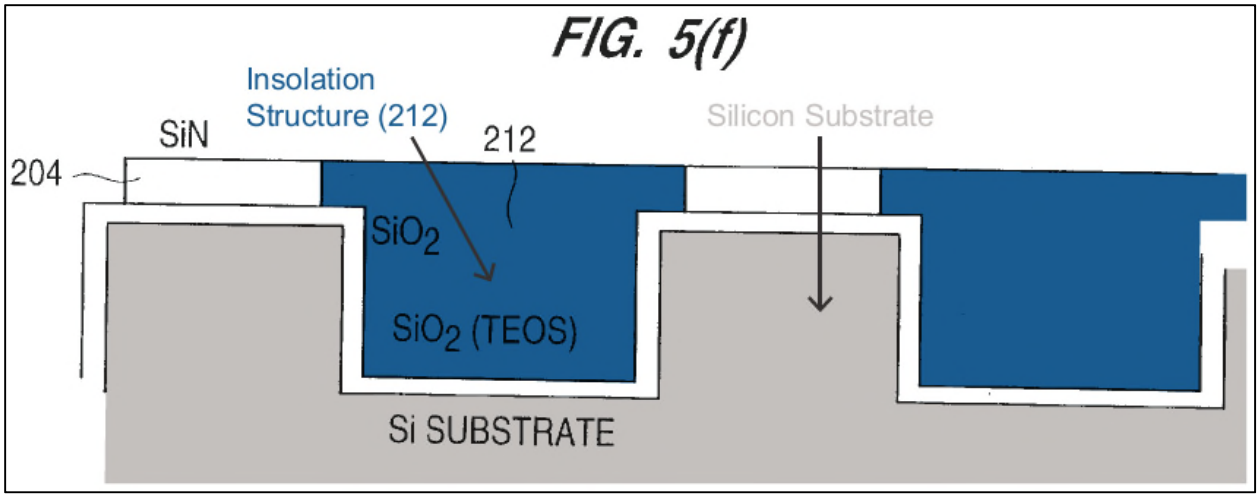
Saki discloses forming transistors, and isolation structures between them, on silicon substrate 200. Fig. 5(b); *see also* Ex. 1006, 1:13-17 and 3:65 – 4:28; Kiaei, ¶173.



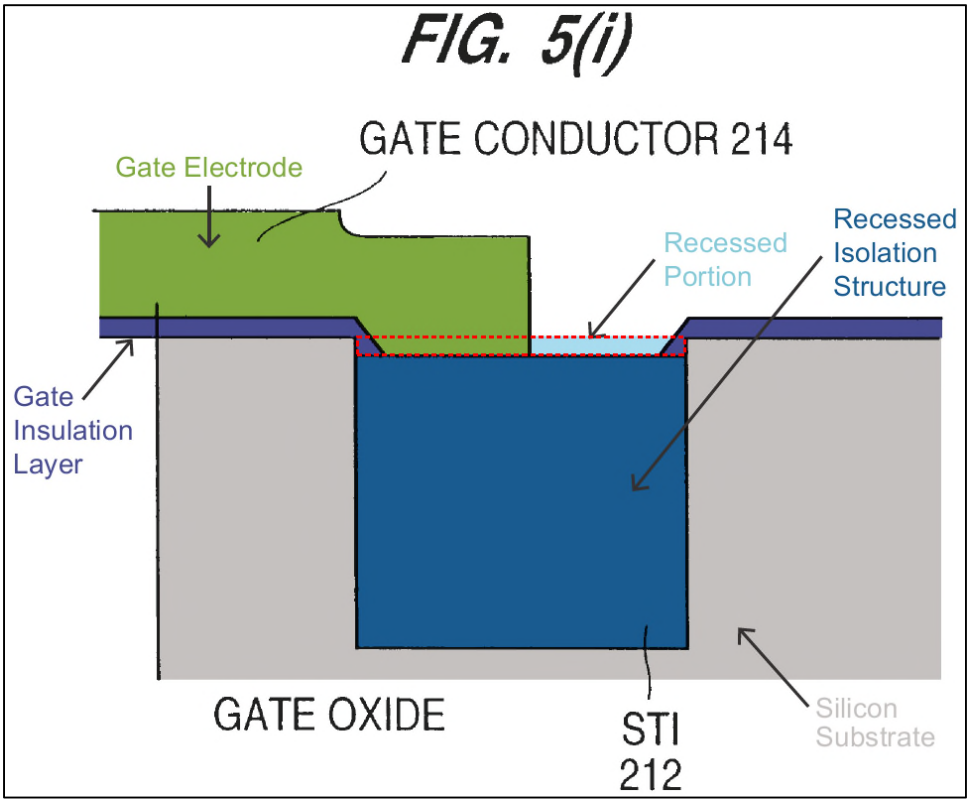
(iii) **[1.2] and [13.2] "a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove;"**

Saki discloses forming a recessed isolation structure as discussed below in connection with Figs. 5(f) through 5(i). Kiaei, ¶174.

First, a layer of silicon dioxide 212, an insulator, is deposited in the trench and planarized, as shown in Fig. 5(f). Ex. 1006, 4:51-59; Kiaei, ¶175.

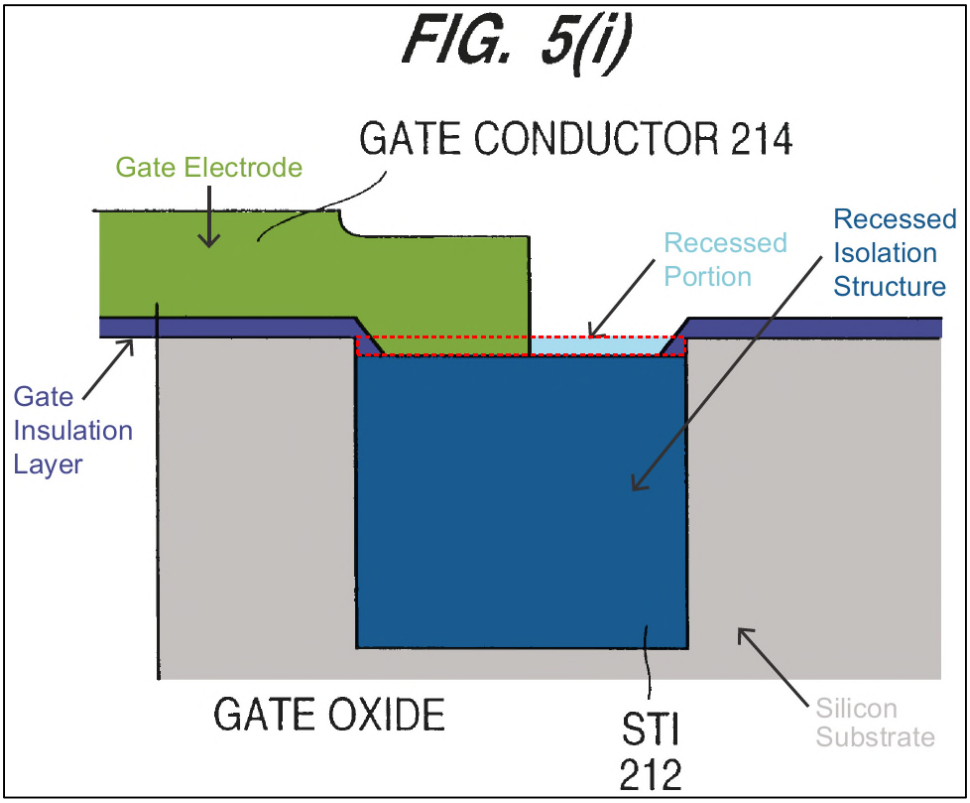


A series of etching processes are then carried out to remove portions of the pad silicon nitride 204 (*see* Fig. 5(g)), the pad silicon dioxide 202 (*see* Fig. 5(h)) and other "extensions" of the STI structure. Ex. 1006, 4:59 – 5:7; Kiaei, ¶176. The resultant transistor and isolation structure is shown in Fig. 5(i). As indicated by the red dashed lines in annotated Fig. 5(i) below, Saki's isolation structure defines a recess in the region above the silicon dioxide isolation structure. Kiaei, ¶176. Thus, Saki discloses this claim limitation. Kiaei, ¶177.



(iv) **[1.3] "a gate electrode and a gate insulation layer formed above said substrate, a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure; and" and [13.3] "a gate electrode comprised of polysilicon . . ."**

Saki discloses gate electrode 214 and a gate insulation layer formed above substrate 200. Ex. 1006, 5:22-26; Kiaei, ¶178. As can be verified visually with reference to Fig. 5(i), the end portions of gate electrode 214 and the gate insulation layer extend into the recess above the silicon dioxide isolation structure. Kiaei, ¶178.

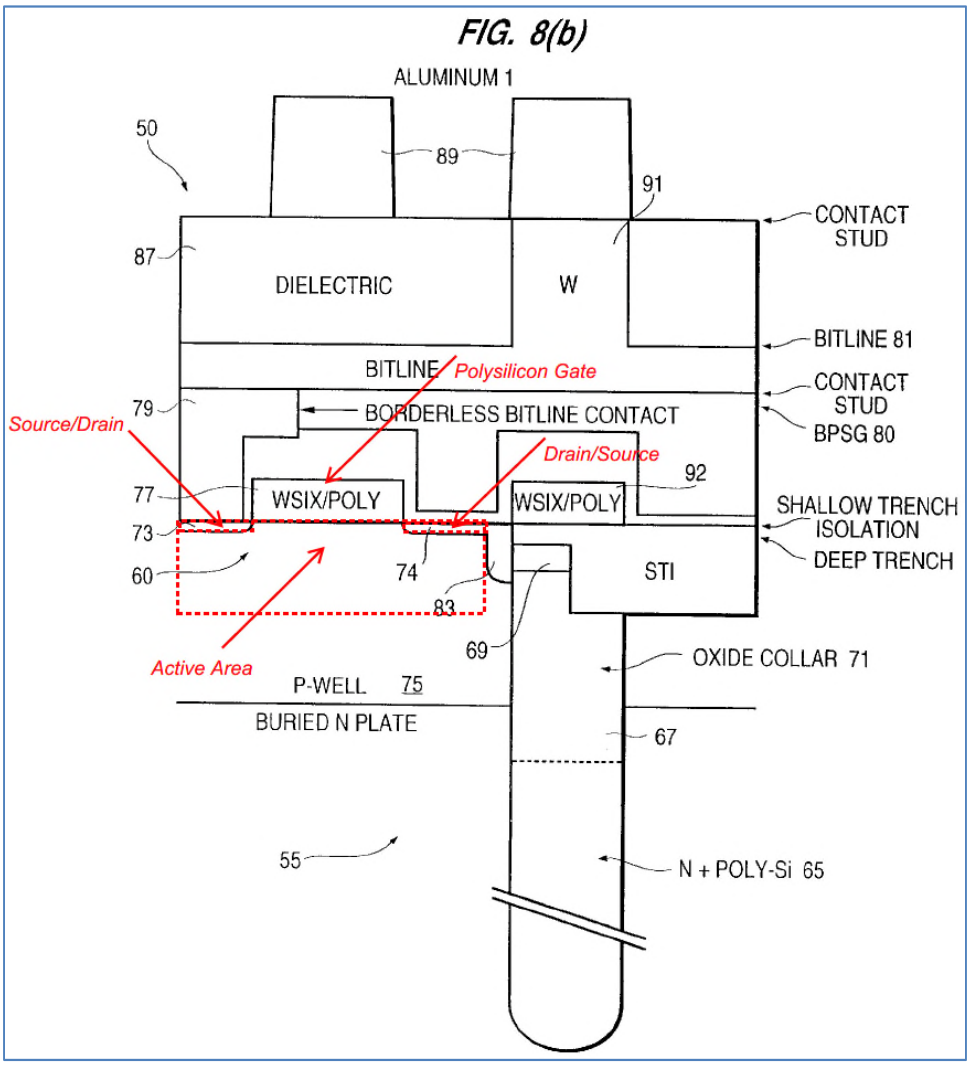


With respect to claim 13, Saki discloses forming the gate electrode from polysilicon. Kiaei, ¶179. For example, Saki discloses—in connection with "a method of manufacturing the DRAM cell 50 using the shallow isolation structure and method of the present invention"—forming conductive material (such as a gate electrode) using "N^+-type ***polycrystalline silicon***" or "undoped polycrystalline silicon." *See, e.g.*, Saki, 7:19-59; Kiaei, ¶179. Thus, Saki discloses this claim limitation. Kiaei, ¶180.

(v) **[1.4] and [13.4] "a source region and a drain region formed in said substrate."**

Saki discloses that the completed semiconductor device includes a source region and a drain region formed in the substrate. Kiaei, ¶181. For example, in

describing a "trench DRAM cell 50" using the isolation techniques of Saki's invention, Saki teaches the formation of source/drain regions 73/74 in the substrate, as indicated by the red dashed lines in Fig. 8(b), reproduced below. Ex. 1006, 6:54 – 7:17 ("Transfer gate 60 includes N-type source/drain and drain/source regions 73 and 74"); Kiaei, ¶181.



Similarly, Saki teaches the formation of source/drain regions in connection with "a method of manufacturing the DRAM cell 50 using the shallow isolation

structure and method of the present invention." Ex. 1006, 7:19-22; Kiaei, ¶182. Saki specifically describes: "Using the gate electrodes as masks, ***source/drain regions may be formed by ion implantation***." Ex. 1006, 8:55-58; Kiaei, ¶182.

5.6.1.2. Claim 23

(i) **[23.P] "A transistor, comprising:"**

See claim [1.P].

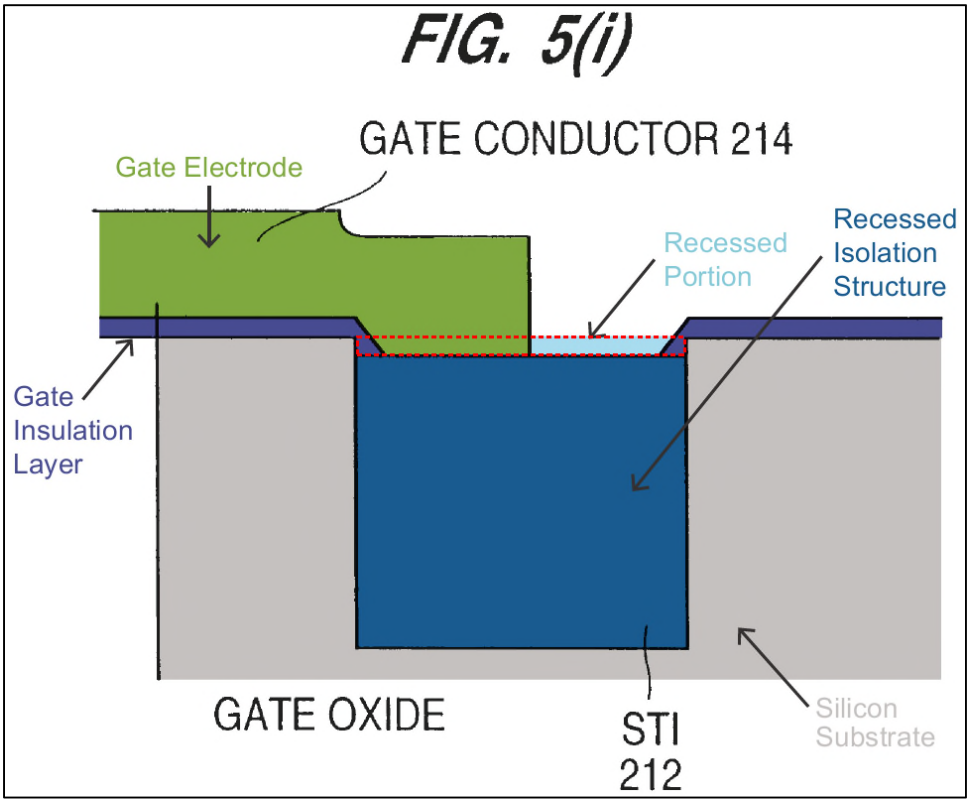
(ii) **[23.1] "a semiconducting substrate;"**

See claim [1.1].

(iii) **[23.2] "a recessed isolation structure defining an active area having an upper surface and an exposed sidewall surface;"**

For the reasons described in Section 5.6.1.1(iii), *supra*, Saki discloses this claim limitation.

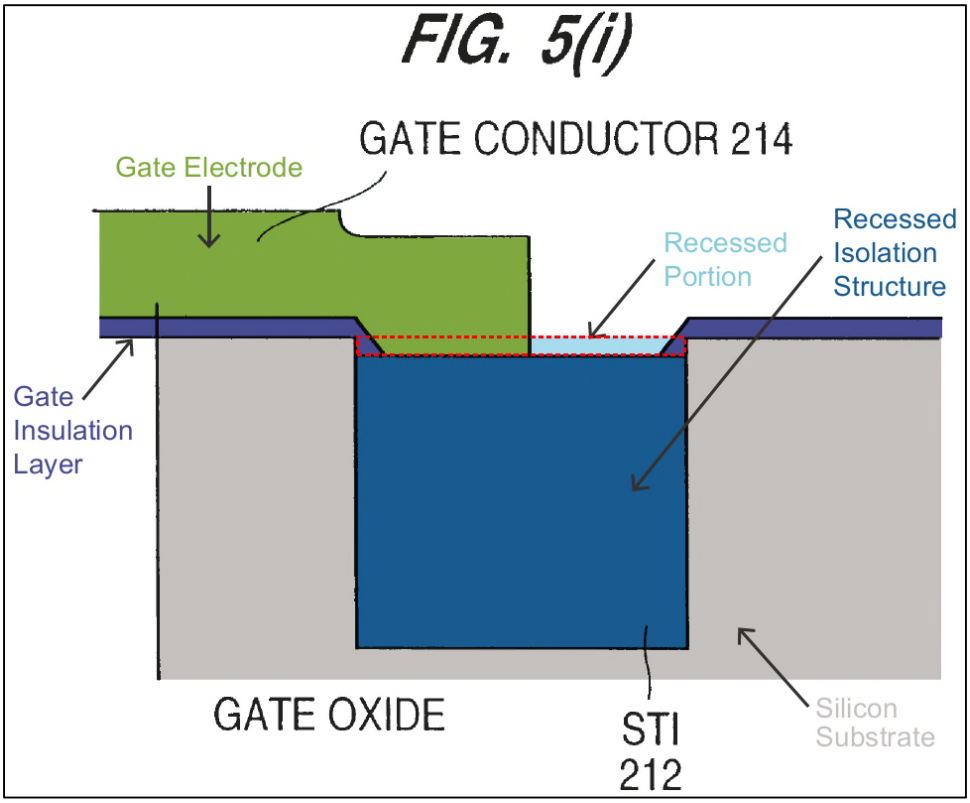
Specifically, Saki teaches forming STI structure 212, which includes a recessed portion and a portion filled with an oxide film insulator, as illustrated in annotated Fig. 5(i) below. Kiaei, ¶186. As shown by the dashed red lines in the annotated figure, the recessed portion is partially filled by the gate electrode and gate insulation layer. *Id.* Further, Saki describes the active area as being defined by the STI structure. Ex. 1006, 3:9-14 (noting "the active area defined by the shallow trench isolation structure"); Kiaei, ¶186. Thus, STI structure 212 defines an active area having an upper surface and an exposed sidewall surface, as shown in the annotated figure. Kiaei, ¶186.



(iv) **[23.3] "a gate insulation layer and a gate electrode positioned above a portion of said upper surface and a portion of said exposed sidewall surface of said active area; and"**

For the reasons described in Section 5.6.1.1(iv), *supra*, Saki discloses this claim limitation.

Specifically, as can be verified visually from Saki's Fig. 5(i) below, gate conductor 214 and the gate insulation layer (oxide) are positioned above the upper surface and exposed sidewall surface of the active area. Kiaei, ¶188.



(v) **[23.4] "a source region and a drain region formed in said active area."**

For the reasons described in Section 5.6.1.1(v), *supra*, Saki discloses this claim limitation.

As discussed previously, Saki teaches forming source/drain regions 73/74 in the substrate. Kiaei, ¶190. A POSITA, reading Saki, would recognize that source/drain regions 73/74 are formed in the "Active Area (AA)" region depicted below by the red dashed lines in Fig. 8(a) (a "top-down view of the trench DRAM cell"). Ex. 1006, 6:57-59; Kiaei, ¶190. This can be verified visually by referring to Fig. 8(b) below, which "is a cross-sectional view taken along line A-A' of FIG. 8(a)." Ex. 1006, 6:57-59; Kiaei, ¶190.

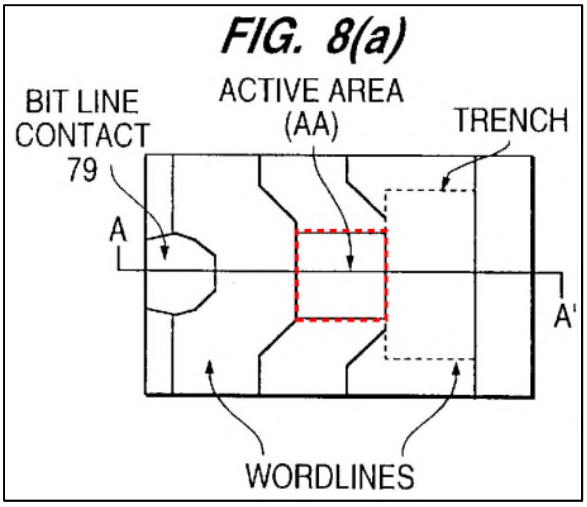


FIG. 8(a)
BIT LINE CONTACT
79
ACTIVE AREA (AA)
TRENCH
A
A'
WORDLINES

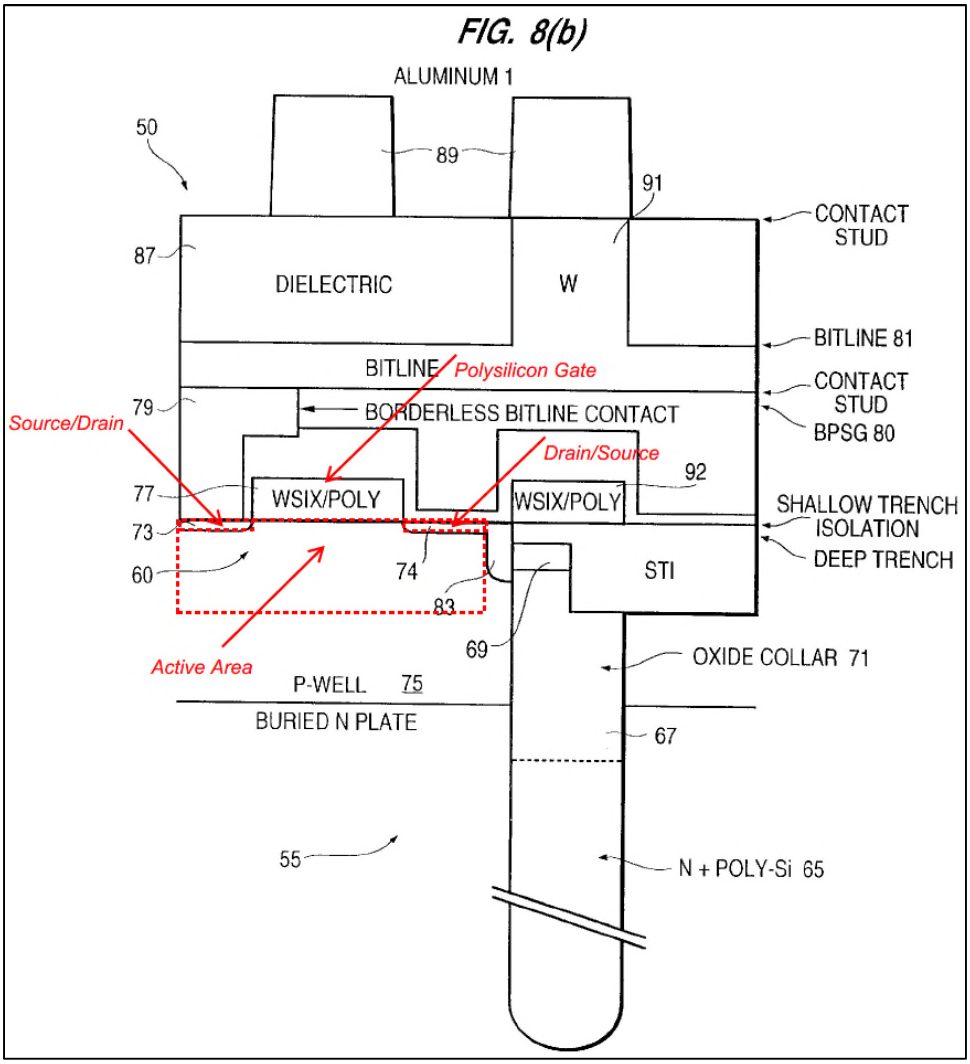


FIG. 8(b)
ALUMINUM 1
50
89
91
CONTACT STUD
87
DIELECTRIC
W
BITLINE 81
BITLINE
Polysilicon Gate
CONTACT STUD
79
BORDERLESS BITLINE CONTACT
BPSG 80
Source/Drain
Drain/Source
92
77
WSIX/POLY
WSIX/POLY
SHALLOW TRENCH ISOLATION
73
DEEP TRENCH
60
74
STI
83
69
OXIDE COLLAR 71
Active Area
P-WELL 75
BURIED N PLATE
67
55
N + POLY-Si 65

This understanding is confirmed by Saki's disclosure at 6:63-67: "Transfer gate 60 includes N-type source/drain and drain/source regions 73 and 74 formed in P-type well 75 and a WSix /polycrystaline silicon gate 77 insulatively spaced from the channel region between source/drain region 73 and drain/source region 74." Kiaei, ¶191. In other words, Saki teaches a "Transfer Gate 60" (for the DRAM cell) that includes polysilicon gate 77, with a diffusion region (under polysilicon gate 77) and source/drain regions 73/74 formed in the active area, as illustrated in annotated Fig. 8(b) above. Kiaei, ¶191.

5.6.1.3. Claims 2 and 24

(i) **[2] "The transistor of claim 1, wherein said semiconducting substrate is comprised of silicon" and [24] "The transistor of claim 23 . . ."**

Claims 2 and 24, which respectively depend from claims 1 and 23, are identical. As discussed in Sections 5.6.1.1 and 5.6.1.2, *supra*, Saki discloses claims 1 and 23.

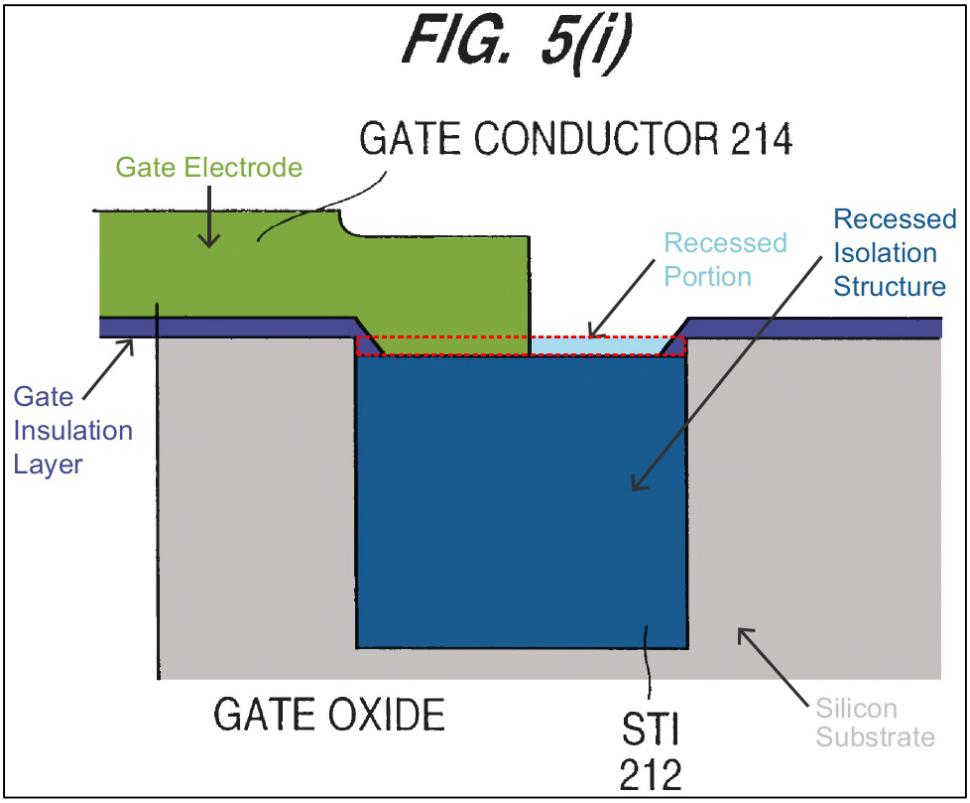
As discussed above, Saki discloses forming a transistor on silicon substrate 200. Kiaei, ¶194.

5.6.1.4. Claims 3, 14 and 25

(i) **[3] "The transistor of claim 1, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride"; [14] "The transistor of claim 13 . . ."; and [25] "The transistor of claim 23 . . ."**

Claims 3, 14 and 25, which respectively depend from claims 1, 14 and 23, are identical. As discussed in Sections 5.6.1.1 and 5.6.1.2, *supra*, Saki discloses claims 1, 13 and 23.

As discussed above, Saki discloses that silicon dioxide is deposited over the substrate, including in isolation structure 212. Ex. 1006, 4:51-59 ("A ***silicon dioxide layer*** 212 is then blanket deposited over the entire surface of the substrate . . ."). Kiaei, ¶197. The isolation structure becomes a recessed isolation structure (formed of silicon dioxide) following a series of etching processes, as discussed in detail in Section IX.B.1.c, above. *See* Fig. 5(i) below; Kiaei, ¶197.



5.6.1.5. Claims 6 and 28

(i) **[6] "The transistor of claim 1, wherein said gate electrode is comprised of polysilicon" and [28] "The transistor of claim 23 . . ."**

Claims 6 and 28, which respectively depend from claims 1 and 23, are identical. As discussed in Sections 5.6.1.1 and 5.6.1.2, *supra*, Saki discloses claims 1 and 23.

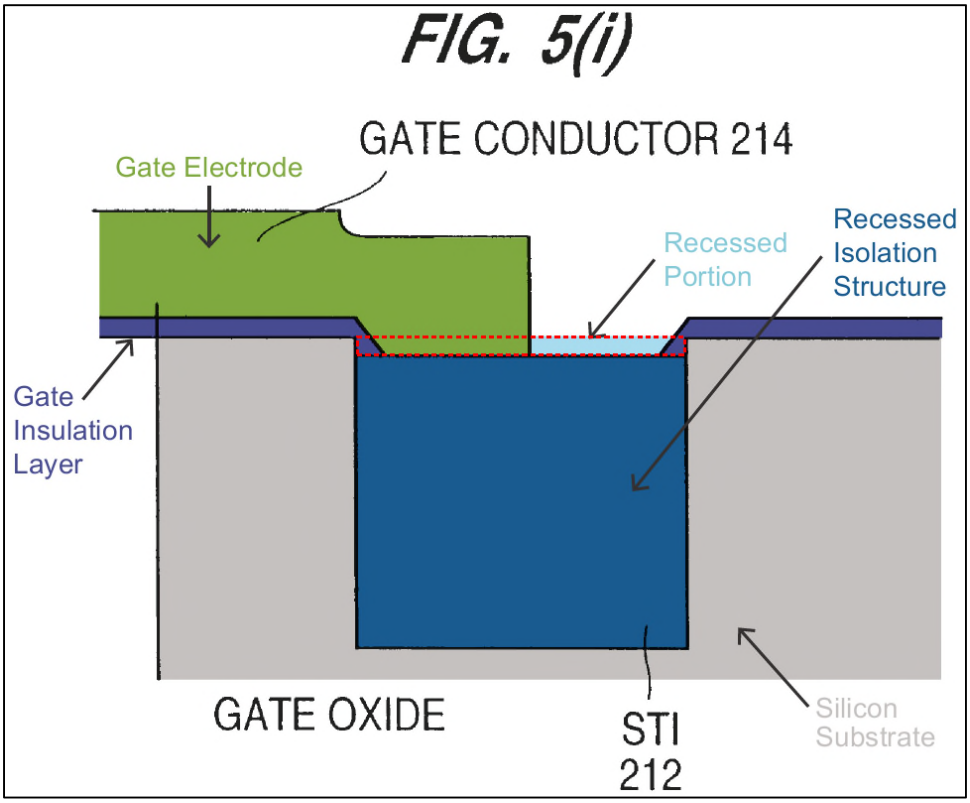
For the reasons provided in Section 5.6.1.1(iv), *supra*, Saki discloses forming a polysilicon gate. Kiaei, ¶200.

5.6.1.6. Claims 11, 21 and 33

(i) **[11] "The transistor of claim 1, wherein said gate electrode has first and second end portions that extend into said recess"; [21] "The transistor of claim 13 . . ."; and [33] "The transistor of claim 23 . . . defined by said recessed isolation structure."**

Claims 11, 21 and 33, which respectively depend from claims 1, 13 and 23, are nearly identical. As discussed in Sections 5.6.1.1 and 5.6.1.2, *supra*, Saki discloses claims 1, 13 and 23.

As discussed above in Section 5.6.1.1(iv), Saki discloses that gate conductor 214 extends into the recess above the oxide film inside the trench. Kiaei, ¶203. More specifically, first and second end portions of gate conductor 214 extend into the recess. *Id.* The annotated figure below depicts a first end portion of gate conductor 214 extending into the trench formed to the right; a second end portion extends into the trench formed to the left (not shown). *Id.*

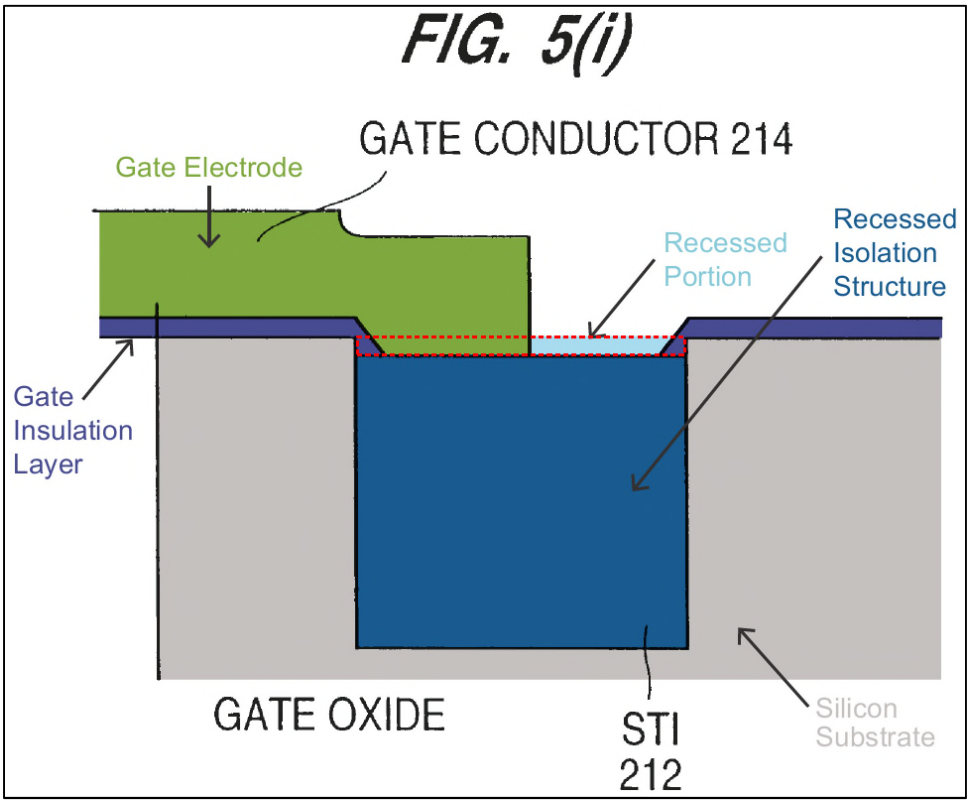


5.6.1.7. Claims 12, 22 and 34

(i) **[12] "The transistor of claim 11, wherein said first and second end portions extending into said recess are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure"; [22] "The transistor claim 21 . . ."; and [34] "The transistor of claim 33 . . .**

Claims 12, 22 and 34, which respectively depend from claims 11, 21 and 33, are nearly identical. As discussed in Sections 5.6.1.6, *supra*, Saki discloses claims 11, 21 and 33.

Further, as can be verified easily by reference to Saki's Fig. 5(i) below, the first and second end portions of gate conductor 214 are positioned above a portion of a sidewall of the active region:



Kiaei, ¶206.

5.6.2 Ground #7: Claims 5, 16 and 27 Are Obvious Over Saki and Wada

5.6.2.1. Claims 5, 16 and 27

(i) **[5] "The transistor of claim 1, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å"; [16] "The transistor of claim 13 . . ."; and [27] "The transistor of claim 23 . . ."**

Claims 5, 16 and 27, which respectively depend from claims 1, 13 and 23, are identical. As discussed in Sections 5.6.1.1 and 5.6.1.2, *supra*, Saki discloses claims 1, 13 and 23.

Wada discloses the subject matter of claims 5, 16 and 27. *See* Sections 5.5.3.2 and 5.5.5.1, *supra*.

5.6.2.2. It Would Have Been Obvious to Combine the Teachings of Saki and Wada

As of the '122 patent's filing date, a POSITA would have found it obvious to form the depth and width of Saki's recessed isolation structures to the thickness ranges as taught by Wada, to arrive, with a reasonable expectation of success, at the subject matter of claims 5, 16 and 27. Kiaei, ¶¶210-211.

As an initial matter, both Saki and Wada are directed to improvements to techniques for isolating transistors on the same substrate. Kiaei, ¶212. It was well recognized in the art that isolating transistors on the same substrate from one another, particularly as transistors continued to shrink in size, was critical to transistor and overall device operation, as discussed in detail in Section 5.5.3.3,

supra. Kiaei, ¶212. Thus, a POSITA reading Saki would have been motivated to combine the teachings of Wada and Saki to achieve a greater degree of isolation, thereby avoiding any adverse effects on transistor performance caused by insufficient isolation. *Id.*

Further, Saki and Wada also share a common aim of simplifying transistor design and manufacturing process. Kiaei, ¶213. As discussed in detail in Section 5.5.3.3, *supra*, Wada's invention "***simplifies the design of interconnection lines***, thereby suggesting a path to production of very large integrated circuits economically in the future." Ex. 1004, Abstract; Kiaei, ¶213. Similarly, Saki is directed to a similar aim: "Still further, the method of the present invention has a small number of steps and therefore contributes to ease of device manufacture and reduced manufacturing costs." Ex. 1006, 3:17-21; Kiaei, ¶213.

A POSITA would also have every reason to believe that applying Wada's teachings to the semiconductor device of Saki would succeed. Kiaei, ¶214. Both are in the same field of semiconductor processing and fabrication. *Id.* This similarity in subject matter would not only motivate a POSITA to combine the teachings of Saki and Wada, but would also lead a POSITA to believe that forming a trench isolation structure based on the width and depth ranges as taught by Wada could be successfully applied to Saki's semiconductor device. *Id.*

5.6.3 Ground #8: Claims 7-10, 17-20 and 29-32 Are Obvious Over Saki and Lu

5.6.3.1. Claims 7, 17 and 29

(i) **[7] "The transistor of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride"; [17] "The transistor of claim 13 . . ."; and [29] "The transistor of claim 23 . . ."**

Claims 7, 17 and 29, which respectively depend from claims 1, 13 and 23, are identical. As discussed in Sections 5.6.1.1 and 5.6.1.2, *supra*, Saki discloses claims 1, 13 and 23.

Saki discloses a gate oxide film. Ex. 1006, 1:25-29 ("***A silicon dioxide (SiO_2) layer 102*** and a silicon nitride (Si_3N_4) layer 104 ***are successively formed on the surface of a silicon substrate 100*** . . . ."); Kiaei, ¶217. Further, as discussed in Section 5.5.2.1, *supra*, an oxide film, in the field of semiconductor fabrication, includes the class of silicon dioxide (SiO_2) insulators, one of the most common insulators used in the art. Kiaei, ¶217. Further, a POSITA, reading Saki, would understand Saki's oxide film as being silicon dioxide when considering that (1) Saki uses a ***silicon*** substrate and discloses ***growing a gate oxide layer*** on the substrate (Ex. 1006, 1:47-51), and (2) Saki uses silicon dioxide throughout the process of forming the STI structure, including to form the pad silicon dioxide layer 202 and deposit silicon dioxide layer 212 into the trench 206. *See, e.g.*, Ex. 1006, 3:66 – 5:7; Kiaei, ¶217.

Further, Lu discloses the subject matter of claims 7, 17 and 29. *See* Section 5.5.4.4, *supra*.

5.6.3.2. Claims 8, 18 and 30

(i) **[8] "The transistor of claim 1, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å"; [18] "The transistor of claim 13 . . ."; and [30] "The transistor of claim 23 . . ."**

Claims 8, 18 and 30, which respectively depend from claims 1, 13 and 23, are identical. As discussed in Sections 5.6.1.1 and 5.6.1.2, *supra*, Saki discloses claims 1, 13 and 23.

Lu discloses the subject matter of claims 8, 18 and 30. *See* Section 5.5.4.5, *supra*.

5.6.3.3. Claims 9, 19 and 31

(i) **[9] "The transistor of claim 1, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å."; [19] "The transistor of claim 13 . . ."; and [31] "The transistor of claim 23 . . ."**

Claims 9, 19 and 31, which respectively depend from claims 1, 13 and 23, are identical. As discussed in Sections 5.6.1.1 and 5.6.1.2, *supra*, Saki discloses claims 1, 13 and 23.

Lu discloses the subject matter of claims 9, 19 and 31. *See* Section 5.5.4.6, *supra*.

5.6.3.4. Claims 10, 20 and 32

(i) **[10] "The transistor of claim 1, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region"; [20] "The transistor of claim 13 . . ."; and [32] "The transistor of claim 23 . . ."**

Claims 10, 20 and 32, which respectively depend from claims 1, 13 and 23, are identical. As discussed in Sections 5.6.1.1 and 5.6.1.2, *supra*, Saki discloses claims 1, 13 and 23.

Lu discloses the subject matter of claims 10, 20 and 32. *See* Section 5.5.4.7, *supra*.

5.6.3.5. It Would Have Been Obvious to Combine the Teachings of Saki and Lu

As of the '122 patent's filing date, a POSITA would have found it obvious to combine the teachings of Saki and Lu to arrive, with a reasonable expectation of success, at the subject matter of claims 7-10, 17-20 and 29-32, for the reasons discussed below. Kiaei, ¶¶228-229. Specifically, a POSITA would have been motivated to: (i) form Saki's *gate electrode* to the thickness taught in Lu (claims 8, 18 and 30); (ii) form Saki's *gate insulation layer* from silicon dioxide or silicon oxynitride (claims 7, 17 and 29) and to the thickness taught in Lu (claims 9, 19 and 31); and (iii) form, in Saki's transistor, *source/drain extension implant regions* as taught in Lu (claims 10, 20 and 32). Kiaei, ¶¶228-229.

As an initial matter, Saki and Lu are directed to improving upon prior art processes related to semiconductor fabrication and enhancing transistor performance. Kiaei, ¶230. For example, Saki teaches improved shallow trench isolation techniques that thereby improve transistor performance, particularly in the context of DRAM applications. Kiaei, ¶230. And as discussed in Section 5.5.4.8, *supra*, Lu focuses on improving MOS transistor performance in connection with DRAM applications; Lu specifically describes forming "thinner" or "thicker" gate insulation layers depending on the voltage requirements of the associated DRAM circuitry. Kiaei, ¶230.

As discussed in detail in Section 5.5.4.8, *supra*, the continued trend of shrinking transistor size and thinner transistor elements (e.g., gate electrode and gate oxide)—and the reliability issues that stemmed from this trend—was generally recognized well before the '122 patent's filing date. Kiaei, ¶231. And with respect to the gate electrode and gate oxide, a POSITA would have appreciated the importance of fabricating devices in a way that achieves reliable and improved transistor performance, for the reasons discussed in Section 5.5.4.8 (*see* Ex. 1005, 2:34-41 and 4:47-52 and discussion regarding same). Kiaei, ¶232. Thus, a POSITA would have been motivated to apply the teachings of Lu to Saki's process of forming the gate electrode and gate oxide to achieve improved transistor performance and reliability. Kiaei, ¶232.

Further, a POSITA would have recognized that addressing the "hot-carrier effect" would have increased the performance of the transistor taught by Saki. Kiaei, ¶233. In particular, a POSITA would have been motivated to use Lu's LDD technique to form source/drain extension implant regions within Saki's source/drain regions, because doing so would: (1) separate the heavily-doped source/drain regions from the conducting channel, (2) thereby diminishing the hot-carrier effect, and (3) as a result, minimize off-state current leakage. Kiaei, ¶233. Put another way, forming source/drain extension implant regions would extend the transistor active area, which in turn would reduce leakage and increase the drive current. *Id.*

A POSITA would also have every reason to believe that applying Lu's teachings to the semiconductor device of Saki would succeed. Kiaei, ¶234. Both are in the same field of semiconductor processing and fabrication; in particular, both relate to DRAM applications and the use of shallow trench isolation (STI) techniques. *Id.* And both are directed to improving semiconductor fabrication methods to realize increased transistor performance. *Id.* These similarities in subject matter would not only motivate a POSITA to combine the teachings of Saki and Lu, but also would lead a POSITA to believe that forming the gate electrode, gate insulation layer, and source/drain extension implant regions in the manner taught by Lu could be successfully applied to Saki. *Id.*

6. CONCLUSION

For the foregoing reasons, claims 1-3, 5-14, 16-25, and 27-34 of the '122 patent are unpatentable. Accordingly, Petitioner respectfully requests institution of IPR and cancellation of each of these claims.

Respectfully submitted by:

Date: June 9, 2020

/ Alex V. Chachkes /

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CERTIFICATE OF WORD COUNT

The undersigned certifies that the foregoing PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,580,122 PURSUANT TO 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42 complies with the type volume limitation in 37 C.F.R. § 42.24(a)(1). According to the utilized word-processing system's word count, the petition—excluding the caption, table of contents, table of exhibits, mandatory notices, certificate of word count, and certificate of service—contains 13,300 words.

Dated: June 9, 2020

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CERTIFICATE OF SERVICE

The undersigned hereby confirms that the foregoing PETITION FOR *INTER PARTES* REVIEW OF U.S. PATENT NO. 6,580,122 PURSUANT TO 35 U.S.C. §§ 311-319 and 37 C.F.R. § 42 and associated Exhibits 1001-1019 were caused to be served on June 9, 2020 via overnight courier upon the following counsel of record for Patent Owner:

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