

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE

PATENT TRIAL AND APPEAL BOARD

SMIC, AMERICAS,
Petitioner

U.S. Patent No. 6,580,122

Case No. IPR2020-01003

DECLARATION OF DR. SAYFE KIAEI

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I, Dr. Sayfe Kiaei, declare as follows:

I. ASSIGNMENT AND MATERIALS CONSIDERED

1. I have been retained by SMIC, AMERICAS (“SMIC”). I have been asked to prepare this Declaration in connection with a Petition for *Inter Partes* Review (IPR) of U.S. Patent No. 6,580,122 to Wristers et al., which I refer to throughout this Declaration as the ’122 patent.

2. I am not an employee of SMIC or any affiliate or subsidiary of SMIC.

3. I am being compensated at the rate of \$400 per hour for my work, plus reimbursement for expenses. My compensation has not influenced any of my opinions in this matter and does not depend on the outcome of the IPR proceeding.

4. I have been asked to provide analysis and explain the subject matter of the ’122 patent, including the state of the art when the ’122 patent application was filed. I have also been asked to consider, analyze, and explain certain prior art to the ’122 patent including how that art relates to the claims of the ’122 patent and to provide my opinions regarding whether that art renders obvious the claimed subject matter.

5. The opinions expressed in this Declaration are not exhaustive of my opinions regarding the unpatentability of the claims of the ’122 patent. Therefore, the fact that I do not address a particular point should not be understood to indicate

an agreement on my part that any claim complies with the requirements of any applicable patent or other rule.

6. I reserve the right to amend and supplement this declaration in light of additional evidence, arguments, or testimony presented during the IPR proceeding.

7. In forming the opinions set forth in this declaration, I have considered and relied upon my education, knowledge of the relevant field, knowledge of scientific and engineering principles, and my experience. I have also reviewed and considered the '122 patent (Exhibit 1001), its prosecution history (Exhibit 1012), and the following additional materials:

Exhibit	Description
Exhibit 1003	Korean Laid-Open Patent Application No. KR1998-074469 (with associated certified English translation and translator's declaration) (" Yun ")
Exhibit 1004	U.S. Patent No. 5,859,466 (" Wada ")
Exhibit 1005	U.S. Patent No. 6,009,023 (" Lu ")
Exhibit 1006	U.S. Patent No. 5,960,297 (" Saki ")
Exhibit 1007	U.S. Patent No. 6,429,062 (" Rubin ")
Exhibit 1008	U.S. Patent No. 6,037,266 (" Tao ")
Exhibit 1009	U.S. Patent No. 5,578,518 (" Koike ")
Exhibit 1010	U.S. Patent No. 5,206,182 (" Freeman ")
Exhibit 1011	U.S. Patent No. 5,177,028 (" Manning ")
Exhibit 1012	Prosecution History of U.S. Patent No. 6,580,122

Exhibit 1013	Excerpt from Chapter 4 of Sedra & Smith, <i>Microelectronic Circuits</i> , 5th Ed. (2004)
Exhibit 1014	R. K. Pancholy, <i>Gate Protection for CMOS/SOS</i> , 15th Int'l Reliability Physics Symposium, pp. 132-37 (1977)
Exhibit 1015	A. Chatterjee et al., <i>A Shallow Trench Isolation Study for 0.25/0.18 μm CMOS Technologies and Beyond</i> , Symposium on VLSI Technology Digest of Technical Papers, pp. 156-57 (1996)
Exhibit 1016	A. C. Ipri, <i>Sub-Micron Polysilicon Gate CMOS/SOS Technology</i> , 1978 International Electron Devices Meeting, pp. 46-49 (1978)
Exhibit 1017	K. Ahmed et al., <i>Transistor Wars</i> , IEEE Spectrum, Vol. 48, No. 11, pp. 50-66 (2011)
Exhibit 1018	S. Aur et al., <i>Circuit Hot Electron Effect Simulation</i> , International Electron Devices Meeting, pp. 498-501 (1987)
Exhibit 1019	W. K. Henson et al., <i>Analysis of Leakage Currents and Impact on Off-State Power Consumption for CMOS Technology in the 100-nm Regime</i> , IEEE Transactions on Electron Devices, Vol. 47, No. 7, pp. 1393-1400 (2000)

II. BACKGROUND AND QUALIFICATIONS

8. My qualifications are set forth in my curriculum vitae, a copy of which is attached as Attachment A to this Declaration. As set forth in my curriculum vitae:

9. I earned my B.S. in Electrical and Computer Engineering from Washington State University-Northeastern in 1982, a M.S. in Electrical and Computer Engineering from Washington State University in 1984, and a Ph.D. in Electrical and Computer Engineering from Washington State University in 1987.

10. I have been a Professor at Arizona State University (ASU) since 2001. In this capacity, I have served as a Motorola Endowed Professor and Chair in Analog and RF Integrated Circuits. I am also Director of ASU's National Science Foundation Center "Connection One" focusing on integrated circuits. Connection One is an industry/university cooperative research center with over thirty industrial members and five university members focused on developing integrated circuits technologies.

11. I have graduated over 100 M.S. and Ph.D. students working under my supervision on their thesis; many of them have become professors in academia or hold senior positions in the industry. Currently, I supervise 8 M.S., Ph.D., and post-doctoral students on research related to integrated circuits, analog and RF integrated circuits, device fabrication, and other technical fields.

12. From 2009 to 2012, and concurrent with my position at ASU, I was the Associate Dean of Research at the Ira A. Fulton Schools of Engineering.

13. From 1993 to 2001, I served as a Senior Member of Technical Staff with the Wireless Technology Center and Broadband Operations at Motorola. In that capacity, I was responsible for the development of integrated circuits for RF and digital subscriber lines (DSL) transceivers.

14. From 1987 to 1993, I served as an Associate Professor at Oregon State University.

15. In addition to the above noted positions, I was the Co-Director of the Industry-University Center for the Design of Analog/Digital ICs (CDADIC). Also, I am an IEEE Fellow, and have been the Chair and on the Technical Program Committee of several IEEE conferences including RFIC, MTT, ISCAS and other international conferences.

16. In total, I have more than 35 years of experience in research, development, design, commercialization, evaluation, and testing, of integrated circuits, wireless technologies and related products and systems. My research interests include mixed-signal IC's in CMOS and SiGe, wireless transceiver design, and RF.

17. I have published over 150 journal and conference papers covering topics such as integrated circuits, communication systems, signal processing, radio frequency, filter design, and related technical fields. A list of my publications can be found in my CV, which accompanies this Declaration as Attachment A. I have also been awarded several U.S. patents.

18. Additional details of my education and work experience, awards and honors, and publications that may be relevant to the opinions I have formed are set forth in my curriculum vitae, which accompanies this Declaration as Attachment A. A listing of the cases in which I have testified either at trial or deposition within the previous 4 years accompanies this declaration as Attachment B.

III. UNDERSTANDING OF THE LAW

19. I am not an attorney, but have been instructed in and applied the law as described in this section.

20. I understand that the first step in comparing an asserted claim to the prior art is for the claim to be properly construed. I address how a person of ordinary skill in the art would have understood the claims of the alleged invention in Section VI below.

21. I understand that a patent claim is anticipated when a single piece of prior art describes every element of the claimed invention, either expressly or inherently, and arranged in the same way as in the claim. For inherent anticipation to be found, it is required that the missing descriptive material is necessarily present in the prior art.

22. I have been further instructed and understand a patent claim is unpatentable and invalid as obvious if the subject matter of the claim as a whole would have been obvious to a person of ordinary skill in the art of the claimed subject matter as of the time of the invention at issue. I understand that when assessing the obviousness of claimed subject matter, the following factors are evaluated: (1) the scope and content of the prior art; (2) the difference or differences between each claim of the patent and the prior art; and (3) the level of

ordinary skill in the art at the time the patent was filed. I have been informed that these are sometimes referred to as the “Graham factors.”

23. I understand that claimed subject matter may be obvious in view of more than one item of prior art. I understand, however, that it is not enough to show simply that all the limitations of the claimed subject matter are spread throughout the prior art. Instead, for claimed subject matter to be obvious over multiple references, there must be some reason or motivation for one of ordinary skill in the art to combine the prior art references to arrive at the claimed subject matter.

24. I have been informed that, in seeking to determine whether an invention that is a combination of known elements would have been obvious to a person of ordinary skill in the art at the time of the invention, one must consider the references in their entirety to ascertain whether the disclosures in those references render the combination obvious to such a person.

25. I have been informed and understand that the prior art references themselves may provide a teaching, suggestion, motivation, or reason to combine, but other times the nexus linking two or more prior art references is common sense to a person of ordinary skill in the art at the time of the invention.

26. I understand that a particular combination may be proven obvious merely by showing that it was obvious to try the combination. I have been

informed that, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his or her skill.

27. I further understand that an obviousness analysis recognizes that market demand, rather than scientific literature, often drives innovation, and that a motivation to combine references also may be supplied by the direction of the marketplace. For example, when there is a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within his or her technical grasp because the result is likely the product not of innovation but of ordinary skill and common sense.

28. I have been informed that the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. Thus, where all of the elements of a claim are used in substantially the same manner, in devices in the same field of endeavor, the claim is likely obvious.

29. Additionally, I understand that a patent is likely to be invalid for obviousness if a person of ordinary skill can implement a predictable variation or if there existed at the time of the invention a known problem for which there was an

obvious solution encompassed by the patent's claims. Therefore, when a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one.

30. I further understand that combining embodiments related to each other (e.g., by being disclosed near each other) in a single prior art reference would not ordinarily require a leap of inventiveness.

31. I also understand that one of ordinary skill in the art must have had a reasonable expectation of success when combining references for claimed subject matter to be obvious.

32. I have been informed and I understand that factors referred to as "objective indicia of non-obviousness" or "secondary considerations" are also to be considered when assessing obviousness when such evidence is available. I understand that these factors can include: (1) commercial success; (2) long-felt but unresolved needs; (3) copying of the invention by others in the field; (4) initial expressions of disbelief by experts in the field; (5) failure of others to solve the problem the claimed subject matter solved; and (6) unexpected results.

33. I also understand that evidence of objective indicia of non-obviousness must be commensurate in scope with the claimed subject matter. I further understand that there must be a relationship, sometimes referred to as a "nexus," between any such secondary indicia and the claimed invention.

34. Finally, I have been informed that one cannot use hindsight to determine that an invention was obvious.

35. I provide my opinions in this report based on the guidelines set forth above.

IV. LEVEL OF SKILL IN THE ART

36. I have been informed and understand that the level of ordinary skill in the relevant art at the time of the invention is relevant to inquiries such as the meaning of claim terms, the meaning of disclosures found in the prior art, and the reasons one of ordinary skill in the art may have for combining references.

37. I have been informed and understand that factors that may be considered in determining the level of ordinary skill include: (1) the education of the inventor; (2) the type of problems encountered in the art; (3) prior art solutions to those problems; (4) rapidity with which innovations are made; (5) sophistication of the technology; and (6) education level of active workers in the relevant field. I have been further informed and understand that a person of ordinary skill in the art is also a person of ordinary creativity.

38. In my opinion, the ordinarily skilled artisan in the technology field of the '122 patent would have had at least a Bachelor of Science degree in electrical engineering, physics, chemistry, chemical engineering, material science, or a closely related field and at least 3 years of experience in

semiconductor process, design, or fabrication. An individual with an advanced degree in a relevant field would require less experience in semiconductor devices.

39. Additionally, the ordinarily skilled artisan in the technology field of the '122 patent would have been familiar with the general structure of semiconductor devices, the fabrication process, isolation structures such as shallow trench isolation (STI), gate insulation layers, implant regions, and methods to improve the performance of semiconductor devices and CMOS integrated circuits.

V. THE '122 PATENT'S EFFECTIVE FILING DATE

40. I understand that the application leading to the '122 patent was filed on March 20, 2001. No earlier filed applications are identified on the face of the '122 patent.

41. For purposes of this declaration, I have considered both the understanding and knowledge of one of ordinary skill in the art and unpatentability as of this July 12, 2001 date.

VI. CLAIM INTERPRETATION

42. I understand that during an *inter partes* review, claim terms are interpreted based on the *Philips* claim construction standard.

43. It is my understanding that this means claim terms are to be given their plain meaning unless it is inconsistent with the specification.

VII. OVERVIEW OF THE '122 PATENT

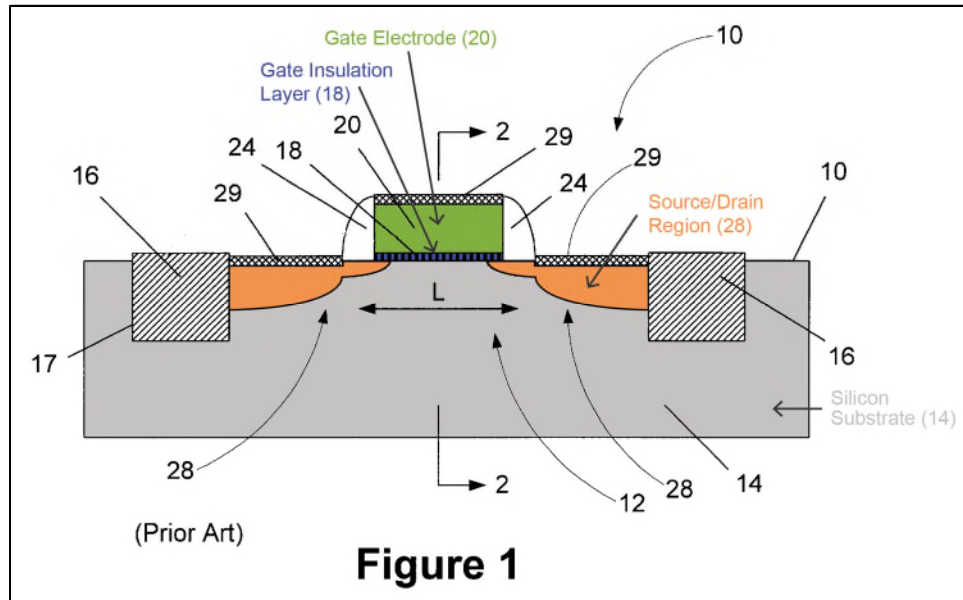
A. Technological Background

1. Introduction to Transistors and MOSFET Technology

44. The '122 patent relates to transistors such as a Metal Oxide Semiconductor Field-Effect Transistor (“**MOSFET**”). MOSFETs are the most common transistors used in integrated circuits (ICs), because, among other things, of their relative ease of fabrication, lower cost, and lower power consumption. The MOS transistor was invented at Bell Labs in 1959 and has become the basic building block of modern electronics and ICs used for memory, processors, analog and digital ICs, wireless and portable systems, and a myriad of other devices and applications.

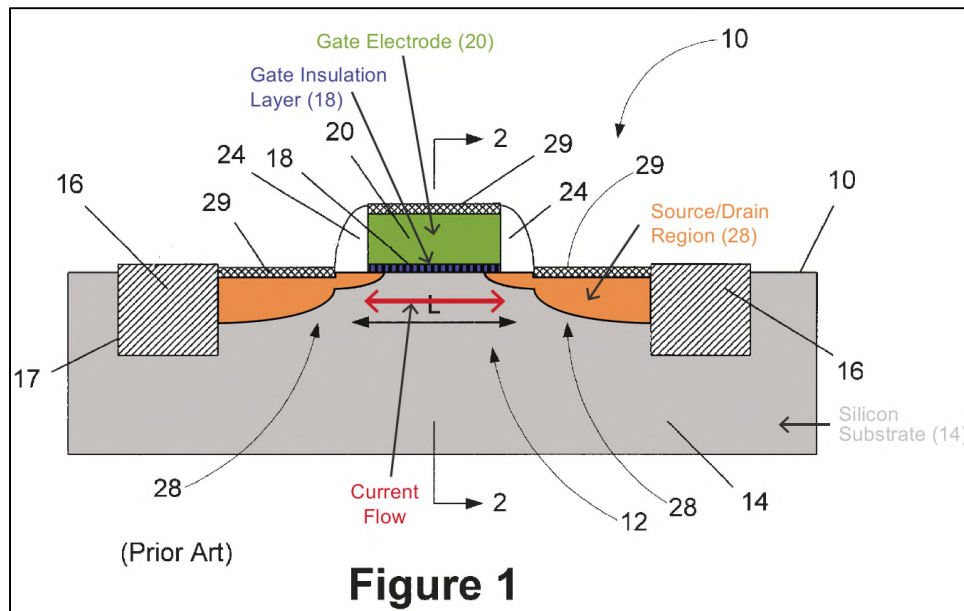
45. MOSFETs can be either *N-type* (also known as an “**NMOS**” or “**N-channel**” transistor) or *P-type* (“**PMOS**” or “**P-channel**” transistor). An integrated circuit with both NMOS and PMOS transistors formed on the same substrate is referred to as a complementary metal–oxide–semiconductor (CMOS) that uses complementary and symmetrical pairs of NMOS and PMOS transistors. A CMOS circuit can be formed on the same substrate by creating a well. CMOS technology is used for constructing IC chips, including memory, processors, analog circuits, image sensors for cameras, wireless radio frequency RF circuits, and a myriad of other devices and applications.

46. I have provided below an example of a prior art transistor from Fig. 1 of the '122 patent:



47. Specifically, a transistor (element 10) is formed in and on a silicon substrate (element 14) and has four terminals: a gate electrode (element 20) that is isolated from the substrate (element 14) by a gate insulation layer (element 18), and source and drain regions (elements 28) formed in the substrate (which can be regarded as the fourth terminal) on each side of the gate.

48. A transistor functions by applying a gate voltage V_G to the gate terminal, which induces a conducting channel under the gate (e.g., in the area in between the source/drain regions of the '122 patent's Fig. 1) that allows current to flow between the source and drain (as shown below).



49. Increasing the gate voltage V_G will cause the channel resistance to decrease further, causing an increase in the drain current, I_{DS} through the channel. The source and drain are doped areas (known as the “active region” or “active area”) that serve as the sources for particles (e.g., electrons or holes) to flow into and out of the channel. The channel region is lightly doped with a dopant type that is opposite to that of the source and drain.

50. Generally speaking, a transistor “gate” refers to two basic components: (1) a *gate insulation layer* (also known as a “gate oxide” or “gate dielectric”; element 18 in the ’122 patent’s Fig. 1, above), and (2) a *gate electrode*. The gate electrode (element 20 in the ’122 patent’s Fig. 1) is a conductor to connect the gate input voltage V_G to the transistor gate. The “conductor” that makes up the gate electrode may be polysilicon and/or a metal silicide, rather than a pure metal (in practice, it is common for the gate electrode to not be a pure

metal) in 2001. Additionally, the gate oxide isolates the gate from the substrate so that there is no current flow from the gate to the conducting channel. The gate oxide is typically formed of silicon dioxide (SiO_2). Excerpt from Chapter 4 of Sedra & Smith, *Microelectronic Circuits*, 5th Ed. (2004) (Ex. 1013); Ex. 1007 (Rubin), 1:23-25 (“The conduction is along a ‘channel’ that is spaced from the gate by a silicon dioxide layer, referred to as a ‘gate oxide.’”); Ex. 1008 (Tao), 1:28-32 (“a substrate is typically formed with an oxide layer, such as silicon dioxide. This oxide layer may function as a gate oxide to the active devices formed on the substrate.”).

51. Thus, the operation of a typical transistor involves applying an input voltage to the gate electrode or terminal, which then creates an electric field in the channel region. Of course, the electric field can be varied to modulate the conductance of the channel region.

2. The Need for Improved Transistor Performance

52. The number of transistors on a IC chip has constantly *increased* over time (a phenomenon widely known as “Moore’s Law”) while the dimensions of transistors have constantly *decreased* over time. Specifically, the transistor gate length L , which is known as the transistor feature size, has shrunk over time. Current advanced CMOS technologies, for example, include transistors less than 20 nm (i.e., 20×10^{-9} m) in size. As the devices shrink in size to *nanometer* device

sizes with lower supply voltages, the transistor switching speed and performance suffers, due to decreased *drive current*. Thus, one way to improve transistor performance is to increase the drive current.

53. Specifically, drive current is a measure of current flow across the channel region of a transistor under the gate and between the source and drain regions. It is well known that the drain to source drive current (“ I_{DS} ”) of a transistor is proportional to its width (“ W ”) and inversely proportional to the length (“ L ”). This relationship is illustrated by the following equation:

$$I_{DS} = K' \frac{W}{L} (V_{GS} - V_{TH})^2$$

54. By examining the equation above, we see that increasing W or reducing L will increase the transistor’s drive current. Increasing W or reducing L , however, affects other transistor properties and may cause an undesirable increase in the “off-state leakage current.” This refers to current flow between the drain and source when the transistor is *not* in an operating state (e.g., for an NMOS transistor, when the device is in the “subthreshold” or “off-state” and V_{GS} is less than V_{TH}). Reducing off-state leakage current is critical to minimizing transistor and integrated circuit power consumption.

3. Forming Isolation Structures in the Substrate Was Well Known in the Art

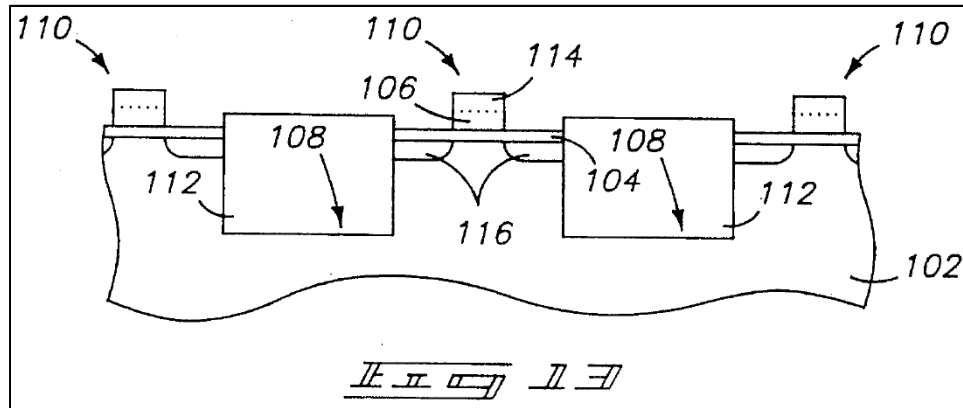
55. Before the '122 patent was filed in 2001, it was well known in the art to use isolation structures to electrically isolate transistors. Sufficient isolation is important to the proper functioning of individual transistors and the electronic devices that rely on them. As an increasing number of transistors were packed into a constantly shrinking area, however, achieving isolation became more challenging. For example, as Koike recognized in 1994:

With the advance of microminiaturization (fine structuring) of integrated circuits, the area allowed for device isolation regions has been increasingly reduced. Thus, these conventional device isolation regions formed by means of LOCOS (Local Oxidation Of Silicon) are becoming difficult to use.

Ex. 1009 (Koike), 1:14-19.

56. Well known methods of isolation include Shallow Trench Isolation (STI) and Local Oxidation Of Silicon (LOCOS). These methods have been utilized since the 1990s and earlier. For example, U.S. Patent No. 5,206,182, filed in 1989, describes “an improved integrated circuit process in which adjacent devices are isolated by a trench” that improves upon prior art trench processes. Ex. 1010, 1:24-30 and 1:64-66. Similarly, U.S. Patent No. 5,177,028 (Ex. 1011)

describes “a method for isolating field effect transistors using trench isolation techniques” as shown in its Fig. 13 below:



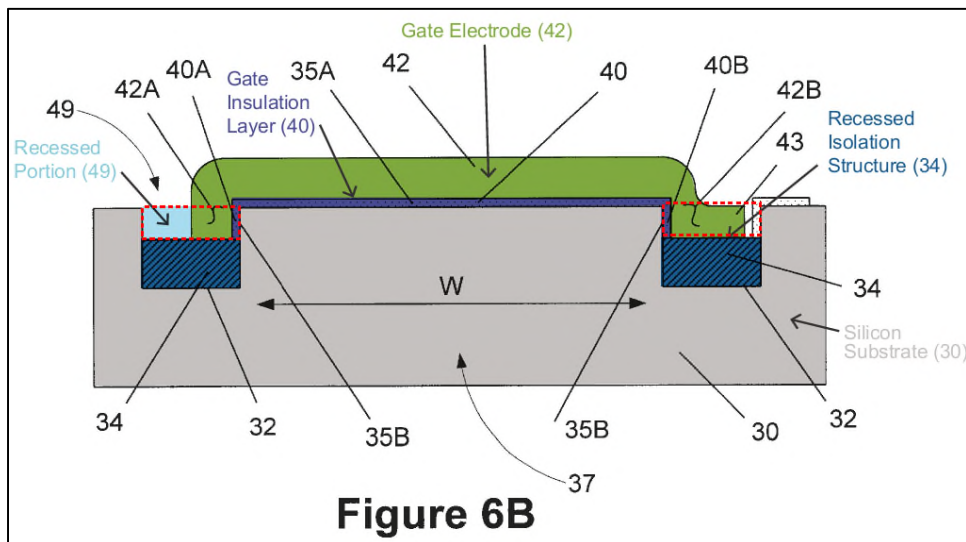
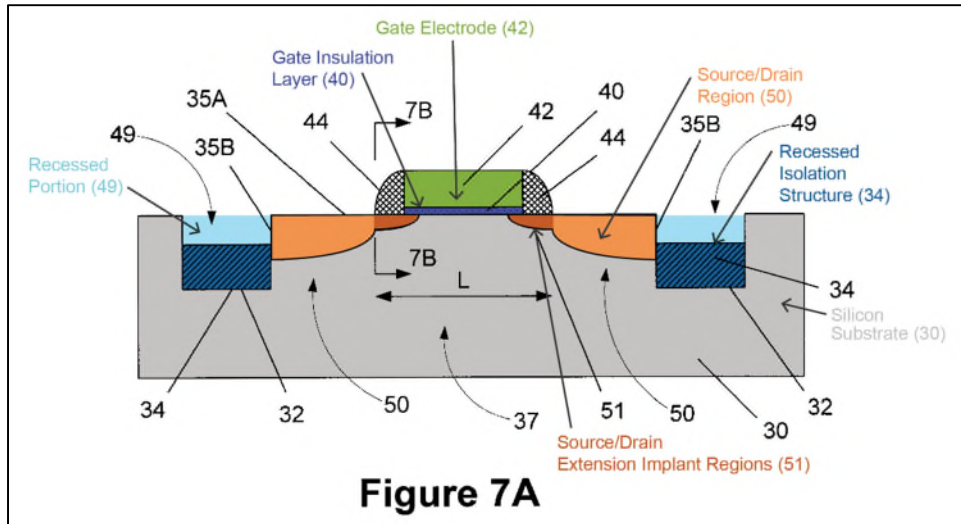
B. Overview of the '122 Patent

57. The '122 patent relates generally to a “semiconductor device having an enhanced width dimension.” Ex. 1001, 1:10-11.

58. The '122 patent states that the “demand for increased speed has resulted in a continual reduction in the size of semiconductor devices.” Ex. 1001, 1:18-20. A transistor’s speed and overall performance depends on its “drive current,” which the '122 patent defines as “the amount of current flowing from the drain region to the source region of the transistor.” Ex. 1001, 1:62-66. As discussed above and recognized in the prior art, the '122 patent explains that the drive current, in turn, depends on the transistor’s channel length (“ L ”) and width (“ W ”). Ex. 1001, 2:5-20. Specifically, reducing L or increasing W results in increased drive current. Ex. 1001, 2:5-20.

59. According to the '122 patent, it is desirable to maximize the drive current without otherwise adversely impacting the transistor's performance, such as "generating excessive heat or excessive off-state leakage currents." Ex. 1001, 1:66 – 2:4. In this regard, the '122 patent notes that off-state leakage current increases *exponentially* as *L* decreases; in contrast, the leakage current increases at a lower rate as *W* increases. Ex. 1001, 2:5-20. "Thus, it would be desirable to have a transistor in which the width dimension of a substrate can be maximized in a given plot space of semiconducting substrate." Ex. 1001, 2:35-38.

60. Figures 3 – 7C depict the semiconductor device contemplated by the '122 patent. The figures show the semiconductor device at various stages of the fabrication process. Fig. 6B, for example, is a view of the device along the *transistor gate width (W) dimension* after the gate electrode has been patterned from a layer of polysilicon. Ex. 1001, 5:33-45. And Fig. 7A, which shows the device after the following step of forming source/drain regions, shows the device along the *transistor gate length (L) dimension*. Ex. 1001, 5:58-65. The annotations of Figs. 7A and 6B provided below illustrate the relevant device elements visible in each view.



61. It is common to provide multiple views of a transistor to highlight different features; typical views include a top or plan view, along the length (L) dimension, along the width (W) dimension, and so forth. Certain transistor elements may be depicted in one view but not another. For example, the source/drain regions appear in the '122 patent's length dimension view (Fig. 7A above) but not in the width dimension view (Fig. 6B above).

62. The transistor includes substrate 30 with gate electrode 42 and gate insulation layer 40 formed on the substrate. Ex. 1001, 6:62 – 7:3. Recessed isolation structure 34, as well as source and drain regions 50, are formed in the substrate. Ex. 1001, 5:58-63; 7:45 – 55. I note that the '122 patent also uses the term “recessed isolation material” to refer to the same element 34. Further, recessed isolation structure 34 defines a recessed portion (indicated by element 49) and includes a layer of insulating material in the trench 32. Ex. 1001, 4:21-56. The recessed portion includes the full void above the insulating material as indicated by the red dashed lines in annotated Fig. 6B above. And as depicted in Fig. 6B, the recessed portion is partially filled in by the gate insulation layer and gate electrode.

C. Claims of the '122 Patent

63. Claims 1-3, 5-14, 16-25, and 27-34 are reproduced below for reference:

1. A transistor, comprising:

a semiconducting substrate;

a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove;

a gate electrode and a gate insulation layer formed above said substrate, a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure; and

a source region and a drain region formed in said substrate.

2. The transistor of claim 1, wherein said semiconducting substrate is comprised of silicon.

3. The transistor of claim 1, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.

5. The transistor of claim 1, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.

6. The transistor of claim 1, wherein said gate electrode is comprised of polysilicon.

7. The transistor of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.

8. The transistor of claim 1, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.

9. The transistor of claim 1, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.

10. The transistor of claim 1, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.

11. The transistor of claim 1, wherein said gate electrode has first and second end portions that extend into said recess.

12. The transistor of claim 11, wherein said first and second end portions extending into said recess are positioned above a portion of a sidewall of an active

region of said substrate defined by said recessed isolation structure.

13. A transistor, comprising:

a semiconducting substrate comprised of silicon;

a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove;

a gate electrode comprised of polysilicon and a gate insulation layer formed above said substrate, a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure; and

a source region and a drain region formed in said substrate.

14. The transistor of claim 13, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.

16. The transistor of claim 13, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.

17. The transistor of claim 13, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.

18. The transistor of claim 13, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.

19. The transistor of claim 13, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.

20. The transistor of claim 13, wherein said source region and said drain region are each comprised of an

extension implant region and a source/drain implant region.

21. The transistor of claim 13, wherein said gate electrode has first and second end portions that extend into said recess in said substrate.

22. The transistor of claim 21, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.

23. A transistor, comprising:

a semiconducting substrate;

a recessed isolation structure defining an active area having an upper surface and an exposed sidewall surface;

a gate insulation layer and a gate electrode positioned above a portion of said upper surface and a portion of said exposed sidewall surface of said active area; and

a source region and a drain region formed in said active area.

24. The transistor of claim 23, wherein said semiconducting substrate is comprised of silicon.

25. The transistor of claim 23, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.

27. The transistor of claim 23, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.

28. The transistor of claim 23, wherein said gate electrode is comprised of polysilicon.

29. The transistor of claim 23, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.

30. The transistor of claim 23, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.

31. The transistor of claim 23, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.

32. The transistor of claim 23, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.

33. The transistor of claim 23, wherein said gate electrode has first and second end portions that extend into a recess in said substrate defined by said recessed isolation structure.

34. The transistor of claim 33, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.

VIII. INVALIDITY ANALYSIS BASED ON YUN

64. Yun indicates on its face that it published on November 5, 1998. In view of this date of publication, I understand that Yun is prior art pursuant to 35 U.S.C. § 102(b).

65. I note that Yun was neither cited nor discussed by the Examiner during prosecution.

A. Overview of Yun

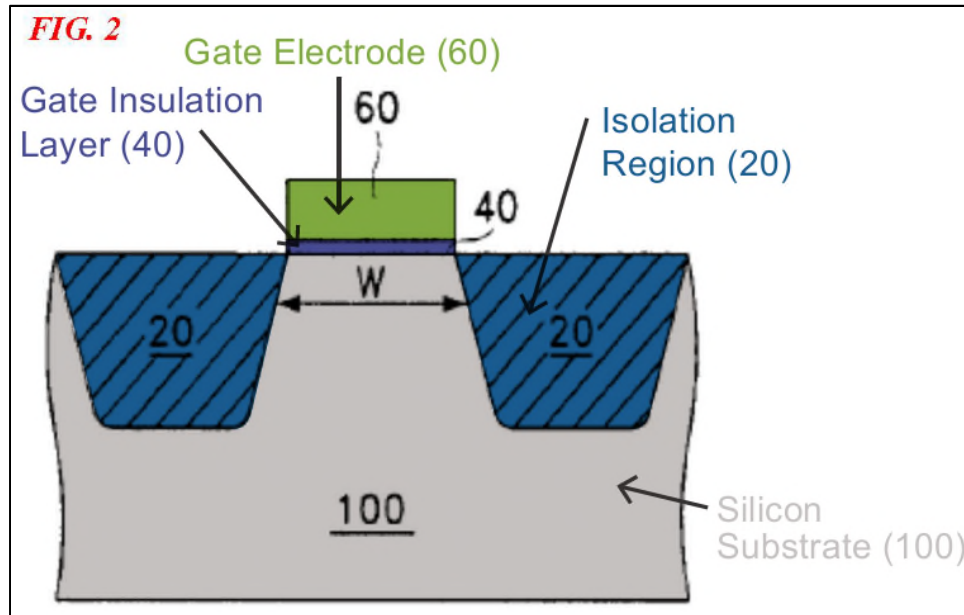
66. Yun relates to semiconductor devices and methods for manufacturing them. Like the '122 patent, Yun focuses on increasing the drive current of a transistor by increasing the channel width. Ex. 1003 (Yun), 1-5 and 2-5.¹ In particular, Yun describes that:

It is the object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can *improve the electric current driving capability of a transistor by increasing the channel width* without increasing the chip area by vertically forming a part of the channel region.

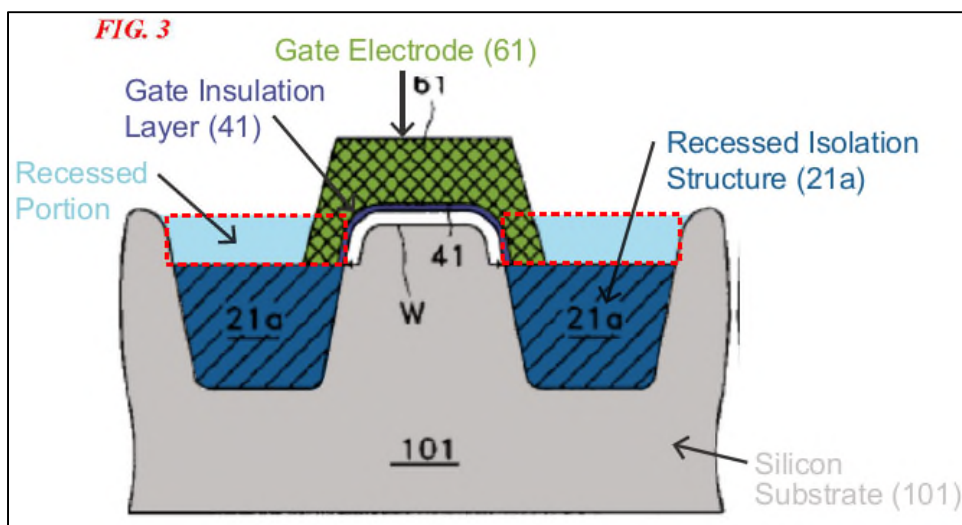
Ex. 1003 (Yun), 2-5. In other words, Yun teaches increasing the effective width of the transistor active area without increasing the chip size. Ex. 1003 (Yun), 2-5.

67. With respect to Fig. 2 below, Yun discloses a prior art transistor having: (i) “a channel region W directly formed on a silicon substrate 100”; (ii) “an isolation region 20 for isolating the device”; (iii) “a gate oxide film 40 formed on top of channel width W”; and (iv) “gate electrode 60 formed thereon.” Ex. 1003 (Yun), 1-5. As Yun explains: “when the channel width W is increased to increase the current-driving amount of a transistor, it immediately results in an increase in the size of the area.” Ex. 1003 (Yun), 1-5. As I discussed above, an increase in

¹ All references to Yun are to the certified English translation.



68. To improve upon the prior art transistor, Yun teaches the transistor depicted in Fig. 3 below. Yun's transistor includes: (i) "isolation regions 21a" formed on silicon substrate 101 and with a gate formed between the isolation regions; (ii) "gate oxide film 41" formed "on the area where the silicon substrate is higher by a predetermined height relative to the upper part of the isolation region 21a"; and (iii) "a gate electrode 61" formed "on the upper part thereof." Ex. 1003 (Yun), 2-5.



69. Yun also explains that “the *channel width is raised by a predetermined height relative to the isolation region 21a and for a curve by as much as the height, thereby increasing the channel width*. In doing so, there will not be any change in the chip area.” Ex. 1003 (Yun), 2-5. Thus, by forming the transistor in this way, Yun notes that it is possible “to obtain stable isolation characteristics while increasing the channel width of a transistor by adjusting the depth of the oxide film in the trench.” Ex. 1003 (Yun), 2-5. In other words, the channel width can be further increased by extending gate electrode 61 and gate oxide film 41 further into the trench. This is accomplished by reducing the depth of the oxide film in the trench.

B. Ground 1. Claims 1-2 and 11-12 Are Anticipated By Yun

1. Yun Anticipates Claim 1

a. “A transistor, comprising:”

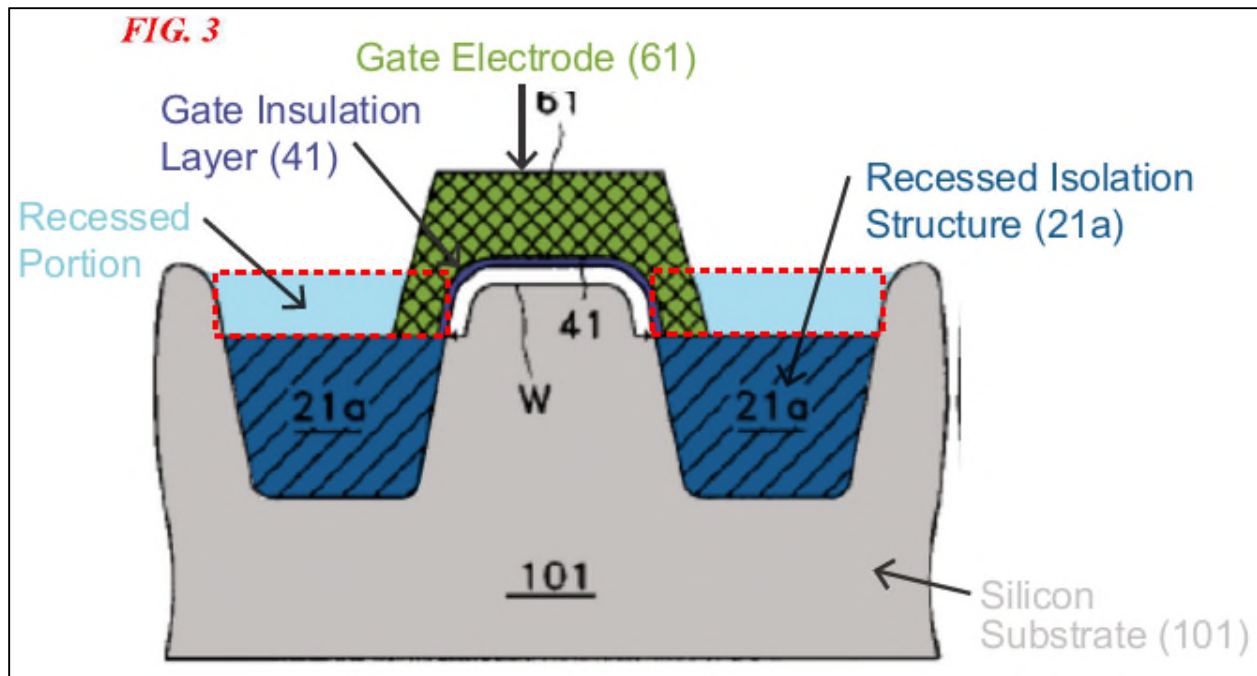
70. Yun discloses a transistor. See Ex. 1003 (Yun), 1-5 and 2-5.

b. “a semiconducting substrate;”

71. Yun discloses forming a transistor on substrate 101. Ex. 1003 (Yun), 2-5. I note that substrate 101 is formed of silicon. Ex. 1003 (Yun), 2-5.

c. “a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove;”

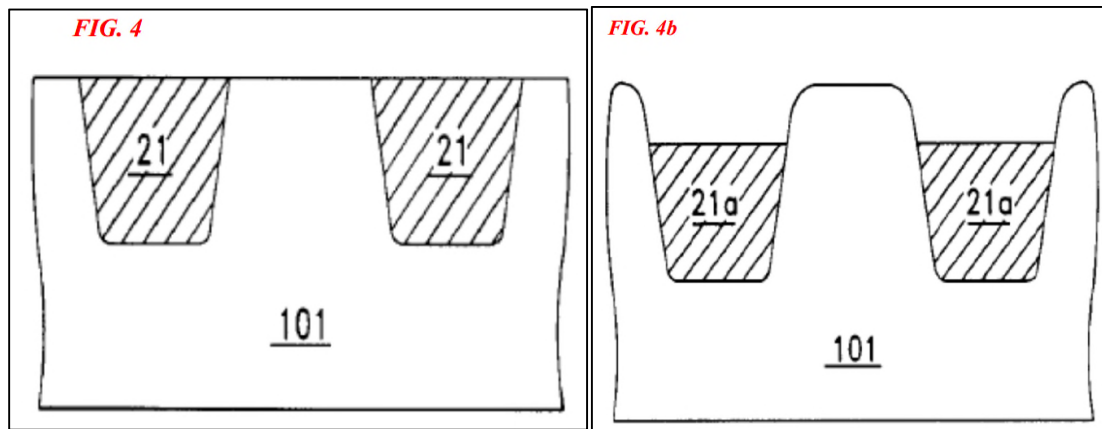
72. Yun discloses a transistor having isolation regions 21a formed on substrate 101, as depicted in Fig. 3 below. Isolation region 21 includes an oxide film, which is an insulating material, formed inside the trench. As can be verified visually, isolation region 21 defines a recess in the region above the oxide film. *See* Ex. 1003 (Yun), 2-5. This recessed portion includes the full void above the insulating material as indicated by the red dashed lines in annotated Fig. 3 below. And, as shown, the recessed portion is partially filled in by the gate insulation layer and gate electrode.



73. Yun's Figs. 4a and 4b (reproduced below), which provide views of the transistor fabrication process, further illustrate the formation of the recessed isolation region. Fig. 4a describes forming isolation region 21a using a "conventional trench isolation process." Ex. 1003 (Yun), 2-5. And in Fig. 4b, the oxide film in the trench is etched in order to increase the channel width, thereby forming the recess above. As Yun explains:

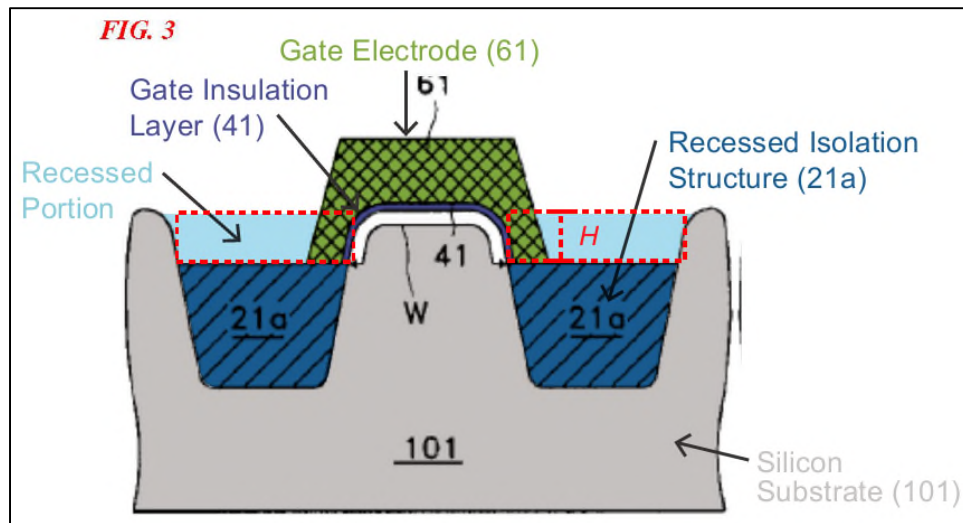
With reference to FIG. 4b, the oxide film 21a inside the trench isolation in the region desired to increase the channel width is etched by 10nm – 200nm by means of a wet etching process. Also, the sacrificial oxide film is sacrificed by 10nm – 30nm to allow the channel region in the angular part to become a more curved surface, thereby increasing the channel width W.

Ex. 1003 (Yun), 2-5.



- d. “a gate electrode and a gate insulation layer formed above said substrate, a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure; and”

74. Yun teaches the formation of gate electrode 61 and gate insulation layer above substrate 101. Ex. 1003 (Yun), 2-5. As can be verified visually with reference to Fig. 3, the end portions of gate electrode 61 and gate insulation layer 41 extend into the recess above the oxide film inside the trench (see element 21a). As Yun explains, extending gate electrode 61 and gate insulation layer 41 into the trench increases the channel width of the transistor. Ex. 1003 (Yun), 2-5. In particular, the effective width is increased by an amount equal to the height by which gate electrode 61 and gate insulation layer 41 are raised above isolate region 21a, as illustrated by the height of the curve (“*H*”) in the figure below. See Ex. 1003 (Yun), 2-5.



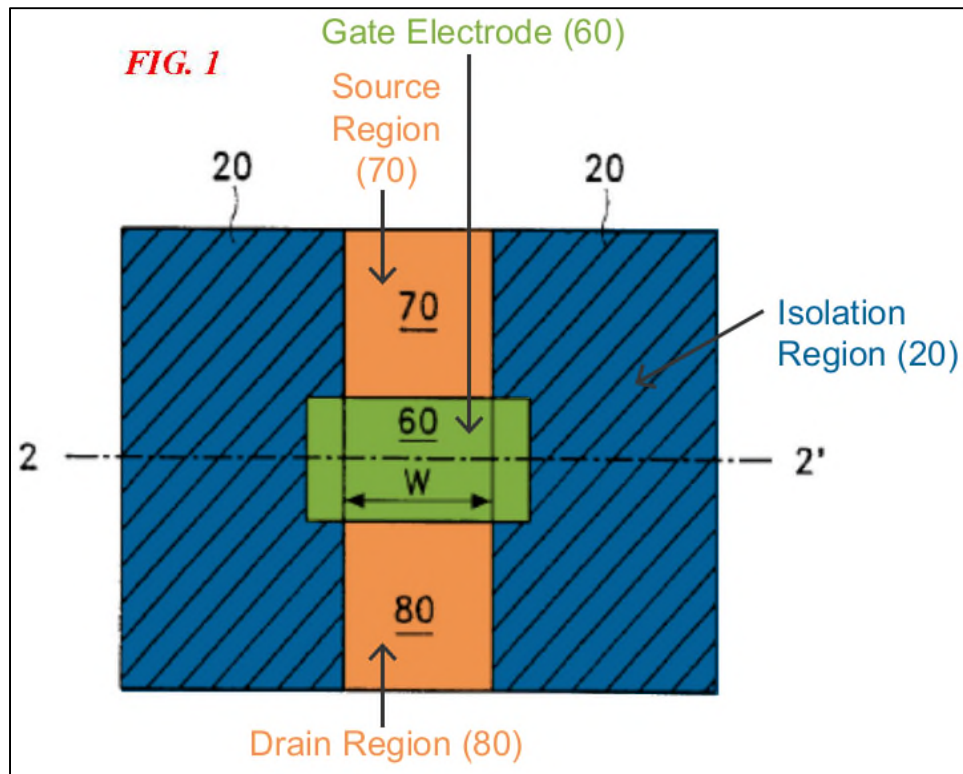
e. “a source region and a drain region formed in said substrate.”

75. Yun notes that the completed transistor includes a source region and a drain region formed in the substrate. As Yun explains:

With reference to FIG. 4c, after the process described above is performed, *a transistor is formed by means of* a gate oxide 41 formation process and *a source and drain formation process*.

Ex. 1003 (Yun), 2-5.

76. Further, Yun describes forming source and drain regions using a “conventional” process (Ex. 1003 (Yun), 1-5 and 2-5); these regions are formed in substrate 101. For example, Fig. 1 of Yun (reproduced below) depicts source 70 and drain 80 formed in the substrate of a prior art transistor fabricated from a conventional process.



2. Yun Anticipates Claim 2

77. Claim 2 depends from claim 1. As I explained above, Yun teaches the subject matter of claim 1.

78. As I will explain below, in my opinion, Yun teaches the additional subject matter of claim 2.

a. “The transistor of claim 1, wherein said semiconducting substrate is comprised of silicon”

79. As discussed above, Yun discloses forming a transistor on silicon substrate 101.

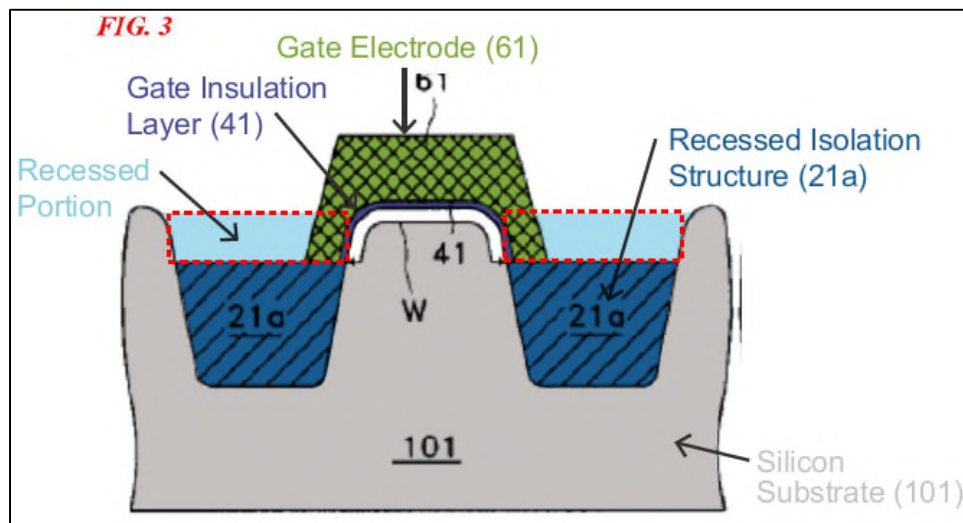
3. Yun Anticipates Claim 11

80. Claim 11 depends from claim 1. As I explained above, Yun teaches the subject matter of claim 1.

81. As I will explain below, in my opinion, Yun teaches the additional subject matter of claim 11.

a. “The transistor of claim 1, wherein said gate electrode has first and second end portions that extend into said recess”

82. As discussed above, Yun discloses that gate electrode 61 extends into the recess above the oxide film inside the trench. Specifically, first and second end portions of gate electrode 61 extend into the recess, as illustrated by the annotated figure below.



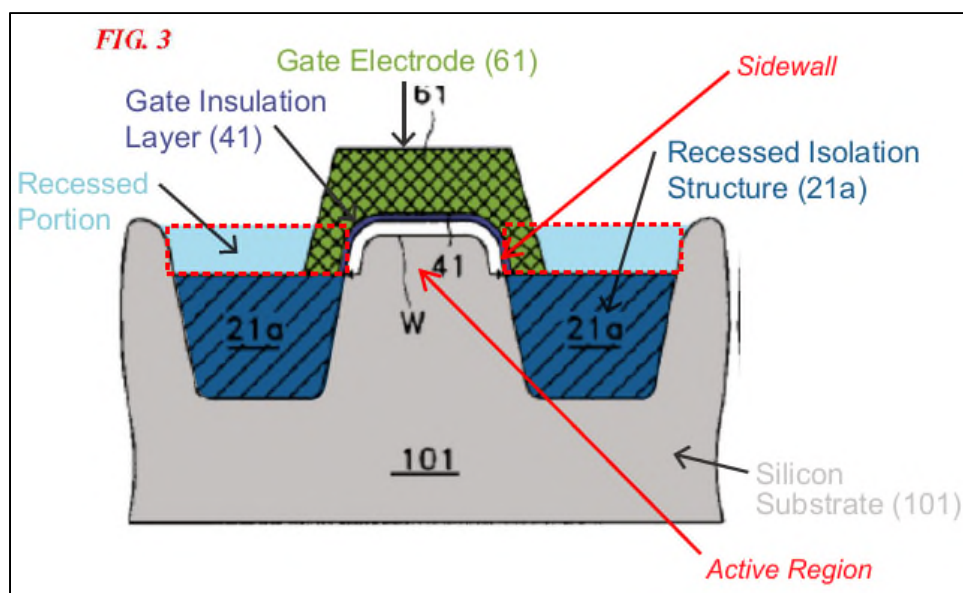
4. Yun Anticipates Claim 12

83. Claim 12 depends from claim 11. As I explained above, Yun teaches the subject matter of claim 11.

84. As I will explain below, in my opinion, Yun teaches the additional subject matter of claim 12.

- a. **“The transistor of claim 11, wherein said first and second end portions extending into said recess are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure”**

85. As can be verified easily by reference to Yun’s Fig. 3 below, the first and second end portions of gate electrode 61 are positioned above a portion of a sidewall of the active region:



C. **Ground 2. Claims 3, 23-25 and 33-34 Are Obvious Over Yun In Light of the Knowledge of a POSITA**

1. **Yun Renders Obvious Claim 3**

86. Claim 3 depends from claim 1. As I explained above, Yun teaches the subject matter of claim 1.

87. As I will explain below, in my opinion, Yun teaches the additional subject matter of claim 3.

a. “The transistor of claim 1, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride”

88. Yun teaches forming a recessed isolation structure (isolation region 21a), which includes an oxide film formed inside the trench. An oxide film, in the field of semiconductor fabrication, includes the class of silicon dioxide (SiO_2) insulators, which is one of the most common CMOS gate insulators used in the art. *See, e.g.*, Excerpt from Chapter 4 of Sedra & Smith, *Microelectronic Circuits*, 5th Ed. (2004) (Ex. 1013) (noting, for an illustrative MOSFET transistor, that an “oxide” layer is formed of SiO_2). As another example, Tao notes that “a substrate is typically formed with an oxide layer, such as silicon dioxide. This oxide layer may function as a gate oxide to the active devices formed on the substrate.” Tao, 1:28-32. Further, “oxide” and “oxide film” are well understood in the field of semiconductor fabrication as terms that refer to silicon dioxide, as discussed above in ¶50. *See also* R. K. Pancholy, *Gate Protection for CMOS/SOS*, 15th Int’l Reliability Physics Symposium, pp. 132-37 (1977) (describing the gate oxide and using the terms “oxide” and “silicon dioxide” interchangeably) (Ex. 1014).

89. Further, a POSITA reading Yun would understand Yun’s oxide film as being silicon dioxide when also considering that Yun uses a *silicon* substrate.

90. Thus, in my opinion, Yun teaches the subject matter of this claim.

2. Yun Renders Obvious Claim 23

a. “A transistor, comprising:”

91. Yun teaches the subject matter of this claim limitation for the reasons provided in Section VIII.B.1.a.

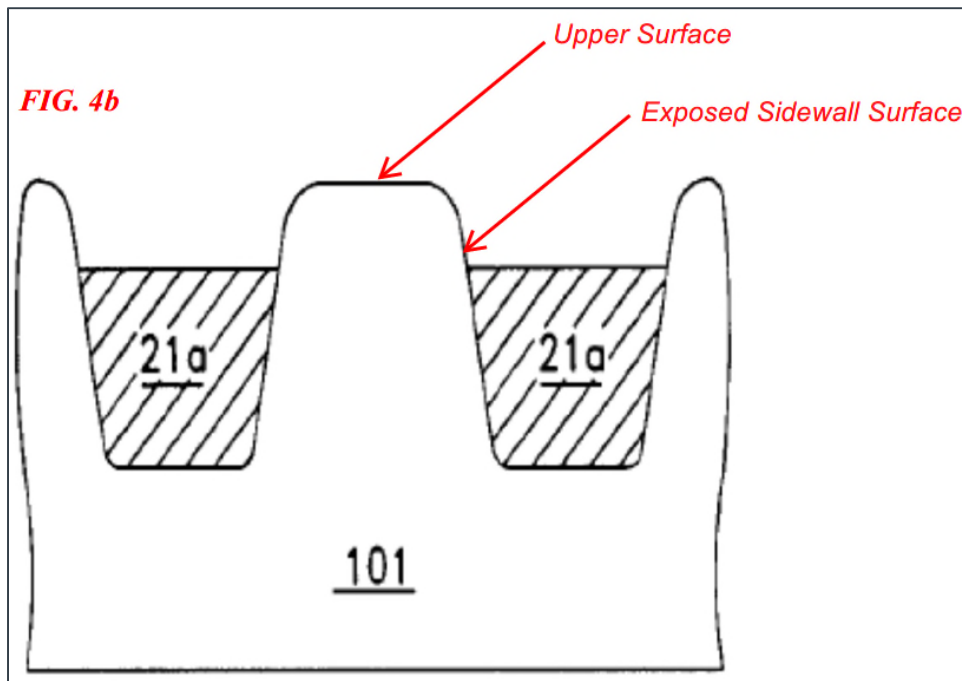
b. “a semiconducting substrate;”

92. Yun teaches the subject matter of this claim limitation for the reasons provided in Section VIII.B.1.b.

c. “a recessed isolation structure defining an active area having an upper surface and an exposed sidewall surface;”

93. Yun teaches the subject matter of this claim limitation for the reasons provided in Section VIII.B.1.c.

94. Further, Yun teaches “a process of *forming a trench isolation region and an active region on a silicon substrate* by means of a conventional trench isolation process.” Ex. 1003 (Yun), 1-5. Specifically, Yun teaches forming isolation regions 21a, which include a recessed portion over a portion filled with an oxide film insulator, as illustrated in Fig. 3 below. As shown, isolation regions 21a define an active area having an upper surface and an exposed sidewall surface.

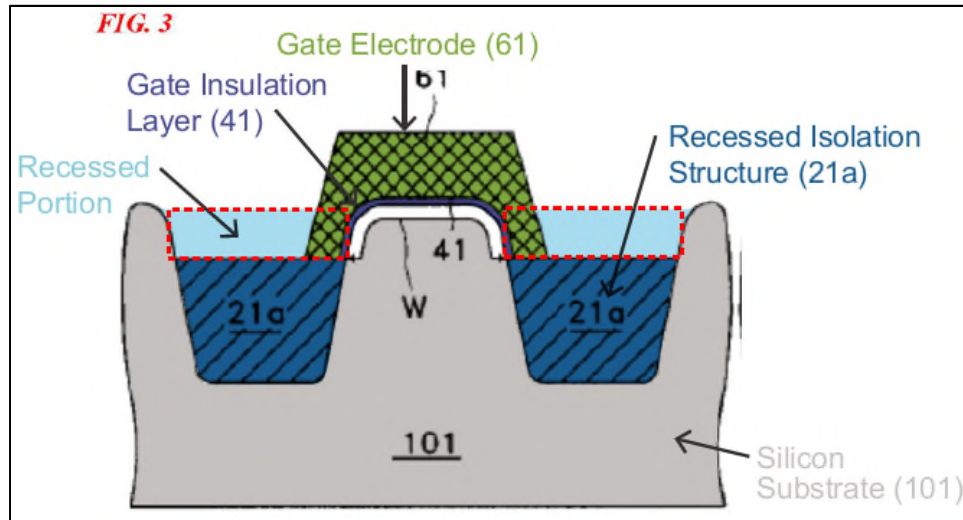


- d. “a gate insulation layer and a gate electrode positioned above a portion of said upper surface and a portion of said exposed sidewall surface of said active area; and”

95. Yun teaches the subject matter of this claim limitation for the reasons provided in Section VIII.B.1.d.

96. Yun teaches forming gate electrode 61 and gate insulation layer 41 above substrate 101. Specifically, Yun discloses that “a *gate oxide film 41 is formed on the area where the silicon substrate is higher* by a predetermined height relative to the upper part of the isolation region 21a; and a *gate electrode 61 is formed on the upper part thereof.*” Ex. 1003 (Yun), 2-5. And as can be verified visually from Yun’s Fig. 3 below, gate electrode 61 and gate insulation

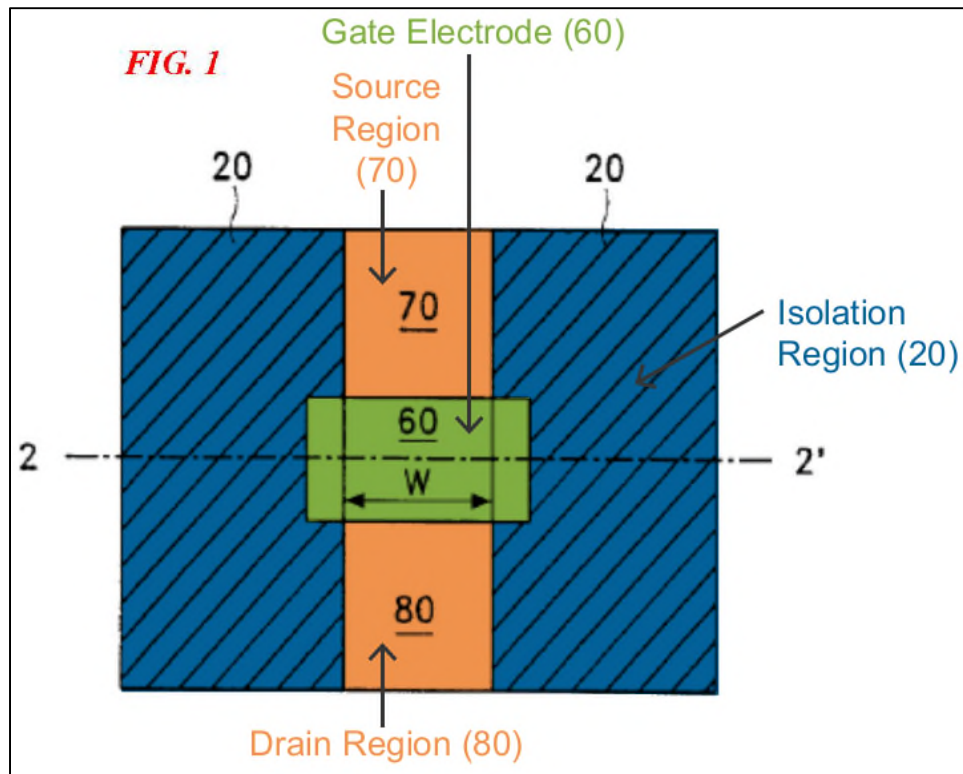
layer 41 are positioned above the upper surface and exposed sidewall surface of the active area.



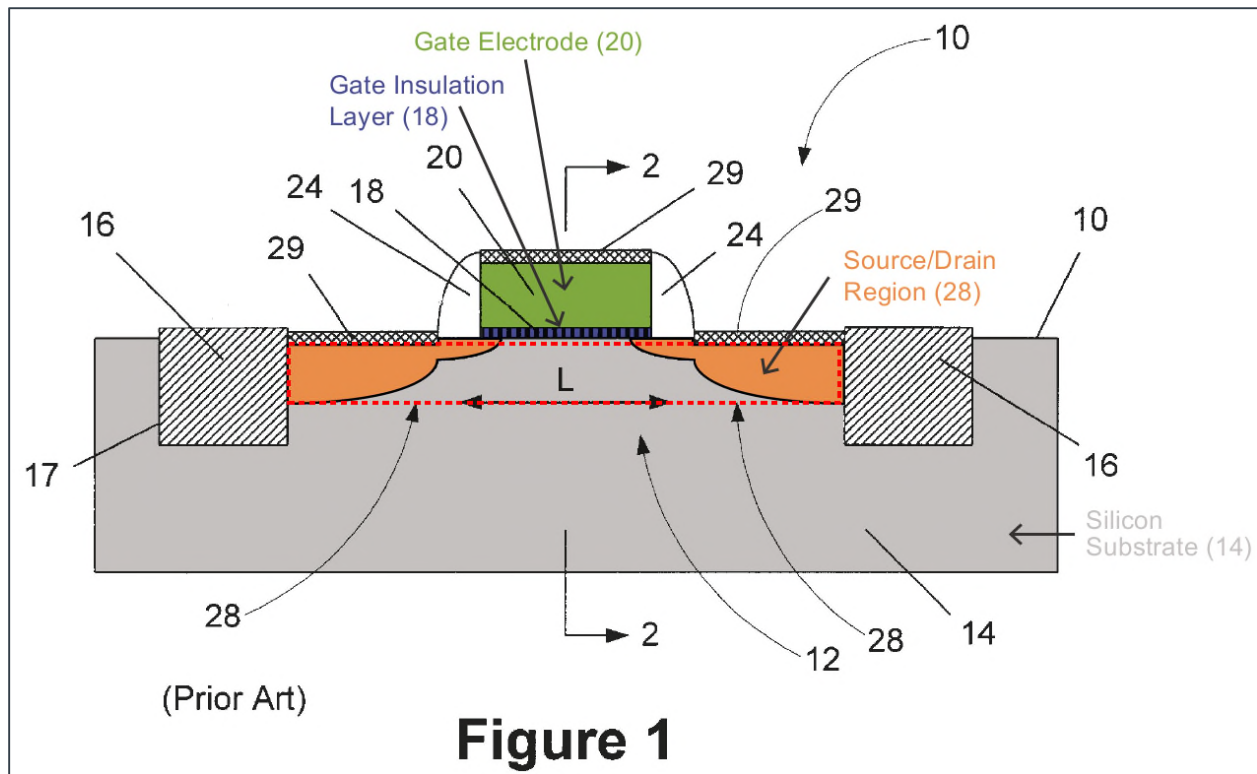
e. “a source region and a drain region formed in said active area.”

97. Yun teaches the subject matter of this claim limitation for the reasons provided in Section VIII.B.1.e.

98. Yun teaches “a process of forming *conventional* gate oxide film, gate electrode, *source, and drain*.” Ex. 1003 (Yun), 1-5. As Yun explains: “Here, the width W of the channel formed at the lower part of the gate 60 is formed with the same width as that of the source 70 and the drain 80.” Thus, as can be visualized from Yun’s Fig. 1 below, the source and drain regions are formed on either side of the gate electrode and would extend below the upper surface to form a conducting channel for the transistor drive current.



99. I note also that a POSITA, reading Yun, would recognize that conventional source and drain regions are formed in the active area over the substrate. For example, Fig. 1 of the '122 patent shows an “illustrative *prior art transistor* in the transistor length direction” (Ex. 1001, 3:9-10); as shown in the annotated figure below, active area 12 includes source/drain regions 28, as indicated by the red dashed lines.



3. Yun Renders Obvious Claim 24

100. Claim 24 depends from claim 23. As I explained above, Yun teaches the subject matter of claim 23.

101. As I will explain below, in my opinion, Yun teaches the additional subject matter of claim 24.

a. “The transistor of claim 23, wherein said semiconducting substrate is comprised of silicon.”

102. The additional subject matter of claim 24 is identical to claim 2. As I explained above, Yun teaches the subject matter of claim 2. Thus, Yun teaches the subject matter of claim 24.

4. Yun Renders Obvious Claim 25

103. Claim 25 depends from claim 23. As I explained above, Yun teaches the subject matter of claim 23.

104. As I will explain below, in my opinion, Yun teaches the additional subject matter of claim 25.

- a. “The transistor of claim 23, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.”**

105. The additional subject matter of claim 25 is identical to claim 3. As I explained above, Yun teaches the subject matter of claim 3. Thus, Yun teaches the subject matter of claim 25.

5. Yun Renders Obvious Claim 33

106. Claim 33 depends from claim 23. As I explained above, Yun teaches the subject matter of claim 23.

107. As I will explain below, in my opinion, Yun teaches the additional subject matter of claim 33.

- a. “The transistor of claim 23, wherein said gate electrode has first and second end portions that extend into a recess in said substrate defined by said recessed isolation structure.”**

108. The additional subject matter of claim 33 is identical to claim 11. As I explained above, Yun teaches the subject matter of claim 11. Thus, Yun teaches the subject matter of claim 33.

6. Yun Renders Obvious Claim 34

109. Claim 34 depends from claim 33. As I explained above, Yun teaches the subject matter of claim 33.

110. As I will explain below, in my opinion, Yun teaches the additional subject matter of claim 34.

- a. “The transistor of claim 33, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.”**

111. The additional subject matter of claim 34 is identical to claim 12. As I explained above, Yun teaches the subject matter of claim 12. Thus, Yun teaches the subject matter of claim 34.

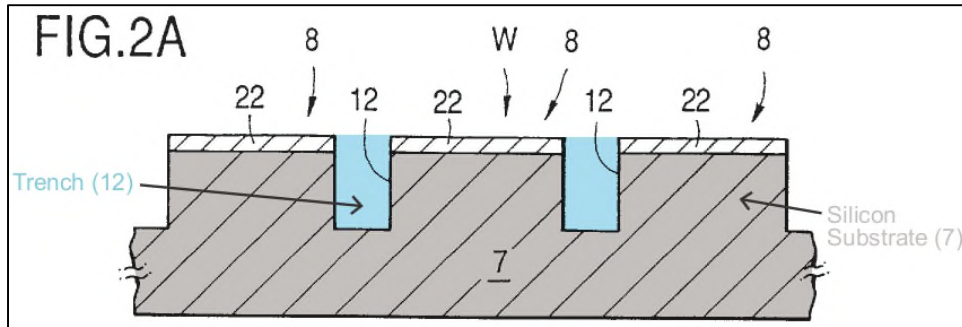
D. Ground 3. Claims 5 and 27 Are Obvious Over Yun and Wada

1. Overview of Wada

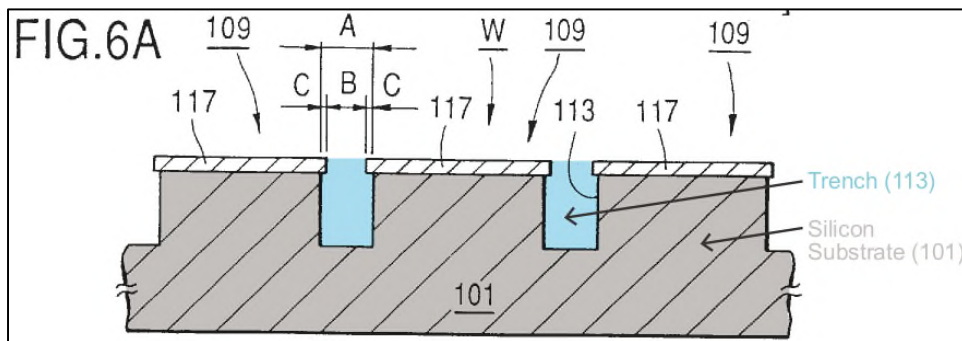
112. Wada relates to semiconductor devices and focuses on techniques for isolating transistors. Ex. 1004 (Wada), 1:8-12. Specifically, Wada improves upon conventional methods of “field-shield device isolation” (FSDI), which includes forming an isolation structure in between two active regions of an integrated circuit to isolate the two devices from each other. Ex. 1004 (Wada), 1:29-38. Wada achieves this by forming the isolation structure in a “trench cavity” having dimensions tailored to the device parameters (e.g., the depth of the trench relates to properties of the source/drain diffusion layers), thereby “substantially” increasing

the “effective isolation dimension.” Ex. 1004 (Wada), 2:1-27. And, because “the area required for the device isolation structure is only that area required for the width of the trench cavity,” Wada explains that “a higher degree of integration density can be achieved in a given area of a substrate.” Ex. 1004 (Wada), 2:28-35. As a result, Wada’s invention enables “the high degree of integration density required for modern semiconductor devices” and provides a simplified method of fabricating isolation structures. Ex. 1004 (Wada), 3:22-32.

113. Wada’s Figs. 2A-2G and 6A-6G illustrate the successive steps of making the contemplated semiconductor device. As relevant here, Fig. 2A, reproduced below, shows the cavities for trenches 12 that are fabricated on silicon substrate 7. Ex. 1004 (Wada), 4:42-49. Specifically, the cavities are formed by “etching through an etching mask of a SiO₂ film 22, for protecting those active regions 8 for fabricating the N-channel MOS transistor but exposing those regions for forming the trenches 12.” Ex. 1004 (Wada), 4:42-49. And Wada further explains: “The process of forming the trenches 12 used in this embodiment is a dry etching process using gaseous chlorine to make a cavity measuring 0.5~1.5 μm [5000 to 15000 Å] in depth and 0.2~0.5 μm [2000 to 5000 Å] in width.” Ex. 1004 (Wada), 4:49-52.



114. Wada's Fig. 6A shows a similar structure in connection with another embodiment in which substrate 101 includes trenches 113:



See Ex. 1004 (Wada), 9:59 – 10:9.

115. Wada discusses the insulator film thickness and the trench size. Wada notes with respect to the trench dimensions that:

The dimensions quoted in the embodiments are meant to be examples, and they are not limited to the exact dimensions quoted.

For example, it is permissible to have a range of dimensions such as:

the trench widths may range from 80 nm~several mm; the depth of the trench may be made deeper by up to 10 μm than the depth of the diffusion layers for source and drain

Ex. 1004 (Wada), 7:54-62 and 13:64 – 14:6.

2. Yun and Wada Render Obvious Claims 5 and 27

116. Claims 5 and 27 respectively depend from claims 1 and 23. I note that claims 5 and 27 are otherwise identical. As I explained above, Yun teaches the subject matter of claims 1 and 23.

117. As I will explain below, in my opinion, the combination of Yun and Wada teaches and renders obvious the additional subject matter of claims 5 and 27.

- a. **[Claim 5] “The transistor of claim 1, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å” and [Claim 27] “The transistor of claim 23 ...”**

118. Wada teaches forming trenches 12 having a width ranging from 2000 to 5000 Å and a depth ranging from 5000 to 15000 Å. Ex. 1004 (Wada), 4:41-51. Further, Wada notes that “[t]he dimensions quoted in the embodiments are meant to be examples, and they are not limited to the exact dimensions quoted.” Ex. 1004 (Wada), 7:54-62 and 13:64 – 14:6. A POSITA reading Wada would appreciate, for example, that the depth of trenches 12 could be less than 5000 Å.

119. Thus, in my opinion, Wada teaches the subject matter of claims 5 and 27.

3. It Would Have Been Obvious to Combine the Teachings of Yun and Wada

120. In my opinion, as of the '122 patent's filing date, a POSITA would have found it obvious to form the depth and width of Yun's recessed isolation structures to the thickness ranges as taught by Wada.

121. One of ordinary skill would also have a reasonable expectation that this combination would succeed and result in a semiconductor device falling within the scope of claims 5 and 27.

122. I note that Yun and Wada both focus on improvements to techniques for isolating active devices and transistors on the same substrate. It was well recognized in the art that isolating transistors on the same substrate from one another, particularly as transistors continued to shrink in size, was critical to transistor and overall device operation. *See, e.g., A. Chatterjee et al., A Shallow Trench Isolation Study for 0.25/0.18 μm CMOS Technologies and Beyond, Symposium on VLSI Technology Digest of Technical Papers, pp. 156-57 (1996)* (discussing the importance of isolating active devices and the application of STI techniques) (Ex. 1015). Further, it was desirable to attain a higher degree of integration, smaller transistor sizes, and minimize overall integrated circuit area, in order to, for example, reduce cost and complexity when manufacturing semiconductor devices at large scale. *See, e.g., Ex. 1004 (Wada), Abstract; see also Ex. 1008 (Tao), 2:8-16 and 2:40-65* (describing an improved etching process

that achieves reduced operating costs and processing time); Ex. 1007 (Rubin), 4:23-28 (providing, in the context of semiconductor fabrication, “an alternative to the more complex procedures and more expensive equipment required for low-energy implants. The invention does not require any special equipment . . .”).

123. Wada, for example, improves upon prior art isolation structures in order to enable “a higher degree of integration of circuits in the semiconductor device.” Ex. 1004 (Wada), 1:63-67. It achieves this by providing a trench having sufficient depth, reducing the surface area for the isolation structure relative to prior art structures, and simplifying the processing required to form the isolation structure. Ex. 1004 (Wada), 5:63 – 6:33. Therefore, in my opinion, a POSITA reading Yun would have been motivated to combine the teachings of Wada and Yun to achieve a greater degree of isolation, thereby avoiding any adverse effects on transistor performance caused by insufficient isolation such as current leakage, while also increasing drive current without increasing the integrated circuit area.

124. Further, in the context of describing an improved isolation technique, Wada teaches forming the trench to a depth of approximately 5000 to 15000 Å and a width of approximately 2000 to 5000 Å. Ex. 1004 (Wada), 4:41-51. It is also my opinion that a POSITA reading Yun would be able to select appropriate parameters for the trench (such as the depth and width) based on the device design and any relevant constraints. Yun teaches, for example, “adjusting the depth” of

the oxide film inside the trench: oxide film 21a “is etched by 10nm [100 Å] – 200nm [2000 Å] by means of a wet etching process.” Ex. 1003 (Yun), 2-5. Thus, in my opinion, a POSITA would have been motivated to form Yun’s recessed isolation structures to the thickness ranges as taught by Wada to improve transistor isolation, better protect against potential leakage issues, and increase overall device functioning.

125. I also note that Yun and Wada share a common aim of simplifying transistor design and manufacturing process without increasing the integrated circuit area. For example, Wada explains that its improved isolation structure “not only achieves a *higher density of integration of active devices in a given space of the substrate* but also *simplifies the design of interconnection lines*, thereby suggesting a path to production of very large integrated circuits economically in the future.” Ex. 1004 (Wada), Abstract. In a similar vein, Yun states: “It is yet another object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can increase the channel width and, at the same time, *decrease the number of processes while forming an isolation region.*” Ex. 1003 (Yun), 2-5.

126. It is my further opinion that a POSITA would have every reason to believe that applying Wada’s teachings to the semiconductor device of Yun would succeed. As I explained above, Yun and Wada are in the same field of

semiconductor processing and fabrication. Thus, in my opinion, the overlap and similarity in subject matter between Yun and Wada would lead a POSITA to believe that forming a trench isolation structure based on the width and depth ranges as taught by Wada could be successfully applied to Yun's semiconductor device.

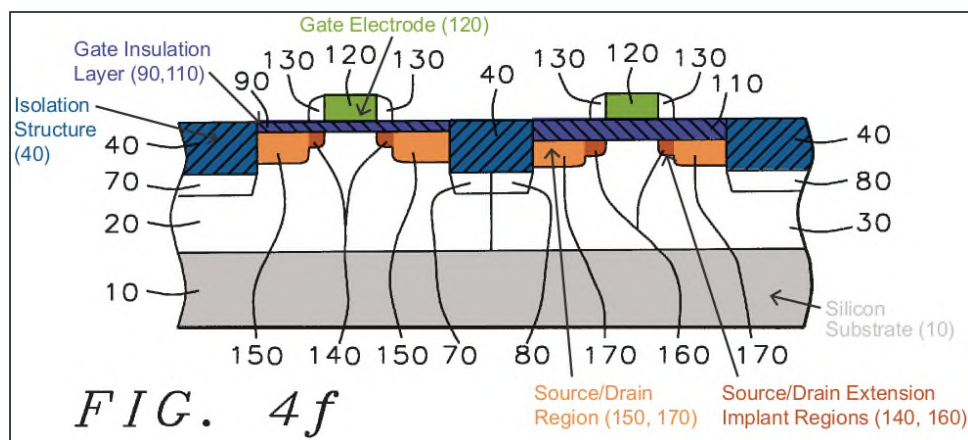
E. Ground 4. Claims 6-10, 13-14, 17-22 and 28-32 Are Obvious Over Yun and Lu

1. Overview of Lu

127. Lu relates to semiconductor “fabrication processes that will enhance performance,” particularly in the context of dynamic random access memory (“**DRAM**”) applications. Ex. 1005 (Lu), 1:6-10. To improve transistor performance and reliability, Lu discloses, among other things, forming transistors having either a “thinner” or “thicker” gate insulation layer. Ex. 1005 (Lu), 2:33-41. Specifically, Lu teaches forming: (i) a “thinner gate oxide in circuits having a lower voltage” to improve performance, due to the reduced threshold voltage (V_{TH}) and resulting faster switching time, and (ii) a “thicker gate oxide” in circuits subject to a higher voltage to improve reliability. Ex. 1005 (Lu), 2:33-41; *see also* 3:1-26 (discussing various circuit elements and identifying whether they should be formed using “thinner” or “thicker” gate oxides). In this regard, Lu further notes that “[t]he embedded DRAM will have MOS transistors with a thicker gate oxide while the separate logic circuits will have MOS transistors with a thinner gate

oxide. The performance of the embedded DRAM will have the same performance issues as described above, since the peripheral circuits of the embedded DRAM will have the thicker gate oxide.” Ex. 1005 (Lu), 1:53-59.

128. Fig. 4f, annotated below, shows the elements of a transistor formed in accordance with Lu’s invention. The transistor includes polysilicon gate 120 (Ex. 1005 (Lu), 7:8-13), “thinner” gate oxide 90 and “thicker” gate oxide 110 (7:2-7), and source/drain extension implant regions 140/160 within the source/drain regions 150/170 (7:14-21). Further, trench 40 isolates transistors on the substrate. Ex. 1005 (Lu), 6:54-63.



129. Lu discloses that the “thinner” gate oxide 90 has a thickness of 30 to 60 Å, the “thicker” gate oxide 110 has a thickness of 50 to 80 Å, and the polysilicon gate electrode 120 has a thickness of 0.1 to 0.4 μm, which is equivalent to 1000 to 4000 Å. Ex. 1005 (Lu), 7:2-13. With respect to the gate oxide thickness, Lu further explains that:

The *thinner gate oxide will provide approximately a 20% improvement in performance parameters* such as delay over the equivalent circuits fabricated using the thicker gate oxide. *Placing the thicker gate oxide selectively* in areas of the DRAM having higher voltages present on the MOS transistors *will insure [sic] that the MOS transistors meet their reliability requirements.*

Ex. 1005 (Lu), 7:59-65.

2. Yun and Lu Render Obvious Claims 13, 14, 21 and 22

130. I note that independent claim 13 differs from independent claim 1 in two respects only: (1) claim 13 recites a semiconducting substrate “comprised of silicon,” and (2) claim 13 recites a gate electrode “comprised of polysilicon.” Yun teaches the subject matter of claim 1 for the reasons discussed previously. As I will explain below, in my opinion, the combination of Yun and Lu teaches and renders obvious the additional subject matter of claim 13.

131. Dependent claims 14, 21 and 22, which depend from claim 13, are identical to dependent claims 3, 11 and 12. Yun teaches the subject matter of claims 3, 11 and 12 for the reasons discussed previously.

132. Yun teaches a silicon substrate, as required by claim 13.

133. With respect to a polysilicon gate electrode, in my opinion, a POSITA would have found it obvious to form Yun’s gate electrode from polysilicon. It has

long been common practice in the art to form a gate electrode using layers of polysilicon, including during the time of Yun and the '122 patent. *See, e.g., A. C. Ipri, Sub-Micron Polysilicon Gate CMOS/SOS Technology*, 1978 International Electron Devices Meeting, pp. 46-49 (1978) (discussing the use and benefits of polysilicon gate electrodes in submicron devices in the context of smaller device feature sizes) (Ex. 1016). Further, in describing prior art transistors, the '122 patent notes that “the gate electrode 20 may be comprised of polysilicon.” Ex. 1001, 1:50-52.

134. Further, I note that Lu teaches the use of a polysilicon gate electrode, as discussed in detail in Section VIII.E.3 below.

135. Thus, in my opinion, the combination of Yun and Lu teaches and renders obvious the subject matter of claims 13, 14, 21 and 22.

3. Yun and Lu Render Obvious Claims 6 and 28

136. Claims 6 and 28 respectively depend from claims 1 and 23. I note that claims 6 and 28 are otherwise identical. As I explained above, Yun teaches the subject matter of claims 1 and 23.

137. As I will explain below, in my opinion, the combination of Yun and Lu teaches and renders obvious the additional subject matter of claims 6 and 28.

- a. **[Claim 6] “The transistor of claim 1, wherein said gate electrode is comprised of polysilicon” and [Claim 28] “The transistor of claim 23 . . .”**

138. Lu teaches forming a polysilicon gate electrode. Specifically, Lu notes that: “After the dual gate oxide 90 and 110 is grown, *the polysilicon gate layer is deposited and gate 120 is formed* for both NMOS and PMOS by the photolithographic process, as shown in FIG. 4e.” Ex. 1005 (Lu), 7:8-12. Thus, in my opinion, Lu teaches the claimed subject matter.

4. Yun and Lu Render Obvious Claims 7, 17 and 29

139. Claims 7, 17 and 29 respectively depend from claims 1, 13 and 23. I note that claims 7, 17 and 29 are otherwise identical. As I explained above, Yun teaches the subject matter of claims 1 and 23, and the combination of Yun and Lu teaches the subject matter of claim 13.

140. As I will explain below, in my opinion, the combination of Yun and Lu teaches and renders obvious the additional subject matter of claims 7, 17 and 29.

- a. **[Claim 7] “The transistor of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride” and [Claim 29] “The transistor of claim 23 . . .”**

141. Yun teaches a gate insulation layer formed of an oxide film (see gate oxide 41). As discussed in detail in Section VIII.C.1 above, an oxide film, in the field of semiconductor fabrication, includes the class of silicon dioxide (SiO₂)

insulators, one of the most common insulators used in the art. Further, in my opinion, a POSITA reading Yun would understand Yun's oxide film as being silicon dioxide when considering that Yun uses a *silicon* substrate.

142. Further, Lu discloses forming the gate insulation layer from at least one of silicon dioxide and silicon oxynitride. Lu specifically notes that the "gate oxide is formed of silicon oxide, silicon nitride, or silicon oxynitride" Ex. 1005 (Lu), 3:39-41. Thus, in my opinion, Lu teaches the claimed subject matter.

5. Yun and Lu Render Obvious Claims 8, 18 and 30

143. Claims 8, 18 and 30 respectively depend from claims 1, 13 and 23. I note that claims 8, 18 and 30 are otherwise identical. As I explained above, Yun teaches the subject matter of claims 1 and 23, and the combination of Yun and Lu teaches the subject matter of claim 13.

144. As I will explain below, in my opinion, the combination of Yun and Lu teaches and renders obvious the additional subject matter of claims 8, 18 and 30.

- a. **[Claim 8] "The transistor of claim 1, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å"; [Claim 18] "The transistor of claim 13 . . ."; and [Claim 30] "The transistor of claim 23 . . ."**

145. Lu teaches that "[t]he thickness of polysilicon gate 120 is from 0.1 [1000 Å] to 0.4 μm [4000 Å] and its deposition temperature is from 550° C. to

750° C.” Ex. 1005 (Lu), 7:11-13. Thus, in my opinion, Lu teaches forming a gate electrode having a thickness that falls within the claimed range.

6. Yun and Lu Render Obvious Claims 9, 19 and 31

146. Claims 9, 19 and 31 respectively depend from claims 1, 13 and 23. I note that claims 9, 19 and 31 are otherwise identical. As I explained above, Yun teaches the subject matter of claims 1 and 23, and the combination of Yun and Lu teaches the subject matter of claim 13.

147. As I will explain below, in my opinion, the combination of Yun and Lu teaches and renders obvious the additional subject matter of claims 9, 19 and 31.

- a. **[Claim 9] “The transistor of claim 1, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.”; [Claim 19] “The transistor of claim 13 . . .”; and [Claim 31] “The transistor of claim 23 . . .”**

148. Lu teaches forming “thinner” and “thicker” gate oxides. As Lu explains: “*The thickness of thinner gate oxide is from 30 to 60 Ångstroms (preferably 45 Ångstroms)* and is grown temperature is from 750 to 1000° C.” Ex. 1005 (Lu), 7:2-6. Thus, in my opinion, Lu teaches forming a gate insulation layer having a thickness that falls within the claimed range.

7. Yun and Lu Render Obvious Claims 10, 20 and 32

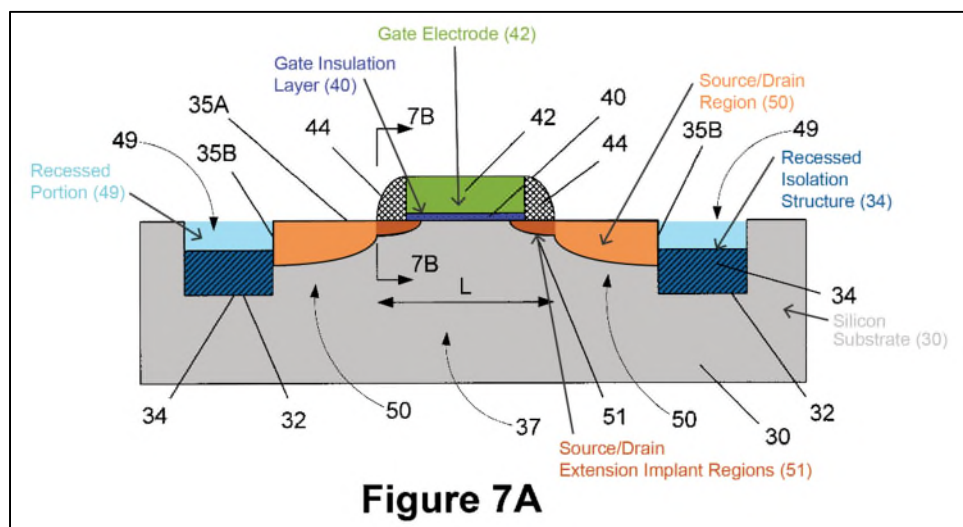
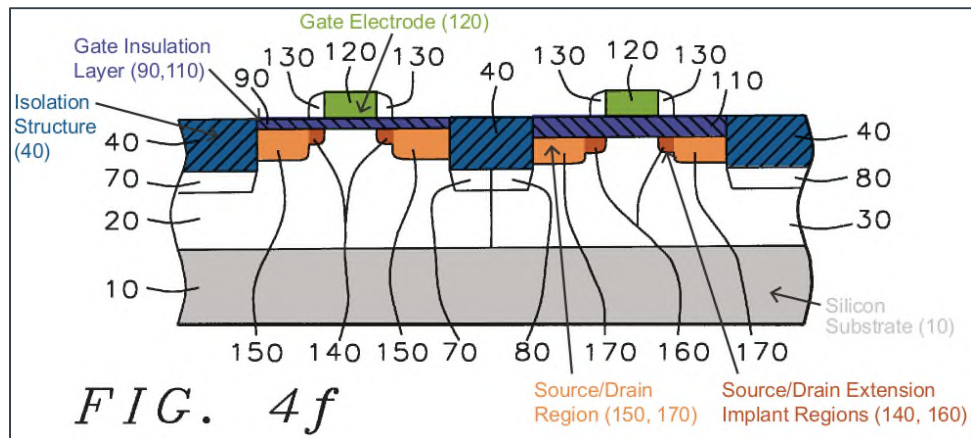
149. Claims 10, 20 and 32 respectively depend from claims 1, 13 and 23. I note that claims 10, 20 and 32 are otherwise identical. As I explained above, Yun

teaches the subject matter of claims 1 and 23, and the combination of Yun and Lu teaches the subject matter of claim 13.

150. As I will explain below, in my opinion, the combination of Yun and Lu teaches and renders obvious the additional subject matter of claims 10, 20 and 32.

- a. **[Claim 10] “The transistor of claim 1, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region” and [32] “The transistor of claim 23 . . .”**

151. Lu teaches forming source/drain extension regions 140 and 160, and source/drain regions 150 and 170, as illustrated below in the annotated figure. Ex. 1005 (Lu), 7:14-21. I note that, like the ’122 patent, Lu teaches implanting boron into the source/drain regions of PMOS transistors, and arsenic into the source/drain regions of NMOS transistors. Ex. 1005 (Lu), 7:22-36; *compare* ’122 patent, 6:1-6. Further, the structure of Lu’s source/drain extension regions 140 and 160, and source/drain regions 150 and 170 mirrors the structure disclosed in the ’122 patent, as illustrated below. Thus, in my opinion, Lu teaches the claimed subject matter.



8. It Would Have Been Obvious to Combine the Teachings of Yun and Lu

152. In my opinion, as of the '122 patent's filing date, a POSITA would have found it obvious combine the teachings of Yun and Lu, as I discuss below. Specifically, a POSITA would have been motivated to: (i) form Yun's *gate electrode* from polysilicon (as described in claims 6, 13, 14, 21, 22 and 28) and to the thickness taught in Lu (as described in claims 8, 18 and 30); (ii) form Yun's *gate insulation layer* from silicon dioxide or silicon oxynitride (as described in claims 7, 17 and 29) and to the thickness taught in Lu (as described in claims 9, 19

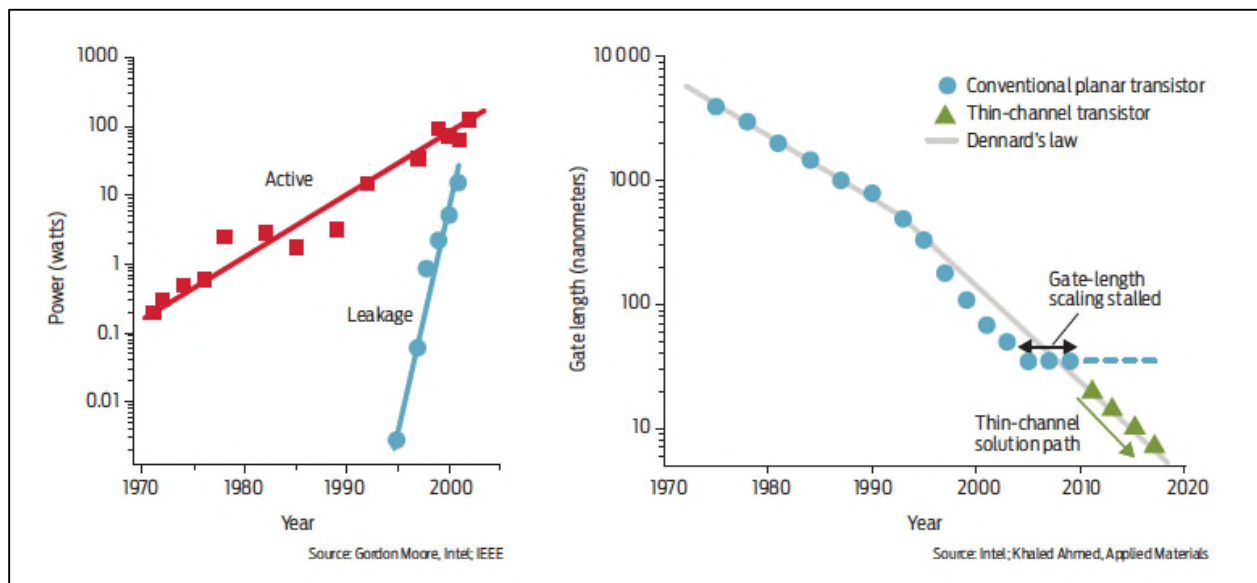
and 31); and (iii) form, in Yun's transistor, *source/drain extension implant regions* as taught in Lu (as described in claims 10, 20 and 32).

153. One of ordinary skill would also have a reasonable expectation that these combinations would succeed and result in a semiconductor device falling within the scope of claims 6-10, 13-14, 17-22 and 28-32.

154. I note that Yun and Lu both focus on improving upon prior art processes related to semiconductor fabrication and enhancing transistor performance. Yun teaches methods for increasing transistor drive current without increasing integrated circuit area, by extending the gate electrode and gate insulation layer into the recessed portion of an isolation structure. Lu, similarly, focuses on improving MOS transistor performance in connection with DRAM (memory) applications; Lu specifically describes forming "thinner" or "thicker" gate insulation layers depending on the voltage requirements of the associated DRAM circuitry.

155. The continued trend of shrinking transistor size and thinner transistor elements (e.g., gate electrode and gate oxide) was generally recognized well before the '122 patent's filing date. *See, e.g.*, Ex. 1008 (Tao), 1:53-60 ("As the industry move[d] towards higher density applications, the gate oxides used for the active devices of a semiconductor have tended to become thinner"). This trend, however, presented new technical challenges. *See, e.g.*, Ex. 1008 (Tao), 1:53-60 (noting that

thinner gate oxides, in turn, require “highly selective” etching techniques and etchants). By the time of the ’122 patent’s filing in 2001, transistor gate length had decreased to less than 100 nm, while off-state leakage current had become increasingly problematic. K. Ahmed et al., *Transistor Wars*, IEEE Spectrum, Vol. 48, No. 11, pp. 50-66 (2011) (Ex. 1017). Specifically, the thinner gate electrode and gate oxide layers resulted in greater current leakage, made transistor fabrication more difficult, and caused reliability issues with process control. This is illustrated by the figure below, which shows that in the late 1990s and early 2000s, current leakage increased dramatically as device sizes became smaller (approaching a gate length of 30-50 nm) and oxide layers became thinner.



Ex. 1017. Refer also to Exhibit 1019 for an additional example from the technical literature that discusses the issue of leakage current in the context of decreasing transistor device sizes in the 2001 timeframe, when the ’122 patent was filed. *See*,

e.g., W. K. Henson et al., *Analysis of Leakage Currents and Impact on Off-State Power Consumption for CMOS Technology in the 100-nm Regime*, IEEE Transactions on Electron Devices, Vol. 47, No. 7, pp. 1393-1400 (2000) (Ex. 1019).

156. A POSITA reading Yun would have understood Yun's desire to improve semiconductor fabrication techniques to account for devices with smaller feature sizes. For example, Yun notes:

It is the object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can *improve the electric current driving capability of a transistor by increasing the channel width without increasing the chip area by vertically forming a part of the channel region.*

Ex. 1003 (Yun), 2-5.

157. Further, with respect to the gate electrode and gate oxide, a POSITA would have appreciated the importance of fabricating devices in a way that achieves reliable and improved transistor performance. For example, as Lu notes:

An object of this invention is to provide a DRAM device having improved performance of peripheral circuitry by having MOS transistors with a thinner gate oxide in circuits having a lower voltage.

Another object of this invention is to provide a DRAM device having

improved reliability by having the memory cells and selected peripheral subcircuitry subjected to a higher voltage having thicker gate oxide.

Ex. 1005 (Lu), 2:34-41 and 4:47-52. Thus, in my opinion, a POSITA would have been motivated to apply Lu's process to Yun's "conventional" process of forming the gate electrode and gate oxide to achieve improved transistor performance and reliability.

158. In my opinion, a POSITA would have also recognized that Lu's technique of using lightly-doped drains ("**LDD**") would have increased the performance of the transistor taught by Yun. For example, Lu's LDD technique addresses the well-known "hot-carrier effect," in which carriers (electrons and holes) are injected inadvertently into certain areas of the device (e.g., the gate oxide), resulting in device degradation and decreased transistor performance. *See, e.g., S. Aur et al., Circuit Hot Electron Effect Simulation*, International Electron Devices Meeting, pp. 498-501 (1987) (discussing the impacts of the "hot-carrier effect" in terms of leakage current, effects on threshold voltage, and degradation of integrated circuit performance) (Ex. 1018). To reduce the "hot-carrier effect," each source and each drain can include a lightly-doped extension (LDD region) that separates a respective heavily doped "deep" source/drain region from the channel;

the channel then separates the source extension from the drain extension. *See, e.g.*, Ex. 1007 (Rubin), 1:32-40 (discussing same).

159. Thus, a POSITA would have been motivated to use Lu's LDD technique to form source/drain extension implant regions within Yun's source/drain regions, because doing so would: (1) separate the heavily-doped source/drain regions from the conducting channel, (2) thereby diminishing the hot-carrier effect, and (3) as a result, minimize off-state current leakage. Put another way, forming source/drain extension implant regions would extend the transistor active area and width (W) and thereby increase the drive current, an express aim of Yun. Ex. 1003 (Yun), 2-5 ("It is the object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can improve the electric current driving capability of a transistor by increasing the channel width without increasing the chip area . . .").

160. It is my further opinion that a POSITA would have every reason to believe that applying Lu's teachings to the semiconductor device of Yun would succeed. As I explained above, Yun and Lu are in the same field of semiconductor processing and fabrication. And both focus on improving semiconductor fabrication methods to realize increased transistor performance. Thus, in my opinion, the overlap and similarity in subject matter between Yun and Lu would lead a POSITA to believe that forming the gate electrode, gate insulation layer, and

source/drain extension implant regions in the manner taught by Lu could be successfully applied to Yun.

F. Ground 5. Claim 16 Is Obvious Over Yun in view of Wada and Lu

1. Claim 16

161. Claim 16 depends from claim 13. As I noted above, claim 1 and claim 13 differ in two minor respects only: (1) claim 13 requires a *silicon* substrate (which Yun teaches), and (2) claim 13 requires a *polysilicon* gate electrode (which Lu teaches). As I explained above, Yun and Lu teaches the subject matter of claim 13.

162. I note also that claim 16 is identical to dependent claims 5 and 27 (which depend from independent claims 1 and 23, respectively). As discussed previously, the combination of Yun and Wada teaches the subject matter of claims 5 and 27.

163. Further, a POSITA would have found it obvious to combine the teachings of Yun, Wada and Lu for the reasons provided above in Sections VIII.D.3 and VIII.E.8. In particular, I note that Yun, Wada and Lu are in the same field of semiconductor processing and fabrication, and each focuses on improving prior art fabrication methods that result in increased transistor performance. In view of the overlap and similarity in subject matter between Yun, Wada and Lu, a POSITA would believe that forming the gate electrode from polysilicon (as taught

by Lu) and a trench isolation structure based on the width and depth ranges as taught by Wada could be successfully applied to Yun's semiconductor device.

164. Thus, in my opinion, the combination of Yun, Wada and Lu teaches the subject matter of claim 16.

IX. INVALIDITY ANALYSIS BASED ON SAKI

165. Saki indicates on its face that it published on Sept. 28, 1999. In view of this date of publication, I understand that Yun is prior art pursuant to 35 U.S.C. § 102(b).

166. I note that Saki was neither cited nor discussed by the Examiner during prosecution.

A. Overview of Saki

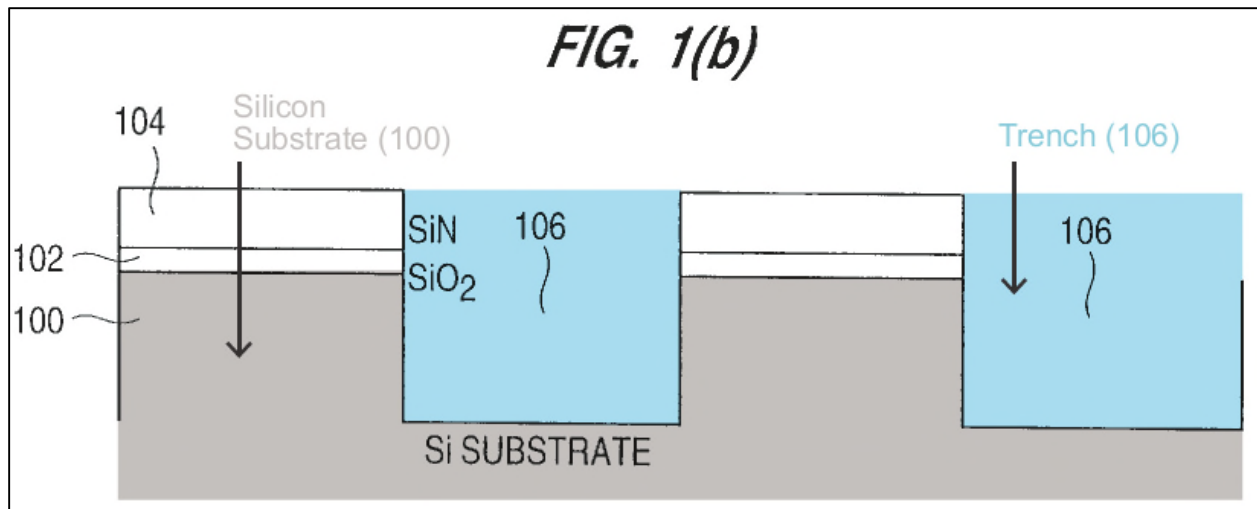
167. Saki relates to semiconductor devices and, like the '122 patent, is specifically directed to "an isolation structure for such devices and the methods for forming the isolation structure." Ex. 1006 (Saki), 1:8-12. As Saki explains:

An integrated circuit may be formed by connecting together various elements such as transistors which are formed on a semiconductor substrate. *To ensure proper functioning of the integrated circuit, these elements must be electrically isolated from each other.* Such isolation can be achieved using local oxidation of silicon (LOCOS) or shallow trench isolation (STI). *Shallow trench isolation is*

particularly advantageous for circuits having a high integration density since shallow trench isolation can provide for a relatively planar surface on which subsequent insulating and/or conducting layers may be formed.

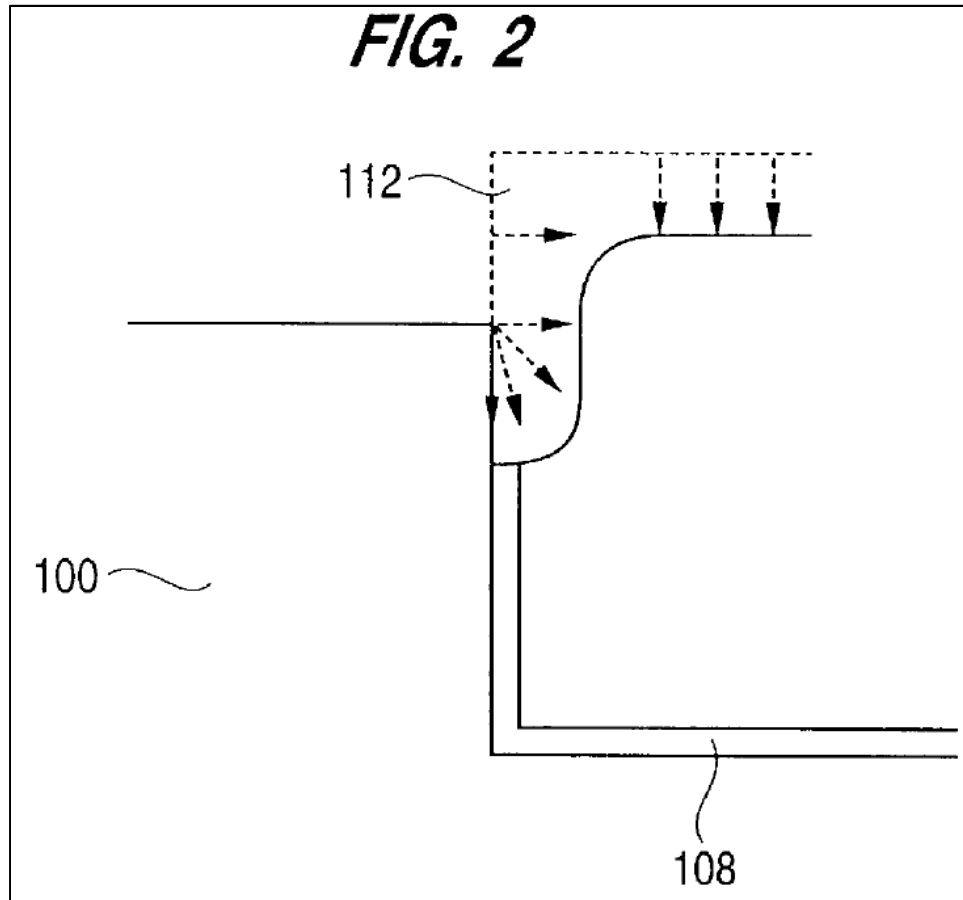
Ex. 1006 (Saki), 1:14-24.

168. Saki's Figs. 1(a)-1(f) illustrate a "conventional process" for forming an STI structure; Fig. 1(b), reproduced below, shows trenches 106 formed in silicon substrate 100.

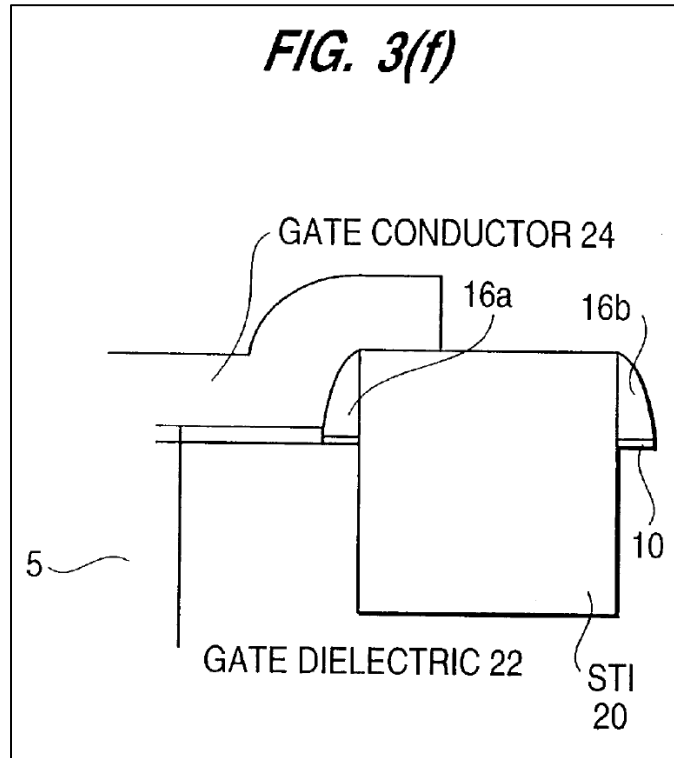


169. Saki observes that prior art etching processes could result in silicon dioxide being removed (etched away) from the corners of an STI structure, as illustrated in Fig. 2 below. Ex. 1006 (Saki), 1:43-59. This may "result in a lowering of the threshold voltage of a transistor formed in the active area defined

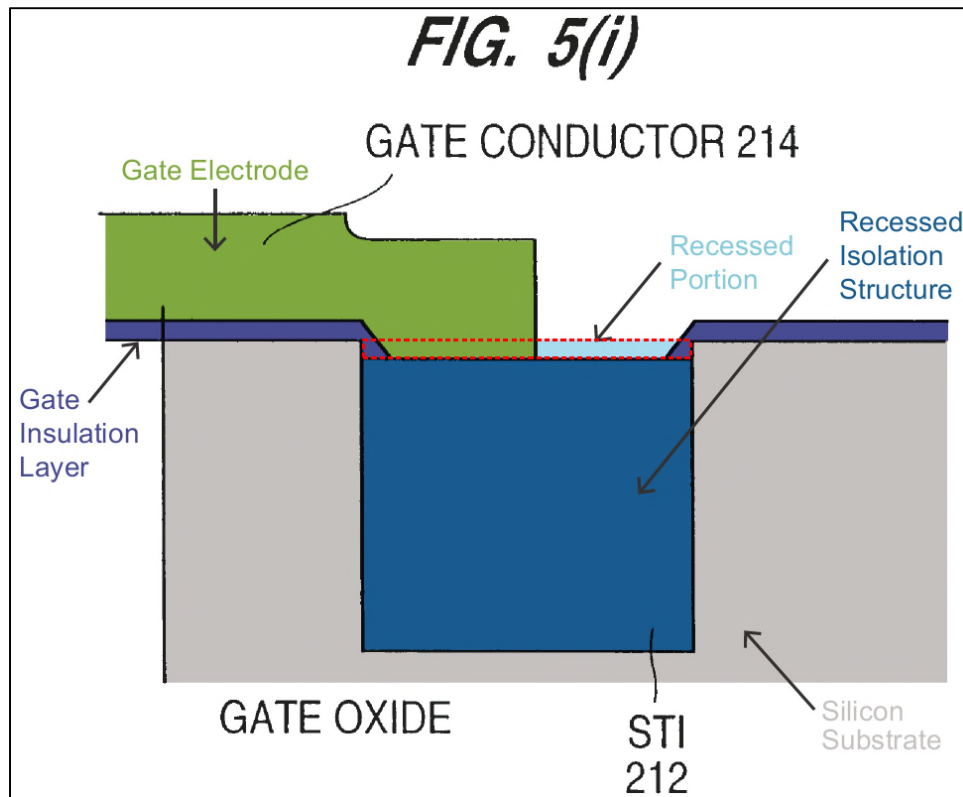
by the shallow trench isolation structure,” which ultimately affects transistor performance. Ex. 1006 (Saki), 1:54-59.



170. Saki also recognized that prior art processes could lead to formation of a “step” on the gate electrode caused by the difference in level between the surface of the silicon substrate and the insulator, as illustrated in Saki’s Fig. 3(f), below. Ex. 1006 (Saki), 2:42-47. As Saki explains, “[t]his can lead to difficulties in the patterning of the gate conductor 24,” especially in important applications such as DRAM. Ex. 1006 (Saki), 2:47-50.



171. Saki's invention improves upon conventional STI in several ways, including by providing "enhanced controllability of the shape of the shallow trench isolation structure." Ex. 1006 (Saki), 3:14-21. Saki's invention is illustrated in Figs. 5(a)-5(i). Specifically, a benefit of Saki's method is suppressing "etching of the insulator at the corner of the shallow trench isolation structure." Ex. 1006 (Saki), 4:61 – 5:7. Further, as illustrated in Fig. 5(i) below, the gate conductor and gate insulating layer (oxide) extend into the recess formed by the trench, thereby avoiding the problems of the prior art "step." Ex. 1006 (Saki), 5:18-27.



B. Ground 6. Claims 1-3, 6, 11-14, 21-25, 28 and 33-34 Are Obvious Over Saki In Light of the Knowledge of a POSITA

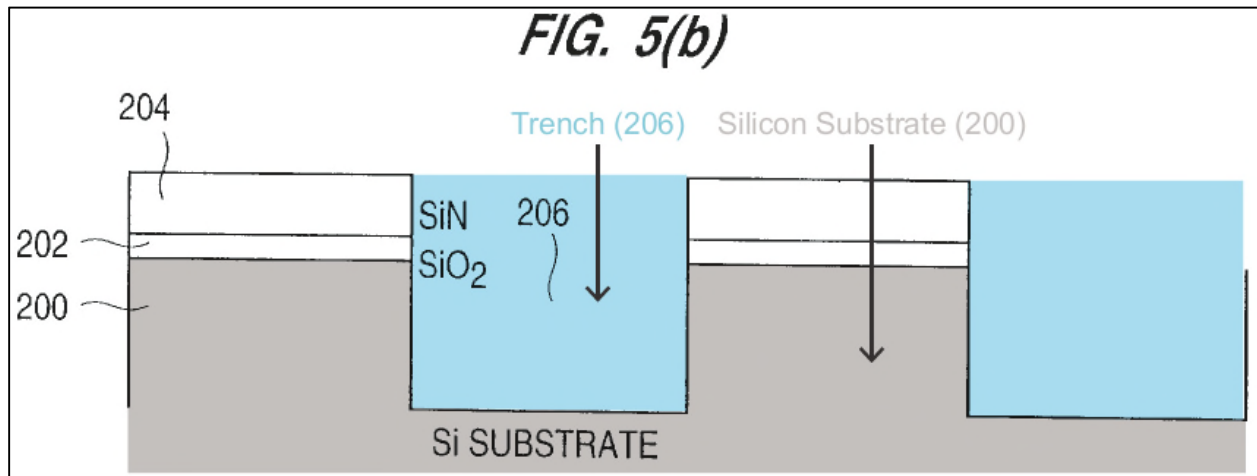
1. Saki Renders Obvious Claims 1 and 13

a. [1.P] and [13.P] “A transistor, comprising:”

172. Saki relates to “semiconductor devices such as semiconductor memory devices,” which are made up of transistors. Ex. 1006 (Saki), 1:8-16. Saki specifically relates to isolation structures that are formed in between transistors on a common substrate. Ex. 1006 (Saki), 1:14-24.

- b. [1.1] “a semiconducting substrate;” and [13.1] “a semiconducting substrate comprised of silicon;”

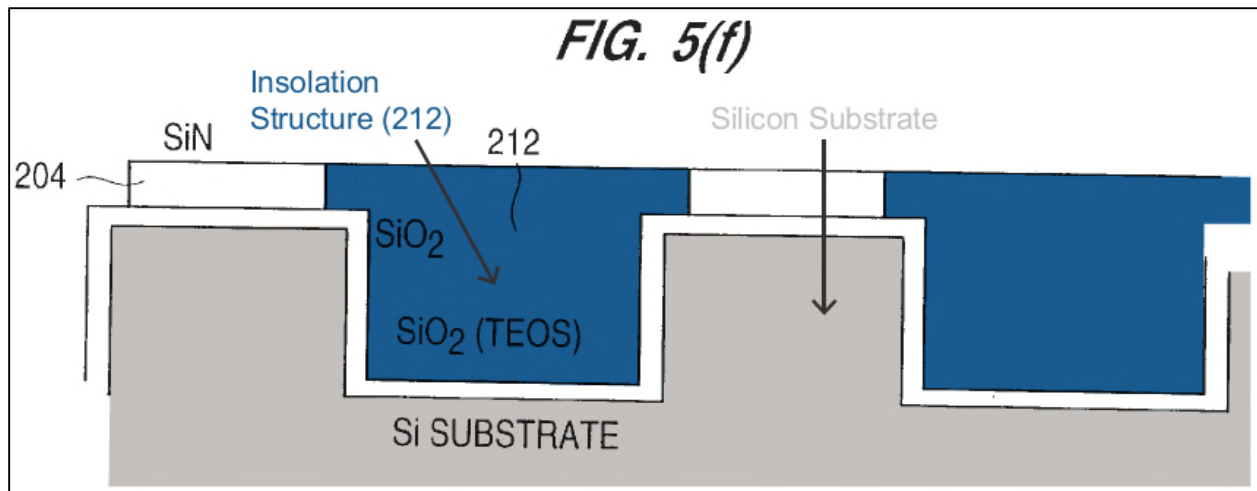
173. Saki discloses forming transistors, and isolation structures between them, on silicon substrate 200. Fig. 5(b); *see also* Ex. 1006 (Saki), 1:13-17 and 3:65 – 4:28.



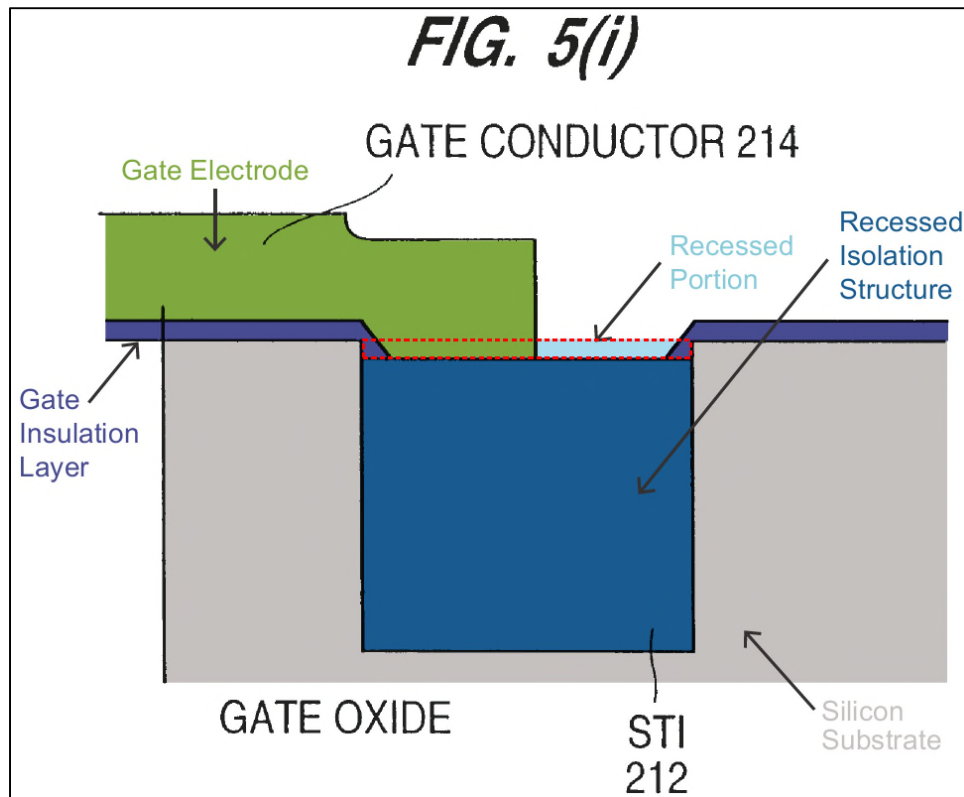
- c. [1.2] and [13.2] “a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove;”

174. Saki teaches forming a recessed isolation structure as discussed below in connection with Figs. 5(f) through 5(i).

175. First, a layer of silicon dioxide 212, an insulator, is deposited in the trench and planarized, as shown in Fig. 5(f). Ex. 1006 (Saki), 4:51-59.



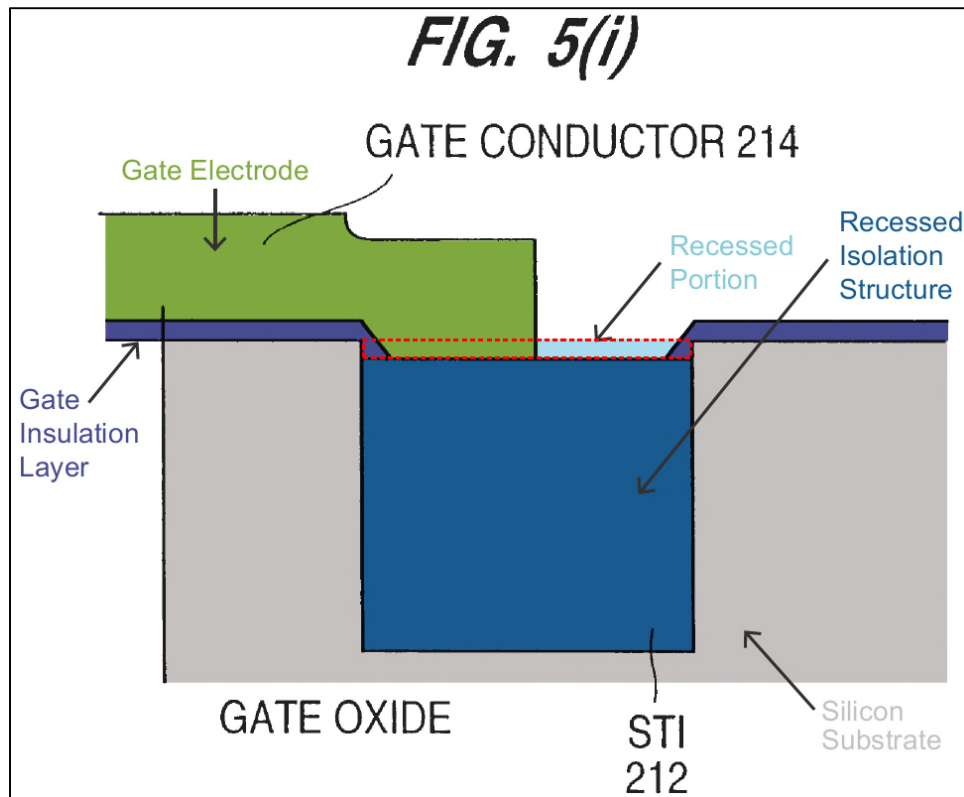
176. A series of etching processes are then carried out to remove portions of the pad silicon nitride 204 (*see* Fig. 5(g)), the pad silicon dioxide 202 (*see* Fig. 5(h)) and other “extensions” of the STI structure. Ex. 1006 (Saki), 4:59 – 5:7. The resultant transistor and isolation structure is shown in Fig. 5(i). I note, as shown in Fig. 5(i), that Saki’s isolation structure defines a recess in the region above the silicon dioxide isolation structure, as indicated by the red dashed lines.



177. Thus, in my opinion, Saki teaches the subject matter of this claim limitation.

- d. [1.3] “a gate electrode and a gate insulation layer formed above said substrate, a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure; and” and [13.3] “a gate electrode comprised of polysilicon . . .”

178. Saki teaches forming gate electrode 214 and a gate insulation layer above substrate 200. Ex. 1006 (Saki), 5:22-26. As can be verified visually with reference to Fig. 5(i), the end portions of gate electrode 214 and the gate insulation layer extend into the recess above the silicon dioxide isolation structure.

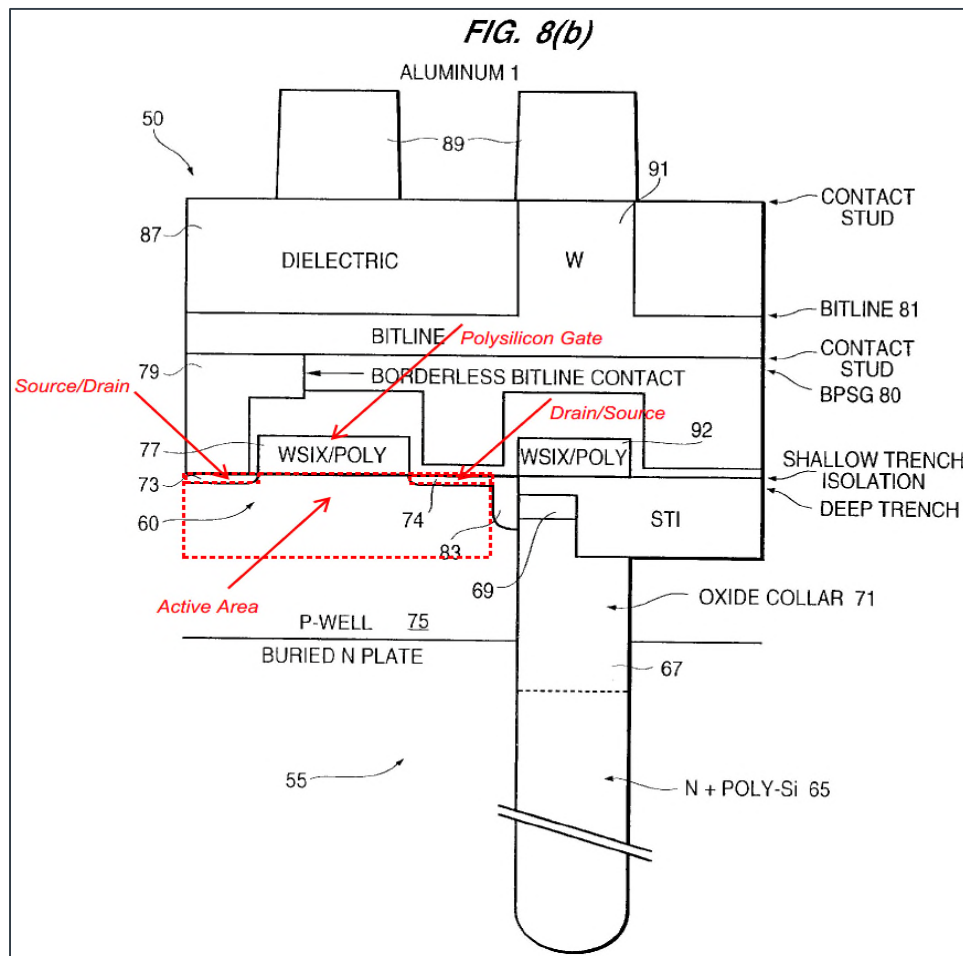


179. With respect to claim 13, I note that Saki teaches forming the gate electrode from polysilicon. For example, Saki teaches—in connection with “a method of manufacturing the DRAM cell 50 using the shallow isolation structure and method of the present invention”—forming conductive material (such as a gate electrode) using “N+-type polycrystalline silicon” or “undoped polycrystalline silicon.” Saki discusses in detail its method of manufacturing DRAM cell 50 at 7:19-59.

180. Thus, Saki teaches the subject matter of this claim limitation.

e. [1.4] and [13.4] “a source region and a drain region formed in said substrate.”

181. Saki teaches that the completed semiconductor device includes a source region and a drain region formed in the substrate. For example, in describing a “trench DRAM cell 50” using the isolation techniques of Saki’s invention, Saki teaches the formation of source/drain regions 73/74 in the substrate, as indicated by the red dashed lines in Fig. 8(b), reproduced below. Ex. 1006 (Saki), 6:54 – 7:17 (“Transfer gate 60 includes N-type source/drain and drain/source regions 73 and 74”).



182. Similarly, Saki teaches the formation of source/drain regions in connection with “a method of manufacturing the DRAM cell 50 using the shallow isolation structure and method of the present invention.” Ex. 1006 (Saki), 7:19-22. Saki specifically describes: “Using the gate electrodes as masks, *source/drain regions may be formed by ion implantation.*” Ex. 1006 (Saki), 8:55-58.

2. Saki Renders Obvious Claims 23

a. [23.P] “A transistor, comprising:”

183. Saki teaches the subject matter of this claim limitation for the reasons provided in Section IX.B.1.a.

b. [23.1] “a semiconducting substrate;”

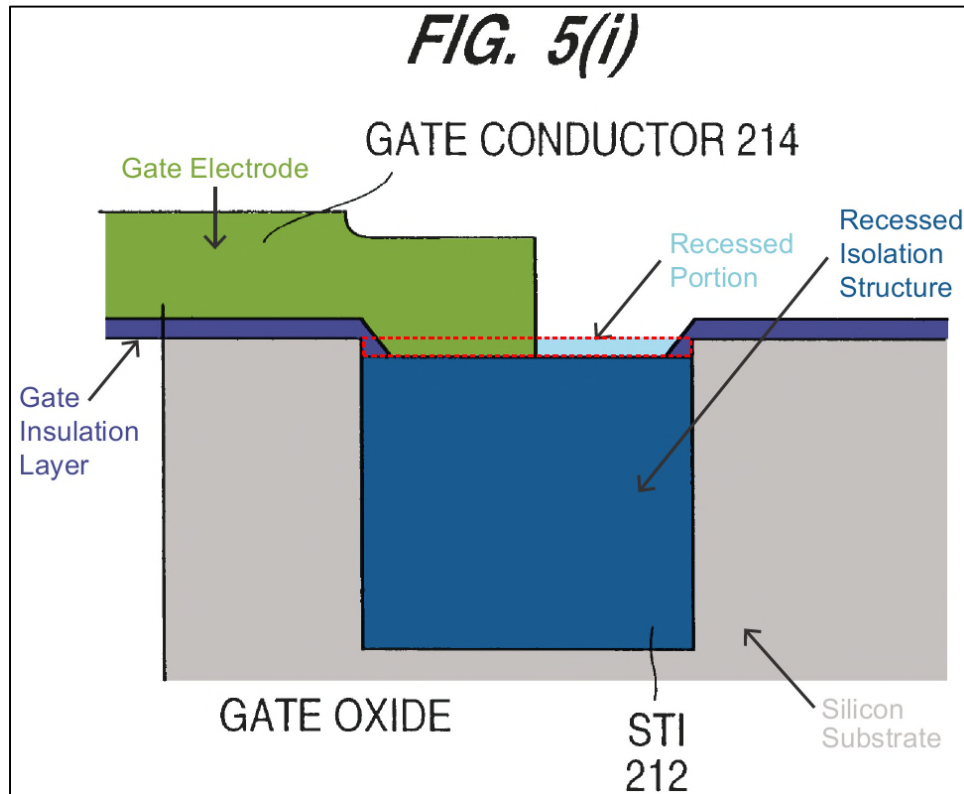
184. Saki teaches the subject matter of this claim limitation for the reasons provided in Section IX.B.1.b.

c. [23.2] “a recessed isolation structure defining an active area having an upper surface and an exposed sidewall surface;”

185. Saki teaches the subject matter of this claim limitation for the reasons provided in Section IX.B.1.c.

186. Further, Saki teaches forming STI structure 212, which includes a recessed portion and a portion filled with an oxide film insulator, as illustrated in annotated Fig. 5(i) below. As shown by the dashed red lines in the annotated figure, the recessed portion is partially filled by the gate electrode and gate insulation layer. I note also that Saki describes the active area as being defined by

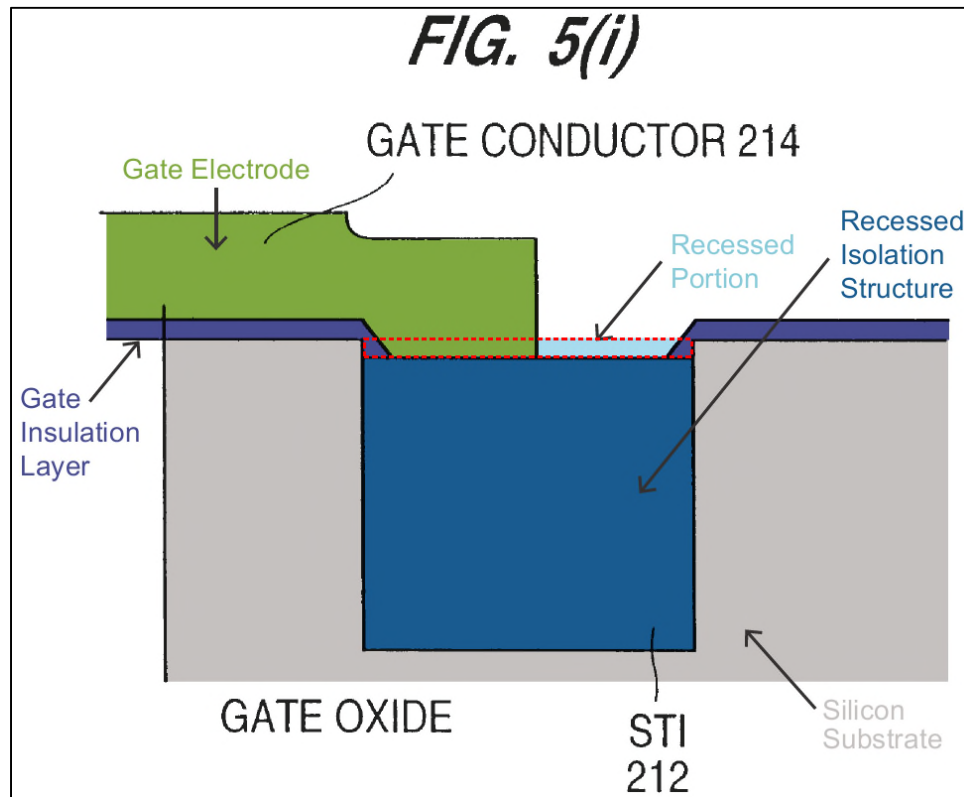
the STI structure. Ex. 1006 (Saki), 3:9-14 (noting “the active area defined by the shallow trench isolation structure”). Thus, STI structure 212 defines an active area having an upper surface and an exposed sidewall surface, as shown in the annotated figure.



- d. [23.3] “a gate insulation layer and a gate electrode positioned above a portion of said upper surface and a portion of said exposed sidewall surface of said active area; and”

187. Saki teaches the subject matter of this claim limitation for the reasons provided in Section IX.B.1.d.

188. Further, as can be verified visually from Saki's Fig. 5(i) below, gate conductor 214 and the gate insulation layer (oxide) are positioned above the upper surface and exposed sidewall surface of the active area.

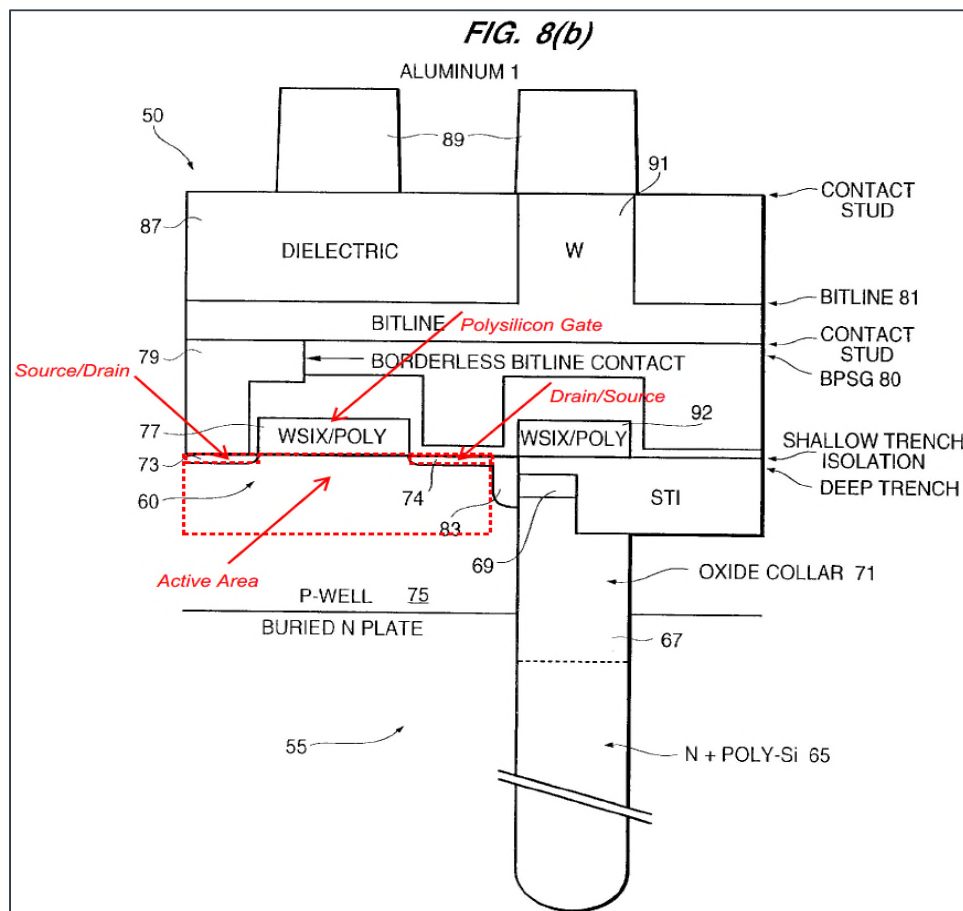
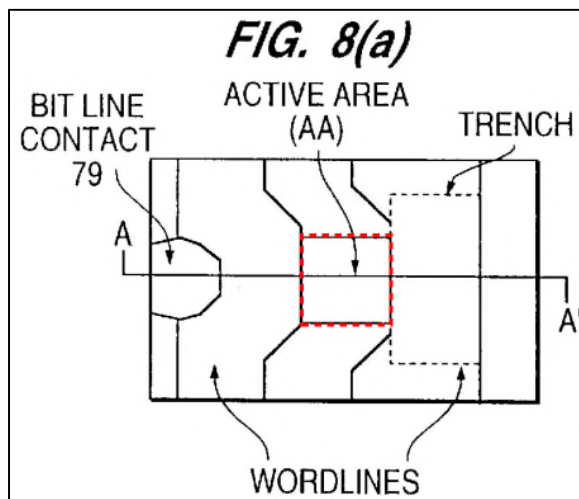


e. [23.4] “a source region and a drain region formed in said active area.”

189. Saki teaches the subject matter of this claim limitation for the reasons provided in Section IX.B.1.e.

190. As discussed previously, Saki teaches forming source/drain regions 73/74 in the substrate. A POSITA, reading Saki, would recognize that source/drain regions 73/74 are formed in the “Active Area (AA)” region depicted below by the red dashed lines in Fig. 8(a) (a “top-down view of the trench DRAM cell”). Ex.

1006 (Saki), 6:57-59. This can be verified visually by referring to Fig. 8(b) below, which “is a cross-sectional view taken along line A-A’ of FIG. 8(a).” Ex. 1006 (Saki), 6:57-59



191. This understanding is confirmed by Saki's disclosure at 6:63-67:
"Transfer gate 60 includes N-type source/drain and drain/source regions 73 and 74 formed in P-type well 75 and a WSix /polycrystalline silicon gate 77 insulatively spaced from the channel region between source/drain region 73 and drain/source region 74." In other words, Saki teaches a "Transfer Gate 60" (for the DRAM cell) that includes polysilicon gate 77, with a diffusion region (under polysilicon gate 77) and source/drain regions 73/74 formed in the active area, as illustrated in annotated Fig. 8(b) above.

3. Saki Renders Obvious Claims 2 and 24

192. Claims 2 and 24 respectively depend from claims 1 and 23. I note that claims 2 and 24 are otherwise identical. As I explained above, Saki teaches the subject matter of claims 1 and 23.

193. As I will explain below, in my opinion, Saki renders obvious the additional subject matter of claims 2 and 24.

a. [Claim 2] "The transistor of claim 1, wherein said semiconducting substrate is comprised of silicon" and [24] "The transistor of claim 23 . . ."

194. As discussed above, Saki discloses forming a transistor on silicon substrate 200.

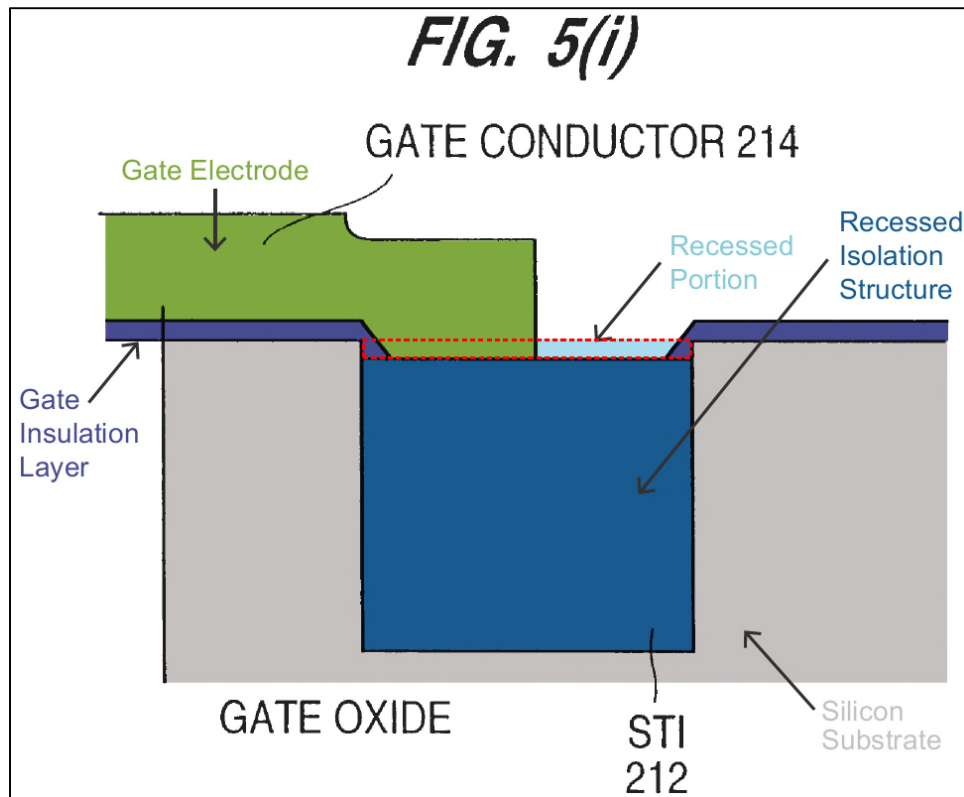
4. Saki Renders Obvious Claims 3, 14 and 25

195. Claims 3, 14 and 25 respectively depend from claims 1, 13 and 23. I note that claims 3, 14 and 25 are otherwise identical. As I explained above, Saki teaches the subject matter of claims 1, 13 and 23.

196. As I will explain below, in my opinion, Saki renders obvious the additional subject matter of claims 3, 14 and 25.

- a. [Claim 3] “The transistor of claim 1, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride”; [14] “The transistor of claim 13 . . .”; and [25] “The transistor of claim 23 . . .”

197. As discussed above, Saki discloses that silicon dioxide is deposited over the substrate, including in isolation structure 212. Ex. 1006 (Saki), 4:51-59 (“A *silicon dioxide layer* 212 is then blanket deposited over the entire surface of the substrate . . .”). The isolation structure becomes a recessed isolation structure (formed of silicon dioxide) following a series of etching processes, as discussed in detail in Section IX.B.1.c, above. Refer to Fig. 5(i) below.



5. Saki Renders Obvious Claims 6 and 28

198. Claims 6 and 28 respectively depend from claims 1 and 23. I note that claims 6 and 28 are otherwise identical. As I explained above, Saki teaches the subject matter of claims 1 and 23.

199. As I will explain below, in my opinion, Saki renders obvious the additional subject matter of claims 6 and 28.

- a. **[Claim 6] “The transistor of claim 1, wherein said gate electrode is comprised of polysilicon” and [28] “The transistor of claim 23 . . .”**

200. As discussed above, Saki teaches forming a polysilicon gate.

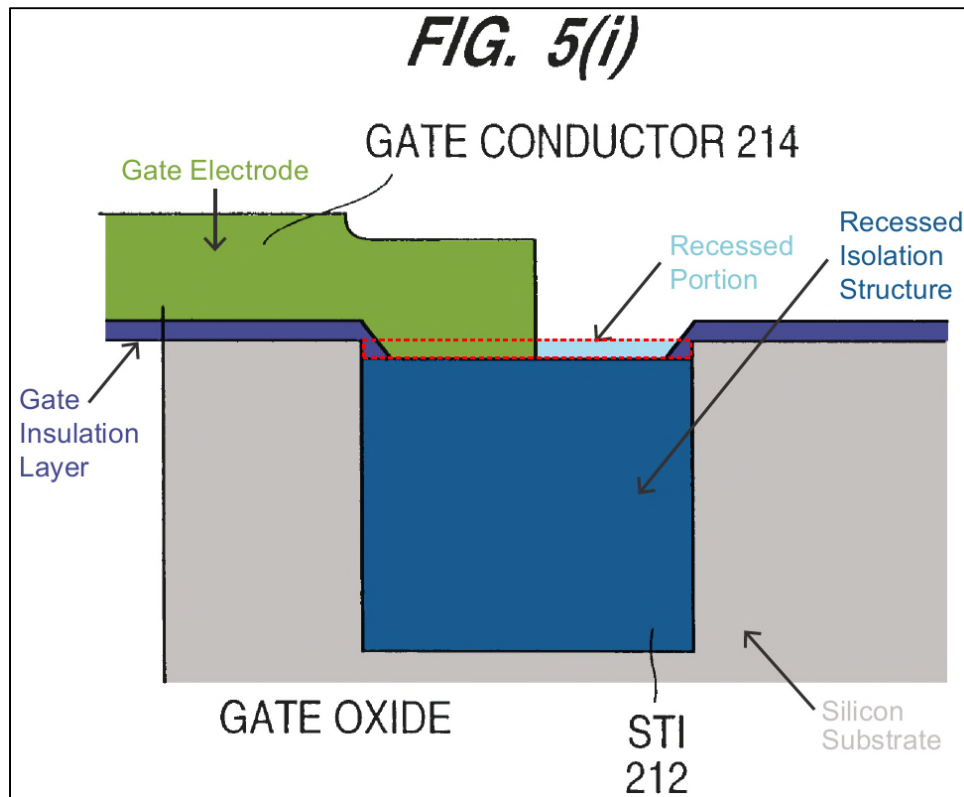
6. Saki Renders Obvious Claims 11, 21 and 33

201. Claims 11, 21 and 33 respectively depend from claims 1, 13 and 23. I note that claims 11, 21 and 33 are otherwise identical. As I explained above, Saki teaches the subject matter of claims 1, 13 and 23.

202. As I will explain below, in my opinion, Saki renders obvious the additional subject matter of claims 11, 21 and 33.

- a. **[Claim 11] “The transistor of claim 1, wherein said gate electrode has first and second end portions that extend into said recess”; [21] “The transistor of claim 13 . . .”; and [33] “The transistor of claim 23 . . . defined by said recessed isolation structure.”**

203. As discussed above, Saki teaches that gate conductor 214 extends into the recess above the oxide film inside the trench. More specifically, first and second end portions of gate conductor 214 extend into the recess. The annotated figure below depicts a first end portion of gate conductor 214 extending into the trench formed to the right; a second end portion extends into the trench formed to the left (not shown).



7. Saki Renders Obvious Claims 12, 22 and 34

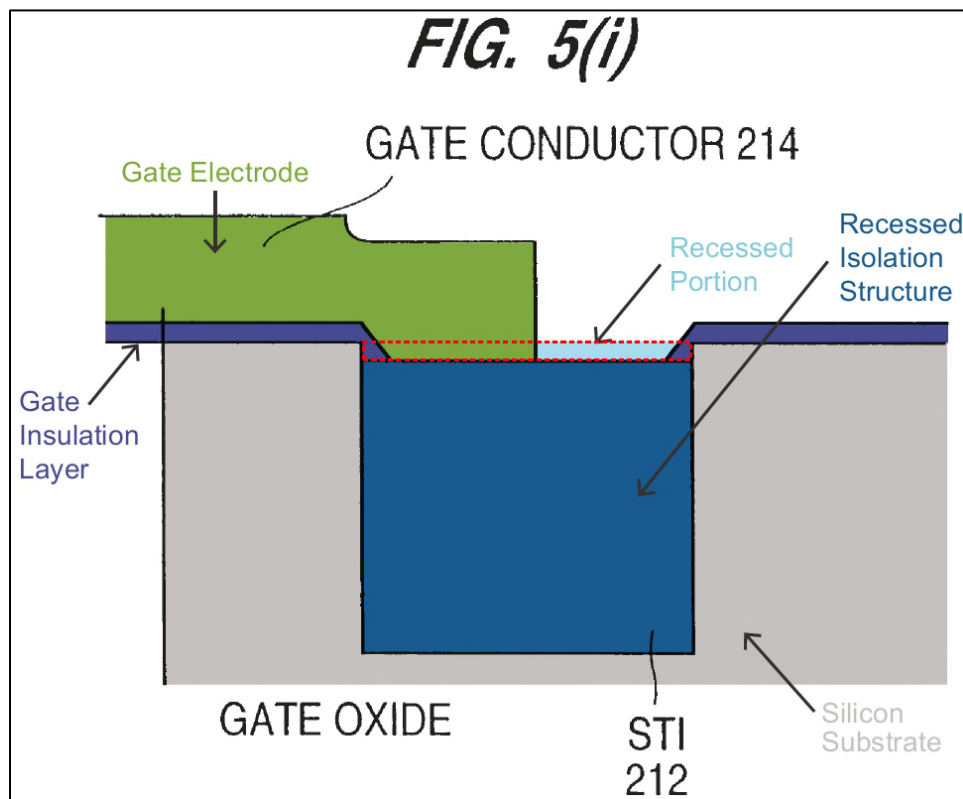
204. Claims 12, 22 and 34 respectively depend from claims 11, 21 and 33.

I note that claims 12, 22 and 34 are otherwise identical. As I explained above, Saki teaches the subject matter of claims 11, 21 and 33.

205. As I will explain below, in my opinion, Saki renders obvious the additional subject matter of claims 12, 22 and 34.

- a. [Claim 11] “The transistor of claim 11, wherein said first and second end portions extending into said recess are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure”; [22] “The transistor claim 21 . . .”; and [34] “The transistor of claim 33 . . .

206. Further, as can be verified easily by reference to Saki’s Fig. 5(i) below, the first and second end portions of gate conductor 214 are positioned above a portion of a sidewall of the active region:



C. Ground 7. Claims 5, 16 and 27 Are Obvious Over Saki and Wada

1. Saki and Wada Render Obvious Claims 5, 16 and 27

207. Claims 5, 16 and 27 respectively depend from claims 1, 13 and 23. I note that claims 5, 16 and 27 are otherwise identical. As I explained above, Saki teaches the subject matter of claims 1, 13 and 23.

208. As I will explain below, in my opinion, the combination of Saki and Wada teaches and renders obvious the additional subject matter of claims 5, 16 and 27.

- a. **[Claim 5] “The transistor of claim 1, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å” and [Claim 27] “The transistor of claim 23 . . .”**

209. As discussed above, Wada teaches the subject matter of claims 5, 16 and 27.

2. It Would Have Been Obvious to Combine the Teachings of Saki and Wada

210. In my opinion, as of the '122 patent's filing date, a POSITA would have found it obvious to form the depth and width of Saki's recessed isolation structures to the thickness ranges as taught by Wada.

211. One of ordinary skill would also have a reasonable expectation that this combination would succeed and result in a semiconductor device falling within the scope of claims 5, 16 and 27.

212. I note that Saki and Wada both focus on improvements to techniques for isolating transistors on the same substrate. As discussed above, it was well recognized in the art that isolating transistors on the same substrate from one another, particularly as transistors continued to shrink in size, was critical to transistor and overall device operation. Therefore, in my opinion, a POSITA reading Saki would have been motivated to combine the teachings of Wada and Saki to achieve a greater degree of isolation, thereby avoiding any adverse effects on transistor performance caused by insufficient isolation.

213. I note that Saki and Wada also share a common aim of simplifying transistor design and manufacturing process. As discussed above, Wada explains that its improved isolation structure “not only achieves a higher density of integration of active devices in a given space of the substrate but also *simplifies the design of interconnection lines*, thereby suggesting a path to production of very large integrated circuits economically in the future.” Ex. 1004 (Wada), Abstract. And Saki states: “Still further, the method of the present invention has a small number of steps and therefore contributes to ease of device manufacture and reduced manufacturing costs.” Ex. 1006 (Saki), 3:17-21.

214. It is my further opinion that a POSITA would have every reason to believe that applying Wada’s teachings to the semiconductor device of Saki would succeed. As I explained above, Saki and Wada are in the same field of

semiconductor processing and fabrication. Thus, in my opinion, the overlap and similarity in subject matter between Saki and Wada would lead a POSITA to believe that forming a trench isolation structure based on the width and depth ranges as taught by Wada could be successfully applied to Saki's semiconductor device.

D. Ground 8. Claims 7-10, 17-20 and 29-32 Are Obvious Over Saki and Lu

1. Saki and Lu Render Obvious Claims 7, 17 and 29

215. Claims 7, 17 and 29 respectively depend from claims 1, 13 and 23. I note that claims 7, 17 and 29 are otherwise identical. As I explained above, Saki teaches the subject matter of claims 1, 13 and 23.

216. As I will explain below, in my opinion, the combination of Saki and Lu teaches and renders obvious the additional subject matter of claims 7, 17 and 29.

- a. **[Claim 7] “The transistor of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride”; [Claim 17] “The transistor of claim 13 . . .”; and [Claim 29] “The transistor of claim 23 . . .”**

217. Saki teaches a gate oxide film. Ex. 1006 (Saki), 1:25-29 (“*A silicon dioxide (SiO₂) layer 102 and a silicon nitride (Si₃N₄) layer 104 are successively formed on the surface of a silicon substrate 100 . . .*”). Further, as discussed in detail in Section VIII.C.1 above, an oxide film, in the field of semiconductor

fabrication, includes the class of silicon dioxide (SiO₂) insulators, one of the most common insulators used in the art. Further, a POSITA, reading Saki, would understand Saki's oxide film as being silicon dioxide when considering that (1) Saki uses a *silicon* substrate and discloses *growing a gate oxide layer* on the substrate (Saki, 1:47-51), and (2) Saki uses silicon dioxide throughout the process of forming the STI structure, including to form the pad silicon dioxide layer 202 and deposit silicon dioxide layer 212 into the trench 206. *See, e.g.*, Ex. 1006 (Saki), 3:66 – 5:7.

218. I note further that, as discussed above, Lu teaches the subject matter of claims 7, 17 and 29.

2. Saki and Lu Render Obvious Claims 8, 18 and 30

219. Claims 8, 18 and 30 respectively depend from claims 1, 13 and 23. I note that claims 8, 18 and 30 are otherwise identical. As I explained above, Saki teaches the subject matter of claims 1, 13 and 23.

220. As I will explain below, in my opinion, the combination of Saki and Lu teaches and renders obvious the additional subject matter of claims 8, 18 and 30.

- a. **[Claim 8] “The transistor of claim 1, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å”; [18] “The transistor of claim 13 . . .”; and [30] “The transistor of claim 23 . . .”**

221. As discussed above, Lu teaches the subject matter of claims 8, 18 and 30.

3. Saki and Lu Render Obvious Claims 9, 19 and 31

222. Claims 9, 19 and 31 respectively depend from claims 1, 13 and 23. I note that claims 9, 19 and 31 are otherwise identical. As I explained above, Saki teaches the subject matter of claims 1, 13 and 23.

223. As I will explain below, in my opinion, the combination of Saki and Lu teaches and renders obvious the additional subject matter of claims 9, 19 and 31.

- a. **[Claim 9] “The transistor of claim 1, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.”; [19] “The transistor of claim 13 . . .”; and [31] “The transistor of claim 23 . . .”**

224. As discussed above, Lu teaches the subject matter of claims 9, 19 and 31.

4. Saki and Lu Render Obvious Claims 10, 20 and 32

225. Claims 10, 20 and 32 respectively depend from claims 1, 13 and 23. I note that claims 10, 20 and 32 are otherwise identical. As I explained above, Saki teaches the subject matter of claims 1, 13 and 23.

226. As I will explain below, in my opinion, the combination of Saki and Lu teaches and renders obvious the additional subject matter of claims 10, 20 and 32.

- a. **[Claim 10] “The transistor of claim 1, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region”; [20] “The transistor of claim 13 . . .”; and [32] “The transistor of claim 23 . . .”**

227. As discussed above, Lu teaches the subject matter of claims 10, 20 and 32.

5. It Would Have Been Obvious to Combine the Teachings of Saki and Lu

228. In my opinion, as of the '122 patent's filing date, a POSITA would have found it obvious combine the teachings of Saki and Lu, as I discuss below. Specifically, a POSITA would have been motivated to: (i) form Saki's *gate electrode* to the thickness taught in Lu (as described in claims 8, 18 and 30); (ii) form Saki's *gate insulation layer* from silicon dioxide or silicon oxynitride (as described in claims 7, 17 and 29) and to the thickness taught in Lu (as described in claims 9, 19 and 31); and (iii) form, in Saki's transistor, *source/drain extension implant regions* as taught in Lu (as described in claims 10, 20 and 32).

229. One of ordinary skill would also have a reasonable expectation that these combinations would succeed and result in a semiconductor device falling within the scope of claims 7-10, 17-20 and 29-32.

230. I note that Saki and Lu both focus on improving upon prior art processes related to semiconductor fabrication and enhancing transistor performance. Saki teaches improved shallow trench isolation techniques that thereby improve transistor performance, particularly in the context of DRAM applications. And as I explained previously, Lu, similarly, focuses on improving MOS transistor performance in connection with DRAM (memory) applications; Lu specifically describes forming “thinner” or “thicker” gate insulation layers depending on the voltage requirements of the associated DRAM circuitry.

231. As discussed in detail above, the continued trend of shrinking transistor size and thinner transistor elements (e.g., gate electrode and gate oxide)—and the reliability issues that stemmed from this trend—was generally recognized well before the ’122 patent’s filing date. Refer to the discussion in Section VIII.E.8, above.

232. With respect to the gate electrode and gate oxide, a POSITA would have appreciated the importance of fabricating devices in a way that achieves reliable and improved transistor performance, as discussed in Section VIII.E.8 and Lu, 2:34-41 and 4:47-52. Thus, in my opinion, a POSITA would have been

motivated to apply the teachings of Lu to Saki's process of forming the gate electrode and gate oxide to achieve improved transistor performance and reliability.

233. Further, in my opinion, a POSITA would have also recognized that Lu's technique of using lightly-doped drains ("**LDD**") would have increased the performance of the transistor taught by Saki. As discussed in Section VIII.E.8, above, Lu's LDD technique addresses the well-known "hot-carrier effect." Specifically, a POSITA would have been motivated to use Lu's LDD technique to form source/drain extension implant regions within Saki's source/drain regions, because doing so would: (1) separate the heavily-doped source/drain regions from the conducting channel, (2) thereby diminishing the hot-carrier effect, and (3) as a result, minimize off-state current leakage. Put another way, forming source/drain extension implant regions would extend the transistor active area, which in turn would reduce leakage and increase the drive current.

234. It is my further opinion that a POSITA would have every reason to believe that applying Lu's teachings to the semiconductor device of Saki would succeed. As I explained above, Saki and Lu are in the same field of semiconductor processing and fabrication; in particular, both relate to DRAM applications and the use of shallow trench isolation (STI) techniques. And both focus on improving semiconductor fabrication methods to realize increased transistor performance.

Thus, in my opinion, the overlap and similarity in subject matter between Saki and Lu would lead a POSITA to believe that forming the gate electrode, gate insulation layer, and source/drain extension implant regions in the manner taught by Lu could be successfully applied to Saki.

X. CONCLUSION

235. I am therefore of the opinion that claims 1-3, 5-14, 16-25, and 27-34 of the '122 patent are unpatentable given the prior art references discussed above.

236. I hereby declare under penalty of perjury under the laws of the United States of America that the foregoing is true and correct, and that all statements made of my own knowledge are true and that all statements made on information and belief are believed to be true. I understand that willful false statements and the like are punishable by fine or imprisonment, or both (18 U.S.C. § 1001).

A handwritten signature in cursive script, reading "Sayfe Kiaei".

Date: June 8, 2020

Dr. Sayfe Kiaei, Ph.D.

ATTACHMENT A

Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

Sayfe Kiaei

Professor, Motorola Endowed Chair Professor in Analog and RF Integrated Circuits
School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ

FIELDS OF SPECIALIZATION

- Analog, Digital and RF Integrated Circuits, Sensors, Bio-Electronics, Power Management IC
- Digital Signal Processing, Adaptive & Array processing, Wireless and Wireline Communication System,

DEGREES

- **Ph.D.**, Electrical and Computer Engineering, Washington State University, 1987
- **M.S.**, Electrical and Computer Engineering, Washington State University, 1984
- **B.S.E.E.**, Electrical Engineering, Northeastern University/WSU, 1982

ACADEMIC POSITIONS

2001-Present: Professor, Motorola Endowed Chair Professor in Analog and RFIC School of Electrical, Computer and Energy Engineering, Arizona State University, Tempe, AZ

- **Professor:** Research and teaching in integrated circuits, RF circuits and systems, Communications, Wireless and Wireline transceiver, mixed-signal and Analog IC, Sensors, Power management IC.
- **Research Projects:**
 - Analog and digital IC, Power Management IC, Radio Frequency IC, RF transceiver
 - Digital Signal Processing, Audio processing, adaptive signal processing, Array processing, AI
 - Wireless communication system, wireless modems, 1G, 2G GSM, 3G CDMA, 4G LTE, 5G wireless mobile system, LTE, WiFi, Bluetooth, Wireless system standards
 - Wireline Communication system and transceivers, MODEM standards, CABLE MODEM DOCIS, DSL
 - Sensors, bio-electronics circuits and systems, heart monitoring system, hearing aid
- Research Funded by NSF, USAID, DARPA, JPL, NASA, Motorola Inc., Intel Inc., Broadcom, Qualcomm, Raytheon, General Dynamics, Texas Instruments, and over 10 other industries. List of Current significant research awards:
 - Partnership Center for Energy systems, USAID, 2015-2020, \$18M. Principle Investigator
 - QESST NSF ERC Center on Solar Energy, NSF, 2010-2020, \$36M, Co-PI, Test-bed Director
 - Solar Energy Development in ME, Private funds and World Bank, \$2M
 - Connection One NSF Center, Director, 2004-Present, Total funding \$10M, annual funding over \$500K.

2004-Present, Director and founder of NSF IUCRC Center Connection One, School of Electrical, Computer, and Energy Engineering, Arizona State University, Tempe, AZ; <https://connectionone.org>

- The NSF Connection One Industry/University Cooperative Research Center was established the center in 2002 with focus on communication system, integrated Circuits and Systems, wireless system, RF, sensors,

Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

and related areas. The center has five university member with over 30 industrial members. Total funding over \$10M, annually over \$500K. www.connectionone.org

2014-2020, Director, USAID, US-PCASE: Center for Advance Studies in Energy, Funding \$18M.

<https://uspcase.asu.edu/>

- **Director and PI:** PCASE - Partnership Center for Energy systems, Energy Center funded by the USAID.
- USIAD Centers for Advanced Studies in Energy program (USPCAS-E) is a partnership between Arizona State University and two leading Pakistani universities: the National University of Science and Technology (NUST) Islamabad and the University of Engineering and Technology in Peshawar (UET).
- PCASE has developed two new Graduate schools of Energy. Within 5 years, the center has over 1000 MS and PHD Students, with 14 new energy degrees in MS and PhD, two new building with 20+ energy labs in the power system, grid, power electronics, renewable energy, PV, Wind, Hydro, bio-fuel, fuel cell, batteries and storage, and thermal areas.

2008-2012: Associate Dean of Research, Ira A. Fulton Schools of Engineering, Arizona State University

Responsible for leading the research infrastructure, promoting and developing research programs with industry and federal agencies, leading large multi-university proposals, investing and providing seed funding to foster new research areas, and promoting graduate program in the college of engineering. Research Enterprise support included:

- Increase College of Engineering research funding from \$50M to over \$80M.
- Working with Vice President for Research, Dean's, and directors on University-wide research initiatives.
- Established the first NSF Engineering Research Center (ERC) at the ASU on Solar Energy QESST. Managed, organized and planned the ERC proposal process. ASU is the lead school partnering with MIT, Georgia Tech, U of Delaware, Cal-Tech, U of New Mexico, and UA.
- Lead several trans-disciplinary 4M research projects (4M: multi-million, multi-investigator, multi-disciplinary, multi-university grants) in energy, security, and related initiatives.
- Oversight of over 20 existing research centers in the college of Engineering.
- Engage with industry and federal government to establish new research collaborations.
- Organized workshops and supported proposals for NSF, NIH, DOE, DOD, DARPA, etc.
- Organized workshops for new assistant professors to apply for NSF CAREER Awards. ASU CAREER awards grew from 3 annual awards in 2008 to over 15 CAREER awards by 2012.
- Research Administration and pre-award proposal administration for the schools. Developed a decentralized research administration and advancement team for the Schools supporting 5 schools, 12 departments, over 220 engineering faculty, with funding over \$70M.
- Annual budget over \$7M for supporting research centers, seed funding for new center, cost sharing, proposal support, equipment and infrastructure support, graduate scholarships, and research administration.
- ADR Staffs included, Director of industrial and government liaison, Director of research administration, and 14 research advancement staff.
- Graduate Programs: Recruiting, Fellowships, marketing, outreach, coordination with departments

1995-2002, Adjunct Professor, Electrical and Computer Engineering Dept., The University of Texas, Austin, Texas, Taught graduate courses at UT Austin on Introduction to Telecommunication System and Digital Communications. Co-advised two Ph.D. program committees in IC design and Telecomm (while at Motorola)

Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

1987-1994, NSF Center For Digital / Analog IC (CDADIC) Co-Director, NSF IUCRC Center director at Oregon State University. The CDADIC was established the center in 1987 with focus on integrated circuits at WSU, UW, and OSU with over 20 industrial members - <https://cdadic.oregonstate.edu/>

1987-1993, Assistant / Associate Professor (Tenured) Electrical and Computer Engineering Department, Oregon State University, Corvallis, OR

- Research and classes in Electronics, DSP, Communication system and networks, Wireless systems, MODEMS. Graduated 30 MS and Ph.D. students.
- Faculty Chair, Computer Engineering Program, Developed a new Computer Engineering Program at OSU in 1987

INDUSTRIAL POSITIONS

1993-2002: Motorola Inc., Senior Member of Technical Staff, Personal Communication Sector, Austin, Texas - Worked projects related to wireless communications, two way radios, wireless networks, ADSL and MODEM, RF, and related areas.

- **Motorola Cellular Division, Wireless Technology Center (WITC), 1997-2002.** Responsible for development of integrated circuits and systems for wireless handset. Lead number of projects including cellular (2G, 3G, 4G), wireless connectivity (Bluetooth and WIFI transceiver), GPS and location Receiver, wireless networks, 2-way radios and related areas. Worked on the development of various subcomponents including system design, link budget, RF front-end, filtering, analog front-end, power management, and baseband circuits and systems.
- **Motorola SPS, Broadband Products Operations, 1993-1997,** Worked on the development of XDSL (ADSL, VDSL, G.lite) systems including OFDM, modulation, synchronization, equalization and the development of a single chip ADSL transceiver (*CopperGold™*). The transceiver contained Analog Front End (A/D, D/A, Hybrid), DMT, modulation/demodulation, FFT, IFFT, echo canceler, time domain equalizer, front-end constellation mapping, Trellis code modulation, Viterbi decoder) and an on-chip DSP core.
- **Standards,** Represented Motorola in various standards including 2G-4G, GPS, Bluetooth, WiFi, 802.11, and DSL standards including T1E1, International Telecommunication Unit (ITU), T1E1, ETSI, 3GPPP, Universal ADSL Working Group (UAWG), Bluetooth working group, G.Lite working group, etc.
- **Land Mobile Products Sector,** Responsible for Wireless digital two-way radios, hot spot wireless network, next generation of digital two-way radios, "*Talk about Radios*", Japanese cellular systems (PHS).
- **University relations,** Responsible for the development of collaborative research programs with several universities. Responsible for funding research in the areas of Wireless Transceiver IC Design, RF, and mixed-signal and baseband system architecture.

1985-87: Member of Research Staff, Boeing Co., Bellevue, Wa, Flight Systems Research and Technology Center, summer. Design Engineer, Hardware and CAD tool development for system control.

Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

AWARDS

- IEEE Fellow 2004-Present
- IEEE Fellows CAS Committee Chair, 2009-2012
- Global Standards Award, For contributions in the International Telecommunication Unit (ITU) for Asymmetric Digital Subscriber Line (ADSL) G.Lite Standards. Motorola Inc., 1999.
- 10X Cycle Reduction Award, for development of new IC design process from DSP algorithm to IC layout, Motorola Inc., 1995.
- IEEE Darlington best paper Award, IEEE Circuits and Systems Society Best Paper Award, 1995. For “Characterization and Comparison of CMOS FSCL Circuits with Conventional CMOS for mixed-signal ICs,” Published at: *IEEE Trans. on Circuits and Systems II*, Sept. 93.
- Carter Best Teaching Award, College of Engineering Best Teacher Award, Oregon State University, 1992. For “*outstanding and inspirational teaching in the College of Engineering*”. Award is selected by the confidential vote of all of the undergraduate students in the College of Engineering among over 125 professors in the College.
- Industrial University Fellowship (IUF) Award, *National Science Foundation*, 1993.
- Research Initiation Award, *National Science Foundation*, 1990-93.
- Outstanding Graduate Student Scholarship, *Azur-Data Inc.* WSU, 1984

RESEARCH PROJECTS

Partial list of Research Awards:

- USAID, PCASE – Center for Energy systems, 2015-2020, \$18M. PI and Director
- NSF, QESST NSF ERC Center on Solar Energy, 2010-2020, \$36M, Kiaei, Co-PI, Testbed Director,
- Private Donors, \$1.5M, 2012-2015, Solar Energy Development
- NSF IUCRC Center, Connection One 2002-present, Over \$10M as PI, over \$0.5M annual center awards
- NSF, Micro-Power Multi-Phase MEMS Hearing Aid, 2007-2011, \$500K
- NSF - Design for Implantable Bio-Sensors, 2007-2009, \$480K
- Science Foundation of AZ, PEPER- Photovoltaic Environmental Performance and Reliability for the Arizona-Wide Electric Grid, 2009-2013, \$1.2M
- SRC –Self Characterization for Calibration and Process Feedback of MEMS Devices, 2011-2014, \$300K
- NSF- Cognitive MIMO Communications for Dynamic-Spectrum Wireless Networks – 2012-2014, \$150K
- NSF, Autonomous Self-Healing Sensor Network Radio, 2010-2014, \$250K
- DARPA, Neural-Enabled Prostheses with Sensorimotor Integration, \$500K
- NSF, Microwave Sensors for Vital Signs Monitoring Device Design, 2011-2013, \$250K
- NSF, Various REU funds, 8/31/12-8/31/13, \$400K
- DARPA, Nano-Mechanical RF Band pass resonator for 2GhZ RF Applications, with JPL, \$2.2 M, 2002-2005,
- Qualcomm, Connection One Center, Various projects in 3G-5G, WiFi (802.11), GPS, and Bluetooth ,

Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

2005-Present, \$1.2M

- Texas Instruments, Various projects in Power management and RFIC, 2005-20012, \$1.5M
- *Motorola Inc.*, Various projects in Power management and RFIC Various projects 2002-2010, \$1.2M.
- *SIRF Technologies*, GPS Transceiver, 2005, \$300K.
- *Ridgetop Inc.*, RF Harsh Environment, \$200K
- Freescale Semiconductor, PWM Power Management, 2006, \$150K
- State of Arizona, *WINTeCH- Wireless Integrated Nano Technology Center Support* (2005-2009), Ranging from 450K annually from 2005-2009.
- BAE Systems; “New Techniques for Time Measurement Circuits LiDAR; 2005-2008; \$650K
- SRC (Semi-conductors research Corp), Ultra-Wideband Transceivers for cellular and WiFi 802.11, \$225K, 2001-2003
- Intel Corporation, Design of Multi-Standard RF Front-End Circuits for Cellular and WiFi, \$300K, 2002-2005
- *National Science Foundation*, Adaptive Compensation of Analog circuits imperfections using DSP methods, \$150K, 1996 (tie project with UC San Diego NSF center), 2010-2011
- Center for the Design of Analog/Digital IC’s (CDADIC) 1987-1995, At Oregon State, \$1.5M
- Low Power IF processing for Direct Digital Transceivers, *Motorola Inc*, \$100K, 93.
- Hewlett-Packard Faculty Chair position in Mixed-Signal IC, HP, 1995-97, \$500K
- *National Science Foundation*, *Motorola Inc.* Faculty Industry Fellowship, \$250K, 93-94.
- *National Science Foundation*, *Research Initiation Award (RIA)* (same as current *CAREER Award*), Synthesis and Automatic Derivation of Multi-Rate VLSI Arrays for DSP Algorithms, , 90-93. \$320K.
- CDADIC, various projects on Low-Noise Source Coupled Logic (SCL), Mixed-Mode IC's, *CDACIC* \$350K, 1988-1992.
- Decimation Filters for A/D Noise Enhancements, Tektronix, Inc., \$100K, 1988.
- Various grants for IC Fabrication (DARPA/MOSIS, VLSI), testing equipment (Tek, HP), DSP system development (TI, Motorola), ranging in various amounts up to \$200K/year. At Oregon State, 1988-1997.

PROFESSIONAL RECOGNITION

- IEEE Fellow, 2002-Present
- IEEE Fellow Committee Chair, CAS, 2008-2010
- IEEE Fellow Committee member, 2007-2010.
- IEEE Senior Member, 1993-Present, IEEE Member 1987-1992.
- IEEE Faculty Advisor, Oregon State University, 1987-1990

IEEE Editorials

- IEEE Microwave Magazine, Guest Editor,

Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

- IEEE System Journal, Associate Editor, 2010-2011.
- Associate Editor, IEEE Transactions on VLSI, Jan 2001-2008.
- IEEE Comm. Magazine, guest Editor, Feature Issues on “Circuits for Wireless and Wireline Communications,” April 1999.
- IEEE Transactions on Microwave Theory and Techniques , Guest editor, Special Issue on: "Radio Frequency IC Design,” Dec. 1998.
- IEEE Transactions on Circuits and Systems-II , guest editor, Special Issue on: “Low-Power Wireless Communication Systems,” June 1997.
- Associate Editor, IEEE Transactions on Circuits and Systems-II, 1993-1996.
- *Editor and Reviewer for IEEE ASIC/SOC Conference,*
- *Editor and Reviewer for IEEE Microwave Theory and Techniques Journal*
- *Editor and Reviewer for International Journal of Analog Integrated Circuits and Signal Processing*
- *Founding member of IEEE RF Integrated Circuits Symposium*
- *Associate Editor, IEEE Communications, Tutorial & Surveys Magazine, 2006-2009.*

Conference Organizations

- RFIC Executive Committee members, 2000-2017
- RFIC Steering Committee Member, RFIC symposium, 1996-2017.
- RFIC Founding member, 1995-96.
- Technical Program Chair, IEEE International Sym. on Circuits and Systems, Phoenix, AZ, 2002.
- ISSCC Admin Council, Conferences Committee 2000-2005.
- General Chair, Radio Frequency IC (RFIC) Symposium, Seattle, WA, 2002.
- Technical Program Chair, RFIC Symposium, Phoenix, AZ, 2001.
- Finance Chair, RFIC symposium, Boston, MA, 2000.
- Publicity Chair, RFIC symposium, Los Angeles, CA, 1999.
- Transactions Chair, RFIC symposium, Baltimore, MD, 1998.
- General Chair, Int. Sym. on Low-Power Electronics and Design (ISLPED), Monterey, CA, 97.
- Executive Committee Member, Int. Symp. On Low-Power Electronics and Design, 96-2000.
- Technical Program Committee Member of the following conferences:
 - International Conference on Circuits and Systems: 1996, 2000, 2001, 2004-2008
 - RFIC Symposium, 1996-2018
 - Application Specific Array Processing (ASAP): 2000-2002
 - Technical Program Chair, Int. Sym. on Low-Power Electronics and Design, Monterey, CA, 96.
 - Arizona Telecom Comm (ATIC)
 - GLS VLSI 1998, Lafayette, Louisiana, 1998

Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

- VLSI Design 98, Chennai, India, Jan. 1998.
- ICECS, Lisbon, Portugal, 98.
- Application Specific Array Processing, 1995-97, 2000
- Vehicular Technology Conference, 1995-97.
- Inter. Conf. on Intelligent Information Systems, D.C., 1994-95.
- IEEE Pacific Rim Conference on Communications & Computers, Victoria, BC, Canada, 1991.

Invited talks, Panelist, Session Chairs, Workshop Speaker

- Conference chair, Technical Program committee chair and TPC member, tutorials, workshops, session chair, etc. in RFIC, ISSCC, ISCAS, VLSI, ICASSP, Low-Power Symposium, ICC, Application Specific IC's, IMS, MTT, etc.

CONSULTANT

- Intel Inc. Chandler, AZ, 2002-2006: Development of 3G-4G Wireless transceiver.
- Sony Inc., San Diego, CA and Tokyo, Japan, 2002-2004: Review and development of various telecom cellular system architecture including 3G system architecture, and GPS system.
- Motorola Inc. 2002-2005: Supporting development of BT, WiFi, E911, GPS integrated circuits and systems for the cellular and mobile handsets.
- Hewlett Packard, Corvallis, OR – 1990-1993: Various project on development of custom analog and digital IC's for printer and inkjet system. Some of this work was under consultation, and some under various research grants with Oregon State University.
- Tektronix Inc, Beaverton, OR - 1988-1990: Design and Implementation of Data acquisition system for Spectrum analyzer, development of custom DSP algorithm for the Tektronix spectrum analyzer including system architecture, simulation, analysis, and design of oversampled data acquisition system.
- Boeing Commercial Aircraft, BCAC, Renton, WA - 1985-1987: Development of Airplane Controller Model, Simulation and Implementation of Flight control, Model reduction, and system control.

EXPERT WITNESS (Patent, IP)

Patent litigation, patent validity, IPR, expert reports, deposition, testimony, and trade secrets in the following areas (Complete list of cases available):

- Analog and Digital IC, Radio Frequency Integrated Circuits, Power Management, Power Management IC
- Wireless communication, 3G, 4G, OFDM, WiFi, 802.11, Bluetooth, and related areas
- Communication networks, Signal Processing, Communication system, DSL, xDSL, VDSL, DOCIS MODEM, and related areas.
- Hearing AID, Bio-Electronics, Heart monitoring system, Bi-sensors
- Standards including AMPS, GSM, CDMA, WCDMA, LTE, 1G, 2G, 3G, 4G, BT, WiFi (802.11), DOCIS, and related ITU/ETRI/3G.PPP standards.

Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

- Satellite communications, Satellite Transceiver, ECHO and Multi-path cancelation circuits
- Wireline Communications, MODEM, Digital Subscriber Line, ADSL, VDSL, MODEM
- Wireless LAN, Wi-Fi, 802.11, Bluetooth. ZIGBEE
- GPS system, GPS receiver
- MEMS, Bulk Acoustic Wave Filters, SAW, MEMS resonators, MEMS accelerometer Signal Processing, Communication Systems.

PATENTS, PUBLICATIONS

Patents

1. US-10213134-B2, Wireless in-shoe physical activity monitoring implementation
2. US-10264996-B2, Method and apparatus for wirelessly monitoring repetitive bodily movements
3. US-7528754-B1, Finite impulse response digital to analog converter
4. US-2007033000-A1, Efficient non-iterative frequency domain method and system for nonlinear analysis
5. US-7372333-B2, Monolithic supply-modulated RF power amplifier and DC-DC power converter IC
6. US-2006052988-A1, Compressed vector-based spectral analysis method and system for nonlinear rf blocks
7. US-7218085-B2, Integrated ZVS synchronous buck DC-DC converter with adaptive control
8. US-6661371-B2, Oscillator frequency correction in GPS signal acquisition

Standards Contributions

1. "Spectral Compatibility of ADSL: Frequency Overlap vs. FDM," T1E1, Dec. 97.
2. "Echo Cancellation for G.Lite Universal ADSL," OFDM, Universal ADSL Working Group, Atlanta, GA, Jan 98.
3. "8-bit QAM Constellation effects on reach for universal ADSL," OFDM, Universal ADAL Working Group, Atlanta, GA, Jan 98.
4. "Trellis Code Modulation coding gain for OFDM," Universal ADSL Working Group, Atlanta, GA, Jan 98.
5. "Monte Carlo Modeling and simulation of twisted pair wiring for OFDM," Universal ADAL Working Group, Atlanta, GA, Jan 98.
6. "Overlap Upstream/Downstream spectral allocation for OFDM ADSL ," International Telecommunication Unit, Chicago, March 98.
7. "Echo Cancellation for ADSL OFDM," International Telecommunication Unit, Antwerp, Belgium, 98.
8. "Performance of Echo Cancellation ADSL in OFDM system in the presence of Near End Cross Talk (NEXT)," International Telecommunication Unit, Honolulu, Hawaii, June 98.
9. Presentations and editorials at various XDSL and OFDM standards: ITU, ETSI, UAWG, and T1E1, 97-99.
10. Presentations and editorials at various 3G and 4G and wireless standards including ITU, 3GPPP, 802.11,

Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

BT,

Books

“Design, Modeling and Testing of Data Converters, P Carbone, S Kiaei,” F Xu - 2014 – Springer, © Springer-Verlag Berlin Heidelberg 2014

Refereed Journal Papers

1. Wideband Hybrid Envelope Tracking Modulator With Hysteretic-Controlled Three-Level Switching Converter and Slew-Rate Enhanced Linear Amplifier, P. Mahmoudidaryan; D. Mandal; B. Bakaloglu; S. Kiaei, IEEE Journal of Solid-State Circuits, 2019.
2. Low-Power/Low-Voltage Integrated CMOS Sense Resistor-Free Analog Power/Current Sensor Compatible With High-Voltage Switching DC, AC Converter, S. Singh; D. Mandal; B. Bakaloglu; S. Kiaei IEEE Transactions on Circuits and Systems I, 2019
3. Adaptively Biased Output Cap-Less NMOS LDO With 19 ns Settling Time, D. Mandal; C. Desai; B. Bakaloglu; S. Kiaei, IEEE Transactions on Circuits and Systems II: Express Briefs, 2019
4. Doohwang Chang ; Jennifer N. Kitchen ; Sayfe Kiaei ; Sule Ozev, In-field Recovery of RF Circuits from Wearout Based Performance Degradation, IEEE Transactions on Emerging Topics in Computing, 2018
5. Chengxi Liu ; Debashis Mandal ; Zhao Yao ; Ming Sun ; Jim Todsén ; Brian Johnson ; Sayfe Kiaei; Bertan Bakaloglu, 50 V Isolation, 100 MHz, 50 mW Single-Chip Junction Isolated DC-DC Converter with Self-Tuned Maximum Power Transfer Frequency, IEEE Transactions on Circuits and Systems II, Sept 2018.
6. Chirag Desai; Debashis Mandal; Bertan Bakaloglu; Sayfe Kiaei, “A 1.66 mV FOM Output Cap-Less LDO With Current-Reused Dynamic Biasing and 20 ns Settling Time,” IEEE Solid-State Circuits Letters Year: 2018, Volume: 1, Issue: 2, Pages: 50-53
7. Debashis Mandal ; Chirag Desai ; Bertan Bakaloglu ; Sayfe Kiaei, Adaptively Biased Output Cap-Less NMOS LDO with 19 ns Settling-Time;; IEEE Transactions on Circuits and Systems II: Feb 2019
8. Ayati, Mandal, Bakaloglu, Kiaei, “Integrated Quasi-Circulator With RF Leakage Cancellation for Full-Duplex Wireless Transceivers,”, IEEE Trans of Microwave theory and techniques, Dec 2017.
9. “A 50-mA 99.2% Peak Current Efficiency, 250-ns Settling Time Digital Low-Dropout Regulator With Transient Enhanced PI Controller”, ChaiYong Lim ; Debashis Mandal ; Bertan Bakaloglu ; Sayfe Kiaei; IEEE Transactions on Very Large Scale Integration (VLSI) Systems; Year: 2017, Volume: 25, Issue: 8; Pages: 2360 - 2370
10. Doohwang Chang; Jennifer N. Kitchen; Sayfe Kiaei; “Sule Ozev, In-field Recovery of RF Circuits from Wearout Based Performance Degradation”, IEEE Transactions on Emerging Topics in Computing, 2017.
11. Edgar Martí-Arbona; Debashis Mandal; Bertan Bakaloglu; Sayfe Kiaei, A High-Voltage-Compliant Current-to-Digital Sensor for DC–DC Converters in Standard CMOS Technology, , IEEE Transactions on Power Electronics, 2017, Volume: 32, Issue: 3. Pp. 2180 - 2188
12. Michael Cheah ; Debashis Mandal ; Bertan Bakaloglu ; Sayfe Kiaei, “A 100-mA, 99.11% Current Efficiency, 2-mVpp Ripple Digitally Controlled LDO With Active Ripple Suppression”, Aug 2016.
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15. Chang, D.; Kitchen, J.N.; Bakaloglu, B.; Kiaei, S.; Ozev, S., "Design-Time Reliability Enhancement Using Hotspot Identification for RF Circuits," in *IEEE transactions on Very Large Scale Integration (VLSI) Systems*, -vol. 24, no. 3, pp. 1179-1183, 2016

Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

16. Seungkee Min; Copani, T.; Kiaei, S.; Bakkaloglu, B., "A 90-nm CMOS 5-GHz Ring-Oscillator PLL With Delay-Discriminator-Based Active Phase-Noise Cancellation," *Solid-State Circuits, IEEE Journal of*, vol.48, no.5, pp.1151,1160, May 2013
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18. Seungkee Min; Copali, T.; Kiaei, S.; Bakkaloglu, B.; , "A 90nm CMOS 5GHz ring oscillator PLL with delay-discriminator based active phase noise cancellation," *Radio Frequency Integrated Circuits Symposium (RFIC), 2012 IEEE*, pp. 173-176, 2012
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23. Hyungseok Kim; Junghan Lee; Copani, T.; Bazarjani, S.; Kiaei, S.; Bakkaloglu, B.; , "Adaptive Blocker Rejection Continuous-Time $\Sigma\Delta$ ADC for Mobile WiMAX Applications," *Solid-State Circuits, IEEE Journal of*, vol.44, no.10, pp.2766-2779, Oct. 2009
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27. Wing-Yee Chu; Bakkaloglu, B.; Kiaei, S.; , "A 10 MHz Bandwidth, 2 mV Ripple PA Regulator for CDMA Transmitters," *Solid-State Circuits, IEEE Journal of*, vol.43, no.12, pp.2809-2819, Dec. 2008.
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Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

32. Abedinpour, S.; Bakkaloglu, B.; Kiaei, S.; , "A Multistage Interleaved Synchronous Buck Converter With Integrated Output Filter in 0.18 μm SiGe Process," *Power Electronics, IEEE Transactions on* , vol.22, no.6, pp.2164-2175, Nov. 2007
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34. A Multistage Interleaved Synchronous Buck Converter With Integrated Output Filter in 0.18 micron. , S Abedinpour, B Bakkaloglu, S Kiaei - *Power Electronics, IEEE Transactions on*, Nov. 2007, Volume: 22, pp - 2164-2175
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37. Bandwidth extension technique for polar modulated RF transmitters ; Bakkaloglu, B.; Kiaei, S.; Dwyer, R.; *Electronics Letters*; Volume: 42 Issue: 8 13 April 2006 ; Page(s): 476- 478 ;
38. Frequency modulated bandpass SD chirp synthesizer for sensor applications; Chung, H.H.; Lyles, U.; Copani, T.; Bakkaloglu, B.; Kiaei, S.; *Electronics Letters*; Volume: 42 Issue: 16 August 3, 2006 ; Page(s): 917- 918
39. Radiation Hardened by Design RF Circuits Implemented in 0.13 mm CMOS Technology; Chen, W.; Pouget, V.; Gentry, G. K.; Barnaby, H. J.; Vermeire, B.; Bakkaloglu, B.; Kiaei, K.; Holbert, K. E.; Fouillat, P. ; *Nuclear Science, IEEE Transactions on* ; Volume: 53 Issue: 6 Part=1, Dec. 2006 ; Page(s): 3449-3454 ;
40. Analysis of Single Events Effects on Monolithic PLL Frequency Synthesizers ; Chung, H. H.; Chen, W.; Bakkaloglu, B.; Barnaby, H. J.; Vermeire, B.; Kiaei, S. ; *Nuclear Science, IEEE Transactions on* ; Volume: 53 Issue: 6 Part=1, Dec. 2006 ; Page(s): 3539-3543
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48. *Optimum equalization of multicarrier systems: a unified geometric approach, for OFDM* Lashkarian, N.; Kiaei, S. ; *IEEE Transactions on Communications*, Volume: 49 Issue: 10 , Oct. 2001 Page(s): 1762 – 1769
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Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

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51. *Westgate, C.R.; Gupta, R.K.; Kiaei, S. ; Microwave Theory and Techniques, IEEE Transactions on* , Volume: 46 Issue: 12 Part: 2 , Dec. 1998 ; Page(s): 2180 –2181
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60. "Characterization and Comparison of CMOS FSCL Circuits with Conventional CMOS Logic for Hybrid ICs," *IEEE Trans. on Circuits and Systems*, Sept. 93. [S.H. Chee, S. Kiaei, D. Allstot]
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64. "Adaptive self-correcting D-S Modulators," *IEE Electronics Letters*, Vol. 28, No. 14, pp. 1288-1290, July 92. [S. Abdenadher, S. Kiaei, G. Temes, R. Schreier]
65. "On-line Adaptive Digital Correction of Dual-Quantization Delta-Sigma Modulators," *IEE Electronics Letters*, Vol. 28, No. 16, pp. 1511-1513, July 92.[Y. Yang, R. Schreier, G. Temes, S. Kiaei]
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Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

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Conference Publications

1. 27.5 A 91%-Efficiency Envelope-Tracking Modulator Using Hysteresis-Controlled Three-Level Switching Regulator and Slew-Rate-Enhanced Linear Amplifier for LTE-80MHz Applications P. Mahmoudidaryan; D. Mandal; B. Bakaloglu; S. Kiaei, 2019 IEEE International Solid- State Circuits Conference - (ISSCC), 2019
2. Integrated High-Efficiency Single-Inductor CCM Boost Converter for Multi-Junction PV Energy Harvesting, Q. Peng; D. Mandal; P. Mahmoudidaryan; B. Bakaloglu; S. Kiaei, 2019 IEEE Applied Power Electronics Conference and Exposition (APEC), 2019
3. Sense resistor-free analog power sensor for boost converter with 14.1% gain error and 9.4% offset error, Shrikant Singh ; Debashis Mandal ; Bertan Bakaloglu ; Sayfe Kiaei; 2018 IEEE 9th Latin American Symposium on Circuits & Systems (LASCAS), 2018
4. Ayati, S. A.; Mandal, D.; Bakaloglu, B.; Kiaei, S., "Adaptive Integrated CMOS Circulator," in *IEEE Symposium on Radio Frequency Integrated Circuits (RFIC)*, May 2016
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Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

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Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

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Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

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Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

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Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

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Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

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Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

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Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

GRADUATE STUDENT ADVISEES & RESEARCH PROJECT

(Partial list of Students graduated, current employment to the best of my knowledge)

1. J. Durgam, VLSI Design of Dynamically Reconfigurable Array Processors, MSEE, 1988. Intel.
2. J. Gilbert, Minimization Techniques for PLAs, MSEE, 1988, Tektronix Inc.
3. L. Luo, CCA Methods for ARMA Spectral Estimation, MSEE, 1989. Berkeley Research Center
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Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

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Dr. Sayfe Kiaei
School of Electrical, Computer and Energy Engineering
Arizona State University, Tempe, AZ 85287
Sayfe@asu.edu

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INDUSTRY COMMITTEES

- Arizona Telecommunications and Information Council (ATIC), Board Member
- CAS Fellows Committee (ends December 31, 2006)
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- *Executive Committee, RFIC 2006.*
- *Technical Program Comm, IEEE RFIC 2006.*
- *Executive Committee, Conferences, International Solid State System's Conference.*
- *IEEE CAS Society, VLSI Technical Comm. Member*
- *Editorial Board, IEEE Communications Surveys & Tutorials*
- *Radio Frequency Integrated Circuits- RFIC 2006*
- *IEEE RF Integrated Circuits Conference, Committee Chair for two workshops*
- *International Microwave Symposium, IMS-MTT 2006*
- *Int. Symposium on Circuits and Systems - ISCAS 2006*
- *Wireless Networks & Emerging Technologies, WNET06*
- *Midwest Symposium on Circuits and System*
- *Arizona Governor IT Advisory Committee – GITA*
- *Arizona Telecom – ATIC*

INSTRUCTIONAL SUMMARY

- Digital IC Design, Analog IC Design, Advance CMOS Analog IC, VLSI, RFIC Design
- Wireless Transceiver Design, Wireless Communications, GPS, Telecomm Systems, Digital Communication
- Signal Processing, Advance digital signal processing, Communication, Digital Communication, Digital Audio Processing, Adaptive array processing
- Computer Architecture, Microprocessor System Architecture, Pipeline Array Processing

ATTACHMENT B

Date	Case Title	Case Number
2017-2019	<i>Red Rock Analytics, LLC v. Samsung Electronics Co. Ltd. et al.</i>	Case No. 2:17-cv-00101-RWS-RSP (E.D. Tex.)
2018-2019	<i>Interactive ToyBox, LLC v. Disney Store USA, LLC et al.</i>	Case No. 1:18-cv-00819 (W.D. Tex.)
2016-2017	<i>Theta IP, LLC v. Samsung Electronics Co., Ltd. et al.</i>	Case No. 2:16-cv-00527-JRG-RSP (E.D. Tex.)
2016-2017	<i>Cisco Systems, Inc. v. TQ Delta, LLC</i>	Case No. IPR2016-01760 (P.T.A.B.) Case No. IPR2016-01466 (P.T.A.B.) Case Nos. IPR2016-01006; -01007; -01008; -01009 (P.T.A.B.)
2016-2017	<i>K/S HIMPP v. III HOLDINGS 4, LLC</i>	Case No. IPR2017-00367 (P.T.A.B.)
2015-2016	<i>Wearable Activity Tracking Devices, Systems, and Components Thereof</i>	Inv. No. 337-TA-973 (U.S.I.T.C.)
2015-2016	<i>Samsung Electronics Co., Ltd. v. IXI IP, LLC</i>	Case No. IPR2015-01445 (P.T.A.B.) Case No. IPR2015-01446 (P.T.A.B.)