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FILE HISTORY

US 6,580,122

PATENT: 6,580,122

INVENTORS: Wristers, Derick J.
Cheek, Jon D.
Pellerin, John G.

TITLE: Transistor device having an enhanced
width dimension and a method of making
same

APPLICATION NO: US2001812521A

FILED: 20 MAR 2001

ISSUED: 17 JUN 2003

COMPILED: 17 JAN 2020

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J1033 U.S. PTO

09/812521



257	330
Class	Subclass
ISSUE CLASSIFICATION	

 PATENT NUMBER
6580122

 6580122

U.S. UTILITY Patent Application

O.I.P.E. SCANNED <i>HKM</i> Q.A. <i>KC</i>	PATENT DATE JUN 17 2003
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APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/812521		<i>438</i>	<i>301</i>	<i>2812</i>	<i>Pompey</i>

APPLICANTS

 Don't know
 Tom Cheab
 John Bell...

TITLE

 Title: ...
 OR ...
PTO-2040
12/99

ISSUING CLASSIFICATION							
ORIGINAL		CROSS REFERENCE(S)					
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)				
<i>257</i>	<i>330</i>	<i>257</i>	<i>332</i>	<i>374</i>			
INTERNATIONAL CLASSIFICATION		<i>438</i>	<i>270</i>	<i>259</i>	<i>589</i>		
<i>H01L</i>	<i>29/76,94</i>						
<i>H01L</i>	<i>31/062,113,19</i>						
<i>H01L</i>	<i>21/336</i>						
<i>H01L</i>	<i>21/3205</i>						
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*5.12.03**Pompey Drawings (5 sheets)**3.20.01*

<input type="checkbox"/> TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg. <i>5</i>	Figs. Drwg. <i>10</i>	Print Fig. <i>7A, 7B</i>	Total Claims <i>34</i>	Print Claim for O.G. <i>1</i>
<input type="checkbox"/> The term of this patent subsequent to _____ (date) has been disclaimed.	<i>Ron Pompey</i> (Assistant Examiner)			NOTICE OF ALLOWANCE MAILED	
<input type="checkbox"/> The term of this patent shall not extend beyond the expiration date of U.S. Patent. No. _____	<i>John F. Niebling</i> Supervisory Patent Examiner Technology Center 2800 <i>3/16/03</i> (Primary Examiner)			<i>3/11/03</i> ISSUE FEE <i>6R</i>	
<input type="checkbox"/> The terminal _____ months of this patent have been disclaimed.	<i>3-18-03</i> (Legal Instruments Examiner)			Amount Due <i>1300</i>	Date Paid <i>4.15.03</i>
			ISSUE BATCH NUMBER		

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6,580,122

**TRANSISTOR DEVICE HAVING AN ENHANCED WIDTH DIMENSION
AND A METHOD OF MAKING SAME**

Transaction History

Date	Transaction Description
03-20-2001	Workflow - Drawings Finished
03-20-2001	Workflow - Drawings Matched with File at Contractor
03-20-2001	Initial Exam Team nn
04-05-2001	IFW Scan & PACR Auto Security Review
05-02-2001	Correspondence Address Change
05-30-2001	Application Dispatched from OIPE
06-24-2001	Case Docketed to Examiner in GAU
08-08-2001	Change in Power of Attorney (May Include Associate POA)
08-08-2001	Change in Power of Attorney (May Include Associate POA)
06-17-2002	Restriction/Election Requirement
06-18-2002	Mail Restriction Requirement
07-08-2002	Response to Election / Restriction Filed
07-23-2002	Date Forwarded to Examiner
09-23-2002	Non-Final Rejection
09-25-2002	Mail Non-Final Rejection
02-03-2003	Response after Non-Final Action
02-03-2003	Request for Extension of Time - Granted
02-03-2003	Affidavit(s) (Rule 131 or 132) or Exhibit(s) Received
02-11-2003	Date Forwarded to Examiner
03-10-2003	Notice of Allowance Data Verification Completed
03-10-2003	Case Docketed to Examiner in GAU
03-11-2003	Mail Notice of Allowance
03-24-2003	Receipt into Pubs
03-26-2003	Workflow - File Sent to Contractor
04-09-2003	Issue Fee Payment Verified
04-15-2003	Issue Fee Payment Received
05-09-2003	Receipt into Pubs
05-12-2003	Application Is Considered Ready for Issue
05-14-2003	Receipt into Pubs
05-29-2003	Issue Notification Mailed
06-17-2003	Recordation of Patent Grant Mailed
06-17-2003	Patent Issue Date Used in PTA Calculation

PATENT APPLICATION



09812521

11033 U.S. PTO

09/812521



03/20/01

INITIALS APR 2001 29

CONTENTS

Date Received
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Date Received
(Incl. C. of M.)
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Date Mailed

1. Application 5 papers.

2. Rev. Power of Atty

6-22-01

3. Notice of Acceptance

8-9-01

4. Restriction

6/13/02

5. Electron

7/8/02

6. non final reg

9/18/02

7. Change of Address

10-28-02

8. Declaration

2/3/03 plm

9. Response / ext 11

2/3/03 1/27

10. allowance / amdt A

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IPR2020-01003

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ISSUE SLIP STAPLE AREA (for additional cross references)

POSITION	INITIALS	ID NO.	DATE
FEE DETERMINATION	Boua/Hay	21	23-22-01
O.I.P.E. CLASSIFIER			4/20/01
FORMALITY REVIEW	MW	920	05-29-01
RESPONSE FORMALITY REVIEW			

INDEX OF CLAIMS

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Claim	Date
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SEARCHED			
Class	Sub.	Date	Exmr.
257	283	9-19-02	RD
	330	↓	
	332		
	374		
438	270		
	259		
	589	✓	
updated	search	3-6-03	RD

SEARCH NOTES (INCLUDING SEARCH STRATEGY)		
	Date	Exmr.

INTERFERENCE SEARCHED			
Class	Sub.	Date	Exmr.
257	283	-8-03	20
	330		
	332		
	374		
438	270		
	259		
	589		

SMIC Ex. 1012
IPR2020-01003
Page 7 of 126

CLIPPEDIMAGE= JP02001036048A

PAT-NO: JP02001036048A

DOCUMENT-IDENTIFIER: JP 2001036048 A

TITLE: SEMICONDUCTOR MEMORY AND MANUFACTURE
THEREOF

PUBN-DATE: February 9, 2001

INVENTOR-INFORMATION:

NAME	COUNTRY
FUKATSU, SHIGEMITSU	N/A

ASSIGNEE-INFORMATION:

NAME	COUNTRY
DENSO CORP	N/A

APPL-NO: JP11203563

APPL-DATE: July 16, 1999

INT-CL (IPC): H01L027/115;H01L027/10 ;H01L021/8247
;H01L029/788 ;H01L029/792

ABSTRACT:

PROBLEM TO BE SOLVED: To provide a semiconductor

memory which can be increased in write, erase, and read speed and also provide a method for manufacturing such a memory.

SOLUTION: An element isolation layer 3a is formed thinner than the depth of a recess 2, so that a recess may still be left over in the recess 2, after the element isolation layer 3a is formed. A floating gate 5 and a control gate 7 are formed deeper into the recess. Thereby, the floating gate 5 and the control gate 7 can be made longer by the depth of the recess. Accordingly, the write, erase, and read speed can be increased.

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US006580122B1

(12) **United States Patent**
Wristers et al.

(10) **Patent No.:** **US 6,580,122 B1**
(45) **Date of Patent:** **Jun. 17, 2003**

(54) **TRANSISTOR DEVICE HAVING AN ENHANCED WIDTH DIMENSION AND A METHOD OF MAKING SAME**

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6,277,697 B1 * 8/2001 Lee
6,376,313 B1 * 4/2002 Goebel et al.

(75) **Inventors:** **Derick J. Wristers**, Bee Caves, TX (US); **Jon D. Cheek**, Round Rock, TX (US); **John G. Pellerin**, Austin, TX (US)

(73) **Assignee:** **Advanced Micro Devices, Inc.**, Austin, TX (US)

(*) **Notice:** Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) **Appl. No.:** **09/812,521**
(22) **Filed:** **Mar. 20, 2001**

(51) **Int. Cl.⁷** **H01L 29/76; H01L 29/94; H01L 31/062; H01L 31/113; H01L 31/119; H01L 21/336; H01L 21/3205**
(52) **U.S. Cl.** **257/330; 257/332; 257/374; 438/270; 438/259; 438/589**
(58) **Field of Search** **257/283, 330, 257/332, 374; 438/270, 259, 589**

(56) **References Cited**
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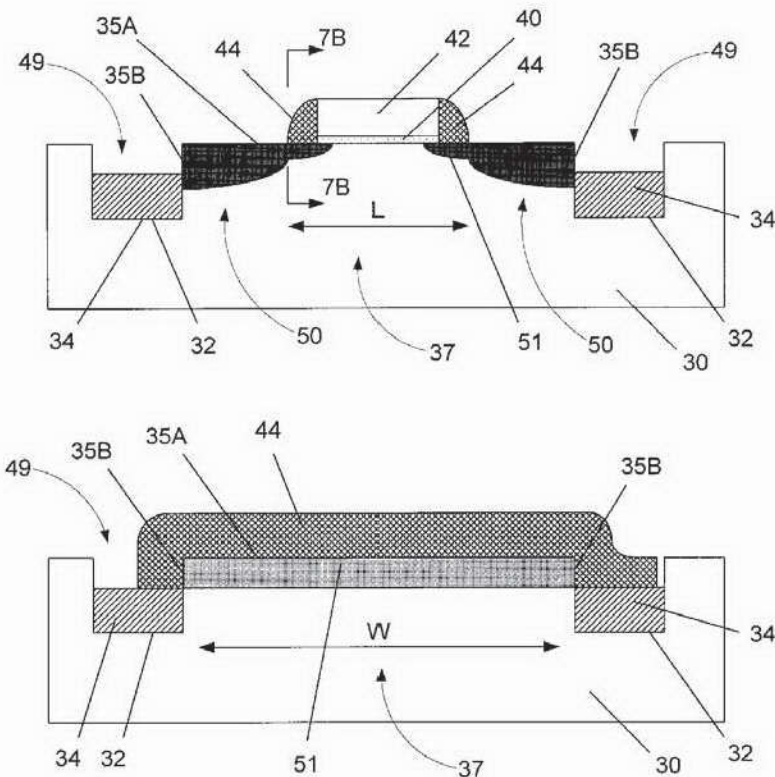
FOREIGN PATENT DOCUMENTS
JP 2001036048 * 7/1999
* cited by examiner

Primary Examiner—John F. Niebling
Assistant Examiner—Ron Pompey
(74) *Attorney, Agent, or Firm*—Williams, Morgan & Amerson

(57) **ABSTRACT**

The present invention is directed to a transistor having an enhanced width dimension and a method of making same. In one illustrative embodiment, the transistor comprises a semiconducting substrate, a recessed isolation structure formed in the substrate, the isolation structure defining a recess thereabove, a gate electrode and a gate insulation layer positioned above the substrate, a portion of the gate electrode and the gate insulation layer extending into the recess above the recessed isolation structure, and a source region and a drain region formed in the substrate. In another illustrative embodiment, the transistor comprises a semiconducting substrate, a recessed isolation structure that defines an active area having an upper surface and an exposed sidewall surface, a gate insulation layer and a gate electrode positioned above a portion of the upper surface and a portion of the exposed sidewall surface of the active area, and a source region and a drain region formed in the active area.

34 Claims, 5 Drawing Sheets



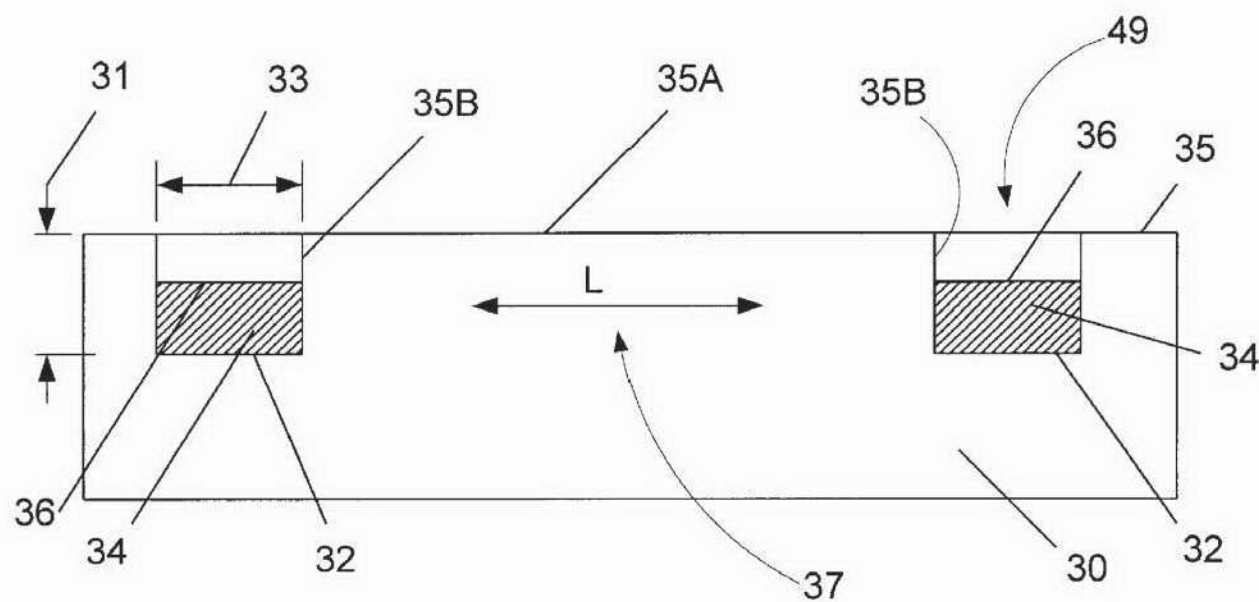


Figure 3

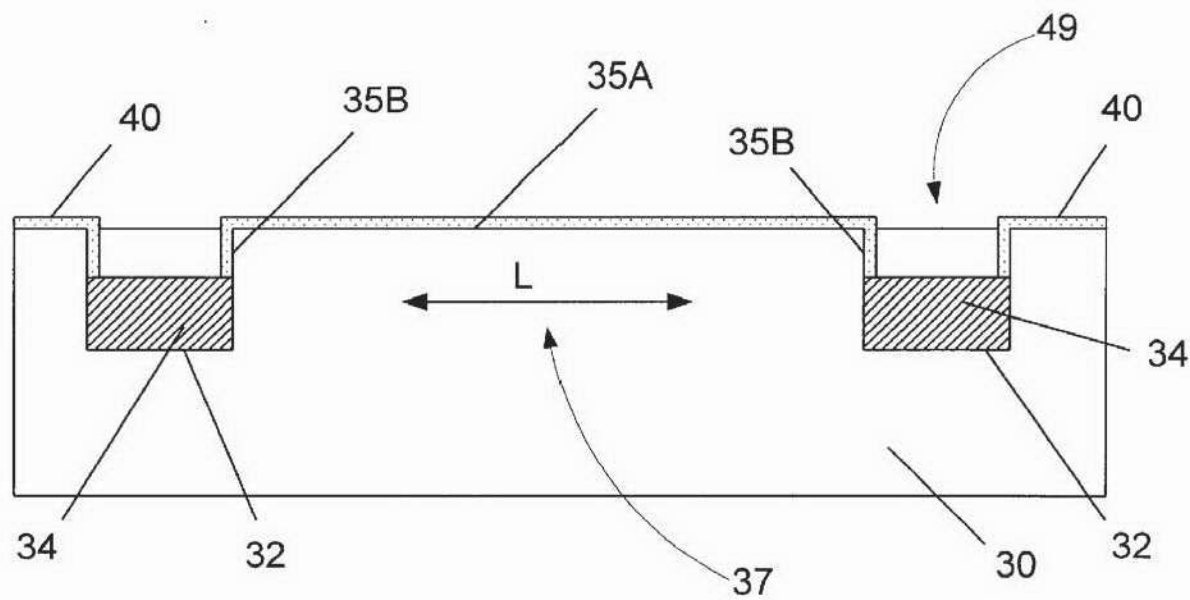


Figure 4

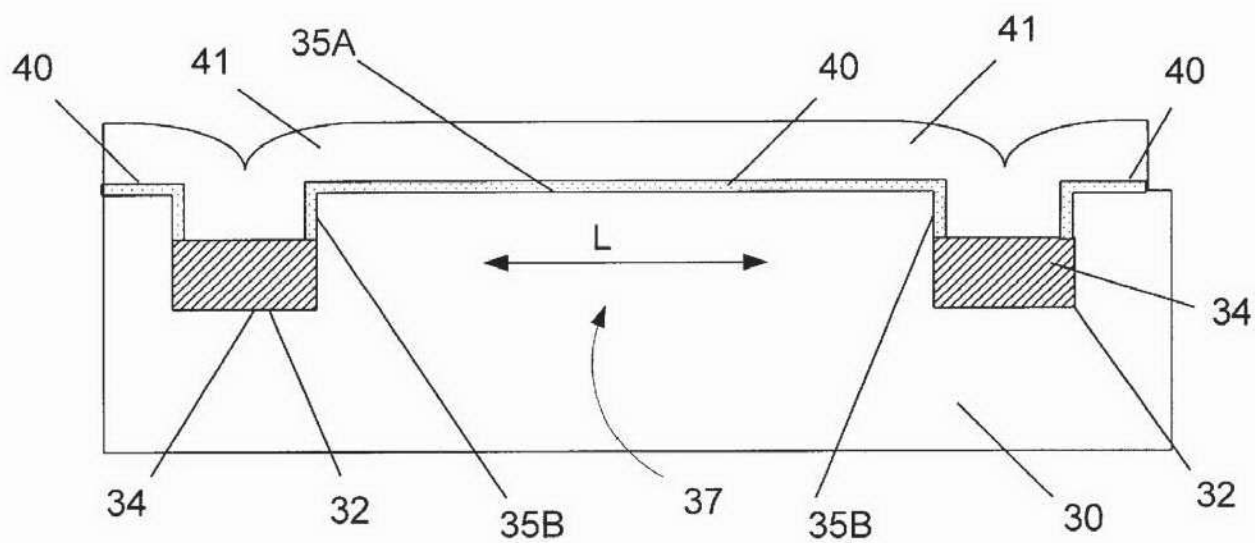


Figure 5

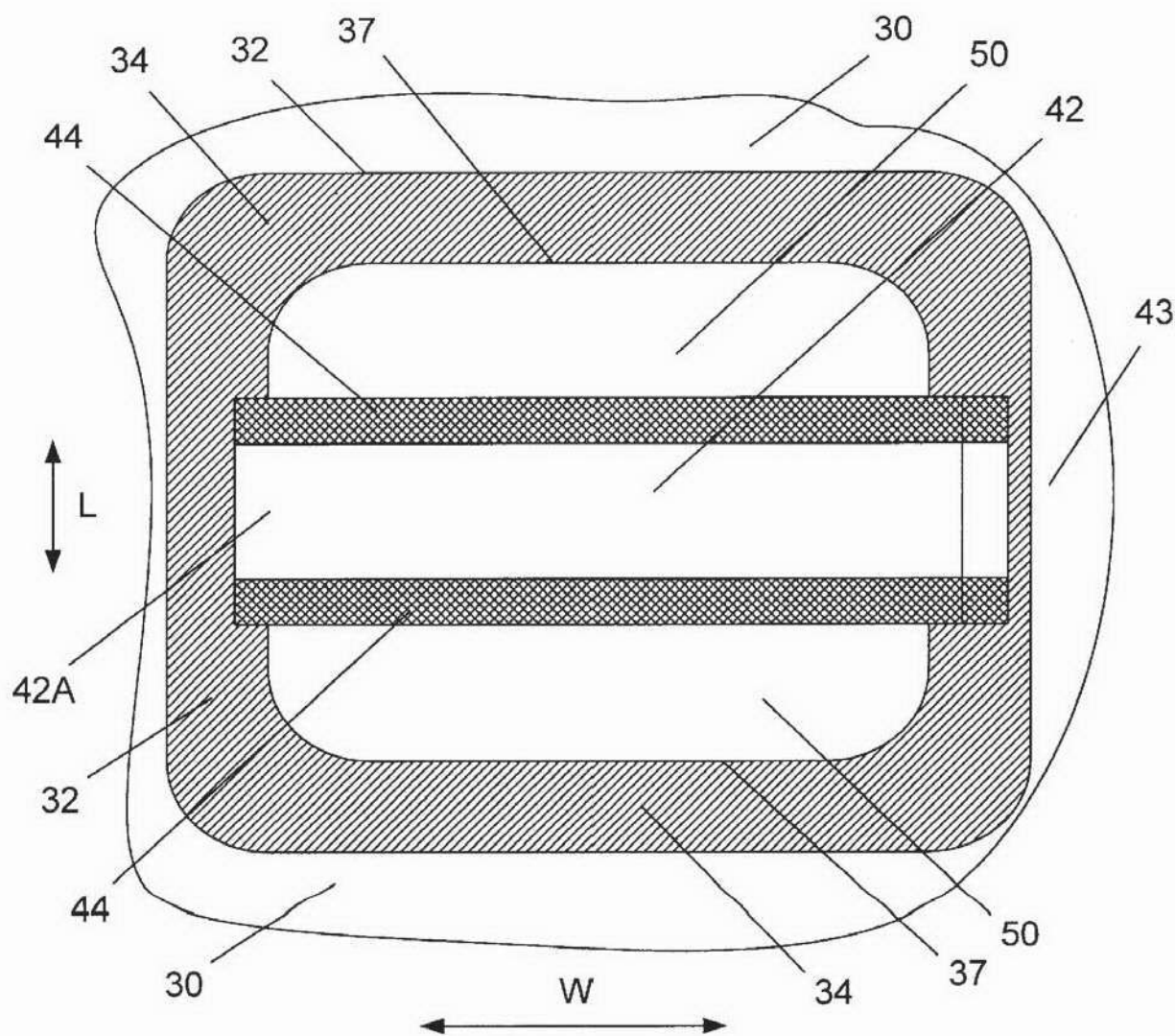


Figure 7C

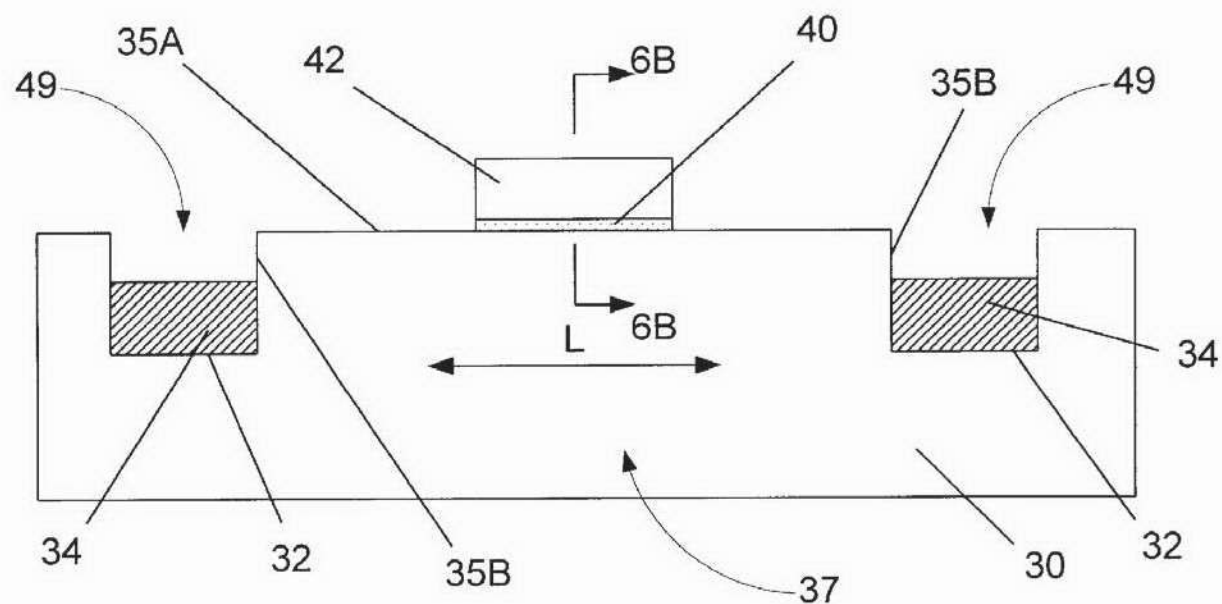


Figure 6A

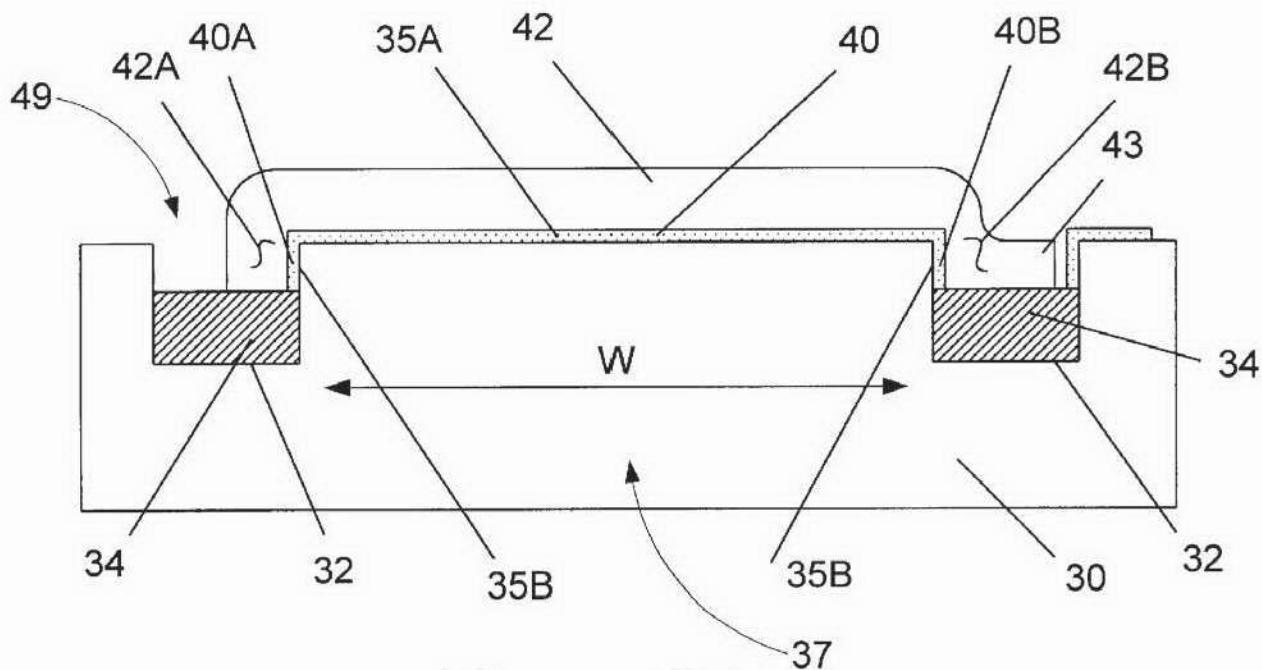


Figure 6B

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TRANSISTOR DEVICE HAVING AN ENHANCED WIDTH DIMENSION AND A METHOD OF MAKING SAME

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention is generally directed to semiconductor devices and processing, and, more particularly, to a novel semiconductor device having an enhanced width dimension and a method of making same.

2. DESCRIPTION OF THE RELATED ART

There is a constant drive within the semiconductor industry to increase the operating speed of integrated circuit devices, e.g., microprocessors, memory devices, etc. This drive is fueled by consumer demands for computers and electronic devices that operate at increasingly greater speeds. This demand for increased speed has resulted in a continual reduction in the size of semiconductor devices, e.g., transistors. That is, the size of many components of a typical field effect transistor, e.g., channel length, source/drain junction depths, gate dielectric thickness, etc., are reduced. For example, all other things being equal, the smaller the channel length of the transistor, the faster the transistor will operate. Thus, there is a constant drive to reduce the size, or scale, of the components of a typical transistor to increase the overall speed of the transistor, as well as integrated circuit devices incorporating such transistors.

By way of background, FIG. 1 and FIG. 2 depict an illustrative transistor 10 for purposes of explaining one or more problems that may be solved or reduced by the present invention. FIG. 1 is a cross-sectional front view of the transistor 10 showing the channel length or transistor length "L." FIG. 2 is a cross-sectional side view of the transistor 10 shown in FIG. 1 taken along the line "2—2," i.e., showing the transistor width "W." As shown in FIG. 1, the transistor 10 is formed in an active area 12 that is defined in a semiconducting substrate 14 by an isolation structure 16 formed therein. The transistor 10 is comprised of a gate insulation layer 18, a gate electrode 20, a sidewall spacer 24, and a plurality of source/drain regions 28. The transistor 10 is also comprised of metal silicide layers 29 formed above the source/drain regions 28 and the gate electrode 20.

All of the various components of the transistor 10 depicted in FIG. 1 may be formed using a variety of known processing techniques, and they may be comprised of a variety of materials. For example, the gate insulation layer 18 may be comprised of a thermally grown layer of silicon dioxide, the gate electrode 20 may be comprised of polysilicon, the sidewall spacer 24 may be comprised of silicon dioxide, and the metal silicide regions 29 may be comprised of, for example, cobalt silicide or titanium silicide. The isolation structure 16 is typically comprised of an insulating material, such as silicon dioxide, or other like material. The isolation structure 16 may be constructed by forming a trench 17 in the substrate 14, filling the trench with an appropriate insulating material, e.g., silicon dioxide, and, thereafter, performing a chemical mechanical polishing operation to remove any excess material.

In designing modern integrated circuit devices, one parameter of a transistor that is of particular importance is known as its drive current. Stated simply, the drive current of a transistor is the amount of current flowing from the drain region to the source region of a transistor. All other things being equal, it is desirable that transistors have as

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large a drive current as possible without otherwise adversely impacting the performance of the transistor, i.e., without generating excessive heat or excessive off-state leakage currents, etc.

The drive current of the device may be increased by reducing the channel length of the transistor. However, all other things being equal, the smaller the channel length of the transistor, the greater the off-state leakage current. Moreover, the off-state leakage current increases exponentially as the channel length of the device decreases. Off-state leakage currents also increase as the transistor width increases, but at a rate that is less than the exponential rate associated with reductions in the channel length of a device. Thus, in attempting to increase the drive current of a transistor, increasing the width of the transistor results in lower off-state leakage currents, as compared to increasing the drive current the same amount by reducing the channel length. Moreover, to a great extent, reducing the channel length of the device is limited by available photolithography and etching processes.

Typically, the amount of drive current that can be generated per unit width ("w") of the transistor is a known value. Thus, when a total drive current is desired or required for a particular circuit application, the required width of the transistor to accomplish this purpose may be readily determined. Thus, for a given type of transistor, an application requiring a transistor having a width of 30 w may be satisfied by a single transistor having a width of approximately 30 w or six transistors, arranged in parallel, each having a width of approximately 5 w. Using this process, the layout of integrated circuit devices across the surface of a portion of a semiconducting substrate is accomplished, with the ultimate goal being to minimize consumption of wafer plot space, i.e., to maximize the use of available substrate. Thus, it would be desirable to have a transistor in which the width dimension of a substrate can be maximized in a given plot space of semiconducting substrate.

The present invention is directed to a method that solves or reduces some or all of the aforementioned problems.

SUMMARY OF THE INVENTION

The present invention is directed to a transistor having an enhanced width dimension and a method of making same. In one illustrative embodiment, the transistor comprises a semiconducting substrate, a recessed isolation structure formed in the substrate, the isolation structure defining a recess thereabove, a gate electrode and a gate insulation layer positioned above the substrate, a portion of the gate electrode and the gate insulation layer extending into the recess above the recessed isolation structure, and a source region and a drain region formed in the substrate. In another illustrative embodiment, the transistor comprises a semiconducting substrate, a recessed isolation structure that defines an active area having an upper surface and an exposed sidewall surface, a gate insulation layer and a gate electrode positioned above a portion of the upper surface and a portion of the exposed sidewall surface of the active area, and a source region and a drain region formed in the active area.

In one illustrative embodiment, the method of making a transistor comprises providing a semiconducting substrate, forming a recessed isolation structure in a trench formed in the substrate, the recessed isolation structure thereby defining a recess in the substrate, forming a gate insulation layer and a gate electrode above the substrate, a portion of the gate insulation layer and gate electrode extending into the recess in the substrate and above the recessed isolation structure,

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and forming a plurality of source/drain regions in the substrate adjacent the gate electrode.

BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

FIG. 1 is a cross-sectional front view of an illustrative prior art transistor in the transistor length direction;

FIG. 2 is a cross-sectional side view of the prior art transistor shown in FIG. 1 along the line "2—2";

FIG. 3 is a cross-sectional front view of a partially formed transistor in accordance with one illustrative embodiment of the present invention;

FIG. 4 is a cross-sectional front view of the device shown in FIG. 3 after a gate insulation layer has been formed thereabove;

FIG. 5 is a cross-sectional front view of the device shown in FIG. 4 after a layer of polysilicon has been formed thereabove;

FIG. 6A is a cross-sectional front view of the device shown in FIG. 5 after a gate electrode has been patterned from the layer of polysilicon;

FIG. 6B is a cross-sectional side view, in the transistor width direction, of the device shown in FIG. 6A taken along the line "6B—6B";

FIG. 7A is a cross-sectional front view of the device shown in FIG. 6A after source/drain regions have been formed on the device;

FIG. 7B is a cross-sectional side view, in the transistor width direction, of the device shown in FIG. 7A taken along the line "7B—7B"; and

FIG. 7C is a plan view of the device shown in FIG. 7A.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The present invention will now be described with reference to the attached figures. Although the various regions and structures of a semiconductor device are depicted in the drawings as having very precise, sharp configurations and profiles, those skilled in the art recognize that, in reality,

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these regions and structures are not as precise as indicated in the drawings. Additionally, the relative sizes of the various features depicted in the drawings may be exaggerated or reduced as compared to the size of those features or regions on fabricated devices. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present invention. As will be readily apparent to those skilled in the art upon a complete reading of the present application, the present method is applicable to a variety of technologies, e.g., NMOS, PMOS, CMOS, etc., is readily applicable to a variety of devices, including, but not limited to, logic devices, memory devices, etc.

In general, the present invention is directed to a transistor device having an enhanced width dimension and a method of making same. As will be recognized after a complete reading of the present application, the present invention provides a method to maximize the width of a transistor in a given plot space of semiconducting substrate. In turn, integrated circuit devices incorporating such transistors may be more efficient in terms of plot spacer consumption.

As shown in FIG. 3, a trench 32 is formed in a semiconducting substrate 30. For reference, the transistor length direction "L" is also shown in FIG. 1. A recessed isolation material 34, comprised of materials such as silicon dioxide, silicon oxynitride, etc., is formed in the trench 32. The width 33 and the depth 31 of the trench 32 may be varied as a matter of design choice. In one embodiment, the depth 31 of the trench 32 ranges from approximately 3000–6000 Å. The width 33 of the trench 32 may vary from a minimum of the smallest feature size that can be patterned using existing photolithography and etching techniques, up to any desired width. In one illustrative embodiment, the width 33 of the trench 32 ranges from approximately 2000–3000 Å.

The recessed isolation material 34 may be formed in the trench 32 by a variety of techniques. In one illustrative embodiment, a layer of insulating material (not shown) is blanket deposited above the surface 35 of the substrate 30 and in the trench 32. Thereafter, a chemical mechanical polishing operation is performed on the layer of insulating material such that the insulating material in the trench 32 is approximately planar (not shown) with the surface 35 of the substrate 30. An etching process, such as a wet etching process, may then be performed to reduce the level of insulating material 34 in the trench 32 to the level depicted in FIG. 3. In one illustrative embodiment, the insulating material 34 is removed until such time as a surface 36 of the isolation material 34 in the trench 32 is positioned approximately 1000–1500 Å beneath the surface 35 of the substrate 30. This process results in the definition of an active island 37 of substrate material having an exposed upper surface 35A and an exposed sidewall surface 35B. The island 37 of substrate material may be of any desired shape, i.e., circular, oval, rectangular, etc. This process also results in the definition of a recess 49 in the substrate 30 above the recessed isolation material 34. In the disclosed embodiment, the recess 49 has a depth of approximately 1000–1500 Å.

Thereafter, one or more channel doping operations are performed at this stage of manufacturing. For example, in one illustrative embodiment, a threshold voltage implant process is performed on the device. This may be accomplished by performing a four-way angled channel implant process wherein each of the angled implants are spaced approximately 90 degrees apart with respect to one another. In one illustrative embodiment, this threshold voltage implant may be accomplished by a four-way angled implant process performed at an implant angle of approximately 30–50 degrees (with respect to a line perpendicular to the

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surface 35 of the substrate 30) using dopant atoms at a concentration ranging from approximately $1\text{--}3\times 10^{12}$ ions/cm² per rotation. For an NMOS device, boron may be implanted during the threshold voltage implant step at an energy level ranging from approximately 10–15 keV. For a PMOS device, such a threshold voltage implant may be performed using phosphorous at an energy level ranging from approximately 90–110 keV. Additional channel doping implantation processes may be performed at this time if desired or required by the device under construction.

Thereafter, as shown in FIG. 4, a gate insulation layer 40 for the transistor 10 is formed for the device. The gate insulation layer 40 may be formed from a variety of materials, such as silicon dioxide, silicon oxynitride, silicon nitride, or any dielectric material having a dielectric constant less than approximately four. The gate insulation layer 40 may be formed by a variety of processes, e.g., chemical vapor deposition (CVD), thermal growth, etc. In one illustrative embodiment, as shown in FIG. 4, the gate insulation layer 40 is comprised of a thermally grown layer of silicon dioxide having a thickness ranging from approximately 20–50 Å.

Next, as shown in FIG. 5, a layer of polysilicon 41 is blanket deposited above the gate insulation layer 40 and above the recessed isolation material 34. The layer of polysilicon 41 may be formed by a variety of techniques, e.g., chemical vapor deposition, low pressure chemical vapor deposition, etc. In one illustrative embodiment, the layer of polysilicon 41 has a thickness ranging from approximately 1000–2000 Å, and it is formed by conformally depositing the layer of polysilicon 41 using a chemical vapor deposition process.

Next, as shown in FIG. 6A, using traditional photolithography and one or more etching processes, a gate electrode 42 is patterned from the layer of polysilicon 41. The gate insulation layer 40 may also be patterned at this time, as shown in FIG. 6A. FIG. 6B is a side view of the structure depicted in FIG. 6A taken along the line “6B–6B.” That is, FIG. 6B is a cross-sectional view of the device in the transistor width dimension “W.” As shown therein, a portion 43 of the gate electrode 42 extends beyond the isolation structure 34. The portion 43 of the gate electrode 42 is coupled to a power supply (not shown) so that a voltage may be applied to the gate electrode 42.

Then, halo implant regions (not shown) are formed in the device by performing a four-way angled halo implant process. Each of the angled implant processes are performed at an angle ranging from approximately 30–45 degrees with respect to a line generally perpendicular to the surface 35 of the substrate 30, and at a concentration level ranging from approximately $1\text{--}6\times 10^{13}$ ions/cm² total (for all four rotations). In an illustrative NMOS device, boron atoms may be implanted at an energy level ranging from approximately 7–15 keV. In an illustrative PMOS device, arsenic may be implanted during this halo implant process at an energy level ranging from approximately 40–65 keV.

Thereafter, source and drain regions 50 for the device may be formed using a variety of process flows. FIGS. 7A and 7B (side view taken along the line “7B–7B” in FIG. 7A) depict the transistor after the source/drain regions 50 have been formed. FIG. 7C is a plan view of the device shown in FIG. 7A. In one illustrative embodiment, a source/drain extension implant process is performed to form source/drain extensions 51 of the completed device. This extension implantation process may be performed at a relatively low energy level and at a relatively high concentration of dopant atoms.

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For example, the concentration of dopant atoms in the extension implant process may vary from approximately 1×10^{14} to 2×10^{15} ions/cm² of the appropriate dopant atoms, e.g., arsenic (As) or phosphorous (P) for NMOS technology, boron (B) or boron difluoride (BF₂) for PMOS technology, etc. The energy level for the extension implant process will vary depending upon the dopant material used in the process. For example, in one illustrative embodiment for forming the source/drain extension implants in an NMOS device, the extension implantation process is performed using arsenic as the dopant atoms at a concentration ranging from approximately 6×10^{14} to 2×10^{15} ions/cm² and at an energy level ranging from approximately 3–15 keV. Typically, the extension implant process will result in implant regions in the substrate that are generally self-aligned with respect to the gate electrode 42 (as implanted). However, for a PMOS device, a small sidewall spacer (not shown) may be formed adjacent the gate electrode 42 prior to performing the extension implant step. This spacer is used in PMOS devices due to the increased mobility of the dopant atoms that may be implanted, e.g., boron.

Next, as indicated in FIGS. 7A–7C, a sidewall spacer 44 is formed adjacent the gate electrode 42. The sidewall spacer 44 is formed by depositing a layer (not shown) of spacer material above the surface of the device and thereafter performing an anisotropic etching process to define the spacer 44. The layer of spacer material may be comprised of a variety of materials, such as silicon dioxide, silicon oxynitride, or other like materials. Moreover, it may be formed by any of a variety of techniques for forming such layers, such as chemical vapor deposition (CVD), physical vapor deposition (PVD), etc.

Next, a source/drain implant process is performed on the device. Note that the source/drain implant process is self-aligned with respect to the sidewall spacer 44. The dopant concentration levels and implant energy for the source/drain implant process may vary. For example, the concentration of dopant atoms in the source/drain implantation process may vary from approximately 5×10^{14} to 5×10^{15} ions/cm² of the appropriate dopant atoms, e.g., arsenic or phosphorous for NMOS technology, boron for PMOS technology, etc. The energy level for the source/drain implantation process will vary depending upon the dopant material. For example, in one illustrative embodiment for forming the source/drain regions in an NMOS device, the source/drain implantation process is performed using arsenic as the dopant atoms at a concentration of approximately 5×10^{14} to 5×10^{15} ions/cm² and at an energy level ranging from approximately 20–70 keV.

Thereafter, one or more thermal anneal processes is performed to activate the dopant atoms introduced into the substrate 30 during various ion implant processes described above, and to repair the damage to the lattice structure of the semiconducting substrate 30 resulting from the ion implantation processes. In one embodiment, this anneal process may be at a temperature ranging from approximately 1000–1050° C. for a duration of approximately 5–20 seconds in a rapid thermal anneal chamber. Note that during this process, the previously implanted dopant atoms migrate, or move, from their original implanted position. This migration of the dopant atoms is generally isotropic in direction.

As shown in FIGS. 6A, 6B and 7A–7C, the present invention is directed to a novel transistor structure. The gate electrode 42 has first and second ends 42A, 42B, respectively. The first and second ends 42A, 42B, as well as first and second portions 40A, 40B of the gate insulation layer 40 thereunder, are positioned above a portion of the exposed

sidewall 35B of the active area 37. The remainder of the gate electrode 42 is positioned above the surface 35A of the active area 37. In the embodiment depicted in the attached drawings, the first end 42A of the gate electrode 42 is shown as being patterned such that it does not extend beyond the recessed isolation structure 34. Of course, if desired, the first end 42A of the gate electrode 42 may be patterned so as to extend completely beyond the recessed isolation structure 34 in a manner similar to the configuration depicted for the portion 43 of the gate electrode 42 depicted in FIGS. 6B and 7B. Stated another way, the novel transistor structure disclosed herein is comprised of a gate electrode 42 and a gate insulation layer 40 wherein a portion of the gate electrode 42 and the gate insulation layer 40 extends downwardly into a recess 49 in the substrate above a recessed isolation structure 34. In the disclosed embodiment, both ends 42A, 42B of the gate electrode 42 and both portions 40A, 40B of the gate insulation layer 40 extend into the recess 49 above the recessed isolation structure 34.

After the formation of the gate electrode 42, additional insulating material (not shown), e.g., silicon dioxide, BPSG, etc., may be blanket deposited above the device shown in FIGS. 7A and 7B to fill the portions of the recess 49 not filled, or at least partially filled by the downwardly extending portions of the gate electrode 41 and gate insulation layer 40.

The present invention is directed to a transistor having an enhanced width dimension and a method of making same. In one illustrative embodiment, the transistor comprises a semiconducting substrate 30, a recessed isolation structure 34 formed in the substrate 30, the isolation structure 34 defining a recess 49 thereabove, a gate electrode 42 and a gate insulation layer 40 positioned above the substrate 30, a portion of the gate electrode 42 and the gate insulation layer 40 extending into the recess 49 above the recessed isolation structure 49, and a source region 51A and a drain region 51B formed in the substrate 30. In another illustrative embodiment, the transistor comprises a semiconducting substrate 30, a recessed isolation structure 34 that defines an active area 37 having an upper surface 35A and an exposed sidewall surface 35, a gate insulation layer 40 and a gate electrode 42 positioned above a portion of the upper surface 35A and a portion of the exposed sidewall surface 35B of the active area 37, and a source region 51A and a drain region 51B formed in the active area 37.

In one illustrative embodiment, the method of making a transistor comprises providing a semiconducting substrate 30, forming a recessed isolation structure 34 in a trench 32 formed in the substrate 30, the recessed isolation structure 34 thereby defining a recess 49 in the substrate 30, forming a gate insulation layer 40 and a gate electrode 42 above the substrate 30, a portion of the gate insulation layer 40 and gate electrode 42 extending into the recess 49 above the recessed isolation structure 49, and forming a plurality of source/drain regions 51A, 51B in the substrate 30 adjacent the gate electrode.

The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

What is claimed:

1. A transistor, comprising:

a semiconducting substrate;

a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove;

a gate electrode and a gate insulation layer formed above said substrate, a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure; and

a source region and a drain region formed in said substrate.

2. The transistor of claim 1, wherein said semiconducting substrate is comprised of silicon.

3. The transistor of claim 1, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.

4. The transistor of claim 1, wherein said recessed isolation structure has a surface that is positioned approximately 1000–1500 Å below a surface of said substrate.

5. The transistor of claim 1, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000–3000 Å and a depth ranging from approximately 4000–5000 Å.

6. The transistor of claim 1, wherein said gate electrode is comprised of polysilicon.

7. The transistor of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.

8. The transistor of claim 1, wherein said gate electrode has a thickness ranging from approximately 1000–2000 Å.

9. The transistor of claim 1, wherein said gate insulation layer has a thickness ranging from approximately 20–50 Å.

10. The transistor of claim 1, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.

11. The transistor of claim 1, wherein said gate electrode has first and second end portions that extend into said recess.

12. The transistor of claim 11, wherein said first and second end portions extending into said recess are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.

13. A transistor, comprising:

a semiconducting substrate comprised of silicon;

a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove;

a gate electrode comprised of polysilicon and a gate insulation layer formed above said substrate, a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure; and

a source region and a drain region formed in said substrate.

14. The transistor of claim 13, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.

15. The transistor of claim 13, wherein said recessed isolation structure has a surface that is positioned approximately 1000–1500 Å below a surface of said substrate.

16. The transistor of claim 13, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000–3000 Å and a depth ranging from approximately 4000–5000 Å.

17. The transistor of claim 13, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.

18. The transistor of claim 13, wherein said gate electrode has a thickness ranging from approximately 1000–2000 Å.

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19. The transistor of claim 13, wherein said gate insulation layer has a thickness ranging from approximately 20–50 Å.
20. The transistor of claim 13, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.
21. The transistor of claim 13, wherein said gate electrode has first and second end portions that extend into said recess in said substrate.
22. The transistor of claim 21, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.
23. A transistor, comprising:
- a semiconducting substrate;
 - a recessed isolation structure defining an active area having an upper surface and an exposed sidewall surface;
 - a gate insulation layer and a gate electrode positioned above a portion of said upper surface and a portion of said exposed sidewall surface of said active area; and
 - a source region and a drain region formed in said active area.
24. The transistor of claim 23, wherein said semiconducting substrate is comprised of silicon.
25. The transistor of claim 23, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.

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26. The transistor of claim 23, wherein said recessed isolation structure has a surface that is positioned approximately 1000–1500 Å below a surface of said substrate.
27. The transistor of claim 23, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000–3000 Å and a depth ranging from approximately 4000–5000 Å.
28. The transistor of claim 23, wherein said gate electrode is comprised of polysilicon.
29. The transistor of claim 23, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.
30. The transistor of claim 23, wherein said gate electrode has a thickness ranging from approximately 1000–2000 Å.
31. The transistor of claim 23, wherein said gate insulation layer has a thickness ranging from approximately 20–50 Å.
32. The transistor of claim 23, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.
33. The transistor of claim 23, wherein said gate electrode has first and second end portions that extend into a recess in said substrate defined by said recessed isolation structure.
34. The transistor of claim 33, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.

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APPLICANTS Derick J. Wristers, Bee Caves, TX; Jon D. Cheek, Round Rock, TX; John G. Pellerin, Austin, TX; ** CONTINUING DATA ***** ** FOREIGN APPLICATIONS ***** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** 05/29/2001						
Foreign Priority claimed 35 USC 119 (a-d) conditions met Verified and Acknowledged		<input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> yes <input checked="" type="checkbox"/> no <input type="checkbox"/> Met after met Allowance Examiner's Signature Initials	STATE OR COUNTRY TX	SHEETS DRAWING 5	TOTAL CLAIMS 55	INDEPENDENT CLAIMS 5
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TITLE Transistor device having an enhanced width dimension and a method of making same						
FILING FEE RECEIVED 1500	FEES: Authority has been given in Paper No. _____ to charge/credit DEPOSIT ACCOUNT No. _____ for following:			<input type="checkbox"/> All Fees <input type="checkbox"/> 1.16 Fees (Filing) <input type="checkbox"/> 1.17 Fees (Processing Ext. of time) <input type="checkbox"/> 1.18 Fees (Issue) <input type="checkbox"/> Other _____ <input type="checkbox"/> Credit		

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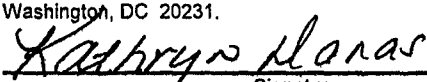
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March 20, 2001

BOX PATENT APPLICATION
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RE: *U.S. Patent Application Entitled: A TRANSISTOR DEVICE HAVING AN ENHANCED WIDTH DIMENSION AND A METHOD OF MAKING SAME - Derick J. Wristers, Jon D. Cheek and John G. Pellerin (2000.065000/TT4203)*

Sir:

Transmitted herewith for filing are:

- (1) 27-page patent specification with 55 claims and an abstract (also Figures 1-7B on 5 sheets);
- (2) Declaration;
- (3) Power of Attorney;
- (4) Assignment and Assignment Cover Sheet; and
- (5) Request and Certification Under 35 U.S.C. 122(b)(2)(B)(i).

All correspondence, notices, official letters and other communications should be directed to J. Mike Amerson, Williams, Morgan & Amerson, P.C., 7676 Hillmont, Suite 250, Houston, TX 77040, and all telephone calls should be directed to J. Mike Amerson at (713) 934-4055.

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Page 2

The Assistant Commissioner is authorized to deduct the amount of the total filing fee (listed below) from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT4203.

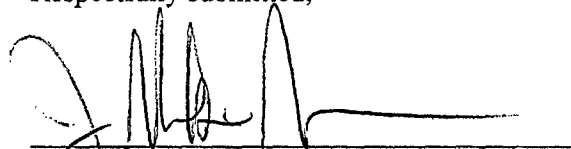
FILING FEE CALCULATION

FOR		Small Entity	Large Entity
Total Claims	55 - 20 = 35	x \$9 = \$	or x \$18 = \$ 630.00
Independent Claims	5 - 3 = 2	x \$40 = \$	or x \$80 = \$ 160.00
Multiple Dependent Claim(s)		+ \$135 = \$	or + \$270 = \$ 0.00
Basic Fee:		+ \$355 = \$	or + \$710 = \$ 710.00
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TOTAL FILING FEES		\$ 0.00	\$1,540.00

Pursuant to 37 C.F.R. § 1.10 the Applicants request the Patent and Trademark Office to accept this application and accord a serial number and filing date as of the date this application is deposited with the U.S. Postal Service for Express Mail.

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Respectfully submitted,



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Application for United States Letters Patent
for
A TRANSISTOR DEVICE HAVING AN ENHANCED WIDTH
DIMENSION AND A METHOD OF MAKING SAME

by
Derick J. Wristers
Jon D. Cheek
John G. Pellerin

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A TRANSISTOR DEVICE HAVING AN ENHANCED WIDTH DIMENSION AND A METHOD OF MAKING SAME

BACKGROUND OF THE INVENTION

1. FIELD OF THE INVENTION

The present invention is generally directed to semiconductor devices and processing, and, more particularly, to a novel semiconductor device having an enhanced width dimension and a method of making same.

2. DESCRIPTION OF THE RELATED ART

There is a constant drive within the semiconductor industry to increase the operating speed of integrated circuit devices, *e.g.*, microprocessors, memory devices, etc. This drive is fueled by consumer demands for computers and electronic devices that operate at increasingly greater speeds. This demand for increased speed has resulted in a continual reduction in the size of semiconductor devices, *e.g.*, transistors. That is, the size of many components of a typical field effect transistor, *e.g.*, channel length, source/drain junction depths, gate dielectric thickness, etc., are reduced. For example, all other things being equal, the smaller the channel length of the transistor, the faster the transistor will operate. Thus, there is a constant drive to reduce the size, or scale, of the components of a typical transistor to increase the overall speed of the transistor, as well as integrated circuit devices incorporating such transistors.

By way of background, Figure 1 and Figure 2 depict an illustrative transistor 10 for purposes of explaining one or more problems that may be solved or reduced by the present invention. Figure 1 is a cross-sectional front view of the transistor 10 showing the channel length or transistor length "L." Figure 2 is a cross-sectional side view of the transistor 10

shown in Figure 1 taken along the line "2-2," *i.e.*, showing the transistor width "W." As shown in Figure 1, the transistor 10 is formed in an active area 12 that is defined in a semiconducting substrate 14 by an isolation structure 16 formed therein. The transistor 10 is comprised of a gate insulation layer 18, a gate electrode 20, a sidewall spacer 24, and a plurality of source/drain regions 28. The transistor 10 is also comprised of metal silicide layers 29 formed above the source/drain regions 28 and the gate electrode 20.

All of the various components of the transistor 10 depicted in Figure 1 may be formed using a variety of known processing techniques, and they may be comprised of a variety of materials. For example, the gate insulation layer 18 may be comprised of a thermally grown layer of silicon dioxide, the gate electrode 20 may be comprised of polysilicon, the sidewall spacer 24 may be comprised of silicon dioxide, and the metal silicide regions 29 may be comprised of, for example, cobalt silicide or titanium silicide. The isolation structure 16 is typically comprised of an insulating material, such as silicon dioxide, or other like material. The isolation structure 16 may be constructed by forming a trench 17 in the substrate 14, filling the trench with an appropriate insulating material, *e.g.*, silicon dioxide, and, thereafter, performing a chemical mechanical polishing operation to remove any excess material.

In designing modern integrated circuit devices, one parameter of a transistor that is of particular importance is known as its drive current. Stated simply, the drive current of a transistor is the amount of current flowing from the drain region to the source region of a transistor. All other things being equal, it is desirable that transistors have as large a drive current as possible without otherwise adversely impacting the performance of the transistor, *i.e.*, without generating excessive heat or excessive off-state leakage currents, etc.

5 The drive current of the device may be increased by reducing the channel length of the transistor. However, all other things being equal, the smaller the channel length of the transistor, the greater the off-state leakage current. Moreover, the off-state leakage current increases exponentially as the channel length of the device decreases. Off-state leakage
10 currents also increase as the transistor width increases, but at a rate that is less than the exponential rate associated with reductions in the channel length of a device. Thus, in attempting to increase the drive current of a transistor, increasing the width of the transistor results in lower off-state leakage currents, as compared to increasing the drive current the same amount by reducing the channel length. Moreover, to a great extent, reducing the channel length of the device is limited by available photolithography and etching processes.

15 Typically, the amount of drive current that can be generated per unit width ("w") of the transistor is a known value. Thus, when a total drive current is desired or required for a particular circuit application, the required width of the transistor to accomplish this purpose may be readily determined. Thus, for a given type of transistor, an application requiring a transistor having a width of 30w may be satisfied by a single transistor having a width of approximately 30w or six transistors, arranged in parallel, each having a width of approxi-
20 mately 5w. Using this process, the layout of integrated circuit devices across the surface of a portion of a semiconducting substrate is accomplished, with the ultimate goal being to minimize consumption of wafer plot space, *i.e.*, to maximize the use of available substrate. Thus, it would be desirable to have a transistor in which the width dimension of a substrate can be maximized in a given plot space of semiconducting substrate.

25 The present invention is directed to a method that solves or reduces some or all of the aforementioned problems.

SUMMARY OF THE INVENTION

5 The present invention is directed to a transistor having an enhanced width dimension and a method of making same. In one illustrative embodiment, the transistor comprises a semiconducting substrate, a recessed isolation structure formed in the substrate, the isolation structure defining a recess thereabove, a gate electrode and a gate insulation layer positioned above the substrate, a portion of the gate electrode and the gate insulation layer extending into the recess above the recessed isolation structure, and a source region and a drain region formed in the substrate. In another illustrative embodiment, the transistor comprises a semiconducting substrate, a recessed isolation structure that defines an active area having an upper surface and an exposed sidewall surface, a gate insulation layer and a gate electrode positioned above a portion of the upper surface and a portion of the exposed sidewall surface of the active area, and a source region and a drain region formed in the active area.

10 In one illustrative embodiment, the method of making a transistor comprises providing a semiconducting substrate, forming a recessed isolation structure in a trench formed in the substrate, the recessed isolation structure thereby defining a recess in the substrate, forming a gate insulation layer and a gate electrode above the substrate, a portion of the gate insulation layer and gate electrode extending into the recess in the substrate and above the recessed isolation structure, and forming a plurality of source/drain regions in the substrate adjacent the gate electrode.

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BRIEF DESCRIPTION OF THE DRAWINGS

The invention may be understood by reference to the following description taken in conjunction with the accompanying drawings, in which like reference numerals identify like elements, and in which:

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Figure 1 is a cross-sectional front view of an illustrative prior art transistor in the transistor length direction;

Figure 2 is a cross-sectional side view of the prior art transistor shown in Figure 1 along the line "2-2";

Figure 3 is a cross-sectional front view of a partially formed transistor in accordance with one illustrative embodiment of the present invention;

Figure 4 is a cross-sectional front view of the device shown in Figure 3 after a gate insulation layer has been formed thereabove;

Figure 5 is a cross-sectional front view of the device shown in Figure 4 after a layer of polysilicon has been formed thereabove;

Figure 6A is a cross-sectional front view of the device shown in Figure 5 after a gate electrode has been patterned from the layer of polysilicon;

Figure 6B is a cross-sectional side view, in the transistor width direction, of the device shown in Figure 6A taken along the line "6B-6B";

Figure 7A is a cross-sectional front view of the device shown in Figure 6A after source/drain regions have been formed on the device;

5 Figure 7B is a cross-sectional side view, in the transistor width direction, of the device shown in Figure 7A taken along the line "7B-7B"; and

Figure 7C is a plan view of the device shown in Figure 7A.

While the invention is susceptible to various modifications and alternative forms, specific embodiments thereof have been shown by way of example in the drawings and are herein described in detail. It should be understood, however, that the description herein of specific embodiments is not intended to limit the invention to the particular forms disclosed, but on the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

DETAILED DESCRIPTION OF THE INVENTION

Illustrative embodiments of the invention are described below. In the interest of clarity, not all features of an actual implementation are described in this specification. It will
20 of course be appreciated that in the development of any such actual embodiment, numerous implementation-specific decisions must be made to achieve the developers' specific goals, such as compliance with system-related and business-related constraints, which will vary from one implementation to another. Moreover, it will be appreciated that such a development effort might be complex and time-consuming, but would nevertheless be a routine
25 undertaking for those of ordinary skill in the art having the benefit of this disclosure.

The present invention will now be described with reference to the attached figures. Although the various regions and structures of a semiconductor device are depicted in the drawings as having very precise, sharp configurations and profiles, those skilled in the art recognize that, in reality, these regions and structures are not as precise as indicated in the drawings. Additionally, the relative sizes of the various features depicted in the drawings may be exaggerated or reduced as compared to the size of those features or regions on fabricated devices. Nevertheless, the attached drawings are included to describe and explain illustrative examples of the present invention. As will be readily apparent to those skilled in the art upon a complete reading of the present application, the present method is applicable to a variety of technologies, *e.g.*, NMOS, PMOS, CMOS, etc., is readily applicable to a variety of devices, including, but not limited to, logic devices, memory devices, etc.

In general, the present invention is directed to a transistor device having an enhanced width dimension and a method of making same. As will be recognized after a complete reading of the present application, the present invention provides a method to maximize the width of a transistor in a given plot space of semiconducting substrate. In turn, integrated circuit devices incorporating such transistors may be more efficient in terms of plot space consumption.

As shown in Figure 3, a trench 32 is formed in a semiconducting substrate 30. For reference, the transistor length direction "L" is also shown in Figure 1. A recessed isolation material 34, comprised of materials such as silicon dioxide, silicon oxynitride, etc., is formed in the trench 32. The width 33 and the depth 31 of the trench 32 may be varied as a matter of design choice. In one embodiment, the depth 31 of the trench 32 ranges from approximately

3000-6000 Å. The width 33 of the trench 32 may vary from a minimum of the smallest feature size that can be patterned using existing photolithography and etching techniques, up to any desired width. In one illustrative embodiment, the width 33 of the trench 32 ranges from approximately 2000-3000 Å.

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The recessed isolation material 34 may be formed in the trench 32 by a variety of techniques. In one illustrative embodiment, a layer of insulating material (not shown) is blanket deposited above the surface 35 of the substrate 30 and in the trench 32. Thereafter, a chemical mechanical polishing operation is performed on the layer of insulating material such that the insulating material in the trench 32 is approximately planar (not shown) with the surface 35 of the substrate 30. An etching process, such as a wet etching process, may then be performed to reduce the level of insulating material 34 in the trench 32 to the level depicted in Figure 3. In one illustrative embodiment, the insulating material 34 is removed until such time as a surface 36 of the isolation material 34 in the trench 32 is positioned approximately 1000-1500 Å beneath the surface 35 of the substrate 30. This process results in the definition of an active island 37 of substrate material having an exposed upper surface 35A and an exposed sidewall surface 35B. The island 37 of substrate material may be of any desired shape, *i.e.*, circular, oval, rectangular, etc. This process also results in the definition of a recess 49 in the substrate 30 above the recessed isolation material 34. In the disclosed embodiment, the recess 49 has a depth of approximately 1000-1500 Å

Thereafter, one or more channel doping operations are performed at this stage of manufacturing. For example, in one illustrative embodiment, a threshold voltage implant process is performed on the device. This may be accomplished by performing a four-way angled channel implant process wherein each of the angled implants are spaced approxi-

mately 90 degrees apart with respect to one another. In one illustrative embodiment, this threshold voltage implant may be accomplished by a four-way angled implant process performed at an implant angle of approximately 30-50 degrees (with respect to a line perpendicular to the surface 35 of the substrate 30) using dopant atoms at a concentration ranging from approximately $1-3 \times 10^{12}$ ions/cm² per rotation. For an NMOS device, boron may be implanted during the threshold voltage implant step at an energy level ranging from approximately 10-15 keV. For a PMOS device, such a threshold voltage implant may be performed using phosphorous at an energy level ranging from approximately 90-110 keV. Additional channel doping implantation processes may be performed at this time if desired or required by the device under construction.

Thereafter, as shown in Figure 4, a gate insulation layer 40 for the transistor 10 is formed for the device. The gate insulation layer 40 may be formed from a variety of materials, such as silicon dioxide, silicon oxynitride, silicon nitride, or any dielectric material having a dielectric constant less than approximately four. The gate insulation layer 40 may be formed by a variety of processes, *e.g.*, chemical vapor deposition (CVD), thermal growth, etc. In one illustrative embodiment, as shown in Figure 4, the gate insulation layer 40 is comprised of a thermally grown layer of silicon dioxide having a thickness ranging from approximately 20-50 Å.

Next, as shown in Figure 5, a layer of polysilicon 41 is blanket deposited above the gate insulation layer 40 and above the recessed isolation material 34. The layer of polysilicon 41 may be formed by a variety of techniques, *e.g.*, chemical vapor deposition, low pressure chemical vapor deposition, etc. In one illustrative embodiment, the layer of polysilicon 41

has a thickness ranging from approximately 1000-2000 Å, and it is formed by conformally depositing the layer of polysilicon 41 using a chemical vapor deposition process.

Next, as shown in Figure 6A, using traditional photolithography and one or more etching processes, a gate electrode 42 is patterned from the layer of polysilicon 41. The gate insulation layer 40 may also be patterned at this time, as shown in Figure 6A. Figure 6B is a side view of the structure depicted in Figure 6A taken along the line "6B-6B." That is, Figure 6B is a cross-sectional view of the device in the transistor width dimension "W." As shown therein, a portion 43 of the gate electrode 42 extends beyond the isolation structure 34. The portion 43 of the gate electrode 42 is coupled to a power supply (not shown) so that a voltage may be applied to the gate electrode 42.

Then, halo implant regions (not shown) are formed in the device by performing a four-way angled halo implant process. Each of the angled implant processes are performed at an angle ranging from approximately 30-45 degrees with respect to a line generally perpendicular to the surface 35 of the substrate 30, and at a concentration level ranging from approximately $1-6 \times 10^{13}$ ions/cm² total (for all four rotations). In an illustrative NMOS device, boron atoms may be implanted at an energy level ranging from approximately 7-15 keV. In an illustrative PMOS device, arsenic may be implanted during this halo implant process at an energy level ranging from approximately 40-65 keV.

Thereafter, source and drain regions 50 for the device may be formed using a variety of process flows. Figures 7A and 7B (side view taken along the line "7B-7B" in Figure 7A) depict the transistor after the source/drain regions 50 have been formed. Figure 7C is a plan view of the device shown in Figure 7A. In one illustrative embodiment, a source/drain exten-

sion implant process is performed to form source/drain extensions 51 of the completed device. This extension implantation process may be performed at a relatively low energy level and at a relatively high concentration of dopant atoms. For example, the concentration of dopant atoms in the extension implant process may vary from approximately 1×10^{14} to 2×10^{15} ions/cm² of the appropriate dopant atoms, *e.g.*, arsenic (Ar) or phosphorous (P) for NMOS technology, boron (B) or boron difluoride (BF₂) for PMOS technology, etc. The energy level for the extension implant process will vary depending upon the dopant material used in the process. For example, in one illustrative embodiment for forming the source/drain extension implants in an NMOS device, the extension implantation process is performed using arsenic as the dopant atoms at a concentration ranging from approximately 6×10^{14} to 2×10^{15} ions/cm² and at an energy level ranging from approximately 3-15 keV. Typically, the extension implant process will result in implant regions in the substrate that are generally self-aligned with respect to the gate electrode 42 (as implanted). However, for a PMOS device, a small sidewall spacer (not shown) may be formed adjacent the gate electrode 42 prior to performing the extension implant step. This spacer is used in PMOS devices due to the increased mobility of the dopant atoms that may be implanted, *e.g.*, boron.

Next, as indicated in Figures 7A-7C, a sidewall spacer 44 is formed adjacent the gate electrode 42. The sidewall spacer 44 is formed by depositing a layer (not shown) of spacer material above the surface of the device and thereafter performing an anisotropic etching process to define the spacer 44. The layer of spacer material may be comprised of a variety of materials, such as silicon dioxide, silicon oxynitride, or other like materials. Moreover, it may be formed by any of a variety of techniques for forming such layers, such as chemical vapor deposition (CVD), physical vapor deposition (PVD), etc.

Next, a source/drain implant process is performed on the device. Note that the source/drain implant process is self-aligned with respect to the sidewall spacer 44. The dopant concentration levels and implant energy for the source/drain implant process may vary. For example, the concentration of dopant atoms in the source/drain implantation process may vary from approximately 5×10^{14} to 5×10^{15} ions/cm² of the appropriate dopant atoms, *e.g.*, arsenic or phosphorous for NMOS technology, boron for PMOS technology, etc. The energy level for the source/drain implantation process will vary depending upon the dopant material. For example, in one illustrative embodiment for forming the source/drain regions in an NMOS device, the source/drain implantation process is performed using arsenic as the dopant atoms at a concentration of approximately 5×10^{14} to 5×10^{15} ions/cm² and at an energy level ranging from approximately 20-70 keV.

Thereafter, one or more thermal anneal processes is performed to activate the dopant atoms introduced into the substrate 30 during various ion implant processes described above, and to repair the damage to the lattice structure of the semiconducting substrate 30 resulting from the ion implantation processes. In one embodiment, this anneal process may be at a temperature ranging from approximately 1000-1050°C for a duration of approximately 5-20 seconds in a rapid thermal anneal chamber. Note that during this process, the previously implanted dopant atoms migrate, or move, from their original implanted position. This migration of the dopant atoms is generally isotropic in direction.

As shown in Figures 6A, 6B and 7A-7C, the present invention is directed to a novel transistor structure. The gate electrode 42 has first and second ends 42A, 42B, respectively. The first and second ends 42A, 42B, as well as first and second portions 40A, 4B of the gate insulation layer 40 thereunder, are positioned above a portion of the exposed sidewall 35B of

the active area 37. The remainder of the gate electrode 42 is positioned above the surface 35A of the active area 37. In the embodiment depicted in the attached drawings, the first end 42A of the gate electrode 42 is shown as being patterned such that it does not extend beyond the recessed isolation structure 34. Of course, if desired, the first end 42A of the gate electrode 42 may be patterned so as to extend completely beyond the recessed isolation structure 34 in a manner similar to the configuration depicted for the portion 43 of the gate electrode 42 depicted in Figures 6B and 7B. Stated another way, the novel transistor structure disclosed herein is comprised of a gate electrode 42 and a gate insulation layer 40 wherein a portion of the gate electrode 42 and the gate insulation layer 40 extends downwardly into a recess 49 in the substrate above a recessed isolation structure 34. In the disclosed embodiment, both ends 42A, 42B of the gate electrode 42 and both portions 40A, 40B of the gate insulation layer 40 extend into the recess 49 above the recessed isolation structure 34.

After the formation of the gate electrode 42, additional insulating material (not shown), *e.g.*, silicon dioxide, BPSG, etc., may be blanket deposited above the device shown in Figures 7A and 7B to fill the portions of the recess 49 not filled, or at least partially filled by the downwardly extending portions of the gate electrode 41 and gate insulation layer 40.

The present invention is directed to a transistor having an enhanced width dimension and a method of making same. In one illustrative embodiment, the transistor comprises a semiconducting substrate 30, a recessed isolation structure 34 formed in the substrate 30, the isolation structure 34 defining a recess 49 thereabove, a gate electrode 42 and a gate insulation layer 40 positioned above the substrate 30, a portion of the gate electrode 42 and the gate insulation layer 40 extending into the recess 49 above the recessed isolation structure 49, and

5 a source region 51A and a drain region 51B formed in the substrate 30. In another illustrative embodiment, the transistor comprises a semiconducting substrate 30, a recessed isolation structure 34 that defines an active area 37 having an upper surface 35A and an exposed side-wall surface 35, a gate insulation layer 40 and a gate electrode 42 positioned above a portion of the upper surface 35A and a portion of the exposed sidewall surface 35B of the active area 37, and a source region 51A and a drain region 51B formed in the active area 37.

10 In one illustrative embodiment, the method of making a transistor comprises providing a semiconducting substrate 30, forming a recessed isolation structure 34 in a trench 32 formed in the substrate 30, the recessed isolation structure 34 thereby defining a recess 49 in the substrate 30, forming a gate insulation layer 40 and a gate electrode 42 above the substrate 30, a portion of the gate insulation layer 40 and gate electrode 42 extending into the recess 49 above the recessed isolation structure 49, and forming a plurality of source/drain regions 51A, 51B in the substrate 30 adjacent the gate electrode.

15 The particular embodiments disclosed above are illustrative only, as the invention may be modified and practiced in different but equivalent manners apparent to those skilled in the art having the benefit of the teachings herein. For example, the process steps set forth above may be performed in a different order. Furthermore, no limitations are intended to the details of construction or design herein shown, other than as described in the claims below. It is therefore evident that the particular embodiments disclosed above may be altered or modified and all such variations are considered within the scope and spirit of the invention. Accordingly, the protection sought herein is as set forth in the claims below.

20

CLAIMS

WHAT IS CLAIMED:

1. A transistor, comprising:
a semiconducting substrate;
a recessed isolation structure formed in said substrate, said isolation structure defining
a recess thereabove;
a gate electrode and a gate insulation layer formed above said substrate, a portion of
said gate electrode and said gate insulation layer extending into said recess
above said recessed isolation structure; and
a source region and a drain region formed in said substrate.
2. The transistor of claim 1, wherein said semiconducting substrate is comprised
of silicon.
3. The transistor of claim 1, wherein said recessed isolation structure is
comprised of at least one of silicon dioxide and silicon oxynitride.
4. The transistor of claim 1, wherein said recessed isolation structure has a
surface that is positioned approximately 1000-1500 Å below a surface of said substrate.
5. The transistor of claim 1, wherein said recessed isolation structure is formed in
a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from
approximately 4000-5000 Å.

6. The transistor of claim 1, wherein said gate electrode is comprised of polysilicon.

5 7. The transistor of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.

8. The transistor of claim 1, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.

10 9. The transistor of claim 1, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.

15 10. The transistor of claim 1, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.

11. The transistor of claim 1, wherein said gate electrode has first and second end portions that extend into said recess.

20 12. The transistor of claim 11, wherein said first and second end portions extending into said recess are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.

13. A transistor, comprising:
a semiconducting substrate comprised of silicon;

a recessed isolation structure formed in said substrate, said isolation structure defining
a recess thereabove;

a gate electrode comprised of polysilicon and a gate insulation layer formed above
said substrate, a portion of said gate electrode and said gate insulation layer
extending into said recess above said recessed isolation structure; and

a source region and a drain region formed in said substrate.

14. The transistor of claim 13, wherein said recessed isolation structure is
comprised of at least one of silicon dioxide and silicon oxynitride.

15. The transistor of claim 13, wherein said recessed isolation structure has a
surface that is positioned approximately 1000-1500 Å below a surface of said substrate.

16. The transistor of claim 13, wherein said recessed isolation structure is formed
in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging
from approximately 4000-5000 Å.

17. The transistor of claim 13, wherein said gate insulation layer is comprised of
at least one of silicon dioxide and silicon oxynitride.

18. The transistor of claim 13, wherein said gate electrode has a thickness ranging
from approximately 1000-2000 Å.

19. The transistor of claim 13, wherein said gate insulation layer has a thickness
ranging from approximately 20-50 Å.

20. The transistor of claim 13, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.

5 21. The transistor of claim 13, wherein said gate electrode has first and second end portions that extend into said recess in said substrate.

22. The transistor of claim 21, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.

23. A transistor, comprising:
a semiconducting substrate;
a recessed isolation structure defining an active area having an upper surface and an exposed sidewall surface;
5 a gate insulation layer and a gate electrode positioned above a portion of said upper surface and a portion of said exposed sidewall surface of said active area; and
a source region and a drain region formed in said active area.

20 24. The transistor of claim 23, wherein said semiconducting substrate is comprised of silicon.

25 25. The transistor of claim 23, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.

26. The transistor of claim 23, wherein said recessed isolation structure has a surface that is positioned approximately 1000-1500 Å below a surface of said substrate.

27. The transistor of claim 23, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.

28. The transistor of claim 23, wherein said gate electrode is comprised of polysilicon.

29. The transistor of claim 23, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.

30. The transistor of claim 23, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.

31. The transistor of claim 23, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.

32. The transistor of claim 23, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.

33. The transistor of claim 23, wherein said gate electrode has first and second end portions that extend into a recess in said substrate defined by said recessed isolation structure.

34. The transistor of claim 33, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.

5 35. A method of making a transistor, comprising:
providing a semiconducting substrate;
forming a recessed isolation structure in a trench formed in said substrate, said recessed isolation structure thereby defining a recess in said substrate;
forming a gate insulation layer and a gate electrode above said substrate, a portion of said gate insulation layer and gate structure extending into said recess above said recessed isolation structure; and
forming a plurality of source/drain regions in said substrate adjacent said gate electrode.

10 36. The method of claim 35, wherein providing a semiconducting substrate comprises providing a semiconducting substrate comprised of silicon.

15 37. The method of claim 35, wherein forming a recessed isolation structure in a trench formed in said substrate, said recessed isolation structure thereby defining a recess in said substrate, comprises forming a recessed isolation structure comprised of at least one of silicon dioxide and silicon oxynitride in a trench formed in said substrate, said recessed isolation structure thereby defining a recess in said substrate.

20 38. The method of claim 35, wherein forming a recessed isolation structure in a trench formed in said substrate, said recessed isolation structure thereby defining a recess in

said substrate, comprises forming a recessed isolation structure in a trench formed in said substrate, said recessed isolation structure thereby defining a recess in said substrate having a depth ranging from approximately 1000-1500 Å.

5 39. The method of claim 35, wherein forming a gate insulation layer and a gate electrode above said substrate comprises forming a gate insulation layer comprised of at least one of silicon dioxide and silicon oxynitride and a gate electrode comprised of polysilicon above said substrate.

40. The method of claim 35, wherein forming a plurality of source/drain regions in said substrate adjacent said gate electrode comprises:
performing an extension implant process;
performing a source/drain implant process; and
performing at least one anneal process.

41. The method of claim 35, wherein forming a recessed isolation structure in a trench formed in said substrate, said recessed isolation structure thereby defining a recess in said substrate, comprises:

forming a trench in said substrate;
20 depositing an insulating material above said substrate and in said trench;
performing a chemical mechanical polishing operation on said deposited layer of insulating material; and
performing a wet etch process to remove at least some of said insulating material in said trench to define a recess in said substrate having a depth ranging from
25 approximately 1000-1500 Å.

42. The method of claim 35, wherein forming a gate insulation layer comprises forming a gate insulating layer by performing at least one of a deposition process and a thermal growth process.

5

43. The method of claim 35, wherein forming a gate electrode comprises depositing a layer of polysilicon and performing an etching process on the layer of polysilicon to define a gate electrode.

44. The method of claim 35, wherein forming a gate insulation layer and a gate electrode above said substrate, a portion of said gate insulation layer and gate structure extending into said recess above said recessed isolation structure, comprises forming a gate insulation layer and a gate electrode above said substrate, each of said gate insulation layer and said gate electrode having first and second end portions that extend into said recess in said substrate above said recessed isolation structure.

45. The method of claim 44, wherein each of said first and second end portions of said gate insulation layer and said gate electrode extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.

20

46. A method of making a transistor, comprising:
providing a semiconducting substrate comprised of silicon;
forming a trench in said substrate;
depositing an insulating material above said substrate and in said trench;

25

performing a chemical mechanical polishing operation on said deposited layer of insulating material;

performing a wet etch process to remove at least some of said insulating material in said trench to define a recess in said substrate, said recessed isolation structure thereby defining a recess in said substrate;

forming a gate insulation layer and a gate electrode above said substrate, a portion of said gate insulation layer and gate structure extending into said recess above said recessed isolation structure; and

forming a plurality of source/drain regions in said substrate adjacent said gate electrode.

47. The method of claim 46, wherein forming a trench in said substrate comprises etching a trench in said substrate.

48. The method of claim 46, wherein depositing an insulating material above said substrate and in said trench comprises depositing a layer of insulating material comprised of at least one of silicon dioxide and silicon oxynitride above said substrate and in said trench.

49. The method of claim 46, wherein said recess in said substrate has a depth ranging from approximately 1000-1500 Å.

50. The method of claim 46, wherein forming a gate insulation layer and a gate electrode above said substrate, a portion of said gate insulation layer and gate structure extending into said recess above said recessed isolation structure, comprises forming a gate insulation layer comprised of at least one of silicon dioxide and silicon oxynitride and a gate

electrode comprised of polysilicon above said substrate, a portion of said gate insulation layer and gate structure extending into said recess above said recessed isolation structure.

51. The method of claim 46, wherein forming a plurality of source/drain regions
5 in said substrate adjacent said gate electrode comprises:

- performing an extension implant process;
- performing a source/drain implant process; and
- performing at least one anneal process.

52. The method of claim 46, wherein forming a gate insulation layer comprises forming a gate insulating layer by performing at least one of a deposition process and a thermal growth process.

53. The method of claim 46, wherein forming a gate electrode comprises depositing a layer of polysilicon and performing an etching process on the layer of polysilicon to define a gate electrode.

54. The method of claim 46, wherein said forming a gate insulation layer and a gate electrode above said substrate, a portion of said gate insulation layer and gate structure
20 extending into said recess above said recessed isolation structure, comprises forming a gate insulation layer and a gate electrode above said substrate, each of said gate insulation layer and said gate electrode having first and second end portions that extend into said recess in said substrate above said recessed isolation structure.

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55. The method of claim 54, wherein each of said first and second end portions of said gate insulation layer and said gate electrode extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.

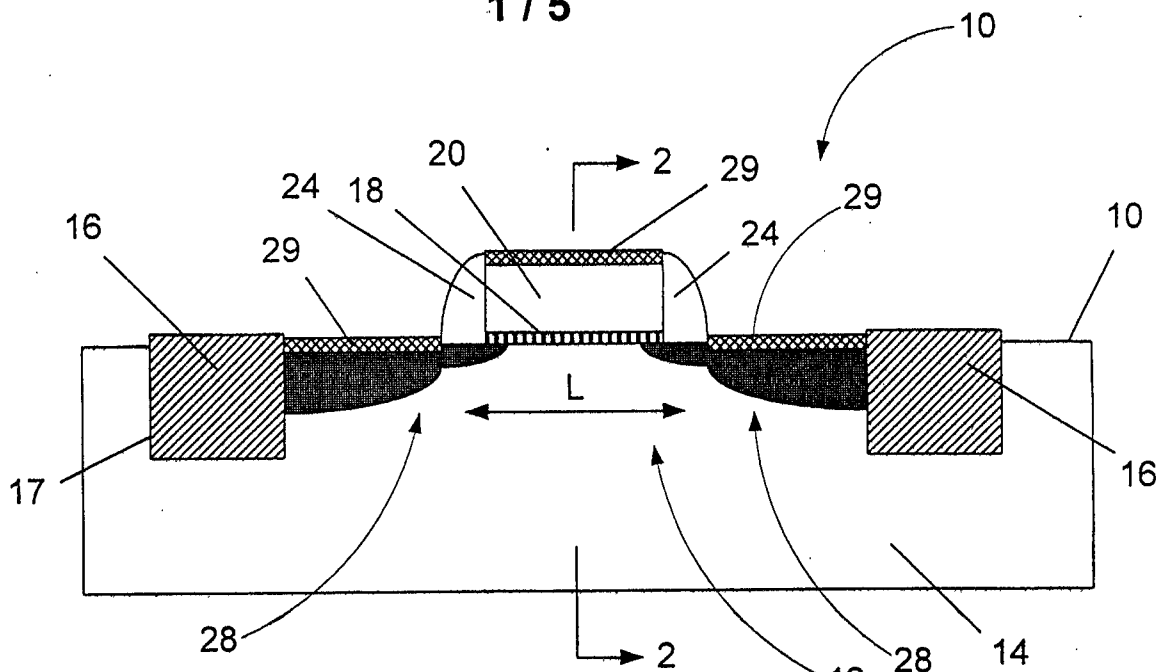
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FILED - 10/23/00

ABSTRACT OF THE DISCLOSURE

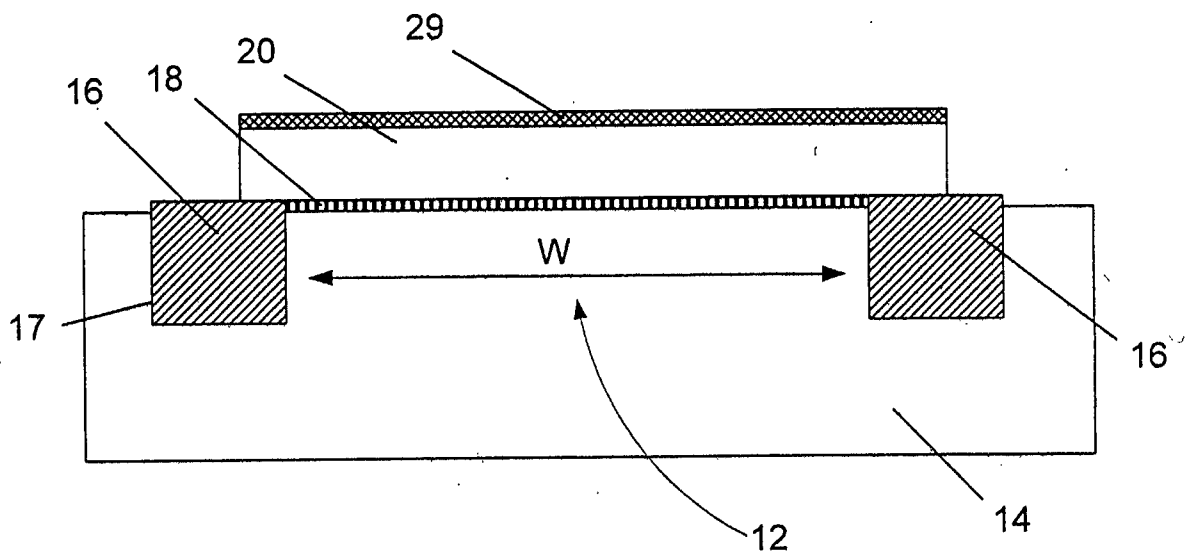
5 The present invention is directed to a transistor having an enhanced width dimension and a method of making same. In one illustrative embodiment, the transistor comprises a semiconducting substrate, a recessed isolation structure formed in the substrate, the isolation structure defining a recess thereabove, a gate electrode and a gate insulation layer positioned above the substrate, a portion of the gate electrode and the gate insulation layer extending into the recess above the recessed isolation structure, and a source region and a drain region formed in the substrate. In another illustrative embodiment, the transistor comprises a semiconducting substrate, a recessed isolation structure that defines an active area having an upper surface and an exposed sidewall surface, a gate insulation layer and a gate electrode positioned above a portion of the upper surface and a portion of the exposed sidewall surface of the active area, and a source region and a drain region formed in the active area.

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(Prior Art)

Figure 1



(Prior Art)

Figure 2

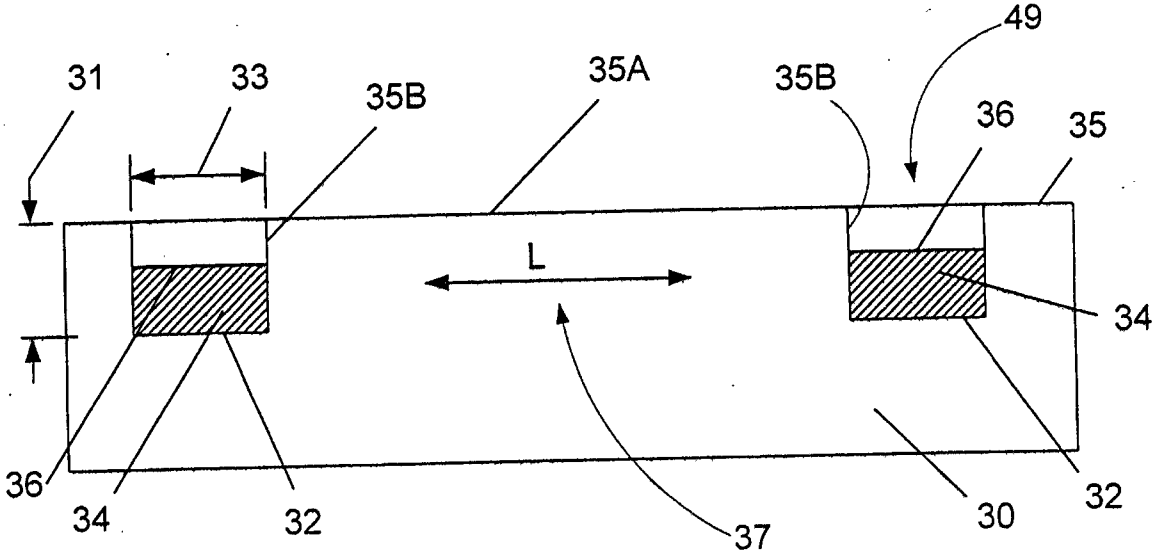


Figure 3

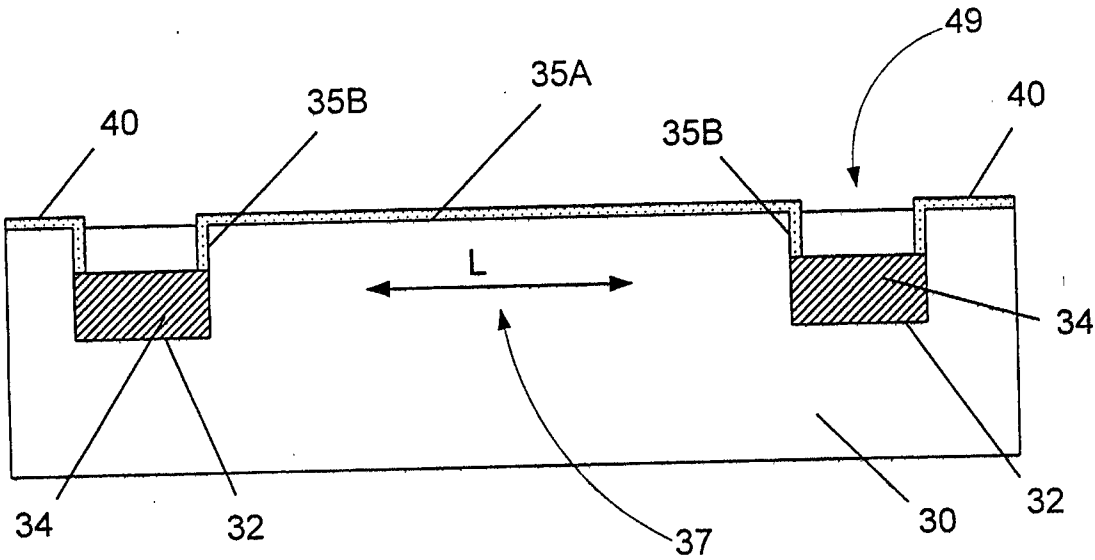


Figure 4

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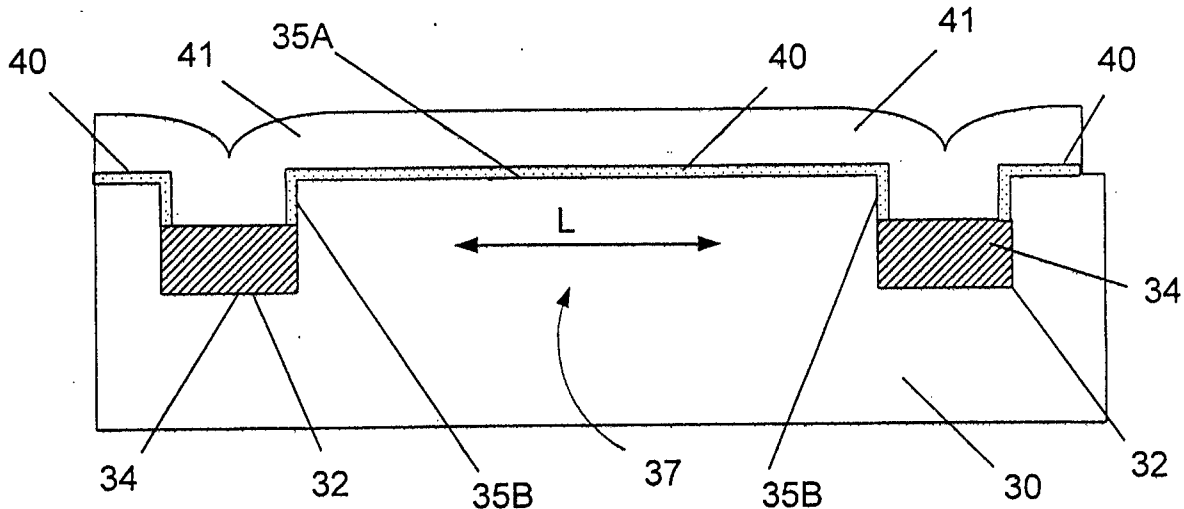


Figure 5

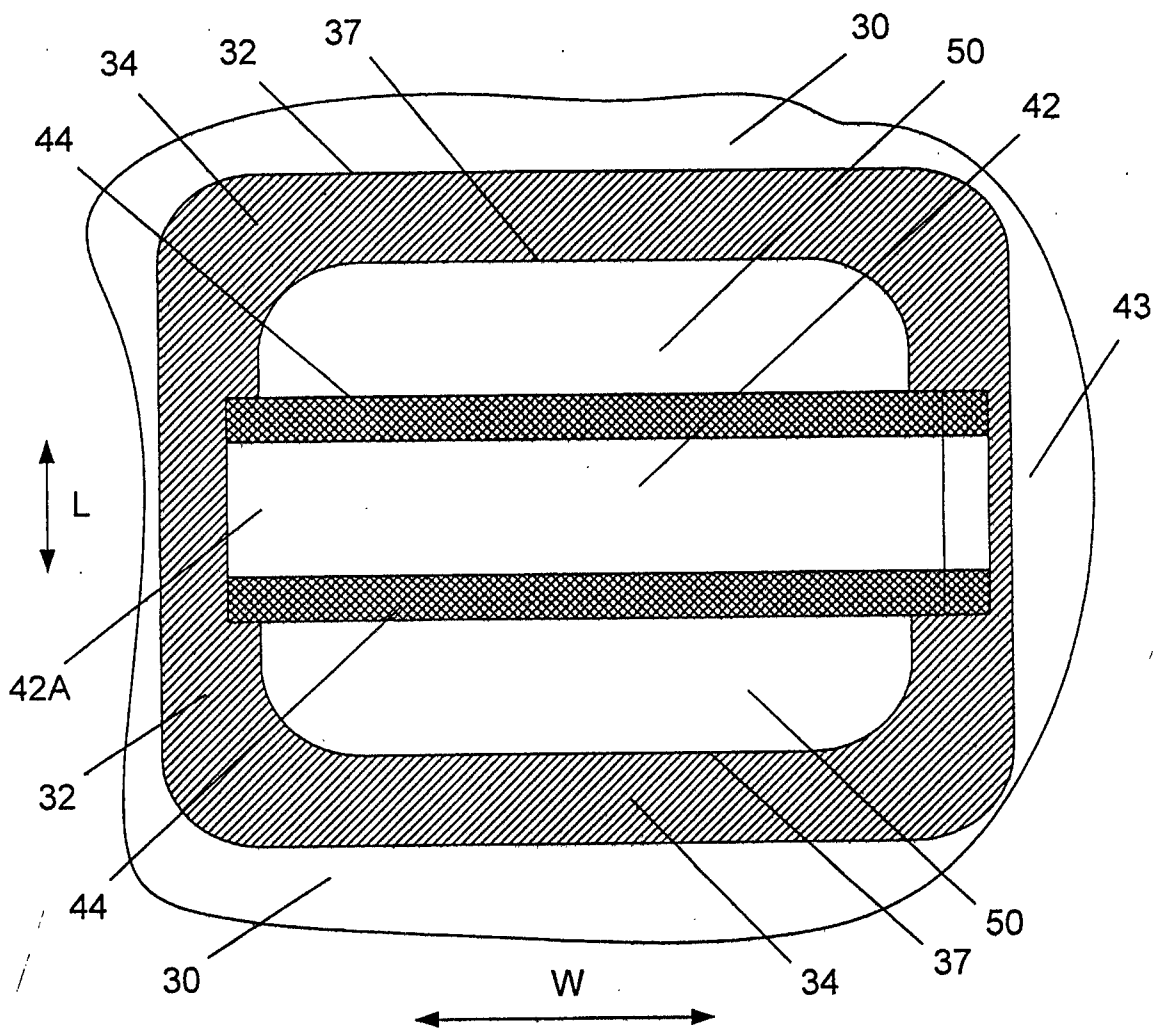


Figure 7C

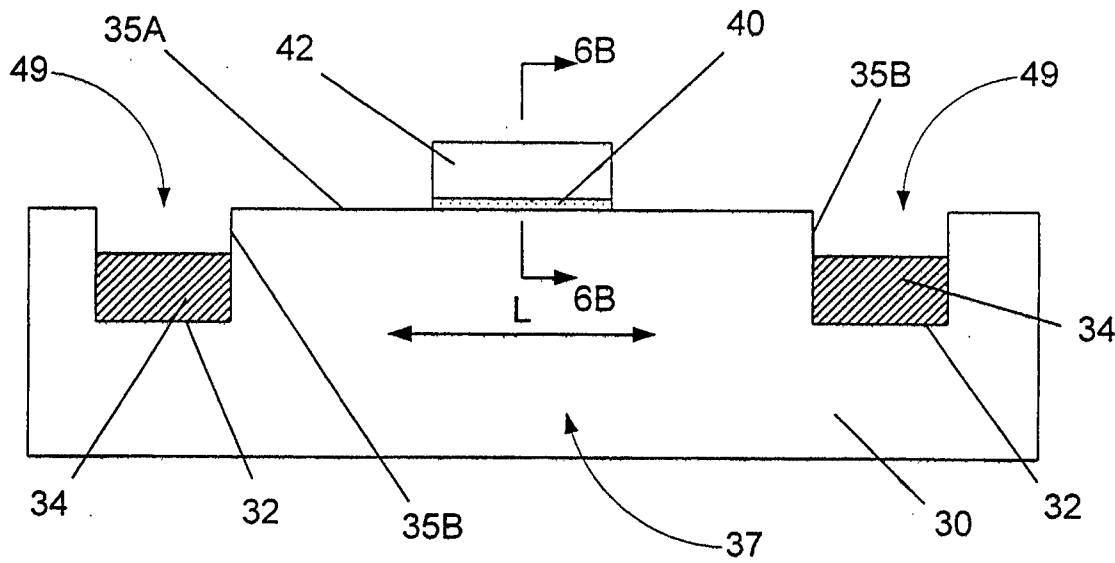


Figure 6A

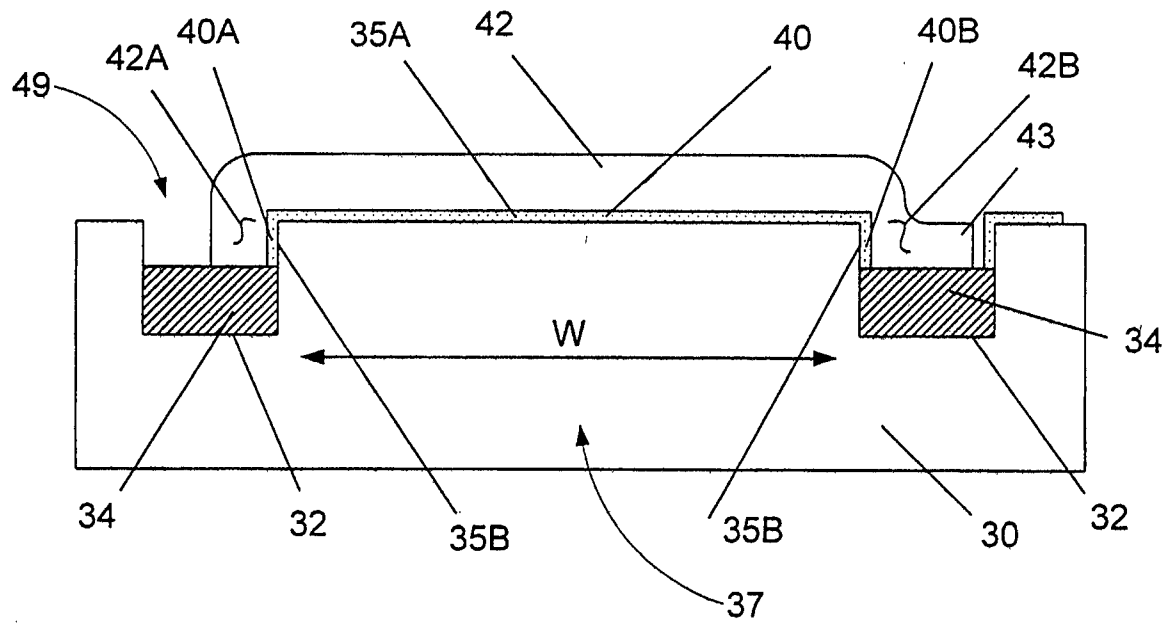


Figure 6B

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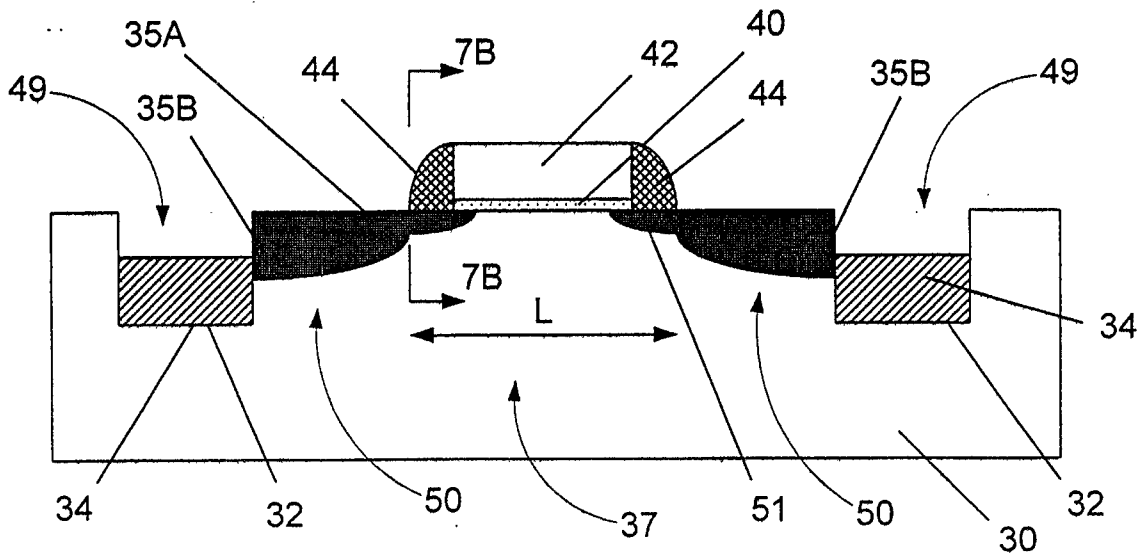


Figure 7A

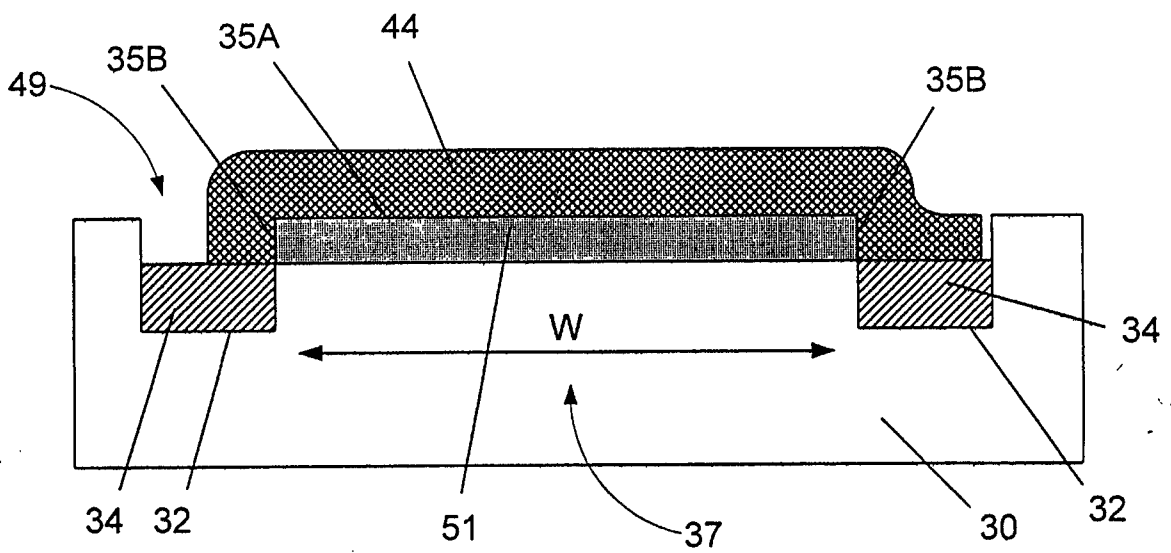


Figure 7B

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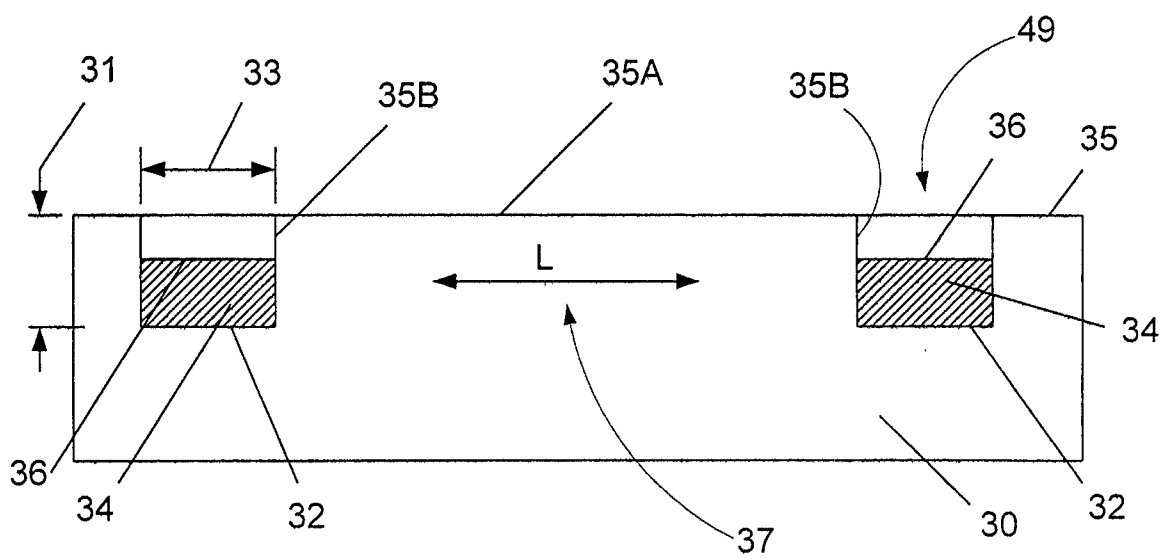


Figure 3

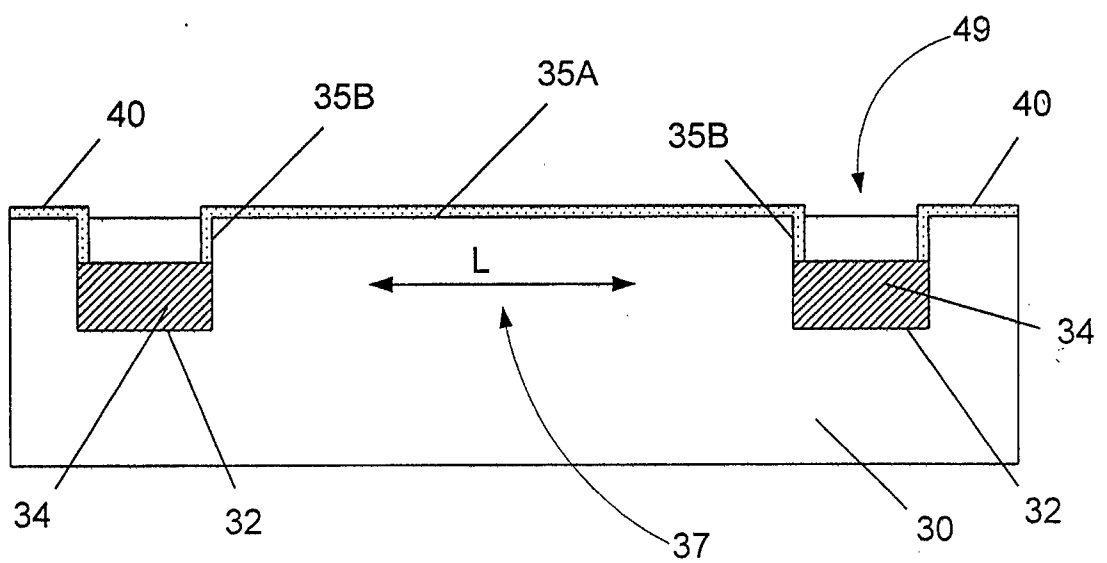


Figure 4

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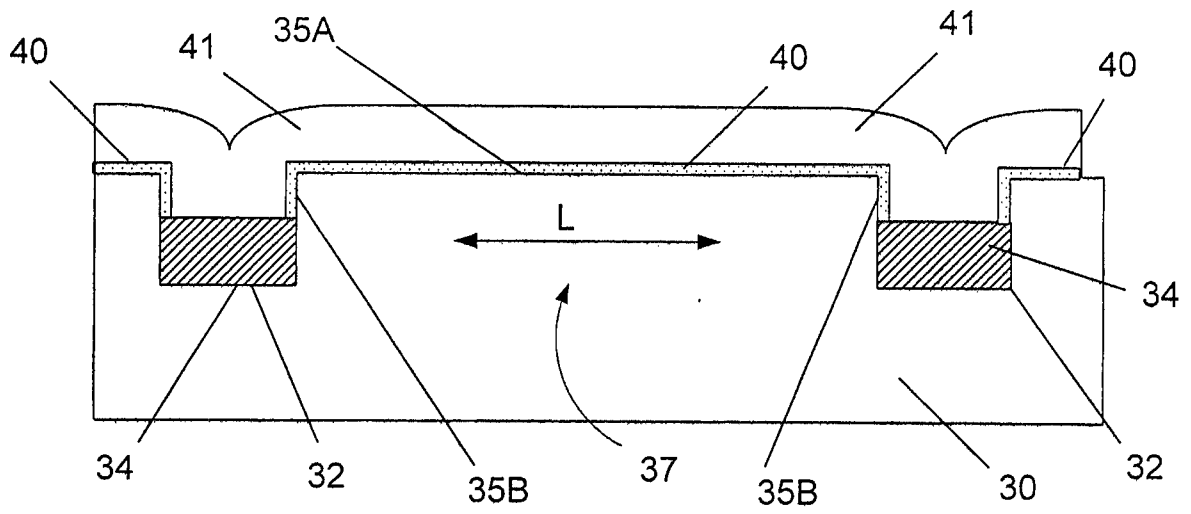


Figure 5

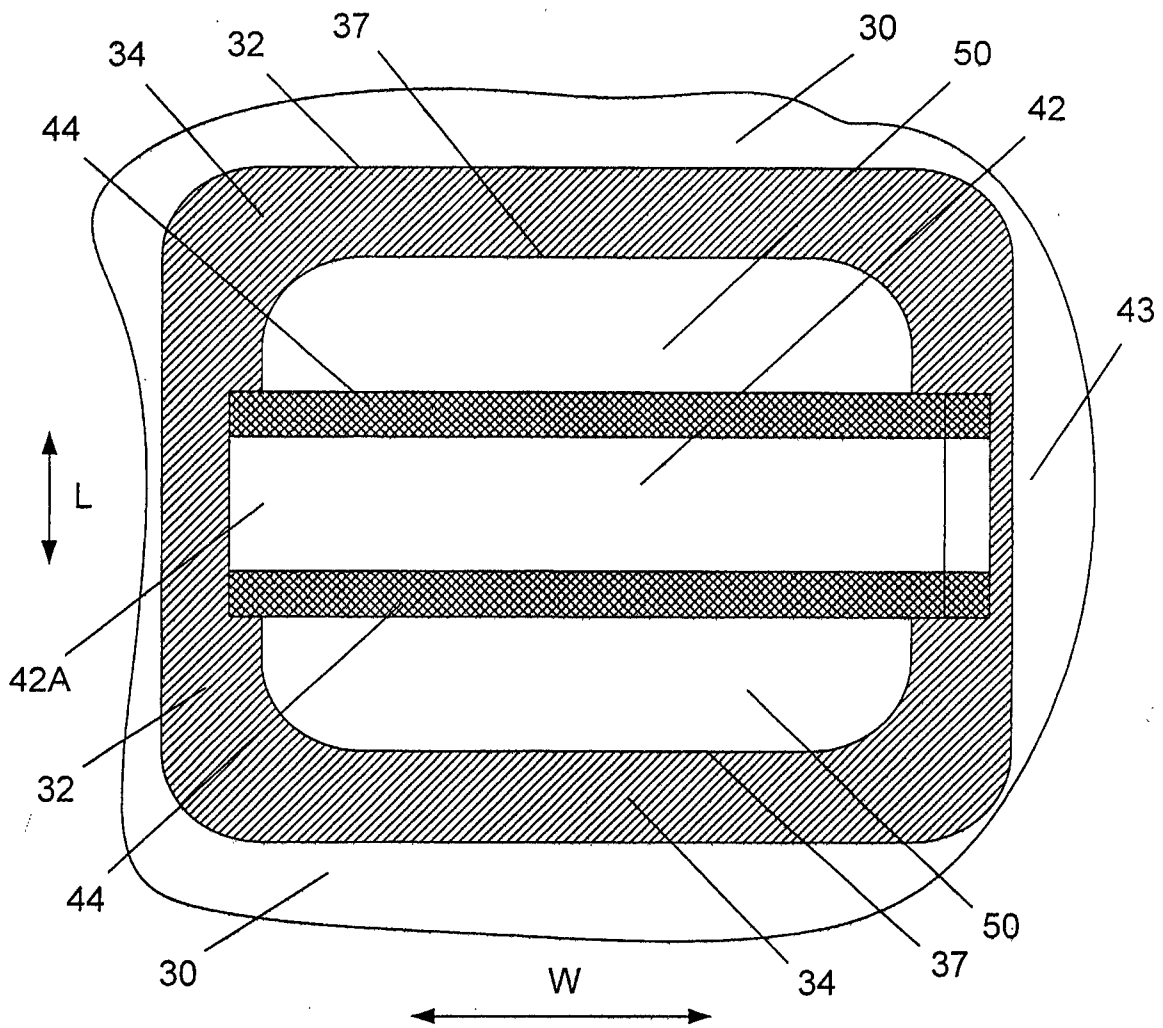


Figure 7C

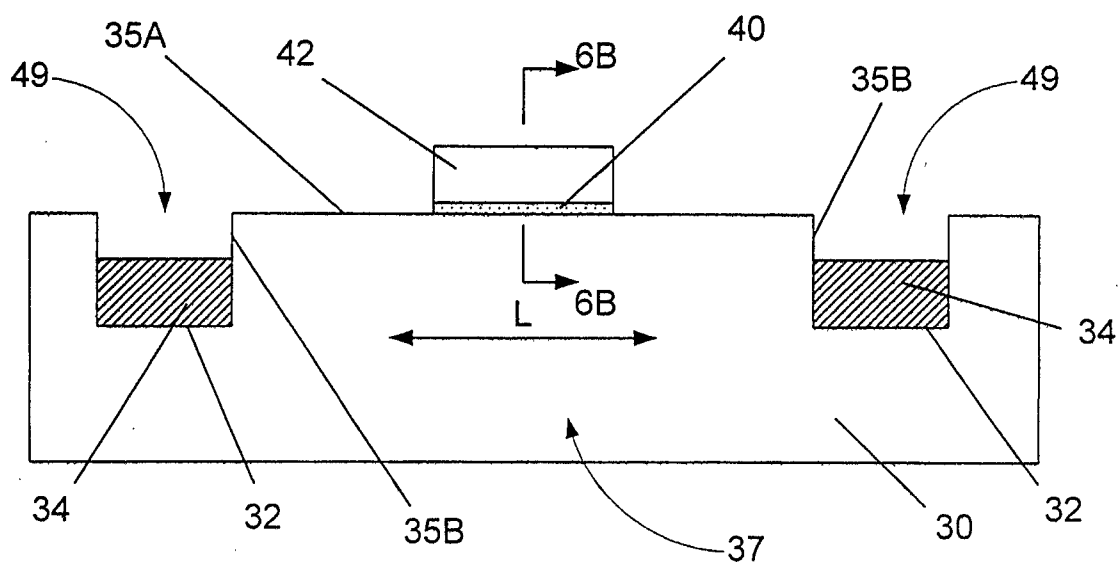


Figure 6A

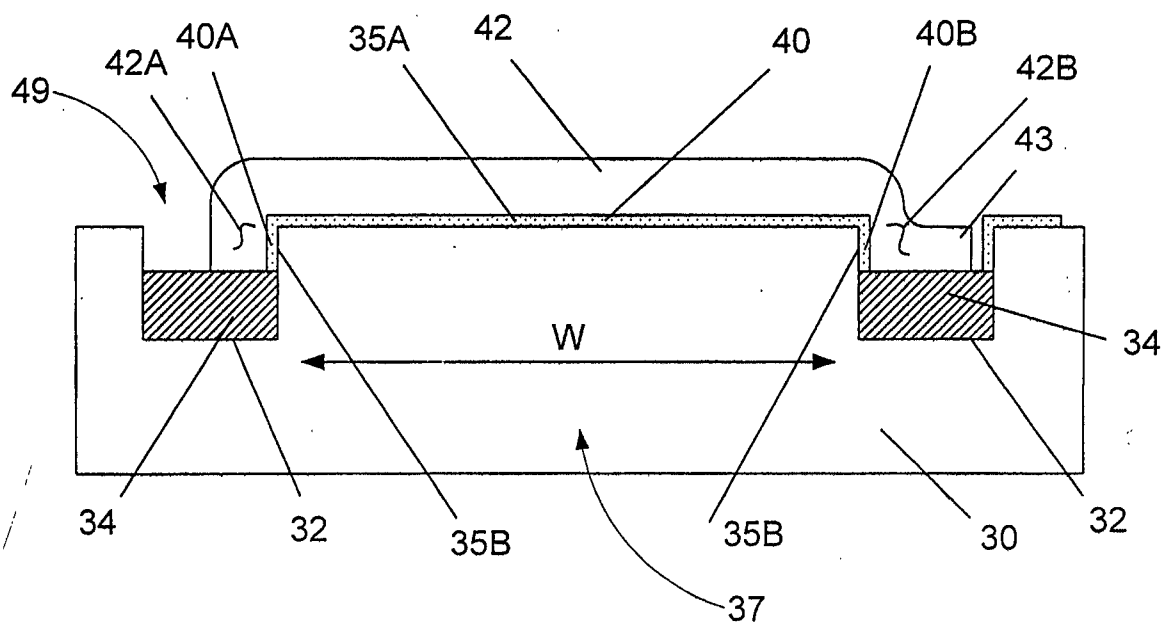


Figure 6B

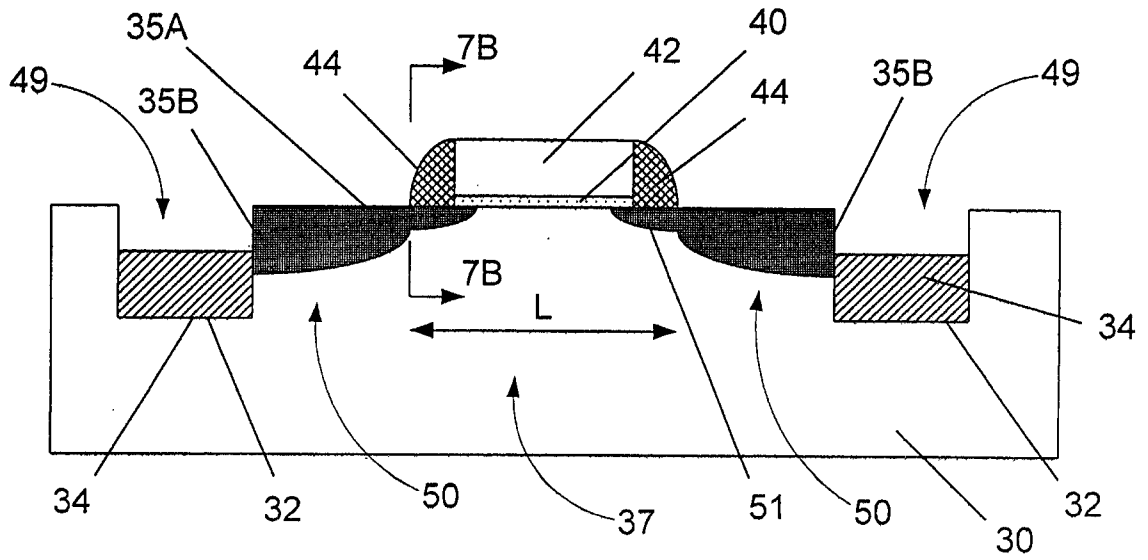


Figure 7A

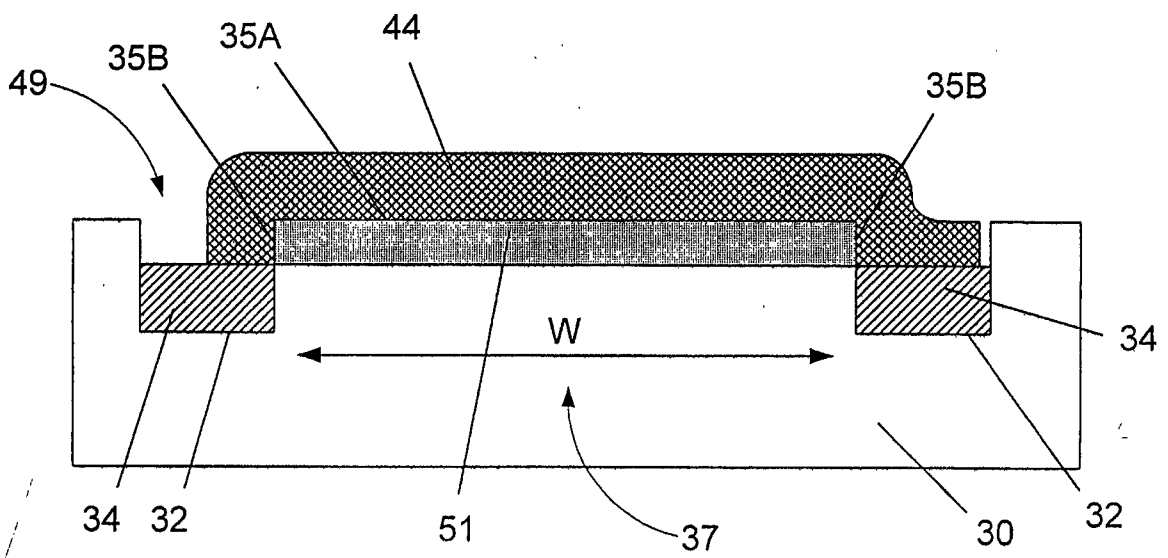


Figure 7B

DECLARATION

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or the below named inventors are the original, first and joint inventors (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled "A TRANSISTOR DEVICE HAVING AN ENHANCED WIDTH DIMENSION AND A METHOD OF MAKING SAME" the Specification of which:

- ☒ is attached hereto.
☐ was filed on _____ as Application Serial No. _____.

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims.

I acknowledge the duty to disclose to the Patent and Trademark Office all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations, § 1.56.

I hereby claim priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent, United States provisional application(s), or inventor's certificate listed below and have also identified below any foreign application for patent, United States provisional application, or inventor's certificate having a filing date before that of the application on which priority is claimed:

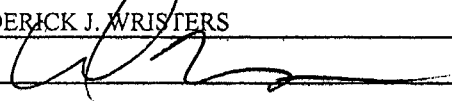
PRIORITY APPLICATION(S)			Priority Claimed
(Number)	(Country)	(Date Filed)	Yes/No
(Number)	(Country)	(Date Filed)	Yes/No

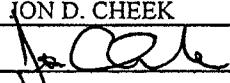
I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose all information known to me to be material to patentability of the subject matter claimed in this application, as "materiality" is defined in Title 37, Code of Federal Regulations, § 1.56, which become available between the filing date of the prior application and the national or PCT international filing date of this application:


(Application Serial No.)	(Filing Date)	(Status)
(Application Serial No.)	(Filing Date)	(Status)

I hereby direct that all correspondence and telephone calls be addressed to J. Mike Amerson, Williams, Morgan & Amerson, P.C., 7676 Hillmont, Suite 250, Houston, Texas 77040, (713) 934-4055.

I HEREBY DECLARE THAT ALL STATEMENTS MADE OF MY OWN KNOWLEDGE ARE TRUE AND THAT ALL STATEMENTS MADE ON INFORMATION AND BELIEF ARE BELIEVED TO BE TRUE; AND FURTHER THAT THESE STATEMENTS WERE MADE WITH THE KNOWLEDGE THAT WILLFUL FALSE STATEMENTS AND THE LIKE SO MADE ARE PUNISHABLE BY FINE OR IMPRISONMENT, OR BOTH, UNDER SECTION 1001 OF TITLE 18 OF THE UNITED STATES CODE AND THAT SUCH WILLFUL FALSE STATEMENTS MAY JEOPARDIZE THE VALIDITY OF THE APPLICATION OR ANY PATENT ISSUED THEREON.

Inventor's Full Name: DERICK J. WRISTERS
Inventor's Signature: 
Country of Citizenship: USA Date: 3/5/01
Residence Address: (street, number, city, state, and/or country) 13710 Overland Pass
Bee Caves, TX 78738
Post Office Address: Same
(if different from above)

Inventor's Full Name: ION D. CHEEK
Inventor's Signature: 
Country of Citizenship: USA Date: 3/12/01
Residence Address: (street, number, city, state, and/or country) 3602 Newland Place
Round Rock, TX 78681
Post Office Address: Same
(if different from above)

Inventor's Full Name: JOHN G. PELLERIN
Inventor's Signature: 
Country of Citizenship: USA Date: 3/5/01
Residence Address: (street, number, city, state, and/or country) 6546 Needham Lane
Austin, Texas 78739
Post Office Address: Same
(if different from above)

File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

Document Date - 2001-03-20
Document Title - Power of Attorney

Application Assignment Record

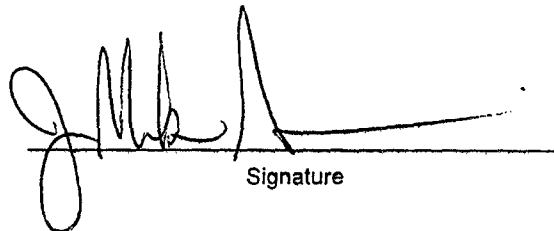
According to the application transmittal letter, an assignment recording ownership was filed with this application; however, a copy of this record was not located in the original file history record obtained from the United States Patent and Trademark Office. Upon your request, we will attempt to obtain the assignment documents from the Assignment Recordation Branch of the United States Patent and Trademark Office or from a related application case (if applicable). Please note that additional charges will apply for this service.

REQUEST AND CERTIFICATION UNDER 35 U.S.C. 122(b)(2)(B)(i)	First Named Inventor	Derick J. Wristers
	Title	A Transistor Device Having an Enhanced Width Dimension...
	Atty Docket Number	2000.065000/TT4203

I hereby certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral agreement, that requires publication at eighteen months after filing. I hereby request that the attached application not be published under 35 U.S.C. 122(b).

March 20, 2001

Date



Signature

J. Mike Amerson

Typed or printed name

This request must be signed in compliance with 37 CFR 1.33(b) and submitted with the application **upon filing**.

Applicant may rescind this nonpublication request at any time. If applicant rescinds a request that an application not be published under 35 U.S.C. 122(b), the application will be scheduled for publication at eighteen months from the earliest claimed filing date for which a benefit is claimed.

If applicant subsequently files an application directed to the invention disclosed in the attached application in another country, or under a multilateral international agreement, that requires publication of applications eighteen months after filing, the applicant **must** notify the United States Patent and Trademark Office of such filing within forty-five (45) days after the date of the filing of such foreign or international application. **Failure to do so will result in abandonment of this application (35 U.S.C. 122(b)(2)(B)(iii)).**

Burden Hour Statement: This collection of information is required by 37 CFR 1.213(a). The information is used by the public to request that an application not be published under 35 U.S.C. 122(b) (and the PTO to process that request). Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This form is estimated to take 6 minutes to complete. This time will vary depending upon the needs of the individual case. Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, Washington, DC 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Assistant Commissioner for Patents, Washington, DC 20231.



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office
ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

11033 U.S. PTO
09/812521
03/20/01

DATE: 03.23.01
TO: utility App.
FROM: Office of Initial Patent Examination
Unit 7 (RAM Team)
SUBJECT: Insufficient Funds

Deposit account number 019365

On 03-23-01 there were insufficient funds available to charge the attached fee.

If you have any question, please contact Cynthia Streater (OIPE/JCWS RAM- Team)
at 703-306-5430.

Terminal Operator: Bonathay

Deposit Account Maintenance	
Deposit Account Window Help	
<div> <div>Deposit Account</div> <div>Print Screen</div> </div>	
Number:	010365
Balance Amount:	32.20
Holder	
Name:	ADVANCED MICRO DEVICES INC.
Address	
Attention:	ATT: TECHNOLOGY LAW DEPT.
Street:	ONE AMD PLACE, M/S 68
	P O BOX 3453
Province:	
City:	SUNNYVALE
State:	CA
Postal Code:	94088-3453
Country:	US
Telephone:	(408) 749-2114
Fax:	(408) 774-7483
Details	
Category Code:	NONGOVNMNT
Type:	REGULAR
Notification Amt:	0.00
Status:	<input checked="" type="radio"/> Active <input type="radio"/> Closed
Access Code:	6336
<div> <div>BSAYASHI</div> <div>03/23/2001</div> </div>	



JP 2811

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
DERICK J. WRISTERS
JON D. CHEEK
JOHN G. PELLERIN

Group Art Unit: 2811

Examiner: Unknown

Att'y Docket: 2000.065000/TT4203

Serial No.: 09/812,521

Filed: March 20, 2001

For: TRANSISTOR DEVICE HAVING AN
ENHANCED WIDTH DIMENSION AND
A METHOD OF MAKING SAME

RECEIVED
JUN 26 2001
TC 2800 MAIL ROOM

TRANSMITTAL LETTER

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

CERTIFICATE OF MAILING 37 C.F.R. 1.8	
I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date below:	
June 19, 2001 Date	 Signature

Attached herewith is the Power of Attorney for the above-referenced patent application. This Power of Attorney was originally submitted to the PTO when the application was filed. However, when Applicants received the Notice of Recordation of Assignment Document, they found the Power of Attorney attached thereto.

Respectfully submitted,

Date: June 19, 2001

J. Mike Amerson
Reg. No. 35,426
WILLIAMS, MORGAN & AMERSON
7676 Hillmont, Suite 250
Houston, Texas 77040
(713) 934-4055
(713) 934-7011 (facsimile)

ATTORNEY FOR APPLICANTS

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:

DERICK J. WRISTERS
JON D. CHEEK
JOHN G. PELLERIN



Examiner: Unknown

Group Art Unit: Unknown

Att'y Docket: 2000.065000/TT4203

Serial No.: Unknown

Filed: Concurrently Herewith

For: A TRANSISTOR DEVICE HAVING AN
ENHANCED WIDTH DIMENSION AND
A METHOD OF MAKING SAME

POWER OF ATTORNEY

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

The undersigned, being the inventor named in the above-identified application, hereby revokes any previous Powers of Attorney and appoints:

Elizabeth A. Apperley, Reg. No. 36,428; Bradley Botsch, Reg. No. 34,552; Michael Caywood, Reg. No. 37,797; Daniel R. Collopy, Reg. No. 33,667; Paul S. Drake, Reg. No. 33,491; Rajendra Jaipershad, Reg. No. 44,168; Richard J. Roddy, Reg. No. 27,688; and Harry A. Wolin, Reg. No. 32,638 of Advanced Micro Devices, Inc.; and

Danny L. Williams, Reg. No. 31,892; Terry D. Morgan, Reg. No. 31,181; J. Mike Amerson, Reg. No. 35,426; Kenneth D. Goodman, Reg. No. 30,460; Jeffrey A. Pyle, Reg. No. 34,904; Randall C. Furlong, Reg. No. 35,144; Scott F. Diring, Reg. No. 35,119; George J. Oehling, Reg. No. 40,471; Shelley P.M. Fussey, Reg. No. 39,458; Mark D. Moore, Reg. No. 42,903; Louis H. Iselin, Reg. No. 42,684; Raymund F. Eich, Reg. No. 42,508; Bradley A. Misley, Reg. No. 46,937; and Thomas H. Belvin, Jr., Reg. No. 43,491 of Williams, Morgan & Amerson, P.C.,

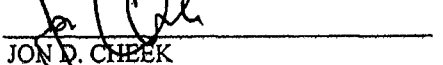
as its attorney or agent so long as they remain with such firms, with full power of substitution and revocation, to prosecute the application, to make alterations and amendments therein, to transact all business in the Patent and Trademark Office in connection therewith, and to receive any Letters Patent, and for one year after issuance of such Letters Patent to file any request for a certificate of correction that may be deemed appropriate.

Please direct all communications as follows:

J. Mike Amerson
WILLIAMS, MORGAN & AMERSON, P.C.
7676 Hillmont, Suite 250
Houston, Texas 77040
(713) 934-7000

Signature: 
DERICK J. WRISTERS

Date: 7/05/01

Signature: 
JON D. CHEEK

Date: 3/12/01

Signature: 
JOHN G. PELLERIN

Date: 3/5/01



UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/812,521	03/20/2001	Derick J. Wristers	2000.065000

CONFIRMATION NO. 2254



OC00000006403335

J. Mike Amerson
Williams, Morgan & Amerson, P.C.
7676 Hillmont, Suite 250
Houston, TX 77040

Date Mailed: 08/09/2001

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/22/2001.

The Power of Attorney in this application is accepted. Correspondence in this application will be mailed to the above address as provided by 37 CFR 1.33.

Sharmilla Coats

Customer Service Center
Initial Patent Examination Division (703) 308-1202 *306-5804*
OFFICE COPY



UNITED STATES PATENT AND TRADEMARK OFFICE

COMMISSIONER FOR PATENTS
UNITED STATES PATENT AND TRADEMARK OFFICE
WASHINGTON, D.C. 20231
www.uspto.gov

APPLICATION NUMBER	FILING DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
09/812,521	03/20/2001	Derick J. Wristers	2000.065000

CONFIRMATION NO. 2254



J. Mike Amerson
Williams, Morgan & Amerson, P.C.
7676 Hillmont, Suite 250
Houston, TX 77040

Date Mailed: 08/09/2001

NOTICE REGARDING POWER OF ATTORNEY

This is in response to the Power of Attorney filed 06/22/2001.

- The Power of Attorney to you in this application has been revoked by the applicant. Future correspondence will be mailed to the new address of record(37 CFR 1.33).

Sharmalle Coats

Customer Service Center
Initial Patent Examination Division (703) 308-1202 306-5804
OFFICE COPY



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,521	03/20/2001	Derick J. Wristers	2000.065000	2254

7590 06/18/2002

J. Mike Amerson
Williams, Morgan & Amerson, P.C.
7676 Hillmont, Suite 250
Houston, TX 77040

EXAMINER

POMPEY, RON EVERETT

ART UNIT	PAPER NUMBER
----------	--------------

2812

DATE MAILED: 06/18/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

09/812,521

Applicant(s)

WRISTERS ET AL.

Examiner

Ron E Pompey

Art Unit

2812

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 1 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☐ Responsive to communication(s) filed on ____.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-55 is/are pending in the application.
- 4a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) ____ is/are allowed.
- 6) ☐ Claim(s) ____ is/are rejected.
- 7) ☐ Claim(s) ____ is/are objected to.
- 8) ☒ Claim(s) 1-55 are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on ____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on ____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. ____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). ____
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) ____ 6) ☐ Other: ____

DETAILED ACTION

Election/Restrictions

1. Restriction to one of the following inventions is required under 35 U.S.C. 121:
 - I. Claims 35-55, drawn to method of making a semiconductor device, classified in class 438, subclass 301.
 - II. Claims 1-34, drawn to a semiconductor device, classified in class 257, subclass 93+.

The inventions are distinct, each from the other because of the following reasons:

2. Inventions of Group I and Group II are related as process of making and product made. The inventions are distinct if either or both of the following can be shown: (1) that the process as claimed can be used to make other and materially different product or (2) that the product as claimed can be made by another and materially different process (MPEP § 806.05(f)). In the instant case the recessed oxide can be etched by wet or dry etching methods..
3. A telephone call was made to Mike Anderson on 6-13-02 to request an oral election to the above restriction requirement, but did not result in an election being made.

Applicant is advised that the reply to this requirement to be complete must include an election of the invention to be examined even though the requirement be traversed (37 CFR 1.143).

Application/Control Number: 09/812,521
Art Unit: 2812

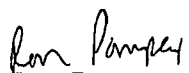
Page 3

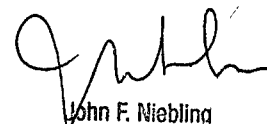
4. Applicant is reminded that upon the cancellation of claims to a non-elected invention, the inventorship must be amended in compliance with 37 CFR 1.48(b) if one or more of the currently named inventors is no longer an inventor of at least one claim remaining in the application. Any amendment of inventorship must be accompanied by a request under 37 CFR 1.48(b) and by the fee required under 37 CFR 1.17(i).

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E Pompey whose telephone number is (703) 305-3016. The examiner can normally be reached on flex schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.


Ron Pompey
Art Unit: 2812
June 17, 2002


John F. Niebling
Supervisory Patent Examiner
Technology Center 2800



COPY OF PAPER
ORIGINALLY FILED

COPY OF PAPERS
ORIGINALLY FILED

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

RECEIVED
JUL 12 2002
TECHNOLOGY CENTER

In re Application of:

DERICK J. WRISTERS
JON D. CHEEK
JOHN G. PELLERIN

Serial No.: 09/812,521

Filed: March 20, 2001

For: TRANSISTOR DEVICE HAVING AN
ENHANCED WIDTH DIMENSION
AND METHOD OF MAKING SAME

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Examiner: Ron Everett Pompey

Group Art Unit: 2812

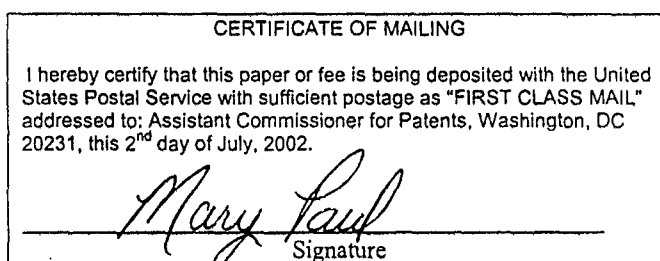
Att'y Docket: 2000.065000/TT4203

#5/ Election
7/23/02
Smith

**RESPONSE TO RESTRICTION
REQUIREMENT DATED JUNE 18, 2002**

Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:



This paper is submitted in response to the Restriction Requirement dated June 18, 2002,
for which the one-month date for response is July 18, 2002.

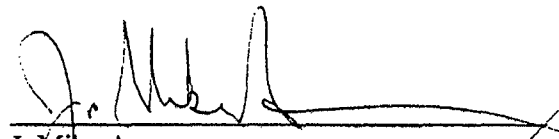
In response to the restriction requirement which the Examiner imposed, Applicant elects,
with traverse, to prosecute claims 1-34, *i.e.*, the Group II claims.

It is believed that no fee is due; however, should any fees under 37 C.F.R. §§ 1.16 to 1.21
be required for any reason relating to this document, the Assistant Commissioner is authorized to
deduct said fees from Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT4203. In
the event the monies in that account are insufficient, the Assistant Commissioner is authorized to
withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No.
50-0786/2000.065000.

The Examiner is invited to contact the undersigned attorney at (713) 934-4055 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

Date: July 2, 2002



J. Mike Amerson
Reg. No. 35,426
WILLIAMS, MORGAN & AMERSON, P.C.
7676 Hillmont, Suite 250
Houston, Texas 77040
(713) 934-4055
(713) 934-7011 (facsimile)

ATTORNEY FOR APPLICANTS



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,521	03/20/2001	Derick J. Wristers	2000.065000	2254

7590 09/25/2002

J. Mike Amerson
Williams, Morgan & Amerson, P.C.
7676 Hillmont, Suite 250
Houston, TX 77040

EXAMINER

POMPEY, RON EVERETT

ART UNIT

PAPER NUMBER

2812

DATE MAILED: 09/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.		Applicant(s)	
	09/812,521		WRISTERS ET AL.	
	Examiner		Art Unit	
	Ron E. Pompey		2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 23 July 2002.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-55 is/are pending in the application.
- 4a) Of the above claim(s) 35-55 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-34 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) Paper No(s). _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

2. Claims 1-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fukatsu (JP2001036048A).

Fukatsu discloses the limitations of:

For Claims 1-34:

a recessed isolation structure formed in said substrate (fig. 4b), said isolation structure defining a recess thereabove;

a gate electrode and a gate insulation layer formed above said substrate (4 and 5, fig. 5), a portion of said gate electrode and said insulation layer extending into said recess above said recessed isolation structure; and

a source and drain region (8 and 9, fig. 2) formed in said substrate.

Fukatsu discloses the claimed invention in general, however fails to disclose the particulars of as disclosed in the claims. Therefore, the examiner takes *official notice* that the gate, gate insulation, isolation material and drain extension region are well known to be used when making a semiconductor device. Also, It would have been obvious to one of ordinary skill in the art at the time the invention was made to form the

Application/Control Number: 09/812,521
Art Unit: 2812


Page 3


trench to the depth and width and the thickness of the electrode and gate insulation as claimed, since it has been held that where the general conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E Pompey whose telephone number is (703) 305-3016. The examiner can normally be reached on flex schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.


Ron Pompey
Art Unit: 2812
September 23, 2002


John F. Niebling
Supervisory Patent Examiner
Technology Center 2800

Notice of References Cited	Application/Control No. 09/812,521	Applicant(s)/Patent Under Reexamination WRISTERS ET AL.	
	Examiner Ron E Pompey	Art Unit 2812	Page 1 of 1

U.S. PATENT DOCUMENTS					
*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	Classification
	A	US-6376313	04-2002	Goebel et al.	
	B	US-5285093	02-1994	Lage et al.	
	C	US-6159801	12-2000	Hsieh et al.	
	D	US-6017801	01-2000	Youn	
	E	US-6133105	10-2000	Chen et al.	
	F	US-6146970	11-2000	Witek et al.	
	G	US-6277697	08-2001	Lee	
	H	US-			
	I	US-			
	J	US-			
	K	US-			
	L	US-			
	M	US-			

FOREIGN PATENT DOCUMENTS						
*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	Classification
	N	JP 2001036048	07-1999	Japan	Fukatsu	
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS		
*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.



UNITED STATES DEPARTMENT OF COMMERCE
Patent and Trademark Office

ASSISTANT SECRETARY AND COMMISSIONER
OF PATENTS AND TRADEMARKS
Washington, D.C. 20231

#7 Change
or
Address
11-27-02
Rstole

CHANGE OF ADDRESS/POWER OF ATTORNEY

FILE LOCATION 28C1 SERIAL NUMBER 09812521 PATENT NUMBER

THE CORRESPONDENCE ADDRESS HAS BEEN CHANGED TO CUSTOMER # 23720

THE PRACTITIONERS OF RECORD HAVE BEEN CHANGED TO CUSTOMER # 23720

THE FEE ADDRESS HAS BEEN CHANGED TO CUSTOMER # 23720

ON 10/28/02 THE ADDRESS OF RECORD FOR CUSTOMER NUMBER 23720 IS:

WILLIAMS MORGAN & AMERSON
7676 HILLMONT
SUITE 250
HOUSTON TX 77040

AND THE PRACTITIONERS OF RECORD FOR CUSTOMER NUMBER 23720 ARE:

30460 31181 31892 34904 35119 35426 39458 40471 42508 42903
48025 52226

RECEIVED
NOV 25 2002
TECHNOLOGY CENTER 2800

PTO INSTRUCTIONS: PLEASE TAKE THE FOLLOWING ACTION WHEN THE
CORRESPONDENCE ADDRESS HAS BEEN CHANGED TO CUSTOMER NUMBER:
RECORD, ON THE NEXT AVAILABLE CONTENTS LINE OF THE FILE JACKET,
'ADDRESS CHANGE TO CUSTOMER NUMBER'. LINE THROUGH THE OLD
ADDRESS ON THE FILE JACKET LABEL AND ENTER ONLY THE 'CUSTOMER
NUMBER' AS THE NEW ADDRESS. FILE THIS LETTER IN THE FILE JACKET.
WHEN ABOVE CHANGES ARE ONLY TO FEE ADDRESS AND/OR PRACTITIONERS
OF RECORD, FILE LETTER IN THE FILE JACKET.
THIS FILE IS ASSIGNED TO GAU 2812.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
DERICK J. WRISTERS
JON D. CHEEK
JOHN G. PELLERIN

Serial No.: 09/812,521

Filed: March 20, 2001

For: A TRANSISTOR DEVICE HAVING AN
ENHANCED WIDTH DIMENSION AND
A METHOD OF MAKING SAME

Group Art Unit: 2812

Examiner: R. Pompey

Atty. Dkt. No.: 2000.065000/TT4203

PATENT

2813/1/1
#9/Response

2/11/03

Smith

RESPONSE TO OFFICE ACTION DATED SEPTEMBER 25, 2002

CERTIFICATE OF MAILING 37 C.F.R. 1.8	
I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date below:	
01-27-03 Date	Kathy H. Jones Signature

RECEIVED
FEB - 6 2003
TECHNOLOGY CENTER 2800

Assistant Commissioner for Patents
Washington, DC 20231

Sir:

This paper is submitted in response to the Office Action dated September 25, 2002 for which the three-month date for response was December 25, 2002.

A request for a one-month extension of time to respond is included herewith along with the required fee. This one-month extension will bring the due date to January 25, 2003, which is within the six-month statutory period. Please note, January 25, 2003 fell on a Saturday,

02/04/2003 ANABI1 00000109 500786 09812521

01 FC:1251 110.00 CH

therefore, the actual due date is January 27, 2003. Should such request or fee be deficient or absent, consider this paragraph such a request and authorization to withdraw the appropriate fee under 37 C.F.R. §§ 1.16 to 1.21 from the Advanced Micro Devices, Inc. Deposit Account No. 01-0365/TT4203. In the event the monies in that account are insufficient, the Assistant Commissioner is authorized to withdraw funds from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2000.065000.

Reconsideration of the application in view of the following remarks is respectfully requested.

REMARKS

In the Office Action, claims 1-34 were rejected under 35 U.S.C. § 103(a) as being obvious over Fukatsu (JP2001036048A). Submitted herewith are the declarations under 37 C.F.R. § 1.131 of the one of the named inventors, Jon D. Cheek, and of the undersigned attorney that recite facts that establish that the Fukatsu patent is not prior art to the present application.

More particularly, the declarations establish that, prior to February 9, 2001, the publication date of the Fukatsu patent, the invention disclosed in the pending application was conceived and that all parties involved in preparing and filing the patent application with the United States Patent and Trademark Office were diligent. Accordingly, the Fukatsu patent is not prior art to the present application.

For the aforementioned reasons, it is respectfully submitted that all claims pending in the present application are in condition for allowance. The Examiner is invited to contact the undersigned attorney at (713) 934-4055 with any questions, comments or suggestions relating to the referenced patent application.

Date:

1/27/03

Respectfully submitted,



J. Mike Amerson

Reg. No. 31,181

WILLIAMS, MORGAN & AMERSON

10333 Richmond Avenue, Suite 1100

Houston, Texas 77042

(713) 934-4055

(713) 934-7011 (facsimile)

ATTORNEY FOR APPLICANTS



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
DERICK J. WRISTERS
JON D. CHEEK
JOHN G. PELLERIN

Serial No.: 09/812,521

Filed: March 20, 2001

For: A TRANSISTOR DEVICE HAVING AN
ENHANCED WIDTH DIMENSION AND
A METHOD OF MAKING SAME

Group Art Unit: 2812

Examiner: R. Pompey

Atty. Dkt. No.: 2000.065000/TT4203

PATENT

2/11/03

John TH

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FEB - 6 2003
TECHNOLOGY CENTER 2800

DECLARATION UNDER 37 C.F.R. § 1.131 OF J. MIKE AMERSON

1. My name is J. Mike Amerson. I am a shareholder in the firm of Williams, Morgan & Amerson. I have personal knowledge of the facts stated herein.

2. I am the attorney within Williams, Morgan & Amerson that prepared and filed application Serial no. 09/812,521, entitled "A transistor device having an enhanced width dimension and a method of making same."

3. On October 6, 2000, I received a request from AMD's legal department to prepare a United States patent application for the invention described in invention disclosure form number TT4203. See Exhibit A. The invention disclosure form is signed by Jon D. Cheek, and it is dated June 29, 2000.

4. At some point after October 6, 2000, I reviewed the invention disclosure form number TT4203, discussed the invention with the inventor identified thereon, Jon D. Cheek, and began preparing the patent application for the invention described in the invention disclosure form.

5. On November 6, 2000, I sent an initial draft of the application to Jon D. Cheek for review. See Exhibit B.

6. At some time after November 6, 2000, I received comments from the inventors regarding the initial draft application. To the extent necessary, I revised the application.

7. On February 26, 2001, I sent a revised copy of the application along with formal papers (assignment, declaration and power of attorney) to AMD for review and the possible execution of the formal papers by the inventors. See Exhibit C.

8. The formal papers for the application were signed on March 5, 2001 by inventors Wristers and Pellerin, and on March 12, 2001 by inventor Cheek.

9. I filed the application on March 20, 2001, with the United States Patent and Trademark Office via Express Mail.

10. I understand that willful false statements and the like so made are punishable by fine or imprisonment, or both, and may jeopardize the validity of the application or any patent issuing thereon.

11. I declare under penalty of perjury that the foregoing is true and correct.

Date:

1/27/03

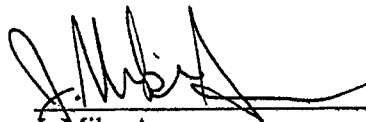

J. Mike Amerson

Exhibit A

05OC2000



5204 E. Ben White Blvd.
Austin, TX 78741
Tel (512) 385-8542

J. MIKE AMERSON
WILLIAMS, MORGAN & AMERSON
7676 HILLMONT, SUITE 250
HOUSTON, TX 77040

RECEIVED

OCT 06 2000

WILLIAMS, MORGAN & AMERSON

RE: Invention Disclosure TT4203

Entitled:

ENHANCEMENT OF MINIMUM WIDTH TRANSISTOR DRIVE CURRENT FOR MA

Dear J. MIKE AMERSON:

2000.065000

Please prepare a US patent application for the subject invention disclosure and file the application in the USPTO within two months of this letter. A copy of the Invention Disclosure is enclosed.

Please follow the instructions set forth in AMD's DIRECTIONS TO OUTSIDE COUNSEL REGARDING PREPARATION AND PROSECUTION OF PATENT APPLICATIONS Version 1.0 dated May 1, 1996.

It is not necessary to prepare a PCT international application at this time. If one is later determined to be needed, AMD will so advise you.

If you have any questions or need additional information, please call me at 512-602-5964, or the responsible AMD Technology Law attorney, PAUL S. DRAKE at 512-602-2103.

Sincerely,

Samantha Cardona
Paralegal
Technology Law Department

Enclosure

cc:

WRISTERS, DERICK J. 63736 (TX) CHEEK, JON D. 65102
PELLERIN, JOHN

AMD INVENTION DISCLOSURE

TLD ID: TT4203

Rec'd date: JUL 03 2000

California x42110, return to MS68,

Texas x55964 return to MS562,

Dresden x83401 Silke Kretschmar at MS-E21-PP

Project: ☐, Product: ☐, Process: ☐, Technology ☒, to which the invention applies (identify):

All CMOS logic technologies

List 2 to 5 key words useful to search by to find patents or art related to this invention:

Field oxide, trench isolation

Working title of invention: Enhancement of minimum width transistor drive current for maximum performance

Inventor's signature: [Signature] date: 6/30/00

Inventor's printed full name: Derick Wristers Citizenship: USA

Employee #: 63736 Extension: 58281 Mail stop: 608 Home telephone: (512) 251-7647

Division: TDG Directorate: LTD Dept #: 7577 Dept: ALTD Manager: Derick Wristers

Residence address: 1904 Terry Cove Austin TX 78728

Post Office address: Same

Co-Inventor's signature: [Signature] date: 6/29/00

Co-Inventor's printed full name: Jon Cheek Citizenship: U.S.A.

Employee #: 65102 Extension: 54592 Mail stop: 608 Home telephone: (512) 246-6204

Division: TDG Directorate: LTD Dept #: 7577 Dept: ALTD Manager: D. Wristers

Residence address: 3602 Newland Place Round Rock, TX 78681

Post Office address:

Co-Inventor's signature: [Signature] date: 6/26/00

Co-Inventor's printed full name: John G. Pellerin Citizenship: USA

Employee #: 67113 Extension: 53398 Mail stop: 608 Home telephone: (512) 301-0160

Division: TDG Directorate: LTD Dept #: 7577 Dept: ALTD Manager: Dirk Wristers

Residence address: 6546 Neudham Lane Austin TX 78739

Post Office address:

Co-Inventor's signature: date:

Co-Inventor's printed full name: Citizenship:

Employee #: Extension: Mail stop: Home telephone: ()

Division: Directorate: Dept #: Dept: Manager:

Residence address:

Post Office address:

List on additional sheet if there are more co-inventors and list total number of inventors here:

Name(s) of attorney(s) preferred by inventor(s) to prepare patent application, if known: DOCKETING

JUL 03 2000

Witness 1 initial: <u>[Signature]</u>	Witness 2 initial: <u>[Signature]</u>	ENTERED
AMD Invention Disclosure.doc DB 7/31/99 printed 6/26/00 11:17 AM page rev 5/10/00		
AMD CONFIDENTIAL		
Page 1		

FILED ID#

Rec'd date

California x42110, return to MS68.

Texas x55964 return to MS562.

Dresden x83401 Silke Kretzschmar at MS E21-PP

Identify known relevant art (patents, publications, products):

State the problem solved by this invention: See attached

Brief description and/or sketch of invention (please attach copies of AMD patent notebook pages, reports or drawings): See attached

Patent notebook # _____ Page numbers _____ Number of drawings _____

Witness 1 initial:

Witness 2 initial:

AMD Invention Disclosure.doc DB 7/31/95 printed: 6/26/00 11:17 AM. page rev 5/10/00

Page 2

AMD CONFIDENTIAL

AMD INVENTION DISCLOSURE

TLD ID#

Rec'd date

California x42110, return to MS68,

Texas x55964 return to MS562,

Dresden x83401 Silke Kretzschmar at MS E21-PP.

Advantages (check all that apply):

<input type="checkbox"/> avoids existing patent(s)	<input type="checkbox"/> improves precision	<input checked="" type="checkbox"/> simplifies manufacturing
<input checked="" type="checkbox"/> new function	<input type="checkbox"/> improves accuracy	<input type="checkbox"/> improves wear characteristic
<input type="checkbox"/> improves density	<input type="checkbox"/> improves efficiency	<input type="checkbox"/> improves signal to noise ratio
<input checked="" type="checkbox"/> increases operating speed	<input type="checkbox"/> fewer component parts	<input type="checkbox"/>
<input type="checkbox"/> improves reliability	<input type="checkbox"/> reduces cost of manufacturing	<input type="checkbox"/>

Discussion of advantage of the invention over other solutions

(emphasize technical advance in the art as measured against known art): This art utilizes processing (to recess the field oxide) which is not limited by processing that is sensitive to small critical dimensions. This art essentially creates a 3D device that occupies the same areal density as a true 2D device.

First written description* of invention, date: <u>5/18/00</u>	First external disclosure to (name):
Date of first drawing*: <u>5/18/00</u>	Date of first external disclosure, none <input type="checkbox"/>
Date invention first reduced to practice:	External disclosure under NDA* No <input type="checkbox"/> Yes <input type="checkbox"/>
Made by (name): <u>Dirk Wristers</u>	First external disclosure or use by: presentation <input type="checkbox"/> ,
Tested by (name):	announcement <input type="checkbox"/> , sample <input type="checkbox"/> , sale <input type="checkbox"/> , other <input type="checkbox"/>
Date of first computer simulation:	Date of Non-Disclosure Agreement*, if any:
Date of first successful test:	Date of first publication*:
any of above occurred outside of USA <input type="checkbox"/>	Publication name:
* attach copy if possible	Date of first commercial use:

Does plan exist to publish, disclose or sell? If so, where and when? NO

Was invention conceived/constructed or tested pursuant to the performance under a development contract with another company: No ☒, Yes ☐. If yes, company name

If yes, name of AMD business contact and contract no.

Was invention jointly developed with participation of inventors from outside AMD: No ☒, Yes ☐.

If yes, Company name

I have read and understood this disclosure and read and signed each page of the attachments:

Witness 1 signature: <u>Thomas E. Spikes Jr.</u>	Date: <u>6-30-00</u>
Printed name: <u>Thomas E. Spikes Jr.</u>	Employee #: <u>77222</u>
Witness 2 signature: <u>John Bush</u>	Date: <u>6/30/2000</u>
Printed name: <u>John Bush</u>	Employee #: <u>63628</u>

After completing to this point, deliver to department reviewer, date delivered

Witness 1 initial: ES Witness 2 initial: JB

AMD Invention Disclosure.doc DB 7/31/95 printed: 6/26/00 11:17 AM page rev 5/10/00

AMD CONFIDENTIAL

Page 3

Rec'd date

Dresden x83401 Silke Kretzschmar at MS E21-PP.

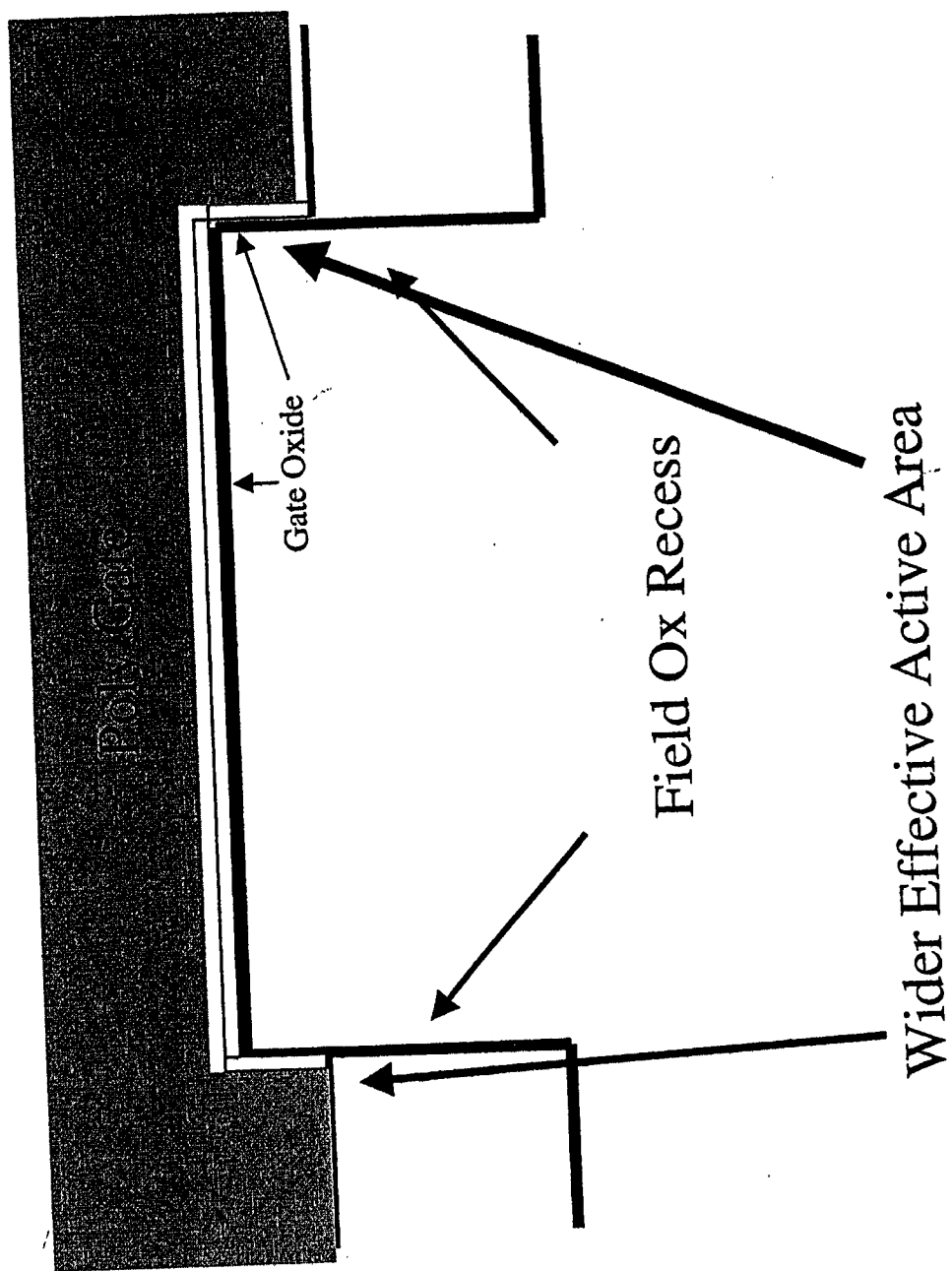
Page 95 of 126

Enhancement of minimum width transistor drive current for maximum performance

Problem: We want more drive current on our minimum devices to drive extrinsic load, but sizing the active area has a negative impact on die size and thus die per wafer (or \$ per wafer). In addition processing limitations in Lithography and Oxide fill limit the size of the feature that can be printed and filled in the active region.

Solution: Intentionally recess the field oxide to provide a "effective" wider device and thus provide more drive current on the minimum transistors. However, this will lead to non-uniform channel doping and thus high transistor leakage degrading the effective performance advantage. Doing the Threshold and/or Halo implants a in 4 pieces each with 1/4 the dose and at 45 degree angle and 4 90degree rotations will dope the channel appropriately(see diagrams)





Handwritten signatures and initials.

Exhibit B

WILLIAMS, MORGAN & AMERSON, P.C.

7676 HILLMONT, SUITE 250, HOUSTON, TX 77040
(713) 934-7000 FAX (713) 934-7011

Danny L. Williams
Terry D. Morgan
J. Mike Amerson
Kenneth D. Goodman
Barbara S. Kitchell, Ph.D.
Jeffrey A. Pyle
Randall C. Furlong, Ph.D.

Scott F. Diring*
George J. Oehling*
Shelley P.M. Fussey, Ph.D.*
Mark D. Moore, Ph.D.*
Carolanne M. King*
Louis H. Iselin, Ph.D.*
Raymund F. Eich, Ph.D.*
Bradley A. Misley*
Thomas H. Belvin, Jr.*

*Patent Agent

Writer's Direct Dial
(713) 934-4055

File: 2000.065000

November 6, 2000

VIA FEDERAL EXPRESS

Mr. Derick J. Wristers
Mr. Jon D. Cheek
Mr. John G. Pellerin
ADVANCED MICRO DEVICES, INC.
5204 E. Ben White Blvd., M/S 568
Austin, TX 78741

*Re: AMD Disclosure Entitled "A TRANSISTOR DEVICE HAVING AN
ENHANCED WIDTH DIMENSION AND A METHOD OF
MAKING SAME"*

*Inventors: Derick J. Wristers, Jon D. Cheek and John G. Pellerin
Your Reference: TT4203; Our Reference: 2000.065000*

Dear Sirs:

Enclosed is a draft application that we have prepared for the above-referenced disclosure. Please spend sufficient time reviewing the entire application so that you understand the content of the application, including each of the claims. You should make sure that the application enables one skilled in the art to make and use the invention and that it discloses the best mode of which you are aware for carrying out the invention.

If the application is inaccurate or incomplete, please mark your changes directly on the application itself and return it to me for revision. Please provide any and all feedback directly to my attention as soon as possible.

In reviewing the application, and especially the claims, keep in mind any relevant prior art of which you are aware. It is important that the claims accurately define your invention and that the claims distinguish over the prior art. If any prior art comes to your attention now or during the pendency of the application, please send it to me.

WILLIAMS, MORGAN & AMERSON, P.C.

Mr. Derick J. Wristers
Mr. Jon D. Cheek
Mr. John G. Pellerin
November 6, 2000
Page 2

We would like to take this opportunity to address several important matters:

Information Disclosure Statement

As we have discussed, a duty of candor and good faith toward the Patent Office rests on the inventors and on every other individual who is substantively involved in the preparation or prosecution of a patent application. All such individuals have a duty to disclose to the Office known information that may be material to the patentability of a pending claim. Such information is material to patentability when: (1) it establishes, by itself or in combination with other information, a *prima facie* case of unpatentability; or (2) it refutes, or is inconsistent with a position the applicant takes in (a) opposing an argument of unpatentability relied on by the patent examiner, or (b) asserting an argument of patentability.

An Information Disclosure Statement should therefore be filed in the Patent Office within about three months of the filing date of the patent application to comply with this duty of disclosure, listing material publications or pertinent information of which you are aware. This includes:

- (a) products or services in public use or on sale in this country prior to your U.S. filing date;
- (b) all related material (including international patent applications) published in this country or a foreign country prior to your U.S. filing date;
- (c) any related U.S. patents; and
- (d) any pertinent applications published prior to your filing date.

We request that you supply us with copies of all material prior art references of which you are aware and any other information which should be disclosed to the Patent Office. We would like to file the Information Disclosure Statement within 3 months of the filing date, so we need you to supply the copies to us about a month prior to that time. Please feel free to call me if you have any questions as to what should be included.

Continuing Duty of Candor

We would like to emphasize that the duty of candor does not cease once the Information Disclosure Statement has been filed. The duty remains throughout examination of the patent application. Therefore, if any additional information of relevance comes to your attention during examination of this patent application, it is important that you advise us immediately so that such information can be submitted to the Patent Office.

WILLIAMS, MORGAN & AMERSON, P.C.

Mr. Derick J. Wristers
Mr. Jon D. Cheek
Mr. John G. Pellerin
November 6, 2000
Page 3

Furthermore, for as long as any patent that may be granted on this patent application is of value to you, we recommend that you keep us advised of any relevant information that comes to light. We can then consider such and advise on options such as limiting the claims to avoid such prior art by filing an application for a reissue patent or an application for reexamination.

Developments and Improvements

It is important that you advise us promptly of any developments or improvements that may affect the uses or value of this invention. You should insure, in particular, that you advise us of such developments or improvements before any disclosure or public use has occurred. If such developments or improvements are of sufficient importance, it may be possible, and indeed advisable, to take immediate steps to secure specific protection for such developments or improvements. This could be done by filing a continuation-in-part patent application, or by filing a new independent patent application, both of which probably require administrative approval.

Examination

In general, an Examiner reviews applications in the order in which they are received. A first office action may be issued within a year, although the time period may vary.

Marking

In commercial exploitation of this invention, it is advisable to mark articles and literature relating to the invention to indicate that a patent application is pending. The notation "Patent Pending" or "Patent Applied For" may be used in connection with any product covered by any claim of the application. This notation may also be used in any advertising, business literature or scientific publication. Products or methods relating to claims in the patent application may be conveniently identified in footnotes as being subjects of one or more pending patent applications. It is usually advisable, however, not to disclose the serial number or filing date of the patent application while it is still pending.

Maintenance Fees

Maintenance fees become payable on all patents (and reissue patents) which issue on applications filed on or after December 12, 1980. The maintenance fees are payable before the expiration of a period of 3½ years, a period of 7½ and a period of 11½ years respectively, calculated from the date of patent issue. There is a six-month grace period for payment of such maintenance fees.

WILLIAMS, MORGAN & AMERSON, P.C.

Mr. Derick J. Wristers
Mr. Jon D. Cheek
Mr. John G. Pellerin
November 6, 2000
Page 4

We will docket the relevant dates in our in-house computer system upon issue of the patent and attempt to advise you accordingly at the appropriate intervals. However, since reminders may not reach you, and since mailing addresses and circumstances can change over time, *Williams, Morgan & Amerson, P.C. does not assume responsibility for reminding patent owners of payment deadlines, nor for ensuring that annuities are in fact paid on time.*

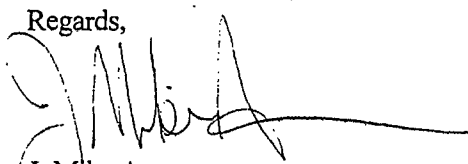
Corresponding Patent Protection in Other Countries

The United States and many other countries are parties to an international treaty called the Paris Convention. Under this treaty you may file a corresponding patent application in any of these other countries and claim the benefit of your United States filing date, provided that the corresponding application is filed within one year from the day on which your United States application was filed. Certain events might have occurred or may occur that will require corresponding foreign applications to be filed before the end of this one-year convention period.

Unless you have concluded that you do not want any corresponding foreign patent applications, you should take this matter up with us as soon as possible. We can then discuss the benefits, requirements, filing procedures, and costs of foreign coverage.

If we can be of further assistance, or if you have any questions concerning the patent application, the preparation of an Information Disclosure Statement, or any of the above topics, please contact us at your convenience.

Regards,



J. Mike Amerson

JMA/mp

Enclosure

cc: Paul S. Drake, Esq. (w/enc.)

Exhibit C

WILLIAMS, MORGAN & AMERSON, P.C.

7676 HILLMONT, SUITE 250, HOUSTON, TX 77040
(713) 934-7000 FAX (713) 934-7011

Danny L. Williams
Terry D. Morgan
J. Mike Amerson
Kenneth D. Goodman
Jeffrey A. Pyle
Randall C. Furlong, Ph.D.
Jaison C. John

Scott F. Diring*
George J. Oehling*
Shelley P.M. Fussey, Ph.D.*
Mark D. Moore, Ph.D.*
Louis H. Iselin, Ph.D.*
Raymund F. Eich, Ph.D.*
Bradley A. Misley*
Thomas H. Belvin, Jr.*

*Patent Agent

Writer's Direct Dial
(713) 934-4055

File: 2000.065000

February 26, 2001

VIA FEDERAL EXPRESS

Mr. Derick J. Wristers
Mr. Jon D. Cheek
Mr. John G. Pellerin
ADVANCED MICRO DEVICES, INC.
5204 E. Ben White Blvd., M/S 568
Austin, TX 78741

*Re: AMD Disclosure Entitled "A TRANSISTOR DEVICE HAVING AN
ENHANCED WIDTH DIMENSION AND A METHOD OF
MAKING SAME"*

*Inventors: Derick J. Wristers, Jon D. Cheek and John G. Pellerin
Your Reference: TT4203; Our Reference: 2000.065000*

Dear Sirs:

Enclosed is a patent application for the above-referenced AMD disclosure **for review by all of the inventors**. Also enclosed are the Declaration, Assignment, and Power of Attorney which should be executed by all of the inventors.

Please review the patent specification carefully to ensure its accuracy. If minor corrections or modifications are necessary, please mark the changes directly on the application. If extensive modification is necessary, please return the application to me for correction prior to execution of the formal papers.

If the application is ready for filing with the U.S. Patent and Trademark Office, please read the Declaration, Assignment, and Power of Attorney carefully to ensure that you understand them and sign and date the documents in the appropriate places. **The Assignment should be**

WILLIAMS, MORGAN & AMERSON, P.C.

Mr. Derick J. Wristers
Mr. Jon D. Cheek
Mr. John G. Pellerin
February 26, 2001
Page 2

signed in the presence of a Notary Public. Additionally, please be sure your home addresses on the second page of the Declaration are correct.

Please return the application, as well as the executed documents, at your earliest convenience, for filing in the U.S. Patent and Trademark Office.

Information Disclosure Statement

A duty of candor and good faith toward the Patent Office rests on the inventors and on every other individual who is substantively involved in the preparation or prosecution of a patent application. All such individuals have a duty to disclose to the Office known information that may be material to the patentability of a pending claim. Such information is material to patentability when: (1) it establishes, by itself or in combination with other information, a *prima facie* case of unpatentability; or (2) it refutes, or is inconsistent with a position the applicant takes in (a) opposing an argument of unpatentability relied on by the patent examiner, or (b) asserting an argument of patentability.

An Information Disclosure Statement should therefore be filed in the Patent Office within about three months of the filing date of the patent application to comply with this duty of disclosure, listing material publications or pertinent information of which you are aware. This includes:

- (a) products or services in public use or on sale in this country prior to your U.S. filing date;
- (b) all related material (including international patent applications) published in this country or a foreign country prior to your U.S. filing date;
- (c) any related U.S. patents; and
- (d) any pertinent applications published prior to your filing date.

We request that you supply us with copies of all material prior art references of which you are aware and any other information which should be disclosed to the Patent Office. We would like to file the Information Disclosure Statement within 3 months of the filing date, so we need you to supply the copies to us about a month prior to that time. Please feel free to call me if you have any questions as to what should be included.

WILLIAMS, MORGAN & AMERSON, P.C.

Mr. Derick J. Wristers
Mr. Jon D. Cheek
Mr. John G. Pellerin
February 26, 2001
Page 3

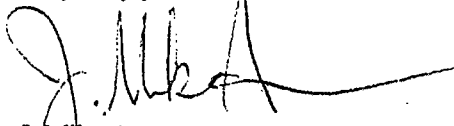
Continuing Duty of Candor

We would like to emphasize that the duty of candor does not cease once the Information Disclosure Statement has been filed. The duty remains throughout examination of the patent application. Therefore, if any additional information of relevance comes to your attention during examination of this patent application, it is important that you advise us immediately so that such information can be submitted to the Patent Office.

Furthermore, for as long as any patent that may be granted on this patent application is of value to you, we recommend that you keep us advised of any relevant information that comes to light. We can then consider such and advise on options such as limiting the claims to avoid such prior art by filing an application for a reissue patent or an application for reexamination.

If you have any questions, please call or fax me at your convenience.

Very truly yours,



J. Mike Amerson

JMA/mp

Enclosures

cc: Paul S. Drake, Esq. (w/o enc.)
Ms. Samantha Cardona (w/o enc.)

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PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
DERICK J. WRISTERS
JON D. CHEEK
JOHN G. PELLERIN

Group Art Unit: 2812

Examiner: R. Pompey

Serial No.: 09/812,521

Atty. Dkt. No.: 2000.065000/TT4203

Filed: March 20, 2001

For: **A TRANSISTOR DEVICE HAVING AN
ENHANCED WIDTH DIMENSION AND
A METHOD OF MAKING SAME**


DECLARATION UNDER 37 C.F.R. § 1.131 OF JON D. CHEEK

1. My name is Jon D. Cheek. I have personal knowledge of the facts stated herein.
2. I am currently employed with Advanced Micro Devices, Inc. in Austin, Texas. I am a named inventor on application Serial No. 09/812,521 entitled "A transistor device having an enhanced width dimension and a method of making same."
3. Attached as Exhibit A is a copy of the invention disclosure form I prepared in Austin, Texas for the invention described in the above-referenced patent application. I prepared and signed the invention disclosure form on June 29, 2000, as indicated by the date adjacent my signature.
4. The attached invention disclosure form was provided with internal tracking number TT4203 by AMD's legal department, and it was sent to the law firm of Williams, Morgan & Amerson on or about October 5, 2000, with a request to prepare a United States patent application for the invention disclosed in the invention form.

5. I understand that willful false statements and the like so made are punishable by fine or imprisonment, or both, and may jeopardize the validity of the application or any patent issuing thereon.

6. I declare under penalty of perjury that the foregoing is true and correct.

1/21/03
Date


Jon D. Cheek

Notice of Allowability	Application No.	Applicant(s)	
	09/812,521	WRISTERS ET AL.	
	Examiner	Art Unit	
	Ron E Pompey	2812	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--
All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS. This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to 2-11-03.
 2. ☒ The allowed claim(s) is/are 1-34.
 3. ☒ The drawings filed on 20 March 2001 are accepted by the Examiner.
 4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 - a) ☐ All b) ☐ Some* c) ☐ None of the:
 1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
- * Certified copies not received: _____.
5. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
 - (a) ☐ The translation of the foreign language provisional application has been received.
 6. ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application. THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

7. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.
8. ☐ CORRECTED DRAWINGS must be submitted.
 - (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
 - 1) ☐ hereto or 2) ☐ to Paper No. _____.
 - (b) ☐ including changes required by the proposed drawing correction filed _____, which has been approved by the Examiner.
 - (c) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No. _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the top margin (not the back) of each sheet. The drawings should be filed as a separate paper with a transmittal letter addressed to the Official Draftsperson.

9. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

- | | |
|--|---|
| 1 <input type="checkbox"/> Notice of References Cited (PTO-892) | 2 <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3 <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 4 <input type="checkbox"/> Interview Summary (PTO-413), Paper No. _____ |
| 5 <input type="checkbox"/> Information Disclosure Statements (PTO-1449), Paper No. _____ | 6 <input checked="" type="checkbox"/> Examiner's Amendment/Comment |
| 7 <input type="checkbox"/> Examiner's Comment Regarding Requirement for Deposit of Biological Material | 8 <input checked="" type="checkbox"/> Examiner's Statement of Reasons for Allowance |
| | 9 <input type="checkbox"/> Other |

EXAMINER'S AMENDMENT

#10
Am J A

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

The application has been amended as follows:

Cancel claims 35-55.

Allowable Subject Matter

2. Claims 1-34 are allowed.
3. The following is an examiner's statement of reasons for allowance: the prior art of record fails to disclose the limitations of:

a recessed isolation structure formed in said substrate, said isolation structure defining a recess there above;

a gate electrode and a gate insulation layer formed above said substrate, a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure; and

a source and drain region formed in said substrate.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."


Application/Control Number: 09/812,521
Art Unit: 2812

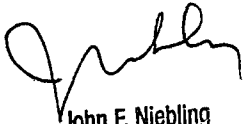
Page 3

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ron E Pompey whose telephone number is (703) 305-3016. The examiner can normally be reached on flex schedule.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John Niebling can be reached on (703) 308-3325. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 305-3432 for regular communications and (703) 305-3432 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.


Ron Pompey
Art Unit: 2812
March 10, 2003


John F. Niebling
Supervisory Patent Examiner
Technology Center 2800



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

NOTICE OF ALLOWANCE AND FEE(S) DUE

023720 7590 03/11/2003
WILLIAMS, MORGAN & AMERSON, P.C.
10333 RICHMOND, SUITE 1100
HOUSTON, TX 77042

EXAMINER	
POMPEY, RON EVERETT	
ART UNIT	CLASS-SUBCLASS
2812	257-330000

DATE MAILED: 03/11/2003

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,521	03/20/2001	Derick J. Wristers	2000.065000	2254

TITLE OF INVENTION: TRANSISTOR DEVICE HAVING AN ENHANCED WIDTH DIMENSION AND A METHOD OF MAKING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1300	\$0	\$1300	06/11/2003

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE REFLECTS A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE APPLIED IN THIS APPLICATION. THE PTOL-85B (OR AN EQUIVALENT) MUST BE RETURNED WITHIN THIS PERIOD EVEN IF NO FEE IS DUE OR THE APPLICATION WILL BE REGARDED AS ABANDONED.

HOW TO REPLY TO THIS NOTICE:

I. Review the SMALL ENTITY status shown above.

If the SMALL ENTITY is shown as YES, verify your current SMALL ENTITY status:

- A. If the status is the same, pay the TOTAL FEE(S) DUE shown above.
- B. If the status is changed, pay the PUBLICATION FEE (if required) and twice the amount of the ISSUE FEE shown above and notify the United States Patent and Trademark Office of the change in status, or

If the SMALL ENTITY is shown as NO:

- A. Pay TOTAL FEE(S) DUE shown above, or
- B. If applicant claimed SMALL ENTITY status before, or is now claiming SMALL ENTITY status, check the box below and enclose the PUBLICATION FEE and 1/2 the ISSUE FEE shown above.
- ☐ Applicant claims SMALL ENTITY status.
See 37 CFR 1.27.

II. PART B - FEE(S) TRANSMITTAL should be completed and returned to the United States Patent and Trademark Office (USPTO) with your ISSUE FEE and PUBLICATION FEE (if required). Even if the fee(s) have already been paid, Part B - Fee(s) Transmittal should be completed and returned. If you are charging the fee(s) to your deposit account, section "4b" of Part B - Fee(s) Transmittal should be completed and an extra copy of the form should be submitted.

III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Box ISSUE FEE unless advised to the contrary.

IMPORTANT REMINDER: Utility patents issuing on applications filed on or after Dec. 12, 1980 may require payment of maintenance fees. It is patentee's responsibility to ensure timely payment of maintenance fees when due.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail** Box ISSUE FEE
Commissioner for Patents
Washington, D.C. 20231
Fax (703)746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)
023720 7590 03/11/2003

WILLIAMS, MORGAN & AMERSON, P.C.
10333 RICHMOND, SUITE 1100
HOUSTON, TX 77042

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission
I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above, or being facsimile transmitted to the USPTO, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,521	03/20/2001	Derick J. Wristers	2000.065000	2254

TITLE OF INVENTION: TRANSISTOR DEVICE HAVING AN ENHANCED WIDTH DIMENSION AND A METHOD OF MAKING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1300	\$0	\$1300	06/11/2003

EXAMINER	ART UNIT	CLASS-SUBCLASS
POMPEY, RON EVERETT	2812	257-330000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1 _____
2 _____
3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent) ☐ individual ☐ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

- ☐ Issue Fee
☐ Publication Fee
☐ Advance Order - # of Copies _____

4b. Payment of Fee(s):

- ☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☐ The Commissioner is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature)

(Date)

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant; a registered attorney or agent; or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

This collection of information is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, Washington, D.C. 20231. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, Washington, DC 20231.

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE(S)

PTOL-85 (REV. 04-02) Approved for use through 01/31/2004. OMB 0651-0033

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,521	03/20/2001	Derick J. Wristers	2000.065000	2254
023720	7590	03/11/2003	EXAMINER	
WILLIAMS, MORGAN & AMERSON, P.C. 10333 RICHMOND, SUITE 1100 HOUSTON, TX 77042			POMPEY, RON EVERETT	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 03/11/2003

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b)
(application filed on or after May 29, 2000)

The patent term adjustment to date is 0 days. If the issue fee is paid on the date that is three months after the mailing date of this notice and the patent issues on the Tuesday before the date that is 28 weeks (six and a half months) after the mailing date of this notice, the term adjustment will be 0 days.

If a continued prosecution application (CPA) was filed in the above-identified application, the filing date that determines patent term adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) system. (<http://pair.uspto.gov>)

Any questions regarding the patent term extension or adjustment determination should be directed to the Office of Patent Legal Administration at (703)305-1383.



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER OF PATENTS AND TRADEMARKS
Washington, D.C. 20231
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,521	03/20/2001	Derick J. Wristers	2000.065000	2254
023720	7590	03/11/2003	EXAMINER	
WILLIAMS, MORGAN & AMERSON, P.C. 10333 RICHMOND, SUITE 1100 HOUSTON, TX 77042 UNITED STATES			POMPEY, RON EVERETT	
			ART UNIT	PAPER NUMBER
			2812	

DATE MAILED: 03/11/2003

Notice of Fee Increase on January 1, 2003

If a reply to a "Notice of Allowance and Fee(s) Due" is filed in the Office on or after January 1, 2003, then the amount due will be higher than that set forth in the "Notice of Allowance and Fee(s) Due" since there will be an increase in fees effective on January 1, 2003. See Revision of Patent and Trademark Fees for Fiscal Year 2003: Final Rule, 67 Fed. Reg. 70847, 70849 (November 27, 2002).

The current fee schedule is accessible from: <http://www.uspto.gov/main/howtofees.htm>.

If the issue fee paid is the amount shown on the "Notice of Allowance and Fee(s) Due," but not the correct amount in view of the fee increase, a "Notice to Pay Balance of Issue Fee" will be mailed to applicant. In order to avoid processing delays associated with mailing of a "Notice to Pay Balance of Issue Fee," if the response to the Notice of Allowance and Fee(s) due form is to be filed on or after January 1, 2003 (or mailed with a certificate of mailing on or after January 1, 2003), the issue fee paid should be the fee that is required at the time the fee is paid. If the issue fee was previously paid, and the response to the "Notice of Allowance and Fee(s) Due" includes a request to apply a previously-paid issue fee to the issue fee now due, then the difference between the issue fee amount at the time the response is filed and the previously paid issue fee should be paid. See Manual of Patent Examining Procedure, Section 1308.01 (Eighth Edition, August 2001).

Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at (703) 305-8283.

PART B - FEE(S) TRANSMITTAL

Complete and send this form, together with applicable fee(s), to: **Mail Box ISSUE FEE**
Commissioner for Patents
Washington, D.C. 20231
Fax (703)746-4000

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 4 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Legibly mark-up with any corrections or use Block 1)

023720 7590 03/11/2003

WILLIAMS, MORGAN & AMERSON, P.C.
 10333 RICHMOND, SUITE 1100
 HOUSTON, TX 77042



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Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Box Issue Fee address above, or being facsimile transmitted to the USPTO, on the date indicated below.

(Depositor's name) Kathryn Danks
 (Signature) Kathryn Danks
 (Date) April 9, 2003

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/812,521	03/20/2001	Derick J. Wisters	2000.065000	2254

TITLE OF INVENTION: TRANSISTOR DEVICE HAVING AN ENHANCED WIDTH DIMENSION AND A METHOD OF MAKING SAME

APPLN. TYPE	SMALL ENTITY	ISSUE FEE	PUBLICATION FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1300	\$0	\$1300	06/11/2003

EXAMINER	ART UNIT	CLASS-SUBCLASS
POMPEY, RON EVERETT	2812	257-330000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

- ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.
☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.

2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

Williams, Morgan &
 Amerson

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. Inclusion of assignee data is only appropriate when an assignment has been previously submitted to the USPTO or is being submitted under separate cover. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

ADVANCED MICRO DEVICES, INC.

AUSTIN, TEXAS

Please check the appropriate assignee category or categories (will not be printed on the patent) ☐ individual ☒ corporation or other private group entity ☐ government

4a. The following fee(s) are enclosed:

- ☒ Issue Fee
☐ Publication Fee

☒ Advance Order - # of Copies 3

4b. Payment of Fee(s):

- ☐ A check in the amount of the fee(s) is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.

☒ The Commissioner is hereby authorized by charge the required fee(s), or credit any overpayment, to Deposit Account Number 01-0365/TP4-203 in extra copy of this form).

Commissioner for Patents is requested to apply the Issue Fee and Publication Fee (if any) or to re-apply any previously paid issue fee to the application identified above.

(Authorized Signature)

(Date)

[Signature]

4/9/03

NOTE: The Issue Fee and Publication Fee (if required) will not be accepted from anyone other than the applicant, a registered attorney or agent, or the assignee or other party in interest as shown by the records of the United States Patent and Trademark Office.

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Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

TRANSMIT THIS FORM WITH FEE(S)

PTOL-85 (REV. 04-02) Approved for use through 01/31/2004. OMB 0651-0033

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

04/16/2003 EAREGAY2 00000231 010365 09812521
 01 FC:1501
 02 FC:8001 1300.00 CH
 9.00 CH

File History Content Report

The following content is missing from the original file history record obtained from the United States Patent and Trademark Office. No additional information is available.

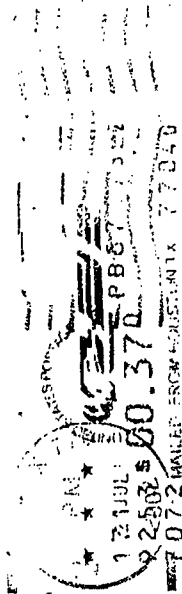
Document Date - 2003-06-17

Document Title - USPTO Grant

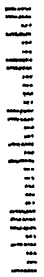
BEST COPY

WILLIAMS, MORGAN & AMERSON, P.C.

7676 HILLMONT, ST. 250
HOUSTON, TEXAS 77040



ASSISTANT COMMISSIONER OF PATENTS
WASHINGTON, DC 20231



PATENT APPLICATION FEE DETERMINATION RECORD
Effective October 1, 2000

Application or Docket Number
09812521

CLAIMS AS FILED - PART I

	(Column 1)	(Column 2)
TOTAL CLAIMS	55	
FOR	NUMBER FILED	NUMBER EXTRA
TOTAL CHARGEABLE CLAIMS	55 minus 20 =	* 35
INDEPENDENT CLAIMS	5 minus 3 =	* 2
MULTIPLE DEPENDENT CLAIM PRESENT <input type="checkbox"/>		

* If the difference in column 1 is less than zero, enter "0" in column 2

CLAIMS AS AMENDED - PART II

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT A	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**
Independent	*	Minus	***
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT B	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**
Independent	*	Minus	***
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

	(Column 1)	(Column 2)	(Column 3)
AMENDMENT C	CLAIMS REMAINING AFTER AMENDMENT	HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA
Total	*	Minus	**
Independent	*	Minus	***
FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM <input type="checkbox"/>			

- * If the entry in column 1 is less than the entry in column 2, write "0" in column 3.
 ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20."
 *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3."
 The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.

SMALL ENTITY TYPE ☐ OR

OTHER THAN SMALL ENTITY

RATE	FEE
BASIC FEE	355.00
X\$ 9=	
X40=	
+135=	
TOTAL	

RATE	FEE
BASIC FEE	710.00
X\$18=	630
X80=	160
+270=	0
TOTAL	1500

SMALL ENTITY OR

OTHER THAN SMALL ENTITY

RATE	ADDI-TIONAL FEE
X\$ 9=	
X40=	
+135=	
TOTAL	

RATE	ADDI-TIONAL FEE
X\$18=	
X80=	
+270=	
TOTAL	

RATE	ADDI-TIONAL FEE
X\$ 9=	
X40=	
+135=	
TOTAL	

RATE	ADDI-TIONAL FEE
X\$18=	
X80=	
+270=	
TOTAL	

RATE	ADDI-TIONAL FEE
X\$ 9=	
X40=	
+135=	
TOTAL	

RATE	ADDI-TIONAL FEE
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X80=	
+270=	
TOTAL	

CLAIMS ONLY

SERIAL NO.	09812521	FILING DATE
APPLICANT(S)		

CLAIMS

	AS FILED		AFTER 1st AMENDMENT		AFTER 2nd AMENDMENT	
	IND.	DEP.	IND.	DEP.	IND.	DEP.
1						
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TOTAL IND.	5					
TOTAL DEP.	50					
TOTAL CLAIMS	55					

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TOTAL IND.						
TOTAL DEP.						
TOTAL CLAIMS						

* MAY BE USED FOR ADDITIONAL CLAIMS OR ADMENDMENTS

U.S.DEPARTMENT OF COMMERCE
Patent and Trademark Office

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Search results for: pns=(US6580122);

Collections searched: DWPI, US Granted, Australian Innovation, Canadian Applications, US Applications, Australian Granted, French Granted, French Applications, European Granted, Australian Applications, German Utility Models, European Applications, British Applications, British Granted, German Granted, WIPO Applications, Canadian Granted, German Applications, Russian Utility Models, Russian Applications, Chinese Utility Models, Indonesian Simple, Korean Utility Models, Singaporean Applications, Chinese Granted, Indonesian Applications, Korean Granted/Examined, Thai Granted/Examined, Chinese Applications, Japanese Utility Models, Korean Applications, Vietnamese Granted, Indian Granted, Japanese Granted, Malaysian Granted, Vietnamese Applications, Indian Applications, Japanese Applications, Singaporean Granted, Argentinean Utility Models, Argentinean Applications, Mexican Granted, Brazilian Utility Models, Mexican Applications, Brazilian Granted, Brazilian Applications, Other Authorities

Table of Contents

1. US6580122B1 Transistor device having an enhanced width dimension and a method of making same

Family 1/1**1 record(s) per family**

Record 1/1 US6580122B1 Transistor device having an enhanced width dimension and a method of making same

Publication Number: US6580122B1 20030617

Title: Transistor device having an enhanced width dimension and a method of making same

Title - DWPI: Transistor, for use in integrated circuit device, comprises semiconducting substrate, recessed isolation structure, gate electrode, gate insulation layer and source/drain regions

Priority Number: US2001812521A

Priority Date: 2001-03-20

Application Number: US2001812521A

Application Date: 2001-03-20

Publication Date: 2003-06-17

IPC Class Table:

IPC	Section	Class	Subclass	Class Group	Subgroup
G01N0027414	G	G01	G01N	G01N0027	G01N0027414

IPC Class Table - DWPI:

IPC - DWPI	Section - DWPI	Class - DWPI	Subclass - DWPI	Class Group - DWPI	Subgroup - DWPI
H01L002976 (IPC 1-7)	H	H01	H01L	H01L0029	H01L002976 (IPC 1-7)
H01L00213205 (IPC 1-7)	H	H01	H01L	H01L0021	H01L00213205 (IPC 1-7)
H01L0021336 (IPC 1-7)	H	H01	H01L	H01L0021	H01L0021336 (IPC 1-7)
H01L002994 (IPC 1-7)	H	H01	H01L	H01L0029	H01L002994 (IPC 1-7)
H01L0031062 (IPC 1-7)	H	H01	H01L	H01L0031	H01L0031062 (IPC 1-7)
H01L0031113 (IPC 1-7)	H	H01	H01L	H01L0031	H01L0031113 (IPC 1-7)

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H01L0031119 (IPC 1-7)	H	H01	H01L	H01L0031	H01L0031119 (IPC 1-7)
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Assignee/Applicant: Advanced Micro Devices Inc.,Austin,TX

JP F Terms:

JP FI Codes:

Assignee - Original: Advanced Micro Devices Inc.

Any CPC Table:

Type	Invention	Additional	Version	Office
Current	G01N 27/414	-	20130101	EP

ECLA: G01N0027414

Abstract:

The present invention is directed to a transistor having an enhanced width dimension and a method of making same. In one illustrative embodiment, the transistor comprises a semiconducting substrate, a recessed isolation structure formed in the substrate, the isolation structure defining a recess thereabove, a gate electrode and a gate insulation layer positioned above the substrate, a portion of the gate electrode and the gate insulation layer extending into the recess above the recessed isolation structure, and a source region and a drain region formed in the substrate. In another illustrative embodiment, the transistor comprises a semiconducting substrate, a recessed isolation structure that defines an active area having an upper surface and an exposed sidewall surface, a gate insulation layer and a gate electrode positioned above a portion of the upper surface and a portion of the exposed sidewall surface of the active area, and a source region and a drain region formed in the active area.

Language of Publication: EN

INPADOC Legal Status Table:

Gazette Date	Code	INPADOC Legal Status Impact
2018-07-06	AS	-
Description: ASSIGNMENT INNOVATIVE FOUNDRY TECHNOLOGIES LLC, NEW HAMPSHIRE ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNOR:ADVANCED MICRO DEVICES, INC.; REEL/FRAME:047014/0777 2018-06-26		
2014-11-19	FPAY	+
Description: FEE PAYMENT FEE PAYMENT YEAR 12		

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2010-11-22	FPAY	+
Description: FEE PAYMENT FEE PAYMENT YEAR 8		
2006-11-16	FPAY	+
Description: FEE PAYMENT FEE PAYMENT YEAR 4		
2003-05-29	STCF	-
Description: INFORMATION ON STATUS: PATENT GRANT PATENTED CASE		
2001-03-20	AS	-
Description: ASSIGNMENT ADVANCED MICRO DEVICES, INC., TEXAS ASSIGNMENT OF ASSIGNORS INTEREST; ASSIGNORS:WRISTERS, DERICK J.; CHEEK, JON D.; PELLERIN, JOHN G.; REEL/FRAME:011633/0354; SIGNING DATES FROM 20010305 TO 20010312		

Post-Issuance (US):

Reassignment (US) Table:

Assignee	Assignor	Date Signed	Reel/Frame	Date
INNOVATIVE FOUNDRY TECHNOLOGIES LLC,PORTSMOUTH,NH,US	ADVANCED MICRO DEVICES, INC.	2018-06-26	047014/0777	2018-07-06
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: CATHERINE XU ONE FINANCIAL CENTER MINTZ LEVIN BOSTON, MA 02111				
ADVANCED MICRO DEVICES INC.,AUSTIN,TX,US	WRISTERS, DERICK J.	2001-03-05	011633/0354	2001-03-20
	CHEEK, JON D.	2001-03-12	-	-
	PELLERIN, JOHN G.	2001-03-05	-	-
Conveyance: ASSIGNMENT OF ASSIGNORS INTEREST (SEE DOCUMENT FOR DETAILS).				
Corresponent: WILLIAMS, MORGAN & AMERSON, PC J. MIKE AMERSON 7676 HILLMONT, SUITE 250 HOUSTON, TX 77040				

Maintenance Status (US):

Litigation (US): 2019-12-20 2019 Innovative Foundry Technologies LLC Semiconductor Manufacturing International Corporation Broadcom Incorporated Broadcom Corporation Cypress

SMIC Ex. 1012

IPR2020-01003

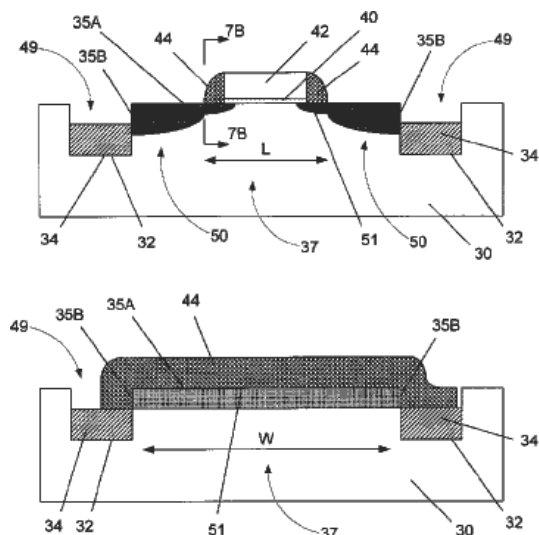
Page 124 of 126

Opposition (EP):

License (EP):

EPO Procedural Status:

Front Page Drawing:



Assignee - Current US: INNOVATIVE FOUNDRY TECHNOLOGIES LLC



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United States Patent and Trademark Office

Office of the Commissioner for Patents

TRANSISTOR DEVICE HAVING AN ENHANCED WIDTH DIMENSION AND A METHOD OF MAKING SAME

PATENT #
6580122

APPLICATION #
09812521

FILING DATE
03/20/2001

ISSUE DATE
06/17/2003

Payment Window Status

WINDOW
11.5 Year

STATUS
Closed

FEES
Paid

No maintenance
fees are due.

Window	First Day to Pay	Surcharge Starts	Last Day to Pay	Status	Fees
3.5 Year	06/17/2006	12/19/2006	06/18/2007	Closed	Paid
7.5 Year	06/17/2010	12/18/2010	06/17/2011	Closed	Paid
11.5 Year	06/17/2014	12/18/2014	06/17/2015	Closed	Paid

Patent Holder Information

Customer # 23720

Entity Status UNDISCOUNTED

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6464 Savoy
Suite 600
HOUSTON, TX 77036
UNITED STATES

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IPR2020-01003

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