



CHAPTER 4

MOS Field-Effect Transistors (MOSFETs)

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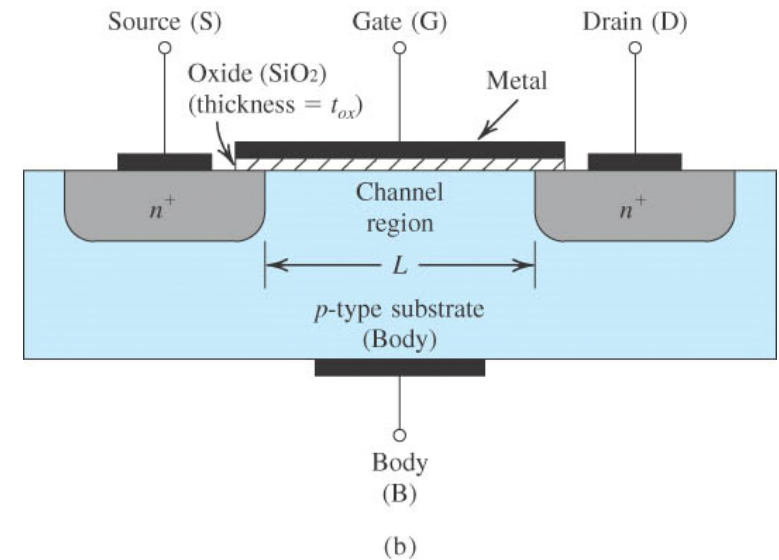
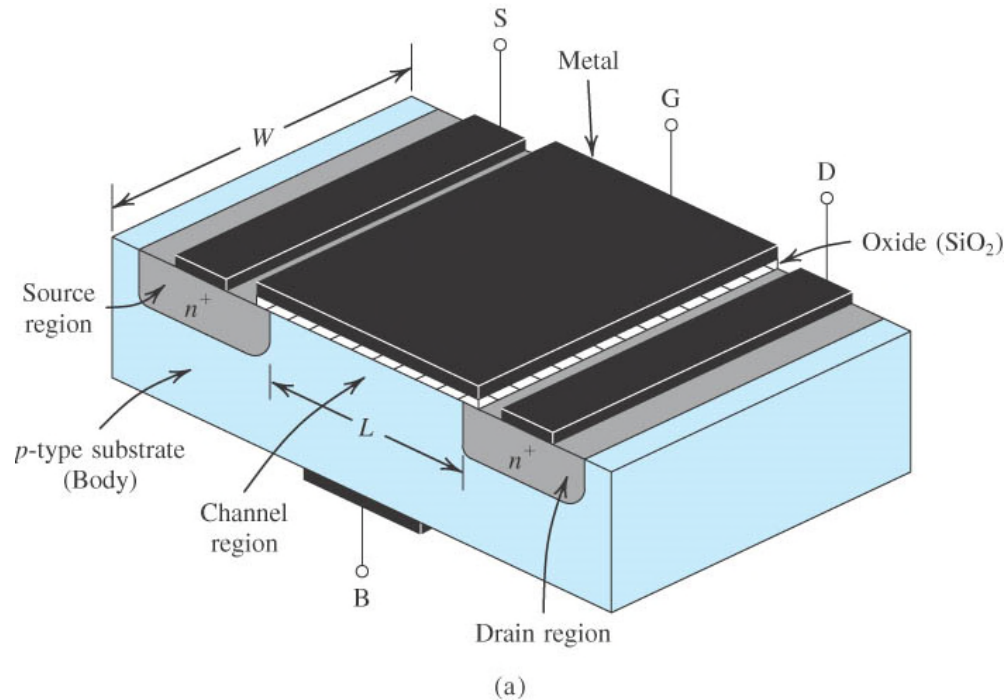


Figure 4.1 Physical structure of the enhancement-type NMOS transistor: **(a)** perspective view; **(b)** cross-section. Typically $L = 0.1$ to $3\ \mu\text{m}$, $W = 0.2$ to $100\ \mu\text{m}$, and the thickness of the oxide layer (t_{ox}) is in the range of 2 to 50 nm.

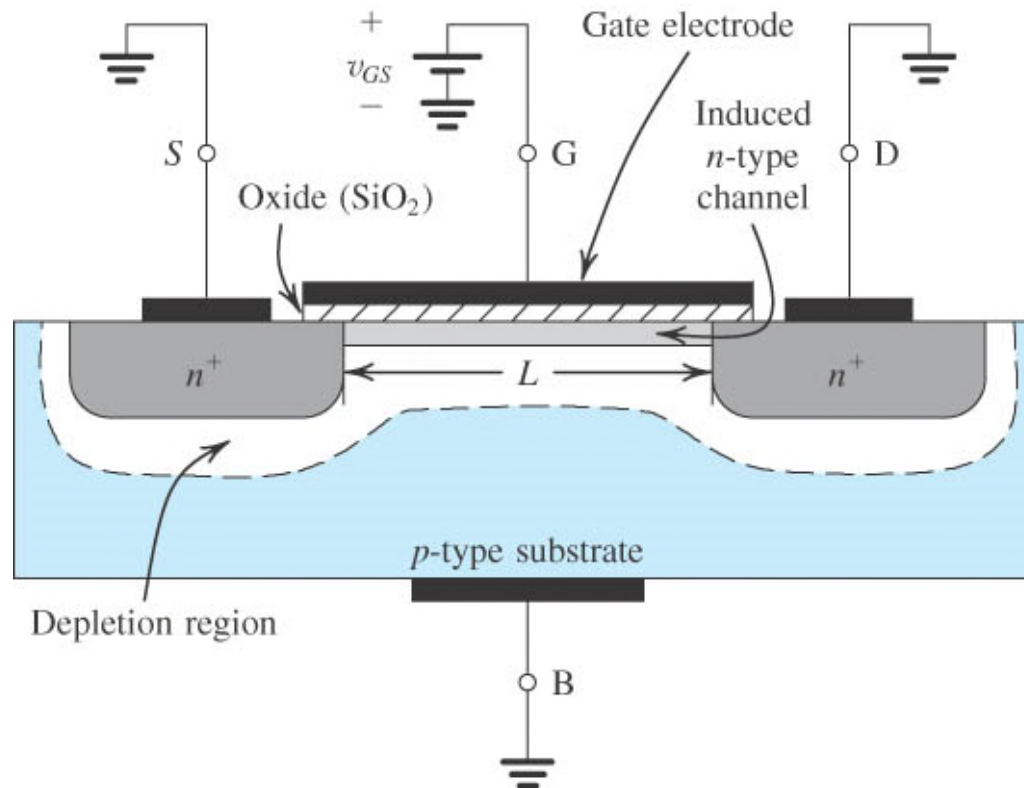


Figure 4.2 The enhancement-type NMOS transistor with a positive voltage applied to the gate. An n channel is induced at the top of the substrate beneath the gate.

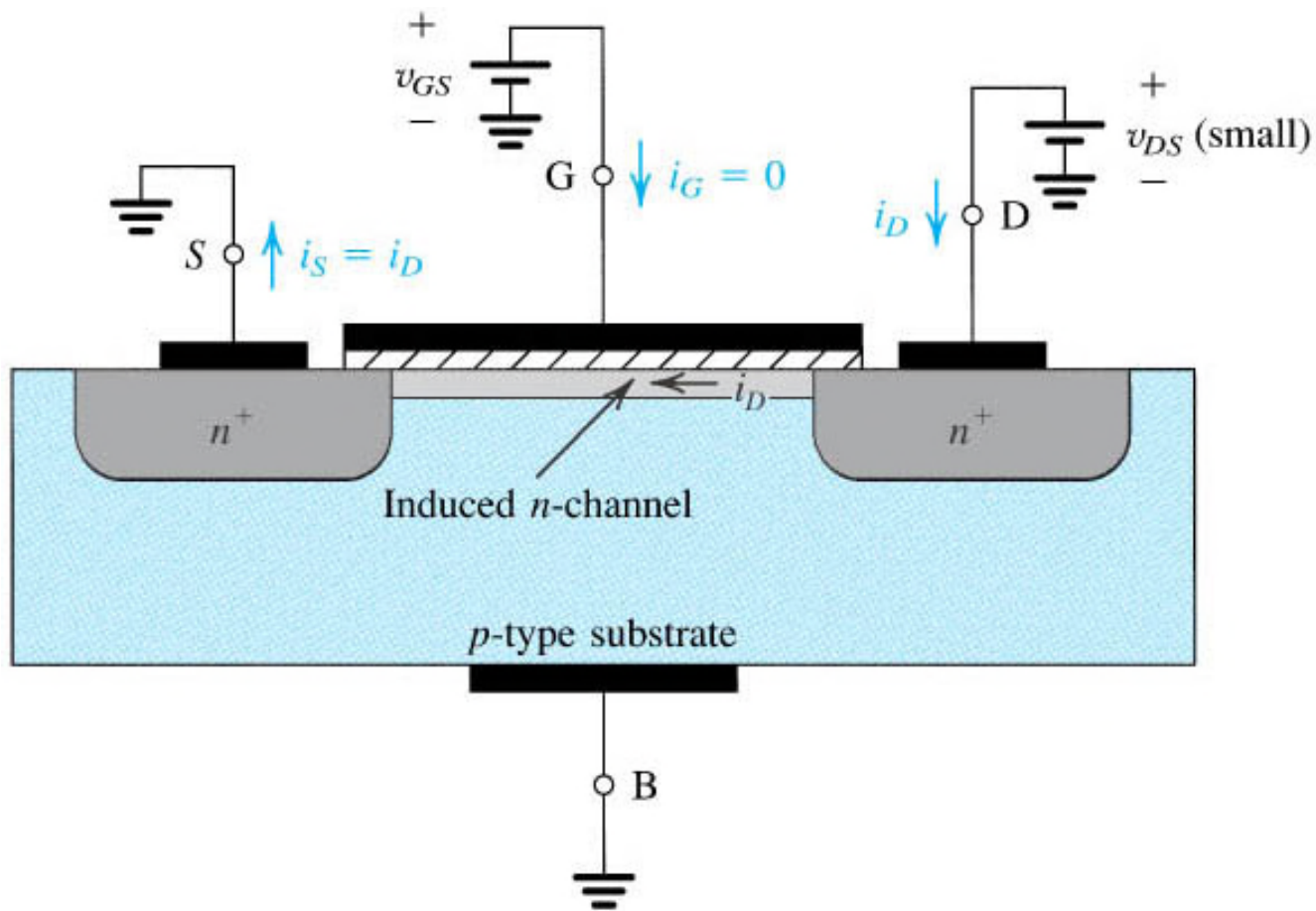


Figure 4.3 An NMOS transistor with $v_{GS} > V_t$ and with a small v_{DS} applied. The device acts as a resistance whose value is determined by v_{GS} . Specifically, the channel conductance is proportional to $v_{GS} - V_t$ and thus i_D is proportional to $(v_{GS} - V_t) v_{DS}$. Note that the depletion region is not shown (for simplicity).

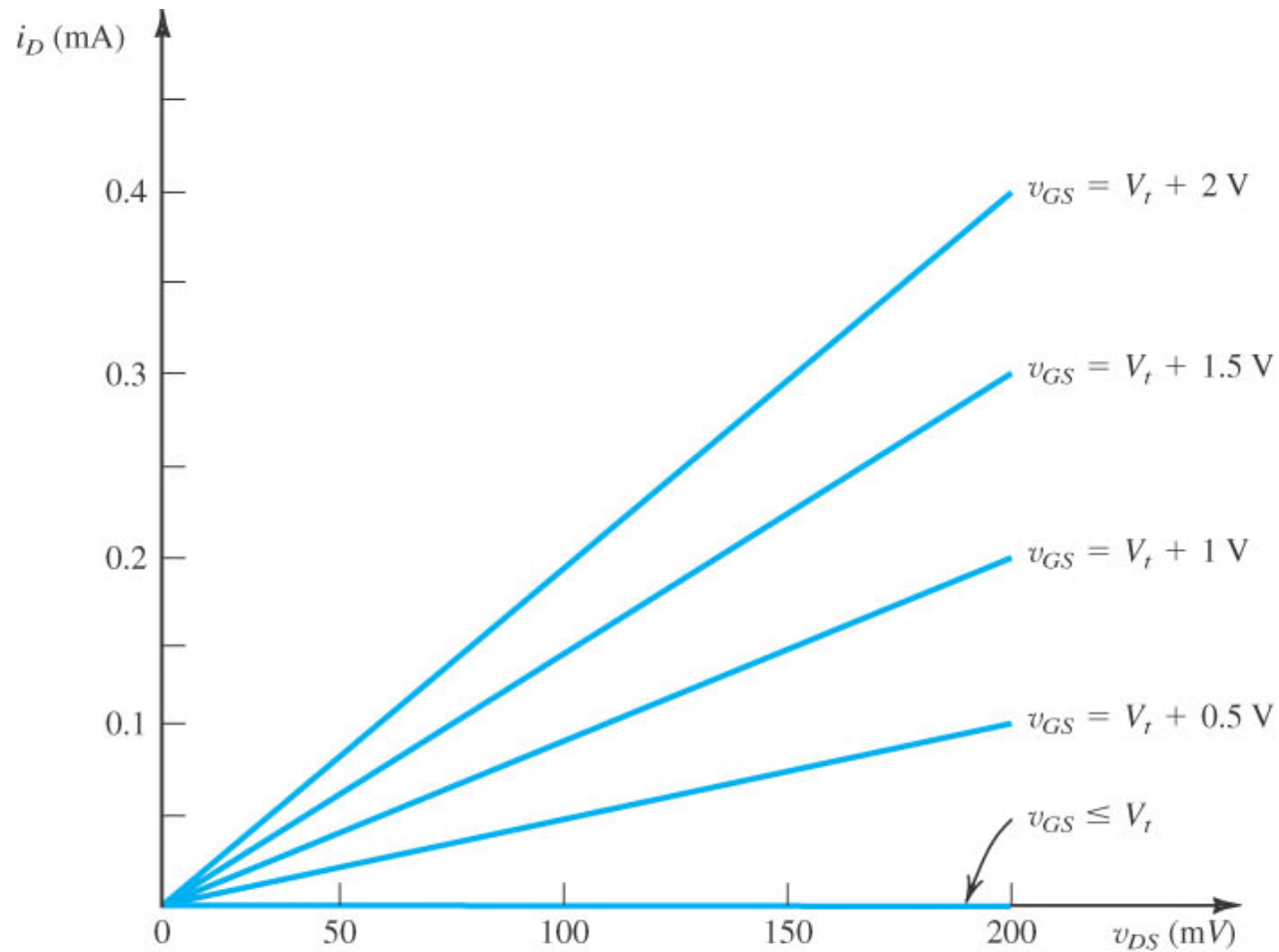


Figure 4.4 The i_D - v_{DS} characteristics of the MOSFET in Fig. 4.3 when the voltage applied between drain and source, v_{DS} , is kept small. The device operates as a linear resistor whose value is controlled by v_{GS} .

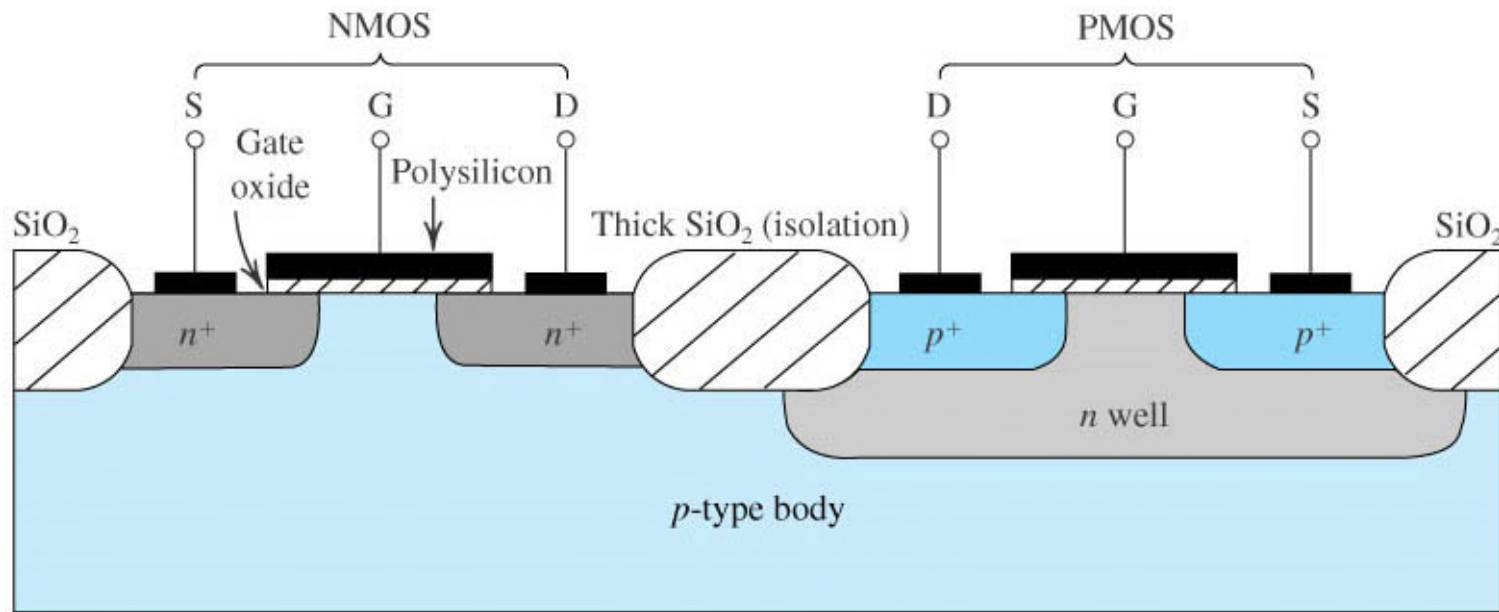


Figure 4.9 Cross-section of a CMOS integrated circuit. Note that the PMOS transistor is formed in a separate n -type region, known as an n well. Another arrangement is also possible in which an n -type body is used and the n device is formed in a p well. Not shown are the connections made to the p -type body and to the n well; the latter functions as the body terminal for the p -channel device.