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Abstract

Pulse-power burn-out test results on SOS resistors, high voltage diodes, and thermally grown gate oxides are described. For SOS diffused resistors, the failure power per unit area ranged from 4×10^6 to 3.7×10^5 watts/cm² for pulse widths of 100 nanoseconds to 10 microseconds. The failure mechanism is heat-induced resistivity variation resulting in formation of low resistivity hot spots or filaments. High voltage diode and resistor combinations extended the failure voltages to 325 volts for 100 nanosecond pulses.

These protection networks were evaluated for use as on-chip protection of CMOS/SOS IC gate oxides. For these gate oxides, the dielectric strength of ~ 800 Å thick silicon dioxide on SOS was $\sim 7 \times 10^6$ volts/cm for 100 nanosecond pulses.

Introduction

Dielectric breakdown of the gate insulator and subsequent catastrophic failure prove to be a major yield and reliability factor in Metal-Oxide-Semiconductor (MOS) devices and integrated circuits. Because of the high impedance ($10^{15} \Omega$) of the gate insulator, and the low leakage characteristics of the thermally grown silicon dioxide, extraneous high voltages can cause destructive breakdown of the dielectric. Unprotected, the breakdown of thermally grown silicon-dioxide gates (of about 1000 Å thickness) occurs at an electric field of $8 - 10 \times 10^6$ volt/cm--i.e., when voltages in excess of 80 - 100 volts are applied to the gate oxide.^{1,2} Local defects such as stacking faults, lattice defects (weak spots), etc., further reduce the dielectric strength of the gate oxide; hence, failures have been observed for fields of 2×10^6 volt/cm. This breakdown characteristic determines the voltage which can be safely applied to the gate of a CMOS device.

Large electrostatic charges may be developed whenever two different materials come into frictional contact and are then separated. Previous studies indicate that personnel can accumulate considerable electrostatic charge while working in laboratory type environments.³ Appendix I describes the origin of the electrostatic charge and indicates that electrostatic voltages as high as several kilovolts can be developed by a person walking across a floor or working at a bench. Devices sliding around in nonconductive handling containers or across bench tops can also develop a large static charge. These high voltages are sufficient to cause degradation in CMOS device parameters or to result in catastrophic breakdown of the gate insulators.

To protect the gate of bulk MOS devices from overvoltages, resulting from static charges or high impedance extraneous sources, a p-n junction type device is often placed in parallel with the gate. The purpose of all MOS protection schemes is to prevent higher-than-normal voltages from reaching the gate of

the MOS device. An ideal protection device should respond to very fast and very slow risetime pulses and effectively limit the gate voltage (clamp to ground) before damage to the gate can occur. The protective device should not degrade normal operation of the MOS device and should be compatible with conventional processing parameters and design constraints.

State-of-the-Art

Differences in fabrication process, design rules, and LSI circuit requirements have resulted in a variety of gate protection networks for use with CMOS LSI circuits. The basic requirement is to limit the voltage appearing at the gate terminals of the CMOS devices to acceptable levels without interfering with normal device operation. The p-n junction diodes, zener diodes, transistors and sparkgaps are among the more common gate protection elements. Figure 1 shows some of the variations of presently used gate protection networks for the CMOS LSI circuits. In Figure 1(a), high-voltage diodes are used to protect the gate oxide. The terminology "high-voltage diode" is used to distinguish these diodes from low breakdown zener diodes. A number of variations exist in such structures due to impurity carrier concentration and device design such as $n^+ - n - p^+$, $n^+ - p - p^+$, $n^+ - n - p - p^+$ structures with and without island edges and gate control of the lightly doped region.

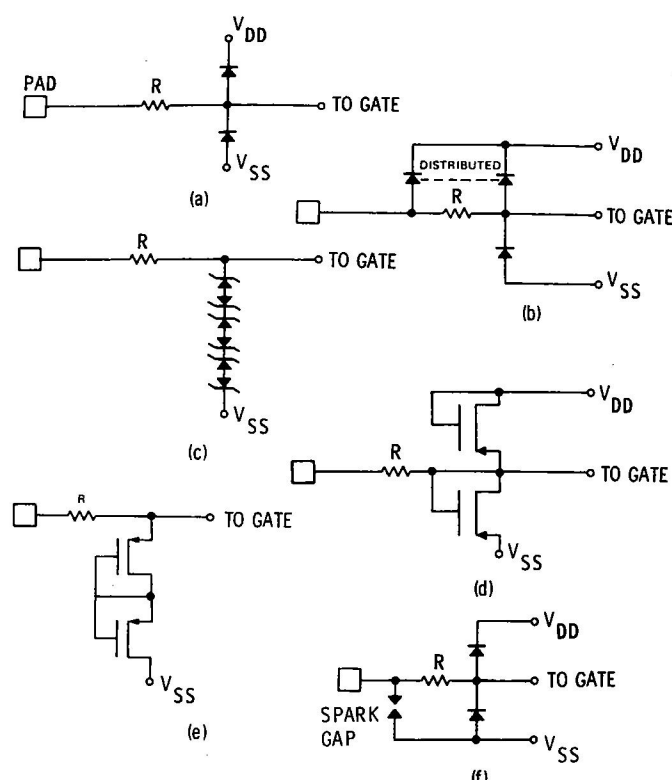


Figure 1

Gate Protection Networks Employing (a) Diodes, (b) Distributed Diodes, (c) Zener Diodes, (d) Transistors, (e) Two Transistors Forming a Bilateral Device, (f) Spark Gap and Diodes

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In Figure 1(b), a distributed diode-resistor combination is used. Figure 1(c) shows three pairs of zener diodes protecting the gate. For this bilateral structure, one stack is sufficient to provide protection against either polarity of extraneous voltage. Although three pairs of zener diodes are shown, any number of pairs, depending on logic level requirements of the CMOS circuit, can be utilized. In Figure 1(d), two p-channel transistors are used to provide the gate protection, and in Figure 1(e), a bilateral combination of p-channel transistors is illustrated. In addition to the solid-state structures, spark gaps⁴ have also been used as shown in Figure 1(f) to provide protection against high voltages.

Special SOS Considerations

LSI circuits fabricated with CMOS technology on silicon-on-sapphire have some special attributes which impact device design as well as the fabrication process employed. These effects can be described as small geometry effects, the island edge effect, the back-channel effect, and the kink effect. The inherent advantage of employing a thin epitaxial silicon layer results in the formation of extremely small-area dielectrically isolated p-n junctions. This feature makes CMOS/SOS devices very attractive for stringent radiation environment applications due to the small collection volumes for the radiation-induced photocurrent.⁵ This advantage must be balanced against the requirement for achieving low p-n junction current densities for gate protection applications (increased junction areas are required to reduce heating effects).

Island edges exist because transistors, resistors and diodes are fabricated in etch-defined silicon island regions to provide dielectric isolation. With epitaxially grown (100) silicon on (1102) sapphire, anisotropic etches expose the (111) silicon surface at the island edges, as shown in Figure 2(a). Thermal oxidation of (111) surfaces result in SiO₂ thickness differences at island edges, as illustrated in Figure 2(a).⁶ Furthermore, the interface state density at Si-SiO₂ interfaces is known to be a function of crystal orientation and is higher for (111) silicon compared to (100) silicon.⁷ Under bias-temperature

stress or in an ionizing radiation environment, these island edges may trap charges or indicate mobile ion-induced instability.⁸ The charges result in formation of a conductive path along island edges which may lower the reverse breakdown voltage and increase the leakage current of a junction. With special device design (e.g., enclosed structures containing p-n junctions which are not exposed to island-edge surfaces) and control of the fabrication procedure, undesirable island-edge effects can be significantly reduced.

The back-channel effect is related to the back-interface, i.e., the silicon-sapphire interface. Positive charge trapping in sapphire near the interface induces an n-type channel in silicon, as shown in Figure 2(b). For an n-channel enhancement mode transistor, with a p-type silicon base region, such an inversion channel forms a current-conduction path between the source and the drain.^{9,10} One of the methods to prevent formation of back-channels is to increase the acceptor-impurity carrier concentration near the silicon-sapphire interface. By employing boron ion-implantation and optimizing the fabrication process to control the redistribution of implanted species, adequate control of the back-channel leakage current has been achieved.⁹ For the p-channel transistors (n-type base region), this effect results in accumulation of the silicon near the Si-sapphire interface and, consequently, no increase in the leakage current is observed.

The *kink* effect arises due to the base region biasing in a transistor. The carriers generated due to impact ionization near the drain region flow through the body and develop a body voltage which in turn increases the saturation current of the transistor, thus exhibiting a *kink* characteristic.¹¹ By connecting the base region to the source through a low resistivity path, this effect can be significantly reduced. In either grounded-base or floating-base condition, the effect of the *kink* mechanism on transistor parameters is to modify the apparent threshold voltage and reduce the saturation resistance. If transistors are used for gate protection purposes, this effect must be taken into account.

Radiation-Hard CMOS/SOS Fabrication Procedure

A radiation hardened self-aligned thick-oxide metal-gate fabrication procedure¹⁰ was used for the fabrication of the gate protection networks shown in Figure 1. The essential steps of this process are shown in Figure 3. Although the process shown is for the fabrication of enhancement mode transistors, appropriate masking steps result in the formation of diodes, resistors and depletion mode devices. Fabrication begins with a boron implant to form a p-type silicon film in selected areas, as shown in Figure 3(a), and the etching of the silicon to form discrete islands. Silicon nitride is then deposited and etched, Figure 3(b), to form a silicon nitride mask over channel areas. This silicon nitride layer serves as a diffusion mask to grow a thick oxide (~4000 Å) over all exposed silicon. The transistor structures at this stage of the process are as shown in Figure 3(c). The silicon nitride layer is then removed by etching, and a radiation resistant gate oxide is regrown over the channel areas. Contact openings are then etched and aluminum metal is deposited and defined. The completed device structure is as shown in Figure 3(d). In the completed structure, the thick oxide covers all but the active channel areas. The gate oxide may be grown by either a dry or a wet process. All results reported here are for a 850 ±50 Å thermal gate oxide grown in steam. The gate

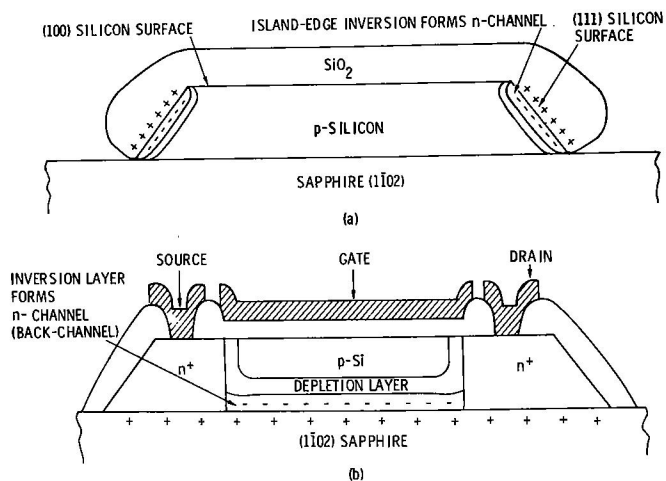


Figure 2

Unique SOS Considerations (a) The Island Edge Effect; Formation of n-Channel on Silicon Island Edges Due to Positive Charge Trapping in the SiO₂ Near the Island Edges, (b) The Back-Channel Effects; Formation of n-Channel Near Silicon-Sapphire Interface Due to Positive Charge Trapping in Sapphire

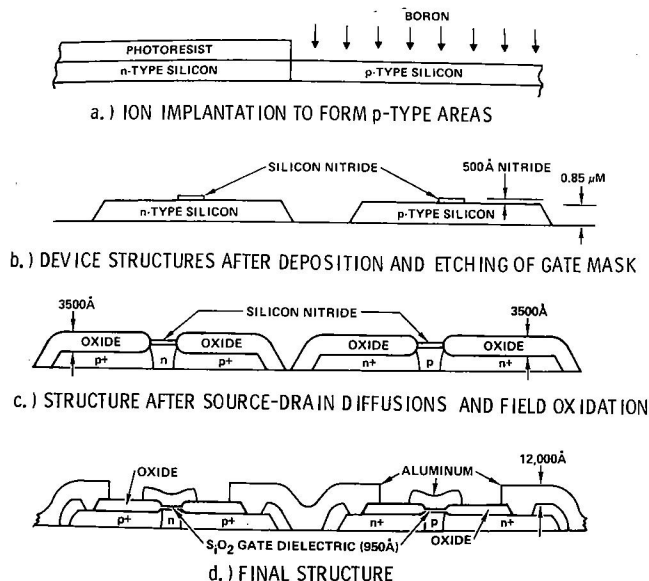


Figure 3

Basic Self-Aligned Nitride-Masked CMOS/SOS Process (Reference 10)

metal is aluminum, evaporated by RF heating to avoid electron-beam damage.

Since radiation induced n-channel back leakage is of concern, the initial boron implant and subsequent oxidation steps are controlled to provide a relatively heavy doping at the Si-sapphire interface. This deep implant procedure has been shown⁹ to minimize, but not completely eliminate, the back leakage. Exact choice of implant energy and dose are important, since too deep an implant will damage the Si-sapphire interface and actually cause a larger back-channel leakage.⁵ The implant energy must also be matched to the thickness of the silicon film. Results reported in this paper are for a 0.75 μm nominal film thickness and a 200 keV implant energy.

Pulse Power Burn-Out Test Procedure

SOS gate protection network electrical over-stress tests were performed by applying a constant voltage pulse of fixed width to the network. Oscilloscopes were used to observe the device parameters and monitor transient current and voltage. The test circuit configuration is shown in Figure 4. A Velonex Model 350 Pulse Generator with appropriate plug-in units was used to provide either a negative or positive pulse as the input to the device under test. The pulse rise and fall times were 25 nanoseconds, and the pulse width was varied from 100 nanoseconds to 10 microseconds. The voltage input was monitored using a low-capacitance voltage probe with the waveform displayed on a storage scope for observation and recording purposes. The current through the device was monitored by a Tektronix CT-2 current probe, and a storage scope was used to display the current waveform.

For a fixed pulse-width, the pulse amplitude was increased, increasing from low values of input voltage until a failure occurred. The experiments were performed at 100 nanoseconds, 1 microsecond and 10 microseconds pulse width. The test devices were packaged in a TO-5 header or 16-pin DIP packages and were examined before and after each pulsed stress. All

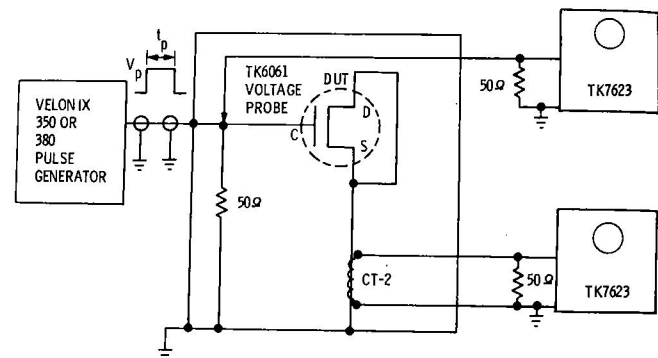


Figure 4

Pulse-Power Burnout Test Conditions for CMOS/SOS Gate Protection Networks Under Pulsed Voltages at 0.1, 1, and 10 Microseconds. Storage scopes are used to record pulse wave shape and device parameter changes.

experiments in this study were conducted at room temperature (23°C).

Results and Discussion

Pulse-power burn-out tests were conducted to characterize transistors, gate oxide SOS resistors, high-voltage diodes, diode-resistor combinations and zener diodes. The drain and source terminals of transistors were grounded, and pulsed voltages of increasing amplitude were applied to ~800 Å thick gate oxide of both n-channel and p-channel transistors. At 0.1, 1 and 10 microsecond pulse widths, the average catastrophic failure voltage was 67, 63 and 55 volts, respectively. No significant difference in gate dielectric strength of n-channel and p-channel transistors was observed. The average value of breakdown voltage was 60 volts, and the dielectric strength of SOS gate oxides of ~800 Å thickness was 7.6×10^6 volts/cm. This result for SOS devices compares favorably with bulk MOS devices and indicates that no adverse effects of SOS silicon material quality (more defect sites), island edges or ion-implantation damage were observed under pulsed test conditions.

The transient pulse characteristics of both n^+ and p^+ SOS resistors (area = 1.75×10^{-5} cm²) indicated changes in resistivity with increasing pulse amplitude. Thermal effects leading to filamentation and hot spot formation were observed. Catastrophic failures occurred where decreased resistance allowed large current transients to melt and vaporize silicon. For 0.1, 1 and 10 microsecond pulses, the catastrophic failures occurred in the range of 280 - 390 volts, 150 - 190 volts and 90 - 115 volts, respectively. The failure power per unit area was evaluated to be 4.4×10^6 , 1.1×10^6 and 3.7×10^5 watts/cm². The data indicate that the type of dopant (n^+ or p^+), carrier concentration (10^{19} - 10^{20} atoms/cm³) and silox overcoat variation did not impact the failure thresholds.

Figure 5 shows the experimental data and theoretical relationship of failure power per unit area to the pulse width according to the Wunsch-Bell model.¹² The Wunsch-Bell model for determining the threshold failure level of semiconductor devices due to pulsed voltage relates the power dissipated per unit area to the thermal characteristics of the semiconductor to determine the local temperature rise and threshold power density for failure. Failure is assumed to occur when the temperature reaches the melting point

of the semiconductor material. Linear heat flow theory is used to derive the following equation:

$$P/A = \sqrt{\pi k \rho C_p} [T_m - T_i] t^{-1/2} \quad (1)$$

where P = power in watts
 A = junction area in cm^2
 k = thermal conductivity
 t = time
 ρ = density
 C_p = specific heat
 T_m = failure temperature
 T_i = initial temperature

Although approximations such as constant thermal conductivity, specific heat and density are used in the Wunsch-Bell model, the failure data indicate the relationship to be applicable to SOS resistors. Based on the experimental data, a failure threshold for short pulses can be predicted. For a 10 nanosecond pulse, from Figure 5, the failure power per unit area is 1.15×10^7 watts/ cm^2 . For the area of the resistors used in this study ($1.78 \times 10^{-5} \text{ cm}^2$), this value corresponds to a failure power of 205 watts. For a 450 ohm n^+ resistor, the predicted failure level is 303 volts with a failure current of 675 milliamperes. For an 1800 ohm p^+ resistor, the predicted failure voltage and current are 607 volts and 338 milliamperes, respectively. If the current through the resistor can be limited, additional high voltages can be tolerated before resistors fail due to heating effects.

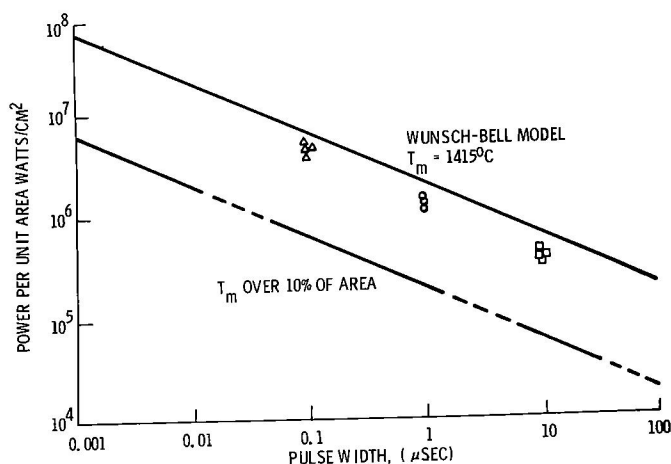


Figure 5

Failure Power per Unit Area Versus Pulse Width. Theoretical calculations for melt-temperature heating of 100% and 10% of the resistor area are shown.

Additional power-handling capability for the resistors can be also achieved by increasing the area of the resistor. For example, if the resistor area is increased from $1.78 \times 10^{-5} \text{ cm}^2$ to 7.6×10^{-5} , (double the width and length), an increase in tolerable power by a factor of 4 (proportional to area) can be achieved.

A $p^+ - p - n^+$ gate-controlled diode enclosed structure was characterized and stressed to failure in both reverse-bias and forward-bias conditions. Series resistors were used to form the gate protection network. Failure data at 0.1, 1 and 10 microseconds pulse width are given in Table 1. Input voltage, V_{in} , and the clamping voltage across the diode, V_D , are shown along with total power dissipated in the structure.

TABLE 1
 SOS High Voltage Diode --
 Resistor Pulse Power Burnout Data

Diode Bias Condition	Series Resistor Type	Ohms	Pulse Width (μsec)	Failure Data				
				V_{in} (volts)	V_D (volts)	I (mA)	Power Diode (Watt)	Power Total (Watt)
Forward	n^+ SOS	500	0.1	325	32	240	7.68	78.0
	n^+ SOS	520	1.0	150	23	120	2.76	18.0
	n^+ SOS	515	10.0	90	15	65	0.98	5.85
	p^+ SOS	1.87K	0.1	300	10	140	1.4	42.0
	p^+ SOS	1.79K	1.0	75	9	40	0.36	3.0
	p^+ SOS	1.70K	10.0	100	7	46	0.32	4.6
Reverse	n^+ SOS	475	0.1	100	50	115	5.75	11.5
	n^+ SOS	497	1.0	100	60	100	5.0	10.0
	n^+ SOS	454	10.0	70	50	60	3.0	4.2
	p^+ SOS	1.8K	0.1	200	40	120	4.8	24.0
	p^+ SOS	1.8K	1.0	180	40	80	3.2	14.4
	p^+ SOS	1.8K	10.0	110	40	45	1.8	4.95

The ratio of diode resistance in the forward-bias condition to the series current limiting resistor determines the voltage across the diode. For effective gate protection, the resistance of the diode must be much smaller than the series current-limiting resistance. Figure 6 shows the clamping voltage, V_D , as a function of applied pulse voltage, V_{in} . A saturation effect is observed which may be related to thermally induced resistivity variations. The analysis of transient impedance and time-dependent thermal/electrical mechanisms of such gate protection networks is difficult due to nonuniform heating effects which occur simultaneously in the SOS diode and the SOS resistor. Data in Figure 6 indicate that a 450 ohm resistor in series with an enclosed-structure (edgeless) gate protection diode is adequate to limit voltages appearing across the diode ($V_D < 35$ volts) for input voltages up to a maximum of V_{in} 325 volts for 0.1 microsecond pulses. The clamping voltage, V_D , is well below the gate dielectric breakdown voltage of ~60 volts. With higher value resistors, the limitation seems to be the total silicon area, as expected. For electrostatic discharge pulses which typically have narrower pulse widths (~20 nanoseconds), higher input voltages can be applied to the network without causing damage to the protection network or to a transistor gate connected in parallel with the diode.

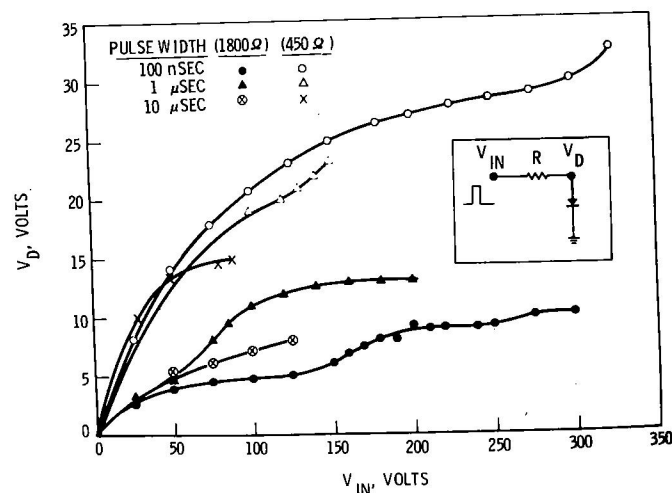


Figure 6

Diode Clamping Voltage V_D as a Function of Pulsed Input Voltage V_{in} for an Edgeless (Enclosed Structure) SOS Diode-Resistor Gate Protection Network

The stability and the reliability of the gate protection elements including high-voltage diodes, zener diodes and transistors were examined under stringent high temperature bias tests. A 260°C, 16-hour test under reverse bias and forward conducting mode of each device was conducted. No appreciable change in the leakage currents (<10 nA) or the reverse breakdown and threshold voltages (<0.2 V) was observed, indicating no ion migration or long-term instability effect. Similarly, Co⁶⁰ gamma irradiation up to a total dose of 1×10^6 rads(Si) did not change any device parameter significantly to cause failure. This result is primarily due to the radiation hardened fabrication process used for this work.

Conclusions

Electrostatic discharge, under normal laboratory environmental conditions can produce voltages in excess of hundreds of volts, which, if applied to gate insulators of CMOS/SOS circuits, results in catastrophic failure. The failure voltage of thermally grown silicon dioxide (~ 800 Å thick) under 100 nanosecond pulse voltage conditions was determined to be between 60 and 70 volts--corresponding to a dielectric strength of $\sim 7 \times 10^6$ volt/cm. The experimental results indicated no major problems due to silicon-on-sapphire starting material impurities, island edge effects, or damage produced by ion-implantation--with respect to the dielectric strength of the thermally grown gate oxide.

Silicon-on-sapphire resistors, characterized under pulsed voltage conditions, indicate a failure power per unit area of 4×10^6 to 3.7×10^5 watts/cm² for pulse widths of 100 nanoseconds to 10 microseconds. The Wunsch and Bell theoretical model for predicting the failure threshold of semiconductor devices was shown to be applicable to SOS resistors. The failures appear to be due to thermal effects which result in resistivity variations and formation of "hot spots" or low-resistivity filaments.

High-voltage diode and resistor combinations were found to extend the failure voltage from ~ 60 volts (gate dielectric breakdown) to ~ 325 volts for 100 nanosecond pulses.

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Appendix I

Electrostatic Discharge

When two dissimilar materials are in contact, the electrons at the interface are attracted to the material with the greater affinity for electrons. Separation of the two materials results in negative static charging of the material which acquired electrons. The magnitude of the static charge is proportional to the number of excess electrons on the surface. It is not necessary for the materials to rub against each other to produce static charge, mere contact and subsequent separation is sufficient; however, rubbing of two dissimilar materials also results in static charging. A list of the materials which charge positive or negative according to their relative position in the Triboelectric series is given by Walker.¹³ Many of the materials, e.g., glass, aluminum, paper, nickel, copper, silver, brass,

stainless steel, rubber, polystyrene foam, and teflon are commonly used in semiconductor hybrid and integrated circuit fabrication and packaging, thus increasing the susceptibility of ICs to electrostatic charge.

Several other factors influence the magnitude of static charge--including the intimacy of contact, the rate of separation of the materials and the environmental conditions, such as relative humidity. Increasing intimacy tends to maximize the interaction of surface charge yielding higher magnitude static charges. Similarly, increases in the rate of separation decreases the leakage of electrons back to donor material, thereby effectively increasing the static charge. High relative-humidity does not affect the magnitude of the generated charge, but increases surface leakage, thereby depleting the accumulated charge.

Electrostatic voltages measured in relative ambient humidity of 15% to 36% under different conditions of laboratory operations ranged from 500 volts to 39,000 volts.^{3,14} In a different survey by Linholm,¹⁵ 88% of the laboratory workers examined had charge accumulation up to 1500 volts.

Two sources of static electricity have been identified as the primary cause of failures of integrated circuits. First, the charge stored on an operator's body is discharged through the device to ground and, second, the charge on the device itself is discharged to ground through one of the terminals. The electrostatic discharge from a person's body results in a rapidly decaying current pulse with a peak value of current dependent on the initial voltage and the effective resistances. The rate of pulse decay depends on the resistances and the capacitance of the person's body. Various researchers have estimated the equivalent body capacitance and body resistance. Although the numbers vary, a capacitance of 100 pF in series with a resistance of 1.5 kΩ seem to be the average.^{2,3,16-18} For simulation of the electrostatic discharges, a 50-ohm system is generally adopted. It simulates adequately the source resistance and the finite amount of charge available. Other overvoltage sources are similar to those due to human handling, because they are of relatively high impedance or, again, the available charge is finite.

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