

A Shallow Trench Isolation Study for 0.25/0.18 μ m CMOS Technologies and Beyond

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Abstract— A manufacturable shallow trench isolation (STI) technology using high density plasma (HDP) CVD oxide as trench filling material is reported for the first time, and compared to using sub-atmospheric CVD (SACVD) oxide as filling material. HDP filled STI has excellent immunity to double-hump, better gate oxide integrity and inverse narrow width effect, due to its lower deglaze rate and thus better corner protection compared to the SACVD case. The ΔV_t (between $W=10$ and $0.18\mu\text{m}$) are 150mV (NMOS) and 60mV (PMOS) for the HDP case, and the transistor width reduction is $\leq 0.03\mu\text{m}$ for both cases. Trench wall passivation and a low sputtering component during deposition are necessary for HDP to achieve low diode edge leakage. $0.28\mu\text{m}$ intra-well isolation (or $0.46\mu\text{m}$ min. pitch), $0.6\mu\text{m}$ n^+ -to- p^+ isolation, latch-up holding voltage of 2V at $0.5\mu\text{m}$ n^+ -to- p^+ spacing, together with outstanding CMOS transistor and inverter performance, have been achieved. These results are either comparable to or better than the best results reported to date. It is concluded that HDP trench filling oxide is a viable approach, while SACVD oxide is marginally acceptable, for the STI of 0.25/0.18 μm CMOS.

Introduction — As high performance CMOS technology is scaled down to the current 0.35-0.25 μm generation, shallow trench isolation (STI) becomes indispensable due to its advantages compared to the conventional LOCOS-type isolation, viz. smaller channel-width encroachment, better isolation/latch-up characteristics, planar topography, and smaller junction edge capacitance. Although STI is used in production [1-3], the processing trade-offs and device characteristics are mostly not reported. Recently Perera et. al. [4] reported an STI processing with excellent latch-up and double-hump free characteristics using an ozonated APCVD TEOS oxide. In this paper we will report, for the first time, the process and device characteristics of using inductively coupled HDP CVD oxide (as opposed to biased ECR CVD oxide [5]), and compare them with using SACVD oxide, an O_3 -TEOS CVD process, for 0.25/0.18 μm CMOS applications.

STI Process — Devices are fabricated on (100) oriented p-type epi wafers with epi resistivity of 5-15 $\Omega\text{-cm}$ and epi thickness of 3.5 or $6\mu\text{m}$. The STI process sequence is similar to ref.[2,4]: after standard diffused twin-well formation, 100-150 \AA pad oxide and 1500-2000 \AA nitride were formed and defined as the active area, and followed by a $\sim 0.5\mu\text{m}$ shallow trench etching. 200 \AA thermal oxide (900 $^\circ\text{C}$ with 5% HCl) was grown on the trench surface to round the trench corner. 9000 \AA HDP or SACVD oxide was then deposited, densified (850 $^\circ\text{C}$ for 30min for SACVD oxide *only*) and planarized by CMP down to the nitride layer which was subsequently removed by standard hot phosphoric acid. V_t adjust implants and optional channel stop (CS) implants (B/150keV for NMOS and P/320keV for PMOS, $4 \times 10^{12}\text{cm}^{-2}$) were done, and followed by pad oxide removal and gate oxide (60 \AA in the present study) growth. The remaining processes are the same as standard 0.25/0.18 μm CMOS [6]. Fig.1a & b show typical TEM pictures of HDP and SACVD filled trenches with the same CMP polish. Note that due to the lower deglaze rate of HDP oxide (only 10% higher than thermal oxide), its surface is higher than that of SACVD, which makes it more immune to trench corner related defects [2,4] as shown below.

Results and Discussions — Fig.2a&b show some CMOS I-V characteristics for the HDP and SACVD cases ($W/L=10/.8$). Fig.3 compares the histograms of the average NMOS sub-threshold slope for the I-V data shown in Fig.2a&b. The SACVD case has many incidences of high sub- V_t slope (due

to double-hump) at $V_{\text{sub}} = -2\text{V}$, while much less at $V_{\text{sub}} = 0\text{V}$, indicating marginal immunity to double-hump at normal operation ($V_{\text{sub}} = 0\text{V}$). In contrast, HDP is indeed free from double-hump at both V_{sub} .

Fig.4 shows the histogram of gate oxide charge-to-breakdown (Q_{bd}) for the HDP or SACVD filled trenches. The STI-edge data is to reveal the edge defects while the S/D-edge data serves as reference. For SACVD, the Q_{bd} distribution of STI-edge capacitor has a tail, meaning the defect density is higher at the STI edge, which is consistent with the double-hump data shown in Fig.2&3.

Fig.5 and Fig.6 show the V_t vs. W for the HDP and SACVD filled trenches. The HDP case has a much smaller ΔV_t (about 150mV for NMOS and 60mV for PMOS) between $W=10$ and $0.18\mu\text{m}$ and much tighter $\pm 3\sigma$ variation at any given W compared to the SACVD case, which is again quite consistent with the above double-hump and GOI data. Fig.7 shows some typical CMOS I-V characteristics of $W/L=10/.18$ and $.18/.3$ transistors. Due to the small ($\leq 0.03\mu\text{m}$) width reduction, the $W=0.18\mu\text{m}$ transistors behave quite normally.

Fig.8 compares distribution of STI-edge n^+ diode leakages for the following cases: (1) HDP deposition/sputtering (D/S) ratios of 2.9 and 3.4, (2) HDP without the 200 \AA trench lining thermal oxide, and (3) SACVD. It is clear that a lower sputtering component (D/S=3.4 vs. 2.9) during HDP deposition and the trench lining thermal oxide are crucial for preventing excessive diode edge leakage. The n^+ bottom-wall leakage and p^+ leakages are less sensitive to these conditions.

Fig.9 and Fig.10 show the intrawell n^+ -to- n^+ and p^+ -to- p^+ trench isolation characteristics for metal-gate and perpendicular poly-gate structures, respectively. The 150keV boron channel stop (CS) implant allow scaling the n^+ -to- n^+ spacing down to $0.28\mu\text{m}$, the patterning limit for the current wafers. p^+ -to- p^+ isolation is good to $0.28\mu\text{m}$ with or without the phosphorus CS implant. Bias-temperature stress (285 $^\circ\text{C}$, +5V for 1hr) of thick trench oxide capacitor does not lower the n^+ isolation V_t for both HDP and SACVD cases, indicating absence of mobile ion contamination. Fig.11 shows the interwell n^+ -to-nwell and p^+ -to-pwell isolation punch-through voltage. With the boron CS implant, an n^+ -to- p^+ spacing of $< 0.6\mu\text{m}$ is achieved, slightly better than the $0.76\text{--}0.7\mu\text{m}$ reported [3,4]. Fig.12 shows the latch-up holding voltage vs. n^+ -to- p^+ spacing with varying epi thicknesses, CS implant, and a LOCOS reference. A latch-up holding voltage of 2V at $0.5\mu\text{m}$ spacing is achieved, satisfying the SRAM requirement of $0.6\mu\text{m}$ for 1.5V/0.18 μm CMOS generation.

Fig.13 shows some typical drive current vs. off-state leakage characteristics for CMOS with HDP filled STI ($\tau_{\text{ox}}(\text{acc.}) = 60\text{\AA}$, $V_d = V_g = 2.5\text{V}$, with gate length ranging from 0.16 to $0.35\mu\text{m}$, and $W=10\mu\text{m}$). Excellent nominal drive currents [6] of 600 and 300 $\mu\text{A}/\mu\text{m}$ for NMOS and PMOS, respectively, are achieved. Fig.14 shows the inverter delay vs. V_{dd} . Despite the enlarged junction area for relaxed contact and metalization processes, a respectably short delay of 25ps/stage at 2.5V is achieved owing to the smaller junction edge capacitance of STI. The isolation, latch-up, and CMOS performance data for the SACVD case are nearly identical to the HDP cases shown above.

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[2] A. Bryant, et al, IEDM Tech. Dig., pp.671, 1994.

[3] M. Bohr, et al, IEDM Tech. Dig., pp.273, 1994

[4] A. H. Perera, et al, IEDM Tech. Dig., pp.679, 1995

[5] T. Gocho, et al, 1991 VLSI Tech. pp.87

[6] M. Rodder et al, IEDM pp.71 (1994), pp.415 (1995).

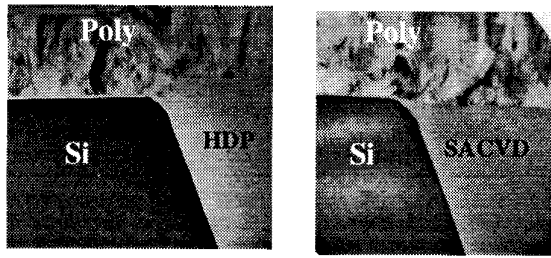


Fig.1a&b TEM cross-sectional view of shallow trench isolation using (a) undensified High Density Plasma (HDP) CVD oxide, and (b) densified ozonated-TEOS sub-atmospheric CVD (SACVD) oxide. Note that the lower HF deglaze rate of HDP oxide makes its surface slightly higher than that of the SACVD case.

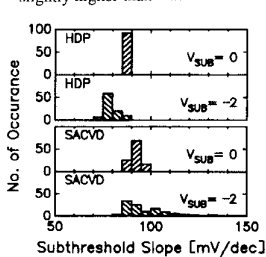


Fig.3 Histograms of average NMOS subthreshold slopes for the IV shown in Fig.2a&b. For the SACVD case, the distribution is wide at $V_{SUB} = -2V$ indicating the double-hump occurs quite frequently.

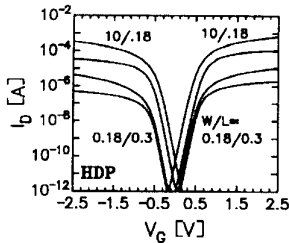


Fig.7 Typical CMOS $I_D - V_G$ characteristics for HDP filled STI ($V_D = 0.1/2.5V$, $V_{SUB} = 0V$). Due to the small width reduction ($<0.03\mu m$), the $W=0.18\mu m$ transistors behave normally.

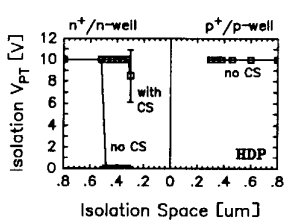


Fig.11 Inter-well isolation punch-through voltage (V_{PT} defined as $10pA/\mu m$) for n+ to nwell and p+ to pwell isolation. A n+ to p+ space of $<0.6\mu m$ is achieved with the 160Kev boron CS implant.

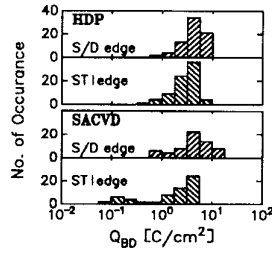


Fig.4 Histograms of NMOS gate oxide charge-to-breakdown (Q_{BD}) at $J_G = -100mA/cm^2$. The S/D-edge capacitor ($1.2E-3 cm^2$) has a minimal ($\sim 100\mu m$) STI edge, while the STI-edge capacitor ($6E-4 cm^2$) has a long ($>6cm$) STI edge.

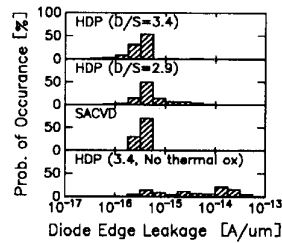


Fig.8 Histograms of n+ diode leakage (STI-edge, 4V reverse bias) for HDP filling with deposition / sputtering (D/S) ratios of 3.4 and 2.9, SACVD, and HDP without trench lining thermal oxide. Higher sputtering (D/S=2.9) or without trench thermal oxide result in higher diode edge leakage.

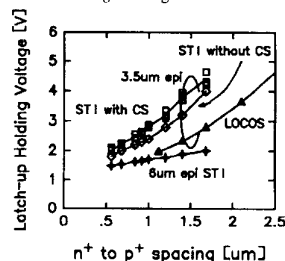


Fig.12 Latch-up holding voltage as a function of n+ to p+ spacing for 3.5um and 6um epi, with or without CS implant, and a LOCOS comparison. With the 3.5um epi and CS implant, the latch-up holding voltage is 2V at 0.5um n+ to p+ spacing, satisfying the 1.5V/0.6um requirements of 0.18um CMOS.

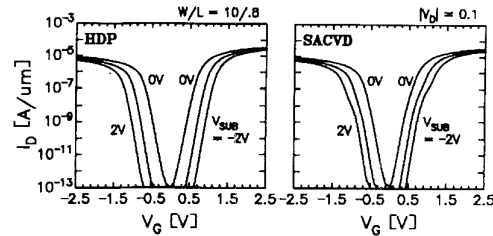


Fig.2a&b CMOS $I_D - V_G$ characteristics for a typical HDP and a bad-case of SACVD filled trench isolation ($W/L=10/8$). The HDP case is free of double-hump, while the SACVD case has pronounced double-hump only with substrate biases.

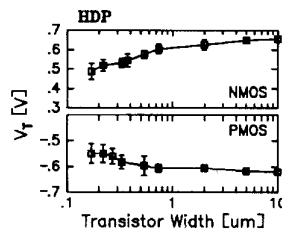


Fig.5 V_T vs. transistor width for HDP filled STI ($L_G = 0.3\mu m$). The V_T difference between $W=0.18\mu m$ and $10\mu m$ devices are about 150mV and 60mV for NMOS and PMOS, respectively.

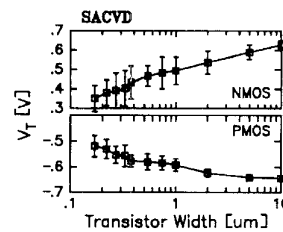


Fig.6 V_T vs. transistor width for SACVD filled STI ($L_G = 0.3\mu m$). The V_T differences (between $W=0.18$ and $10\mu m$) are 260mV and 140mV for NMOS and PMOS, respectively.

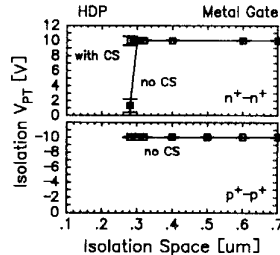


Fig.9 Intra-well isolation punch-through voltage (V_{PT} , the V_D to reach $I_D = 10pA/\mu m$ at $V_G = 2.5V$) for metal-gate n+ to n+ and p+ to p+ isolations. The 150Kev boron channel-stop (CS) implant helps to extend the n+ isolation space to $0.28\mu m$, patterning limit of current wafers.

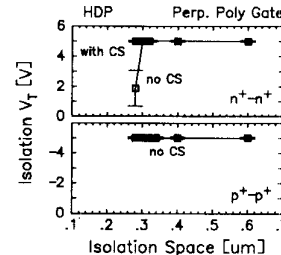


Fig.10 Intra-well isolation threshold voltage (V_T , the V_G to reach $I_D = 10pA/\mu m$ at $V_D = 2.5V$) for perpendicular-poly gate isolation structures. Similar to Fig.9, the 150Kev boron CS implant is important for n+ isolation.

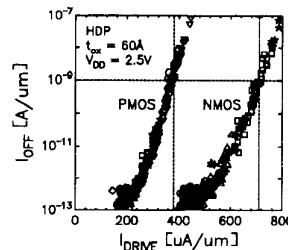


Fig.13 Drive current vs. off-state leakage current for the HDP filled CMOS transistors. The strong (I_{DRIVE} at $I_{OFF} = 1nA/\mu m$) and nominal drive currents are 715/380 and 600/300 $\mu A/\mu m$ (I_{DN}/I_{DP}), respectively.

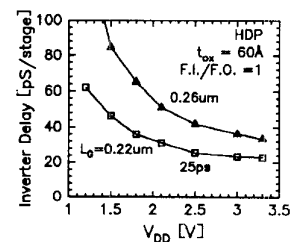


Fig.14 Inverter delay vs. V_{DD} for HDP filled trench isolated CMOS. Despite the relaxed design of contact and metal-1 (thus larger total C_j), the 0.22um chain has a respectably low delay of 25ps at 2.5V due to smaller junction sidewall capacitance ($W_N=W_P=5\mu m$).