

international
**ELECTRON
DEVICES**
meeting

1978

WASHINGTON, D.C.
December 4-5-6

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1978 International Electron Devices Meeting TECHNICAL DIGEST

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SUB-MICRON POLYSILICON GATE CMOS/SOS TECHNOLOGY

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ABSTRACT

A process sequence incorporating the lateral diffusion of Boron into polycrystalline silicon for the fabrication of CMOS/SOS transistors and integrated circuits is described. The resulting polysilicon gate dimensions and channel lengths are typically between 0.2 μm and 2.0 μm . Yield values associated with these narrow polysilicon lines are shown to be equal to present 5 μm yield values. Ring oscillators have been fabricated having 0.5 μm channel lengths which exhibit propagation delays of 200 ps at 5v. In addition, 10 stage dynamic binary counters have also been fabricated having 0.5 μm channel lengths and a maximum input frequency of 600 MHz at 12v and 200 mW was attained.

INTRODUCTION

Short channel MOS transistors have been fabricated using diffused channel processes⁽¹⁾ as well as V-groove approaches.⁽²⁾ Narrow gate MOS transistors, on the other hand, have been fabricated using e-beam direct exposure⁽³⁾ as well as overetching techniques⁽⁴⁾. Another technique for achieving very narrow polysilicon lines was described by Nicholas⁽⁵⁾ et al. and makes use of the non-etchability of heavily boron doped silicon. This technique has the distinct advantage of being a high yield technique and hence permits the fabrication of integrated circuits containing many sub-micron gate devices. This approach also permits the fabrication of symmetric devices as well as complementary devices (CMOS).

FABRICATION

The fabrication sequence is shown in Fig. 1. Using ion-implantation, the starting substrates are doped to various levels depending upon the final gate length. An SiO_2 layer of typically 100-500 Å is grown followed by the deposition of a Si_3N_4 layer of similar thickness. The nitride layer is used to minimize the interaction of the subsequent boron diffusion with the SiO_2 layer. Polysilicon is deposited followed by an SiO_2 deposition and photo-step to define the SiO_2 and polysilicon. The wafers are then exposed to a boron diffusion at 900°C using BN. Only the exposed edges of the polysilicon are doped with boron to a depth which is dependent on the time and temperature. After the boron diffusion, the SiO_2 masking layer is removed and the undoped polysilicon is removed using a KOH-alcohol solution. The Si_3N_4 layer is removed and the sources

and drains are implanted using boron and phosphorus or arsenic to a level of $1-4 \times 10^{15}/\text{cm}^2$. A final SiO_2 layer is deposited over the surface of the wafers, the implants are activated at 900°C for 15 minutes, contacts are opened, and the wafers are metallized.

As can be seen from Fig. 1, it is possible to fabricate either single or multiple gate transistors depending upon the polysilicon mask pattern. Figure 2 shows an SEM photomicrograph of a finished array. Narrow polysilicon lines are shown crossing epi-silicon islands and, in turn, being crossed by aluminum. The continuity yield of narrow polysilicon lines having widths between 0.1 μm and 1.5 μm was measured as a function of length and number of epi-silicon crossunders and the results are given in Fig. 3. These data indicate that there is essentially no yield degradation over this range. In addition, comparison of these results with previous measurements using photolithographic definition techniques⁽⁶⁾ indicates that the continuity yield is only a function of the width of the initial polysilicon pattern (in this case 5.0 μm) not the final polysilicon width.

DEVICE CHARACTERISTICS

Typical D.C. device characteristics for transistors having polygate dimensions of 0.5 μm are shown in Fig. 4. Dual gate, n-channel devices ($L_{SD}=1.0 \mu\text{m}$) generally exhibit initial breakdown at about 10-15 volts while single gate devices show similar effects at about 5-8 volts. P-channel devices are, of course, somewhat better. N-channel device leakage currents for 0.5 μm channel lengths are typically 0.5 nA per micrometer of channel width while p-channel devices have typical leakages of about 0.1 nA per micrometer of channel width.

PERFORMANCE CHARACTERISTICS

Ring oscillators have been fabricated using the narrow gate process and typical results are shown in Fig. 5. Both dual gate devices and single gate devices were fabricated on the same wafer, and stage delay ratios were about 2 to 1. The shortest propagation delays observed to date have been in the 150 to 200 pS range for 0.5 μm gate lengths. Shorter gate length devices have been made but the leakage currents have been substantially higher than the 0.5 μm devices and the propagation values were about the same.

Ten stage dynamic binary counters have also been fabricated with this process. The maximum input frequency for counters having $0.5\text{ }\mu\text{m}$ single gate devices was 600 MHz and the variation with supply voltage is shown in Fig. 6. At 5v the counters operated at about 200 MHz. The dependence of power dissipation with the maximum input frequency is shown in Fig. 7 and it can be seen that the average power dissipation at 200 MHz and 5v is about 8 mW while at 600 MHz and 12v the power dissipation increases to about 200 mW.

- (1) H.J. Sigg, G.D. Vendelin, T.P. Cauge, J. Kocsis, "D-MOS Transistor for Microwave Application," IEEE Transactions on Electron Devices, Vol. 19, #1, pp. 45-53, Jan. 1972.
- (2) T.J. Rodgers, J.D. Meindl, "V-MOS: High Speed Compatible MOS Logic," IEEE Journal of Solid State Circuits, Vol. 9, pp.239-250, Oct. 1974.
- (3) M.T. Elliott, M.R. Splinter, A.B. Jones, J.P. Reekstin, "Size Effects in E-Beam Fabricated MOS Devices," 1977 IEDM Technical Journal, pp. 11A-11B, Dec. 1977.
- (4) R.H. Dennard, F.H. Gaensslen, H. Yu, L. Rideout, E. Bassous, A.R. LeBlanc, "Design of Ion-Implanted MOS FET's with Very Small Physical Dimensions," IEEE Journal of Solid State Circuits Vol. 9, #5, pp. 256-268, Oct. 1974.
- (5) K.H. Nicholas, H.E. Brockman, I.J. Stemp, "Fabricated of Sub-Micron Polysilicon Lines by Conventional Techniques," Applied Physics Letters, Vol. 26, #7, pp. 398-399, April 1975.
- (6) A.C. Ipri, J.C. Sarace, "Integrated Circuit Process and Design Rule Techniques," RCA Review, Vol. 38, pp. 323-350, Sept. 1977.

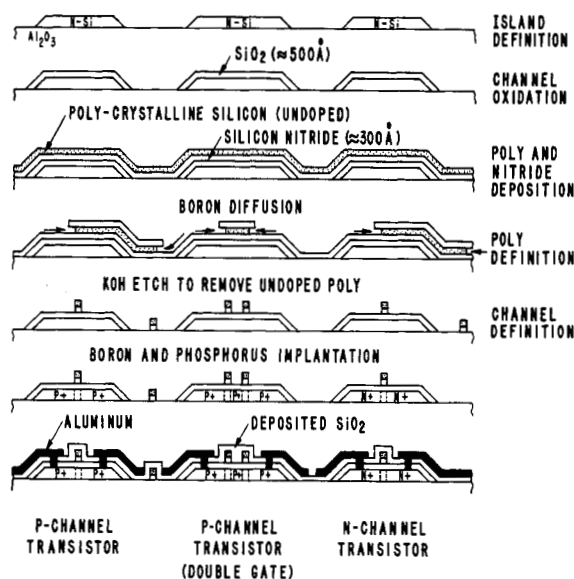
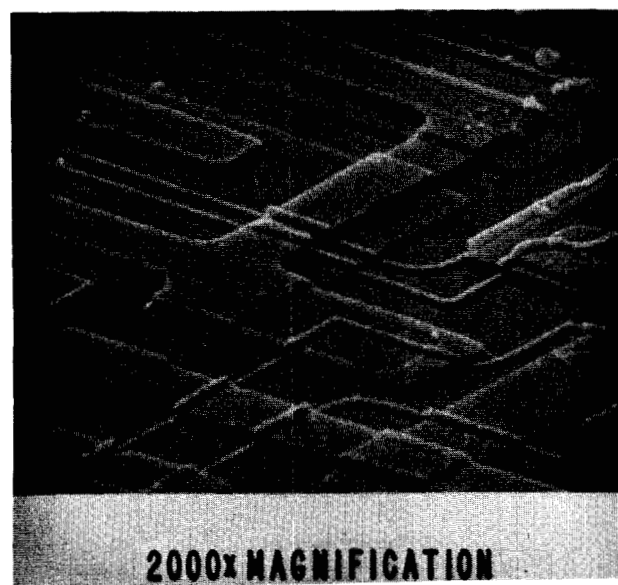
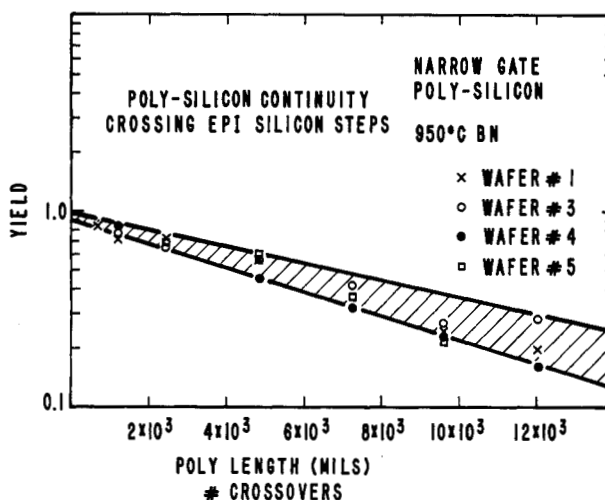


Figure 1 Narrow-gate CMOS/SOS process sequence



Photomicrograph of narrow-gate array

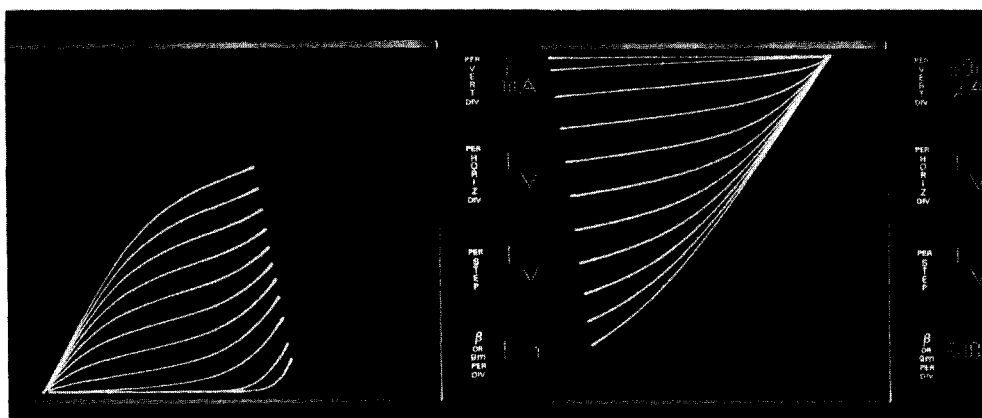
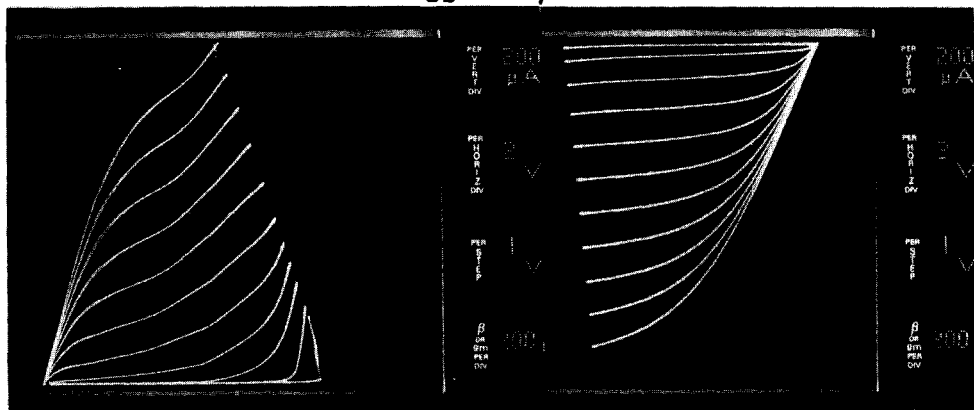
Figure 2



Continuity yield of narrow polysilicon lines crossing-over epi silicon steps

Figure 3

SG-968 #4
 $L_{SD} = 0.5 \mu m$



SINGLE GATE DEVICES

Figure 4 Single and dual gate device characteristics for polysilicon widths of $0.5 \mu m$

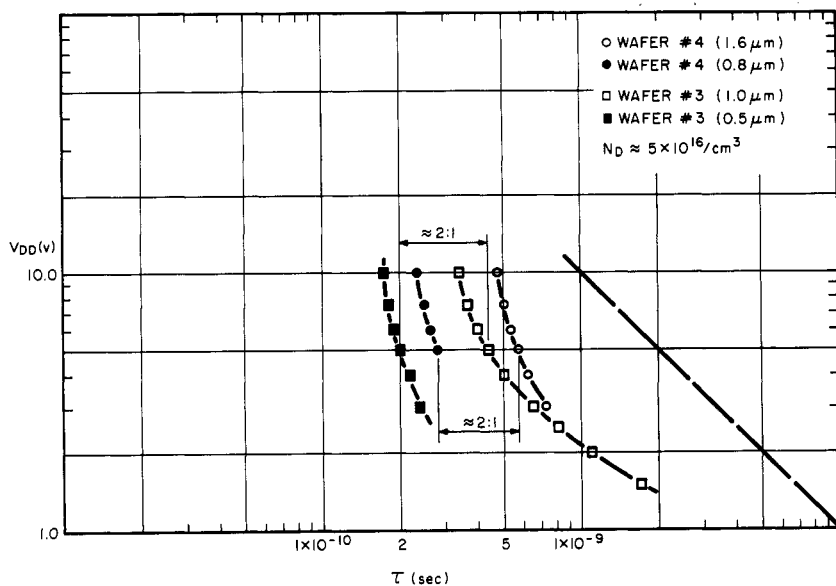


Figure 5 Narrow-gate ring oscillator performance

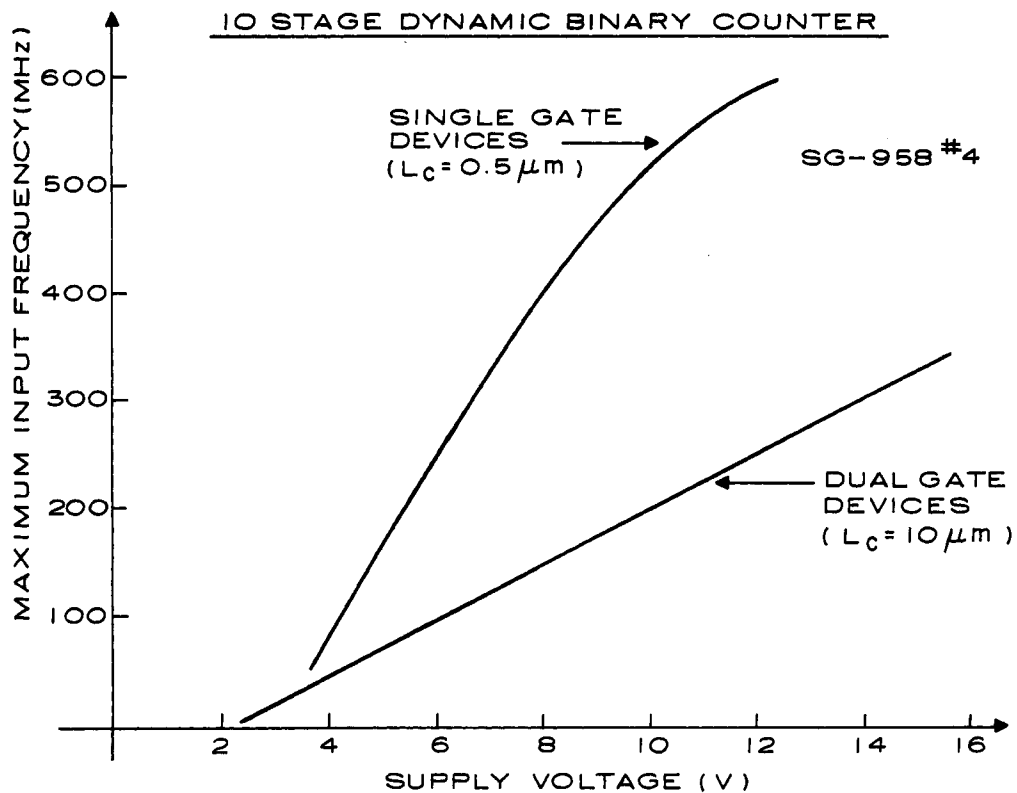


Figure 6 Maximum input frequency versus supply voltage for narrow-gate dynamic counters

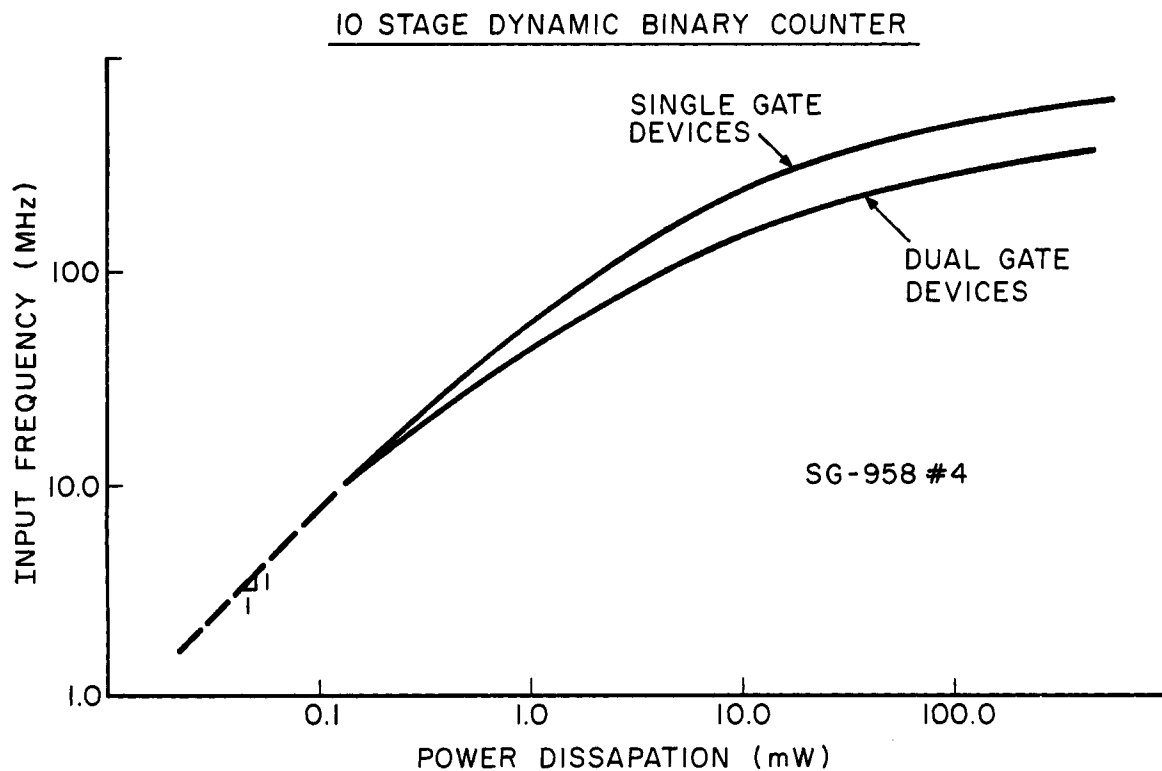
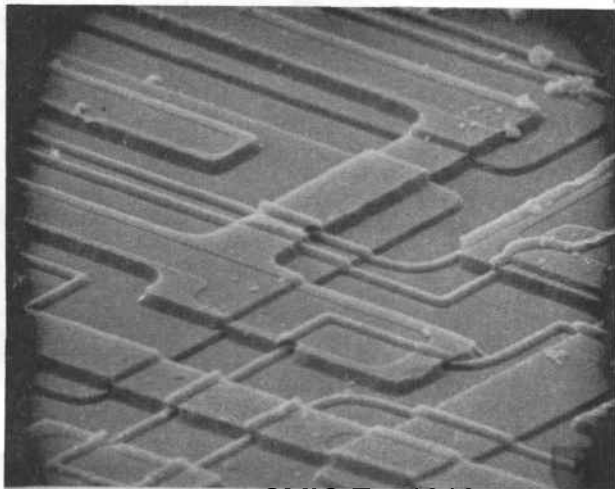


Figure 7 Power dissipation versus input frequency for single gate and dual gate dynamic binary counters



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