CIRCUIT HOT ELECTRON EFFECT SIMULATION

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ABSTRACT

Hot electron effects resulting from high electric fields in submicron devices can severely degrade device characteristics. As a result, severe performance degradation can occur at the circuit level. No simulator exists to predict this effect. The purpose of this paper is to present circuit hot electron effect simulation using our recently developed simulator. As a result, a circuit performance degradation due to hot electron can be simulated and the MOSFETs which results in this degradation can be identified.

INTRODUCTION

Hot electron effects resulting from high electric fields in typical VLSI MOSFET's can severely degrade device characteristics. Threshold voltage shifts and reduced current drive capability are typical. As a result, severe performance degradation can occur at the circuit level. Previous simulators have been done which either calculate the substrate current for MOSFETs only[1] or calculate substrate currents and predict only the threshold voltage (Vt) shift [2]. In a real circuit, device degradation involves not only Vt but also other parameters, like beta, gamma, drain effect, etc [3] as shown in table 1. Also in a circuit environment, substrate current alone is not a good parameter to predict circuit performance. For example, one MOSFET may be under stress (high substrate current) but this does not affect the circuit performance. On the other hand, one MOSFET may not be under much stress (low substrate current) but even a small degradation will affect the circuit performance. The objective of this paper is to simulate hot electron effects in a circuit environment and identify the MOSFETs which result in the performance degradation.

APPROACH

In order to analyze a circuit for hot electron problems, a measure of the stress each MOSFET experiences during normal circuit operation must be determined. The normalized DC substrate current (normalized by dividing by the device width) has been identified as a good indicator for stress and empirical relations have been obtained and used to predict the device degradation [4,5,6]. For example, the device lifetime τ, commonly defined as a $10mV$ threshold voltage shift, can be related to substrate current as

$$\tau = A * (I_{sub}/W)^{-n} \qquad (1)$$

where W is the device width and n is about 3. In a circuit environment, we can still use substrate current (function of time) as an indicator. It is normally done to calculate the substrate current for every MOSFET in the circuit and find out the ones which generate high substrate currents. This approach does not consider the circuit environment at all since some devices may degrade a lot but affect circuit performance very little and others may degrade circuit performance a lot with small characteristics changed.

We approach this problem differently by emphasizing the circuit performance degradation rather than the individual device degradation. The circuit performance degradation can be expressed as :

$$\Delta Perf = \sum \left(\frac{\Delta Perf}{\Delta Stress}\right)_{MOS} * (\Delta Stress)_{MOS} \qquad (2)$$

where the first part on the right hand side is the sensitivity. The usual approach only considers the stress part but not the sensitivity part. Our approach considers both sensitivity and stress of each MOSFET in the circuit.

The degradation of each MOSFET is based on the impact ionization induced substrate current that it generates in typical circuit operation and this must be simulated. To accomplish this, measurements of DC substrate currents are taken and used to curve fit with several parameters[1]. This equation is then used in SPICE so that the substrate current can be obtained from circuit simulations. An equivalent DC stress time was then calculated from empirical relation of degradation with respect to substrate current,

$$t_{DC} = \frac{\int_0^T (I_{sub}/W)^n dt}{(I_{sub}/W)^n_{DC}} \qquad (3)$$

and n=3 was used. The device degradation was then interpolated from the DC stress data table. All important

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parameters to represent the device degradation were included [3]. The performance degradation, could be delay time or precharge time increase depending on the circuit, due to one MOSFET degradation was then evaluated. The sensitivity of that MOSFET was calculated by perturbing its parameters according to stress experiment and evaluating the performance degradation accordingly. This process was repeated for every MOSFET in the circuit. The overall performance degradation could be calculated with all MOSFET degradation included and those sensitive MOSFETs could be pinpointed from the sensitivity information previously calculated.

RESULTS AND DISCUSSION

A precharge circuit in the 256K DRAM was analyzed with our simulator. The circuit is shown in Fig. 1 with four NMOSFETs. The node voltage and substrate current waveforms are shown in Fig. 2 and Fig. 3 respectively with supply voltage of 8V. It can be seen that M4 generates the highest substrate current, followed by M2 and M1, while M3 generates very low substrate current. The precharge time defined as the time required to charge the line BL0 to 90%VDD is the performance measure of interest and the sensitivity results with respect to stress on a device are shown in Fig. 4. These were computed as discussed previously except that the entire procedure was repeated for several values of stress as a perturbation so that curves could be plotted against stress. Notice that M1 has the highest sensitivity with respect to stress while M4 has almost zero sensitivity. The highest experimental stress data had Vt shift of 800 mV and linear current degradation of 22%, but the precharge time change due to M4 was still less than 0.1% which was the resolution due to interpolation. For practical purpose, we will take the sensitivity of M4 to be zero.

The stress of each device is changed continuously as a function of stress time due to device degradation of itself and all other devices in the circuit. The effective stress each device is subjected to from circuit operation is shown in Fig. 5 with and without feedback correction and is shown for different supply voltages and the stress values were normalized to the M1 value. We calculated the stress according to eq. (3) and obtained the without feedback correction result. Then we changed the parameters of each MOSFET according to the stress and generated a new SPICE run. The output of the new SPICE run was used to obtain the feedback correction stress from eq. (3). It can be seen that the stress feedback correction is very important and has to be included. The overall circuit performance degradation is determined from the data in Fig. 4 and Fig. 5. For low supply voltages found in normal operation M2 will be the critical device. M4 has the largest stress degradation, but not much more than M2, and since the sensitivity of M2 in Fig. 4 is much much larger than M4 the overall effect is that M2 is dominant. If only substrate current was considered then it would mistakenly identify M4 to be the critical device.

Substrate current increases exponentially with drain voltage and stress has been shown empirically to vary with a power law (n=3) of substrate current; therefore, with increased power supply voltage, as is usually done in accelerated stress, the stress increase in each MOSFET is different than normal operation. Because sensitivity is independent of power supply voltage, this means that performance degradation due to each MOSFET has been changed. In some cases, this will result in incorrect predictions. For example, in the precharge circuit, although M1 has a higher sensitivity, depending on the supply voltage, the relative performance effect will change between M1 and M2. For supply voltage higher than 8V, M1 will tend to dominate but for lower voltage M2 will dominate. This information can not be obtained without sensitivity analysis and one has to be aware of this effect when doing any accelerated circuit stressing.

In another example, we use the CMOS inverter chain as shown in Fig. 6. The purpose of this example is to study the p-channel contribution and relative position effect (n-channel) in a chain. The substrate currents are generated during the gate voltage switching since the bell-shape substrate current peaks at about half drain voltage. The substrate current from p-channel is much less than that of n-channel due to lower mobility and impact ionization coefficient of hole. The relative stress ratio with respect to N1 is shown in Fig. 7. It can be seen that relative stress ratio of p-channel device increases as VDD increases. This is because the feedback correction increases as VDD increases. The three n-channel MOSFETs have different stress depending on the position. The relative stress ratio respect to N1 is shown in Fig. 8. The first stage nMOSFET has highest stress. The center stage and last stage nMOSFETs have different stress ratio depending on power supply voltage. At low voltage, N3 has lowest stress but at high volatge, N2 has the lowest stress. The results indicate that relative stress of each MOSFET changes when power supply is changed. This implies that accelerated stress in a circuit is very different from a single transistor case.

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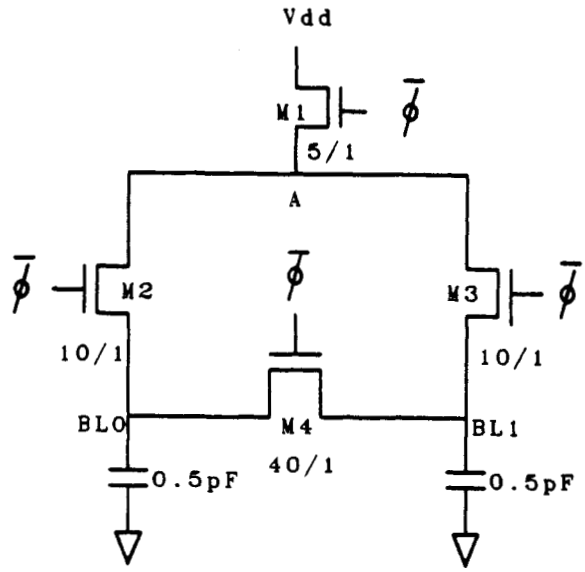

Fig. 1 DRAM precharge circuit used for simulation

Table 1 **EXPERIMENTAL RESULTS**

CHANGES AFTER 40 HOURS STRESS AT VD=8V, VG=3V, L=1.5 um	
VT0	**+ 20 %**
BETA	**- 20 %**
DRAIN EFFECT	**+ 20 %**
LAMDA	**+ 20 %**
THETA	**- 20 %**
GAMMA	**- 10 %**

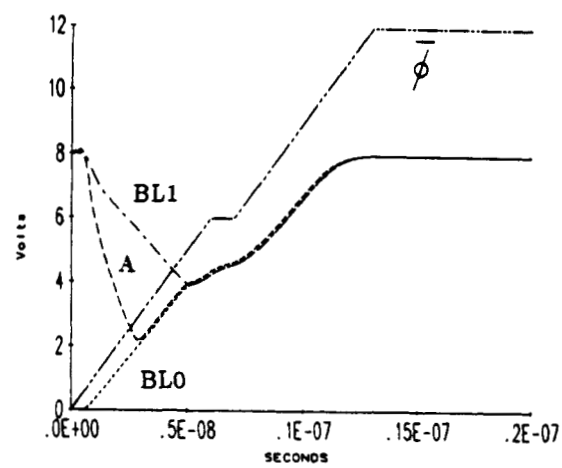

Fig. 2 Node voltage waveforms of the precharge circuit shown in Fig. 1.

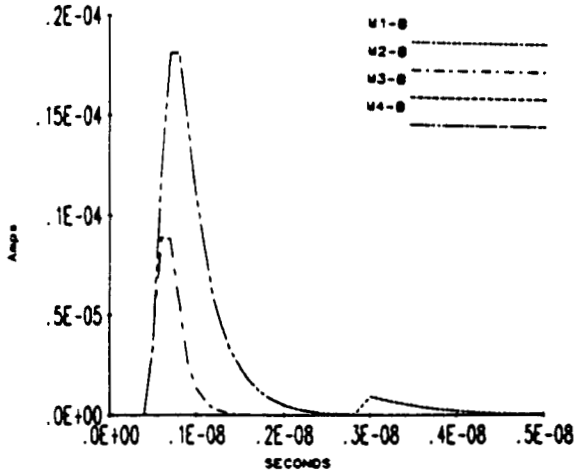

Fig. 3 Substrate currents generated in the precharge circuit

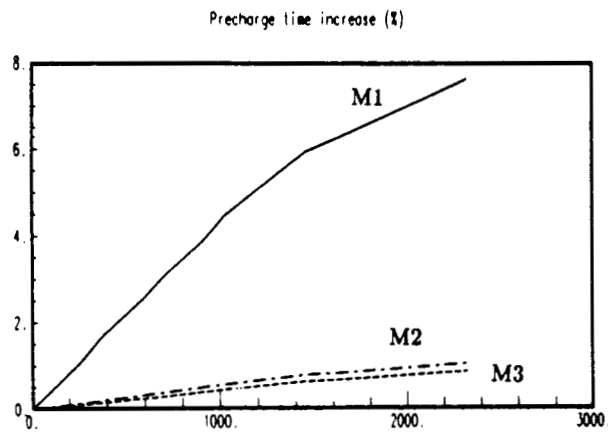

Fig. 4 Sensitivity of the MOSFET's in the precharge circuit, the x-axis is the DC stress time (hours) and y-axis is the precharge time increase (%), M4 is practically zero.

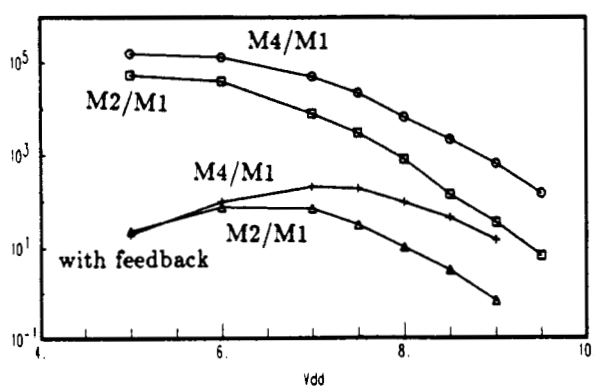

Fig. 5 Stress of M2 and M4 in precharge circuit with respect to M1 with and without stress correction.

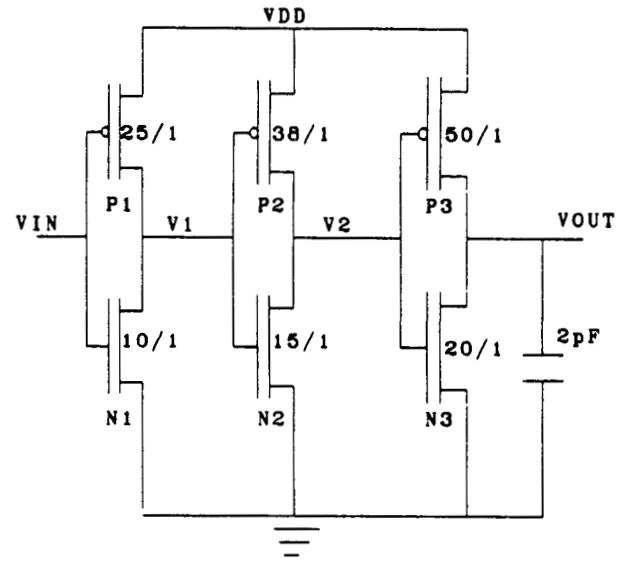

Fig. 6 The three-stage CMOS inverter chain used in the simulation.

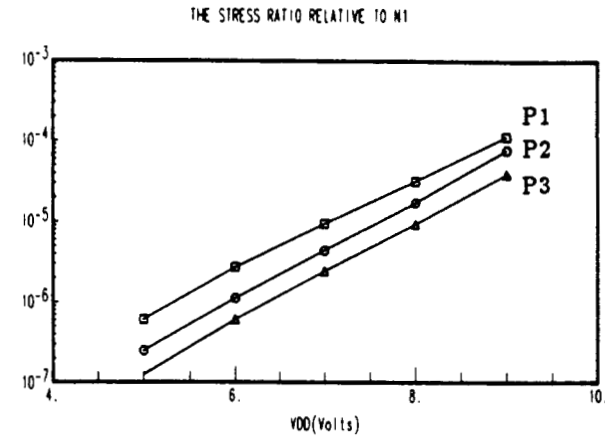

Fig. 7 The stress of p-channel MOSFETs with respect to N1 as a function of supply voltage.

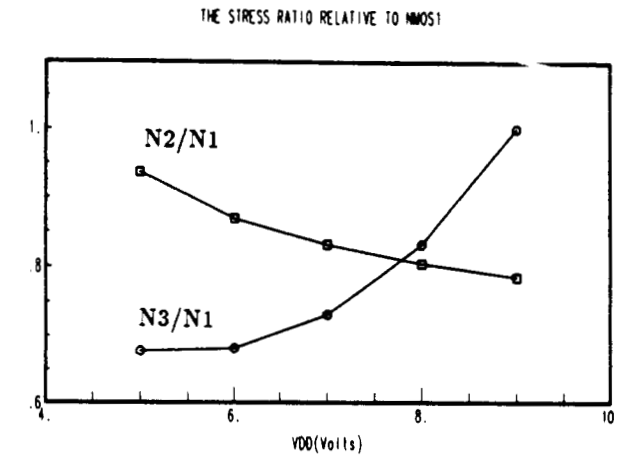

Fig. 8 The stress of n-channel MOSFETs with respect to N1 as a function of supply voltage.