

# **EXHIBIT A-1**

### **Invalidity Claim Chart of U.S. Patent No. 6,580,122 Based on U.S. Patent No. 5,960,297 (“Saki”)**

U.S. Patent No. 5,960,297 to Saki, (“Saki”) was filed on July 2, 1997 and issued on Sept. 29, 1999. Saki is prior art to U.S. Patent No. 6,580,122 (“the ’122 Patent”) at least under pre-AIA 35 U.S.C. § 102(b) because it issued more than one year before the earliest possible effective filing date of the ’122 Patent identified by Plaintiff in its infringement contentions, i.e., March 20, 2001. Plaintiff cannot assert an earlier invention date because Plaintiff failed to comply with paragraph 2 of the Court’s Order Governing Proceedings – Patent Case, including by failing to identify the “earliest date of invention” and failing to produce “all document evidencing conception and reduction to practice for each claimed invention.” Saki anticipates or renders obvious, alone or in combination with other prior art references, claims 1-3, 5-14, 16-25, 27-34 (“the Asserted Claims”) of the ’122 Patent under 35 U.S.C. §§ 102 and/or 103, as set forth in the chart below.

The citations provided in the chart below are only representative of the respective elements, rather than an exhaustive compilation of every aspect of the reference that is relevant to each limitation. To the extent Plaintiff alleges that this reference does not disclose any limitation in the Asserted Claims, either expressly or inherently, it would have been obvious to use the methods and systems described in the reference in combination with the other prior art identified in Defendants’ invalidity contentions, and/or in view of the knowledge of one of ordinary skill in the art at the relevant time about such systems and services.

Furthermore, to the extent Saki alone does not disclose or render obvious the Asserted Claims, it would have been obvious to a person having ordinary skill in the art at the time of the alleged invention to combine the teachings of Saki with the following references, as discussed in the chart below:

1. U.S. Patent No. 6,180,501 to Pey (“Pey”). Pey qualifies as prior art under at least pre-AIA §§ 102 (e). Pey was filed on Oct. 14, 1999 and issued on Jan. 30, 2001.
2. U.S. Patent No. 6,372,602 to Mitsuiki (“Mitsuiki”). Mitsuiki qualifies as prior art under at least pre-AIA §§ 102 (e). Mitsuiki was filed on May 15, 2000 and issued on April 16, 2002.
3. U.S. Patent No. 6,037,266 to Tao, et al. (“Tao”). Tao qualifies as prior art under at least pre-AIA §§ 102(a), 102(b), and 102(e). Tao was filed on Sep. 28, 1998 and issued on March 14, 2000.
4. U.S. Patent No. 6,429,062 to Rubin, et al. (“Rubin”). Rubin qualifies as prior art under at least pre-AIA §§ 102 (e). Rubin was filed on Sept. 20, 1999 and issued Aug. 6, 2002.
5. Korean Patent App. No. KR1997-010326 to Yun, et al. (“Yun”). *See* Ex. A-2.

6. U.S. Patent No. 5,786,263 to Perera (“Perera”). Perera qualifies as prior art under at least pre-AIA §§ 102(a), 102(b), and 102(e). Perera was filed on April 4, 1995 and issued on July 28, 1998.
7. U.S. Patent No. 5,859,466 to Wada (“Wada”). Wada qualifies as prior art under at least pre-AIA §§ 102(a), 102(b), and 102(e). Wada was filed on June 6, 1996 and issued on Jan. 12, 1999.
8. Applicants’ Admitted Prior Art (“APA”) in the ’122 patent, disclosed in, among others, the Background of the Invention and Figures 1 and 2 of the ’122 patent.

With respect to the APA, “[a]dmissions in the specification regarding the prior art are binding on the patentee for purposes of a later inquiry into obviousness.” *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1362 (Fed. Cir. 2007); *see also In re Nomiya*, 509 F.2d 566, 570-71 (CCPA 1975) (“We see no reason why appellants’ representations in their application should not be accepted at face value as admissions that Figs. 1 and 2 may be considered ‘prior art’ for any purpose, including use as evidence of obviousness under § 103.”); *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1570 (Fed. Cir. 1988) (“A statement in a patent that something is in the prior art is binding on the applicant and patentee for determinations of anticipation and obviousness.”).

To the extent the citations provided in the chart below suggest combining aspects of different embodiments from Saki, or modifying an aspect of one of Saki’s embodiments in view of a different embodiment, it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention to combine or modify Saki’s embodiments as suggested. For example, Saki explains that “[t]he same advantages which are obtained in the first embodiment are also obtained in the second embodiment.” Saki at 6:52-53. Saki also describes the formation of “a trench DRAM cell” “in accordance with the present invention,” without limiting that formation to a specific embodiment of the invention. *See id.* at 6:54-9:4. Thus, per Saki’s own disclosure, combining or modifying Saki, in view of Saki, would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.

Nothing in this claim chart should be construed as an admission regarding infringement, either literally or under the doctrine of equivalents, or as an admission regarding Defendants’ understanding of the proper scope of the Asserted Claims. Given the ambiguities and other deficiencies in Plaintiff’s infringement contentions, the exemplary citations herein necessarily account for a variety of possible infringement arguments and claim constructions. Furthermore, the citations provided in these claim charts are intended to be only exemplary in nature. Defendants reserve the right to rely on additional citations or sources of evidence that also

may be applicable. Further, this chart is subject to all reservations, objections, and disclaimers in Defendants' Invalidity Contentions and any amendment, supplement, or modification thereof, which are incorporated herein by reference in their entirety.

Several terms of the Asserted Claims are indefinite under 35 U.S.C. § 112, ¶ 2. For those claim limitations containing indefinite terms, SMIC's offer herein of exemplary prior art disclosures is based solely on SMIC's present understanding of the claim scope that IFT appears to be advocating in its infringement contentions, and nothing provided herein should be construed as an admission that a person of ordinary skill in the art would understand, with reasonable certainty, the scope of the claims.

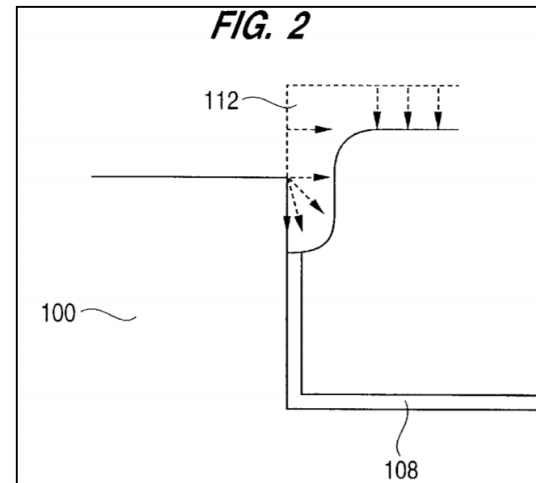
Claim	Prior Art Disclosure
[1pre] A transistor, comprising:	<p><b>To the extent the preamble of claim 1 is found to be limiting, Saki discloses a transistor. By way of non-limiting example, Saki discloses:</b></p> <p>“The present invention generally relates to highly integrated semiconductor devices such as semiconductor memory devices and, more particularly, to an isolation structure for such devices and the methods for forming the isolation structure.”  <i>See, e.g., Saki at 1:7-11.</i></p> <p>“An integrated circuit may be formed by connecting together various elements such as transistors which are formed on a semiconductor substrate. To ensure proper functioning of the integrated circuit, these elements must be electrically isolated from each other. Such isolation can be achieved using local oxidation of silicon (LOCOS) or shallow trench isolation (STI). Shallow trench isolation is particularly advantageous for circuits having a high integration density since shallow trench isolation can provide for a relatively planar surface on which subsequent insulating and/or conducting layers may be formed.</p> <p>A conventional process for forming a shallow trench isolation (STI) structure is shown in FIGS. 1(a)-1(f). A silicon dioxide (SiO<sub>2</sub>) layer 102 and a silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 104 are successively formed on the surface of a silicon substrate 100 as shown in FIG. 1(a). A patterned resist (not shown) is formed on the upper surface of silicon nitride layer 104 and an etching process such as reactive ion etching (RIE) is used to form trenches 106 in silicon substrate 100 as shown in FIG. 1(b). A thermal oxidation process is then performed to form a thermal silicon dioxide (SiO<sub>2</sub>) layer 108 on the exposed surfaces of the silicon substrate 100 as shown in FIG. 1(c). A silicon dioxide (SiO<sub>2</sub>) layer 110 is then deposited by the decomposition of TEOS, for</p>

	<p>example, to fill in trenches 106 as shown in FIG. 1(d). The silicon dioxide layer 110 is then planarized by chemical mechanical polishing (CMP), for example, as shown in FIG. 1(e). Silicon nitride layer 104 serves as a stopper layer for the planarization process. Silicon nitride layer 104 is then removed. Various wet etching processes are used in subsequent manufacturing steps to remove the silicon dioxide layer 102, as well as to remove any sacrificial or dummy silicon dioxide layers which may be formed after removal of the silicon nitride layer. Such sacrificial silicon dioxide layers may be formed to clean the substrate surface prior to growing a gate oxide layer or to repair substrate damage due, for example, to implantation processes (e.g., channel implantation processes for controlling a threshold voltage of a transistor). However, these wet etching processes cause an etching away of the silicon dioxide at the corner 112 of the shallow trench isolation structure as shown in FIG. 1(f). This etching away of the silicon dioxide at the corner of the shallow trench isolation structure is shown in more detail in FIG. 2 and can result in a lowering of the threshold voltage of a transistor formed in the active area defined by the shallow trench isolation structure.”</p> <p><i>See, e.g., Saki at 1:14-59.</i></p> <p>“FIGS. 8(a) and 8(b) illustrate a trench DRAM cell with a self-aligned buried strap which is isolated from other cells by a shallow trench isolation structure in accordance with the present invention. Specifically, FIG. 8(a) is a top-down view of the trench DRAM cell and FIG. 8(b) is a cross-sectional view taken along line A-A' of FIG. 8(a). DRAM cell 50 includes a trench capacitor 55 and a transfer gate 60. Trench capacitor 55 includes a first N<sup>+</sup>-type polycrystalline silicon fill 65, a second polycrystalline silicon fill 67, and a collar oxide 71. Transfer gate 60 includes N-type source/drain and drain/source regions 73 and 74 formed in P-type well 75 and a WSix /polycrystalline silicon gate 77 insulatively spaced from the channel region between source/drain region 73 and drain/source region 74. A bit line contact 79 formed in an opening in an insulating layer 80 (of BPSG, for example) electrically connects source/drain region 73 to bit line 81. A shallow trench isolation structure formed in accordance with the present invention electrically isolates DRAM cell 50 from an adjacent DRAM cell and passing word line 92. Passing word line 92 has a WSix /polycrystalline silicon structure. A dielectric layer 87 is formed on bit line 81 and aluminum wirings 89 are formed on dielectric layer 87. One of the aluminum wirings 89 is connected to bit line 81 by a contact stud 91 of tungsten, for example. A diffusion region 83 electrically connects third polycrystalline silicon fill 69 and drain/source region 74 of MOS transfer gate 60. This diffusion region is formed by outdiffusing dopants</p>
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	<p>from the highly doped polycrystalline silicon fill in the storage trench into P-well 75. Diffusion region 83 and third polycrystalline silicon fill 69 constitute a buried strap for connecting trench capacitor 55 to transfer gate 60.</p> <p><i>See, e.g., Saki at 6:54-7:18.</i></p>
[1a] a semiconducting substrate;	<p><b>Saki discloses a semiconducting substrate. By way of non-limiting example, Saki discloses:</b></p> <p>“An integrated circuit may be formed by connecting together various elements such as transistors which are formed on a semiconductor substrate. To ensure proper functioning of the integrated circuit, these elements must be electrically isolated from each other. Such isolation can be achieved using local oxidation of silicon (LOCOS) or shallow trench isolation (STI). Shallow trench isolation is particularly advantageous for circuits having a high integration density since shallow trench isolation can provide for a relatively planar surface on which subsequent insulating and/or conducting layers may be formed.</p> <p><i>See, e.g., Saki at 1:14-24.</i></p> <p>“A conventional process for forming a shallow trench isolation (STI) structure is shown in FIGS. 1(a)-1(f). A silicon dioxide (SiO<sub>2</sub>) layer 102 and a silicon nitride (Si<sub>3</sub> N<sub>4</sub>) layer 104 are successively formed on the surface of a silicon substrate 100 as shown in FIG. 1(a). A patterned resist (not shown) is formed on the upper surface of silicon nitride layer 104 and an etching process such as reactive ion etching (RIE) is used to form trenches 106 in silicon substrate 100 as shown in FIG. 1(b). A thermal oxidation process is then performed to form a thermal silicon dioxide (SiO<sub>2</sub>) layer 108 on the exposed surfaces of the silicon substrate 100 as shown in FIG. 1(c). A silicon dioxide (SiO<sub>2</sub>) layer 110 is then deposited by the decomposition of TEOS, for example, to fill in trenches 106 as shown in FIG. 1(d). The silicon dioxide layer 110 is then planarized by chemical mechanical polishing (CMP), for example, as shown in FIG. 1(e). Silicon nitride layer 104 serves as a stopper layer for the planarization process. Silicon nitride layer 104 is then removed. Various wet etching processes are used in subsequent manufacturing steps to remove the silicon dioxide layer 102, as well as to remove any sacrificial or dummy silicon dioxide layers which may be formed after removal of the silicon nitride layer. Such sacrificial silicon dioxide layers may be formed to clean the substrate surface prior to growing a gate oxide layer or to repair substrate damage due, for example, to implantation processes (e.g., channel implantation processes for controlling a threshold voltage of a transistor). However,</p>

these wet etching processes cause an etching away of the silicon dioxide at the corner 112 of the shallow trench isolation structure as shown in FIG. 1(f). This etching away of the silicon dioxide at the corner of the shallow trench isolation structure is shown in more detail in FIG. 2 and can result in a lowering of the threshold voltage of a transistor formed in the active area defined by the shallow trench isolation structure.”

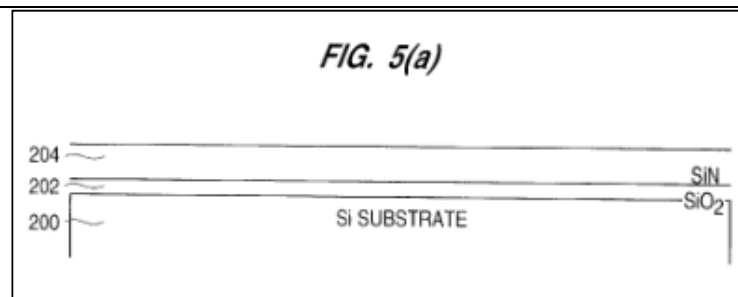
See, e.g., Saki at 1:25-59; see also *id.* at 1:60-2:14, Figs. 1(a)-1(f), Figs. 3(a)-3(f), Fig. 2:



“In accordance with one aspect of the present invention, an isolation structure is provided by a method which includes forming a pad oxide layer on a semiconductor substrate and then forming a pad nitride layer on the pad oxide layer. An opening is then formed which extends through the pad nitride layer, the pad oxide layer, and into the semiconductor substrate. The pad nitride layer is then isotropically etched, thereby pulling-back the pad nitride layer from the portion of the opening extending through the pad oxide layer. An insulating layer is formed to fill in the opening including the portion of the opening formed by the pulling-back of the pad nitride layer. The deposited insulating layer is then planarized using the pulled-back nitride layer as a stopper layer. The pulled-back pad nitride layer and the pad oxide layer are then removed.”

See, e.g., Saki at 2:61-3:8.

	<p>“FIGS. 5(a)-5(i) are cross-sectional views illustrating a method for forming a shallow trench isolation structure in accordance with a first embodiment of the present invention. As shown in FIG. 5(a), a pad silicon dioxide (<math>\text{SiO}_2</math>) layer 202 and a pad silicon nitride (<math>\text{Si}_3\text{N}_4</math>) layer 204 are provided on a substrate 200. Silicon dioxide layer 202 has a thickness of about 80 Å-100 Å (e.g., 82 Å) and may be formed by thermal oxidation or by low pressure chemical vapor deposition (LPCVD), for example. Silicon nitride layer 204 has a thickness of about 1000 Å-2000 Å (e.g., 1300 Å) and may be formed, for example, by LPCVD. Substrate 200 may be a silicon wafer or an epitaxial layer formed on a silicon wafer. A patterned photoresist (not shown) is then formed on pad silicon nitride layer 204. The pad silicon nitride layer, the pad silicon dioxide layer, and the substrate are then etched, for example, by reactive ion etching using the patterned photoresist as a mask to form a trench 206 as shown in FIG. 5(b). A thin silicon dioxide (<math>\text{SiO}_2</math>) layer 208 having a thickness of about 80 Å-100 Å is formed by a high temperature (for example, 1000° C.) thermal oxidation over the portions of the silicon substrate exposed by the forming of trench 206 as shown in FIG. 5(c). This high temperature oxidation removes substrate damage caused by the etching process for forming trench 206. Pad silicon nitride layer 204 is then isotropically etched by, for example, chemical dry etching. In accordance with the present invention, the amount of silicon nitride which is etched during this isotropic etching step is about 250 Å. Thus, the isotropic etch pulls back pad silicon nitride layer 204 by a distance <math>L=250</math> Å relative to the sidewall of trench 206 as shown in FIG. 5(d). It will be apparent to one skilled in the art that the amount of silicon nitride to be isotropically etched in this etching step will depend on the overall manufacturing process into which the teachings of this invention are incorporated. In general, the amount of silicon nitride to be etched should be sufficient to result in the protection of the corners of the shallow trench isolation structure from attack. In addition, the isotropic etching of the pad silicon nitride layer should leave silicon nitride having a thickness which is sufficient to function as a stopper layer for the planarization process to be described below with reference to FIG. 5(f).”</p> <p><i>See, e.g., Saki at 3:66-4:39.</i></p>
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See, e.g., Saki at Fig. 5(a); see also *id.* at Figs. 5(b)-5(i).

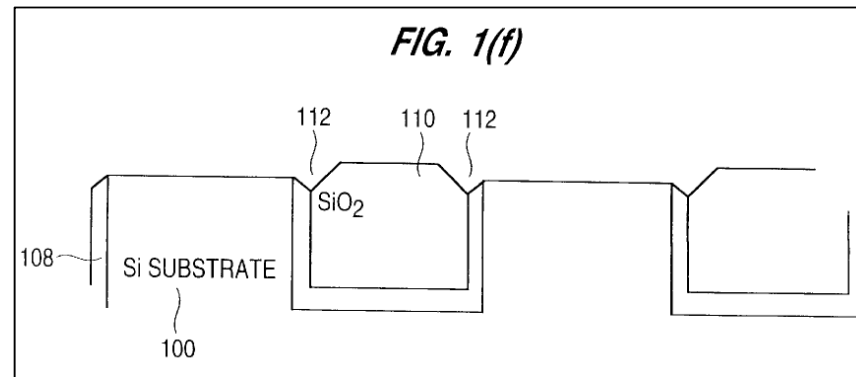
“FIGS. 7(a)-7(h) are cross-sectional views illustrating a method for forming a shallow trench isolation structure in accordance with a second embodiment of the present invention. As shown in FIG. 7(a), a pad silicon dioxide (SiO<sub>2</sub>) layer 202 and a pad silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 204 are provided on a substrate 200. Silicon dioxide layer 202 has a thickness of about 80 Å-100 Å (e.g., 82 Å) and may be formed by thermal oxidation or by low pressure chemical vapor deposition (LPCVD), for example. Silicon nitride layer 204 has a thickness of about 1000 Å-2000 Å (e.g., 1300 Å) and may be formed, for example, by LPCVD. Substrate 200 may be a silicon wafer or an epitaxial layer formed on a silicon wafer. A patterned photoresist (not shown) is then formed on pad silicon nitride layer 204. The pad silicon nitride layer, the pad silicon dioxide layer, and the substrate are then etched by, for example, reactive ion etching using the patterned photoresist as a mask to form a trench 206 as shown in FIG. 7(b). Pad silicon nitride layer 204 is then isotropically etched using, for example, HF/Glycerol or hot phosphoric acid. In accordance with the present embodiment, the amount of silicon nitride which is etched during this isotropic etching step is about 250 Å. Thus, the isotropic etch pulls back the pad silicon nitride layer by a distance  $L=250\text{ Å}$  relative to the sidewall of trench 206, as shown in FIG. 7(c). A thin silicon dioxide (SiO<sub>2</sub>) layer 208 having a thickness of about 80 Å-100 Å is formed by a high temperature (for example, 1000° C.) thermal oxidation over the portions of the silicon substrate exposed by the forming of trench 206 as shown in FIG. 7(d). This high temperature oxidation removes substrate damage caused by the etching process for forming trench 206. Optionally, a thin silicon nitride layer (not shown) having a thickness of about 50 Å may then be deposited by, for example, CVD on pad silicon nitride layer 204 and on silicon dioxide layer 208. The silicon nitride layer may be provided, for example, in order to

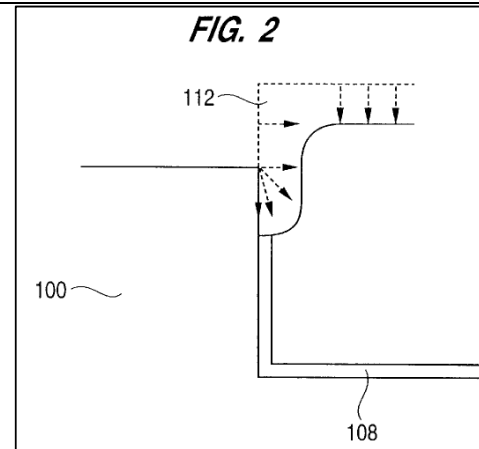
	<p>prevent oxidation of underlying layers during subsequent processing steps. As in the first embodiment, if the 50 Å silicon nitride layer is formed, the amount of silicon nitride which is etched during the isotropic etching step is about 300 Å. In this way, a composite silicon nitride layer is formed which is pulled back by about 250 Å from the sidewall of trench 206. Next, a silicon dioxide layer 212 is blanket deposited over the entire surface of the substrate using, for example, a CVD process in which TEOS (<math>\text{Si}(\text{OC}_2\text{H}_5)_4</math>) is decomposed, as shown in FIG. 7(e). The silicon dioxide layer 212 is then planarized using, for example, RIE, chemical mechanical polishing, or a combination thereof as shown in FIG. 7(f). The pad silicon nitride layer 204 is then removed by, for example, chemical dry etching (CDE) or etching using hot phosphoric acid or HF/glycerol as shown in FIG. 7(g). One or more wet etching processes are then utilized to remove the pad silicon dioxide layer 202, as well as any sacrificial or dummy oxide layers which may be formed, resulting in the structure shown in FIG. 7(h). Because the pad silicon nitride layer was pulled-back by an isotropic etching process, the shallow trench isolation structure of FIG. 7(g) has a T-shape. In this way, subsequent wet etching processes for removing the pad silicon dioxide layer 202 and any sacrificial or dummy oxide layers attack these extensions of the shallow trench isolation structure and do not result in an etching away of the insulator at the corner of the shallow trench isolation structure as can be seen with reference to FIG. 7(h).</p> <p>The same advantages which are obtained in the first embodiment are also obtained in the second embodiment.”</p> <p><i>See, e.g., Saki at 5:55-6:53; see also id. at Figs. 7(a)-(h).</i></p> <p>“A method of manufacturing the DRAM cell 50 using the shallow isolation structure and method of the present invention will be described below with reference to FIGS. 9(a)-9(g). As shown in FIG. 9(a), a buried N-type well 48 is formed in a P-type semiconductor substrate 300 by implanting phosphorous below the intended P-well for a memory cell array. A buried N-type well may also be formed by other methods, e.g., P-well implantation into an N-type semiconductor substrate or by epitaxy, and the invention is not limited in this respect. A silicon nitride layer 302 having a thickness of about 0.2 micrometers is formed by chemical vapor deposition, for example, on the surface of a thin oxide layer 301 having a thickness of about 10 nanometers which is thermally grown on semiconductor substrate 300. Oxide layer 301 and silicon nitride layer 302 are patterned and etched to provide a mask for etching a trench 303.</p>
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	<p>Trench 303 is etched using an anisotropic etching process to a depth of about 8 micrometers as shown in FIG. 9(b). After storage node trench 303 is etched, an N-type capacitor plate 304 is formed by outdiffusing arsenic from the lower portion of trench 303. This may be accomplished, for example, by depositing an arsenic doped glass layer, etching the arsenic doped glass layer to remain only at the lower portion of trench 303, and performing an annealing process to outdiffuse the arsenic. A storage node dielectric layer (not shown) such as an oxide-nitride (ON) layer or a nitride-oxide (NO) layer is then formed in trench 303. After the dielectric layer is formed, a first conductive region is formed by filling trench 303 with an impurity-doped first conductive material such as N<sup>+</sup> -type polycrystalline silicon. The filling step may be carried out using chemical vapor deposition of silane or disilane, for example. The N<sup>+</sup> -type polycrystalline silicon is then etched back to a first level within trench 303 using an isotropic etch process to form first trench fill 65. The level of first trench fill 65 is, for example, about 1.0 micrometer below the surface of semiconductor substrate 300. Collar oxide 71 is then formed on the sidewall of the portion of trench 303 opened by the etching back of the N<sup>+</sup> -type polycrystalline silicon using low pressure chemical vapor deposition (LPCVD) or plasma-enhanced chemical vapor deposition (PECVD) TEOS as shown in FIG. 9(c).”</p> <p><i>See also</i>, Saki at 7:19-59; <i>see also id.</i> at 7:60-25, Figs. 9(a)-9(g).</p>
<p>[1b] a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove;</p>	<p><b>Saki discloses a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove. By way of non-limiting example, Saki discloses:</b></p> <p>“An integrated circuit may be formed by connecting together various elements such as transistors which are formed on a semiconductor substrate. To ensure proper functioning of the integrated circuit, these elements must be electrically isolated from each other. Such isolation can be achieved using local oxidation of silicon (LOCOS) or shallow trench isolation (STI). Shallow trench isolation is particularly advantageous for circuits having a high integration density since shallow trench isolation can provide for a relatively planar surface on which subsequent insulating and/or conducting layers may be formed.</p> <p><i>See, e.g.</i>, Saki at 1:14-24.</p> <p>“A conventional process for forming a shallow trench isolation (STI) structure is shown in FIGS. 1(a)-1(f). A silicon dioxide (SiO<sub>2</sub>) layer 102 and a silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 104 are successively formed on the surface of a silicon substrate 100 as shown in FIG. 1(a). A patterned</p>

resist (not shown) is formed on the upper surface of silicon nitride layer 104 and an etching process such as reactive ion etching (RIE) is used to form trenches 106 in silicon substrate 100 as shown in FIG. 1(b). A thermal oxidation process is then performed to form a thermal silicon dioxide (SiO<sub>2</sub>) layer 108 on the exposed surfaces of the silicon substrate 100 as shown in FIG. 1(c). A silicon dioxide (SiO<sub>2</sub>) layer 110 is then deposited by the decomposition of TEOS, for example, to fill in trenches 106 as shown in FIG. 1(d). The silicon dioxide layer 110 is then planarized by chemical mechanical polishing (CMP), for example, as shown in FIG. 1(e). Silicon nitride layer 104 serves as a stopper layer for the planarization process. Silicon nitride layer 104 is then removed. Various wet etching processes are used in subsequent manufacturing steps to remove the silicon dioxide layer 102, as well as to remove any sacrificial or dummy silicon dioxide layers which may be formed after removal of the silicon nitride layer. Such sacrificial silicon dioxide layers may be formed to clean the substrate surface prior to growing a gate oxide layer or to repair substrate damage due, for example, to implantation processes (e.g., channel implantation processes for controlling a threshold voltage of a transistor). However, these wet etching processes cause an etching away of the silicon dioxide at the corner 112 of the shallow trench isolation structure as shown in FIG. 1(f). This etching away of the silicon dioxide at the corner of the shallow trench isolation structure is shown in more detail in FIG. 2 and can result in a lowering of the threshold voltage of a transistor formed in the active area defined by the shallow trench isolation structure.”

*See, e.g., Saki at 1:25-59.*





See, e.g., Saki at Figs. 1(e)-(f), 2.

“Accordingly, it would be desirable to provide a shallow trench isolation structure and methods for forming the shallow trench isolation structure which avoid these and other problems.”

See, e.g., Saki at 2:55-58.

“In accordance with one aspect of the present invention, an isolation structure is provided by a method which includes forming a pad oxide layer on a semiconductor substrate and then forming a pad nitride layer on the pad oxide layer. An opening is then formed which extends through the pad nitride layer, the pad oxide layer, and into the semiconductor substrate. The pad nitride layer is then isotropically etched, thereby pulling-back the pad nitride layer from the portion of the opening extending through the pad oxide layer. An insulating layer is formed to fill in the opening including the portion of the opening formed by the pulling-back of the pad nitride layer. The deposited insulating layer is then planarized using the pulled-back nitride layer as a stopper layer. The pulled-back pad nitride layer and the pad oxide layer are then removed.”

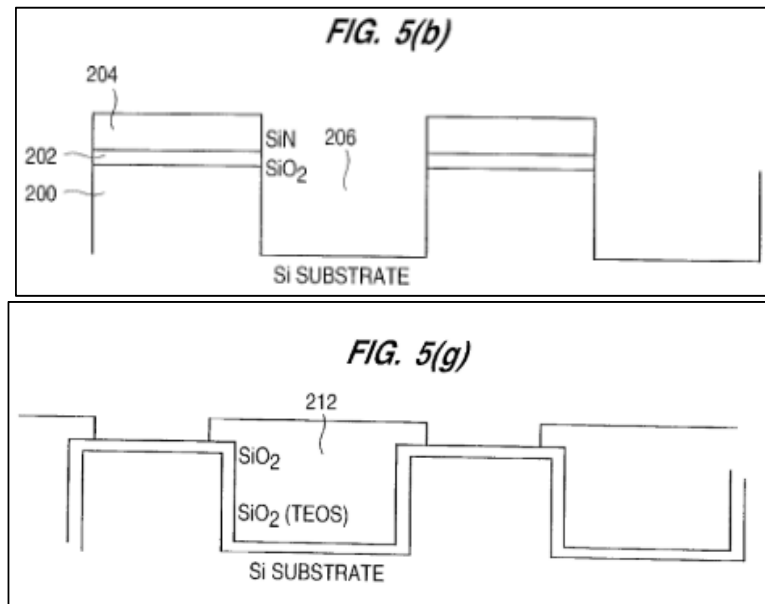
See, e.g., Saki at 2:61-3:8.

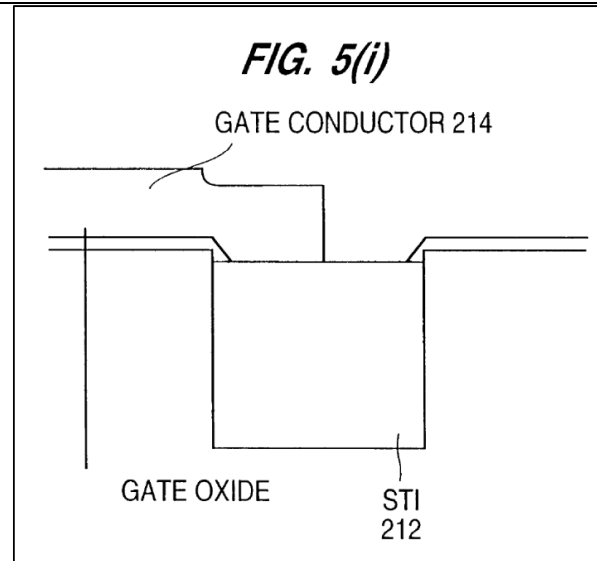
“FIGS. 5(a)-5(i) are cross-sectional views illustrating a method for forming a shallow trench isolation structure in accordance with a first embodiment of the present invention.”

	<p><i>See, e.g., Saki at 3:41-43.</i></p> <p>“FIGS. 5(a)-5(i) are cross-sectional views illustrating a method for forming a shallow trench isolation structure in accordance with a first embodiment of the present invention. As shown in FIG. 5(a), a pad silicon dioxide (<math>\text{SiO}_2</math>) layer 202 and a pad silicon nitride (<math>\text{Si}_3\text{N}_4</math>) layer 204 are provided on a substrate 200. Silicon dioxide layer 202 has a thickness of about 80 Å-100 Å (e.g., 82 Å) and may be formed by thermal oxidation or by low pressure chemical vapor deposition (LPCVD), for example. Silicon nitride layer 204 has a thickness of about 1000 Å-2000 Å (e.g., 1300 Å) and may be formed, for example, by LPCVD. Substrate 200 may be a silicon wafer or an epitaxial layer formed on a silicon wafer. A patterned photoresist (not shown) is then formed on pad silicon nitride layer 204. The pad silicon nitride layer, the pad silicon dioxide layer, and the substrate are then etched, for example, by reactive ion etching using the patterned photoresist as a mask to form a trench 206 as shown in FIG. 5(b). A thin silicon dioxide (<math>\text{SiO}_2</math>) layer 208 having a thickness of about 80 Å-100 Å is formed by a high temperature (for example, 1000° C.) thermal oxidation over the portions of the silicon substrate exposed by the forming of trench 206 as shown in FIG. 5(c). This high temperature oxidation removes substrate damage caused by the etching process for forming trench 206. Pad silicon nitride layer 204 is then isotropically etched by, for example, chemical dry etching. In accordance with the present invention, the amount of silicon nitride which is etched during this isotropic etching step is about 250 Å. Thus, the isotropic etch pulls back pad silicon nitride layer 204 by a distance <math>L=250</math> Å relative to the sidewall of trench 206 as shown in FIG. 5(d). It will be apparent to one skilled in the art that the amount of silicon nitride to be isotropically etched in this etching step will depend on the overall manufacturing process into which the teachings of this invention are incorporated. In general, the amount of silicon nitride to be etched should be sufficient to result in the protection of the corners of the shallow trench isolation structure from attack. In addition, the isotropic etching of the pad silicon nitride layer should leave silicon nitride having a thickness which is sufficient to function as a stopper layer for the planarization process to be described below with reference to FIG. 5(f).”</p> <p><i>See, e.g., Saki at 3:66-4:39.</i></p> <p>“Thus, in accordance with the above-described method of the present invention, etching of the insulator at the corner of the shallow trench isolation structure is suppressed and problems due to changes in the threshold voltages of elements formed in the active area defined by the</p>
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shallow trench isolation structure can be minimized. As discussed with respect to FIG. 4, the degree to which the corner of the structure is protected is determined by the length "L". In accordance with the present invention, this length "L" is determined by the isotropic etching of the pad silicon nitride layer. Since, in accordance with the present invention, only a single process factor affects the length "L", enhanced controllability of the shape of the shallow trench isolation structure can be achieved and therefore fluctuations in device characteristics can be reduced. In addition, because an upper surface of the shallow trench isolation structure and the surface of the substrate are substantially level, no step is created between the shallow trench isolation structure and a subsequently formed gate conductor 214 as shown in FIG. 5(i). Thus, patterning of the gate electrode is simplified. Still further, the method of the present invention has a small number of steps and therefore contributes to ease of device manufacture and reduced manufacturing costs."

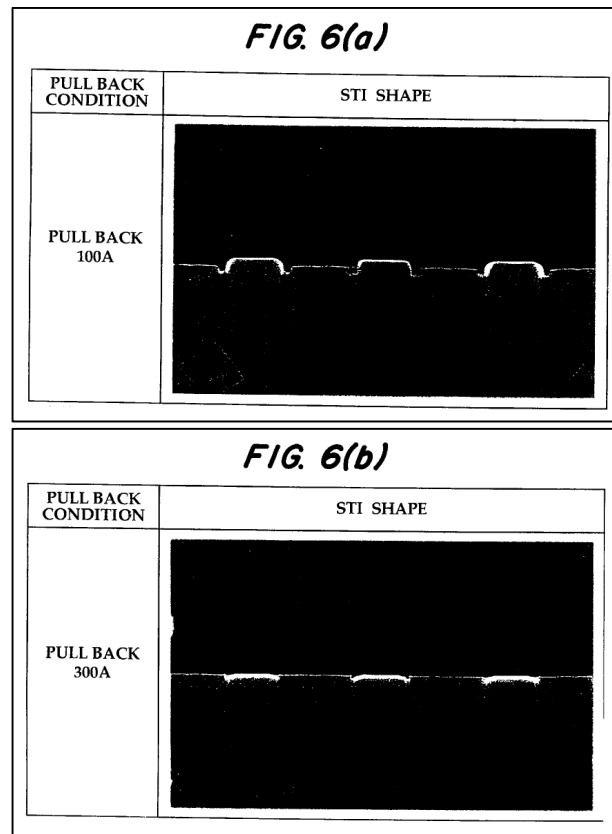
*See, e.g., Saki at 5:7-30.*





*See, e.g., Saki at Fig. 5(b), 5(g), 5(i); see also id. at Figs. 5(a), 5(c)-5(f), 5(h).*

“FIGS. 6(a) and 6(b) illustrate the shapes of shallow trench isolation structures manufactured in accordance with the above-identified method (including the step of forming the silicon nitride layer 210 shown in FIG. 10) in which the amount of the pad silicon nitride layer which is etched during the isotropic etching step is 100 Å and 300 Å, respectively. As can be seen from these Figures, the etching of the insulator at the corners of the shallow trench isolation structures by wet etching processes after formation of the shallow trench isolation structure is greater in the case of the 100 Å isotropic etch than in the case of the 300 Å isotropic etch. Thus, a pull-back of the pad silicon nitride layer by 300 Å provides greater protection for the corners of the shallow trench isolation than a pull-back of the pad silicon nitride layer by 100 Å. The larger the pulling-back of the pad silicon nitride layer, the longer the horizontal extensions of the "T-shape" of the structure of FIG. 5(g), and the greater the protection of the corners of the shallow trench isolation structure. However, since the etching of the pad silicon nitride layer is an isotropic etch, the larger the pulling-back, the thinner the remaining pad silicon nitride layer will be. As noted above, the remaining pad silicon nitride layer should have a thickness sufficient for serving as a stopper layer for the planarization process of FIG. 5(f).”

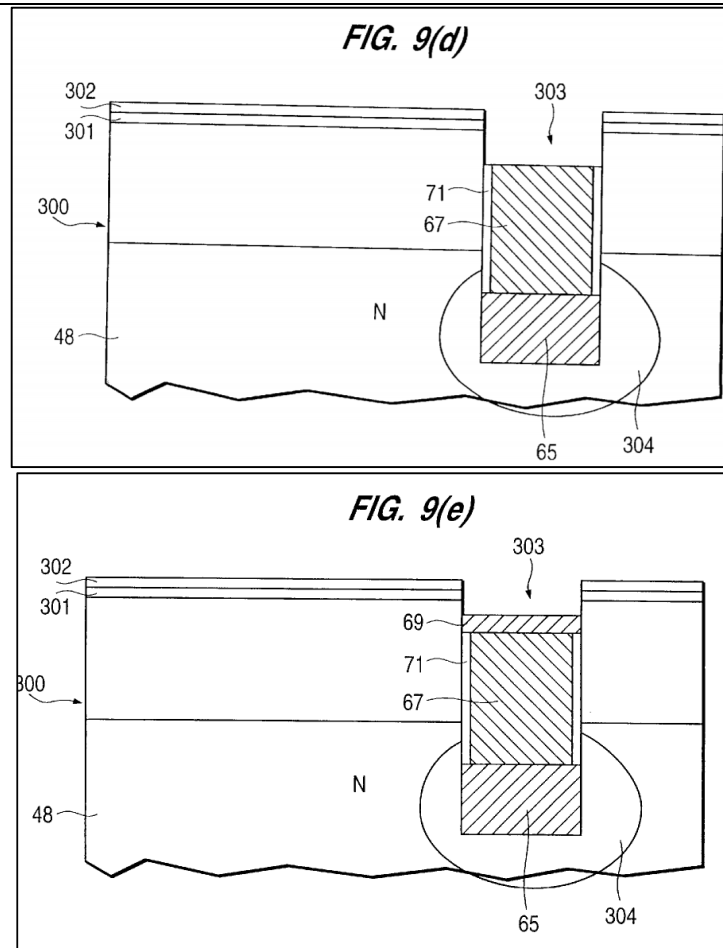


See, e.g., Saki at Figs. 6(a)-6(b).

“FIGS. 7(a)-7(h) are cross-sectional views illustrating a method for forming a shallow trench isolation structure in accordance with a second embodiment of the present invention. As shown in FIG. 7(a), a pad silicon dioxide (SiO<sub>2</sub>) layer 202 and a pad silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 204 are provided on a substrate 200. Silicon dioxide layer 202 has a thickness of about 80 Å-100 Å (e.g., 82 Å) and may be formed by thermal oxidation or by low pressure chemical vapor deposition (LPCVD), for example. Silicon nitride layer 204 has a thickness of about 1000 Å-

	<p>2000 Å (e.g., 1300 Å) and may be formed, for example, by LPCVD. Substrate 200 may be a silicon wafer or an epitaxial layer formed on a silicon wafer. A patterned photoresist (not shown) is then formed on pad silicon nitride layer 204. The pad silicon nitride layer, the pad silicon dioxide layer, and the substrate are then etched by, for example, reactive ion etching using the patterned photoresist as a mask to form a trench 206 as shown in FIG. 7(b). Pad silicon nitride layer 204 is then isotropically etched using, for example, HF/Glycerol or hot phosphoric acid. In accordance with the present embodiment, the amount of silicon nitride which is etched during this isotropic etching step is about 250 Å. Thus, the isotropic etch pulls back the pad silicon nitride layer by a distance <math>L=250</math> Å relative to the sidewall of trench 206, as shown in FIG. 7(c). A thin silicon dioxide (SiO<sub>2</sub>) layer 208 having a thickness of about 80Å-100Å is formed by a high temperature (for example, 1000° C.) thermal oxidation over the portions of the silicon substrate exposed by the forming of trench 206 as shown in FIG. 7(d). This high temperature oxidation removes substrate damage caused by the etching process for forming trench 206. Optionally, a thin silicon nitride layer (not shown) having a thickness of about 50 Å may then be deposited by, for example, CVD on pad silicon nitride layer 204 and on silicon dioxide layer 208. The silicon nitride layer may be provided, for example, in order to prevent oxidation of underlying layers during subsequent processing steps. As in the first embodiment, if the 50 Å silicon nitride layer is formed, the amount of silicon nitride which is etched during the isotropic etching step is about 300 Å. In this way, a composite silicon nitride layer is formed which is pulled back by about 250 Å from the sidewall of trench 206. Next, a silicon dioxide layer 212 is blanket deposited over the entire surface of the substrate using, for example, a CVD process in which TEOS (Si(OC<sub>2</sub>H<sub>5</sub>)<sub>4</sub>) is decomposed, as shown in FIG. 7(e). The silicon dioxide layer 212 is then planarized using, for example, RIE, chemical mechanical polishing, or a combination thereof as shown in FIG. 7(f). The pad silicon nitride layer 204 is then removed by, for example, chemical dry etching (CDE) or etching using hot phosphoric acid or HF/glycerol as shown in FIG. 7(g). One or more wet etching processes are then utilized to remove the pad silicon dioxide layer 202, as well as any sacrificial or dummy oxide layers which may be formed, resulting in the structure shown in FIG. 7(h). Because the pad silicon nitride layer was pulled-back by an isotropic etching process, the shallow trench isolation structure of FIG. 7(g) has a T-shape. In this way, subsequent wet etching processes for removing the pad silicon dioxide layer 202 and any sacrificial or dummy oxide layers attack these extensions of the shallow trench isolation structure and do not result in an etching away of</p>
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	<p>the insulator at the corner of the shallow trench isolation structure as can be seen with reference to FIG. 7(h).</p> <p>The same advantages which are obtained in the first embodiment are also obtained in the second embodiment.”</p> <p><i>See, e.g., Saki at 5:55-6:53; see also id. at Figs. 7(a)-(h).</i></p> <p>“A second conductive region is formed by filling in the remainder of trench 303 with a second conductive material. The second conductive material may be, for example, N<sup>+</sup> -type polycrystalline silicon or undoped polycrystalline silicon and may be formed by chemical vapor deposition (CVD). The second conductive material and the oxide collar 71 are then etched back to a second level within trench 303 to form second trench fill 67 which is insulated from the semiconductor substrate by collar oxide 71 as shown in FIG. 9(d). The depth of the buried strap to be formed in a subsequent process step is defined by this controlled etch-back of the second conductive material and collar oxide 71. Second trench fill 67 is etched back to about 0.1 micrometer below the surface of semiconductor substrate 300. An in-situ removal of a native oxide in trench 303 is then performed. In particular, the native oxide on the upper surface of second trench fill 67 and on the sidewall of trench 303 through which impurities for the buried strap will subsequently be outdiffused are removed. This removal of native oxide may be carried out by an in-situ prebake in a hydrogen ambient at a temperature greater than 850° C., for example.”</p> <p><i>See, e.g., Saki at 7:60-8:13.</i></p>
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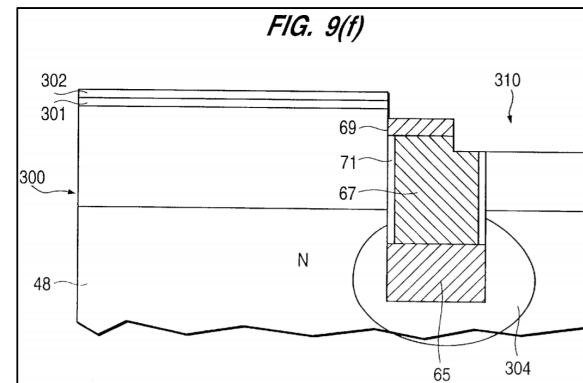
See, e.g., Saki at Fig. 9(d), (e); see also *id.* at 9(b)-(c), (f).

“The portion of trench 303 opened by the etching back of collar oxide 71 and the second conductive material is then filled by a third conductive material. The third conductive material may be, for example, undoped polycrystalline silicon deposited by chemical vapor deposition

	<p>(CVD). The polycrystalline silicon is then etched back using reactive ion etching, for example, to form a third trench fill 69 as shown in FIG. 9(e). The polycrystalline silicon is preferably etched back to about 0.05 micrometer below the surface of semiconductor substrate 300 as determined by the tolerable resistance of the buried strap, and by the recess etch controllability.</p> <p>With reference to FIG. 9(f), a shallow trench 310 is formed to provide for shallow trench isolation. As described above, shallow trench isolation is used to isolate discrete memory cell devices to prevent interference therebetween. In particular, a shallow trench is formed as described above with respect to FIGS. 5(a)-5(i) or FIGS. 7(a)-7(h). Thus, for example, the trench 310 may be etched using a patterned photoresist formed on the pad silicon nitride layer 302 as a mask. The pad silicon nitride layer 302 is then isotropically etched to remove about 300 Å. The trench sidewall is then oxidized to form an oxide layer 320 having a thickness of about 100 Å and a silicon nitride layer 322 having a thickness of about 50 Å is then deposited. The oxide and nitride linings serve to isolate collar oxide 71 from oxidant, and thereby suppress dislocation and stress. The trench is then filled with an insulator 324 such as silicon dioxide and the trench fill is then planarized using chemical mechanical polishing (CMP) and/or reactive ion etching (RIE). The pad silicon nitride layer is then stripped by chemical dry etching (CDE) or hot phosphoric acid and the pad oxide is then removed using a wet etch for removing, for example, 200 Å of silicon dioxide. At this time, the silicon dioxide in the trench is also etched. A sacrificial silicon dioxide layer having a thickness of about 100 Å is then formed on the surface of the substrate 300 and impurities may be implanted in what will become the channel regions of the transfer gates in order to control the threshold voltages thereof. The sacrificial oxide is then removed by etching away 120 Å of silicon dioxide.</p> <p>A gate insulator may then be formed on the planar surface, and gate material may be deposited and patterned to form gate electrodes. Using the gate electrodes as masks, source/drain regions may be formed by ion implantation. Accordingly, transfer gates coupled to trench capacitors are realized. Interconnection between devices and metallization to the output terminals are conducted using techniques known in the art. During the complete DRAM fabrication process, impurities from the conductive regions within the trench are outdiffused to form strap portion 83.</p>
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In accordance with the above process, the corner portions of the shallow trench isolation structure are protected from etching during the memory cell fabrication process such that these corner portions are substantially level with the surface portion of said semiconductor substrate and the upper surface portion of the insulator 324 filling the shallow trench as shown in FIG. 9(g).”

See, e.g., Saki at 8:14-9:4.



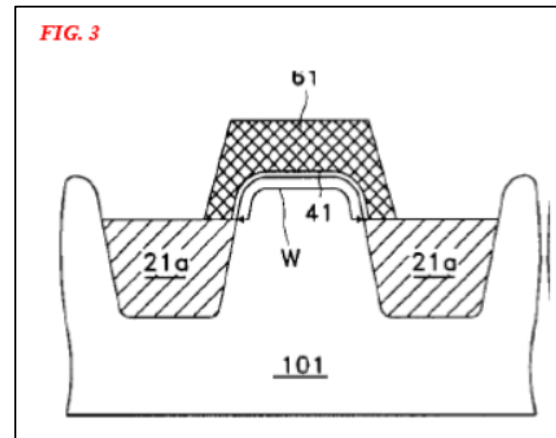
See, e.g., Saki at Fig. 9(f).

**In the event it is determined that Saki does not disclose this element, it would have been obvious to modify Saki to include this element based either on the knowledge of a person of skill in the art and/or the teaching of other references. For example, Yun teaches this element:**

“FIG. 3 is a vertical cross-sectional view illustrating a transistor according to one embodiment of the present invention. With reference to FIG. 3, isolation regions 21a are formed on a silicon substrate 101 and gates are formed between the isolation regions 21a. Here, a gate oxide film 41 is formed on the area where the silicon substrate is higher by a predetermined height relative to the upper part of the isolation region 21a; and a gate electrode 61 is formed on the upper part thereof. Accordingly, the channel width is raised by a predetermined height relative to the

isolation region 21a and for a curve by as much as the height, thereby increasing the channel width. In doing so, there will not be any change in the chip area.”

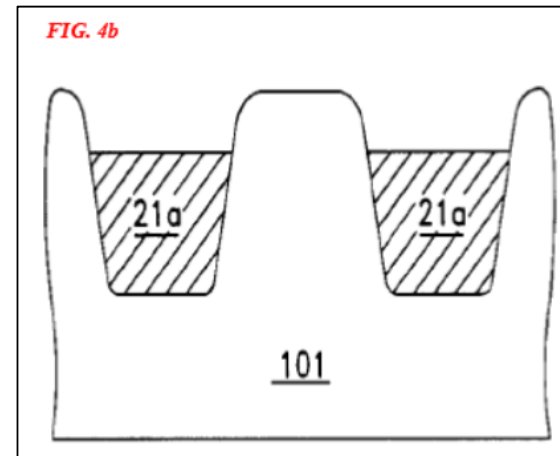
See, e.g., Yun at pg. 2.



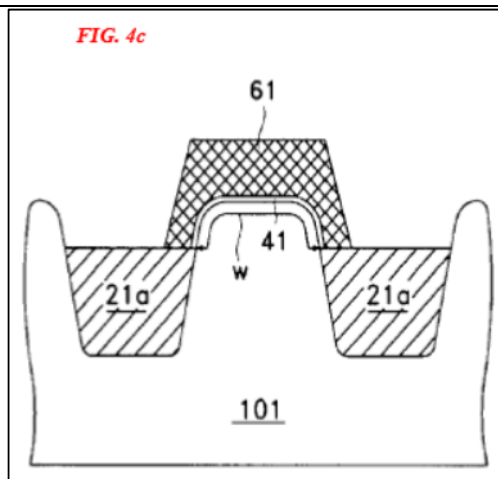
See, e.g., Yun at Fig. 3.

“FIGS. 4a to 4c are the cross-sectional views of the fabrication process, and as such they illustrate the sequence of manufacturing a transistor according to one embodiment of the present invention. With reference to FIG. 4a, a trench isolation region 21 is formed on a silicon substrate 101 by means of a conventional trench isolation process and a well region is formed on a conventional Local Implantation on Field LIF process. With reference to FIG. 4b, the oxide film 21a inside the trench isolation in the region desired to increase the channel width is etched by 10nm - 200nm by means of a wet etching process. Also, the sacrificial oxide film is sacrificed by 10nm - 30nm to allow the channel region in the angular part to become a more curved surface, thereby increasing the channel width W. Then, ion implantation to optimize the threshold voltage of the transistor is performed for  $3.0 \times 10^{11}/\text{cm}^2$  -  $2.0 \times 10^{12}/\text{cm}^2$  and, after that, the sacrificial film is etched by wet etching. Accordingly, it is shown that the oxide film 21a filled in the isolation region is formed underneath the silicon substrate 101. With reference

to FIG. 4c, after the process described above is performed, a transistor is formed by means of a gate oxide 41 formation process and a source and drain formation process.”  
*See, e.g., Yun at pg. 2.*



*See, e.g., Yun at Fig. 4b.*



See, e.g., Yun at Fig. 4c.

**Furthermore, this element is obvious based on the knowledge of a person of ordinary skill in the art.**

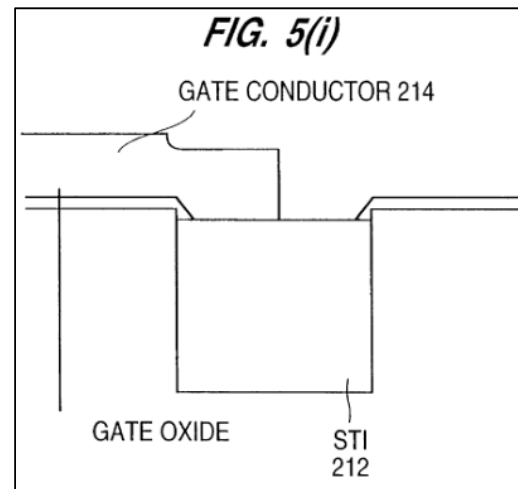
A person of ordinary skill in the art would have been motivated to incorporate this element from Yun or their own knowledge into Saki to obtain stable isolation characteristics, “the present invention described above has an effect of increasing the channel width of a transistor without increasing the chip area and obtaining stable isolation characteristics by adjusting the trench depth as a result thereof.” See, e.g. Yun at pg. 2. A person of ordinary skill in the art would have a reasonable expectation of success in incorporating this limitation as the mechanisms for doing so are disclosed in references themselves. See, e.g., Saki at 1:19-24. (“Shallow trench isolation is particularly advantageous for circuits having a high integration density since shallow trench isolation can provide for a relatively planar surface on which subsequent insulating and/or conducting layers may be formed.”)

In addition to being a combination taught directly by these references, such a combination would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain

	<p>predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.</p>
<p>[1c](i) a gate electrode and a gate insulation layer formed above said substrate,...</p>	<p><b>Saki discloses a gate electrode and a gate insulation layer formed above said substrate. By way of non-limiting example, Saki discloses:</b></p> <p>“A conventional process for forming a shallow trench isolation (STI) structure is shown in FIGS. 1(a)-1(f). A silicon dioxide (SiO<sub>2</sub>) layer 102 and a silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 104 are successively formed on the surface of a silicon substrate 100 as shown in FIG. 1(a). A patterned resist (not shown) is formed on the upper surface of silicon nitride layer 104 and an etching process such as reactive ion etching (RIE) is used to form trenches 106 in silicon substrate 100 as shown in FIG. 1(b). A thermal oxidation process is then performed to form a thermal silicon dioxide (SiO<sub>2</sub>) layer 108 on the exposed surfaces of the silicon substrate 100 as shown in FIG. 1(c). A silicon dioxide (SiO<sub>2</sub>) layer 110 is then deposited by the decomposition of TEOS, for example, to fill in trenches 106 as shown in FIG. 1(d). The silicon dioxide layer 110 is then planarized by chemical mechanical polishing (CMP), for example, as shown in FIG. 1(e). Silicon nitride layer 104 serves as a stopper layer for the planarization process. Silicon nitride layer 104 is then removed. Various wet etching processes are used in subsequent manufacturing steps to remove the silicon dioxide layer 102, as well as to remove any sacrificial or dummy silicon dioxide layers which may be formed after removal of the silicon nitride layer. Such sacrificial silicon dioxide layers may be formed to clean the substrate surface prior to growing a gate oxide layer or to repair substrate damage due, for example, to implantation processes (e.g., channel implantation processes for controlling a threshold voltage of a transistor). However, these wet etching processes cause an etching away of the silicon dioxide at the corner 112 of the shallow trench isolation structure as shown in FIG. 1(f). This etching away of the silicon dioxide at the corner of the shallow trench isolation structure is shown in more detail in FIG. 2 and can result in a lowering of the threshold voltage of a transistor formed in the active area defined by the shallow trench isolation structure.</p> <p>One technique of protecting the corner of a shallow trench isolation structure is described in U.S. Pat. No. 5,521,422 to Mandelman et al. In one embodiment of the Mandelman et al. process shown in FIGS. 3(a)-3(f), a pad oxide 10 and a nitride surface coating 12 are</p>

	<p>successively formed on the surface of a silicon substrate 5. The nitride surface coating 12 is then etched to form an opening 14 as shown in FIG. 3(a). Next, an insulator 16 such as a CVD oxide is deposited as shown in FIG. 3(b) and layer 16 and layer 10 are then etched as shown in FIG. 3(c) to leave spacers 16a and 16b on the sidewalls of the nitride surface coating. A trench 18, defined by the spacers 16a and 16b, is then formed in the silicon substrate 5 as shown in FIG. 3(d). An insulator 20 is deposited to fill trench 18 and opening 14. Insulator 20 is then planarized, stopping on nitride surface coating 12. Nitride surface coating 12 is then removed, leaving insulator 20 with spacers 16a and 16b extending above the surface of silicon substrate 5 as shown in FIG. 3(e). Subsequently, pad oxide 10 is etched and a gate dielectric 22 is formed. A gate conductor 24 is then deposited and photolithographically defined as shown in FIG. 3(f).” <i>See, e.g., Saki at 1:25-2:13, Figs. 3(a)-(f).</i></p> <p>“In addition, as can be seen in FIG. 3(f), insulator 20 and sidewall spacers 16a and 16b extend above the surface of silicon substrate 5. A step is formed inevitably on the gate electrode 24 since there is a difference in level created between the surface of silicon substrate 5 and the insulator 20. This can lead to difficulties in the patterning of the gate conductor 24, particularly in highly integrated devices such as 64 Mbit and 256 Mbit dynamic random access memories (DRAMs).” <i>See, e.g., Saki at 2:41-50.</i></p> <p>“Thus, in accordance with the above-described method of the present invention, etching of the insulator at the corner of the shallow trench isolation structure is suppressed and problems due to changes in the threshold voltages of elements formed in the active area defined by the shallow trench isolation structure can be minimized. As discussed with respect to FIG. 4, the degree to which the corner of the structure is protected is determined by the length "L". In accordance with the present invention, this length "L" is determined by the isotropic etching of the pad silicon nitride layer. Since, in accordance with the present invention, only a single process factor affects the length "L", enhanced controllability of the shape of the shallow trench isolation structure can be achieved and therefore fluctuations in device characteristics can be reduced. In addition, because an upper surface of the shallow trench isolation structure and the surface of the substrate are substantially level, no step is created between the shallow trench isolation structure and a subsequently formed gate conductor 214 as shown in FIG. 5(i). Thus, patterning of the gate electrode is simplified. Still further, the method of the present invention</p>
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has a small number of steps and therefore contributes to ease of device manufacture and reduced manufacturing costs.”  
*See, e.g., Saki at 5:7-30.*



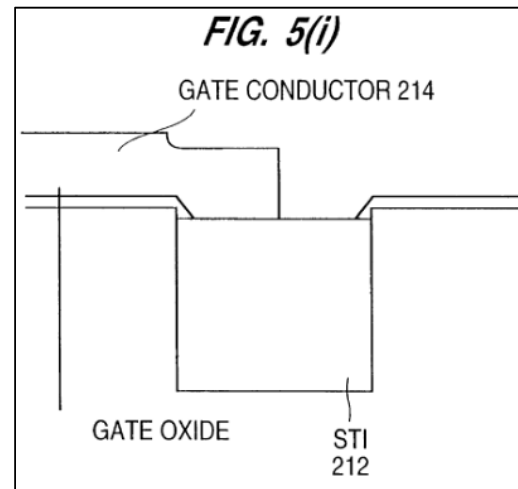
*See, e.g., Saki at Fig. 5(i).*

“FIGS. 8(a) and 8(b) illustrate a trench DRAM cell with a self-aligned buried strap which is isolated from other cells by a shallow trench isolation structure in accordance with the present invention. Specifically, FIG. 8(a) is a top-down view of the trench DRAM cell and FIG. 8(b) is a cross-sectional view taken along line A-A' of FIG. 8(a). DRAM cell 50 includes a trench capacitor 55 and a transfer gate 60. Trench capacitor 55 includes a first N<sup>+</sup> -type polycrystalline silicon fill 65, a second polycrystalline silicon fill 67, and a collar oxide 71. Transfer gate 60 includes N-type source/drain and drain/source regions 73 and 74 formed in P-type well 75 and a WSix /polycrystalline silicon gate 77 insulatively spaced from the channel region between source/drain region 73 and drain/source region 74. A bit line contact 79 formed in an opening in an insulating layer 80 (of BPSG, for example) electrically connects source/drain region 73 to bit line 81. A shallow trench isolation structure formed in accordance with the present invention electrically isolates DRAM cell 50 from an adjacent DRAM cell and passing word line 92. Passing word line 92 has a WSix /polycrystalline silicon structure. A dielectric layer 87 is

	<p>formed on bit line 81 and aluminum wirings 89 are formed on dielectric layer 87. One of the aluminum wirings 89 is connected to bit line 81 by a contact stud 91 of tungsten, for example. A diffusion region 83 electrically connects third polycrystalline silicon fill 69 and drain/source region 74 of MOS transfer gate 60. This diffusion region is formed by outdiffusing dopants from the highly doped polycrystalline silicon fill in the storage trench into P-well 75. Diffusion region 83 and third polycrystalline silicon fill 69 constitute a buried strap for connecting trench capacitor 55 to transfer gate 60.”</p> <p><i>See, e.g., Saki at 6:54-7:18, Figs. 8(a)-(b).</i></p> <p>“A gate insulator may then be formed on the planar surface, and gate material may be deposited and patterned to form gate electrodes. Using the gate electrodes as masks, source/drain regions may be formed by ion implantation. Accordingly, transfer gates coupled to trench capacitors are realized. Interconnection between devices and metallization to the output terminals are conducted using techniques known in the art. During the complete DRAM fabrication process, impurities from the conductive regions within the trench are outdiffused to form strap portion 83.”</p> <p><i>See, e.g., Saki at 8:55-64, Figs. 9(f)-(g).</i></p>
[1c](ii) ...a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure; and	<p><b>Saki discloses a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure. By way of non-limiting example, Saki discloses:</b></p> <p><i>See disclosure for claim 1(c)(i). This disclosure is incorporated by reference herein. By way of further non-limiting example:</i></p> <p>“Thus, in accordance with the above-described method of the present invention, etching of the insulator at the corner of the shallow trench isolation structure is suppressed and problems due to changes in the threshold voltages of elements formed in the active area defined by the shallow trench isolation structure can be minimized. As discussed with respect to FIG. 4, the degree to which the corner of the structure is protected is determined by the length "L". In accordance with the present invention, this length "L" is determined by the isotropic etching of the pad silicon nitride layer. Since, in accordance with the present invention, only a single process factor affects the length "L", enhanced controllability of the shape of the shallow trench</p>

isolation structure can be achieved and therefore fluctuations in device characteristics can be reduced. In addition, because an upper surface of the shallow trench isolation structure and the surface of the substrate are substantially level, no step is created between the shallow trench isolation structure and a subsequently formed gate conductor 214 as shown in FIG. 5(i). Thus, patterning of the gate electrode is simplified. Still further, the method of the present invention has a small number of steps and therefore contributes to ease of device manufacture and reduced manufacturing costs.”

*See, e.g., Saki at 5:7-30.*



*See, e.g., Saki at Fig. 5(i); see also id. at Figs. 5(a)-(h).*

“Subsequently, pad oxide 10 is etched and a gate dielectric 22 is formed. A gate conductor 24 is then deposited and photolithographically defined as shown in FIG. 3(f).”

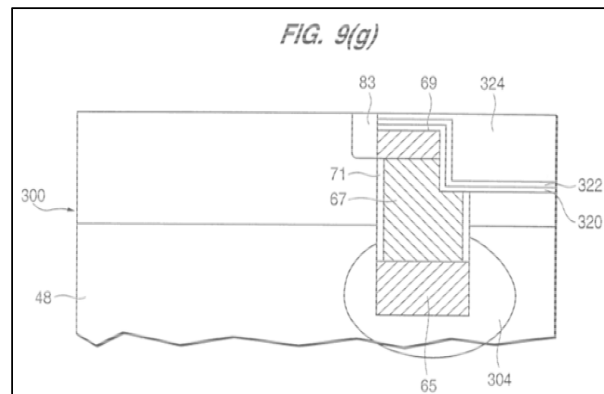
*See, e.g., Saki at 2:10-13; see also id. at Fig. 3(f).*

“A gate insulator may then be formed on the planar surface, and gate material may be deposited and patterned to form gate electrodes. Using the gate electrodes as masks, source/drain regions may be formed by ion implantation. Accordingly, transfer gates coupled to trench capacitors are realized. Interconnection between devices and metallization to the output terminals are

conducted using techniques known in the art. During the complete DRAM fabrication process, impurities from the conductive regions within the trench are outdiffused to form strap portion 83.

In accordance with the above process, the corner portions of the shallow trench isolation structure are protected from etching during the memory cell fabrication process such that these corner portions are substantially level with the surface portion of said semiconductor substrate and the upper surface portion of the insulator 324 filling the shallow trench as shown in FIG. 9(g).”

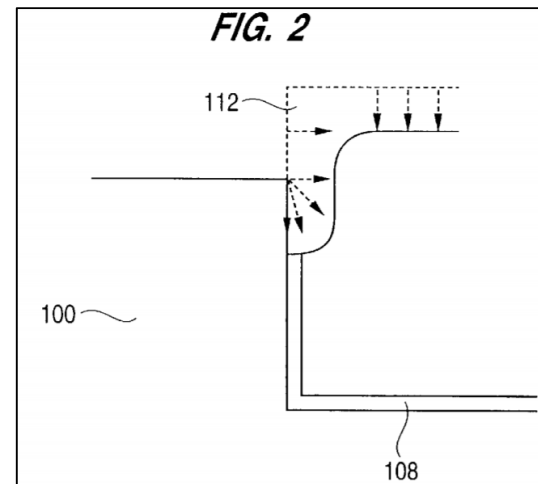
*See, e.g., Saki at 8:55-64.*



*See, e.g., Saki at Fig. 9(g); see also id. at Figs. 9(a)-(f).*

“A conventional process for forming a shallow trench isolation (STI) structure is shown in FIGS. 1(a)-1(f). A silicon dioxide ( $\text{SiO}_2$ ) layer 102 and a silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 104 are successively formed on the surface of a silicon substrate 100 as shown in FIG. 1(a). A patterned resist (not shown) is formed on the upper surface of silicon nitride layer 104 and an etching process such as reactive ion etching (RIE) is used to form trenches 106 in silicon substrate 100 as shown in FIG. 1(b). A thermal oxidation process is then performed to form a thermal silicon dioxide ( $\text{SiO}_2$ ) layer 108 on the exposed surfaces of the silicon substrate 100 as shown in FIG. 1(c). A silicon dioxide ( $\text{SiO}_2$ ) layer 110 is then deposited by the decomposition of TEOS, for

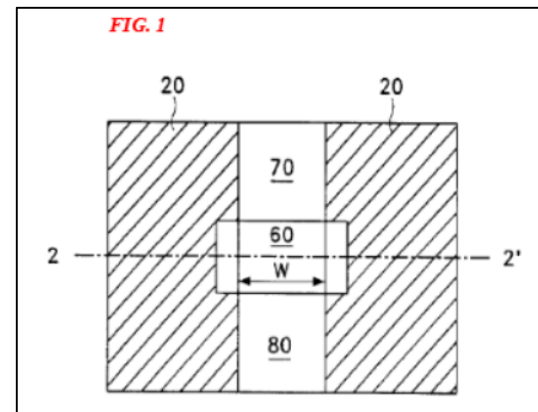
example, to fill in trenches 106 as shown in FIG. 1(d). The silicon dioxide layer 110 is then planarized by chemical mechanical polishing (CMP), for example, as shown in FIG. 1(e). Silicon nitride layer 104 serves as a stopper layer for the planarization process. Silicon nitride layer 104 is then removed. Various wet etching processes are used in subsequent manufacturing steps to remove the silicon dioxide layer 102, as well as to remove any sacrificial or dummy silicon dioxide layers which may be formed after removal of the silicon nitride layer. Such sacrificial silicon dioxide layers may be formed to clean the substrate surface prior to growing a gate oxide layer or to repair substrate damage due, for example, to implantation processes (e.g., channel implantation processes for controlling a threshold voltage of a transistor). However, these wet etching processes cause an etching away of the silicon dioxide at the corner 112 of the shallow trench isolation structure as shown in FIG. 1(f). This etching away of the silicon dioxide at the corner of the shallow trench isolation structure is shown in more detail in FIG. 2 and can result in a lowering of the threshold voltage of a transistor formed in the active area defined by the shallow trench isolation structure.”  
*See, e.g., Saki at 1:25-59.*



*See, e.g., Saki at Fig. 2.*

	<p><b>In the event it is determined that Saki does not disclose this element, it would have been obvious to modify Saki to include this element based either on the knowledge of a person of skill in the art and/or the teaching of other references. For example, Yun teaches this element:</b></p> <p>“FIG. 1 is a plan view of a transistor according to the prior art. With reference to FIG. 1, it illustrates a plan view comprising an isolation region 20, a source 20 [sic] and a drain 80 of a transistor, and a gate 60 between the source 20 and the drain 80. Here, the width W of the channel formed at the lower part of the gate 60 is formed with the same width as that of the source 70 and the drain 80. Here, the width W of the channel formed at the lower part of the gate 60 is formed with the same width as that of the source 70 and the drain 80. Also, an increase in the channel width immediately results in an increase in the chip area. On another note, a vertical cross-sectional view in the 2-2' direction of FIG. 1 is shown in FIG. 2. With reference to FIG. 2, it comprises: a channel region W directly formed on a silicon substrate 100 or formed inside a well formed on a silicon substrate 100; an isolation region 20 for isolating the device; a gate oxide film 40 formed on top of channel width W; and a gate electrode 60 formed thereon. When formed in a structure like this, a transistor is positioned on a surface that runs in parallel with the silicon substrate 100 and, when the channel width W is increased to increase the current-driving amount of a transistor, it immediately results in an increase in the size of the area. Since increasing the channel width immediately results in an increase in the size of the area, Patent No. 5,115,289 registered in the U.S. presents, as disclosed therein, a transistor structure to increase the channel width without increasing the area by vertically forming a part of the channel width to thereby solve the problem that made it difficult to increase the channel width. Although not illustrated, a manufacturing method to form such a transistor will now be briefly described here. After etching a silicon substrate with the width of 0.1μm and depth of 1μm, the area where a channel will be formed is formed in such a way as to be wrapped up with a silicon oxide film SiO<sub>2</sub> and a silicon nitride film SiN. Next, after isolating the channel region from the substrate by means of an oxidation process, the silicon nitride film and the silicon oxide film are removed; and the gate oxide film and the gate are formed. Then, a transistor is manufactured by means of a conventional transistor formation process such as forming a drain and a source, etc. Since the channel region is isolated from the silicon substrate by adopting a process of Silicon-On-Insulator (“SOI”), as described earlier, the channel region must be completely isolated from the substrate by “bird’s beak” during the</p>
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oxidation process to form SOI. Accordingly, all the channel widths must be  $0.1\mu\text{m}$ . Consequently, it becomes difficult to form a large-size pattern. Also, even though all the patterns are formed at  $0.1\mu\text{m}$  or less, it causes a problem, among others, that the channel region is lifted during the oxidation process. In addition, a process of wrapping the channel region with a silicon nitride film is required to prevent oxidation of the channel region during the oxidation process for SOI, which causes a problem that the process becomes complicated.”  
*See, e.g., Yun at pgs. 1-2.*

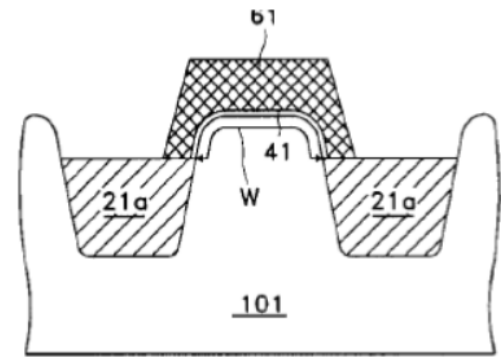


*See, e.g., Yun at Fig. 1.*

“FIG. 3 is a vertical cross-sectional view illustrating a transistor according to one embodiment of the present invention. With reference to FIG. 3, isolation regions 21a are formed on a silicon substrate 101 and gates are formed between the isolation regions 21a. Here, a gate oxide film 41 is formed on the area where the silicon substrate is higher by a predetermined height relative to the upper part of the isolation region 21a; and a gate electrode 61 is formed on the upper part thereof. Accordingly, the channel width is raised by a predetermined height relative to the isolation region 21a and for a curve by as much as the height, thereby increasing the channel width. In doing so, there will not be any change in the chip area.”

*See, e.g., Yun at pg. 2.*

**FIG. 3**

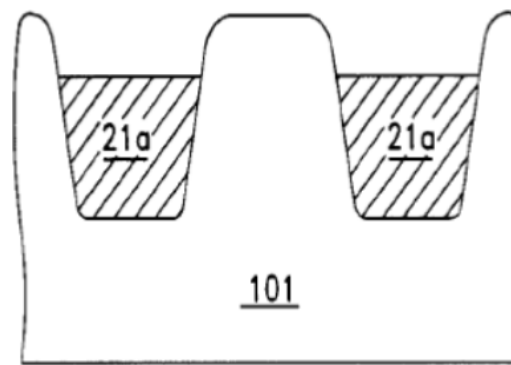


See, e.g., Yun at Fig. 3.

“FIGS. 4a to 4c are the cross-sectional views of the fabrication process, and as such they illustrate the sequence of manufacturing a transistor according to one embodiment of the present invention. With reference to FIG. 4a, a trench isolation region 21 is formed on a silicon substrate 101 by means of a conventional trench isolation process and a well region is formed on a conventional Local Implantation on Field LIF process. With reference to FIG. 4b, the oxide film 21a inside the trench isolation in the region desired to increase the channel width is etched by 10nm - 200nm by means of a wet etching process. Also, the sacrificial oxide film is sacrificed by 10nm - 30nm to allow the channel region in the angular part to become a more curved surface, thereby increasing the channel width W. Then, ion implantation to optimize the threshold voltage of the transistor is performed for  $3.0 \times 10^{11}/\text{cm}^2$  -  $2.0 \times 10^{12}/\text{cm}^2$  and, after that, the sacrificial film is etched by wet etching. Accordingly, it is shown that the oxide film 21a filled in the isolation region is formed underneath the silicon substrate 101. With reference to FIG. 4c, after the process described above is performed, a transistor is formed by means of a gate oxide 41 formation process and a source and drain formation process.”

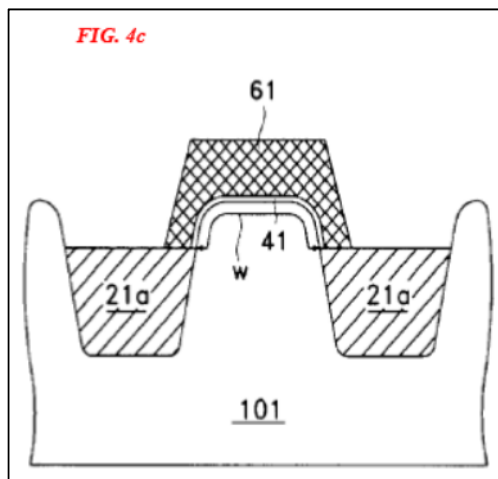
See, e.g., Yun at pg. 2.

**FIG. 4b**



*See, e.g., Yun at Fig. 4b.*

**FIG. 4c**



*See, e.g., Yun at Fig. 4c.*

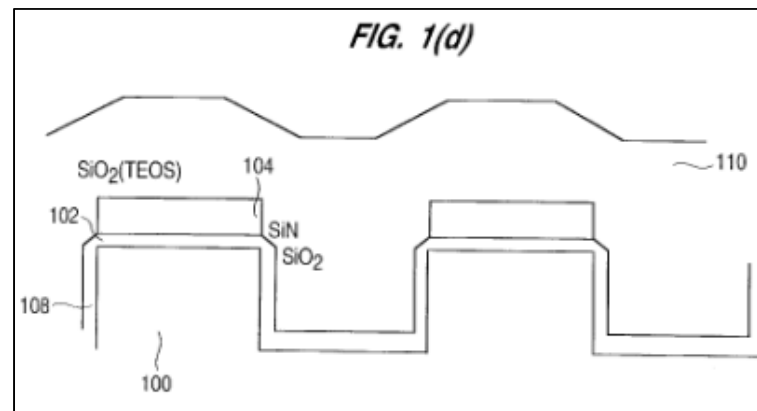
	<p><b>Furthermore, this element is obvious based on the knowledge of a person of ordinary skill in the art.</b></p> <p>A person of ordinary skill in the art would have been motivated to incorporate this element from Yun or their own knowledge into Saki to obtain stable isolation characteristics, “the present invention described above has an effect of increasing the channel width of a transistor without increasing the chip area and obtaining stable isolation characteristics by adjusting the trench depth as a result thereof.” <i>See, e.g.</i> Yun at pg. 2. A person of ordinary skill in the art would have a reasonable expectation of success in incorporating this limitation as the mechanisms for doing so are disclosed in references themselves. <i>See, e.g.</i>, Saki at 1:19-24. (“Shallow trench isolation is particularly advantageous for circuits having a high integration density since shallow trench isolation can provide for a relatively planar surface on which subsequent insulating and/or conducting layers may be formed.”)</p> <p>In addition to being a combination taught directly by these references, such a combination would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.</p>
[1d] a source region and a drain region formed in said substrate.	<p><b>Saki discloses a source region and a drain region formed in said substrate. By way of non-limiting example, Saki discloses:</b></p> <p>“An integrated circuit may be formed by connecting together various elements such as transistors which are formed on a semiconductor substrate. To ensure proper functioning of the integrated circuit, these elements must be electrically isolated from each other. Such isolation can be achieved using local oxidation of silicon (LOCOS) or shallow trench isolation (STI). Shallow trench isolation is particularly advantageous for circuits having a high integration density since shallow trench isolation can provide for a relatively planar surface on which subsequent insulating and/or conducting layers may be formed.</p>

	<p>A conventional process for forming a shallow trench isolation (STI) structure is shown in FIGS. 1(a)-1(f). A silicon dioxide (SiO<sub>2</sub>) layer 102 and a silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 104 are successively formed on the surface of a silicon substrate 100 as shown in FIG. 1(a). A patterned resist (not shown) is formed on the upper surface of silicon nitride layer 104 and an etching process such as reactive ion etching (RIE) is used to form trenches 106 in silicon substrate 100 as shown in FIG. 1(b). A thermal oxidation process is then performed to form a thermal silicon dioxide (SiO<sub>2</sub>) layer 108 on the exposed surfaces of the silicon substrate 100 as shown in FIG. 1(c). A silicon dioxide (SiO<sub>2</sub>) layer 110 is then deposited by the decomposition of TEOS, for example, to fill in trenches 106 as shown in FIG. 1(d). The silicon dioxide layer 110 is then planarized by chemical mechanical polishing (CMP), for example, as shown in FIG. 1(e). Silicon nitride layer 104 serves as a stopper layer for the planarization process. Silicon nitride layer 104 is then removed. Various wet etching processes are used in subsequent manufacturing steps to remove the silicon dioxide layer 102, as well as to remove any sacrificial or dummy silicon dioxide layers which may be formed after removal of the silicon nitride layer. Such sacrificial silicon dioxide layers may be formed to clean the substrate surface prior to growing a gate oxide layer or to repair substrate damage due, for example, to implantation processes (e.g., channel implantation processes for controlling a threshold voltage of a transistor). However, these wet etching processes cause an etching away of the silicon dioxide at the corner 112 of the shallow trench isolation structure as shown in FIG. 1(f). This etching away of the silicon dioxide at the corner of the shallow trench isolation structure is shown in more detail in FIG. 2 and can result in a lowering of the threshold voltage of a transistor formed in the active area defined by the shallow trench isolation structure.”</p> <p><i>See, e.g., Saki at 1:14-59.</i></p> <p>“FIGS. 8(a) and 8(b) illustrate a trench DRAM cell with a self-aligned buried strap which is isolated from other cells by a shallow trench isolation structure in accordance with the present invention. Specifically, FIG. 8(a) is a top-down view of the trench DRAM cell and FIG. 8(b) is a cross-sectional view taken along line A-A' of FIG. 8(a). DRAM cell 50 includes a trench capacitor 55 and a transfer gate 60. Trench capacitor 55 includes a first N<sup>+</sup>-type polycrystalline silicon fill 65, a second polycrystalline silicon fill 67, and a collar oxide 71. Transfer gate 60 includes N-type source/drain and drain/source regions 73 and 74 formed in P-type well 75 and a WSix /polycrystalline silicon gate 77 insulatively spaced from the channel region between source/drain region 73 and drain/source region 74. A bit line contact 79 formed in an opening in</p>
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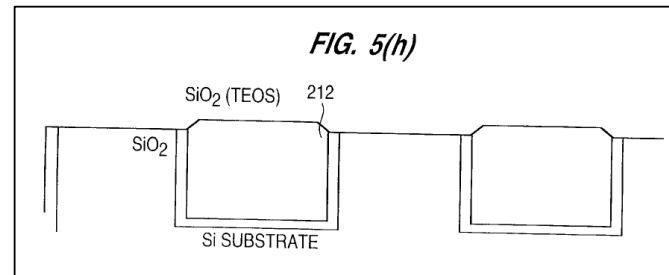
	<p>“A gate insulator may then be formed on the planar surface, and gate material may be deposited and patterned to form gate electrodes. Using the gate electrodes as masks, source/drain regions may be formed by ion implantation. Accordingly, transfer gates coupled to trench capacitors are realized. Interconnection between devices and metallization to the output terminals are conducted using techniques known in the art. During the complete DRAM fabrication process, impurities from the conductive regions within the trench are outdiffused to form strap portion 83.</p> <p>In accordance with the above process, the corner portions of the shallow trench isolation structure are protected from etching during the memory cell fabrication process such that these corner portions are substantially level with the surface portion of said semiconductor substrate and the upper surface portion of the insulator 324 filling the shallow trench as shown in FIG. 9(g).”</p> <p><i>See, e.g., Saki at 8:55-64.</i></p>
[2] The transistor of claim 1, wherein said semiconducting substrate is comprised of silicon.	<p><b>Saki discloses the transistor of claim 1, wherein said semiconducting substrate is comprised of silicon. By way of non-limiting example, Saki discloses:</b></p> <p><i>See disclosure for claim 1(a). This disclosure is incorporated by reference herein.</i></p>
[3] The transistor of claim 1, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.	<p><b>Saki discloses the transistor of claim 1, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride. By way of non-limiting example, Saki discloses:</b></p> <p><i>See disclosure for claim 1(b). This disclosure is incorporated by reference herein. By way of further example:</i></p> <p>“A conventional process for forming a shallow trench isolation (STI) structure is shown in FIGS. 1(a)-1(f). A silicon dioxide (SiO<sub>2</sub>) layer 102 and a silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 104 are successively formed on the surface of a silicon substrate 100 as shown in FIG. 1(a). A patterned resist (not shown) is formed on the upper surface of silicon nitride layer 104 and an etching process such as reactive ion etching (RIE) is used to form trenches 106 in silicon substrate 100</p>

as shown in FIG. 1(b). A thermal oxidation process is then performed to form a thermal silicon dioxide ( $\text{SiO}_2$ ) layer 108 on the exposed surfaces of the silicon substrate 100 as shown in FIG. 1(c). A silicon dioxide ( $\text{SiO}_2$ ) layer 110 is then deposited by the decomposition of TEOS, for example, to fill in trenches 106 as shown in FIG. 1(d). The silicon dioxide layer 110 is then planarized by chemical mechanical polishing (CMP), for example, as shown in FIG. 1(e). Silicon nitride layer 104 serves as a stopper layer for the planarization process. Silicon nitride layer 104 is then removed. Various wet etching processes are used in subsequent manufacturing steps to remove the silicon dioxide layer 102, as well as to remove any sacrificial or dummy silicon dioxide layers which may be formed after removal of the silicon nitride layer. Such sacrificial silicon dioxide layers may be formed to clean the substrate surface prior to growing a gate oxide layer or to repair substrate damage due, for example, to implantation processes (e.g., channel implantation processes for controlling a threshold voltage of a transistor). However, these wet etching processes cause an etching away of the silicon dioxide at the corner 112 of the shallow trench isolation structure as shown in FIG. 1(f). This etching away of the silicon dioxide at the corner of the shallow trench isolation structure is shown in more detail in FIG. 2 and can result in a lowering of the threshold voltage of a transistor formed in the active area defined by the shallow trench isolation structure.”  
*See, e.g., Saki at 1:25-59.*



*See, e.g., Saki at Fig. 1(d); see also id. at Figs. 1(e)-1(f), Fig. 2.*

“A silicon dioxide layer 212 is then blanket deposited over the entire surface of the substrate using, for example, a CVD process in which TEOS ( $\text{Si}(\text{OC}_2\text{H}_5)_4$ ) is decomposed, as shown in FIG. 5(e). Other deposition techniques for depositing the silicon dioxide layer 212, such as a plasma CVD process using  $\text{O}_3$  and TEOS, may be utilized. The silicon dioxide layer 212 is then planarized using, for example, RIE, chemical mechanical polishing, or a combination thereof as shown in FIG. 5(f). The pad silicon nitride layer 204 is then removed by, for example, chemical dry etching (CDE), hot phosphoric acid or HF/Glycerol as shown in FIG. 5(g). One or more wet etching processes are then utilized to remove the pad silicon dioxide layer 202, as well as to remove any sacrificial or dummy oxides which may be formed, resulting in the structure shown in FIG. 5(h). Because pad silicon nitride layer 204 was pulled-back by an isotropic etching process, the shallow trench isolation structure of FIG. 5(g) has a T-shape. In this way, subsequent wet etching processes for removing the pad silicon dioxide layer 202 and any sacrificial or dummy oxide layers attack these extensions of the shallow trench isolation structure and do not result in an etching away of the insulator at the corner of the shallow trench isolation structure as can be seen with reference to FIG. 5(h).”  
*See, e.g., Saki at 4:51-5:7.*



*See, e.g., Saki at Fig. 5(h); see also Figs. 5(e)-(g), (i).*

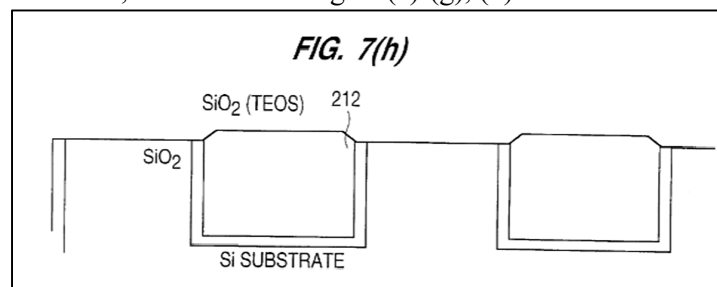
“FIGS. 7(a)-7(h) are cross-sectional views illustrating a method for forming a shallow trench isolation structure in accordance with a second embodiment of the present invention. As shown in FIG. 7(a), a pad silicon dioxide ( $\text{SiO}_2$ ) layer 202 and a pad silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 204 are provided on a substrate 200. Silicon dioxide layer 202 has a thickness of about 80 Å-100 Å (e.g., 82 Å) and may be formed by thermal oxidation or by low pressure chemical vapor deposition (LPCVD), for example. Silicon nitride layer 204 has a thickness of about 1000 Å-

	<p>2000 Å (e.g., 1300 Å) and may be formed, for example, by LPCVD. Substrate 200 may be a silicon wafer or an epitaxial layer formed on a silicon wafer. A patterned photoresist (not shown) is then formed on pad silicon nitride layer 204. The pad silicon nitride layer, the pad silicon dioxide layer, and the substrate are then etched by, for example, reactive ion etching using the patterned photoresist as a mask to form a trench 206 as shown in FIG. 7(b). Pad silicon nitride layer 204 is then isotropically etched using, for example, HF/Glycerol or hot phosphoric acid. In accordance with the present embodiment, the amount of silicon nitride which is etched during this isotropic etching step is about 250 Å. Thus, the isotropic etch pulls back the pad silicon nitride layer by a distance <math>L=250</math> Å relative to the sidewall of trench 206, as shown in FIG. 7(c). A thin silicon dioxide (SiO<sub>2</sub>) layer 208 having a thickness of about 80Å-100Å is formed by a high temperature (for example, 1000° C.) thermal oxidation over the portions of the silicon substrate exposed by the forming of trench 206 as shown in FIG. 7(d). This high temperature oxidation removes substrate damage caused by the etching process for forming trench 206. Optionally, a thin silicon nitride layer (not shown) having a thickness of about 50 Å may then be deposited by, for example, CVD on pad silicon nitride layer 204 and on silicon dioxide layer 208. The silicon nitride layer may be provided, for example, in order to prevent oxidation of underlying layers during subsequent processing steps. As in the first embodiment, if the 50 Å silicon nitride layer is formed, the amount of silicon nitride which is etched during the isotropic etching step is about 300 Å. In this way, a composite silicon nitride layer is formed which is pulled back by about 250 Å from the sidewall of trench 206. Next, a silicon dioxide layer 212 is blanket deposited over the entire surface of the substrate using, for example, a CVD process in which TEOS (Si(OC<sub>2</sub>H<sub>5</sub>)<sub>4</sub>) is decomposed, as shown in FIG. 7(e). The silicon dioxide layer 212 is then planarized using, for example, RIE, chemical mechanical polishing, or a combination thereof as shown in FIG. 7(f). The pad silicon nitride layer 204 is then removed by, for example, chemical dry etching (CDE) or etching using hot phosphoric acid or HF/glycerol as shown in FIG. 7(g). One or more wet etching processes are then utilized to remove the pad silicon dioxide layer 202, as well as any sacrificial or dummy oxide layers which may be formed, resulting in the structure shown in FIG. 7(h). Because the pad silicon nitride layer was pulled-back by an isotropic etching process, the shallow trench isolation structure of FIG. 7(g) has a T-shape. In this way, subsequent wet etching processes for removing the pad silicon dioxide layer 202 and any sacrificial or dummy oxide layers attack these extensions of the shallow trench isolation structure and do not result in an etching away of</p>
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the insulator at the corner of the shallow trench isolation structure as can be seen with reference to FIG. 7(h).

The same advantages which are obtained in the first embodiment are also obtained in the second embodiment.”

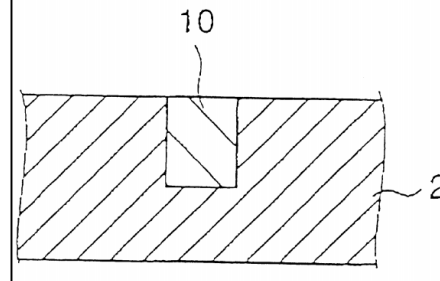
See, e.g., Saki at 5:55-6:53; see also *id.* at Figs. 7(a)-(g), (h):



“With reference to FIG. 9(f), a shallow trench 310 is formed to provide for shallow trench isolation. As described above, shallow trench isolation is used to isolate discrete memory cell devices to prevent interference therebetween. In particular, a shallow trench is formed as described above with respect to FIGS. 5(a)-5(i) or FIGS. 7(a)-7(h). Thus, for example, the trench 310 may be etched using a patterned photoresist formed on the pad silicon nitride layer 302 as a mask. The pad silicon nitride layer 302 is then isotropically etched to remove about 300 Å. The trench sidewall is then oxidized to form an oxide layer 320 having a thickness of about 100 Å and a silicon nitride layer 322 having a thickness of about 50 Å is then deposited. The oxide and nitride linings serve to isolate collar oxide 71 from oxidant, and thereby suppress dislocation and stress. The trench is then filled with an insulator 324 such as silicon dioxide and the trench fill is then planarized using chemical mechanical polishing (CMP) and/or reactive ion etching (RIE). The pad silicon nitride layer is then stripped by chemical dry etching (CDE) or hot phosphoric acid and the pad oxide is then removed using a wet etch for removing, for example, 200 Å of silicon dioxide. At this time, the silicon dioxide in the trench is also etched. A sacrificial silicon dioxide layer having a thickness of about 100 Å is then formed on the surface of the substrate 300 and impurities may be implanted in what will become the channel

	<p>regions of the transfer gates in order to control the threshold voltages thereof. The sacrificial oxide is then removed by etching away 120 Å of silicon dioxide.</p> <p><i>See, e.g., Saki at 8:26-54, Figs. 9(f)-9(g).</i></p>
<p>[5] The transistor of claim 1, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.</p>	<p><b>In the event it is determined that Saki does not disclose this element, it would have been obvious to modify Saki to include this element based either on the knowledge of a person of skill in the art and/or the teaching of other references. For example, Mitsuiki, Wada, or Perera teach this element:</b></p> <p>“A first embodiment according to the present invention will be described in detail with reference to the drawings. FIG. 4 is a fragmentary cross sectional elevation view illustrative of a shallow trench isolation in a shallow trench in a semiconductor substrate, wherein a shallow trench isolation is free of any divots, voids or cavities formed in a novel method of forming the shallow trench isolation structure in accordance with the present invention. A silicon substrate 2 has a shallow trench which has a width in the range of 0.1-1.0 micrometer and a depth in the range of 200-600 nanometers. A trench isolation oxide film 10 is filled within the shallow trench of the silicon substrate 2. The top of the trench isolation oxide film 10 and the top surface of the silicon substrate 2 are exactly planarized. The trench isolation oxide film 10 free of any divots and voids or cavities.”</p> <p><i>See, e.g., Mitsuiki at 3:51-65.</i></p>

FIG. 4

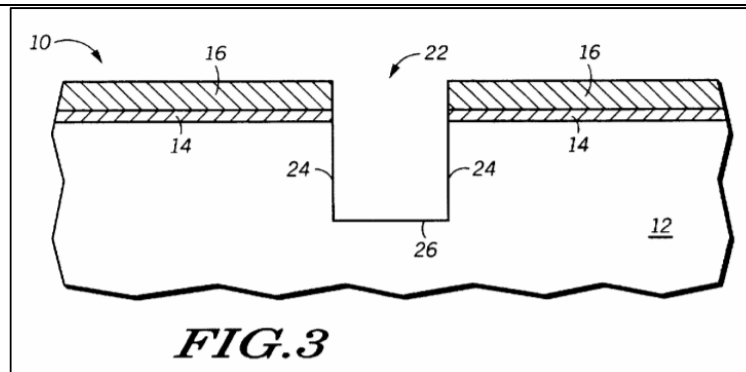


*See, e.g.,* Mitsuiki at Fig. 4.

**By way of further example, Perera also teaches this element:**

“In FIG. 3, first portion 20 of semiconductor substrate 12 is then anisotropically etched using standard etching techniques to form a trench 22 having a trench sidewall 24 and a trench bottom 26. After trench 22 has been formed, photoresist mask 18 is removed using standard photoresist stripping techniques. Trench 22 preferably has a trench width ranging from about 200 to 600 nanometers and a trench depth ranging from about 200 to 1000 nanometers.”

*See, e.g.,* Perera at 2:28-35; *see also id.* at 3:20-4:2.



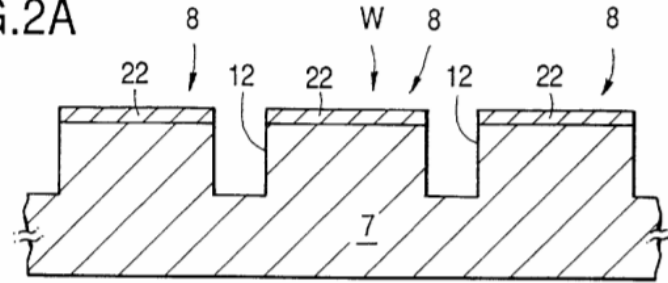
*See, e.g., Perera at Fig. 3; see also id. at Fig. 7.*

**As another example, Wada also teaches this element:**

“First, as shown in FIG. 2A, the cavities for the trenches 12 are fabricated on the upper surface of a wafer W (includes a substrate 7 of a P-type monocrystalline silicon having a specific resistance  $3\sim 4\text{ ohm}\cdot\text{cm}$ ) by process of etching through an etching mask of a  $\text{SiO}_2$  film 22, for protecting those active regions 8 for fabricating the N-channel MOS transistor but exposing those regions for forming the trenches 12. The process of forming the trenches 12 used in this embodiment is a dry etching process using gaseous chlorine to make a cavity measuring  $0.5\sim 1.5\text{ }\mu\text{m}$  in depth and  $0.2\sim 0.5\text{ }\mu\text{m}$  in width.”

*See, e.g., Wada at 4:41-51.*

FIG.2A



*See, e.g., Wada at Fig. 2A; see also id. at Fig. 6A.*

“The dimensions quoted in the embodiments are meant to be examples, and they are not limited to the exact dimensions quoted. For example, it is permissible to have a range of dimensions such as: the trench widths may range from 80 nm~several mm; the depth of the trench may be made deeper by up to 10  $\mu\text{m}$  than the depth of the diffusion layers for source and drain; the film thickness of the field-shield insulator film may range 5~200 nm; and the film thickness of the polycrystalline silicon film may range 40~800 nm.”

*See, e.g., Wada at 7:54-62.*

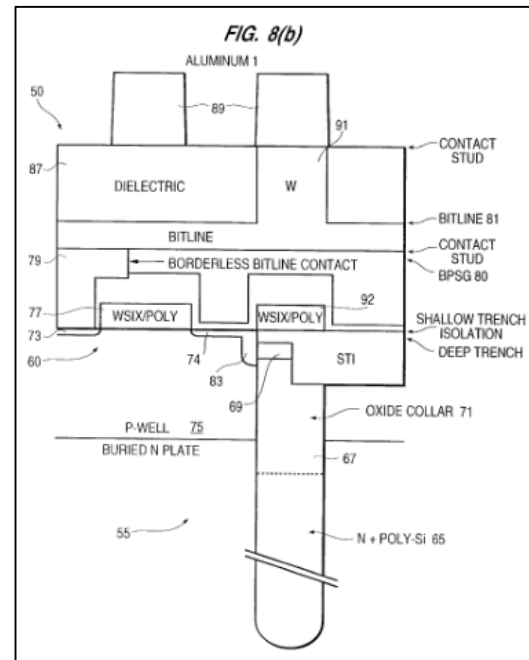
“The process of forming the trenches 113 is a dry etching process using gaseous chlorine to make cavities measuring 0.5~1.5  $\mu\text{m}$  in depth and 0.2~0.5  $\mu\text{m}$  in width. As illustrated in FIG. 6A, the etching process is carried out under conditions to favor etching on the side-wall surface of the cavities so that the width A of the trench 113 can be made to include an undercutting dimension C of about 0.02~0.2  $\mu\text{m}$  more than the opening dimension B on the  $\text{SiO}_2$  film 117. This undercut structure facilitates making of the subsequent fabrication of insulative isolation with trenches 113 to surround the active regions 109.”

*See, e.g., Wada at 9:66-10:9.*

**Furthermore, this element is obvious based on the knowledge of a person of ordinary skill in the art.**

	<p>A person of ordinary skill in the art would have been motivated to incorporate this element from Mitsuiki, Perera, Wada, or their own knowledge into Saki as a means “for further improvements in scaling down and isolation property” in “ultra large scale integrated circuits.” <i>See, e.g.</i> Mitsuiki at 1:14-16; Perera at 1:7-9; Wada at 1:9-13. A person of ordinary skill in the art would have a reasonable expectation of success in incorporating this limitation as the mechanisms for doing so are disclosed in references themselves. <i>See, e.g.</i>, Saki at 1:19-24. (“Shallow trench isolation is particularly advantageous for circuits having a high integration density since shallow trench isolation can provide for a relatively planar surface on which subsequent insulating and/or conducting layers may be formed.”).</p> <p>In addition to being a combination taught directly by these references, such a combination would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.</p>
[6] The transistor of claim 1, wherein said gate electrode is comprised of polysilicon.	<p><b>Saki discloses the transistor of claim 1, wherein said gate electrode is comprised of polysilicon. By way of non-limiting example, Saki discloses:</b></p> <p><i>See</i> disclosure for claim 1(c)(i). This disclosure is incorporated by reference herein. By way of further example:</p> <p>“FIGS. 8(a) and 8(b) illustrate a trench DRAM cell with a self-aligned buried strap which is isolated from other cells by a shallow trench isolation structure in accordance with the present invention. Specifically, FIG. 8(a) is a top-down view of the trench DRAM cell and FIG. 8(b) is a cross-sectional view taken along line A-A' of FIG. 8(a). DRAM cell 50 includes a trench capacitor 55 and a transfer gate 60. Trench capacitor 55 includes a first N<sup>+</sup> -type polycrystalline silicon fill 65, a second polycrystalline silicon fill 67, and a collar oxide 71. Transfer gate 60 includes N-type source/drain and drain/source regions 73 and 74 formed in P-type well 75 and a WSi<sub>x</sub> /polycrystalline silicon gate 77 insulatively spaced from the channel region between source/drain region 73 and drain/source region 74. A bit line contact 79 formed in an opening in an insulating layer 80 (of BPSG, for example) electrically connects source/drain region 73 to bit</p>

line 81. A shallow trench isolation structure formed in accordance with the present invention electrically isolates DRAM cell 50 from an adjacent DRAM cell and passing word line 92. Passing word line 92 has a WSix /polycrystalline silicon structure. A dielectric layer 87 is formed on bit line 81 and aluminum wirings 89 are formed on dielectric layer 87. One of the aluminum wirings 89 is connected to bit line 81 by a contact stud 91 of tungsten, for example. A diffusion region 83 electrically connects third polycrystalline silicon fill 69 and drain/source region 74 of MOS transfer gate 60. This diffusion region is formed by outdiffusing dopants from the highly doped polycrystalline silicon fill in the storage trench into P-well 75. Diffusion region 83 and third polycrystalline silicon fill 69 constitute a buried strap for connecting trench capacitor 55 to transfer gate 60.”  
*See, e.g., Saki at 6:54-7:18.*



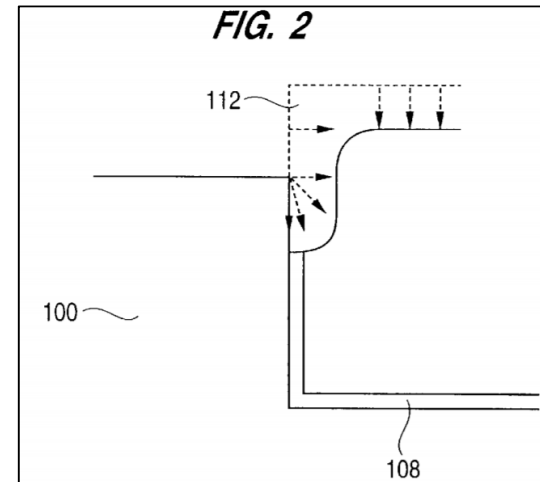
*See, e.g., Saki at Fig. 8(b).*

	<p>“A method of manufacturing the DRAM cell 50 using the shallow isolation structure and method of the present invention will be described below with reference to FIGS. 9(a)-9(g). As shown in FIG. 9(a), a buried N-type well 48 is formed in a P-type semiconductor substrate 300 by implanting phosphorous below the intended P-well for a memory cell array. A buried N-type well may also be formed by other methods, e.g., P-well implantation into an N-type semiconductor substrate or by epitaxy, and the invention is not limited in this respect. A silicon nitride layer 302 having a thickness of about 0.2 micrometers is formed by chemical vapor deposition, for example, on the surface of a thin oxide layer 301 having a thickness of about 10 nanometers which is thermally grown on semiconductor substrate 300. Oxide layer 301 and silicon nitride layer 302 are patterned and etched to provide a mask for etching a trench 303. Trench 303 is etched using an anisotropic etching process to a depth of about 8 micrometers as shown in FIG. 9(b). After storage node trench 303 is etched, an N-type capacitor plate 304 is formed by outdiffusing arsenic from the lower portion of trench 303. This may be accomplished, for example, by depositing an arsenic doped glass layer, etching the arsenic doped glass layer to remain only at the lower portion of trench 303, and performing an annealing process to outdiffuse the arsenic. A storage node dielectric layer (not shown) such as an oxide-nitride (ON) layer or a nitride-oxide (NO) layer is then formed in trench 303. After the dielectric layer is formed, a first conductive region is formed by filling trench 303 with an impurity-doped first conductive material such as N<sup>+</sup>-type polycrystalline silicon. The filling step may be carried out using chemical vapor deposition of silane or disilane, for example. The N<sup>+</sup>-type polycrystalline silicon is then etched back to a first level within trench 303 using an isotropic etch process to form first trench fill 65. The level of first trench fill 65 is, for example, about 1.0 micrometer below the surface of semiconductor substrate 300. Collar oxide 71 is then formed on the sidewall of the portion of trench 303 opened by the etching back of the N<sup>+</sup>-type polycrystalline silicon using low pressure chemical vapor deposition (LPCVD) or plasma-enhanced chemical vapor deposition (PECVD) TEOS as shown in FIG. 9(c).</p> <p>A second conductive region is formed by filling in the remainder of trench 303 with a second conductive material. The second conductive material may be, for example, N<sup>+</sup>-type polycrystalline silicon or undoped polycrystalline silicon and may be formed by chemical vapor deposition (CVD). The second conductive material and the oxide collar 71 are then etched back to a second level within trench 303 to form second trench fill 67 which is insulated from the semiconductor substrate by collar oxide 71 as shown in FIG. 9(d). The depth of the buried strap</p>
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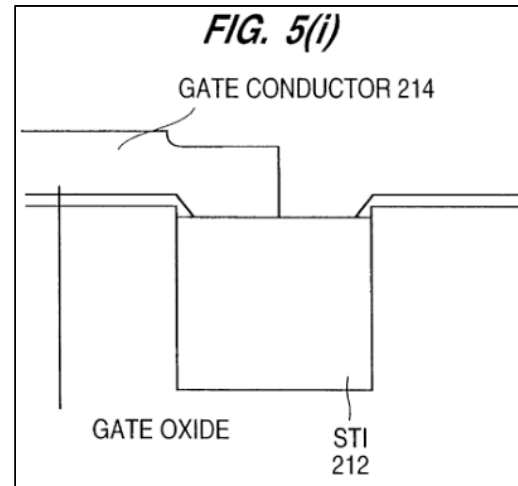
	<p>to be formed in a subsequent process step is defined by this controlled etch-back of the second conductive material and collar oxide 71. Second trench fill 67 is etched back to about 0.1 micrometer below the surface of semiconductor substrate 300. An in-situ removal of a native oxide in trench 303 is then performed. In particular, the native oxide on the upper surface of second trench fill 67 and on the sidewall of trench 303 through which impurities for the buried strap will subsequently be outdiffused are removed. This removal of native oxide may be carried out by an in-situ prebake in a hydrogen ambient at a temperature greater than 850° C., for example.</p> <p>The portion of trench 303 opened by the etching back of collar oxide 71 and the second conductive material is then filled by a third conductive material. The third conductive material may be, for example, undoped polycrystalline silicon deposited by chemical vapor deposition (CVD). The polycrystalline silicon is then etched back using reactive ion etching, for example, to form a third trench fill 69 as shown in FIG. 9(e). The polycrystalline silicon is preferably etched back to about 0.05 micrometer below the surface of semiconductor substrate 300 as determined by the tolerable resistance of the buried strap, and by the recess etch controllability.”</p> <p><i>See, e.g., Saki at 7:19-8:25; see also id. at Figs. 9(a)-(g).</i></p>
<p>[7] The transistor of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.</p>	<p><b>Saki discloses the transistor of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride. By way of non-limiting example, Saki discloses:</b></p> <p><i>See disclosure for claim 1(c)(i). This disclosure is incorporated by reference herein. By way of further example:</i></p> <p>“A conventional process for forming a shallow trench isolation (STI) structure is shown in FIGS. 1(a)-1(f). A silicon dioxide (SiO<sub>2</sub>) layer 102 and a silicon nitride (Si<sub>3</sub> N<sub>4</sub>) layer 104 are successively formed on the surface of a silicon substrate 100 as shown in FIG. 1(a). A patterned resist (not shown) is formed on the upper surface of silicon nitride layer 104 and an etching process such as reactive ion etching (RIE) is used to form trenches 106 in silicon substrate 100 as shown in FIG. 1(b). A thermal oxidation process is then performed to form a thermal silicon dioxide (SiO<sub>2</sub>) layer 108 on the exposed surfaces of the silicon substrate 100 as shown in FIG.</p>

1(c). A silicon dioxide ( $\text{SiO}_2$ ) layer 110 is then deposited by the decomposition of TEOS, for example, to fill in trenches 106 as shown in FIG. 1(d). The silicon dioxide layer 110 is then planarized by chemical mechanical polishing (CMP), for example, as shown in FIG. 1(e). Silicon nitride layer 104 serves as a stopper layer for the planarization process. Silicon nitride layer 104 is then removed. Various wet etching processes are used in subsequent manufacturing steps to remove the silicon dioxide layer 102, as well as to remove any sacrificial or dummy silicon dioxide layers which may be formed after removal of the silicon nitride layer. Such sacrificial silicon dioxide layers may be formed to clean the substrate surface prior to growing a gate oxide layer or to repair substrate damage due, for example, to implantation processes (e.g., channel implantation processes for controlling a threshold voltage of a transistor). However, these wet etching processes cause an etching away of the silicon dioxide at the corner 112 of the shallow trench isolation structure as shown in FIG. 1(f). This etching away of the silicon dioxide at the corner of the shallow trench isolation structure is shown in more detail in FIG. 2 and can result in a lowering of the threshold voltage of a transistor formed in the active area defined by the shallow trench isolation structure.”

*See, e.g., Saki at 1:25-59.*



*See, e.g., Saki at Fig. 2.*



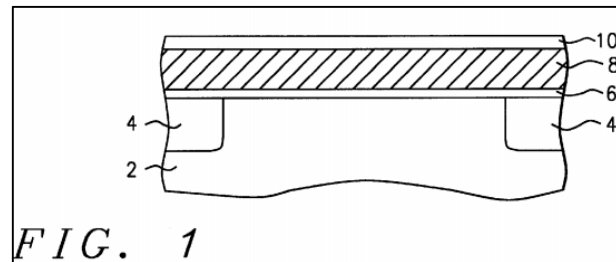
See, e.g., Saki at Figs. 5(i).

“FIGS. 7(a)-7(h) are cross-sectional views illustrating a method for forming a shallow trench isolation structure in accordance with a second embodiment of the present invention. As shown in FIG. 7(a), a pad silicon dioxide ( $\text{SiO}_2$ ) layer 202 and a pad silicon nitride ( $\text{Si}_3\text{N}_4$ ) layer 204 are provided on a substrate 200. Silicon dioxide layer 202 has a thickness of about 80 Å-100 Å (e.g., 82 Å) and may be formed by thermal oxidation or by low pressure chemical vapor deposition (LPCVD), for example. Silicon nitride layer 204 has a thickness of about 1000 Å-2000 Å (e.g., 1300 Å) and may be formed, for example, by LPCVD. Substrate 200 may be a silicon wafer or an epitaxial layer formed on a silicon wafer. A patterned photoresist (not shown) is then formed on pad silicon nitride layer 204. The pad silicon nitride layer, the pad silicon dioxide layer, and the substrate are then etched by, for example, reactive ion etching using the patterned photoresist as a mask to form a trench 206 as shown in FIG. 7(b). Pad silicon nitride layer 204 is then isotropically etched using, for example, HF/Glycerol or hot phosphoric acid. In accordance with the present embodiment, the amount of silicon nitride which is etched during this isotropic etching step is about 250 Å. Thus, the isotropic etch pulls back the pad silicon nitride layer by a distance  $L=250$  Å relative to the sidewall of trench 206, as shown in FIG. 7(c). A thin silicon dioxide ( $\text{SiO}_2$ ) layer 208 having a thickness of about 80 Å-

	<p>100Å is formed by a high temperature (for example, 1000° C.) thermal oxidation over the portions of the silicon substrate exposed by the forming of trench 206 as shown in FIG. 7(d). This high temperature oxidation removes substrate damage caused by the etching process for forming trench 206. Optionally, a thin silicon nitride layer (not shown) having a thickness of about 50 Å may then be deposited by, for example, CVD on pad silicon nitride layer 204 and on silicon dioxide layer 208. The silicon nitride layer may be provided, for example, in order to prevent oxidation of underlying layers during subsequent processing steps. As in the first embodiment, if the 50 Å silicon nitride layer is formed, the amount of silicon nitride which is etched during the isotropic etching step is about 300 Å. In this way, a composite silicon nitride layer is formed which is pulled back by about 250 Å from the sidewall of trench 206. Next, a silicon dioxide layer 212 is blanket deposited over the entire surface of the substrate using, for example, a CVD process in which TEOS (Si(OC<sub>2</sub>H<sub>5</sub>)<sub>4</sub>) is decomposed, as shown in FIG. 7(e). The silicon dioxide layer 212 is then planarized using, for example, RIE, chemical mechanical polishing, or a combination thereof as shown in FIG. 7(f). The pad silicon nitride layer 204 is then removed by, for example, chemical dry etching (CDE) or etching using hot phosphoric acid or HF/glycerol as shown in FIG. 7(g). One or more wet etching processes are then utilized to remove the pad silicon dioxide layer 202, as well as any sacrificial or dummy oxide layers which may be formed, resulting in the structure shown in FIG. 7(h). Because the pad silicon nitride layer was pulled-back by an isotropic etching process, the shallow trench isolation structure of FIG. 7(g) has a T-shape. In this way, subsequent wet etching processes for removing the pad silicon dioxide layer 202 and any sacrificial or dummy oxide layers attack these extensions of the shallow trench isolation structure and do not result in an etching away of the insulator at the corner of the shallow trench isolation structure as can be seen with reference to FIG. 7(h).</p> <p>The same advantages which are obtained in the first embodiment are also obtained in the second embodiment.”</p> <p><i>See, e.g., Saki at 5:55-6:53; see also id. at Figs. 7(a)-(h).</i></p> <p><b>In the event it is determined that Saki does not disclose this element, it would have been obvious to modify Saki to include this element based either on the knowledge of a person of skill in the art and/or the teaching of other references. For example, Pey teaches this element:</b></p>
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“Referring to FIG. 1, an overlying stack consisting of a gate oxide layer 6, an overlying first polysilicon layer 8, and a still further overlying silicon nitride layer 10 is then formed. Said gate oxide 6 is a thin thermal oxide, with a typical thickness range of about 25 to 30 angstroms, that is subsequently nitrided. A preferred gate oxide thickness of about 40 angstroms is grown in a dry followed by a partial wet ambient, at a typical temperature range of about 800 to 1000 degrees centigrade for a duration of about 1 to 3 minutes. Said subsequent nitridation process can be performed at a temperature range of about 900 to 1000 degrees centigrade, in a nitrous oxide (N<sub>2</sub>O) ambient, using an RTA.”

*See, e.g., Pey at 4:56-67.*



*See, e.g., Pey at Fig. 1.*

**Furthermore, this element is obvious based on the knowledge of a person of ordinary skill in the art.**

A person of ordinary skill in the art would have been motivated to incorporate this element from Pey or their own knowledge into Saki because in typical device structures, “a gate oxide layer and an overlying polysilicon layer are first patterned into gate regions.” *See, e.g., Pey at 1:44-46.* A person of ordinary skill in the art would have a reasonable expectation of success in incorporating this limitation as the mechanisms for doing so are disclosed in references themselves. *See, e.g., Saki at 8:55-57* (“A gate insulator may then be formed on the planar surface, and gate material may be deposited and patterned to form gate electrodes.”).

	<p>In addition to being a combination taught directly by these references, such a combination would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.</p>																																			
<p>[8] The transistor of claim 1, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.</p>	<p><b>In the event it is determined that Saki does not disclose this element, it would have been obvious to modify Saki to include this element based either on the knowledge of a person of skill in the art and/or the teaching of other references. For example, Tao teaches this element:</b></p> <p>“The polysilicon layer can is a poly-crystalline layer of silicon that is deposited on the gate oxide 14. The polysilicon layer can be uses as a silicon gate or can be used for interconnecting interconnections between devices. The polysilicon layer 18 preferably has a thickness in a range of between about 1000 and 3000 Å.</p> <p>The polysilicon layer can also include a top WSi<sub>x</sub> or other refractory metal layer.” See, e.g., Tao at 6:8-16.</p> <table><tr><th colspan="5">TABLE</th></tr><tr><th>Element No.</th><th>generic name</th><th>preferred examples</th><th>Preferred Parameters (thickness, doping, etc . . . )</th><th>Other alternate examples</th></tr><tr><td>14</td><td>gate oxide layer</td><td>oxide</td><td>Thickness = 20 to 100 Å</td><td>nitrided oxide</td></tr><tr><td>20</td><td>polysilicon layer</td><td>Polysilicon or amorphous silicon</td><td>Th = 1000 to 3000 Å = doped or undoped</td><td>WSi<sub>x</sub> over polysilicon</td></tr><tr><td>22</td><td>a hard mask layer</td><td>Oxide</td><td>200 to 3000 Å</td><td>nitride or oxynitride</td></tr><tr><td>26</td><td>bottom anti-reflective coating (BARC) layer</td><td>organic</td><td>Thickness = 500 to 2000 Å</td><td></td></tr><tr><td>30</td><td>resist layer</td><td>DUV photoresist</td><td>6000 to 13000 Å</td><td>i-line</td></tr></table> <p>See, e.g., Tao at 5:45-67.</p>	TABLE					Element No.	generic name	preferred examples	Preferred Parameters (thickness, doping, etc . . . )	Other alternate examples	14	gate oxide layer	oxide	Thickness = 20 to 100 Å	nitrided oxide	20	polysilicon layer	Polysilicon or amorphous silicon	Th = 1000 to 3000 Å = doped or undoped	WSi <sub>x</sub> over polysilicon	22	a hard mask layer	Oxide	200 to 3000 Å	nitride or oxynitride	26	bottom anti-reflective coating (BARC) layer	organic	Thickness = 500 to 2000 Å		30	resist layer	DUV photoresist	6000 to 13000 Å	i-line
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	<p><b>Furthermore, this element is obvious based on the knowledge of a person of ordinary skill in the art.</b></p> <p>A person of ordinary skill in the art would have been motivated to incorporate this element from Tao or their own knowledge into Saki because Tao is focused on fabricating polysilicon gates (“This invention relates generally to fabrication of polysilicon gates in a semiconductor device”). <i>See, e.g.</i> Tao 1:7-8. A person of ordinary skill in the art would have a reasonable expectation of success in incorporating this limitation as the mechanisms for doing so are disclosed in references themselves. <i>See, e.g.</i>, Saki at 8:55-57 (“A gate insulator may then be formed on the planar surface, and gate material may be deposited and patterned to form gate electrodes.”).</p> <p>In addition to being a combination taught directly by these references, such a combination would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.</p>
[9] The transistor of claim 1, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.	<p><b>In the event it is determined that Saki does not disclose this element, it would have been obvious to modify Saki to include this element based either on the knowledge of a person of skill in the art and/or the teaching of other references. For example, Tao or Pey teach this element:</b></p> <p>“The gate oxide layer 14 is preferably composed of silicon oxide having a thickness in a range of between about 20 and 100 Å.”  <i>See, e.g.</i>, Tao at 6:5-7.</p>

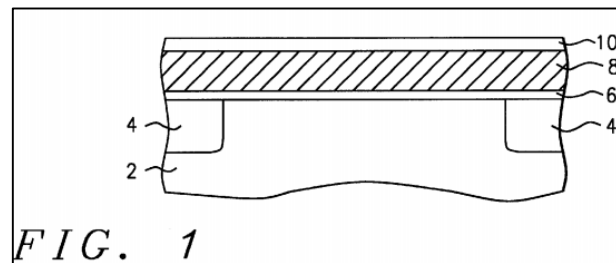
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22	a hard mask layer	Oxide	200 to 3000 Å	
26	bottom anti-reflective coating (BARC) layer	organic	Thickness = 500 to 2000 Å	
30	resist layer	DUV photoresist	6000 to 13000 Å	i-line

See, e.g., Tao at 5:45-67.

**As another example, Pey also teaches this element:**

“Referring to FIG. 1, an overlying stack consisting of a gate oxide layer 6, an overlying first polysilicon layer 8, and a still further overlying silicon nitride layer 10 is then formed. Said gate oxide 6 is a thin thermal oxide, with a typical thickness range of about 25 to 30 angstroms, that is subsequently nitrided. A preferred gate oxide thickness of about 40 angstroms is grown in a dry followed by a partial wet ambient, at a typical temperature range of about 800 to 1000 degrees centigrade for a duration of about 1 to 3 minutes. Said subsequent nitridation process can be performed at a temperature range of about 900 to 1000 degrees centigrade, in a nitrous oxide (N<sub>2</sub>O) ambient, using an RTA.”

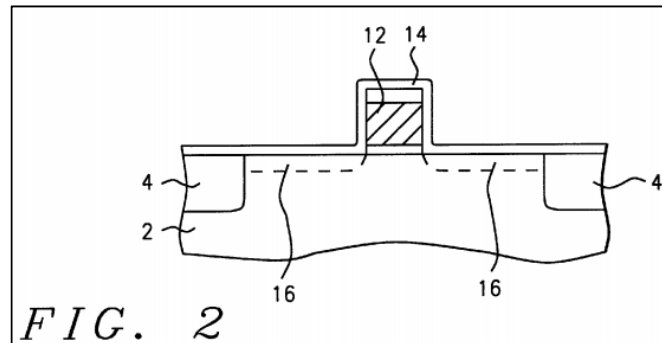
See, e.g., Pey at 4:56-67.



	<p><i>See, e.g.,</i> Pey at Fig. 1.</p> <p><b>Furthermore, this element is obvious based on the knowledge of a person of ordinary skill in the art.</b></p> <p>A person of ordinary skill in the art would have been motivated to incorporate this element from Pey, Tao, or their own knowledge into Saki because in typical device structures, “a gate oxide layer and an overlying polysilicon layer are first patterned into gate regions.” <i>See, e.g.</i> Pey at 1:44-46; Tao 1:7-8. A person of ordinary skill in the art would have a reasonable expectation of success in incorporating this limitation as the mechanisms for doing so are disclosed in references themselves. <i>See, e.g.,</i> Saki at 8:55-57 (“A gate insulator may then be formed on the planar surface, and gate material may be deposited and patterned to form gate electrodes.”).</p> <p>In addition to being a combination taught directly by these references, such a combination would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.</p>
<p>[10] The transistor of claim 1, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.</p>	<p><b>In the event it is determined that Saki does not disclose this element, it would have been obvious to modify Saki to include this element based either on the knowledge of a person of skill in the art and/or the teaching of other references. For example, Rubin or Pey teach this element:</b></p> <p>“Referring now more particularly to FIG. 2, conventional masking and plasma etching is now performed on said stack, consisting of said nitride layer 10, said first polysilicon layer 8 and said gate oxide layer 6, in order to form first polysilicon gate 12. The gate oxide acts as an etch stop, after which a cleaning step is used to remove the remaining oxide from the active regions. A Bromine based (HBr) plasma etching chemistry is typically used to form said first polysilicon gate 12. An overlying thin TEOS, SiO<sub>2</sub> liner 14 is then blanket deposited to a thickness of about 150 angstroms, to reduce overlap capacitance. At this stage Low Doped</p>

Drain, LDD, regions 16 are formed, by means of conventional masking and ion implantation processing.”

*See, e.g., Pey at 5:12-24.*



*See, e.g., Pey at Fig. 2.*

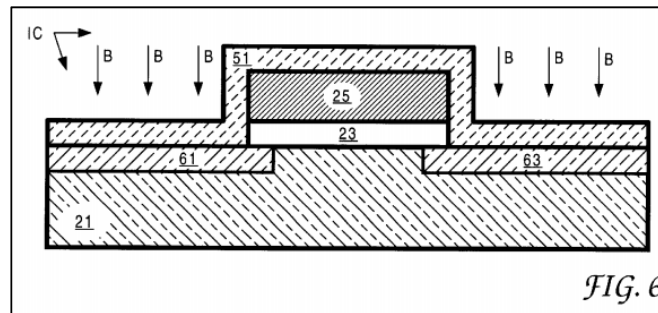
**As another example, Rubin also teaches this element:**

“The present invention provides for implanting through a blocking layer of material that promotes interstitial recombination at its interface with crystalline silicon better than does a conventionally grown oxide layer. For example, the blocking layer can be of carbon-bearing silicon dioxide such as that resulting from a TEOS oxide deposition. The invention applies most favorably to boron or other p-type source/drain extension implants for a PMOS transistor.”

*See, e.g., Rubin at 3:13-20.*

“Source/drain extension implants are performed at step S5. Separate masks are used for the PMOS and NMOS transistors. For each implant, the energy is selected so that the bulk of the respective dopant is implanted just below the silicon surface. Step S5 involves implanting boron B into the source/drain regions of the PMOS transistors and arsenic (or phosphorous) into the source/drain regions of the NMOS transistors. Step S5 can also provide for an oblique “halo” implant of complementary dopant (boron for NMOS, arsenic or phosphorous for PMOS) under the gate to help counter the short-channel effect.

Step S5 can also provide for thermal “drive-in” of the dopants. Elevated temperatures increase the mobility of atoms entrained in the silicon crystal lattice. Initially, dopants diffuse in all directions. However, as interstitial silicon migrates into the TEOS layer, it sweeps other dopants, particularly boron (which comprises relatively small atoms), with it. As a result, the boron is confined closer to the TEOS covered silicon surface than it would be if a material, such as a thermal oxide, with a lower interstitial recombination rate were used. The post-diffusion extents of the source extension 61 and a drain extension 63 are shown in FIG. 6.”



See, e.g., Rubin at Fig. 6.

**Furthermore, this element is obvious based on the knowledge of a person of ordinary skill in the art.**

A person of ordinary skill in the art would have been motivated to incorporate this element from Pey, Rubin, or their own knowledge into Saki because in typical device structures, “a gate oxide layer and an overlying polysilicon layer are first patterned into gate regions.” See, e.g. Pey at 1:44-46. (“To reduce what is known as a “hot-carrier effect”, each source and each drain can include a lightly-doped extension that separates a respective heavily doped “deep” source/drain region from the channel. The channel then separates the source extension from the drain extension (also known as a “lightly doped drain” or “LDD”).”); see also, e.g. Rubin at 1:34-39. A person of ordinary skill in the art would have a reasonable expectation of success in incorporating this limitation as the mechanisms for doing so are disclosed in references themselves. See, e.g., Saki at 8:55-57 (“A gate insulator may then be formed on the planar surface, and gate material may be deposited and patterned to form gate electrodes.”).

	<p>In addition to being a combination taught directly by these references, such a combination would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.</p>
[11] The transistor of claim 1, wherein said gate electrode has first and second end portions that extend into said recess.	<p><b>Saki discloses the transistor of claim 1, wherein said gate electrode has first and second end portions that extend into said recess. By way of non-limiting example, Saki discloses:</b></p> <p><i>See disclosure for claim 1(c)(ii). This disclosure is incorporated by reference herein.</i></p>
[12] The transistor of claim 11, wherein said first and second end portions extending into said recess are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.	<p><b>Saki discloses the transistor of claim 11, wherein said first and second end portions extending into said recess are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure. By way of non-limiting example, Saki discloses:</b></p> <p><i>See disclosure for claims 1(c)(ii) and 23(b). This disclosure is incorporated by reference herein.</i></p>
[13pre] A transistor, comprising:	<p><b>Saki discloses a transistor.</b></p> <p><i>See disclosure for claim 1(p). This disclosure is incorporated by reference herein.</i></p>
[13a] a semiconducting substrate comprised of silicon;	<p><b>Saki discloses a semiconducting substrate comprised of silicon.</b></p> <p><i>See disclosure for claims 1(a) and 2. This disclosure is incorporated by reference herein.</i></p>
[13b] a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove;	<p><b>Saki discloses a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove.</b></p> <p><i>See disclosure for claim 1(b). This disclosure is incorporated by reference herein.</i></p>

[13c] a gate electrode comprised of polysilicon and a gate insulation layer formed above said substrate, a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure; and	<p><b>Saki discloses a gate electrode comprised of polysilicon and a gate insulation layer formed above said substrate, a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure.</b></p> <p><i>See disclosure for claims 1(c)(i), 1(c)(ii), and 6. This disclosure is incorporated by reference herein.</i></p>
[13d] a source region and a drain region formed in said substrate.	<p><b>Saki discloses a source region and a drain region formed in said substrate.</b></p> <p><i>See disclosure for claim 1(d). This disclosure is incorporated by reference herein.</i></p>
[14] The transistor of claim 13, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.	<p><b>Saki discloses the transistor of claim 13, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.</b></p> <p><i>See disclosure for claim 3. This disclosure is incorporated by reference herein.</i></p>
[16] The transistor of claim 13, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.	<p><b>Saki discloses the transistor of claim 13, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.</b></p> <p><i>See disclosure for claim 5. This disclosure is incorporated by reference herein.</i></p>
[17] The transistor of claim 13, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.	<p><b>Saki discloses the transistor of claim 13, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.</b></p> <p><i>See disclosure for claim 7. This disclosure is incorporated by reference herein.</i></p>
[18] The transistor of claim 13, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.	<p><b>Saki discloses the transistor of claim 13, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.</b></p> <p><i>See disclosure for claim 8. This disclosure is incorporated by reference herein.</i></p>

<p>[19] The transistor of claim 13, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.</p>	<p><b>Saki discloses the transistor of claim 13, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.</b></p> <p><i>See disclosure for claim 9. This disclosure is incorporated by reference herein.</i></p>
<p>[20] The transistor of claim 13, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.</p>	<p><b>Saki discloses the transistor of claim 13, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.</b></p> <p><i>See disclosure for claim 10. This disclosure is incorporated by reference herein.</i></p>
<p>[21] The transistor of claim 13, wherein said gate electrode has first and second end portions that extend into said recess in said substrate.</p>	<p><b>Saki discloses the transistor of claim 13, wherein said gate electrode has first and second end portions that extend into said recess in said substrate.</b></p> <p><i>See disclosure for claim 11. This disclosure is incorporated by reference herein.</i></p>
<p>[22] The transistor of claim 21, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.</p>	<p><b>Saki discloses the transistor of claim 21, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.</b></p> <p><i>See disclosure for claim 12. This disclosure is incorporated by reference herein.</i></p>
<p>[23pre] A transistor, comprising:</p>	<p><b>Saki discloses a transistor.</b></p> <p><i>See disclosure for claim 1(p). This disclosure is incorporated by reference herein.</i></p>
<p>[23a] a semiconducting substrate;</p>	<p><b>Saki discloses a semiconducting substrate.</b></p> <p><i>See disclosure for claim 1(a). This disclosure is incorporated by reference herein.</i></p>

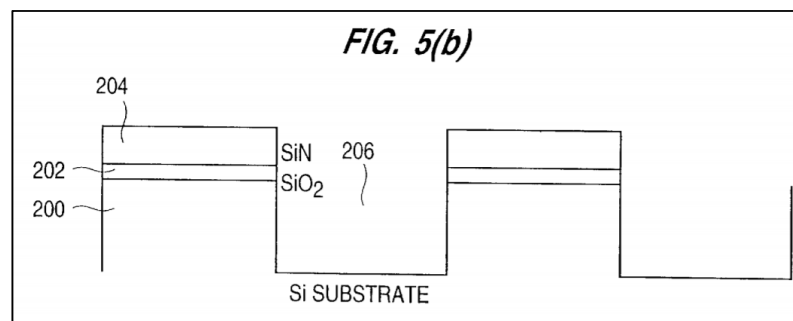
<p>[23b] a recessed isolation structure defining an active area having an upper surface and an exposed sidewall surface;</p>	<p><b>Saki discloses a recessed isolation structure defining an active area having an upper surface and an exposed sidewall surface. By way of non-limiting example, Saki discloses:</b></p> <p><i>See also</i> disclosure for claim 1(b). This disclosure is incorporated by reference herein. Additional relevant disclosure includes at least the following non-limiting examples:</p> <p>“A conventional process for forming a shallow trench isolation (STI) structure is shown in FIGS. 1(a)-1(f). A silicon dioxide (SiO<sub>2</sub>) layer 102 and a silicon nitride (Si<sub>3</sub> N<sub>4</sub>) layer 104 are successively formed on the surface of a silicon substrate 100 as shown in FIG. 1(a). A patterned resist (not shown) is formed on the upper surface of silicon nitride layer 104 and an etching process such as reactive ion etching (RIE) is used to form trenches 106 in silicon substrate 100 as shown in FIG. 1(b). A thermal oxidation process is then performed to form a thermal silicon dioxide (SiO<sub>2</sub>) layer 108 on the exposed surfaces of the silicon substrate 100 as shown in FIG. 1(c). A silicon dioxide (SiO<sub>2</sub>) layer 110 is then deposited by the decomposition of TEOS, for example, to fill in trenches 106 as shown in FIG. 1(d). The silicon dioxide layer 110 is then planarized by chemical mechanical polishing (CMP), for example, as shown in FIG. 1(e). Silicon nitride layer 104 serves as a stopper layer for the planarization process. Silicon nitride layer 104 is then removed. Various wet etching processes are used in subsequent manufacturing steps to remove the silicon dioxide layer 102, as well as to remove any sacrificial or dummy silicon dioxide layers which may be formed after removal of the silicon nitride layer. Such sacrificial silicon dioxide layers may be formed to clean the substrate surface prior to growing a gate oxide layer or to repair substrate damage due, for example, to implantation processes (e.g., channel implantation processes for controlling a threshold voltage of a transistor). However, these wet etching processes cause an etching away of the silicon dioxide at the corner 112 of the shallow trench isolation structure as shown in FIG. 1(f). This etching away of the silicon dioxide at the corner of the shallow trench isolation structure is shown in more detail in FIG. 2 and can result in a lowering of the threshold voltage of a transistor formed in the active area defined by the shallow trench isolation structure.”</p> <p><i>See, e.g.,</i> Saki at 1:25-59; <i>see also</i> Figs. 1(b)-(f).</p> <p>“In accordance with the above-described method, the insulator at the corner of the shallow trench isolation structure is protected from attack during subsequent etching processes and problems due to changes in the threshold voltages of elements formed in the active area defined</p>
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	<p>by the shallow trench isolation structure can be reduced. In addition, since the pulling-back of the pad nitride is carried out in an isotropic etching step, the method of the present invention provides for enhanced controllability of the shape of the shallow trench isolation structure. Still further, the method of the present invention has a small number of steps and therefore contributes to ease of device manufacture and reduced manufacturing costs.”  <i>See, e.g., Saki at 3:9-21.</i></p> <p>“FIGS. 5(a)-5(i) are cross-sectional views illustrating a method for forming a shallow trench isolation structure in accordance with a first embodiment of the present invention. As shown in FIG. 5(a), a pad silicon dioxide (SiO<sub>2</sub>) layer 202 and a pad silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 204 are provided on a substrate 200. Silicon dioxide layer 202 has a thickness of about 80 Å-100 Å (e.g., 82 Å) and may be formed by thermal oxidation or by low pressure chemical vapor deposition (LPCVD), for example. Silicon nitride layer 204 has a thickness of about 1000 Å-2000 Å (e.g., 1300 Å) and may be formed, for example, by LPCVD. Substrate 200 may be a silicon wafer or an epitaxial layer formed on a silicon wafer. A patterned photoresist (not shown) is then formed on pad silicon nitride layer 204. The pad silicon nitride layer, the pad silicon dioxide layer, and the substrate are then etched, for example, by reactive ion etching using the patterned photoresist as a mask to form a trench 206 as shown in FIG. 5(b). A thin silicon dioxide (SiO<sub>2</sub>) layer 208 having a thickness of about 80 Å-100 Å is formed by a high temperature (for example, 1000° C.) thermal oxidation over the portions of the silicon substrate exposed by the forming of trench 206 as shown in FIG. 5(c). This high temperature oxidation removes substrate damage caused by the etching process for forming trench 206. Pad silicon nitride layer 204 is then isotropically etched by, for example, chemical dry etching. In accordance with the present invention, the amount of silicon nitride which is etched during this isotropic etching step is about 250 Å. Thus, the isotropic etch pulls back pad silicon nitride layer 204 by a distance L=250 Å relative to the sidewall of trench 206 as shown in FIG. 5(d). It will be apparent to one skilled in the art that the amount of silicon nitride to be isotropically etched in this etching step will depend on the overall manufacturing process into which the teachings of this invention are incorporated. In general, the amount of silicon nitride to be etched should be sufficient to result in the protection of the corners of the shallow trench isolation structure from attack. In addition, the isotropic etching of the pad silicon nitride layer should leave silicon nitride having a thickness which is sufficient to function as a stopper layer for the planarization process to be described below with reference to FIG. 5(f).”</p>
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*See, e.g., Saki at 3:66-4:39.*

“Thus, in accordance with the above-described method of the present invention, etching of the insulator at the corner of the shallow trench isolation structure is suppressed and problems due to changes in the threshold voltages of elements formed in the active area defined by the shallow trench isolation structure can be minimized. As discussed with respect to FIG. 4, the degree to which the corner of the structure is protected is determined by the length "L". In accordance with the present invention, this length "L" is determined by the isotropic etching of the pad silicon nitride layer. Since, in accordance with the present invention, only a single process factor affects the length "L", enhanced controllability of the shape of the shallow trench isolation structure can be achieved and therefore fluctuations in device characteristics can be reduced. In addition, because an upper surface of the shallow trench isolation structure and the surface of the substrate are substantially level, no step is created between the shallow trench isolation structure and a subsequently formed gate conductor 214 as shown in FIG. 5(i). Thus, patterning of the gate electrode is simplified. Still further, the method of the present invention has a small number of steps and therefore contributes to ease of device manufacture and reduced manufacturing costs.”

*See, e.g., Saki at 5:8-30.*



*See, e.g., Saki at Fig. 5(b); see also id. at Figs. 5(c)-(h).*

“FIGS. 7(a)-7(h) are cross-sectional views illustrating a method for forming a shallow trench isolation structure in accordance with a second embodiment of the present invention. As shown in FIG. 7(a), a pad silicon dioxide (SiO<sub>2</sub>) layer 202 and a pad silicon nitride (Si<sub>3</sub>N<sub>4</sub>) layer 204

	<p>are provided on a substrate 200. Silicon dioxide layer 202 has a thickness of about 80 Å-100 Å (e.g., 82 Å) and may be formed by thermal oxidation or by low pressure chemical vapor deposition (LPCVD), for example. Silicon nitride layer 204 has a thickness of about 1000 Å-2000 Å (e.g., 1300 Å) and may be formed, for example, by LPCVD. Substrate 200 may be a silicon wafer or an epitaxial layer formed on a silicon wafer. A patterned photoresist (not shown) is then formed on pad silicon nitride layer 204. The pad silicon nitride layer, the pad silicon dioxide layer, and the substrate are then etched by, for example, reactive ion etching using the patterned photoresist as a mask to form a trench 206 as shown in FIG. 7(b). Pad silicon nitride layer 204 is then isotropically etched using, for example, HF/Glycerol or hot phosphoric acid. In accordance with the present embodiment, the amount of silicon nitride which is etched during this isotropic etching step is about 250 Å. Thus, the isotropic etch pulls back the pad silicon nitride layer by a distance <math>L=250\text{ Å}</math> relative to the sidewall of trench 206, as shown in FIG. 7(c). A thin silicon dioxide (<math>\text{SiO}_2</math>) layer 208 having a thickness of about 80Å-100Å is formed by a high temperature (for example, 1000° C.) thermal oxidation over the portions of the silicon substrate exposed by the forming of trench 206 as shown in FIG. 7(d). This high temperature oxidation removes substrate damage caused by the etching process for forming trench 206. Optionally, a thin silicon nitride layer (not shown) having a thickness of about 50 Å may then be deposited by, for example, CVD on pad silicon nitride layer 204 and on silicon dioxide layer 208. The silicon nitride layer may be provided, for example, in order to prevent oxidation of underlying layers during subsequent processing steps. As in the first embodiment, if the 50 Å silicon nitride layer is formed, the amount of silicon nitride which is etched during the isotropic etching step is about 300 Å. In this way, a composite silicon nitride layer is formed which is pulled back by about 250 Å from the sidewall of trench 206. Next, a silicon dioxide layer 212 is blanket deposited over the entire surface of the substrate using, for example, a CVD process in which TEOS (<math>\text{Si}(\text{OC}_2\text{H}_5)_4</math>) is decomposed, as shown in FIG. 7(e). The silicon dioxide layer 212 is then planarized using, for example, RIE, chemical mechanical polishing, or a combination thereof as shown in FIG. 7(f). The pad silicon nitride layer 204 is then removed by, for example, chemical dry etching (CDE) or etching using hot phosphoric acid or HF/glycerol as shown in FIG. 7(g). One or more wet etching processes are then utilized to remove the pad silicon dioxide layer 202, as well as any sacrificial or dummy oxide layers which may be formed, resulting in the structure shown in FIG. 7(h). Because the pad silicon nitride layer was pulled-back by an isotropic etching process, the shallow trench isolation structure of FIG. 7(g) has a T-shape. In this way, subsequent wet etching processes for</p>
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	<p>removing the pad silicon dioxide layer 202 and any sacrificial or dummy oxide layers attack these extensions of the shallow trench isolation structure and do not result in an etching away of the insulator at the corner of the shallow trench isolation structure as can be seen with reference to FIG. 7(h).”</p> <p><i>See, e.g., Saki at 5:55-6:51; see also id. at Figs. 7(b)-(h).</i></p>
[23c] a gate insulation layer and a gate electrode positioned above a portion of said upper surface and a portion of said exposed sidewall surface of said active area; and	<p><b>Saki discloses a gate insulation layer and a gate electrode positioned above a portion of said upper surface and a portion of said exposed sidewall surface of said active area.</b></p> <p><i>See disclosure for claims 1(c)(i) and (ii), 12, and 23(b). This disclosure is incorporated by reference herein.</i></p>
[23d] a source region and a drain region formed in said active area.	<p><b>Saki discloses a source region and a drain region formed in said active area.</b></p> <p><i>See disclosure for claim 1(d). This disclosure is incorporated by reference herein.</i></p>
[24] The transistor of claim 23, wherein said semiconducting substrate is comprised of silicon.	<p><b>Saki discloses the transistor of claim 23, wherein said semiconducting substrate is comprised of silicon.</b></p> <p><i>See disclosure for claim 2. This disclosure is incorporated by reference herein.</i></p>
[25] The transistor of claim 23, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.	<p><b>Saki discloses the transistor of claim 23, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.</b></p> <p><i>See disclosure for claim 3. This disclosure is incorporated by reference herein.</i></p>
[27] The transistor of claim 23, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.	<p><b>Saki discloses the transistor of claim 23, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.</b></p> <p><i>See disclosure for claim 5. This disclosure is incorporated by reference herein.</i></p>

[28] The transistor of claim 23, wherein said gate electrode is comprised of polysilicon.	<p><b>Saki discloses the transistor of claim 23, wherein said gate electrode is comprised of polysilicon.</b></p> <p><i>See disclosure for claim 6. This disclosure is incorporated by reference herein.</i></p>
[29] The transistor of claim 23, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.	<p><b>Saki discloses the transistor of claim 23, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride</b></p> <p><i>See disclosure for claim 7. This disclosure is incorporated by reference herein.</i></p>
[30] The transistor of claim 23, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.	<p><b>Saki discloses the transistor of claim 23, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.</b></p> <p><i>See disclosure for claim 8. This disclosure is incorporated by reference herein.</i></p>
[31] The transistor of claim 23, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.	<p><b>Saki discloses the transistor of claim 23, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.</b></p> <p><i>See disclosure for claim 9. This disclosure is incorporated by reference herein.</i></p>
[32] The transistor of claim 23, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.	<p><b>Saki discloses the transistor of claim 23, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.</b></p> <p><i>See disclosure for claim 10. This disclosure is incorporated by reference herein.</i></p>
[33] The transistor of claim 23, wherein said gate electrode has first and second end portions that extend into a recess in said substrate defined by said recessed isolation structure.	<p><b>Saki discloses the transistor of claim 23, wherein said gate electrode has first and second end portions that extend into a recess in said substrate defined by said recessed isolation structure.</b></p> <p><i>See disclosure for claims 1(c)(ii) and 11. This disclosure is incorporated by reference herein.</i></p>

<p>[34] The transistor of claim 33, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.</p>	<p><b>Saki discloses the transistor of claim 33, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.</b></p> <p><i>See disclosure for claim 12. This disclosure is incorporated by reference herein.</i></p>
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