

# **EXHIBIT A-2**

## **Invalidity Claim Chart of U.S. Patent No. 6,580,122 Based on Korean Patent App. No. KR1997-010326 (“Yun”)**

Korean Patent App. No. KR1997-010326 to Yun, et al (“Yun”) was filed on March 25, 1997 and published on Nov. 5, 1998. Yun is prior art to U.S. Patent No. 6,580,122 (“the ’122 Patent”) at least under pre-AIA 35 U.S.C. § 102(b) because it was published more than one year before the earliest possible effective filing date of the ’122 Patent identified by Plaintiff in its infringement contentions, i.e., March 20, 2001. Plaintiff cannot assert an earlier invention date because Plaintiff failed to comply with paragraph 2 of the Court’s Order Governing Proceedings – Patent Case, including by failing to identify the “earliest date of invention” and failing to produce “all document evidencing conception and reduction to practice for each claimed invention.” Yun anticipates or renders obvious, alone or in combination with other prior art references, claims 1-3, 5-14, 16-25, 27-34 (“the Asserted Claims”) of the ’122 Patent under 35 U.S.C. §§ 102 and/or 103, as set forth in the chart below.

The citations provided in the chart below are only representative of the respective elements, rather than an exhaustive compilation of every aspect of the reference that is relevant to each limitation. To the extent Plaintiff alleges that this reference does not disclose any limitation in the Asserted Claims, either expressly or inherently, it would have been obvious to use the methods and systems described in the reference in combination with the other prior art identified in Defendants’ invalidity contentions, and/or in view of the knowledge of one of ordinary skill in the art at the relevant time about such systems and services.

Furthermore, to the extent Yun alone does not disclose or render obvious the Asserted Claims, it would have been obvious to a person having ordinary skill in the art at the time of the alleged invention to combine the teachings of Yun with the following references, as discussed in the chart below:

1. U.S. Patent No. 6,180,501 to Pey (“Pey”). Pey qualifies as prior art under at least pre-AIA §§ 102 (e). Pey was filed on Oct. 14, 1999 and issued on Jan. 30, 2001.
2. U.S. Patent No. 6,372,602 to Mitsuiki (“Mitsuiki”). Mitsuiki qualifies as prior art under at least pre-AIA §§ 102 (e). Mitsuiki was filed on May 15, 2000 and issued on April 16, 2002.
3. U.S. Patent No. 6,037,266 to Tao, et al. (“Tao”). Tao qualifies as prior art under at least pre-AIA §§ 102(a), 102(b), and 102(e). Tao was filed on Sep. 28, 1998 and issued on March 14, 2000.
4. U.S. Patent No. 6,429,062 to Rubin, et al. (“Rubin”). Rubin qualifies as prior art under at least pre-AIA §§ 102 (e). Rubin was filed on Sept. 20, 1999 and issued Aug. 6, 2002.

5. U.S. Patent No. 5,786,263 to Perera (“Perera”). Perera qualifies as prior art under at least pre-AIA §§ 102(a), 102(b), and 102(e). Perera was filed on April 4, 1995 and issued on July 28, 1998.
6. U.S. Patent No. 5,859,466 to Wada (“Wada”). Wada qualifies as prior art under at least pre-AIA §§ 102(a), 102(b), and 102(e). Wada was filed on June 6, 1996 and issued on Jan. 12, 1999.
7. Applicants’ Admitted Prior Art (“APA”) in the ’122 patent, disclosed in, among others, the Background of the Invention and Figures 1 and 2 of the ’122 patent.

With respect to the APA, “[a]dmissions in the specification regarding the prior art are binding on the patentee for purposes of a later inquiry into obviousness.” *PharmaStem Therapeutics, Inc. v. ViaCell, Inc.*, 491 F.3d 1342, 1362 (Fed. Cir. 2007); *see also In re Nomiya*, 509 F.2d 566, 570-71 (CCPA 1975) (“We see no reason why appellants’ representations in their application should not be accepted at face value as admissions that Figs. 1 and 2 may be considered ‘prior art’ for any purpose, including use as evidence of obviousness under § 103.”); *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1570 (Fed. Cir. 1988) (“A statement in a patent that something is in the prior art is binding on the applicant and patentee for determinations of anticipation and obviousness.”).

Nothing in this claim chart should be construed as an admission regarding infringement, either literally or under the doctrine of equivalents, or as an admission regarding Defendants’ understanding of the proper scope of the Asserted Claims. Given the ambiguities and other deficiencies in Plaintiff’s infringement contentions, the exemplary citations herein necessarily account for a variety of possible infringement arguments and claim constructions. Furthermore, the citations provided in these claim charts are intended to be only exemplary in nature. Defendants reserve the right to rely on additional citations or sources of evidence that also may be applicable. Further, this chart is subject to all reservations, objections, and disclaimers in Defendants’ Invalidity Contentions and any amendment, supplement, or modification thereof, which are incorporated herein by reference in their entirety.

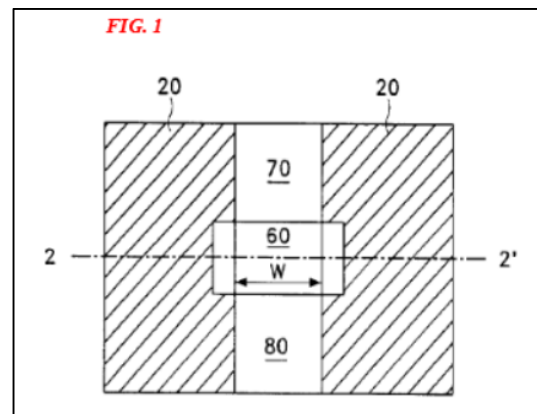
Several terms of the Asserted Claims are indefinite under 35 U.S.C. § 112, ¶ 2. For those claim limitations containing indefinite terms, SMIC’s offer herein of exemplary prior art disclosures is based solely on SMIC’s present understanding of the claim scope that IFT appears to be advocating in its infringement contentions, and nothing provided herein should be construed as an admission that a person of ordinary skill in the art would understand, with reasonable certainty, the scope of the claims.

To the extent the citations provided in the chart below suggest combining aspects of different embodiments from Yun, or modifying an aspect of one of Yun’s embodiments in view of a different embodiment, it would have been obvious to a person of ordinary skill in the art at the time of the alleged invention to combine or modify Yun’s embodiments as suggested. For example, Yun itself suggests that all of its embodiments are directed to the same goal. *See* Yun at pg. 2 (“that various changes and modifications

may be made without departing from the scope of the technical ideas of the present invention.”). Thus, per Yun’s own disclosure, combining or modifying Yun, in view of Yun, would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.

Claim	Prior Art Disclosure
[1pre] A transistor, comprising:	<p><b>To the extent the preamble of claim 1 is found to be limiting, Yun discloses a transistor. By way of non-limiting example, Yun discloses:</b></p> <p>“Method of manufacturing a transistor for a semiconductor device”  <i>See, e.g., Yun at Title.</i></p> <p>“Generally, transistors have predetermined channel width and length. Such a channel width is closely related to the electric current driving capability of the transistor. The wider the channel width becomes, the higher the electric current driving capability becomes. However, increasing the channel width causes a problem that the area increases in terms of chip integration. FIG. 1 is a plan view of a transistor according to the prior art. With reference to FIG. 1, it illustrates a plan view comprising an isolation region 20, a source 20 [sic] and a drain 80 of a transistor, and a gate 60 between the source 20 and the drain 80. Here, the width W of the channel formed at the lower part of the gate 60 is formed with the same width as that of the source 70 and the drain 80. Also, an increase in the channel width immediately results in an increase in the chip area. On another note, a vertical cross-sectional view in the 2-2’ direction of FIG. 1 is shown in FIG. 2. With reference to FIG. 2, it comprises: a channel region W directly formed on a silicon substrate 100 or formed inside a well formed on a silicon substrate 100; an isolation region 20 for isolating the device; a gate oxide film 40 formed on top of channel width W; and a gate electrode 60 formed thereon. When formed in a structure like this, a transistor is positioned on a surface that runs in parallel with the silicon substrate 100 and, when the channel width W is increased to increase the current-driving amount of a transistor, it immediately results in an increase in the size of the area. Since increasing the channel width immediately results in an increase in the size of the area, Patent No. 5,115,289 registered in the U.S. presents, as disclosed therein, a transistor structure to increase the channel width without increasing the area by vertically forming a part of the channel width to thereby solve the problem that made it difficult to increase the channel width. Although not illustrated, a manufacturing method to form such a transistor will now be briefly described here. After etching a</p>

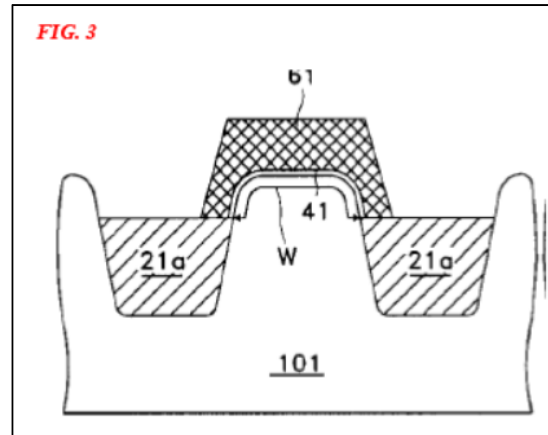
silicon substrate with the width of  $0.1\mu\text{m}$  and depth of  $1\mu\text{m}$ , the area where a channel will be formed is formed in such a way as to be wrapped up with a silicon oxide film  $\text{SiO}_2$  and a silicon nitride film  $\text{SiN}$ . Next, after isolating the channel region from the substrate by means of an oxidation process, the silicon nitride film and the silicon oxide film are removed; and the gate oxide film and the gate are formed. Then, a transistor is manufactured by means of a conventional transistor formation process such as forming a drain and a source, etc. Since the channel region is isolated from the silicon substrate by adopting a process of Silicon-On-Insulator (“SOI”), as described earlier, the channel region must be completely isolated from the substrate by “bird’s beak” during the oxidation process to form SOI. Accordingly, all the channel widths must be  $0.1\mu\text{m}$ . Consequently, it becomes difficult to form a large-size pattern. Also, even though all the patterns are formed at  $0.1\mu\text{m}$  or less, it causes a problem, among others, that the channel region is lifted during the oxidation process. In addition, a process of wrapping the channel region with a silicon nitride film is required to prevent oxidation of the channel region during the oxidation process for SOI, which causes a problem that the process becomes complicated.”  
*See, e.g., Yun at pg. 1-2.*



*See, e.g., Yun at Fig. 1; see also id. at Fig. 2.*

“It is the object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can improve the electric current driving capability of a transistor by increasing the channel width without increasing the chip area by vertically forming a part of the channel region.

	<p>It is another object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can eliminate the problem of lifting in increasing the channel width without increasing the chip area.</p> <p>It is yet another object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can improve the characteristics of the isolation region without introducing any additional process by increasing the channel width and, at the same time, adjusting the depth of the trench.</p> <p>It is yet another object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can increase the channel width and, at the same time, decrease the number of processes while forming an isolation region.”  <i>See e.g., Yun at pg. 2.</i></p> <p>“According to the technical ideas of the present invention to achieve the objects described above, the method of manufacturing a transistor for a semiconductor device comprises: a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process; a process of forming a well region on the silicon substrate by means of a conventional process of local ion implantation on the field; a process of partially etching a first oxide film inside the trench isolation by means of wet etching; a process of forming a second oxide film by performing an oxidation process; a process of ion implantation for optimization of the threshold voltage; a process of etching the second oxide film by means of wet etching; and a process of forming conventional gate oxide film, gate electrode, source, and drain.”  <i>See, e.g., Yun at pg. 2.</i></p> <p>“FIG. 3 is a vertical cross-sectional view illustrating a transistor according to one embodiment of the present invention. With reference to FIG. 3, isolation regions 21a are formed on a silicon substrate 101 and gates are formed between the isolation regions 21a. Here, a gate oxide film 41 is formed on the area where the silicon substrate is higher by a predetermined height relative to the upper part of the isolation region 21a; and a gate electrode 61 is formed on the upper part thereof. Accordingly, the channel width is raised by a predetermined height relative to the isolation region 21a and for a curve by as much as the height, thereby increasing the channel width. In doing so, there will not be any change in the chip area.”  <i>See, e.g., Yun at pg. 2.</i></p>
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See, e.g., Yun at Fig. 3.

“The present invention described above has an effect of increasing the channel width of a transistor without increasing the chip area and obtaining stable isolation characteristics by adjusting the trench depth as a result thereof.”

See, e.g., Yun at pg. 2.

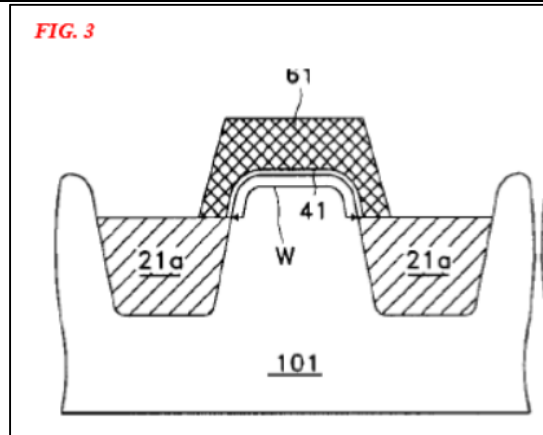
“FIGS. 4a to 4c are the cross-sectional views of the fabrication process, and as such they illustrate the sequence of manufacturing a transistor according to one embodiment of the present invention. With reference to FIG. 4a, a trench isolation region 21 is formed on a silicon substrate 101 by means of a conventional trench isolation process and a well region is formed on a conventional Local Implantation on Field **LIF** process. With reference to FIG. 4b, the oxide film 21a inside the trench isolation in the region desired to increase the channel width is etched by 10nm - 200nm by means of a wet etching process. Also, the sacrificial oxide film is sacrificed by 10nm - 30nm to allow the channel region in the angular part to become a more curved surface, thereby increasing the channel width **W**. Then, ion implantation to optimize the threshold voltage of the transistor is performed for  $3.0 \times 10^{11}/\text{cm}^2$  -  $2.0 \times 10^{12}/\text{cm}^2$  and, after that, the sacrificial film is etched by wet etching. Accordingly, it is shown that the oxide film **21a** filled in the isolation region is formed underneath the silicon substrate **101**. With reference to FIG. 4c, after the process described above is performed, a transistor is formed by means of a gate oxide **41** formation process and a source and drain formation process.

	<p>Meanwhile, by means of the processes described above, only a few processes are added to the conventional trench isolation process to increase the channel width of a transistor, which increases the electric current driving capability without increasing the area. Also, such a manufacturing process makes it possible to obtain stable isolation characteristics while increasing the channel width of a transistor by adjusting the depth of the oxide film in the trench. Meanwhile, the purpose of making the angular part of the channel become a more curved surface by means of the sacrificial oxide film is to mitigate the hump effect in the sub-threshold region during an operation of the transistor.”  <i>See, e.g., Yun at pg. 2; see also id. at Figs. 4a-c.</i></p> <p>“Claim 1  A method of manufacturing a transistor for a semiconductor device comprising:</p> <p>a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process;</p> <p>a process of forming a well region on the silicon substrate by means of a conventional process of localized ion implantation on the field;</p> <p>a process of partially etching a first oxide film inside the trench isolation by means of wet etching;</p> <p>a process of forming a second oxide film by performing an oxidation process;</p> <p>a process of ion implantation for optimization of the threshold voltage;</p> <p>a process of etching the second oxide film by means of wet etching; and</p> <p>a process of forming conventional gate oxide film, gate electrode, source, and drain.”  <i>See, e.g., Yun at Claim 1; see also id. at claims 2-4.</i></p>
[1a] a semiconducting substrate;	<b>Yun discloses a semiconducting substrate. By way of non-limiting example, Yun discloses:</b>



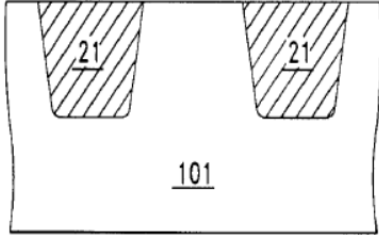
	<p>“Generally, transistors have predetermined channel width and length. Such a channel width is closely related to the electric current driving capability of the transistor. The wider the channel width becomes, the higher the electric current driving capability becomes. However, increasing the channel width causes a problem that the area increases in terms of chip integration. FIG. 1 is a plan view of a transistor according to the prior art. With reference to FIG. 1, it illustrates a plan view comprising an isolation region 20, a source 20 [sic] and a drain 80 of a transistor, and a gate 60 between the source 20 and the drain 80. Here, the width <b>W</b> of the channel formed at the lower part of the gate 60 is formed with the same width as that of the source 70 and the drain 80. Also, an increase in the channel width immediately results in an increase in the chip area. On another note, a vertical cross-sectional view in the 2-2' direction of FIG. 1 is shown in FIG. 2. With reference to FIG. 2, it comprises: a channel region <b>W</b> directly formed on a silicon substrate 100 or formed inside a well formed on a silicon substrate 100; an isolation region 20 for isolating the device; a gate oxide film 40 formed on top of channel width <b>W</b>; and a gate electrode 60 formed thereon. When formed in a structure like this, a transistor is positioned on a surface that runs in parallel with the silicon substrate 100 and, when the channel width <b>W</b> is increased to increase the current-driving amount of a transistor, it immediately results in an increase in the size of the area. Since increasing the channel width immediately results in an increase in the size of the area, Patent No. 5,115,289 registered in the U.S. presents, as disclosed therein, a transistor structure to increase the channel width without increasing the area by vertically forming a part of the channel width to thereby solve the problem that made it difficult to increase the channel width. Although not illustrated, a manufacturing method to form such a transistor will now be briefly described here. After etching a silicon substrate with the width of 0.1μm and depth of 1μm, the area where a channel will be formed is formed in such a way as to be wrapped up with a silicon oxide film <b>SiO<sub>2</sub></b> and a silicon nitride film <b>SiN</b>. Next, after isolating the channel region from the substrate by means of an oxidation process, the silicon nitride film and the silicon oxide film are removed; and the gate oxide film and the gate are formed. Then, a transistor is manufactured by means of a conventional transistor formation process such as forming a drain and a source, etc. Since the channel region is isolated from the silicon substrate by adopting a process of Silicon-On-Insulator (“SOI”), as described earlier, the channel region must be completely isolated from the substrate by “bird’s beak” during the oxidation process to form SOI. Accordingly, all the channel widths must be 0.1μm. Consequently, it becomes difficult to form a large-size pattern. Also, even though all the patterns are formed at 0.1μm or less, it causes a problem, among others, that the channel region is lifted during the oxidation process. In addition, a process of wrapping the channel region with a silicon nitride film is required to prevent oxidation of the channel region during the oxidation process for SOI, which causes a problem that the process becomes complicated.”</p>
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	<p><i>See, e.g., Yun at pg. 1-2; see also id. at Figs. 1-2.</i></p> <p>“According to the technical ideas of the present invention to achieve the objects described above, the method of manufacturing a transistor for a semiconductor device comprises: a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process; a process of forming a well region on the silicon substrate by means of a conventional process of local ion implantation on the field; a process of partially etching a first oxide film inside the trench isolation by means of wet etching; a process of forming a second oxide film by performing an oxidation process; a process of ion implantation for optimization of the threshold voltage; a process of etching the second oxide film by means of wet etching; and a process of forming conventional gate oxide film, gate electrode, source, and drain.”</p> <p><i>See, e.g., Yun at pg. 2.</i></p> <p>“FIG. 3 is a vertical cross-sectional view illustrating a transistor according to one embodiment of the present invention. With reference to FIG. 3, isolation regions 21a are formed on a silicon substrate 101 and gates are formed between the isolation regions 21a. Here, a gate oxide film 41 is formed on the area where the silicon substrate is higher by a predetermined height relative to the upper part of the isolation region 21a; and a gate electrode 61 is formed on the upper part thereof. Accordingly, the channel width is raised by a predetermined height relative to the isolation region 21a and for a curve by as much as the height, thereby increasing the channel width. In doing so, there will not be any change in the chip area.”</p> <p><i>See, e.g., Yun at pg. 2.</i></p>
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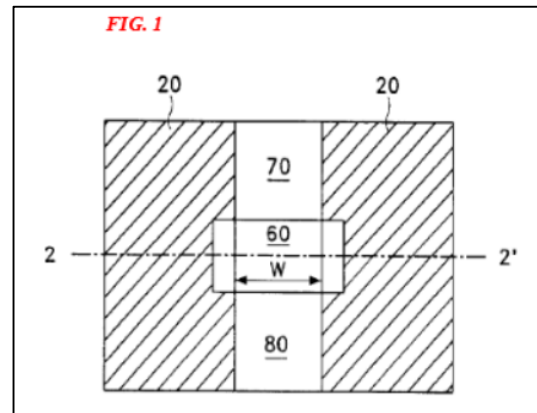
See, e.g., Yun at Fig. 3.

“FIGS. 4a to 4c are the cross-sectional views of the fabrication process, and as such they illustrate the sequence of manufacturing a transistor according to one embodiment of the present invention. With reference to FIG. 4a, a trench isolation region 21 is formed on a silicon substrate 101 by means of a conventional trench isolation process and a well region is formed on a conventional Local Implantation on Field **LIF** process. With reference to FIG. 4b, the oxide film 21a inside the trench isolation in the region desired to increase the channel width is etched by 10nm - 200nm by means of a wet etching process. Also, the sacrificial oxide film is sacrificed by 10nm - 30nm to allow the channel region in the angular part to become a more curved surface, thereby increasing the channel width **W**. Then, ion implantation to optimize the threshold voltage of the transistor is performed for  $3.0 \times 10^{11}/\text{cm}^2$  -  $2.0 \times 10^{12}/\text{cm}^2$  and, after that, the sacrificial film is etched by wet etching. Accordingly, it is shown that the oxide film **21a** filled in the isolation region is formed underneath the silicon substrate **101**. With reference to FIG. 4c, after the process described above is performed, a transistor is formed by means of a gate oxide **41** formation process and a source and drain formation process.

	<p style="text-align: center;"><b>FIG. 4</b></p>  <p><i>See e.g., Yun at Fig. 4a; see also id. at Figs. 4b-c.</i></p> <p><b>“Claim 1</b></p> <p>A method of manufacturing a transistor for a semiconductor device comprising:</p> <ul style="list-style-type: none"> <li>a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process;</li> <li>a process of forming a well region on the silicon substrate by means of a conventional process of localized ion implantation on the field;</li> <li>a process of partially etching a first oxide film inside the trench isolation by means of wet etching;</li> <li>a process of forming a second oxide film by performing an oxidation process;</li> <li>a process of ion implantation for optimization of the threshold voltage;</li> <li>a process of etching the second oxide film by means of wet etching; and</li> <li>a process of forming conventional gate oxide film, gate electrode, source, and drain.</li> </ul> <p><i>See, e.g., Yun at Claim 1.</i></p>
[1b] a recessed isolation structure formed in said	<p><b>Yun discloses a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove. By way of non-limiting example, Yun discloses:</b></p>

<p>substrate, said isolation structure defining a recess thereabove;</p>	<p>“Generally, transistors have predetermined channel width and length. Such a channel width is closely related to the electric current driving capability of the transistor. The wider the channel width becomes, the higher the electric current driving capability becomes. However, increasing the channel width causes a problem that the area increases in terms of chip integration. FIG. 1 is a plan view of a transistor according to the prior art. With reference to FIG. 1, it illustrates a plan view comprising an isolation region 20, a source 20 [sic] and a drain 80 of a transistor, and a gate 60 between the source 20 and the drain 80. Here, the width W of the channel formed at the lower part of the gate 60 is formed with the same width as that of the source 70 and the drain 80. Also, an increase in the channel width immediately results in an increase in the chip area. On another note, a vertical cross-sectional view in the 2-2' direction of FIG. 1 is shown in FIG. 2. With reference to FIG. 2, it comprises: a channel region W directly formed on a silicon substrate 100 or formed inside a well formed on a silicon substrate 100; an isolation region 20 for isolating the device; a gate oxide film 40 formed on top of channel width W; and a gate electrode 60 formed thereon. When formed in a structure like this, a transistor is positioned on a surface that runs in parallel with the silicon substrate 100 and, when the channel width W is increased to increase the current-driving amount of a transistor, it immediately results in an increase in the size of the area. Since increasing the channel width immediately results in an increase in the size of the area, Patent No. 5,115,289 registered in the U.S. presents, as disclosed therein, a transistor structure to increase the channel width without increasing the area by vertically forming a part of the channel width to thereby solve the problem that made it difficult to increase the channel width. Although not illustrated, a manufacturing method to form such a transistor will now be briefly described here. After etching a silicon substrate with the width of 0.1μm and depth of 1μm, the area where a channel will be formed is formed in such a way as to be wrapped up with a silicon oxide film SiO<sub>2</sub> and a silicon nitride film SiN. Next, after isolating the channel region from the substrate by means of an oxidation process, the silicon nitride film and the silicon oxide film are removed; and the gate oxide film and the gate are formed. Then, a transistor is manufactured by means of a conventional transistor formation process such as forming a drain and a source, etc. Since the channel region is isolated from the silicon substrate by adopting a process of Silicon-On-Insulator (“SOI”), as described earlier, the channel region must be completely isolated from the substrate by “bird’s beak” during the oxidation process to form SOI. Accordingly, all the channel widths must be 0.1μm. Consequently, it becomes difficult to form a large-size pattern. Also, even though all the patterns are formed at 0.1μm or less, it causes a problem, among others, that the channel region is lifted during the oxidation process. In addition, a process of wrapping</p>
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the channel region with a silicon nitride film is required to prevent oxidation of the channel region during the oxidation process for SOI, which causes a problem that the process becomes complicated.”  
*See, e.g., Yun at pg. 1-2.*

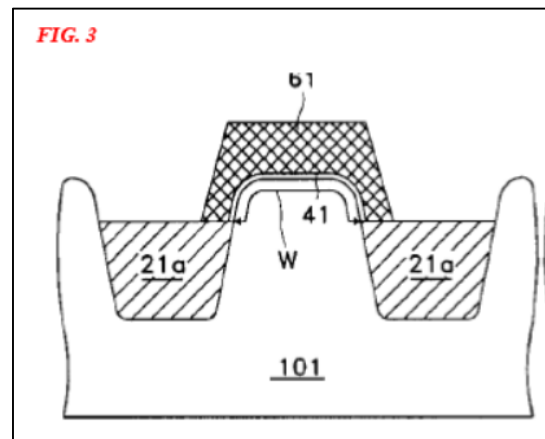


*See, e.g., Yun at Fig. 1; see also id. at Fig. 2.*

“It is yet another object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can improve the characteristics of the isolation region without introducing any additional process by increasing the channel width and, at the same time, adjusting the depth of the trench.”  
*See, e.g., Yun at pg. 2.*

“According to the technical ideas of the present invention to achieve the objects described above, the method of manufacturing a transistor for a semiconductor device comprises: a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process; a process of forming a well region on the silicon substrate by means of a conventional process of local ion implantation on the field; a process of partially etching a first oxide film inside the trench isolation by means of wet etching; a process of forming a second oxide film by performing an oxidation process; a process of ion implantation for optimization of the threshold voltage; a process of etching the second oxide film by means of wet etching; and a process of forming conventional gate oxide film, gate electrode, source, and drain.”  
*See, e.g., Yun at pg. 2.*

“FIG. 3 is a vertical cross-sectional view illustrating a transistor according to one embodiment of the present invention. With reference to FIG. 3, isolation regions 21a are formed on a silicon substrate 101 and gates are formed between the isolation regions 21a. Here, a gate oxide film 41 is formed on the area where the silicon substrate is higher by a predetermined height relative to the upper part of the isolation region 21a; and a gate electrode 61 is formed on the upper part thereof. Accordingly, the channel width is raised by a predetermined height relative to the isolation region 21a and for a curve by as much as the height, thereby increasing the channel width. In doing so, there will not be any change in the chip area.”  
*See, e.g., Yun at pg. 2.*

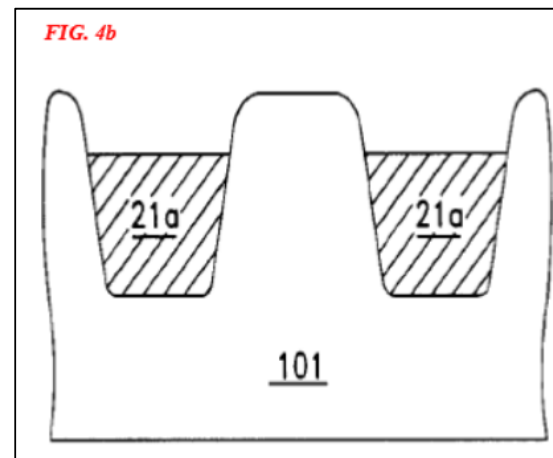


*See, e.g., Yun at Fig. 3.*

“FIGS. 4a to 4c are the cross-sectional views of the fabrication process, and as such they illustrate the sequence of manufacturing a transistor according to one embodiment of the present invention. With reference to FIG. 4a, a trench isolation region 21 is formed on a silicon substrate 101 by means of a conventional trench isolation process and a well region is formed on a conventional Local Implantation on Field LIF process. With reference to FIG. 4b, the oxide film 21a inside the trench isolation in the region desired to increase the channel width is etched by 10nm - 200nm by means of a wet etching process. Also, the sacrificial oxide film is sacrificed by 10nm - 30nm to allow the channel region in the angular part to become a more curved surface, thereby increasing the channel width W. Then, ion implantation to optimize the threshold voltage of the transistor is performed for  $3.0 \times 10^{11}/\text{cm}^2$  -  $2.0 \times$

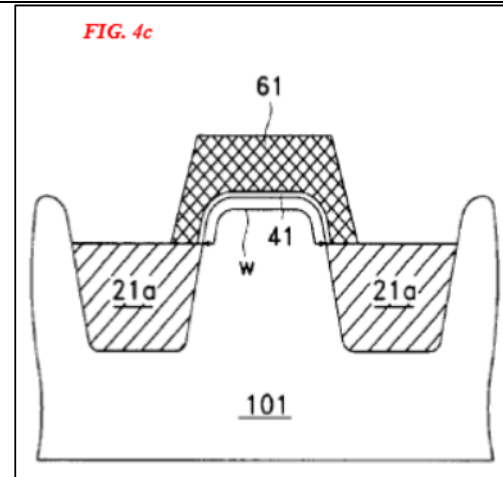
$10^{12}/\text{cm}^2$  and, after that, the sacrificial film is etched by wet etching. Accordingly, it is shown that the oxide film 21a filled in the isolation region is formed underneath the silicon substrate 101. With reference to FIG. 4c, after the process described above is performed, a transistor is formed by means of a gate oxide 41 formation process and a source and drain formation process.”

*See, e.g., Yun at pg. 2.*



*See, e.g., Yun at Fig. 4b.*





*See, e.g., Yun at Fig. 4c, see also id. at Fig. 4a.*

“Meanwhile, by means of the processes described above, only a few processes are added to the conventional trench isolation process to increase the channel width of a transistor, which increases the electric current driving capability without increasing the area. Also, such a manufacturing process makes it possible to obtain stable isolation characteristics while increasing the channel width of a transistor by adjusting the depth of the oxide film in the trench. Meanwhile, the purpose of making the angular part of the channel become a more curved surface by means of the sacrificial oxide film is to mitigate the hump effect in the sub-threshold region during an operation of the transistor.”

*See, e.g., Yun at pg. 2.*

“The present invention described above has an effect of increasing the channel width of a transistor without increasing the chip area and obtaining stable isolation characteristics by adjusting the trench depth as a result thereof.”

*See, e.g., Yun at pg. 2.*

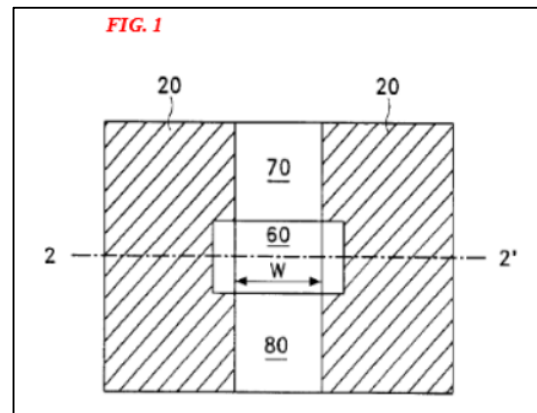
“Claim 1

A method of manufacturing a transistor for a semiconductor device comprising:

	<p>a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process;</p> <p>a process of forming a well region on the silicon substrate by means of a conventional process of localized ion implantation on the field;</p> <p>a process of partially etching a first oxide film inside the trench isolation by means of wet etching;</p> <p>a process of forming a second oxide film by performing an oxidation process;</p> <p>a process of ion implantation for optimization of the threshold voltage;</p> <p>a process of etching the second oxide film by means of wet etching; and</p> <p>a process of forming conventional gate oxide film, gate electrode, source, and drain.”  <i>See, e.g., Yun at claim 1.</i></p> <p>“The present invention relates to a semiconductor device. In a method of manufacturing a transistor for a semiconductor device, the summary of the present invention comprises: a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process; a process of forming a well region on the silicon substrate by means of a conventional process of local ion implantation on the field; a process of partially etching a first oxide film inside the trench isolation by means of wet etching; a process of forming a second oxide film by performing an oxidation process; a process of ion implantation for optimization of the threshold voltage; a process of etching the second oxide film by means of wet etching; and a process of forming conventional gate oxide film, gate electrode, source, and drain.”  <i>See, e.g., Yun at Abstract.</i></p>
[1c] a gate electrode and a gate insulation layer formed above said substrate, a portion of said gate electrode and said gate	<p><b>Yun discloses a gate electrode and a gate insulation layer formed above said substrate, a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure. By way of non-limiting example, Yun discloses:</b></p>

insulation layer extending into said recess above said recessed isolation structure; and	<p>“Generally, transistors have predetermined channel width and length. Such a channel width is closely related to the electric current driving capability of the transistor. The wider the channel width becomes, the higher the electric current driving capability becomes. However, increasing the channel width causes a problem that the area increases in terms of chip integration. FIG. 1 is a plan view of a transistor according to the prior art. With reference to FIG. 1, it illustrates a plan view comprising an isolation region 20, a source 20 [sic] and a drain 80 of a transistor, and a gate 60 between the source 20 and the drain 80. Here, the width W of the channel formed at the lower part of the gate 60 is formed with the same width as that of the source 70 and the drain 80. Also, an increase in the channel width immediately results in an increase in the chip area. On another note, a vertical cross-sectional view in the 2-2' direction of FIG. 1 is shown in FIG. 2. With reference to FIG. 2, it comprises: a channel region W directly formed on a silicon substrate 100 or formed inside a well formed on a silicon substrate 100; an isolation region 20 for isolating the device; a gate oxide film 40 formed on top of channel width W; and a gate electrode 60 formed thereon. When formed in a structure like this, a transistor is positioned on a surface that runs in parallel with the silicon substrate 100 and, when the channel width W is increased to increase the current-driving amount of a transistor, it immediately results in an increase in the size of the area. Since increasing the channel width immediately results in an increase in the size of the area, Patent No. 5,115,289 registered in the U.S. presents, as disclosed therein, a transistor structure to increase the channel width without increasing the area by vertically forming a part of the channel width to thereby solve the problem that made it difficult to increase the channel width. Although not illustrated, a manufacturing method to form such a transistor will now be briefly described here. After etching a silicon substrate with the width of 0.1μm and depth of 1μm, the area where a channel will be formed is formed in such a way as to be wrapped up with a silicon oxide film SiO<sub>2</sub> and a silicon nitride film SiN. Next, after isolating the channel region from the substrate by means of an oxidation process, the silicon nitride film and the silicon oxide film are removed; and the gate oxide film and the gate are formed. Then, a transistor is manufactured by means of a conventional transistor formation process such as forming a drain and a source, etc. Since the channel region is isolated from the silicon substrate by adopting a process of Silicon-On-Insulator (“SOI”), as described earlier, the channel region must be completely isolated from the substrate by “bird’s beak” during the oxidation process to form SOI. Accordingly, all the channel widths must be 0.1μm. Consequently, it becomes difficult to form a large-size pattern. Also, even though all the patterns are formed at 0.1μm or less, it causes a problem, among others, that the channel region is lifted during the oxidation process. In addition, a process of wrapping the channel region with a silicon nitride film is required to prevent oxidation of the channel region during the oxidation process for SOI, which causes a problem that the process becomes complicated.”</p>
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See, e.g., Yun at pg. 1-2.



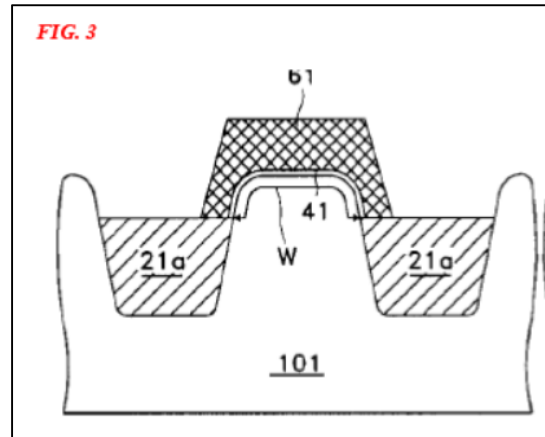
See, e.g., Yun at Fig. 1.

“According to the technical ideas of the present invention to achieve the objects described above, the method of manufacturing a transistor for a semiconductor device comprises: a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process; a process of forming a well region on the silicon substrate by means of a conventional process of local ion implantation on the field; a process of partially etching a first oxide film inside the trench isolation by means of wet etching; a process of forming a second oxide film by performing an oxidation process; a process of ion implantation for optimization of the threshold voltage; a process of etching the second oxide film by means of wet etching; and a process of forming conventional gate oxide film, gate electrode, source, and drain.”

See, e.g., Yun at pg. 2.

“FIG. 3 is a vertical cross-sectional view illustrating a transistor according to one embodiment of the present invention. With reference to FIG. 3, isolation regions 21a are formed on a silicon substrate 101 and gates are formed between the isolation regions 21a. Here, a gate oxide film 41 is formed on the area where the silicon substrate is higher by a predetermined height relative to the upper part of the isolation region 21a; and a gate electrode 61 is formed on the upper part thereof. Accordingly, the channel width is

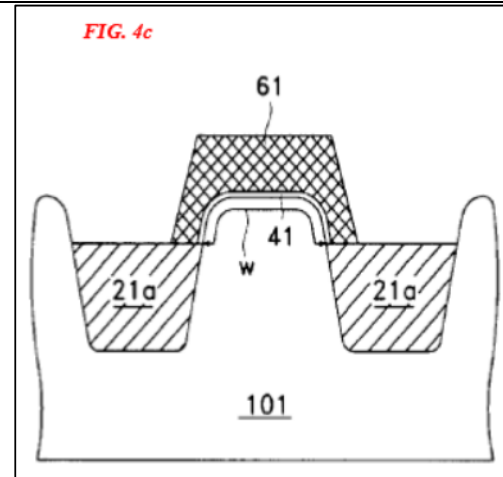
raised by a predetermined height relative to the isolation region 21a and for a curve by as much as the height, thereby increasing the channel width. In doing so, there will not be any change in the chip area.”  
*See, e.g., Yun at pg. 2.*



*See, e.g., Yun at Fig. 3.*

“FIGS. 4a to 4c are the cross-sectional views of the fabrication process, and as such they illustrate the sequence of manufacturing a transistor according to one embodiment of the present invention. With reference to FIG. 4a, a trench isolation region 21 is formed on a silicon substrate 101 by means of a conventional trench isolation process and a well region is formed on a conventional Local Implantation on Field LIF process. With reference to FIG. 4b, the oxide film 21a inside the trench isolation in the region desired to increase the channel width is etched by 10nm - 200nm by means of a wet etching process. Also, the sacrificial oxide film is sacrificed by 10nm - 30nm to allow the channel region in the angular part to become a more curved surface, thereby increasing the channel width W. Then, ion implantation to optimize the threshold voltage of the transistor is performed for  $3.0 \times 10^{11}/\text{cm}^2$  -  $2.0 \times 10^{12}/\text{cm}^2$  and, after that, the sacrificial film is etched by wet etching. Accordingly, it is shown that the oxide film 21a filled in the isolation region is formed underneath the silicon substrate 101. With reference to FIG. 4c, after the process described above is performed, a transistor is formed by means of a gate oxide 41 formation process and a source and drain formation process.”

*See, e.g., Yun at pg. 2.*



See, e.g., Yun at Fig. 4c; see also *id.* at Figs. 4a-b.

“Claim 1

A method of manufacturing a transistor for a semiconductor device comprising:

a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process;

a process of forming a well region on the silicon substrate by means of a conventional process of localized ion implantation on the field;

a process of partially etching a first oxide film inside the trench isolation by means of wet etching;

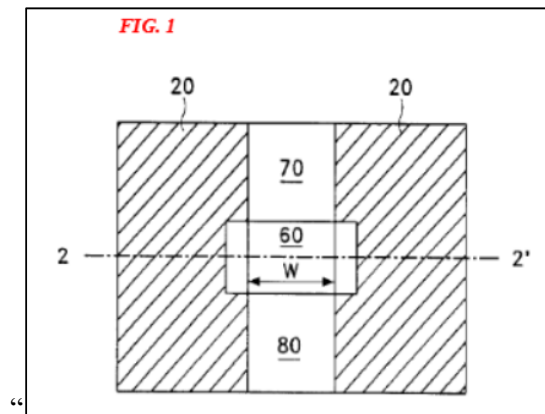
a process of forming a second oxide film by performing an oxidation process;

a process of ion implantation for optimization of the threshold voltage;

a process of etching the second oxide film by means of wet etching; and

	<p>a process of forming conventional gate oxide film, gate electrode, source, and drain.”  <i>See, e.g., Yun at Claim 1.</i></p> <p>“The present invention relates to a semiconductor device. In a method of manufacturing a transistor for a semiconductor device, the summary of the present invention comprises: a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process; a process of forming a well region on the silicon substrate by means of a conventional process of local ion implantation on the field; a process of partially etching a first oxide film inside the trench isolation by means of wet etching; a process of forming a second oxide film by performing an oxidation process; a process of ion implantation for optimization of the threshold voltage; a process of etching the second oxide film by means of wet etching; and a process of forming conventional gate oxide film, gate electrode, source, and drain.”  <i>See, e.g., Yun at abstract.</i></p>
[1d] a source region and a drain region formed in said substrate.	<p><b>Yun discloses a source region and a drain region formed in said substrate. By way of non-limiting example, Yun discloses:</b></p> <p>“Generally, transistors have predetermined channel width and length. Such a channel width is closely related to the electric current driving capability of the transistor. The wider the channel width becomes, the higher the electric current driving capability becomes. However, increasing the channel width causes a problem that the area increases in terms of chip integration. FIG. 1 is a plan view of a transistor according to the prior art. With reference to FIG. 1, it illustrates a plan view comprising an isolation region 20, a source 20 [sic] and a drain 80 of a transistor, and a gate 60 between the source 20 and the drain 80. Here, the width W of the channel formed at the lower part of the gate 60 is formed with the same width as that of the source 70 and the drain 80. Also, an increase in the channel width immediately results in an increase in the chip area. On another note, a vertical cross-sectional view in the 2-2' direction of FIG. 1 is shown in FIG. 2. With reference to FIG. 2, it comprises: a channel region W directly formed on a silicon substrate 100 or formed inside a well formed on a silicon substrate 100; an isolation region 20 for isolating the device; a gate oxide film 40 formed on top of channel width W; and a gate electrode 60 formed thereon. When formed in a structure like this, a transistor is positioned on a surface that runs in parallel with the silicon substrate 100 and, when the channel width W is increased to increase the current-driving amount of a transistor, it immediately results in an increase in the size of the area. Since increasing the channel width immediately results in an increase in the size of the area, Patent</p>

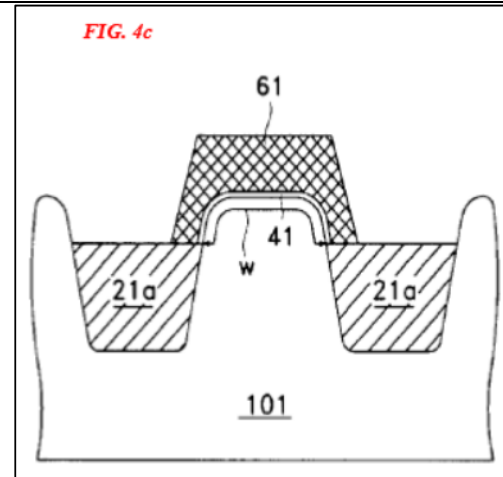
No. 5,115,289 registered in the U.S. presents, as disclosed therein, a transistor structure to increase the channel width without increasing the area by vertically forming a part of the channel width to thereby solve the problem that made it difficult to increase the channel width. Although not illustrated, a manufacturing method to form such a transistor will now be briefly described here. After etching a silicon substrate with the width of  $0.1\mu\text{m}$  and depth of  $1\mu\text{m}$ , the area where a channel will be formed is formed in such a way as to be wrapped up with a silicon oxide film  $\text{SiO}_2$  and a silicon nitride film  $\text{SiN}$ . Next, after isolating the channel region from the substrate by means of an oxidation process, the silicon nitride film and the silicon oxide film are removed; and the gate oxide film and the gate are formed. Then, a transistor is manufactured by means of a conventional transistor formation process such as forming a drain and a source, etc. Since the channel region is isolated from the silicon substrate by adopting a process of Silicon-On-Insulator (“SOI”), as described earlier, the channel region must be completely isolated from the substrate by “bird’s beak” during the oxidation process to form SOI. Accordingly, all the channel widths must be  $0.1\mu\text{m}$ . Consequently, it becomes difficult to form a large-size pattern. Also, even though all the patterns are formed at  $0.1\mu\text{m}$  or less, it causes a problem, among others, that the channel region is lifted during the oxidation process. In addition, a process of wrapping the channel region with a silicon nitride film is required to prevent oxidation of the channel region during the oxidation process for SOI, which causes a problem that the process becomes complicated.”  
*See, e.g., Yun at pg. 1-2.*



*See, e.g., Yun at Fig. 1; see also id. at Fig. 2.*



	<p>“According to the technical ideas of the present invention to achieve the objects described above, the method of manufacturing a transistor for a semiconductor device comprises: a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process; a process of forming a well region on the silicon substrate by means of a conventional process of local ion implantation on the field; a process of partially etching a first oxide film inside the trench isolation by means of wet etching; a process of forming a second oxide film by performing an oxidation process; a process of ion implantation for optimization of the threshold voltage; a process of etching the second oxide film by means of wet etching; and a process of forming conventional gate oxide film, gate electrode, source, and drain.”  <i>See, e.g., Yun at pg. 2.</i></p> <p>“FIGS. <b>4a</b> to <b>4c</b> are the cross-sectional views of the fabrication process, and as such they illustrate the sequence of manufacturing a transistor according to one embodiment of the present invention. With reference to FIG. <b>4a</b>, a trench isolation region 21 is formed on a silicon substrate 101 by means of a conventional trench isolation process and a well region is formed on a conventional Local Implantation on Field <b>LIF</b> process. With reference to FIG. <b>4b</b>, the oxide film 21a inside the trench isolation in the region desired to increase the channel width is etched by 10nm - 200nm by means of a wet etching process. Also, the sacrificial oxide film is sacrificed by 10nm - 30nm to allow the channel region in the angular part to become a more curved surface, thereby increasing the channel width <b>W</b>. Then, ion implantation to optimize the threshold voltage of the transistor is performed for <math>3.0 \times 10^{11}/\text{cm}^2</math> - <math>2.0 \times 10^{12}/\text{cm}^2</math> and, after that, the sacrificial film is etched by wet etching. Accordingly, it is shown that the oxide film <b>21a</b> filled in the isolation region is formed underneath the silicon substrate <b>101</b>. With reference to FIG. <b>4c</b>, after the process described above is performed, a transistor is formed by means of a gate oxide <b>41</b> formation process and a source and drain formation process.”  <i>See, e.g., Yun at pg. 2.</i></p>
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See, e.g., Yun at Fig. 4c; see also *id.* at Figs. 4a-b.

“Claim 1

A method of manufacturing a transistor for a semiconductor device comprising:

a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process;

a process of forming a well region on the silicon substrate by means of a conventional process of localized ion implantation on the field;

a process of partially etching a first oxide film inside the trench isolation by means of wet etching;

a process of forming a second oxide film by performing an oxidation process;

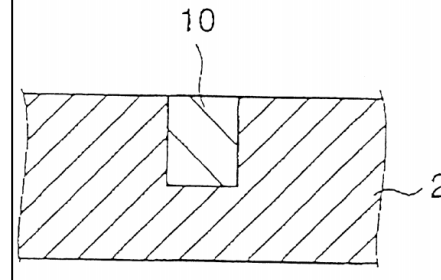
a process of ion implantation for optimization of the threshold voltage;

a process of etching the second oxide film by means of wet etching; and

	<p>a process of forming conventional gate oxide film, gate electrode, source, and drain.”  <i>See, e.g., Yun at Claim 1.</i></p> <p>“FIG. 3 is a vertical cross-sectional view illustrating a transistor according to one embodiment of the present invention. With reference to FIG. 3, isolation regions 21a are formed on a silicon substrate 101 and gates are formed between the isolation regions 21a. Here, a gate oxide film 41 is formed on the area where the silicon substrate is higher by a predetermined height relative to the upper part of the isolation region 21a; and a gate electrode 61 is formed on the upper part thereof. Accordingly, the channel width is raised by a predetermined height relative to the isolation region 21a and for a curve by as much as the height, thereby increasing the channel width. In doing so, there will not be any change in the chip area.”  <i>See, e.g., Yun at pg. 2.</i></p> <div data-bbox="997 721 1549 1154"> </div> <p><i>See, e.g., Yun at Fig. 3.</i></p>
<p>[2] The transistor of claim 1, wherein said semiconducting substrate is comprised of silicon.</p>	<p><b>Yun discloses the transistor of claim 1, wherein said semiconducting substrate is comprised of silicon. By way of non-limiting example, Yun discloses:</b></p> <p><i>See disclosure for claim 1(a). This disclosure is incorporated by reference herein.</i></p>

<p>[3] The transistor of claim 1, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.</p>	<p><b>Yun discloses the transistor of claim 1, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride. By way of non-limiting example, Yun discloses:</b></p> <p><i>See</i> disclosure for claim 1(b). This disclosure is incorporated by reference herein.</p>
<p>[5] The transistor of claim 1, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.</p>	<p><b>In the event it is determined that Yun does not disclose this element, it would have been obvious to modify Yun to include this element based either on the knowledge of a person of skill in the art and/or the teaching of other references. For example, Mitsuiki, Wada, or Perera teach this element:</b></p> <p>“A first embodiment according to the present invention will be described in detail with reference to the drawings. FIG. 4 is a fragmentary cross sectional elevation view illustrative of a shallow trench isolation in a shallow trench in a semiconductor substrate, wherein a shallow trench isolation is free of any divots, voids or cavities formed in a novel method of forming the shallow trench isolation structure in accordance with the present invention. A silicon substrate 2 has a shallow trench which has a width in the range of 0.1-1.0 micrometer and a depth in the range of 200-600 nanometers. A trench isolation oxide film 10 is filled within the shallow trench of the silicon substrate 2. The top of the trench isolation oxide film 10 and the top surface of the silicon substrate 2 are exactly planarized. The trench isolation oxide film 10 free of any divots and voids or cavities.”</p> <p><i>See, e.g., Mitsuiki at 3:51-65.</i></p>

FIG. 4

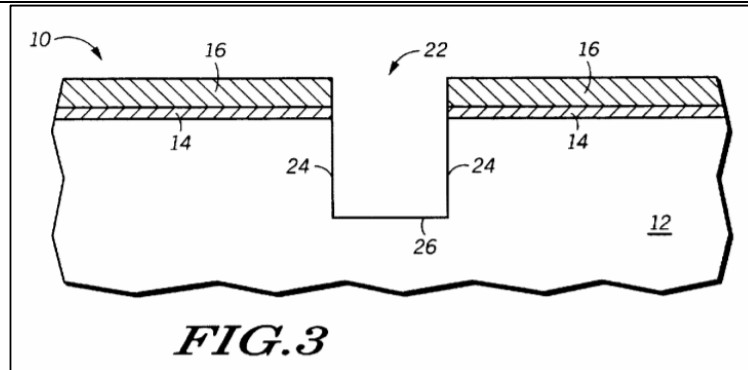


*See, e.g., Mitsuiki at Fig. 4.*

**By way of further example, Perera also teaches this element:**

“In FIG. 3, first portion 20 of semiconductor substrate 12 is then anisotropically etched using standard etching techniques to form a trench 22 having a trench sidewall 24 and a trench bottom 26. After trench 22 has been formed, photoresist mask 18 is removed using standard photoresist stripping techniques. Trench 22 preferably has a trench width ranging from about 200 to 600 nanometers and a trench depth ranging from about 200 to 1000 nanometers.”

*See, e.g., Perera at 2:28-35; see also id. at 3:20-4:2.*

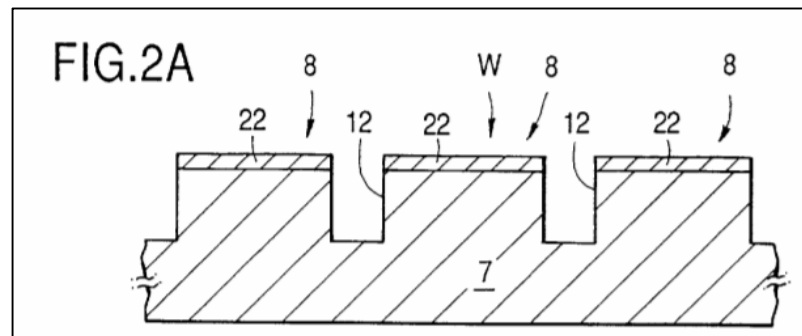


*See, e.g., Perera at Fig. 3; see also id. at Fig. 7.*

**By way of further example, Wada also teaches this element:**

“First, as shown in FIG. 2A, the cavities for the trenches 12 are fabricated on the upper surface of a wafer W (includes a substrate 7 of a P-type monocrystalline silicon having a specific resistance  $3 \sim 4$  ohm·cm) by process of etching through an etching mask of a SiO<sub>2</sub> film 22, for protecting those active regions 8 for fabricating the N-channel MOS transistor but exposing those regions for forming the trenches 12. The process of forming the trenches 12 used in this embodiment is a dry etching process using gaseous chlorine to make a cavity measuring  $0.5 \sim 1.5$   $\mu\text{m}$  in depth and  $0.2 \sim 0.5$   $\mu\text{m}$  in width.”

*See, e.g., Wada at 4:41-51.*



*See, e.g., Wada at Fig. 2A; see also id. at Fig. 6A.*

	<p>“The dimensions quoted in the embodiments are meant to be examples, and they are not limited to the exact dimensions quoted. For example, it is permissible to have a range of dimensions such as: the trench widths may range from 80 nm~several mm; the depth of the trench may be made deeper by up to 10 <math>\mu</math>m than the depth of the diffusion layers for source and drain; the film thickness of the field-shield insulator film may range 5~200 nm; and the film thickness of the polycrystalline silicon film may range 40~800 nm.”  <i>See, e.g., Wada at 7:54-62.</i></p> <p>“The process of forming the trenches 113 is a dry etching process using gaseous chlorine to make cavities measuring 0.5~1.5 <math>\mu</math>m in depth and 0.2~0.5 <math>\mu</math>m in width. As illustrated in FIG. 6A, the etching process is carried out under conditions to favor etching on the side-wall surface of the cavities so that the width A of the trench 113 can be made to include an undercutting dimension C of about 0.02~0.2 <math>\mu</math>m more than the opening dimension B on the SiO<sub>2</sub> film 117. This undercut structure facilitates making of the subsequent fabrication of insulative isolation with trenches 113 to surround the active regions 109.”  <i>See, e.g., Wada at 9:66-10:9.</i></p> <p><b>Furthermore, this element is obvious based on the knowledge of a person of ordinary skill in the art.</b></p> <p>A person of ordinary skill in the art would have been motivated to incorporate this element from Mitsuiki, Perera, Wada, or their own knowledge into Yun as a means “for further improvements in scaling down and isolation property” in ultra large scale integrated circuits. <i>See, e.g. Mitsuiki at 1:14-16; Perera at 1:7-9; Wada at 1:9-13.</i> A person of ordinary skill in the art would have a reasonable expectation of success in incorporating this limitation as the mechanisms for doing so are disclosed in references themselves. <i>See, e.g., Yun at pg. 2.</i> (“It is yet another object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can increase the channel width and, at the same time, decrease the number of processes while forming an isolation region.”).</p> <p>In addition to being a combination taught directly by these references, such a combination would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a</p>
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	known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.																														
[6] The transistor of claim 1, wherein said gate electrode is comprised of polysilicon.	<p><b>In the event it is determined that Yun does not disclose this element, it would have been obvious to modify Yun to include this element based either on the knowledge of a person of skill in the art and/or the teaching of other references. For example, Tao teaches this element:</b></p> <p>“The polysilicon layer can is a poly-crystalline layer of silicon that is deposited on the gate oxide 14. The polysilicon layer can be uses as a silicon gate or can be used for interconnecting interconnections between devices. The polysilicon layer 18 preferably has a thickness in a range of between about 1000 and 3000 Å.”</p> <p><i>See, e.g.,</i> Tao at 6:8-13.</p> <div><p>TABLE</p><table><tr><th>Element No.</th><th>generic name</th><th>preferred examples</th><th>Preferred Parameters (thickness, doping, etc . . . )</th><th>Other alternate examples</th></tr><tr><td>14</td><td>gate oxide layer</td><td>oxide</td><td>Thickness = 20 to 100 Å</td><td>nitrided oxide</td></tr><tr><td>20</td><td>polysilicon layer</td><td>Polysilicon or amorphous silicon</td><td>Th = 1000 to 3000 Å = doped or undoped</td><td>WSi<sub>x</sub> over polysilicon</td></tr><tr><td>22</td><td>a hard mask layer</td><td>Oxide</td><td>200 to 3000 Å</td><td>nitride or oxynitride</td></tr><tr><td>26</td><td>bottom anti-reflective coating (BARC) layer</td><td>organic</td><td>Thickness = 500 to 2000 Å</td><td></td></tr><tr><td>30</td><td>resist layer</td><td>DUV photoresist</td><td>6000 to 13000 Å</td><td>i-line</td></tr></table></div> <p><i>See, e.g.,</i> Tao at 5:55.</p> <p><b>Furthermore, this element is obvious based on the knowledge of a person of ordinary skill in the art.</b></p> <p>A person of ordinary skill in the art would have been motivated to incorporate this element from Tao or their own knowledge into Yun because Tao is focused on fabricating polysilicon gates (“This invention relates generally to fabrication of polysilicon gates in a semiconductor device”) <i>See, e.g.</i> Tao 1:7-8. A person of ordinary skill in the art would have a reasonable expectation of success in incorporating this</p>	Element No.	generic name	preferred examples	Preferred Parameters (thickness, doping, etc . . . )	Other alternate examples	14	gate oxide layer	oxide	Thickness = 20 to 100 Å	nitrided oxide	20	polysilicon layer	Polysilicon or amorphous silicon	Th = 1000 to 3000 Å = doped or undoped	WSi <sub>x</sub> over polysilicon	22	a hard mask layer	Oxide	200 to 3000 Å	nitride or oxynitride	26	bottom anti-reflective coating (BARC) layer	organic	Thickness = 500 to 2000 Å		30	resist layer	DUV photoresist	6000 to 13000 Å	i-line
Element No.	generic name	preferred examples	Preferred Parameters (thickness, doping, etc . . . )	Other alternate examples																											
14	gate oxide layer	oxide	Thickness = 20 to 100 Å	nitrided oxide																											
20	polysilicon layer	Polysilicon or amorphous silicon	Th = 1000 to 3000 Å = doped or undoped	WSi <sub>x</sub> over polysilicon																											
22	a hard mask layer	Oxide	200 to 3000 Å	nitride or oxynitride																											
26	bottom anti-reflective coating (BARC) layer	organic	Thickness = 500 to 2000 Å																												
30	resist layer	DUV photoresist	6000 to 13000 Å	i-line																											



	<p>limitation as the mechanisms for doing so are disclosed in references themselves. <i>See, e.g.</i>, Yun at pg. 2 (“a process of forming conventional gate oxide film, gate electrode, source, and drain.”).</p> <p>In addition to being a combination taught directly by these references, such a combination would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.</p>
<p>[7] The transistor of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.</p>	<p><b>Yun discloses the transistor of claim 1, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride. By way of non-limiting example, Yun discloses:</b></p> <p><i>See</i> disclosure for claim 1(c). This disclosure is incorporated by reference herein.</p> <p><b>In the event it is determined that Yun does not disclose this element, it would have been obvious to modify Yun to include this element based either on the knowledge of a person of skill in the art and/or the teaching of other references. For example, Pey teaches this element:</b></p> <p>“Referring to FIG. 1, an overlying stack consisting of a gate oxide layer 6, an overlying first polysilicon layer 8, and a still further overlying silicon nitride layer 10 is then formed. Said gate oxide 6 is a thin thermal oxide, with a typical thickness range of about 25 to 30 angstroms, that is subsequently nitrided. A preferred gate oxide thickness of about 40 angstroms is grown in a dry followed by a partial wet ambient, at a typical temperature range of about 800 to 1000 degrees centigrade for a duration of about 1 to 3 minutes. Said subsequent nitridation process can be performed at a temperature range of about 900 to 1000 degrees centigrade, in a nitrous oxide (N<sub>2</sub>O) ambient, using an RTA.”</p> <p><i>See, e.g.</i>, Pey at 4:56-67.</p>

	<div data-bbox="961 311 1581 573" data-label="Image"> <p>FIG. 1</p> </div> <p>See, e.g., Pey at Fig. 1.</p> <p><b>Furthermore, this element is obvious based on the knowledge of a person of ordinary skill in the art.</b></p> <p>A person of ordinary skill in the art would have been motivated to incorporate this element from Pey or their own knowledge into Yun because in typical device structures, “a gate oxide layer and an overlying polysilicon layer are first patterned into gate regions.” See, e.g. Pey at 1:44-46. A person of ordinary skill in the art would have a reasonable expectation of success in incorporating this limitation as the mechanisms for doing so are disclosed in references themselves. See, e.g., Yun at pg. 2 (“a process of forming conventional gate oxide film, gate electrode, source, and drain.”).</p> <p>In addition to being a combination taught directly by these references, such a combination would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.</p>
<p>[8] The transistor of claim 1, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.</p>	<p><b>In the event it is determined that Yun does not disclose this element, it would have been obvious to modify Yun to include this element based either on the knowledge of a person of skill in the art and/or the teaching of other references. For example, Tao teaches this element:</b></p> <p>“The polysilicon layer can is a poly-crystalline layer of silicon that is deposited on the gate oxide 14. The polysilicon layer can be uses as a silicon gate or can be used for interconnecting interconnections</p>

between devices. The polysilicon layer 18 preferably has a thickness in a range of between about 1000 and 3000 Å.”

*See, e.g.,* Tao at 6:8-13.

TABLE				
Element No.	generic name	preferred examples	Preferred Parameters (thickness, doping, etc . . . )	Other alternate examples
14	gate oxide layer	oxide	Thickness = 20 to 100 Å	nitrided oxide
20	polysilicon layer	Polysilicon or amorphous silicon	Th = 1000 to 3000 Å = doped or undoped	WSi <sub>2</sub> over polysilicon
22	a hard mask layer	Oxide	200 to 3000 Å	nitride or oxynitride
26	bottom anti-reflective coating (BARC) layer	organic	Thickness = 500 to 2000 Å	
30	resist layer	DUV photoresist	6000 to 13000 Å	i-line

*See, e.g.,* Tao at 5:55.

**Furthermore, this element is obvious based on the knowledge of a person of ordinary skill in the art.**

A person of ordinary skill in the art would have been motivated to incorporate this element from Tao or their own knowledge into Yun because Tao is focused on fabricating polysilicon gates (“This invention relates generally to fabrication of polysilicon gates in a semiconductor device”) *See, e.g.* Tao 1:7-8. A person of ordinary skill in the art would have a reasonable expectation of success in incorporating this limitation as the mechanisms for doing so are disclosed in references themselves. *See, e.g.,* Yun at pg. 2 (“a process of forming conventional gate oxide film, gate electrode, source, and drain.”).

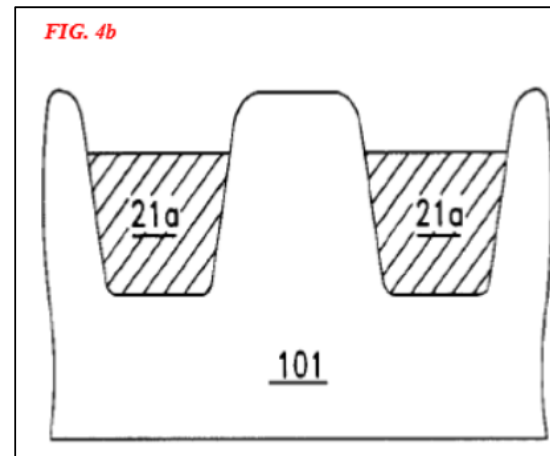
In addition to being a combination taught directly by these references, such a combination would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a

	known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.																												
[9] The transistor of claim 1, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.	<p><b>In the event it is determined that Yun does not disclose this element, it would have been obvious to modify Yun to include this element based either on the knowledge of a person of skill in the art and/or the teaching of other references. For example, Tao or Pey, which are also directed to semiconductor devices and methods of manufacturing semiconductor devices, teach this element:</b></p> <p>“The gate oxide layer 14 is preferably composed of silicon oxide having a thickness in a range of between about 20 and 100 Å.” <i>See, e.g.,</i> Tao at 6:5-7.</p> <div><p style="text-align: center;">TABLE</p><table><tr><th>Element No.</th><th>generic name</th><th>preferred examples</th><th>Preferred Parameters (thickness, doping, etc . . . )</th><th>Other alternate examples</th></tr><tr><td>14</td><td>gate oxide layer</td><td>oxide</td><td>Thickness = 20 to 100 Å</td><td rowspan="3">nitrided oxide</td></tr><tr><td>20</td><td>polysilicon layer</td><td>Polysilicon or amorphous silicon</td><td>Th = 1000 to 3000 Å = doped or undoped</td></tr><tr><td>22</td><td>a hard mask layer</td><td>Oxide</td><td>200 to 3000 Å</td></tr><tr><td>26</td><td>bottom anti-reflective coating (BARC) layer</td><td>organic</td><td>Thickness = 500 to 2000 Å</td><td>WSi<sub>x</sub> over polysilicon nitride or oxynitride</td></tr><tr><td>30</td><td>resist layer</td><td>DUV photoresist</td><td>6000 to 13000 Å</td><td>i-line</td></tr></table></div> <p><i>See, e.g.,</i> Tao at 5:45-67.</p> <p><b>As another example, Pey also teaches this element:</b></p> <p>“Referring to FIG. 1, an overlying stack consisting of a gate oxide layer 6, an overlying first polysilicon layer 8, and a still further overlying silicon nitride layer 10 is then formed. Said gate oxide 6 is a thin thermal oxide, with a typical thickness range of about 25 to 30 angstroms, that is subsequently nitrided. A preferred gate oxide thickness of about 40 angstroms is grown in a dry followed by a partial wet ambient, at a typical temperature range of about 800 to 1000 degrees centigrade for a duration of about 1 to 3 minutes. Said subsequent nitridation process can be performed at a temperature range of about 900 to 1000 degrees centigrade, in a nitrous oxide (N<sub>2</sub>O) ambient, using an RTA.”</p>	Element No.	generic name	preferred examples	Preferred Parameters (thickness, doping, etc . . . )	Other alternate examples	14	gate oxide layer	oxide	Thickness = 20 to 100 Å	nitrided oxide	20	polysilicon layer	Polysilicon or amorphous silicon	Th = 1000 to 3000 Å = doped or undoped	22	a hard mask layer	Oxide	200 to 3000 Å	26	bottom anti-reflective coating (BARC) layer	organic	Thickness = 500 to 2000 Å	WSi <sub>x</sub> over polysilicon nitride or oxynitride	30	resist layer	DUV photoresist	6000 to 13000 Å	i-line
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	<p><i>See, e.g.,</i> Pey at 4:56-67.</p> <div data-bbox="961 386 1581 643" data-label="Image"> <p>The diagram is a cross-sectional view of a transistor. It shows a substrate with a gate stack on top. The gate stack consists of several layers: a bottom layer (2), a middle layer (4), and a top layer (6). Above the top layer (6) are two more layers (8 and 10). The gate stack is flanked by source/drain regions (4). The label 'FIG. 1' is positioned below the diagram.</p> </div> <p><i>See, e.g.,</i> Pey at Fig. 1.</p> <p><b>Furthermore, this element is obvious based on the knowledge of a person of ordinary skill in the art.</b></p> <p>A person of ordinary skill in the art would have been motivated to incorporate this element from Pey, Tao or their own knowledge into Yun because in typical device structures, “a gate oxide layer and an overlying polysilicon layer are first patterned into gate regions.” <i>See, e.g.</i> Pey at 1:44-46; Tao 1:7-8. A person of ordinary skill in the art would have a reasonable expectation of success in incorporating this limitation as the mechanisms for doing so are disclosed in references themselves. <i>See, e.g.,</i> Yun at pg. 2 (“a process of forming conventional gate oxide film, gate electrode, source, and drain.”).</p> <p>In addition to being a combination taught directly by these references, such a combination would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.</p>
<p>[10] The transistor of claim 1, wherein said source region and said drain region are each comprised of an extension implant region</p>	<p><b>Yun discloses the transistor of claim 1, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region. By way of non-limiting example, Yun discloses:</b></p>

<p>and a source/drain implant region.</p>	<p>“The present invention relates to a semiconductor device. In a method of manufacturing a transistor for a semiconductor device, the summary of the present invention comprises: a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process; a process of forming a well region on the silicon substrate by means of a conventional process of local ion implantation on the field; a process of partially etching a first oxide film inside the trench isolation by means of wet etching; a process of forming a second oxide film by performing an oxidation process; a process of ion implantation for optimization of the threshold voltage; a process of etching the second oxide film by means of wet etching; and a process of forming conventional gate oxide film, gate electrode, source, and drain.”  <i>See, e.g., Yun at abstract.</i></p> <p>“According to the technical ideas of the present invention to achieve the objects described above, the method of manufacturing a transistor for a semiconductor device comprises: a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process; a process of forming a well region on the silicon substrate by means of a conventional process of local ion implantation on the field; a process of partially etching a first oxide film inside the trench isolation by means of wet etching; a process of forming a second oxide film by performing an oxidation process; a process of ion implantation for optimization of the threshold voltage; a process of etching the second oxide film by means of wet etching; and a process of forming conventional gate oxide film, gate electrode, source, and drain.”  <i>See, e.g., Yun at pg. 1.</i></p> <p>“FIGS. 4a to 4c are the cross-sectional views of the fabrication process, and as such they illustrate the sequence of manufacturing a transistor according to one embodiment of the present invention. With reference to FIG. 4a, a trench isolation region 21 is formed on a silicon substrate 101 by means of a conventional trench isolation process and a well region is formed on a conventional Local Implantation on Field LIF process. With reference to FIG. 4b, the oxide film 21a inside the trench isolation in the region desired to increase the channel width is etched by 10nm - 200nm by means of a wet etching process. Also, the sacrificial oxide film is sacrificed by 10nm - 30nm to allow the channel region in the angular part to become a more curved surface, thereby increasing the channel width W. Then, ion implantation to optimize the threshold voltage of the transistor is performed for <math>3.0 \times 10^{11}/\text{cm}^2</math> - <math>2.0 \times 10^{12}/\text{cm}^2</math> and, after that, the sacrificial film is etched by wet etching. Accordingly, it is shown that the oxide film 21a filled in the isolation region is formed underneath the silicon substrate 101. With</p>
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reference to FIG. 4c, after the process described above is performed, a transistor is formed by means of a gate oxide 41 formation process and a source and drain formation process.”  
*See, e.g., Yun at pg. 2.*



*See, e.g., Yun at Fig. 4b; see also, Figs. 4a and 4c.*

“Claim 1

A method of manufacturing a transistor for a semiconductor device comprising:

a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process;

a process of forming a well region on the silicon substrate by means of a conventional process of localized ion implantation on the field;

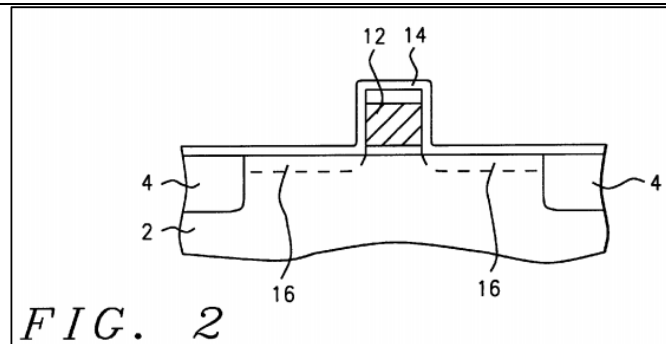
a process of partially etching a first oxide film inside the trench isolation by means of wet etching;

a process of forming a second oxide film by performing an oxidation process;

a process of ion implantation for optimization of the threshold voltage;

	<p>a process of etching the second oxide film by means of wet etching; and</p> <p>a process of forming conventional gate oxide film, gate electrode, source, and drain.”</p> <p><i>See, e.g., Yun at claim 1.</i></p> <p><b>“Claim 4</b></p> <p>A method of manufacturing a transistor for a semiconductor device, according to claim 1, wherein the impurity in the ion implantation is boron fluoride being ion implanted in the concentration of <math>3.0 \times 10^{11}</math> - <math>2.0 \times 10^{12}</math> per unit area at 40 KeV - 60 KeV.”</p> <p><i>See, e.g., Yun at claim 4.</i></p> <p><b>In the event it is determined that Yun does not disclose this element, it would have been obvious to modify Yun to include this element based either on the knowledge of a person of skill in the art and/or the teaching of other references. For example, Rubin or Pey, teach this element:</b></p> <p>“Referring now more particularly to FIG. 2, conventional masking and plasma etching is now performed on said stack, consisting of said nitride layer 10, said first polysilicon layer 8 and said gate oxide layer 6, in order to form first polysilicon gate 12. The gate oxide acts as an etch stop, after which a cleaning step is used to remove the remaining oxide from the active regions. A Bromine based (HBr) plasma etching chemistry is typically used to form said first polysilicon gate 12. An overlying thin TEOS, SiO<sub>2</sub> liner 14 is then blanket deposited to a thickness of about 150 angstroms, to reduce overlap capacitance. At this stage Low Doped Drain, LDD, regions 16 are formed, by means of conventional masking and ion implantation processing.”</p> <p><i>See, e.g., Pey at 5:12-24.</i></p>
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*See, e.g., Pey at Fig. 2.*

**As another example, Rubin also teaches this element:**

“The present invention provides for implanting through a blocking layer of material that promotes interstitial recombination at its interface with crystalline silicon better than does a conventionally grown oxide layer. For example, the blocking layer can be of carbon-bearing silicon dioxide such as that resulting from a TEOS oxide deposition. The invention applies most favorably to boron or other p-type source/drain extension implants for a PMOS transistor.”

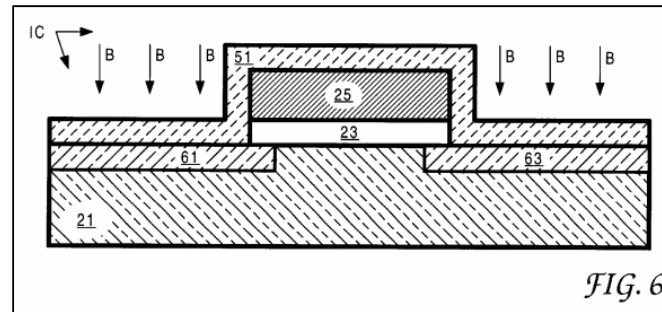
*See, e.g., Rubin at 3:13-20.*

“Source/drain extension implants are performed at step S5. Separate masks are used for the PMOS and NMOS transistors. For each implant, the energy is selected so that the bulk of the respective dopant is implanted just below the silicon surface. Step S5 involves implanting boron B into the source/drain regions of the PMOS transistors and arsenic (or phosphorous) into the source/drain regions of the NMOS transistors. Step S5 can also provide for an oblique “halo” implant of complementary dopant (boron for NMOS, arsenic or phosphorous for PMOS) under the gate to help counter the short-channel effect.

Step S5 can also provide for thermal “drive-in” of the dopants. Elevated temperatures increase the mobility of atoms entrained in the silicon crystal lattice. Initially, dopants diffuse in all directions. However, as interstitial silicon migrates into the TEOS layer, it sweeps other dopants, particularly boron (which comprises relatively small atoms), with it. As a result, the boron is confined closer to the TEOS covered silicon surface than it would be if a material, such as a thermal oxide, with a lower interstitial

recombination rate were used. The post-diffusion extents of the source extension 61 and a drain extension 63 are shown in FIG. 6.”

*See, e.g., Rubin at 5:34-56.*



*See, e.g., Rubin at Fig. 6.*

**Furthermore, this element is obvious based on the knowledge of a person of ordinary skill in the art.**

A person of ordinary skill in the art would have been motivated to incorporate this element from Pey, Rubin, or their own knowledge into Yun because in typical device structures, “a gate oxide layer and an overlying polysilicon layer are first patterned into gate regions.” *See, e.g. Pey at 1:44-46.* (“To reduce what is known as a “hot-carrier effect”, each source and each drain can include a lightly-doped extension that separates a respective heavily doped “deep” source/drain region from the channel. The channel then separates the source extension from the drain extension (also known as a “lightly doped drain” or “LDD”).”) *See also, e.g. Rubin at 1:34-39.* A person of ordinary skill in the art would have a reasonable expectation of success in incorporating this limitation as the mechanisms for doing so are disclosed in references themselves. *See, e.g., Yun at pg. 2* (“a process of forming conventional gate oxide film, gate electrode, source, and drain.”).

In addition to being a combination taught directly by these references, such a combination would have been (a) the combination of prior art elements according to known methods to yield predictable results, (b) the simple substitution of one known element for another to obtain predictable results, (c) the use of a known technique to improve similar devices in the same way, (d) applying a known technique to a

	known device ready for improvement to yield predictable results, and (e) obvious to try with a reasonable expectation of success.
[11] The transistor of claim 1, wherein said gate electrode has first and second end portions that extend into said recess.	<p><b>Yun discloses the transistor of claim 1, wherein said gate electrode has first and second end portions that extend into said recess. By way of non-limiting example, Yun discloses:</b></p> <p><i>See disclosure for claim 1(c). This disclosure is incorporated by reference herein.</i></p>
[12] The transistor of claim 11, wherein said first and second end portions extending into said recess are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.	<p><b>Yun discloses the transistor of claim 11, wherein said first and second end portions extending into said recess are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure. By way of non-limiting example, Yun discloses:</b></p> <p><i>See disclosure for claims 1(c) and 23(b). This disclosure is incorporated by reference herein.</i></p>
[13pre] A transistor, comprising:	<p><b>Yun discloses a transistor.</b></p> <p><i>See disclosure for claim 1(p). This disclosure is incorporated by reference herein.</i></p>
[13a] a semiconducting substrate comprised of silicon;	<p><b>Yun discloses a semiconducting substrate comprised of silicon.</b></p> <p><i>See disclosure for claims 1(a) and 2. This disclosure is incorporated by reference herein.</i></p>
[13b] a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove;	<p><b>Yun discloses a recessed isolation structure formed in said substrate, said isolation structure defining a recess thereabove.</b></p> <p><i>See disclosure for claim 1(b). This disclosure is incorporated by reference herein.</i></p>
[13c] a gate electrode comprised of polysilicon and a gate insulation layer	<p><b>Yun discloses a gate electrode comprised of polysilicon and a gate insulation layer formed above said substrate, a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure.</b></p>

formed above said substrate, a portion of said gate electrode and said gate insulation layer extending into said recess above said recessed isolation structure; and	<i>See</i> disclosure for claims 1(c) and 6. This disclosure is incorporated by reference herein.
[13d] a source region and a drain region formed in said substrate.	<b>Yun discloses a source region and a drain region formed in said substrate.</b> <i>See</i> disclosure for claim 1(d). This disclosure is incorporated by reference herein.
[14] The transistor of claim 13, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.	<b>Yun discloses the transistor of claim 13, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.</b> <i>See</i> disclosure for claim 3. This disclosure is incorporated by reference herein.
[16] The transistor of claim 13, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.	<b>Yun discloses the transistor of claim 13, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.</b> <i>See</i> disclosure for claim 5. This disclosure is incorporated by reference herein.
[17] The transistor of claim 13, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.	<b>Yun discloses the transistor of claim 13, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.</b> <i>See</i> disclosure for claim 7. This disclosure is incorporated by reference herein.

[18] The transistor of claim 13, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.	<p><b>Yun discloses the transistor of claim 13, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.</b></p> <p><i>See disclosure for claim 8. This disclosure is incorporated by reference herein.</i></p>
[19] The transistor of claim 13, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.	<p><b>Yun discloses the transistor of claim 13, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.</b></p> <p><i>See disclosure for claim 9. This disclosure is incorporated by reference herein.</i></p>
[20] The transistor of claim 13, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.	<p><b>Yun discloses the transistor of claim 13, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.</b></p> <p><i>See disclosure for claim 10. This disclosure is incorporated by reference herein.</i></p>
[21] The transistor of claim 13, wherein said gate electrode has first and second end portions that extend into said recess in said substrate.	<p><b>Yun discloses the transistor of claim 13, wherein said gate electrode has first and second end portions that extend into said recess in said substrate.</b></p> <p><i>See disclosure for claim 11. This disclosure is incorporated by reference herein.</i></p>
[22] The transistor of claim 21, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.	<p><b>Yun discloses the transistor of claim 21, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.</b></p> <p><i>See disclosure for claim 12. This disclosure is incorporated by reference herein.</i></p>

[23] A transistor, comprising:	<p><b>Yun discloses a transistor.</b></p> <p><i>See disclosure for claim 1(p). This disclosure is incorporated by reference herein.</i></p>
[23a] a semiconducting substrate;	<p><b>Yun discloses a semiconducting substrate.</b></p> <p><i>See disclosure for claim 1(a). This disclosure is incorporated by reference herein.</i></p>
[23b] a recessed isolation structure defining an active area having an upper surface and an exposed sidewall surface;	<p><b>Yun discloses a recessed isolation structure defining an active area having an upper surface and an exposed sidewall surface. By way of non-limiting example, Yun discloses:</b></p> <p><i>See also disclosure for claim 1(b). This disclosure is incorporated by reference herein.</i></p>
[23c] a gate insulation layer and a gate electrode positioned above a portion of said upper surface and a portion of said exposed sidewall surface of said active area; and	<p><b>Yun discloses a gate insulation layer and a gate electrode positioned above a portion of said upper surface and a portion of said exposed sidewall surface of said active area.</b></p> <p><i>See disclosure for claims 1(c), 12 and 23(b). This disclosure is incorporated by reference herein.</i></p>
[23d] a source region and a drain region formed in said active area.	<p><b>Yun discloses a source region and a drain region formed in said active area.</b></p> <p><i>See disclosure for claim 1(d). This disclosure is incorporated by reference herein.</i></p>
[24] The transistor of claim 23, wherein said semiconducting substrate is comprised of silicon.	<p><b>Yun discloses the transistor of claim 23, wherein said semiconducting substrate is comprised of silicon.</b></p> <p><i>See disclosure for claim 2. This disclosure is incorporated by reference herein.</i></p>
[25] The transistor of claim 23, wherein said recessed	<p><b>Yun discloses the transistor of claim 23, wherein said recessed isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.</b></p>

isolation structure is comprised of at least one of silicon dioxide and silicon oxynitride.	<i>See</i> disclosure for claim 3. This disclosure is incorporated by reference herein.
[27] The transistor of claim 23, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.	<p><b>Yun discloses the transistor of claim 23, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.</b></p> <p><i>See</i> disclosure for claim 5. This disclosure is incorporated by reference herein.</p>
[28] The transistor of claim 23, wherein said gate electrode is comprised of polysilicon.	<p><b>Yun discloses the transistor of claim 23, wherein said gate electrode is comprised of polysilicon.</b></p> <p><i>See</i> disclosure for claim 6. This disclosure is incorporated by reference herein.</p>
[29] The transistor of claim 23, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride.	<p><b>Yun discloses the transistor of claim 23, wherein said gate insulation layer is comprised of at least one of silicon dioxide and silicon oxynitride</b></p> <p><i>See</i> disclosure for claim 7. This disclosure is incorporated by reference herein.</p>
[30] The transistor of claim 23, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.	<p><b>Yun discloses the transistor of claim 23, wherein said gate electrode has a thickness ranging from approximately 1000-2000 Å.</b></p> <p><i>See</i> disclosure for claim 8. This disclosure is incorporated by reference herein.</p>
[31] The transistor of claim 23, wherein said gate	<b>Yun discloses the transistor of claim 23, wherein said gate insulation layer has a thickness ranging from approximately 20-50 Å.</b>

insulation layer has a thickness ranging from approximately 20-50 Å.	<i>See</i> disclosure for claim 9. This disclosure is incorporated by reference herein.
[32] The transistor of claim 23, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.	<p><b>Yun discloses the transistor of claim 23, wherein said source region and said drain region are each comprised of an extension implant region and a source/drain implant region.</b></p> <p><i>See</i> disclosure for claim 10. This disclosure is incorporated by reference herein.</p>
[33] The transistor of claim 23, wherein said gate electrode has first and second end portions that extend into a recess in said substrate defined by said recessed isolation structure.	<p><b>Yun discloses the transistor of claim 23, wherein said gate electrode has first and second end portions that extend into a recess in said substrate defined by said recessed isolation structure.</b></p> <p><i>See</i> disclosure for claims 1(c) and 11. This disclosure is incorporated by reference herein.</p>
[34] The transistor of claim 33, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.	<p><b>Yun discloses the transistor of claim 33, wherein said first and second end portions extending into said recess in said substrate are positioned above a portion of a sidewall of an active region of said substrate defined by said recessed isolation structure.</b></p> <p><i>See</i> disclosure for claim 12. This disclosure is incorporated by reference herein.</p>