

1 UNITED STATES PATENT AND TRADEMARK OFFICE

2
3 BEFORE THE PATENT TRIAL AND APPEAL BOARD

4
5 SMIC, AMERICAS,
6 Petitioner,

7 v.

8 INNOVATIVE FOUNDRY TECHNOLOGIES, LLC,
9 Patent Owner.

10 Case No. IPR2020-01003
11 U.S. Patent No. 6,580,122

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15 REMOTE VIDEOCONFERENCE DEPOSITION of

16 SAYFE KIAEI, Ph.D.

17 Friday, March 12, 2021

18 Scottsdale, Arizona

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24 Reporter: MaryJo O'Connor, RDR, RMR
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Friday, March 12, 2021

10:36 a.m. EST

REMOTE VIDEOCONFERENCE DEPOSITION

of SAYFE KIAEI, Ph.D., held via Zoom
videoconference in Scottsdale, Arizona,
pursuant to notice, before MaryJo O'Connor,
Registered Diplomat Reporter, Registered
Merit Reporter and Notary Public in and for
the Commonwealth of Massachusetts.

1 A P P E A R A N C E S

2

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23

24 ALSO PRESENT: Jose Rivera, videographer

25

1 -----I N D E X-----

2 EXAMINATION of SAYFE KIAEI, Ph.D. PAGE

3 By Mr. Constantine 6

4 By Mr. Martinelli 30

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8

9 -----INSTRUCTIONS-----

10 Page Line

11

12

13

14 -----EXHIBITS-----

15 KIAEI EXHIBIT PAGE

16 Exhibit 1 Korean patent, Laid-Open 6

17 Disclosure No. KR1998-074469,

18 Applicant, Jong Yong Yun

19 Exhibit 2 United States Patent No. 6

20 5,960,297, Inventor Kazuo

21 Saki

22 Exhibit 3 United States Patent No. 6

23 5,859,466, Inventor Toshio

24 Wada

25

1 P R O C E E D I N G S

2

3 VIDEO TECHNICIAN: We are now on
4 the record. This is the remote
5 video-recorded deposition of Dr. Sayfe
6 Kiaei.

7 Today is Friday, March 12, 2021.
8 The time is now 10:36 a.m., and the
9 Eastern time zone. We are here in the
10 matter of SMIC Americas versus
11 Innovative Foundry Technologies, LLC.

12 My name is Jose Rivera, remote
13 video technician, on behalf of
14 GregoryEdwards LLC.

15 Will counsel please introduce
16 themselves.

17 MR. CONSTANTINE: Yes. I'm Derek
18 Constantine with Mintz Levin.

19 MR. MARTINELLI: And I'm Rich
20 Martinelli from Orrick on behalf of
21 SMIC, Americas.

22 VIDEO TECHNICIAN: At this time,
23 will the reporter, MaryJo O'Connor, on
24 behalf of GregoryEdwards LLC please
25 swear in the witness.

1 COURT REPORTER: Before we swear
2 in the witness, I'd like a stipulation
3 from the attorneys. That the witness is
4 in Arizona, I am a Massachusetts notary,
5 and I'd like you to stipulate that my
6 oath is binding.

7 MR. CONSTANTINE: Yes, we agree.

8 MR. MARTINELLI: And that's also
9 okay per the petitioner.

10 * * *

11 (Document marked for
12 identification as Kiaei Exhibit 1)

13 (Document marked for
14 identification as Kiaei Exhibit 2)

15 (Document marked for
16 identification as Kiaei Exhibit 3)

17 * * *

18
19 SAYFE KIAEI, Ph.D.,
20 having been duly sworn by the Notary Public,
21 was examined and testified as follows:

22 EXAMINATION

23 BY MR. CONSTANTINE:

24 Q. Thank you for joining us, Doctor.
25 I know you're familiar with this process at

1 this point, but obviously to the extent that
2 you don't understand my question or you can't
3 hear me, please let me know and I can repeat it
4 or I can rephrase to help address any issues.

5 And throughout this process, we
6 can take breaks. I don't think this will be a
7 very long deposition. So to the extent that we
8 end up needing it, obviously we can take a
9 lunch break, but I'm assuming we can probably
10 finish this up before then.

11 Does that all generally make sense
12 and sound reasonable?

13 A. Good morning, Counsel. Yes, it
14 is. Thank you for the background.

15 Q. Okay. All right, great.

16 So the three different exhibits
17 that I want to discuss today is three different
18 pieces of prior art. You'll see Yun on your
19 screen now as Exhibit 1.

20 Can you see the document in front
21 of you?

22 A. I see Wada in front of me right
23 now.

24 Q. You see Wada?

25 A. Yes.

1 Q. Let me see if I can take control.

2 Okay. Can you see Yun now?

3 A. I see Yun, yes. I see the Yun
4 original patent and the translation afterwards.
5 Yeah.

6 Q. Okay. Now, Yun uses a
7 conventional trench isolation process in its
8 semiconductor devices; is that correct?

9 A. Yes, it does.

10 Q. And the conventional trench
11 isolation process uses silicon oxide and
12 silicon nitride to electrically isolate the
13 trench when it's making this process.

14 (Court reporter comment)

15 Q. Conventional trench isolation
16 process uses silicon oxide and silicon nitride
17 to electrically isolate a trench; is that
18 correct?

19 A. That is one of the materials that
20 can be used for isolation. There are other
21 materials for isolations.

22 Q. Can you please describe the steps
23 in a conventional trench isolation process?

24 MR. MARTINELLI: Objection to
25 form.

1 Q. Doctor, could you describe the
2 steps in the process?

3 A. Yes, I am, if you give me a
4 second, please.

5 Q. Okay. If you could just let us
6 know what you're looking at?

7 A. Yes, I am. I am looking at the
8 Yun patent --

9 Q. Okay.

10 A. -- right now. And the steps
11 involves forming a trench and filling the
12 trench with an isolation material. That's one
13 of the steps.

14 Q. And what is the isolation material
15 that's used in Yun?

16 And I apologize, Doctor. To the
17 extent that you're looking at other documents,
18 could you just let us know what you're looking
19 at?

20 A. Sure. Sure. I have a, just to
21 make sure that you're aware of it, I have a
22 printed copy of the Yun's patent, I have a
23 printed copy of the '122 patent, and I have
24 also a printed copy of the Wada patent.

25 Actually, sorry, I don't have a

1 printed copy of the Yun patent. So I have to
2 rely on your copy of this main patent.

3 So right now I'm looking at the
4 Yun itself on the screen if that's okay.

5 Q. Yeah. That's fine.

6 A. It's typically silicon oxide or
7 silicon dioxide or silicon nitride.

8 Q. Okay.

9 A. But it can be, as I said before,
10 it can be other materials, as the '122 patent
11 tells and discusses that.

12 Q. All right. Now, I'm switching
13 over to the Saki reference.

14 Do you see that in front of you?

15 A. Yes, I do, Counsel.

16 Q. Now, the Saki reference discloses
17 a shallow trench isolation structure that's
18 similar to Yun; is that correct?

19 A. I agree, yes, it is.

20 Q. And the shallow trench isolation
21 structure also uses silicon oxide and silicon
22 nitride to electrically isolate a trench; is
23 that correct?

24 A. That is correct. And a trench
25 uses an isolating material such as silicon

1 oxide and silicon nitride, correct.

2 Q. And could you describe the steps
3 in forming a shallow trench isolation structure
4 to the extent that you would consider it to be
5 different than what was used in Yun?

6 A. Again, the process -- sorry, go
7 ahead, please, Rich.

8 MR. MARTINELLI: Yes. Just an
9 objection to form.

10 A. Thank you.

11 Continuing on, as you can see in a
12 bigger, for example, 1(b) of the Saki, if you
13 can go there, it shows that the trench 106 is
14 formed in the substrate.

15 Q. And the third document I wanted to
16 look at was the Wada reference.

17 Do you see that on your screen?

18 A. Yes, Counsel, I do have it. Yes.
19 But I'm looking at it also on my screen as
20 well.

21 Q. Okay. Now, Wada discloses a
22 field-shield device isolation structure, and it
23 uses that structure to isolate a trench; is
24 that correct?

25 MR. MARTINELLI: Objection. Form.

1 A. Wada also, as you can see in the
2 abstract, but the Wada it shows fabrication for
3 the isolation structure similar to what Yun and
4 Saki shows. And, again, it forms a trench and
5 similar to the Yun and Saki as well.

6 Q. But does Wada disclose a
7 field-shield device isolation structure?

8 A. After it shows that the trench is
9 formed, then as, for example, if you look at
10 the Figure 2A of Wada, it shows the first step
11 which is the step performing the trench.

12 Q. I apologize. I think we're
13 getting beyond the question at this point.

14 A. Please repeat the question, yes.

15 Q. Sure. Does Wada disclose a
16 field-shield device isolation structure?

17 A. Wada also discusses a field-shield
18 isolation structure, yes.

19 Q. And the field-shield isolation
20 structure in Wada uses the field-shield
21 insulator film and a field-shield electrode to
22 electrically isolate a trench; is that correct?

23 MR. MARTINELLI: Objection to
24 form.

25 A. Wada shows the isolation material

1 similar to what the other two patents we
2 discussed, which is Yun and Saki. And in
3 addition to that, also it discusses having the
4 electrode in the trench as well.

5 Q. And the field-shield electrode in
6 Wada is embedded in the trench; is that
7 correct?

8 A. Can you repeat the question? I
9 did not hear the last part.

10 Q. The field-shield electrode in
11 Wada, is it embedded in the trench?

12 A. The field-shield material and the
13 structure of it is formed -- it formed within
14 the trench or it could be within the parameters
15 of the trench.

16 Q. And the field-shield electrode in
17 Wada helps to electrically -- I apologize,
18 electrically isolate the trench; is that
19 correct?

20 MR. MARTINELLI: Objection to
21 form.

22 A. I don't think that's exactly
23 correct. What it has is that it has an
24 insulating material. That insulating material
25 insulates the device. And then in addition to

1 that, it uses electrodes for performing
2 additional operations in there.

3 (Court reporter requests
4 clarification)

5 A. For performing additional
6 operations in there.

7 Q. And what is the function or
8 purpose of the field-shield electrode in Wada?

9 A. Let me take a look at Wada
10 closely, if you don't mind, for a second.

11 Q. Take your time.

12 A. Thank you.

13 (Document review.) Wada doesn't --
14 sorry. Wada doesn't go in a lot of details for
15 the purpose of electrode within the structure,
16 but it talks about it in paragraph -- in
17 column 11 line 65 onwards, if you can go there.

18 And it says that "the field-shield
19 electrode is not insulated from the substrate
20 but is actually in electrical contact with the
21 internal surface of the substrate through the
22 bottom surface of the trench."

23 Q. And --

24 A. It has the same potential as by
25 connecting it as a substrate, same potential as

1 a substrate, meaning same electrical potential
2 as the substrate.

3 Q. As an expert in the field, can you
4 describe generally what function an electrode
5 would serve in a field-shield device isolation
6 structure like the one used in Wada?

7 A. In general, it can be used for
8 many different reasons. It really depends on
9 the design requirements and how the system is
10 designed.

11 Q. Do you have some examples that you
12 can provide?

13 A. An example, it could be for
14 attracting minority carriers, electrons that
15 could be noise in the substrate.

16 (Court reporter clarification)

17 A. Minority carriers. Minority
18 carriers — electron minority carriers in the
19 substrate.

20 MR. CONSTANTINE: Can we take
21 about a five-minute break?

22 THE WITNESS: Sure.

23 MR. CONSTANTINE: Is that okay
24 with everyone?

25 MR. MARTINELLI: Absolutely. Yes.

1 VIDEO TECHNICIAN: Okay. Stand
2 by. The time is 10:55 a.m., and we're
3 going off the record.

4 (Proceedings recessed at
5 10:55 a.m., and reconvened at 11:01
6 a.m.)

7 VIDEO TECHNICIAN: The time is
8 11:01 a.m., and we're back on the
9 record.

10 BY MR. CONSTANTINE:

11 Q. All right. I wanted to clarify a
12 point regarding the field-shield electrode in
13 Wada. Previously I had asked if the
14 field-shield electrode helps to electrically
15 isolate the trench, and you didn't feel that
16 that was quite accurate.

17 I just wanted to direct your
18 attention to this section right here of Wada,
19 column 1 lines 29 through about 35. And it
20 seems to indicate that field-shield device
21 isolation methods use a field-shield insulator
22 film and the field-shield electrode between two
23 active regions to electrically isolate them.

24 So I just wanted to clarify what
25 you think the functionality of the field-shield

1 electrode is in Wada.

2 MR. MARTINELLI: Objection to
3 form.

4 A. Do you have a question you want to
5 ask me, please?

6 Q. Yes. Is the field-shield
7 electrode in Wada acting to assist in
8 electrically isolating two regions?

9 A. As I mentioned earlier, they --
10 what Wada teaches is to form a trench, as we
11 discussed, and it discusses the depth of the
12 trench. Then after forming the trench and
13 after discussing the depth and the width of the
14 trench, then it talks about the next steps,
15 which are those additional steps it talks about
16 forming the structure within the trench, which
17 is an insulating material by having an
18 insulator in there.

19 And also, in addition to that, it
20 discusses having a field-shield electrode; and
21 it fixes that field-shield electrode to, as
22 that paragraph also you're reading, is by
23 fixing the field-shield electrode potential at
24 the reference potential, the formation of the
25 parasitic channel on the device surface is

1 prevented.

2 So what it is focusing on here is
3 that the field-shield electrode is connecting
4 to the ground or VDD. VDD is a voltage supply,
5 for the record. It is a voltage supply, and it
6 also says that. It is for the formation of
7 parasitic channels on the device surface is
8 prevented. Meaning that it's helping with
9 parasitic channels, which are primarily dealing
10 with capacitances and other issues in there.

11 But the critical point of Wada is
12 the fact that it forms the trench. And that
13 trench, which is the insulation, the trench,
14 and talks about the trench depth and the width,
15 get closer --

16 Q. And I --

17 A. Let me finish please.

18 Width and depth. And based on
19 that, that insulation material helps with the
20 insulation.

21 And then it talks about also
22 adding to that structure a field-shield
23 electrode with specific potential voltage to
24 help with parasitic channels.

25 Q. I understand that, Doctor. But,

1 again, I am curious -- or I want to know if the
2 field-shield electrode assists in electrically
3 isolating the trench.

4 A. The field-shield electrode
5 structure, as I mentioned already, it has a
6 trench and it has an isolation material in
7 there --

8 Q. I apologize. I --

9 A. -- and that helps with the --

10 Q. I --

11 A. -- that helps with the -- if you
12 let me finish, please.

13 -- and that helps -- thank you,
14 Counsel.

15 -- and that helps with the
16 isolation of the -- of the -- that structure
17 overall helps with the isolation region.

18 Q. And I appreciate what the
19 structure overall does. I'm specifically
20 asking about the field-shield electrode.

21 Does the field-shield electrode
22 help to electrically isolate the trench?

23 A. Okay. Let me read you the
24 paragraph one more time, maybe that way it may
25 help us understand this issue.

1 Reading the same paragraph you
2 mentioned on column 1, it says that the
3 "Field-shield ... isolation method relates to a
4 MOS" -- M-O-S -- "structure for separating
5 devices by forming a field-shield insulator
6 film and a field-shield electrode between two
7 active regions of a device."

8 So it talks about the --
9 separating the devices by forming a
10 field-shield insulator, which is the insulation
11 material within the trench we talked about,
12 that is also shown in Figure 2A. It has a
13 trench.

14 And then also it talks about an
15 additional step in there, which is field-shield
16 electrode between the two active region. And
17 by adding these, it's forming an isolation
18 structure.

19 Q. So based on that, my understanding
20 is that the field-shield electrode is assisting
21 in electrically isolating the trench; is that
22 correct?

23 A. That's not an opinion I have given
24 in my report about this specific of what the
25 electrode does. But, in general, as you asked

1 me earlier, and also as we discussed in the
2 paragraph that I have mentioned earlier, by
3 connecting that electrode to a substrate, to a
4 specific voltage, it helps with the minority
5 carriers as well as the formation of parasitic
6 channels.

7 Q. And I appreciate that, Doctor.
8 But, again, I feel like we're getting off of
9 the question somewhat.

10 My understanding, and that's where
11 I'm hoping you can, you know, correct me if I'm
12 wrong or agree one way or the other, is that
13 the field-shield insulator film and the
14 field-shield electrode in Wada are both acting
15 to electrically isolate the trench; is that
16 correct or is that incorrect?

17 MR. MARTINELLI: Objection to
18 form.

19 A. My answer is also same as before.
20 And if you can bring my report up for a second,
21 I can tell you exactly where I form my opinion.
22 If you can you look at, for example, in
23 Paragraph 123 and 122.

24 Q. What are you looking at?

25 A. If you can look at my declaration,

1 my report.

2 Q. I'm not interested in looking at
3 the declaration right now, Doctor.

4 A. Okay.

5 Q. I feel like the question was very
6 specific to Wada.

7 A. My answer is that the Wada
8 structure focuses on improving techniques for
9 isolating devices and transistors on the same
10 substrate.

11 Q. And that's fine. But, again,
12 Doctor, you're not answering my question.

13 A. Can you repeat your question, if
14 you don't mind, one more time, Counsel?

15 Q. Sure.
16 So my understanding is that the
17 structure used in Wada has a field-shield
18 insulator film and a field-shield electrode,
19 and those two components are assisting in
20 electrically isolating the trench in Wada; is
21 that correct or is that incorrect?

22 MR. MARTINELLI: Objection to
23 form.

24 A. The two components have
25 different -- have the purpose of they function

1 differently. The insulating material, the
2 trench and insulating material is for the
3 insulation.

4 And having the electrode, as this
5 paragraph says also, it helps with a -- a
6 minimizing the formation of parasitic channels
7 on the device.

8 The overall structure for -- is
9 isolation structure. So that, I would say that
10 overall structure is an isolation structure,
11 which consists of a trench with an insulating
12 material. That is the primary insulation that
13 is used for the insulation of forming the
14 trench with insulation material. And then uses
15 a field-shield electrode that is buried within
16 the interior space of the trench, and that is
17 connected to the substrate or zero volt or VDD
18 to additionally help with the formation of
19 parasitic channels.

20 Q. So based on that, you're saying
21 that the electrode in Wada is not helping with
22 isolation?

23 MR. MARTINELLI: Objection to
24 form.

25 A. That's not what I said. What I

1 said was that it's a combination of those two
2 is what is the field-shield structure is
3 talking about, field-shield device isolation
4 structure. And that consists of two different
5 components: One is the trench. And Wada
6 teaches what the width and the length of that
7 trench should be, and the insulating material
8 within the trench.

9 And then in addition to that, it
10 also talks about the field-shield electrode.
11 And that is, as Wada said, is primarily used
12 for the formation of the parasitic channels --

13 Q. I appreciate that, Doctor. But,
14 again, I'm focused on insulation here.

15 So, again, my understanding of
16 Wada is the field-shield electrode and the
17 field-shield insulator film together assists in
18 electrically isolating the trench. Is that a
19 correct statement or is that an incorrect
20 statement?

21 MR. MARTINELLI: Objection to
22 form.

23 A. My answer is the same, which is
24 the overall structure is meant for -- as the
25 title of the patent also says, and it discusses

1 it everywhere, is what an isolation structure.

2 Q. I appreciate that, Doctor. But,
3 again, I feel like I'm asking one question and
4 I'm getting a different answer. I feel like my
5 question is very specific and it's not, you
6 know, directed to generally what else does Wada
7 disclose.

8 A. If you give me a second, let me
9 look at the Wada patent again and see the
10 specifics of how the field-shield electrode
11 functionality is again to answer your question.

12 Q. All right.

13 A. Thank you, Counsel.

14 (Document review.) And I'm looking
15 at the Wada patent, by the way, so if you --
16 for your information.

17 Q. Okay. Thank you.

18 A. Sure.

19 (Document review.)

20 Q. Let me rephrase the question
21 slightly.

22 A. Sure.

23 Q. See if that helps.

24 By fixing the field-shield
25 electrode potential at a ground or a zero

1 voltage, is that assisting in electrically
2 isolating the trench?

3 MR. MARTINELLI: Objection to
4 form.

5 A. One thing of the patent, and my
6 knowledge of having the electrode lines tied to
7 a certain potential voltage, zero or VDD, that
8 helps with what the patent says is in terms of
9 the helping with the parasitic capacitances and
10 also with the minority carriers which is
11 potential -- currently potential noise that is
12 within the structure or within the substrates.

13 It is a -- the electrodes have a
14 higher conductivity. The primary side of the
15 isolation comes in from the isolation structure
16 of the device in there. So it helps in terms
17 of it's not an insulator. The electrodes is
18 not an insulator.

19 Q. The electrode is a conductor, not
20 an insulator, correct?

21 A. That's correct. It is a
22 conductor, yes.

23 Q. And so does the electrode assist
24 in isolation, in electrical isolation of the
25 trench?

1 A. I don't believe it is meant for
2 that. It is meant for the actual isolation
3 comes in from the trench and having the trench
4 filled in with an insulator.

5 The field-shield electrodes are
6 meant, as the patent also says, for reducing
7 the capacitances, parasitic capacitances. And
8 also from my knowledge when I've used this
9 techniques before, it helps with the leakage
10 currents or the noise that's in the substrate
11 that could potentially damage or interfere with
12 the transistor operations. That's the purpose
13 of that. That's an electrode. That's the
14 conductor.

15 Q. But by avoiding formation of
16 parasitic channels, aren't they also providing
17 insulative isolation of the trench?

18 A. Not necessarily. I will not agree
19 with that statement, no. Not necessarily.

20 Q. Because you --

21 A. And I searched in the patent to
22 see, you know, if it is talking about
23 electrodes connectivity being directly related
24 to the insulators. The electrodes are
25 conductors. They're tied to a certain voltage.

1 And as the patent also says, is
2 the purpose of that is the formation of
3 parasitic helping with the formation of
4 parasitic channels, which parasitic channels
5 are, you know, potential capacitances that
6 would impair the transistor's operation in high
7 frequency.

8 And also my own experience of
9 having used those before in different
10 applications, we are primarily using those for
11 helping with the current -- minimizing the
12 current noise or the substrate noise affecting
13 the transistor operation.

14 Q. If you look at column 1
15 line thirty -- it looks like 33 in the Wada
16 patent, it says, "By fixing the field-shield
17 electrode potential at a reference potential
18 (e.g., ground or zero voltage), the formation
19 of parasitic channels on the device surface is
20 prevented, thereby providing insulative
21 isolation of the active regions of the
22 devices."

23 So my understanding of this is,
24 again, the avoiding parasitic channels does
25 assist in electrically isolating the trench.

1 Is my understanding correct?

2 MR. MARTINELLI: Objection to
3 form.

4 A. I don't think -- I agreed up to
5 the last sentence where you added, I agree with
6 what the patent is saying, which is the "fixing
7 the field-shield electrode potential at a
8 reference potential, the formation of parasitic
9 channels on the device surface is prevented,
10 therefore providing insulative isolation of the
11 active regions of the devices."

12 So it was primarily talking about
13 creating an insulative isolation of the active
14 regions of the device, meaning that the
15 transistor's active region is helping with
16 insulations of those devices in terms of the
17 active regions.

18 But the primary -- it's a
19 combination of that structure, which is
20 discussing here. The primary insulation in the
21 substrate is created by having an insulative
22 material, which is the trench and what's filled
23 in there.

24 MR. CONSTANTINE: Okay. Thank
25 you, Doctor. I don't have any more

1 questions.

2 THE WITNESS: Thank you, Counsel.

3 MR. MARTINELLI: Are you saying
4 we're done for this deposition?

5 MR. CONSTANTINE: We're done with
6 the deposition.

7 MR. MARTINELLI: All right. I've
8 got a couple of follow-ups, then.

9 EXAMINATION

10 BY MR. MARTINELLI:

11 Q. So we just spent a little bit of
12 time here talking about the isolation structure
13 that's used to fill the trench in Wada; is that
14 correct?

15 A. Yes, Counsel.

16 Q. Does the isolation structure used
17 to fill the trench affect your obviousness
18 opinions that you rendered in your declaration?

19 A. No, it does not at all. And,
20 actually, my obviousness opinion is there. I
21 mean, fundamentally we're talking about the
22 '122 patent claim, you know, claims 5 for
23 example. If you look at that claim 5, the
24 claim 5 is talking about forming a trench, and
25 it talks about the width and the depth of the

1 trench, and it shows a number in terms of the
2 depth and the width of the trench. And that's
3 really the overall, what the claim 5 talks
4 about in addition to the recess.

5 So it says that the "recessed
6 isolation structure is formed in a trench
7 having a width ranging from approximately
8 2000-3000 angstrom and a depth ranging from
9 approximately 4000-5000 angstrom."

10 There is nothing here about the
11 structure. In here it is simply talking about
12 the trench itself. Meaning that it is only
13 talking about a hole, a trench, which is
14 created within the substrate. And that is
15 identical to what Wada, as I have shown in my
16 report, to Wada Figure 2A, for example.

17 In the Figure 2A of Wada, it has
18 exactly the same thing, if you look at the
19 Figure 2A of Wada.

20 So the obviousness is based on
21 this and nothing else. It does not talk about
22 in claim 5 about anything else but the trench
23 having a width of approximately 2,000 to 3,000
24 angstrom and a depth ranging from approximately
25 4,000 to 5,000 angstrom. And Wada discusses

1 having a trench, and it discusses the depth and
2 the width of the trench approximately what it
3 could be, and then it actually elaborates more
4 than that and talks about this depends on the
5 design and the material, et cetera, which '122
6 patent also discusses the same thing.

7 MR. MARTINELLI: Okay. No further
8 questions for me.

9 THE WITNESS: Thank you, Counsel.

10 VIDEO TECHNICIAN: The time is
11 11:27 a.m., and we're going off the
12 record.

13 (Time Noted: 11:27 a.m.)

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C E R T I F I C A T E

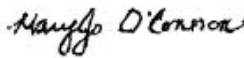
COMMONWEALTH OF MASSACHUSETTS

SUFFOLK, SS.

I, MaryJo O'Connor, a Notary Public
in and for the Commonwealth of
Massachusetts, do hereby certify:

That SAYFE KIAEI, Ph.D., the
witness whose testimony is hereinbefore set
forth, was duly sworn by me and that such
testimony is a true and accurate record of
my stenotype notes taken in the foregoing
matter to the best of my knowledge, skill
and ability.

IN WITNESS WHEREOF, I have hereunto
set my hand and Notarial Seal this 13th day
of March 2021.



MARYJO O'CONNOR, RDR/RMR

Notary Public

My Commission expires:

September 12, 2025

| 1 | LAWYER'S NOTES | | |
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CERTIFICATE OF DEPONENT

I hereby certify that I have read the foregoing pages of my deposition testimony in this proceeding, and with the exception of changes and/or corrections, if any, find them to be a true and correct transcription thereof.

Deponent

Date

NOTARY PUBLIC

Subscribed and sworn to before me this _____ day of _____, 20__.

Notary Republic

My Commission Expires:_____

1 INSTRUCTIONS TO WITNESS

2

3 Please read your deposition over carefully
4 and make any necessary corrections. You
5 should state the reason in the appropriate
6 space on the errata sheet for any corrections
7 that are made.

8 After doing so, please sign the errata
9 sheet and date it.

10 You are signing same subject to the changes
11 you have noted on the errata sheet, which
12 will be attached to your deposition.

13 It is imperative that you return the
14 original errata sheet to the deposing
15 attorney within thirty (30) days of
16 receipt of the deposition transcript by
17 you. If you fail to do so, the deposition
18 transcript may be deemed to be accurate
19 and may be used in court.

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심사청구 : 없음

(54) 반도체 장치의 트랜지스터 제조방법

요약

본 발명은 반도체 장치에 관한 것이다. 본 발명의 요지는 반도체 장치의 트랜지스터 제조방법에 있어서, 실리콘 기판에 통상의 트랜치 분리 공정을 통하여 트랜치 분리영역과 활성 영역을 형성하는 과정과, 상기 실리콘 기판에 통상의 필드상 국부 이온주입 공정을 통하여 웰 영역을 형성하는 과정과, 습식 식각을 통하여 트랜치 분리내의 제1산화막을 일부 식각하는 과정과, 산화공정을 진행하여 제2산화막을 형성하는 과정과, 문턱전압을 최적화하기 위한 이온주입하는 과정과, 습식 식각을 통하여 상기 제2산화막을 식각하는 과정과, 통상의 게이트 산화막, 게이트 전극, 소오스 및 드레인을 형성하는 과정을 특징으로 한다.

대표도

도3

명세서

도면의 간단한 설명

도 1은 종래기술에 따른 트랜지스터의 평면도.
도 2는 도 1의 2-2' 방향으로의 수직단면도.
도 3은 본 발명의 일 실시예에 따른 트랜지스터를 보여주는 수직단면도.
도 4a ~ 도 4c는 본 발명의 일 실시예에 따른 트랜지스터의 제조수순을 보여주는 공정단면도.

발명의 상세한 설명

발명의 목적

발명이 속하는 기술분야 및 그 분야의 종래기술

본 발명은 반도체 장치에 관한 것으로, 특히 반도체 장치 중 칩 면적의 증가 없이 채널폭을 증가시킬 수 있는 트랜지스터의 제조방법에 관한 것이다.

일반적으로, 트랜지스터들은 소정의 채널폭과 길이를 가지게 된다. 이러한 채널폭은 트랜지스터의 전류 드라이브 능력과 밀접한 관계를 가지는데, 채널폭이 커지면 커질수록 전류 드라이브 능력은 커지게 된다. 그러나 채널폭을 크게 하면 칩의 집적도면에서 면적이 증가하는 문제점이 발생하게 된다. 도 1은 종래기술에 따른 트랜지스터의 평면도이다. 도 1을 참조하면, 분리 영역 20과, 트랜지스터의 소오스 20 및 드레인 80과, 상기 소오스 20 및 드레인 80 사이의 게이트 60으로 구성된 트랜지스터의 평면도를 보이는 것이다. 여기서 게이트 60 하부에 형성되는 채널폭 W는 소오스 70 및 드레인 80의 폭과 동일하게 형성된다. 또한 채널폭의 증가는 칩 면적 증가로 바로 이어지게 된다. 한편 상기 도 1의 2-2' 방향으로의 수직단면도가 도 2에 보여진다. 도 2를 참조하면, 실리콘 기판 100상에 직접 형성되거나 실리콘 기판 100상에 형성된 웰(Well)내에 형성된 채널 영역 W와 소자 분리를 위한 분리영역 20, 채널폭 W위에 형성된 게이트 산화막 40과 그 상부에 형성된 게이트 전극 60으로 구성되어 있다. 이와같은 구조로 형성시 트랜지스터는 실리콘 기판 100과 평행한 면에 위치하여 트랜지스터의 전류 드라이브방향을 늘리기 위해서 채널폭 W를 늘리게 되면 바로 면적 증가로 이어지게 된다. 이와 같이 채널폭을 증가시키는 것이 면적 증가로 이어지기 때문에 채널폭을 증가시키기 어려운 문제를 해결하기 위하여 미합중국에 등록된 특허등록번호 5,115,289에 개시되어 있는 바와 같이 채널폭의 일부를 수직으로 형성하여 면적 증가 없이 채널폭을 증가시키는 트랜지스터 구조를 제시하고 있다. 이러한 트랜지스터를 형성하기 위한 제조방법을 도시하지는 않았지만 간

략히 설명한다. 실리콘 기판을 $0.1\mu\text{m}$ 의 폭 및 $1\mu\text{m}$ 깊이로 식각한 후 채널이 형성될 부위를 실리콘 산화막(SiO_2)과 실리콘 질화막(SiN)으로 감싸도록 형성한다. 다음으로 산화공정을 통하여 채널 영역을 기판과 분리시킨 후 실리콘 질화막과 실리콘 산화막을 제거하고 게이트 산화막과 게이트를 형성하며, 이후 드레인 과 소오스를 형성하는 등의 통상의 트랜지스터 형성 공정을 통해 트랜지스터를 제조한다. 전술한 바와 같이 절연막 상 실리콘(Silicon On Insulator: 이하 SOI라 칭함) 공정을 채용함으로써 채널 영역을 실리콘 기판으로부터 분리하였기 때문에 SOI 형성을 위한 산화공정시 버즈빅(Bird's beak)에 의해 채널 영역이 기판과 완전히 분리되어야 한다. 따라서 채널폭이 모두 $0.1\mu\text{m}$ 이어야 한다. 그러므로 큰 사이즈의 패턴은 형성이 곤란하다. 또한 모든 패턴을 $0.1\mu\text{m}$ 이하로 형성한다고 해도 산화공정시 채널 영역이 리프팅(Lifting)되는 등의 문제점이 발생된다. 이밖에도 SOI를 위한 산화공정시 채널 영역이 산화되는 것을 막기 위하여 채널 영역을 실리콘 질화막으로 감싸주어야 하는 공정이 필요하므로 공정이 복잡해지는 문제점이 발생한다.

발명이 이루고자 하는 기술적 과제

본 발명의 목적은 채널 영역의 일부를 수직으로 형성하여 칩의 면적 증가없이 채널폭을 증가시킴으로써 트랜지스터의 전류 드라이브 능력을 향상시킬 수 있는 반도체 장치의 트랜지스터 제조방법을 제공함에 있다.

본 발명의 다른 목적은 칩의 면적 증가 없이 채널폭을 증가시키는데 있어 리프팅을 제거할 수 있는 반도체 장치의 트랜지스터 제조방법을 제공함에 있다.

본 발명의 또다른 목적은 채널폭을 증가시킴과 동시에 트랜치의 깊이를 조절함으로써 추가 공정없이 분리 영역 특성을 향상시킬 수 있는 반도체 장치의 트랜지스터 제조방법을 제공함에 있다.

본 발명의 또다른 목적은 채널폭을 증가시킴과 동시에 분리 영역 형성 공정시 공정 수를 줄일 수 있는 반도체 장치의 트랜지스터 제조방법을 제공함에 있다.

발명의 구성 및 작용

상기한 목적들을 달성하기 위한 본 발명의 기술적 사상에 따르면, 반도체 장치의 트랜지스터 제조방법에 있어서, 실리콘 기판에 통상의 통상의 트랜치 분리 공정을 통하여 트랜치 분리영역과 활성 영역을 형성하는 과정과, 상기 실리콘 기판에 통상의 필드상 국부 이온주입 공정을 통하여 웰 영역을 형성하는 과정과, 습식 식각을 통하여 트랜치 분리내의 제1산화막을 일부 식각하는 과정과, 산화공정을 진행하여 제2산화막을 형성하는 과정과, 문턱전압을 최적화하기 위한 이온주입하는 과정과, 습식 식각을 통하여 상기 제2산화막을 식각하는 과정과, 통상의 게이트 산화막, 게이트 전극, 소오스 및 드레인을 형성하는 과정을 포함한다.

이하 본 발명의 바람직한 실시예를 첨부한 도면을 참조하여 상세히 설명한다. 우선 각 도면의 구성요소들에 참조부호를 부가함에 있어서, 동일한 구성요소들에 한해서는 비록 다른 도면상에 표시되더라도 가능한 한 동일한 부호를 가지도록 하고 있음에 유의해야 한다.

도 3은 본 발명의 일실시예에 따른 트랜지스터를 보여주는 수직단면도이다. 도 3을 참조하면, 실리콘 기판 101상에 분리 영역을 21a이 형성되고, 상기 분리 영역을 21a 사이에 게이트가 형성되는데 이때 실리콘 기판 101이 분리 영역 21a의 상부보다 소정 높이 올라간 부위에 게이트 산화막 41 및 그 상부에 게이트 전극 61이 형성된다. 따라서 채널폭이 분리 영역 21a 보다 소정 높이 올라가며 그 높이만큼 곡선을 이루게 되어 채널폭이 증가하게 된다. 또한 칩의 면적은 변동이 없다.

도 4a ~ 도 4c는 본 발명의 일실시예에 따른 트랜지스터의 제조수순을 보여주는 공정단면도이다. 도 4a를 참조하면, 실리콘 기판 101에 통상의 트랜치 분리공정을 통하여 트랜치 분리 영역 21을 형성하고 통상의 LIF(Local Implantation on Field) 공정을 통하여 웰 영역을 형성한다. 도 4b를 참조하면, 습식 식각 공정을 통하여 채널폭을 증가시키고자 하는 영역의 트랜치 분리내의 산화막 21a를 $10\text{nm} \sim 200\text{nm}$ 정도 식각한다. 또한 희생산화막을 $10\text{nm} \sim 30\text{nm}$ 정도 진행하여 각이 진 부위의 채널 영역을 보다 더 곡면이 되도록 하여 채널폭 W를 증가시킨다. 다음으로 트랜지스터의 문턱전압을 최적화하기 위한 이온주입을 $3.0 \times 10^{11}/\text{cm}^2 \sim 2.0 \times 10^{12}/\text{cm}^2$ 정도 실시한 후 희생 산화막을 습식 식각을 통해 식각한다. 따라서 분리 영역내에 채워진 산화막 21a가 실리콘 기판 101 보다 아래로 형성됨을 알 수 있다. 도 4c를 참조하면, 상기 공정이후 게이트 산화막 41의 형성 공정과 소오스 및 드레인 형성 공정을 통해 트랜지스터를 형성한다.

한편, 전술한 바와 같은 공정을 통하여 통상의 트랜치 분리 형성 공정에 일부의 공정만을 추가함으로써 트랜지스터의 채널폭을 증가시키게 되어 면적의 증가 없이 전류 드라이브 능력을 증가시킬 수 있게 된다. 또한 이러한 제조 공정은 트랜치내의 산화막의 깊이를 조절함으로써 트랜지스터의 채널폭을 증가시키면서도 안정적인 분리 특성을 얻을 수도 있다. 한편, 희생 산화막을 통하여 채널의 각진 부위가 더욱 곡면이 되도록 하는 이유는 트랜지스터 동작시 서브 문턱 영역에서의 험프(Hump) 효과를 완화하기 위함이다.

발명의 효과

상기한 본 발명에 따르면, 칩 면적의 증가없이 트랜지스터의 채널폭을 증가시킬 수 있는 효과를 가지며, 이에 따른 트랜치 깊이를 조절함으로써 안정적인 분리 특성을 얻을 수 있는 효과를 가진다.

상기한 본 발명은 도면을 중심으로 예를들어 한정되었지만, 그 동일한 것은 본 발명의 기술적 사상을 벗어나지 않는 범위내에서 여러가지 변화와 변형이 가능함이 본 분야의 숙련된 자에게 있어 명백할 것이다.

(57) 청구의 범위

청구항 1

반도체 장치의 트랜지스터 제조방법에 있어서,
 실리콘 기판에 통상의 트렌치 분리 공정을 통하여 트렌치 분리영역과 활성 영역을 형성하는 과정과,
 상기 실리콘 기판에 통상의 필드상 국부 이온주입 공정을 통하여 웰 영역을 형성하는 과정과,
 습식 식각을 통하여 트렌치 분리내의 제1산화막을 일부 식각하는 과정과,
 산화공정을 진행하여 제2산화막을 형성하는 과정과,
 문턱전압을 최적화하기 위한 이온주입하는 과정과,
 습식 식각을 통하여 상기 제2산화막을 식각하는 과정과,
 통상의 게이트 산화막, 게이트 전극, 소오스 및 드레인을 형성하는 과정을 포함함을 특징으로 하는 반도체 장치의 트랜지스터 제조방법.

청구항 2

제1항에 있어서, 상기 제1산화막의 식각 후 두께는 10나노 미터에서 200나노 미터로 형성됨을 특징으로 하는 반도체 장치의 트랜지스터 제조방법.

청구항 3

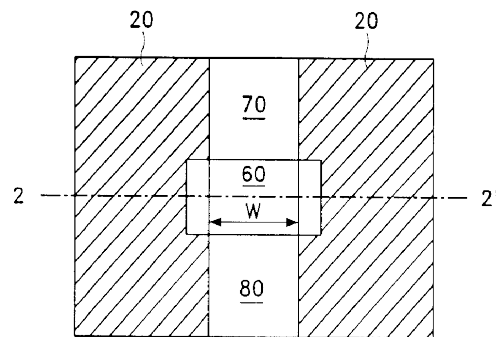
제1항에 있어서, 상기 제2산화막의 두께는 10나노 미터에서 30나노 미터로 형성됨을 특징으로 하는 반도체 장치의 트랜지스터 제조방법.

청구항 4

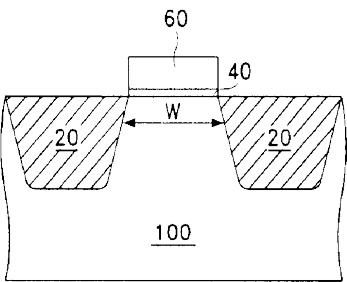
제1항에 있어서, 상기 이온주입의 불순물은 불화붕소로 40킬로 전자볼트에서 60킬로 전자볼트로 단위면적당 3×10^{11} 에서 2×10^{12} 농도로 이온주입됨을 특징으로 하는 반도체 장치의 트랜지스터 제조방법.

도면

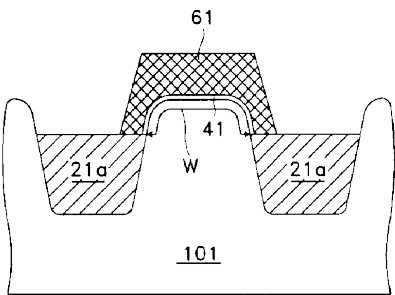
도면1



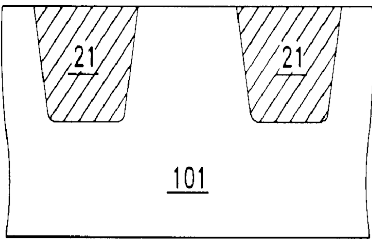
도면2



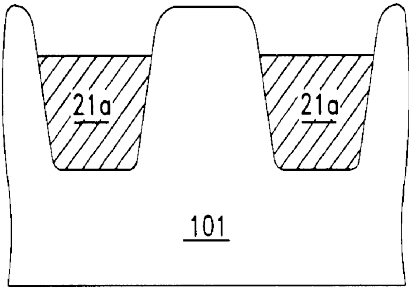
도면3



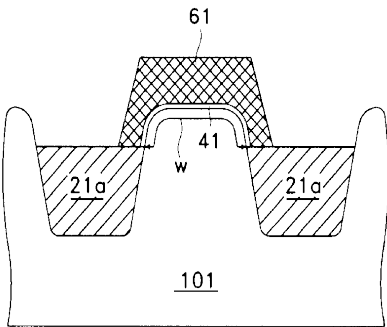
도면4a



도면 4b



도면 4c




CERTIFICATE OF TRANSLATION ACCURACY

I, Alex Jo, declare:

1. I am a professional translator specializing in translating Korean to English and vice versa.
2. I have over 25 years of experience translating thousands of technical, legal, and business documents from Korean to English submitted to, among others, various U.S. federal courts and the ITC.
3. I certify that the Korean to English translation of this patent document (Application No. KR1997-010326) is a true, correct and complete translation to the best of my knowledge and ability.

I hereby certify under penalty of perjury that the foregoing is true and correct. Executed this 13th day of April 2020 in the Contra Costa County of the State of California.

By: 

Alex N. Jo
Member, ATA

SMIC Ex. 1003
IPR2020-01003
Page 6 of 11

(19) Korean Intellectual Property Office (KIPO) (KR)
(12) Laid-Open Patent Application Gazette (A)

(51) Int. Cl.⁶
H01L 21/33

(11) Laid-Open Disclosure No.: KR1998-074469
(43) Laid-Open Disclosure Date: November 5, 1998

| | |
|-----------------------|--|
| (21) Application No. | KR1997-010326 |
| (22) Application date | March 25, 1997 |
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Request for Examination: Not requested

(54) Method of manufacturing a transistor for a semiconductor device

ABSTRACT

The present invention relates to a semiconductor device. In a method of manufacturing a transistor for a semiconductor device, the summary of the present invention comprises: a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process; a process of forming a well region on the silicon substrate by means of a conventional process of local ion implantation on the field; a process of partially etching a first oxide film inside the trench isolation by means of wet etching; a process of forming a second oxide film by performing an oxidation process; a process of ion implantation for optimization of the threshold voltage; a process of etching the second oxide film by means of wet etching; and a process of forming conventional gate oxide film, gate electrode, source, and drain.

REPRESENTATIVE DRAWING

FIG. 3

SPECIFICATION

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1 is a plan view of a transistor according to the prior art.

FIG. 2 is a vertical cross-sectional view along the 2-2' direction in FIG. 1.

FIG. 3 is a vertical cross-sectional view illustrating a transistor according to one embodiment of the present invention.

FIGS. 4a to 4c are the process cross-sectional views illustrating the sequence of manufacturing a transistor according to one embodiment of the present invention.

DETAILED DESCRIPTION OF THE INVENTION

THE OBJECT OF THE INVENTION

TECHNICAL FIELD RELATED TO THE INVENTION AND CONVENTIONAL TECHNOLOGY

The present invention relates to a semiconductor device and, more particularly, to a method of manufacturing a transistor that can increase the channel width without increasing the chip area in a semiconductor device.

Generally, transistors have predetermined channel width and length. Such a channel width is closely related to the electric current driving capability of the transistor. The wider the channel width becomes, the higher the electric current driving capability becomes. However, increasing the channel width causes a problem that the area increases in terms of chip integration. FIG. 1 is a plan view of a transistor according to the prior art. With reference to FIG. 1, it illustrates a plan view comprising an isolation region 20, a source 20 [sic] and a drain 80 of a transistor, and a gate 60 between the source 20 and the drain 80. Here, the width W of the channel formed at the lower part of the gate 60 is formed with the same width as that of the source 70 and the drain 80. Also, an increase in the channel width immediately results in an increase in the chip area. On another note, a vertical cross-sectional view in the 2-2' direction of FIG. 1 is shown in FIG. 2. With reference to FIG. 2, it comprises: a channel region W directly formed on a silicon substrate 100 or formed inside a well formed on a silicon substrate 100; an isolation region 20 for isolating the device; a gate oxide film 40 formed on top of channel width W; and a gate electrode 60 formed thereon. When formed in a structure like this, a transistor is positioned on a surface that runs in parallel with the silicon substrate 100 and, when the channel width W is increased to increase the current-driving amount of a transistor, it immediately results in an increase in the size of the area. Since increasing the channel width immediately results in an increase in the size of the area, Patent No. 5,115,289 registered in the U.S. presents, as disclosed therein, a transistor structure to increase the channel width without increasing the area by vertically forming a part of the channel width to thereby solve the problem that made it difficult to increase the channel width. Although not illustrated, a manufacturing method to form such a transistor will now be briefly described here. After etching a silicon substrate with the width of 0.1 μm and depth of 1 μm, the area where a channel will be formed is formed in such a way as to be wrapped up with a silicon oxide film SiO₂ and a silicon nitride film SiN. Next, after isolating the channel region from the substrate by means of an oxidation process, the silicon nitride film and the silicon oxide film are removed; and the gate oxide film and the gate

are formed. Then, a transistor is manufactured by means of a conventional transistor formation process such as forming a drain and a source, etc. Since the channel region is isolated from the silicon substrate by adopting a process of Silicon-On-Insulator ("SOI"), as described earlier, the channel region must be completely isolated from the substrate by "bird's beak" during the oxidation process to form SOI. Accordingly, all the channel widths must be 0.1 μm . Consequently, it becomes difficult to form a large-size pattern. Also, even though all the patterns are formed at 0.1 μm or less, it causes a problem, among others, that the channel region is lifted during the oxidation process. In addition, a process of wrapping the channel region with a silicon nitride film is required to prevent oxidation of the channel region during the oxidation process for SOI, which causes a problem that the process becomes complicated.

TECHNICAL PROBLEM TO BE SOLVED BY THE PRESENT INVENTION

It is the object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can improve the electric current driving capability of a transistor by increasing the channel width without increasing the chip area by vertically forming a part of the channel region.

It is another object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can eliminate the problem of lifting in increasing the channel width without increasing the chip area.

It is yet another object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can improve the characteristics of the isolation region without introducing any additional process by increasing the channel width and, at the same time, adjusting the depth of the trench.

It is yet another object of the present invention to provide a method of manufacturing a transistor for a semiconductor device that can increase the channel width and, at the same time, decrease the number of processes while forming an isolation region.

CONSTRUCTION AND OPERATION OF THE PRESENT INVENTION

According to the technical ideas of the present invention to achieve the objects described above, the method of manufacturing a transistor for a semiconductor device comprises: a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process; a process of forming a well region on the silicon substrate by means of a conventional process of local ion implantation on the field; a process of partially etching a first oxide film inside the trench isolation by means of wet etching; a process of forming a second oxide film by performing an oxidation process; a process of ion implantation for optimization of the threshold voltage; a process of etching the second oxide film by means of wet etching; and a process of forming conventional gate oxide film, gate electrode, source, and drain.

Hereinunder, a preferred embodiment of the present invention will be explained in detail with reference to the attached drawings. For starters, in assigning referential symbols to indicate the constitutive elements of respective drawings, it should be noted that, even in cases where they are indicated on different drawings, insofar as they are identical constitutive elements, they are to have the same symbols to the extent possible.

FIG. 3 is a vertical cross-sectional view illustrating a transistor according to one embodiment of the present invention. With reference to FIG. 3, isolation regions **21a** are formed on a silicon substrate **101** and gates are formed between the isolation regions **21a**. Here, a gate oxide film **41** is formed on the area where the silicon substrate is higher by a predetermined height relative to the upper part of the isolation region **21a**; and a gate electrode **61** is formed on the upper part thereof. Accordingly, the channel width is raised by a predetermined height relative to the isolation region **21a** and for a curve by as much as the height, thereby increasing the channel width. In doing so, there will not be any change in the chip area.

FIGS. 4a to 4c are the cross-sectional views of the fabrication process, and as such they illustrate the sequence of manufacturing a transistor according to one embodiment of the present invention. With reference to FIG. 4a, a trench isolation region **21** is formed on a silicon substrate **101** by means of a conventional trench isolation process and a well region is formed on a conventional Local Implantation on Field **LIF** process. With reference to FIG. 4b, the oxide film **21a** inside the trench isolation in the region desired to increase the channel width is etched by 10nm - 200nm by means of a wet etching process. Also, the sacrificial oxide film is sacrificed by 10nm - 30nm to allow the channel region in the angular part to become a more curved surface, thereby increasing the channel width **W**. Then, ion implantation to optimize the threshold voltage of the transistor is performed for $3.0 \times 10^{11}/\text{cm}^2$ - $2.0 \times 10^{12}/\text{cm}^2$ and, after that, the sacrificial film is etched by wet etching. Accordingly, it is shown that the oxide film **21a** filled in the isolation region is formed underneath the silicon substrate **101**. With reference to FIG. 4c, after the process described above is performed, a transistor is formed by means of a gate oxide **41** formation process and a source and drain formation process.

Meanwhile, by means of the processes described above, only a few processes are added to the conventional trench isolation process to increase the channel width of a transistor, which increases the electric current driving capability without increasing the area. Also, such a manufacturing process makes it possible to obtain stable isolation characteristics while increasing the channel width of a transistor by adjusting the depth of the oxide film in the trench. Meanwhile, the purpose of making the angular part of the channel become a more curved surface by means of the sacrificial oxide film is to mitigate the hump effect in the sub-threshold region during an operation of the transistor.

EFFECT OF THE INVENTION

The present invention described above has an effect of increasing the channel width of a transistor without increasing the chip area and obtaining stable isolation characteristics by adjusting the trench depth as a result thereof.

While the present invention has been described with examples focused on the drawings, it will be apparent to those skilled in the art that various changes and modifications may be made without departing from the scope of the technical ideas of the present invention.

(57) What is claimed is**Claim 1**

A method of manufacturing a transistor for a semiconductor device comprising:

- a process of forming a trench isolation region and an active region on a silicon substrate by means of a conventional trench isolation process;
- a process of forming a well region on the silicon substrate by means of a conventional process of localized ion implantation on the field;
- a process of partially etching a first oxide film inside the trench isolation by means of wet etching;
- a process of forming a second oxide film by performing an oxidation process;
- a process of ion implantation for optimization of the threshold voltage;
- a process of etching the second oxide film by means of wet etching; and
- a process of forming conventional gate oxide film, gate electrode, source, and drain.

Claim 2

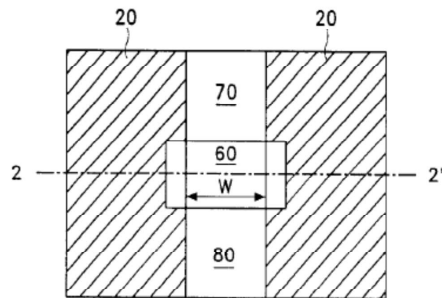
A method of manufacturing a transistor for a semiconductor device, according to claim 1, wherein the post-etching thickness of the first oxide film is formed at 10nm - 200nm.

Claim 3

A method of manufacturing a transistor for a semiconductor device, according to claim 1, wherein the thickness of the second oxide film is formed at 10nm - 30nm.

Claim 4

A method of manufacturing a transistor for a semiconductor device, according to claim 1, wherein the impurity in the ion implantation is boron fluoride being ion implanted in the concentration of 3.0×10^{11} - 2.0×10^{12} per unit area at 40 KeV - 60 KeV.

DRAWINGS**FIG. 1**

3-5

FIG. 2

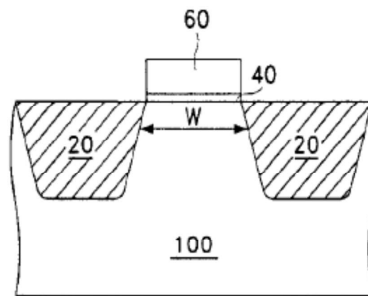


FIG. 3

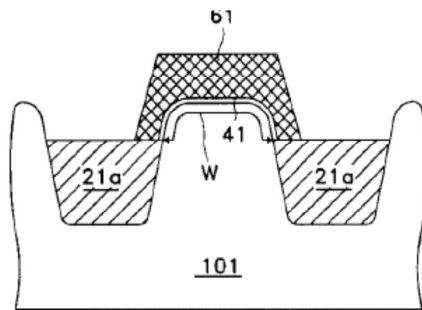
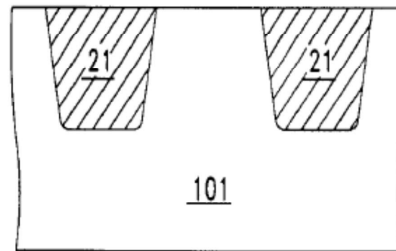


FIG. 4



4-5

FIG. 4b

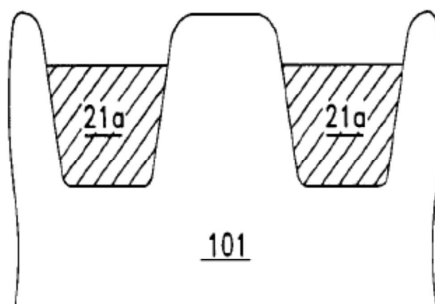
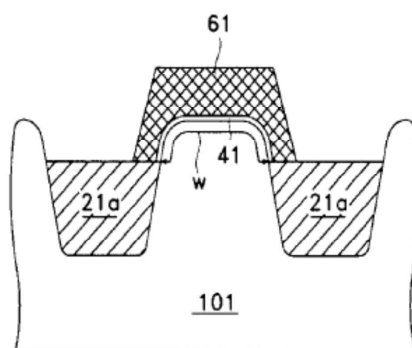


FIG. 4c



5-5



US005960297A

United States Patent [19]
Saki[11] **Patent Number:** **5,960,297**[45] **Date of Patent:** **Sep. 28, 1999**[54] **SHALLOW TRENCH ISOLATION
STRUCTURE AND METHOD OF FORMING
THE SAME**[75] Inventor: **Kazuo Saki**, Yokohama, Japan[73] Assignee: **Kabushiki Kaisha Toshiba**, Kawasaki,
Japan[21] Appl. No.: **08/887,137**[22] Filed: **Jul. 2, 1997**[51] **Int. Cl.**⁶ **H01L 21/762**[52] **U.S. Cl.** **438/424; 438/296**[58] **Field of Search** 438/424, 425,
438/426, 435, 436, 437, 296[56] **References Cited****U.S. PATENT DOCUMENTS**

| | | | |
|-----------|---------|----------------|---------|
| 4,465,532 | 8/1984 | Fukano | 156/643 |
| 4,580,330 | 4/1986 | Pollack et al. | 29/576 |
| 4,994,406 | 2/1991 | Vasquez | 437/67 |
| 5,298,450 | 3/1994 | Verret | 437/67 |
| 5,346,584 | 9/1994 | Nasr et al. | 156/636 |
| 5,356,828 | 10/1994 | Swan et al. | 437/67 |
| 5,358,894 | 10/1994 | Fazan et al. | 437/70 |
| 5,457,339 | 10/1995 | Komori et al. | 257/510 |

| | | | |
|-----------|---------|------------------|---------|
| 5,498,566 | 3/1996 | Lee | 437/67 |
| 5,521,422 | 5/1996 | Mandelman et al. | 257/510 |
| 5,578,518 | 11/1996 | Koike et al. | 437/67 |
| 5,712,185 | 1/1998 | Tsai et al. | 437/67 |
| 5,753,554 | 5/1998 | Park | 438/296 |
| 5,766,823 | 6/1998 | Fumitomo | 430/314 |
| 5,863,827 | 1/1999 | Joyner | 438/425 |

Primary Examiner—Olik Chaudhuri*Assistant Examiner*—Daniel H. Mao*Attorney, Agent, or Firm*—Banner & Witcoff, Ltd.[57] **ABSTRACT**

An isolation structure is provided by a method which includes forming a pad oxide layer on a semiconductor substrate and then forming a pad nitride layer on the pad oxide layer. An opening is then formed which extends through the pad nitride layer, the pad oxide layer, and into the semiconductor substrate. The pad nitride layer is then isotropically etched, thereby pulling-back the pad nitride layer from the portion of the opening extending through the pad oxide layer. An insulating layer is formed to fill in the opening including the portion of the opening formed by the pulling-back of the pad nitride layer. The deposited insulating layer is then planarized using the pulled-back nitride layer as a stopper layer. The pulled-back pad nitride layer and the pad oxide layer are then removed.

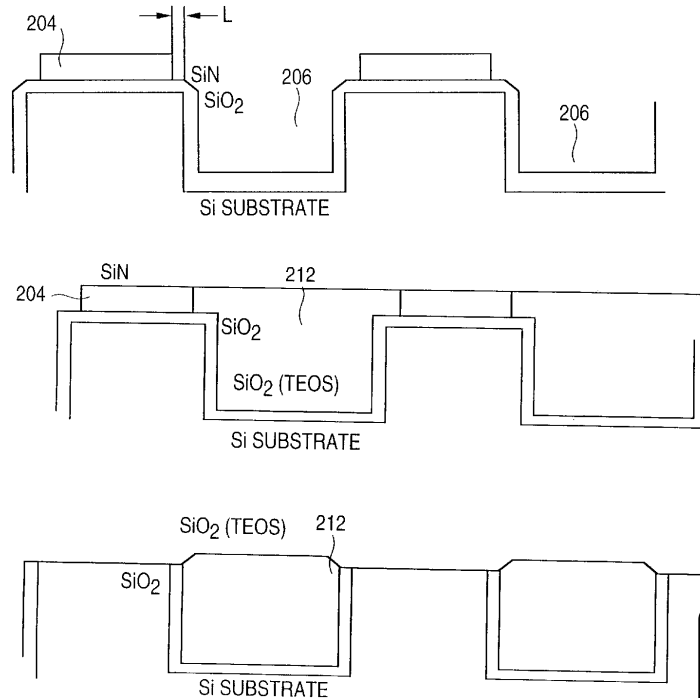
12 Claims, 19 Drawing Sheets**SMIC Ex. 1006**
IPR2020-01003
Page 1 of 26

FIG. 1(a)

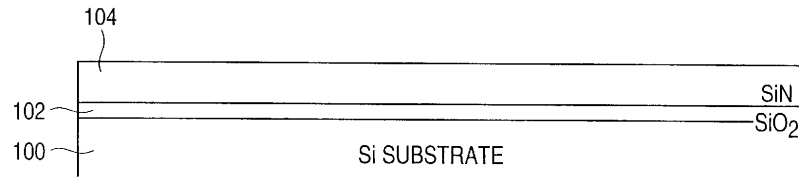


FIG. 1(b)

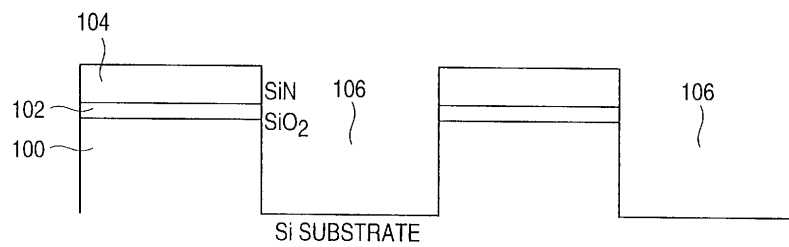
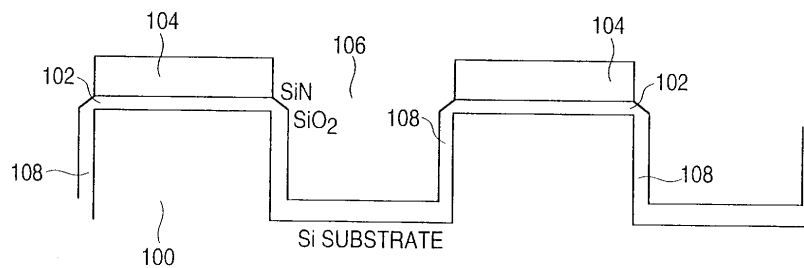


FIG. 1(c)



SMIC Ex. 1006
IPR2020-01003
Page 2 of 26

FIG. 1(d)

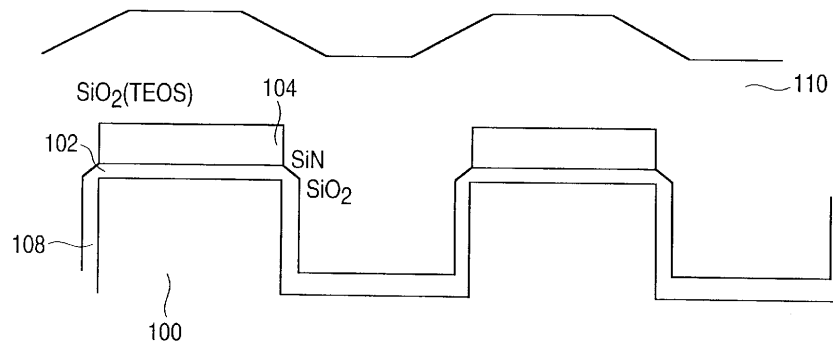


FIG. 1(e)

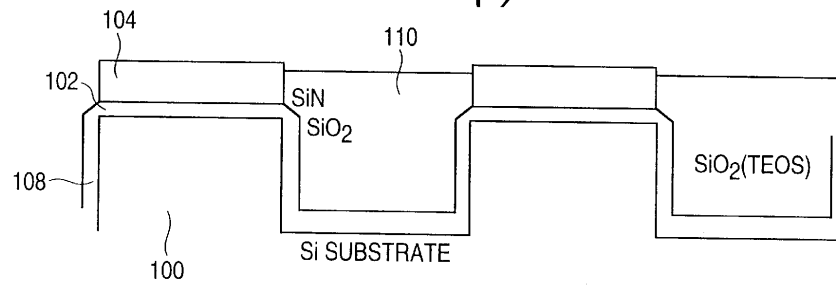


FIG. 1(f)

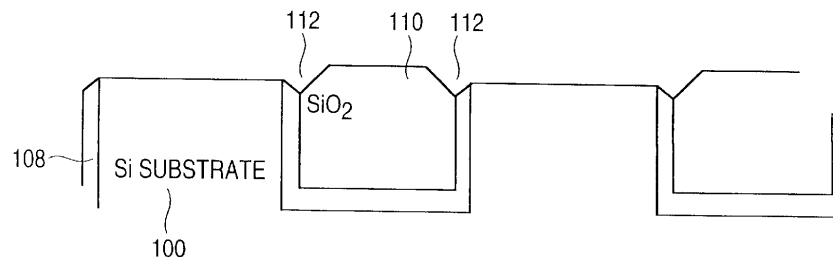


FIG. 2

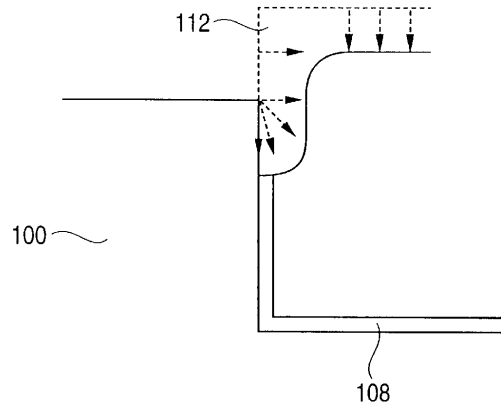


FIG. 3(a)

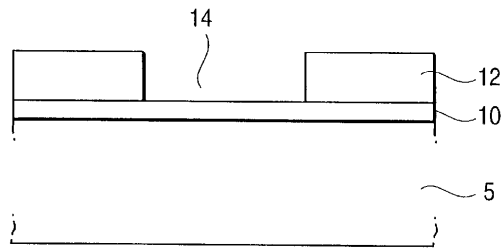
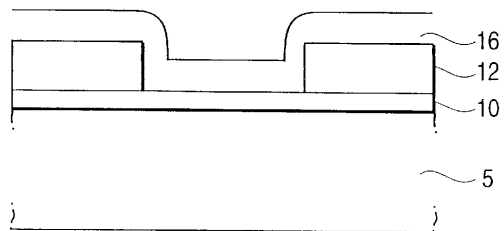


FIG. 3(b)



SMIC Ex. 1006
IPR2020-01003
Page 4 of 26

FIG. 3(c)

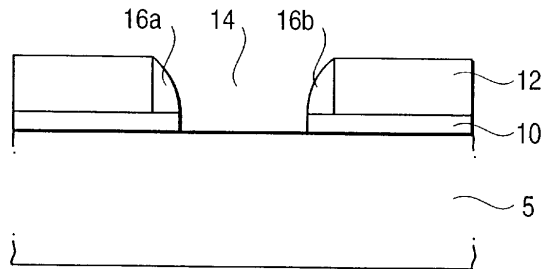


FIG. 3(d)

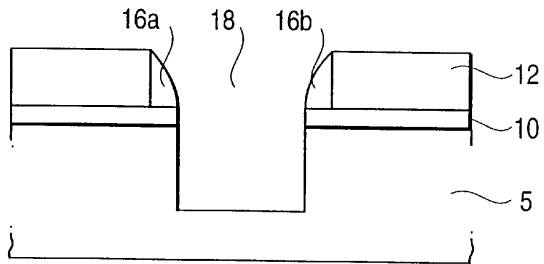
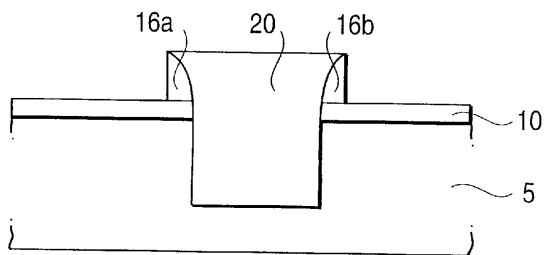


FIG. 3(e)



SMIC Ex. 1006
IPR2020-01003
Page 5 of 26

FIG. 3(f)

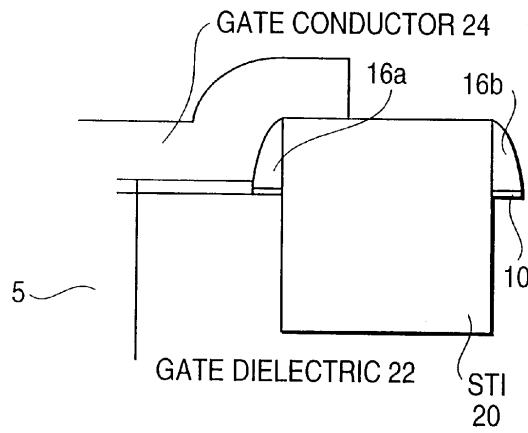
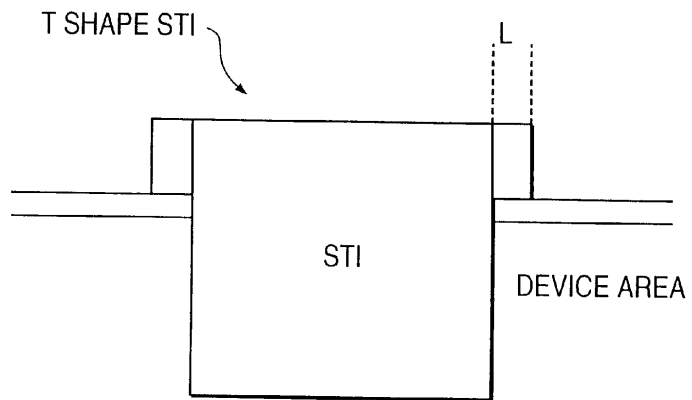


FIG. 4



SMIC Ex. 1006
IPR2020-01003
Page 6 of 26

FIG. 5(a)

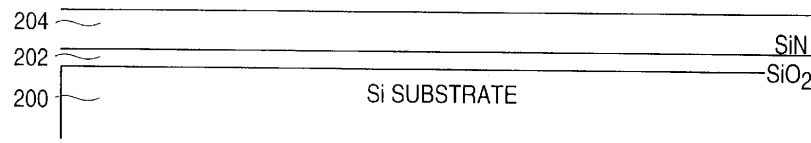


FIG. 5(b)

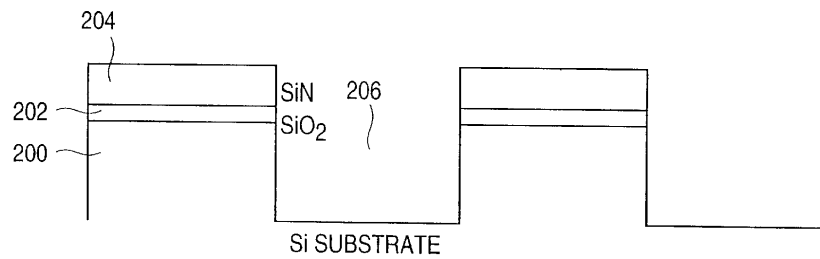


FIG. 5(c)

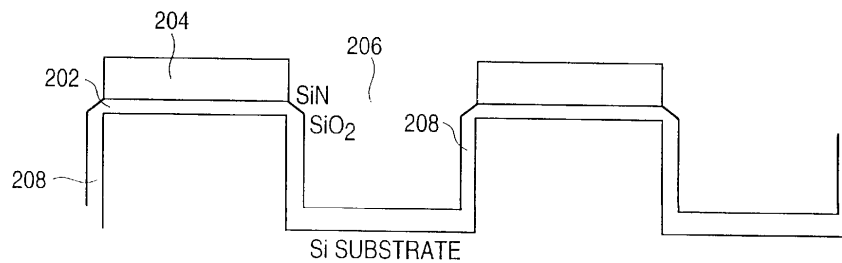


FIG. 5(f)

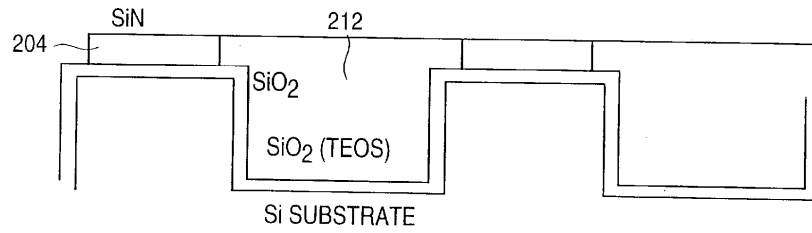


FIG. 5(g)

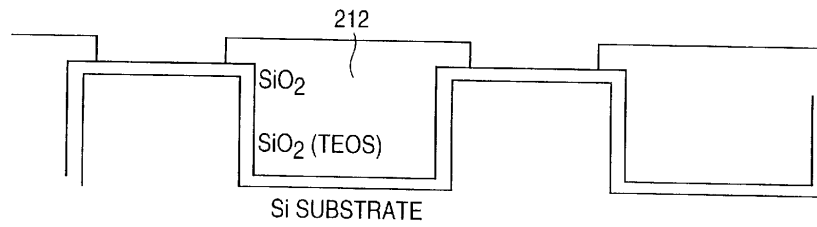


FIG. 5(h)

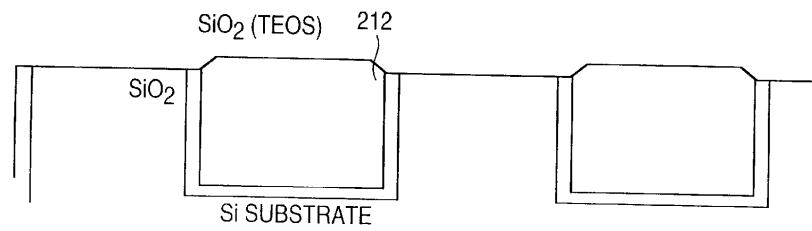


FIG. 5(i)

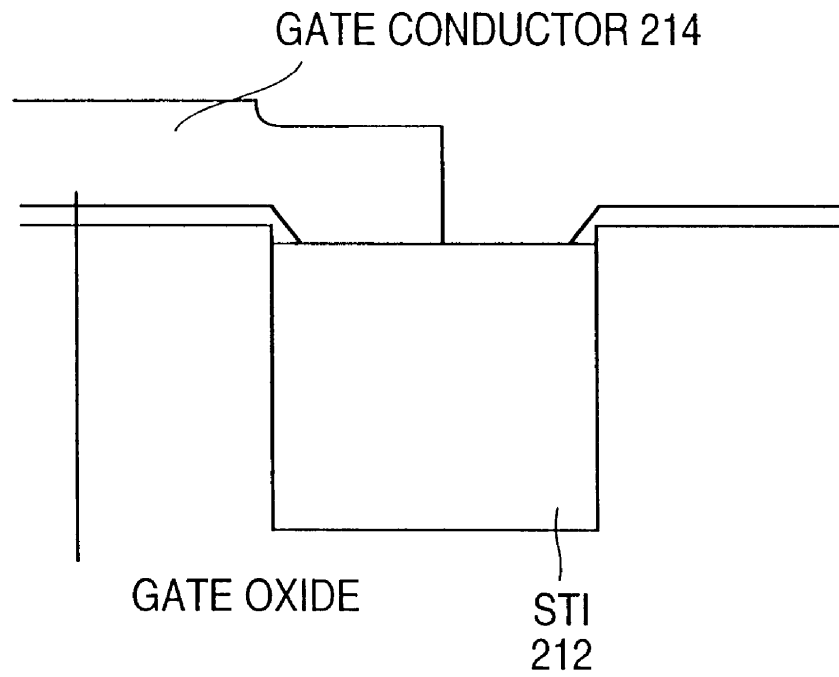


FIG. 6(a)

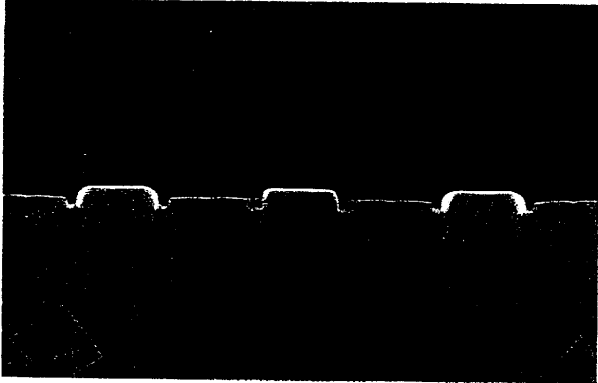
| PULL BACK CONDITION | STI SHAPE |
|------------------------|--|
| PULL BACK 100A |  |

FIG. 6(b)

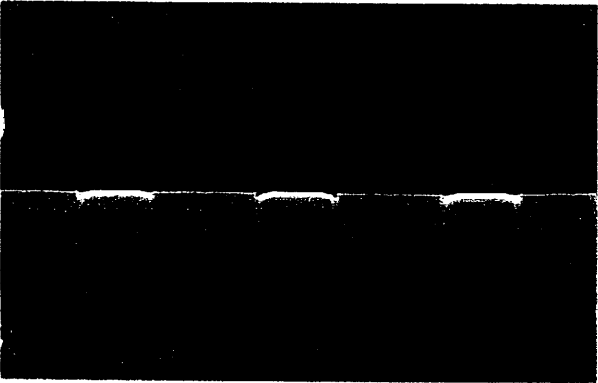
| PULL BACK CONDITION | STI SHAPE |
|------------------------|--|
| PULL BACK 300A |  |

FIG. 7(a)

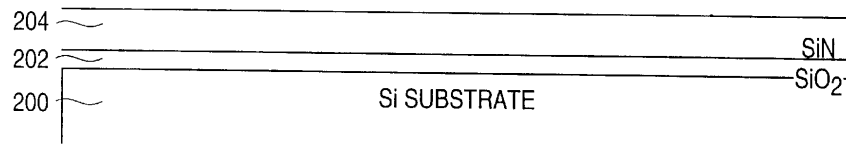


FIG. 7(b)

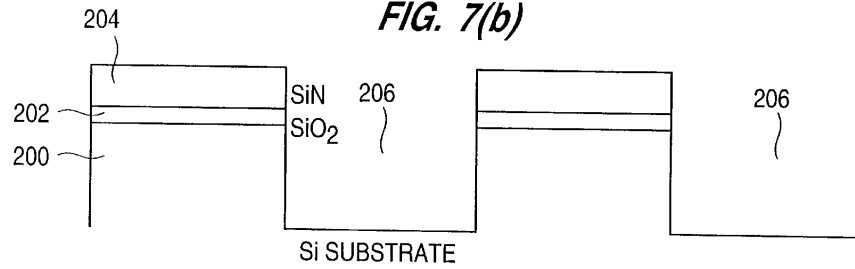


FIG. 7(c)

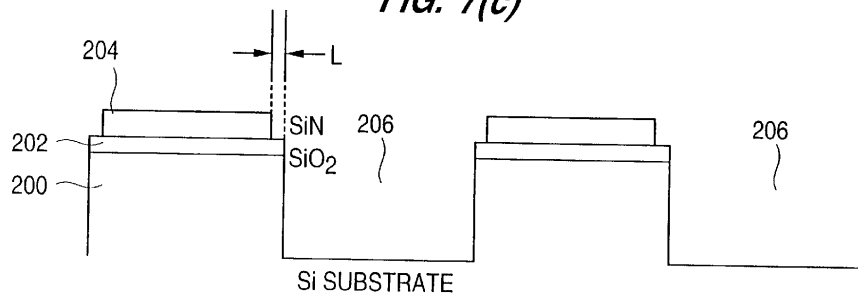


FIG. 7(d)

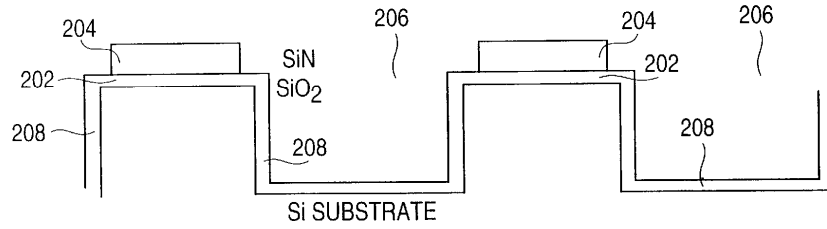


FIG. 7(e)

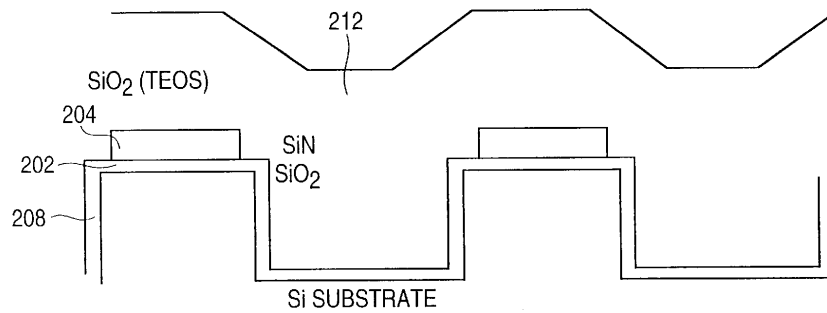


FIG. 7(f)

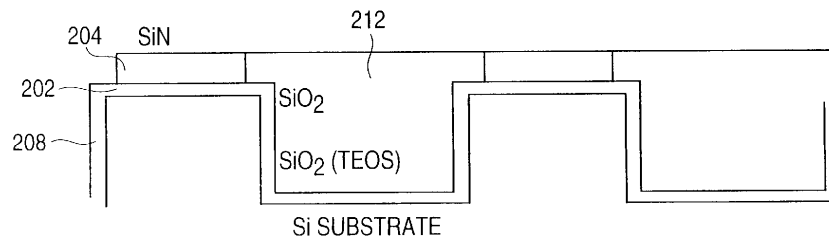


FIG. 7(g)

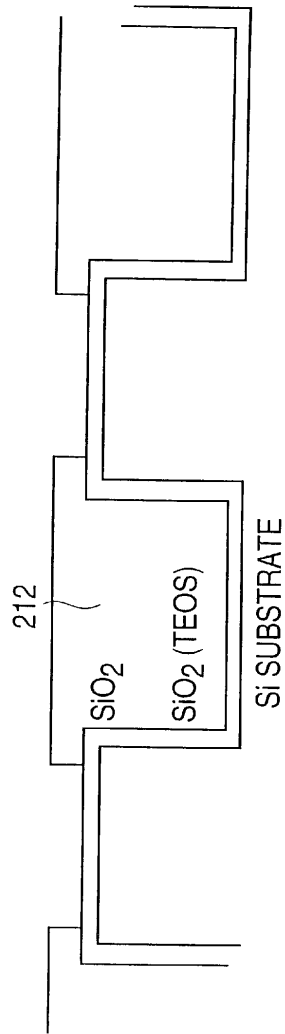


FIG. 7(h)

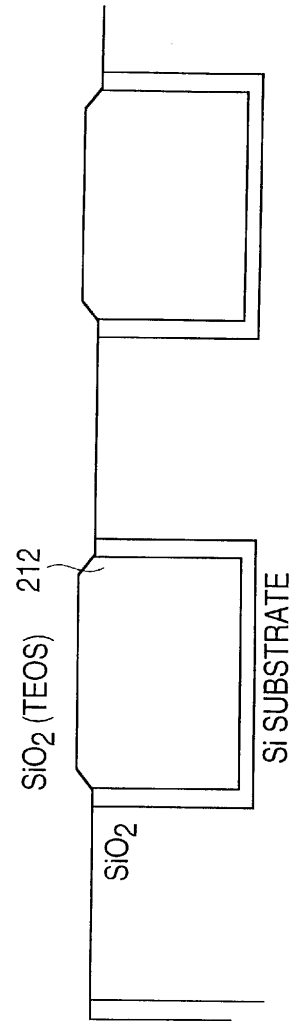


FIG. 8(a)

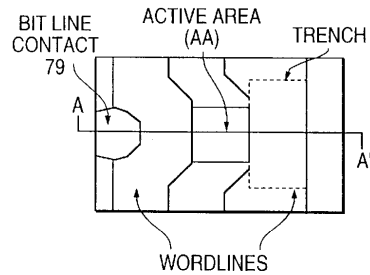
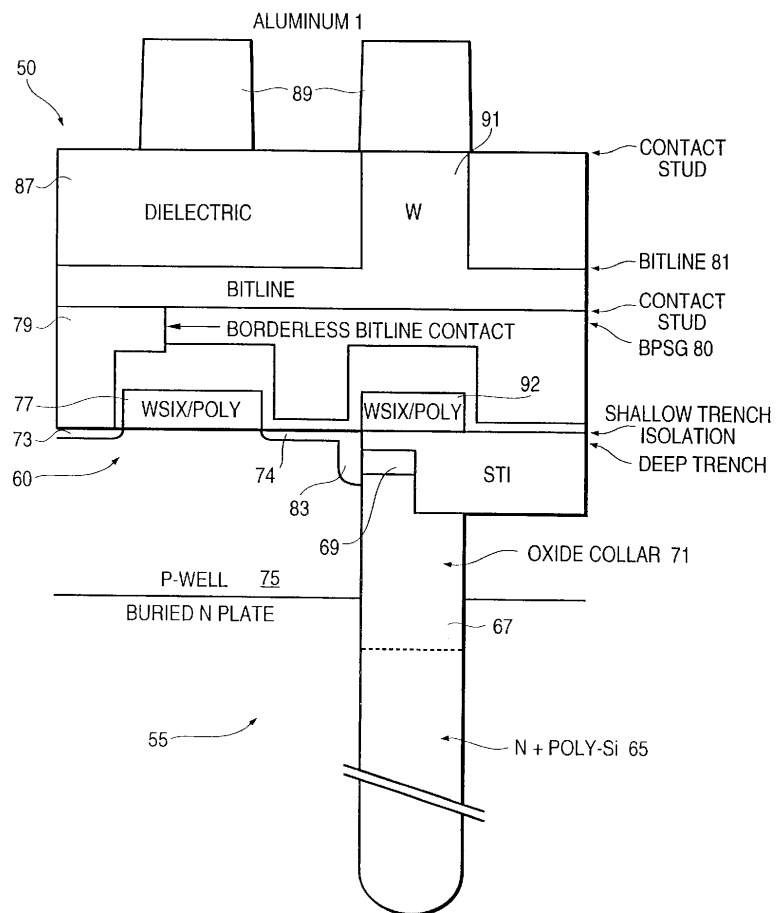


FIG. 8(b)



SMIC Ex. 1006
IPR2020-01003
Page 15 of 26

FIG. 9(a)

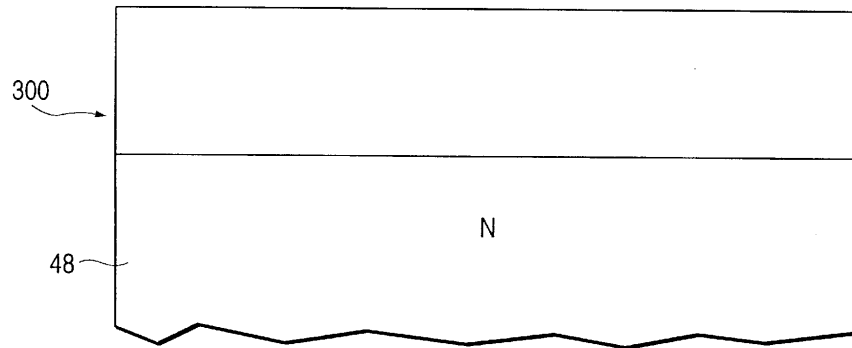


FIG. 9(b)

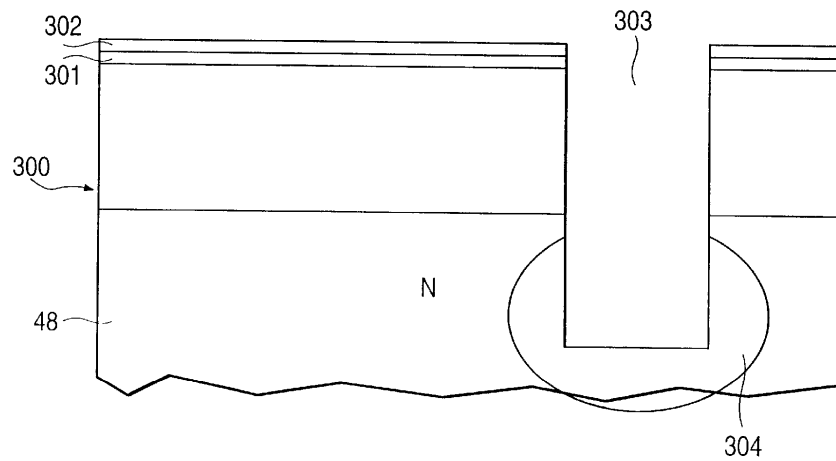


FIG. 9(c)

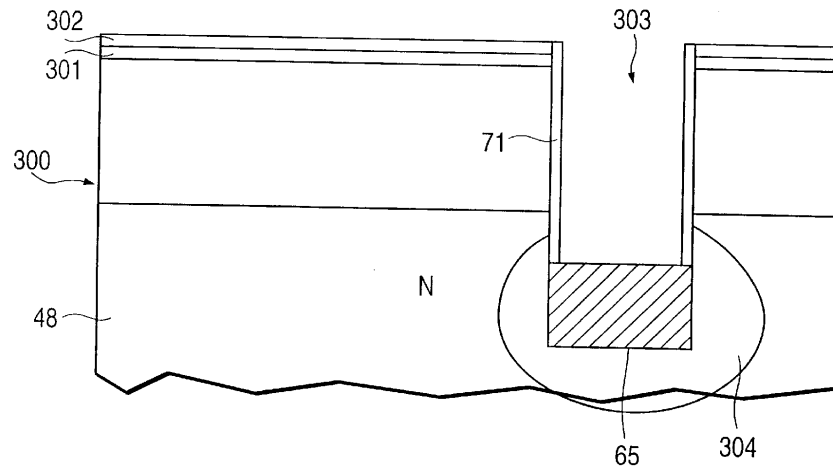
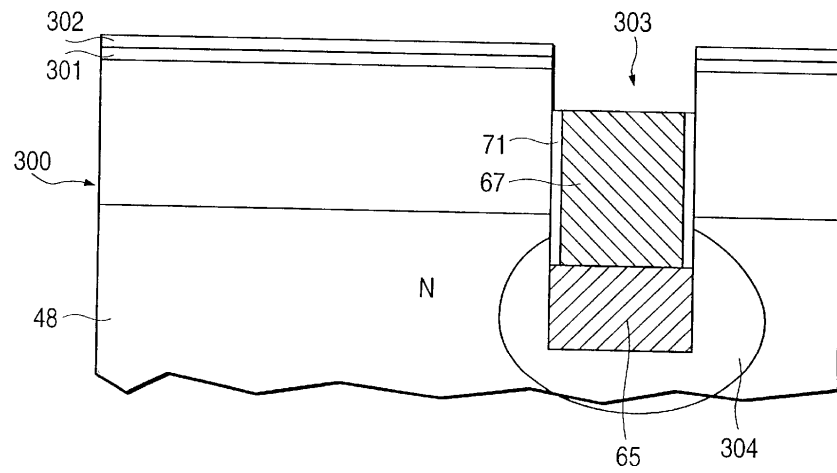


FIG. 9(d)



SMIC Ex. 1006
IPR2020-01003
Page 17 of 26

FIG. 9(e)

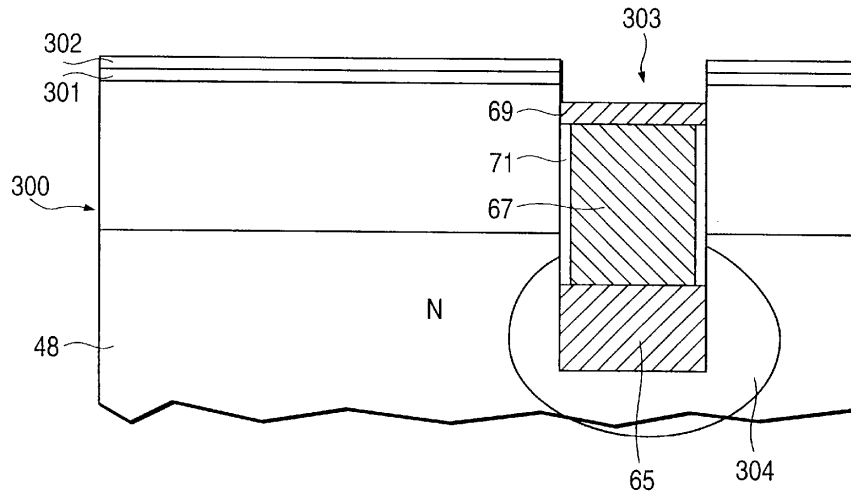
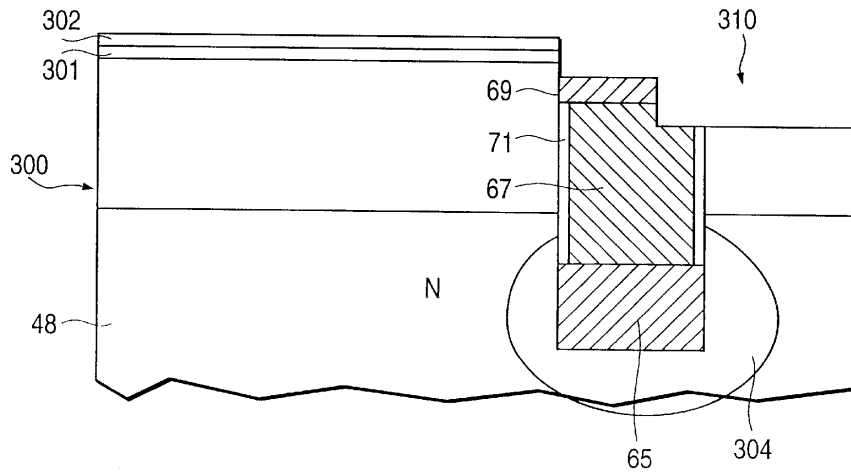
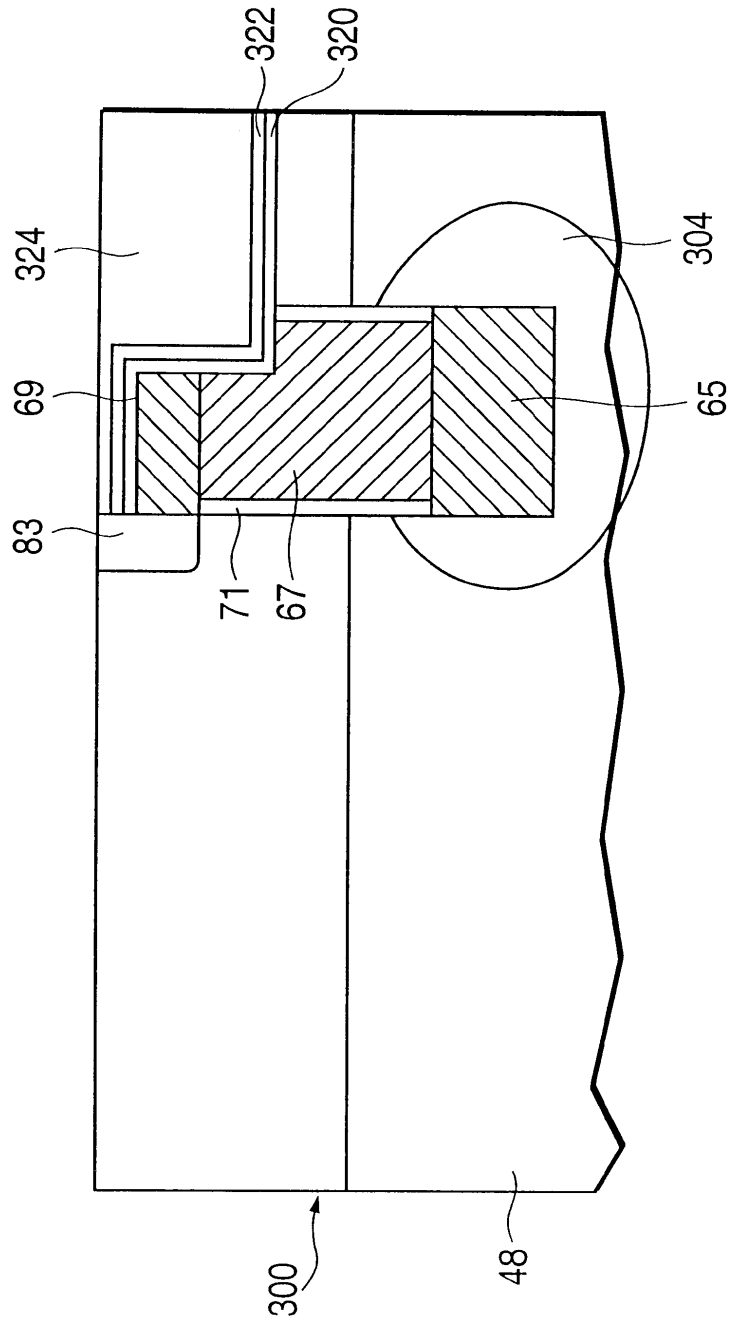


FIG. 9(f)



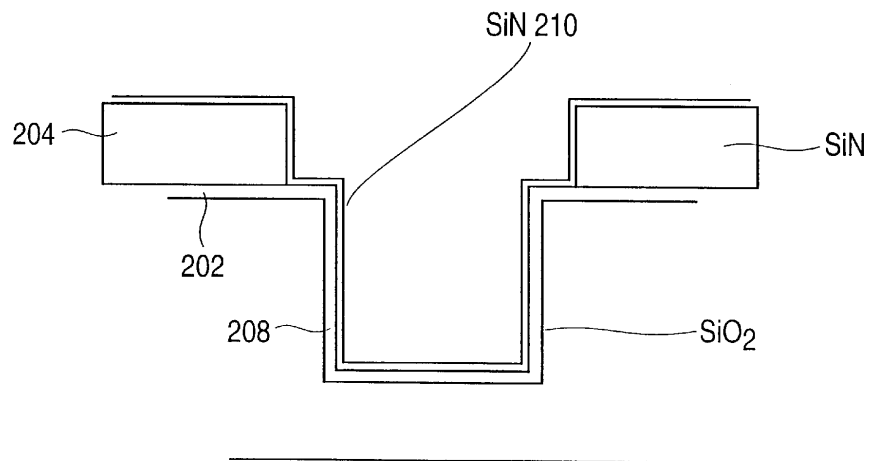
SMIC Ex. 1006
IPR2020-01003
Page 18 of 26

FIG. 9(g)



SMIC Ex. 1006
IPR2020-01003
Page 19 of 26

FIG. 10



SMIC Ex. 1006
IPR2020-01003
Page 20 of 26

SHALLOW TRENCH ISOLATION STRUCTURE AND METHOD OF FORMING THE SAME

BACKGROUND OF THE INVENTION

1. Technical Field

The present invention generally relates to highly integrated semiconductor devices such as semiconductor memory devices and, more particularly, to an isolation structure for such devices and the methods for forming the isolation structure.

2. Description of the Related Art

An integrated circuit may be formed by connecting together various elements such as transistors which are formed on a semiconductor substrate. To ensure proper functioning of the integrated circuit, these elements must be electrically isolated from each other. Such isolation can be achieved using local oxidation of silicon (LOCOS) or shallow trench isolation (STI). Shallow trench isolation is particularly advantageous for circuits having a high integration density since shallow trench isolation can provide for a relatively planar surface on which subsequent insulating and/or conducting layers may be formed.

A conventional process for forming a shallow trench isolation (STI) structure is shown in FIGS. 1(a)–1(f). A silicon dioxide (SiO_2) layer 102 and a silicon nitride (Si_3N_4) layer 104 are successively formed on the surface of a silicon substrate 100 as shown in FIG. 1(a). A patterned resist (not shown) is formed on the upper surface of silicon nitride layer 104 and an etching process such as reactive ion etching (RIE) is used to form trenches 106 in silicon substrate 100 as shown in FIG. 1(b). A thermal oxidation process is then performed to form a thermal silicon dioxide (SiO_2) layer 108 on the exposed surfaces of the silicon substrate 100 as shown in FIG. 1(c). A silicon dioxide (SiO_2) layer 110 is then deposited by the decomposition of TEOS, for example, to fill in trenches 106 as shown in FIG. 1(d). The silicon dioxide layer 110 is then planarized by chemical mechanical polishing (CMP), for example, as shown in FIG. 1(e). Silicon nitride layer 104 serves as a stopper layer for the planarization process. Silicon nitride layer 104 is then removed. Various wet etching processes are used in subsequent manufacturing steps to remove the silicon dioxide layer 102, as well as to remove any sacrificial or dummy silicon dioxide layers which may be formed after removal of the silicon nitride layer. Such sacrificial silicon dioxide layers may be formed to clean the substrate surface prior to growing a gate oxide layer or to repair substrate damage due, for example, to implantation processes (e.g., channel implantation processes for controlling a threshold voltage of a transistor). However, these wet etching processes cause an etching away of the silicon dioxide at the corner 112 of the shallow trench isolation structure as shown in FIG. 1(f). This etching away of the silicon dioxide at the corner of the shallow trench isolation structure is shown in more detail in FIG. 2 and can result in a lowering of the threshold voltage of a transistor formed in the active area defined by the shallow trench isolation structure.

One technique of protecting the corner of a shallow trench isolation structure is described in U.S. Pat. No. 5,521,422 to Mandelman et al. In one embodiment of the Mandelman et al. process shown in FIGS. 3(a)–3(f), a pad oxide 10 and a nitride surface coating 12 are successively formed on the surface of a silicon substrate 5. The nitride surface coating 12 is then etched to form an opening 14 as shown in FIG. 3(a). Next, an insulator 16 such as a CVD oxide is deposited

as shown in FIG. 3(b) and layer 16 and layer 10 are then etched as shown in FIG. 3(c) to leave spacers 16a and 16b on the sidewalls of the nitride surface coating. A trench 18, defined by the spacers 16a and 16b, is then formed in the silicon substrate 5 as shown in FIG. 3(d). An insulator 20 is deposited to fill trench 18 and opening 14. Insulator 20 is then planarized, stopping on nitride surface coating 12. Nitride surface coating 12 is then removed, leaving insulator 20 with spacers 16a and 16b extending above the surface of silicon substrate 5 as shown in FIG. 3(e). Subsequently, pad oxide 10 is etched and a gate dielectric 22 is formed. A gate conductor 24 is then deposited and photolithographically defined as shown in FIG. 3(f).

While the Mandelman et al. process protects the corner of the shallow trench isolation structure from attack during subsequent etching processes, several problems can arise. In particular, the protection of the corner of the shallow trench isolation structure depends on the length “L” shown in FIG. 4. The length “L” refers to the distance that the sidewalls 16a and 16b extend from the corners of the shallow trench isolation structure. Variations in this length “L” can lead to variations in the shape of the shallow trench isolation structures, particularly if the length “L” is varied to be too small such that subsequent etching processes result in the removal of the sidewalls and the attack of the corner of the shallow trench isolation structure. This can result in fluctuations in the device characteristics. Accordingly, the length “L” must be accurately controlled to ensure protection of the corners of the shallow trench isolation structure. In the Mandelman et al. process, the length “L” is determined by the thickness of the insulator 16 deposited during the deposition step shown in FIG. 3(b) and the amount of the insulator 16 which is etched during the reactive ion etching step of FIG. 3(c). Since the length “L” depends on the uniformity of both of these processes and since the uniformity of both of these processes can be affected by, inter alia, wafer position (e.g., center of wafer versus peripheral portion of wafer), the length “L” can be difficult to control in the Mandelman et al. process, leading to possible fluctuations in device characteristics.

In addition, as can be seen in FIG. 3(f), insulator 20 and sidewall spacers 16a and 16b extend above the surface of silicon substrate 5. A step is formed inevitably on the gate electrode 24 since there is a difference in level created between the surface of silicon substrate 5 and the insulator 20. This can lead to difficulties in the patterning of the gate conductor 24, particularly in highly integrated devices such as 64 Mbit and 256 Mbit dynamic random access memories (DRAMs).

Further, the process of Mandelman et al. requires a number of additional steps as compared to the conventional process of FIGS. 1(a)–1(f), e.g., the deposition of insulator 16 and the etching of insulator 16.

Accordingly, it would be desirable to provide a shallow trench isolation structure and methods for forming the shallow trench isolation structure which avoid these and other problems.

SUMMARY OF THE INVENTION

In accordance with one aspect of the present invention, an isolation structure is provided by a method which includes forming a pad oxide layer on a semiconductor substrate and then forming a pad nitride layer on the pad oxide layer. An opening is then formed which extends through the pad nitride layer, the pad oxide layer, and into the semiconductor substrate. The pad nitride layer is then isotropically etched,

thereby pulling-back the pad nitride layer from the portion of the opening extending through the pad oxide layer. An insulating layer is formed to fill in the opening including the portion of the opening formed by the pulling-back of the pad nitride layer. The deposited insulating layer is then planarized using the pulled-back nitride layer as a stopper layer. The pulled-back pad nitride layer and the pad oxide layer are then removed.

In accordance with the above-described method, the insulator at the corner of the shallow trench isolation structure is protected from attack during subsequent etching processes and problems due to changes in the threshold voltages of elements formed in the active area defined by the shallow trench isolation structure can be reduced. In addition, since the pulling-back of the pad nitride is carried out in an isotropic etching step, the method of the present invention provides for enhanced controllability of the shape of the shallow trench isolation structure. Still further, the method of the present invention has a small number of steps and therefore contributes to ease of device manufacture and reduced manufacturing costs.

These and other features and advantages of the present invention will be better understood from a reading of the following detailed description in conjunction with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

FIGS. 1(a)–1(f) are cross-sectional views illustrating a conventional method for forming a shallow trench isolation structure.

FIG. 2 illustrates the etching away of the silicon dioxide at the corner of a shallow trench isolation structure by etching processes after the formation of the shallow trench isolation structure.

FIGS. 3(a)–3(f) illustrate a prior art method which avoids the etching away of silicon dioxide shown in FIG. 2.

FIG. 4 is used in the explanation of a problem which is associated with the method of FIGS. 3(a)–3(f).

FIGS. 5(a)–5(i) are cross-sectional views illustrating a method for forming a shallow trench isolation structure in accordance with a first embodiment of the present invention.

FIGS. 6(a) and 6(b) illustrate shallow trench isolation structures obtained with a silicon nitride pull-back of 100 Å and 300 Å, respectively.

FIGS. 7(a)–7(h) are cross-sectional views illustrating a method for forming a shallow trench isolation structure in accordance with a second embodiment of the present invention.

FIG. 8(a) is a top-down view of a trench DRAM cell with a self-aligned buried strap which is isolated from other cells by a shallow trench isolation structure formed in accordance with the present invention.

FIG. 8(b) is a cross-sectional view taken along line A–A' of FIG. 8(a).

FIGS. 9(a)–9(g) are cross-sectional views illustrating a method for forming a DRAM memory cell which includes the method for forming a shallow trench isolation structure in accordance with the present invention.

FIG. 10 illustrates a modification of the first embodiment of the present invention.

DETAILED DESCRIPTION

FIGS. 5(a)–5(i) are cross-sectional views illustrating a method for forming a shallow trench isolation structure in

accordance with a first embodiment of the present invention. As shown in FIG. 5(a), a pad silicon dioxide (SiO₂) layer 202 and a pad silicon nitride (Si₃N₄) layer 204 are provided on a substrate 200. Silicon dioxide layer 202 has a thickness of about 80 Å–100 Å (e.g., 82 Å) and may be formed by thermal oxidation or by low pressure chemical vapor deposition (LPCVD), for example. Silicon nitride layer 204 has a thickness of about 1000 Å–2000 Å (e.g., 1300 Å) and may be formed, for example, by LPCVD. Substrate 200 may be a silicon wafer or an epitaxial layer formed on a silicon wafer. A patterned photoresist (not shown) is then formed on pad silicon nitride layer 204. The pad silicon nitride layer, the pad silicon dioxide layer, and the substrate are then etched, for example, by reactive ion etching using the patterned photoresist as a mask to form a trench 206 as shown in FIG. 5(b). A thin silicon dioxide (SiO₂) layer 208 having a thickness of about 80 Å–100 Å is formed by a high temperature (for example, 1000° C.) thermal oxidation over the portions of the silicon substrate exposed by the forming of trench 206 as shown in FIG. 5(c). This high temperature oxidation removes substrate damage caused by the etching process for forming trench 206. Pad silicon nitride layer 204 is then isotropically etched by, for example, chemical dry etching. In accordance with the present invention, the amount of silicon nitride which is etched during this isotropic etching step is about 250 Å. Thus, the isotropic etch pulls back pad silicon nitride layer 204 by a distance L=250 Å relative to the sidewall of trench 206 as shown in FIG. 5(d). It will be apparent to one skilled in the art that the amount of silicon nitride to be isotropically etched in this etching step will depend on the overall manufacturing process into which the teachings of this invention are incorporated. In general, the amount of silicon nitride to be etched should be sufficient to result in the protection of the corners of the shallow trench isolation structure from attack. In addition, the isotropic etching of the pad silicon nitride layer should leave silicon nitride having a thickness which is sufficient to function as a stopper layer for the planarization process to be described below with reference to FIG. 5(f).

Optionally, a thin silicon nitride layer 210 having a thickness of about 50 Å may then be deposited by, for example, CVD on pad silicon nitride layer 204 and on silicon dioxide layer 208 as shown in FIG. 10. Silicon nitride layer 210 may be provided, for example, in order to prevent oxidation of underlying layers during subsequent processing steps. In this case, the amount of silicon nitride which is etched during the isotropic etching step is about 300 Å. In this way, the composite silicon nitride layer comprising pad silicon nitride layer 204 and silicon nitride layer 210 is pulled-back by about 250 Å from the sidewall of trench 206.

A silicon dioxide layer 212 is then blanket deposited over the entire surface of the substrate using, for example, a CVD process in which TEOS (Si(OC₂H₅)₄) is decomposed, as shown in FIG. 5(e). Other deposition techniques for depositing the silicon dioxide layer 212, such as a plasma CVD process using O₃ and TEOS, may be utilized. The silicon dioxide layer 212 is then planarized using, for example, RIE, chemical mechanical polishing, or a combination thereof as shown in FIG. 5(f). The pad silicon nitride layer 204 is then removed by, for example, chemical dry etching (CDE), hot phosphoric acid or HF/Glycerol as shown in FIG. 5(g). One or more wet etching processes are then utilized to remove the pad silicon dioxide layer 202, as well as to remove any sacrificial or dummy oxides which may be formed, resulting in the structure shown in FIG. 5(h). Because pad silicon nitride layer 204 was pulled-back by an isotropic etching process, the shallow trench isolation structure of FIG. 5(g)

has a T-shape. In this way, subsequent wet etching processes for removing the pad silicon dioxide layer **202** and any sacrificial or dummy oxide layers attack these extensions of the shallow trench isolation structure and do not result in an etching away of the insulator at the corner of the shallow trench isolation structure as can be seen with reference to FIG. **5(h)**.

Thus, in accordance with the above-described method of the present invention, etching of the insulator at the corner of the shallow trench isolation structure is suppressed and problems due to changes in the threshold voltages of elements formed in the active area defined by the shallow trench isolation structure can be minimized. As discussed with respect to FIG. **4**, the degree to which the corner of the structure is protected is determined by the length "L". In accordance with the present invention, this length "L" is determined by the isotropic etching of the pad silicon nitride layer. Since, in accordance with the present invention, only a single process factor affects the length "L", enhanced controllability of the shape of the shallow trench isolation structure can be achieved and therefore fluctuations in device characteristics can be reduced. In addition, because an upper surface of the shallow trench isolation structure and the surface of the substrate are substantially level, no step is created between the shallow trench isolation structure and a subsequently formed gate conductor **214** as shown in FIG. **5(i)**. Thus, patterning of the gate electrode is simplified. Still further, the method of the present invention has a small number of steps and therefore contributes to ease of device manufacture and reduced manufacturing costs.

FIGS. **6(a)** and **6(b)** illustrate the shapes of shallow trench isolation structures manufactured in accordance with the above-identified method (including the step of forming the silicon nitride layer **210** shown in FIG. **10**) in which the amount of the pad silicon nitride layer which is etched during the isotropic etching step is 100 Å and 300 Å, respectively. As can be seen from these Figures, the etching of the insulator at the corners of the shallow trench isolation structures by wet etching processes after formation of the shallow trench isolation structure is greater in the case of the 100 Å isotropic etch than in the case of the 300 Å isotropic etch. Thus, a pull-back of the pad silicon nitride layer by 300 Å provides greater protection for the corners of the shallow trench isolation than a pull-back of the pad silicon nitride layer by 100 Å. The larger the pulling-back of the pad silicon nitride layer, the longer the horizontal extensions of the "T-shape" of the structure of FIG. **5(g)**, and the greater the protection of the corners of the shallow trench isolation structure. However, since the etching of the pad silicon nitride layer is an isotropic etch, the larger the pulling-back, the thinner the remaining pad silicon nitride layer will be. As noted above, the remaining pad silicon nitride layer should have a thickness sufficient for serving as a stopper layer for the planarization process of FIG. **5(f)**.

FIGS. **7(a)–7(h)** are cross-sectional views illustrating a method for forming a shallow trench isolation structure in accordance with a second embodiment of the present invention. As shown in FIG. **7(a)**, a pad silicon dioxide (SiO_2) layer **202** and a pad silicon nitride (Si_3N_4) layer **204** are provided on a substrate **200**. Silicon dioxide layer **202** has a thickness of about 80 Å–100 Å (e.g., 82 Å) and may be formed by thermal oxidation or by low pressure chemical vapor deposition (LPCVD), for example. Silicon nitride layer **204** has a thickness of about 1000 Å–2000 Å (e.g., 1300 Å) and may be formed, for example, by LPCVD. Substrate **200** may be a silicon wafer or an epitaxial layer formed on a silicon wafer. A patterned photoresist (not

shown) is then formed on pad silicon nitride layer **204**. The pad silicon nitride layer, the pad silicon dioxide layer, and the substrate are then etched by, for example, reactive ion etching using the patterned photoresist as a mask to form a trench **206** as shown in FIG. **7(b)**. Pad silicon nitride layer **204** is then isotropically etched using, for example, HF/Glycerol or hot phosphoric acid. In accordance with the present embodiment, the amount of silicon nitride which is etched during this isotropic etching step is about 250 Å. Thus, the isotropic etch pulls back the pad silicon nitride layer by a distance $L=250$ Å relative to the sidewall of trench **206**, as shown in FIG. **7(c)**. A thin silicon dioxide (SiO_2) layer **208** having a thickness of about 80 Å–100 Å is formed by a high temperature (for example, 1000° C.) thermal oxidation over the portions of the silicon substrate exposed by the forming of trench **206** as shown in FIG. **7(d)**. This high temperature oxidation removes substrate damage caused by the etching process for forming trench **206**. Optionally, a thin silicon nitride layer (not shown) having a thickness of about 50 Å may then be deposited by, for example, CVD on pad silicon nitride layer **204** and on silicon dioxide layer **208**. The silicon nitride layer may be provided, for example, in order to prevent oxidation of underlying layers during subsequent processing steps. As in the first embodiment, if the 50 Å silicon nitride layer is formed, the amount of silicon nitride which is etched during the isotropic etching step is about 300 Å. In this way, a composite silicon nitride layer is formed which is pulled back by about 250 Å from the sidewall of trench **206**. Next, a silicon dioxide layer **212** is blanket deposited over the entire surface of the substrate using, for example, a CVD process in which TEOS ($\text{Si}(\text{OC}_2\text{H}_5)_4$) is decomposed, as shown in FIG. **7(e)**. The silicon dioxide layer **212** is then planarized using, for example, RIE, chemical mechanical polishing, or a combination thereof as shown in FIG. **7(f)**. The pad silicon nitride layer **204** is then removed by, for example, chemical dry etching (CDE) or etching using hot phosphoric acid or HF/glycerol as shown in FIG. **7(g)**. One or more wet etching processes are then utilized to remove the pad silicon dioxide layer **202**, as well as any sacrificial or dummy oxide layers which may be formed, resulting in the structure shown in FIG. **7(h)**. Because the pad silicon nitride layer was pulled-back by an isotropic etching process, the shallow trench isolation structure of FIG. **7(g)** has a T-shape. In this way, subsequent wet etching processes for removing the pad silicon dioxide layer **202** and any sacrificial or dummy oxide layers attack these extensions of the shallow trench isolation structure and do not result in an etching away of the insulator at the corner of the shallow trench isolation structure as can be seen with reference to FIG. **7(h)**.

The same advantages which are obtained in the first embodiment are also obtained in the second embodiment.

FIGS. **8(a)** and **8(b)** illustrate a trench DRAM cell with a self-aligned buried strap which is isolated from other cells by a shallow trench isolation structure in accordance with the present invention. Specifically, FIG. **8(a)** is a top-down view of the trench DRAM cell and FIG. **8(b)** is a cross-sectional view taken along line A–A' of FIG. **8(a)**. DRAM cell **50** includes a trench capacitor **55** and a transfer gate **60**. Trench capacitor **55** includes a first N^+ -type polycrystalline silicon fill **65**, a second polycrystalline silicon fill **67**, and a collar oxide **71**. Transfer gate **60** includes N-type source/drain and drain/source regions **73** and **74** formed in P-type well **75** and a $\text{WSi}_3/\text{polycrystalline silicon}$ gate **77** insulatively spaced from the channel region between source/drain region **73** and drain/source region **74**. A bit line contact **79**

formed in an opening in an insulating layer **80** (of BPSG, for example) electrically connects source/drain region **73** to bit line **81**. A shallow trench isolation structure formed in accordance with the present invention electrically isolates DRAM cell **50** from an adjacent DRAM cell and passing word line **92**. Passing word line **92** has a $\text{WSi}_x/\text{polycrystalline silicon}$ structure. A dielectric layer **87** is formed on bit line **81** and aluminum wirings **89** are formed on dielectric layer **87**. One of the aluminum wirings **89** is connected to bit line **81** by a contact stud **91** of tungsten, for example. A diffusion region **83** electrically connects third polycrystalline silicon fill **69** and drain/source region **74** of MOS transfer gate **60**. This diffusion region is formed by outdiffusing dopants from the highly doped polycrystalline silicon fill in the storage trench into P-well **75**. Diffusion region **83** and third polycrystalline silicon fill **69** constitute a buried strap for connecting trench capacitor **55** to transfer gate **60**.

A method of manufacturing the DRAM cell **50** using the shallow isolation structure and method of the present invention will be described below with reference to FIGS. **9(a)**–**9(g)**. As shown in FIG. **9(a)**, a buried N-type well **48** is formed in a P-type semiconductor substrate **300** by implanting phosphorous below the intended P-well for a memory cell array. A buried N-type well may also be formed by other methods, e.g., P-well implantation into an N-type semiconductor substrate or by epitaxy, and the invention is not limited in this respect. A silicon nitride layer **302** having a thickness of about 0.2 micrometers is formed by chemical vapor deposition, for example, on the surface of a thin oxide layer **301** having a thickness of about 10 nanometers which is thermally grown on semiconductor substrate **300**. Oxide layer **301** and silicon nitride layer **302** are patterned and etched to provide a mask for etching a trench **303**. Trench **303** is etched using an anisotropic etching process to a depth of about 8 micrometers as shown in FIG. **9(b)**. After storage node trench **303** is etched, an N-type capacitor plate **304** is formed by outdiffusing arsenic from the lower portion of trench **303**. This may be accomplished, for example, by depositing an arsenic doped glass layer, etching the arsenic doped glass layer to remain only at the lower portion of trench **303**, and performing an annealing process to outdiffuse the arsenic. A storage node dielectric layer (not shown) such as an oxide-nitride (ON) layer or a nitride-oxide (NO) layer is then formed in trench **303**. After the dielectric layer is formed, a first conductive region is formed by filling trench **303** with an impurity-doped first conductive material such as N⁺-type polycrystalline silicon. The filling step may be carried out using chemical vapor deposition of silane or disilane, for example. The N⁺-type polycrystalline silicon is then etched back to a first level within trench **303** using an isotropic etch process to form first trench fill **65**. The level of first trench fill **65** is, for example, about 1.0 micrometer below the surface of semiconductor substrate **300**. Collar oxide **71** is then formed on the sidewall of the portion of trench **303** opened by the etching back of the N⁺-type polycrystalline silicon using low pressure chemical vapor deposition (LPCVD) or plasma-enhanced chemical vapor deposition (PECVD) TEOS as shown in FIG. **9(c)**.

A second conductive region is formed by filling in the remainder of trench **303** with a second conductive material. The second conductive material may be, for example, N⁺-type polycrystalline silicon or undoped polycrystalline silicon and may be formed by chemical vapor deposition (CVD). The second conductive material and the oxide collar **71** are then etched back to a second level within trench **303** to form second trench fill **67** which is insulated from the

semiconductor substrate by collar oxide **71** as shown in FIG. **9(d)**. The depth of the buried strap to be formed in a subsequent process step is defined by this controlled etch-back of the second conductive material and collar oxide **71**. Second trench fill **67** is etched back to about 0.1 micrometer below the surface of semiconductor substrate **300**. An in-situ removal of a native oxide in trench **303** is then performed. In particular, the native oxide on the upper surface of second trench fill **67** and on the sidewall of trench **303** through which impurities for the buried strap will subsequently be outdiffused are removed. This removal of native oxide may be carried out by an in-situ prebake in a hydrogen ambient at a temperature greater than 850° C., for example.

The portion of trench **303** opened by the etching back of collar oxide **71** and the second conductive material is then filled by a third conductive material. The third conductive material may be, for example, undoped polycrystalline silicon deposited by chemical vapor deposition (CVD). The polycrystalline silicon is then etched back using reactive ion etching, for example, to form a third trench fill **69** as shown in FIG. **9(e)**. The polycrystalline silicon is preferably etched back to about 0.05 micrometer below the surface of semiconductor substrate **300** as determined by the tolerable resistance of the buried strap, and by the recess etch controllability.

With reference to FIG. **9(f)**, a shallow trench **310** is formed to provide for shallow trench isolation. As described above, shallow trench isolation is used to isolate discrete memory cell devices to prevent interference therebetween. In particular, a shallow trench is formed as described above with respect to FIGS. **5(a)–5(i)** or FIGS. **7(a)–7(h)**. Thus, for example, the trench **310** may be etched using a patterned photoresist formed on the pad silicon nitride layer **302** as a mask. The pad silicon nitride layer **302** is then isotropically etched to remove about 300 Å. The trench sidewall is then oxidized to form an oxide layer **320** having a thickness of about 100 Å and a silicon nitride layer **322** having a thickness of about 50 Å is then deposited. The oxide and nitride linings serve to isolate collar oxide **71** from oxidant, and thereby suppress dislocation and stress. The trench is then filled with an insulator **324** such as silicon dioxide and the trench fill is then planarized using chemical mechanical polishing (CMP) and/or reactive ion etching (RIE). The pad silicon nitride layer is then stripped by chemical dry etching (CDE) or hot phosphoric acid and the pad oxide is then removed using a wet etch for removing, for example, 200 Å of silicon dioxide. At this time, the silicon dioxide in the trench is also etched. A sacrificial silicon dioxide layer having a thickness of about 100 Å is then formed on the surface of the substrate **300** and impurities may be implanted in what will become the channel regions of the transfer gates in order to control the threshold voltages thereof. The sacrificial oxide is then removed by etching away 120 Å of silicon dioxide.

A gate insulator may then be formed on the planar surface, and gate material may be deposited and patterned to form gate electrodes. Using the gate electrodes as masks, source/drain regions may be formed by ion implantation. Accordingly, transfer gates coupled to trench capacitors are realized. Interconnection between devices and metallization to the output terminals are conducted using techniques known in the art. During the complete DRAM fabrication process, impurities from the conductive regions within the trench are outdiffused to form strap portion **83**.

In accordance with the above process, the corner portions of the shallow trench isolation structure are protected from etching during the memory cell fabrication process such that

these corner portions are substantially level with the surface portion of said semiconductor substrate and the upper surface portion of the insulator 324 filling the shallow trench as shown in FIG. 9(g).

While a particular example has been described in which the shallow trench isolation structure and method of the present invention are incorporated into a memory device including a trench capacitor, the invention is not limited in this respect and may be applied to isolating elements of any semiconductor device formed on a substrate.

While the invention has been described in detail with reference to the appended drawings, the invention is limited in scope only by the claims. Moreover, any patent or publication cited herein should be construed to be incorporated by reference as to any subject matter deemed essential to the present disclosure.

I claim:

1. A method of forming a shallow trench isolation structure, comprising the steps of:

forming a pad oxide layer on a semiconductor substrate;

forming a pad nitride layer on said pad oxide layer;

forming an opening which extends through said pad nitride layer, said pad oxide layer, and into said semiconductor substrate;

isotropically etching said pad nitride layer, thereby pulling back said pad nitride layer from the portion of said opening extending through said pad oxide layer;

oxidizing portions of said semiconductor substrate exposed by said opening;

depositing an insulating layer to fill in said opening including the portion of said opening formed by the pulling back of said pad nitride layer;

planarizing the deposited insulating layer using said pulled-back pad nitride layer as a stopper layer; and removing said pulled-back pad nitride layer and said pad oxide layer.

2. The method according to claim 1, wherein said pad nitride layer is isotropically etched using one of the group consisting of HF/glycerol and hot phosphoric acid.

3. The method according to claim 1, wherein said insulating layer is planarized using at least one of the group consisting of chemical mechanical polishing and reactive ion etching.

4. The method according to claim 1, wherein the insulating layer comprises silicon dioxide.

5. The method according to claim 1, comprising the further step of:

forming a nitride layer on the oxidized portions of said semiconductor substrate prior to depositing said insulating layer.

6. The method according to claim 1, wherein said nitride layer comprises a silicon nitride layer.

7. A method of forming a shallow trench isolation structure, comprising the steps of:

forming a pad oxide layer on a semiconductor substrate;

forming a pad nitride layer on said pad oxide layer;

forming an opening which extends through said pad nitride layer, said pad oxide layer, and into said semiconductor substrate;

oxidizing portions of said semiconductor substrate exposed by said opening;

isotropically etching said pad nitride layer, thereby pulling back said pad nitride layer from the portion of said opening extending through said pad oxide layer;

depositing an insulating layer to fill in said opening including the portion of said opening formed by the pulling back of said pad nitride layer; and

planarizing the deposited insulating layer using said pulled-back pad nitride layer as a stopper layer; and removing said pulled-back pad nitride layer and said pad oxide layer.

8. The method according to claim 7, wherein said pad nitride layer is isotropically etched using chemical dry etching.

9. The method according to claim 7, wherein said insulating layer is planarized using at least one of the group consisting of chemical mechanical polishing and reactive ion etching.

10. The method according to claim 7, wherein said insulating layer comprises silicon dioxide.

11. The method according to claim 7, comprising the further step of:

forming a nitride layer on the oxidized portions of said semiconductor substrate prior to depositing said insulating layer.

12. The method according to claim 7, wherein said nitride layer comprises a silicon nitride layer.

* * * * *

UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

PATENT NO.: 5,960,297
DATED: September 28, 1999
INVENTORS: Kazuo SAKI

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

On the cover page, in the [54] Title, before "SHALLOW", insert --METHOD OF FORMING--; and

replace "AND METHOD OF FORMING THE SAME" with
--BY ISOTROPICALLY ETCHING A PAD NITRIDE LAYER
WITH EXPOSED TOP STRUCTURE--.

In Claim 1, Column 9, Line 25, after "layer", insert --with a top surface of said pad nitride layer exposed--.

Line 29, after "opening", insert --after said step of isotropically etching--.

In Claim 7, Column 10, Line 17, after "layer", insert --with a top surface of said pad nitride layer exposed after said step of oxidizing--.

Signed and Sealed this
Twenty-second Day of August, 2000

Attest:



Q. TODD DICKINSON

Attesting Officer

Director of Patents and Trademarks

SMIC Ex. 1006
IPR2020-01003
Page 26 of 26



US005859466A

United States Patent [19]
Wada

[11] **Patent Number:** **5,859,466**
[45] **Date of Patent:** **Jan. 12, 1999**

[54] **SEMICONDUCTOR DEVICE HAVING A
FIELD-SHIELD DEVICE ISOLATION
STRUCTURE AND METHOD FOR MAKING
THEREOF**

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[73] Assignee: **Nippon Steel Semiconductor
Corporation**, Tateyama, Japan

[21] Appl. No.: **659,653**

[22] Filed: **Jun. 6, 1996**

[30] **Foreign Application Priority Data**

Jun. 7, 1995 [JP] Japan 7-140881
Aug. 24, 1995 [JP] Japan 7-216378

[51] **Int. Cl.⁶** **H01L 79/40**

[52] **U.S. Cl.** **257/508; 257/520; 257/640**

[58] **Field of Search** **257/508, 513,
257/520**

[56] **References Cited**

U.S. PATENT DOCUMENTS

4,493,740 1/1985 Komeda 437/63
4,688,069 8/1987 Joy et al. 257/508
4,819,052 4/1989 Hutter 257/520
4,825,278 4/1989 Hillenius et al. 257/630
4,924,284 5/1990 Beyer et al. 257/508
4,925,805 5/1990 Van Ommen et al. 437/21
4,939,567 7/1990 Kenney 257/508
4,983,226 1/1991 Hunter et al. 257/513
5,097,310 3/1992 Eimori et al. 257/371
5,457,339 10/1995 Komori et al. 257/513

FOREIGN PATENT DOCUMENTS

61-290753 12/1986 Japan .

62-58658 3/1987 Japan 257/508
2-98959 4/1990 Japan .
2-172253 7/1990 Japan .
2-211651 8/1990 Japan .
3-21039 1/1991 Japan 257/513
5-109886 4/1993 Japan .

OTHER PUBLICATIONS

Onai et al., "SEPIA: A New Isolation Structure for Soft-Error-Immune LSI's", IEEE Transactions on Electron Devices, vol. 40, No. 2, pp. 402-406, Feb. 1993.

Primary Examiner—Valencia Martin-Wallace

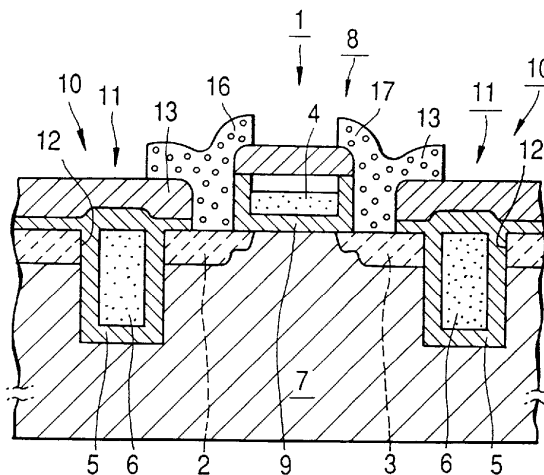
Assistant Examiner—David B. Hardy

Attorney, Agent, or Firm—Oblon, Spivak, McClelland, Maier & Neustadt, P.C.

[57] **ABSTRACT**

An LSI semiconductor device having a device isolation structure and a method of fabricating the isolation structure are presented. The device is a buried-type field-shielding device which is fabricated in non-active regions of the LSI circuit, and includes field-shield insulator film formed on the interior walls of trench cavities formed on the substrate and the field-shield electrodes buried within the trench cavity. Unlike the conventional buried-type isolation devices, the top surface of present isolation structure is level with the upper surface of the substrate. Therefore, this device structure utilizes the interior space of the substrate rather than the surface area of the substrate as in the conventional field-shield isolation structure. The isolation structure not only achieves a higher density of integration of active devices in a given space of the substrate but also simplifies the design of interconnection lines, thereby suggesting a path to production of very large integrated circuits economically in the future.

4 Claims, 11 Drawing Sheets



SAYFE KIAEI, PH.D.

EXHIBIT 3

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SMIC Ex. 1004

IPR2020-01003

Page 1 of 21

FIG.1A

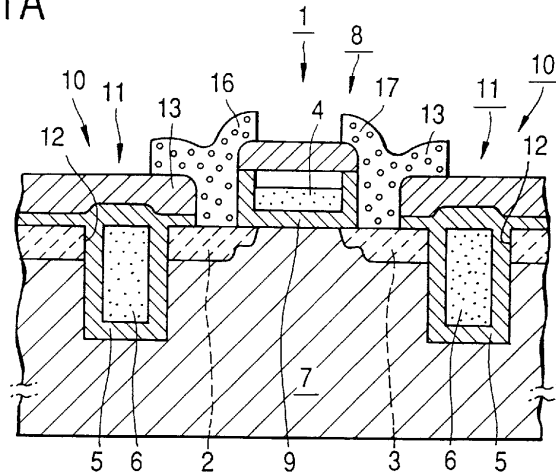


FIG1B

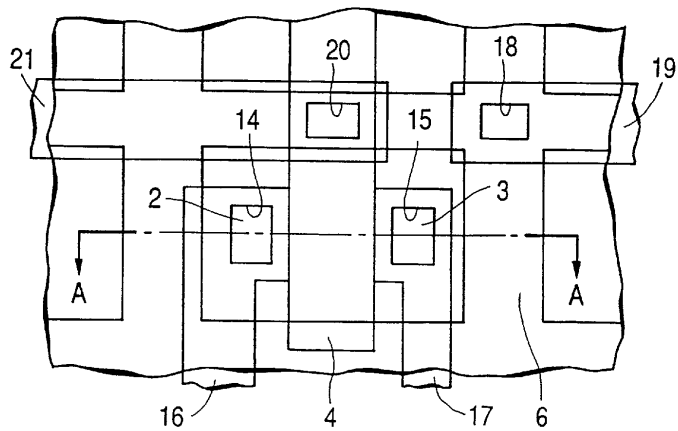


FIG.2A

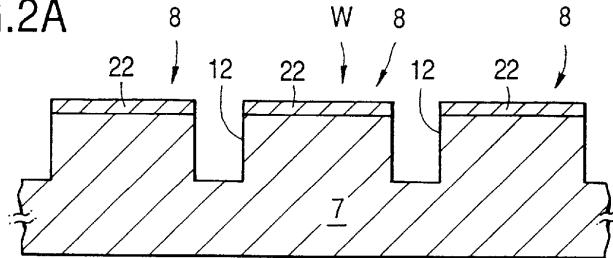


FIG.2B

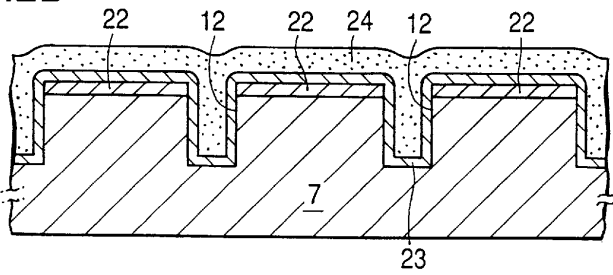


FIG.2C

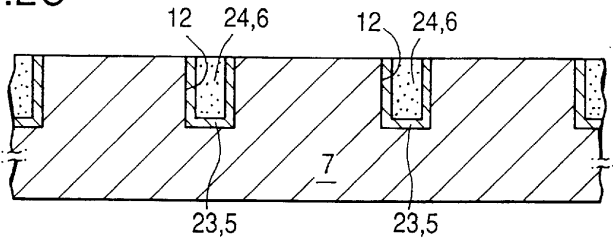
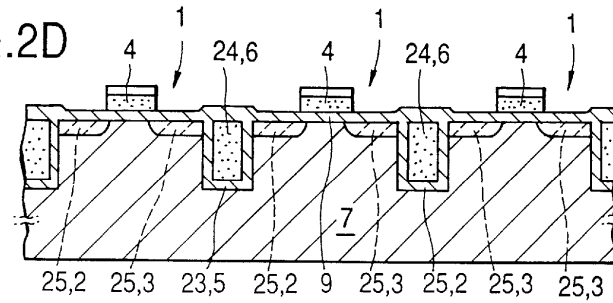


FIG.2D



SMIC Ex. 1004
IPR2020-01003
Page 3 of 21

FIG.2E

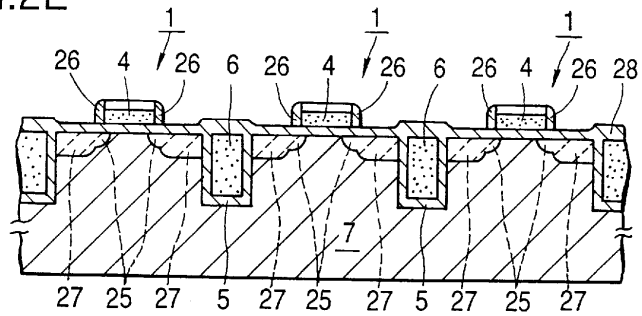


FIG.2F

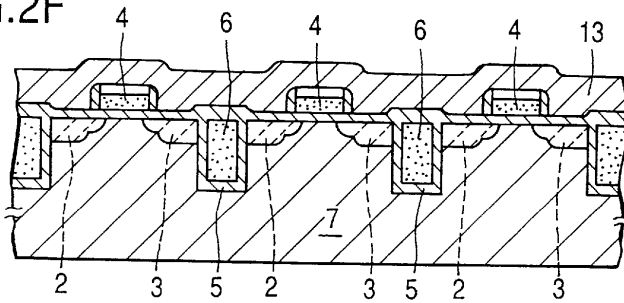


FIG.2G

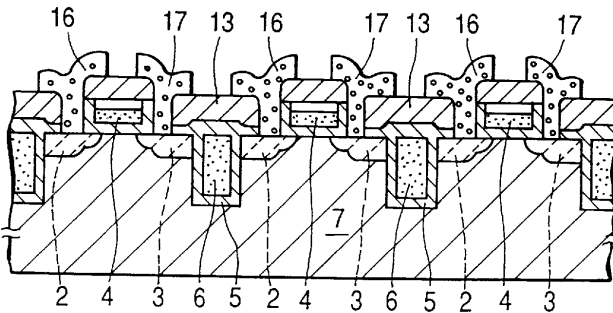
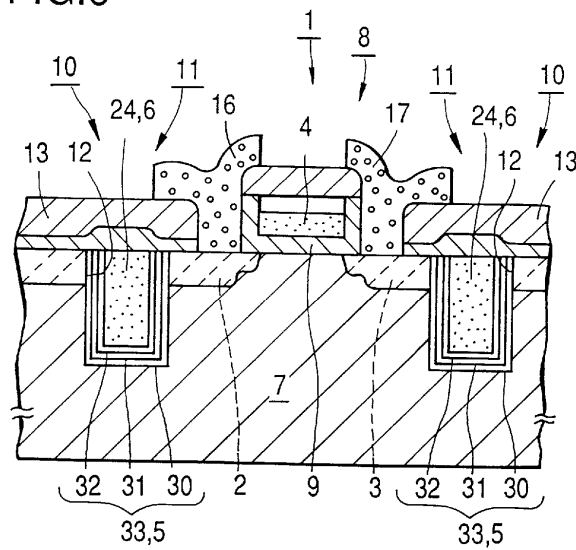
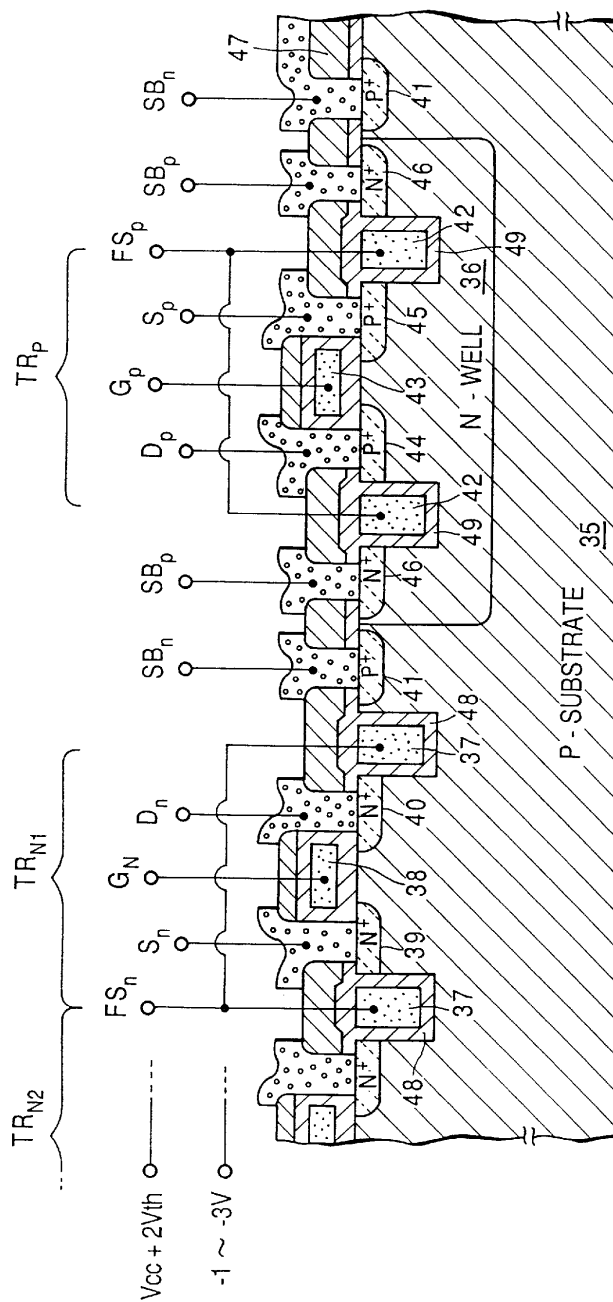


FIG.3



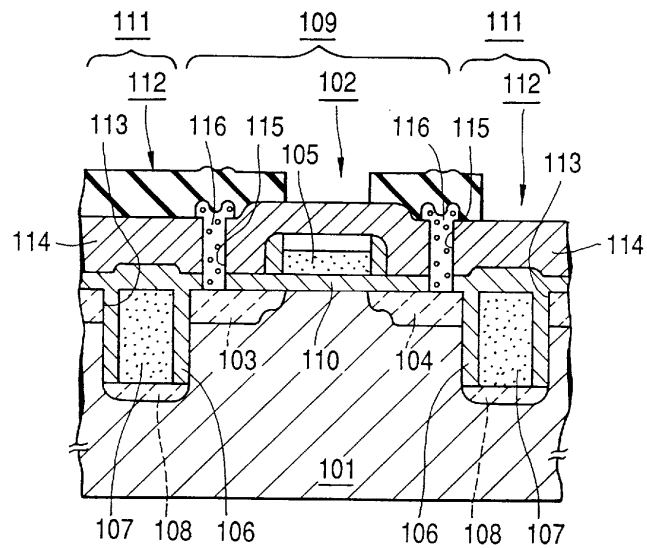
SMIC Ex. 1004
IPR2020-01003
Page 5 of 21

FIG4

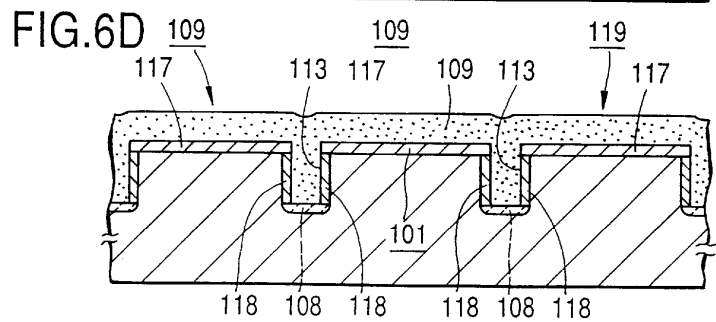
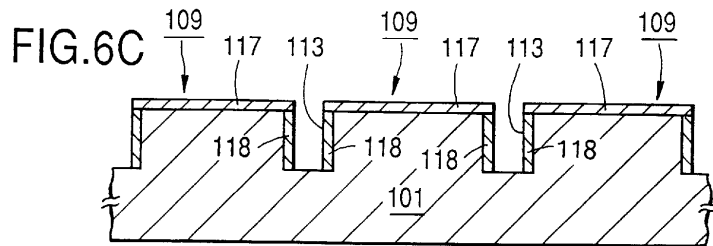
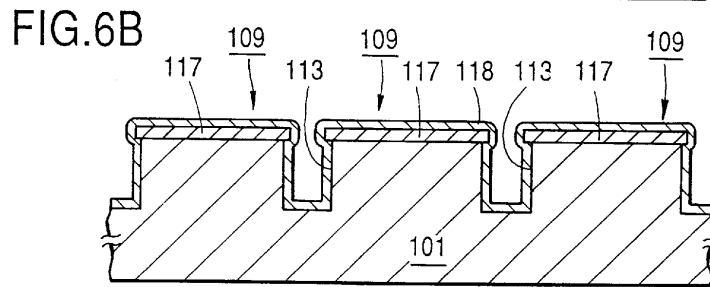
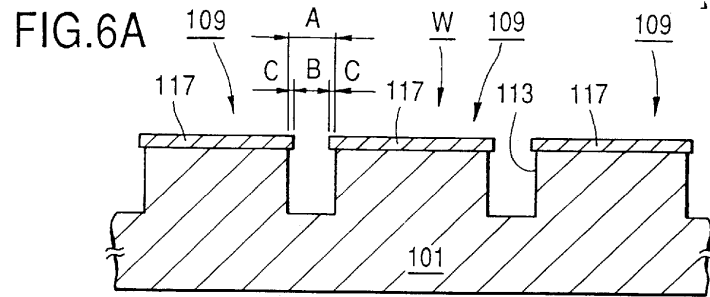


SMIC Ex. 1004
IPR2020-01003
Page 6 of 21

FIG.5



SMIC Ex. 1004
IPR2020-01003
Page 7 of 21



SMIC Ex. 1004
IPR2020-01003
Page 8 of 21

FIG. 6H

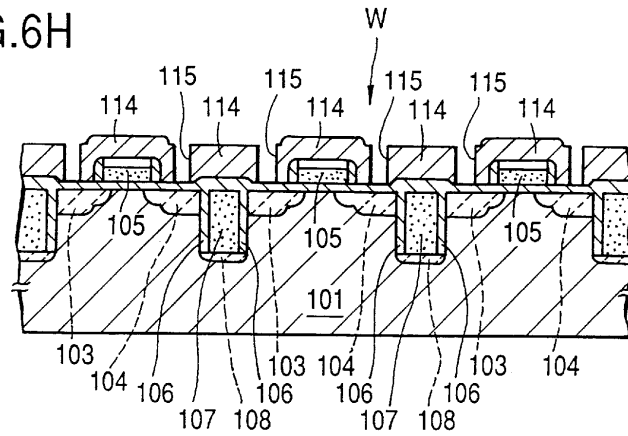
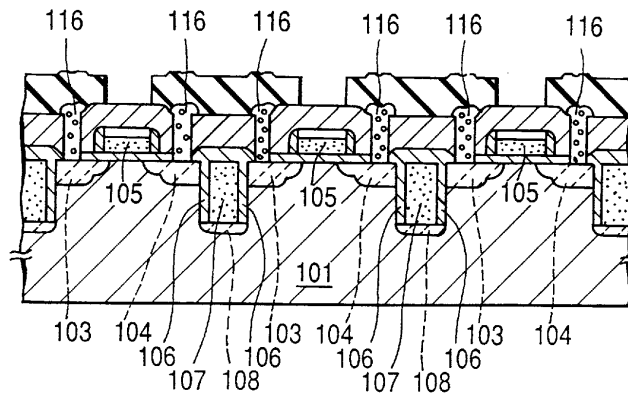
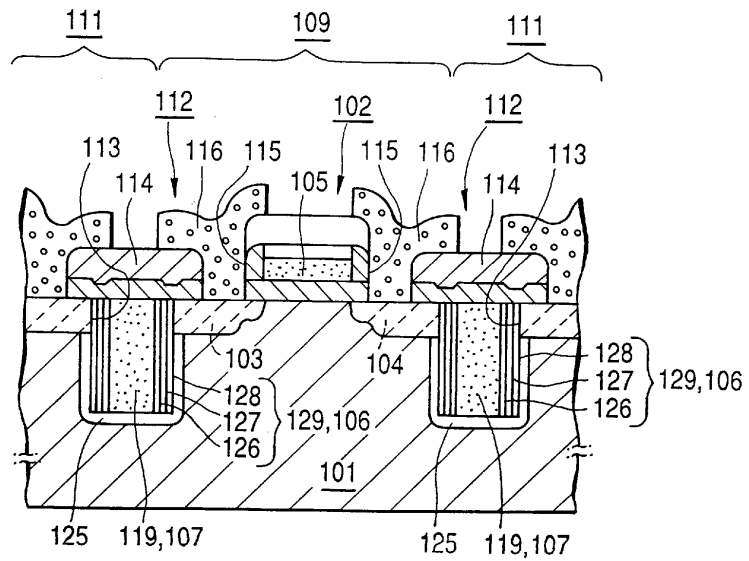


FIG. 6I



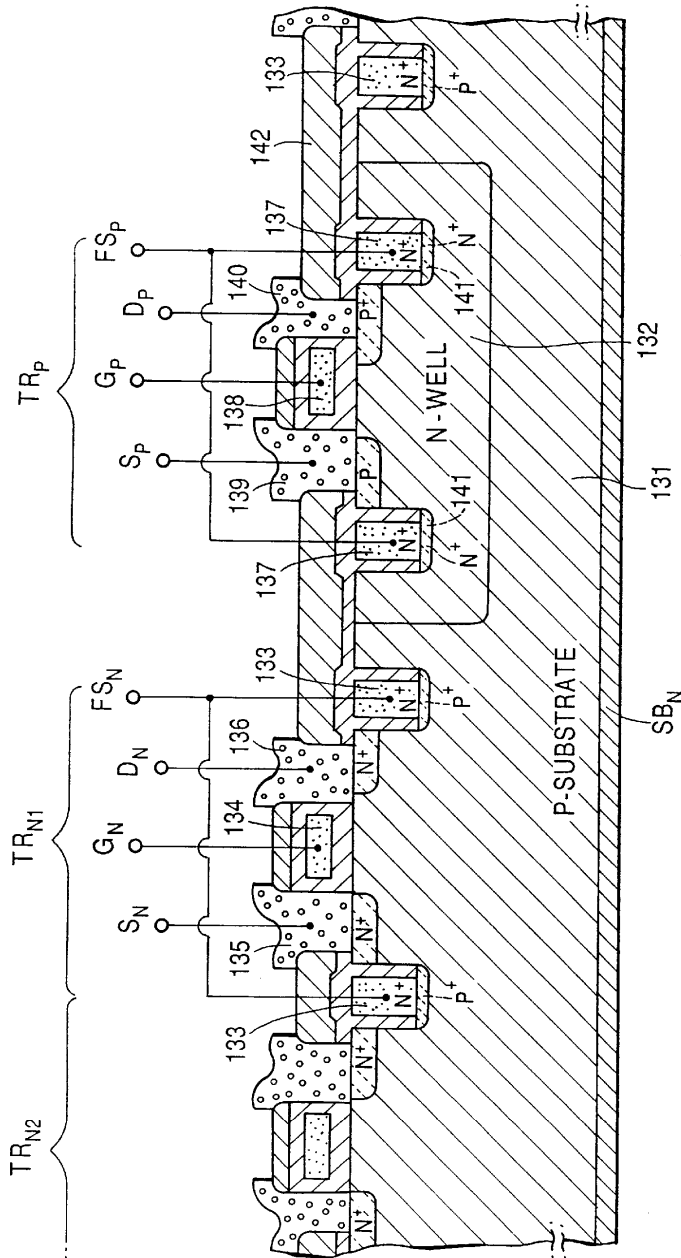
SMIC Ex. 1004
IPR2020-01003
Page 10 of 21

FIG. 7



SMIC Ex. 1004
IPR2020-01003
Page 11 of 21

FIG. 8



SMIC Ex. 1004
IPR2020-01003
Page 12 of 21

SEMICONDUCTOR DEVICE HAVING A FIELD-SHIELD DEVICE ISOLATION STRUCTURE AND METHOD FOR MAKING THEREOF

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates in general to semiconductor devices, and relates in particular to a semiconductor device having a field-shield device isolation structure for isolation of devices in a high density MOSLSI circuit and a method of fabrication thereof.

2. Description of the Related Art

Isolation of device elements fabricated on silicon substrate has often been carried out by forming thick oxide films on selected local areas by the so-called Local Oxidation of Silicon method (shortened to LOCOS method hereinbelow). However, one of the serious barriers to achieving a higher density of integration by the LOCOS method has been a lateral growth of oxide film from the peripheries of the oxide film towards active device regions, the so-called bird's beak growth phenomenon which occurs during the thermal oxidation process. For this reason, there have been interests in other methods of isolation of active devices in large scale integration circuits, and particular interests have been focused on an isolation approach called field-shield device isolation method.

Field-shield device isolation method relates to a MOS (metal oxide semiconductor) structure for separating devices by forming a field-shield insulator film and a field-shield electrode between two active regions of a device. By fixing the field-shield electrode potential at a reference potential (e.g., GND or 0V), the formation of parasitic channels on the device surface is prevented, thereby providing insulative isolation of the active regions of the devices. In the presentation below, the field-shield device isolation is referred to as FSDI.

An improved version of the FSDI structure is known in which the field-shield insulator film and the field-shield electrode are buried in a trench. By utilizing such a buried-structure configuration, it is expected that higher integration of circuits may be realized.

However, the conventional FSDI structure is still inadequate for the purposes of attaining the degree of integration densities required in modern semiconductor devices. For example, even in those devices having the buried FSDI structure intending to increase the integration density, the top portion of T-shaped cross-section field-shield electrode is exposed on the surface of the substrate such that the width of the top end of the field-shield electrode is wider than the width of the trench width. In other words, much of the valuable surface space is occupied by the non-active regions serving the purpose of device isolation. This is obviously an undesirable aspect of the conventional FSDI structure, and there has been a need to improve the structural configuration of the existing FSDI structure to meet the increasing demand for higher integration density in modern semiconductor devices.

SUMMARY OF THE INVENTION

It is an object of the present invention to provide a semiconductor device having a field-shield structure which would enable to attain a higher degree of integration of circuits in the semiconductor device, and a method of making such a field-shield structure.

The object has been achieved in a semiconductor device means having a field-shield device isolation structure fabricated in non-active regions of the semiconductor device arranged on a semiconductor substrate, the field-shield device isolation structure comprising: a field-shield insulator film for providing inter-device electrical isolation among a plurality of devices fabricated on the semiconductor substrate; a field-shield electrode for being provided with a reference potential; wherein the field-shield insulator film is formed on interior surfaces of a trench cavity whose cavity opening faces an upper surface of the semiconductor substrate and whose depth dimension is deeper than a diffusion distance of a dopant species associated with a device of the plurality of devices, and the field-shield electrode is buried in an interior space of the trench cavity lined with the field-shield insulator film so that a top surface of the field-shield electrode is level with the upper surface of the semiconductor substrate.

According to the semiconductor device presented above, because both the field-shield insulator film and the field-shield electrode are buried within their own trenches having a depth dimension larger than those for the source and drain diffusion layers, the effective isolation distance between the diffusion layers is equal to the distance of the width and twice the depth dimensions of a trench. Therefore, compared with a conventional non-buried type device, the effective isolation dimension is increased substantially. Additionally, in the case of the present device, because the top surface of the field-shield electrode is coplanar or level with the upper surface of the substrate, the area required for the device isolation structure is only that area required for the width of the trench cavity. Therefore, compared with the conventional buried-type field-shield device isolation structures, a higher degree of integration density can be achieved in a given area of a substrate.

An aspect of the semiconductor device is that the field-shield device isolation structure comprises: a field-shield insulator film for providing inter-device electrical isolation for a plurality of devices fabricated on the semiconductor substrate; a field-shield electrode for being provided with a reference potential; wherein the field-shield insulator film is formed on interior surfaces of a trench cavity whose cavity opening faces an upper surface of the semiconductor substrate, and whose depth dimension is deeper than a diffusion distance of a dopant species associated with a device of the plurality of devices, and the field-shield electrode is buried in an interior space of the trench cavity lined with the field-shield insulator film so that a top surface of the field-shield electrode is level with the upper surface of the semiconductor substrate and that a bottom surface of the field-shield electrode is in electrical contact with the semiconductor substrate.

According to the aspect of the device presented above, because the bottom surface of the field-shield electrode is in electrical contact with the substrate, the overall interconnection design, including the electrode lines for applying voltages to the field-shield electrode and the substrate, can be greatly simplified. The advantage of this design approach is that, compared with the conventional buried-type isolation devices, a higher degree of integration can be achieved within a given area of a substrate.

Another aspect of the present invention relates to a method for making a semiconductor device presented above, and comprises the steps of: forming a trench cavity, which opens to an upper surface of the semiconductor substrate and has a depth dimension deeper than a diffusion distance of a dopant species associated with a device, on an upper surface

3

of the semiconductor substrate; forming a field-shield insulator film on interior surfaces of the trench cavity; and forming a field-shield electrode by filling an interior space of the trench cavity and terminating a top surface of the field-shield electrode so as to be level with the upper surface of the semiconductor substrate.

Another approach to the method for making a semiconductor device means comprises the steps of: forming a trench cavity, which opens to an upper surface of the semiconductor substrate and has a depth dimension deeper than a diffusion distance of a dopant species associated with a device, on an upper surface of the semiconductor substrate; forming a field-shield insulator film on interior surfaces of the trench cavity; removing the field-shield insulator film only from a bottom surface of the trench cavity so as to expose an internal surface of the semiconductor substrate; fabricating a doped region, of an identical conductivity type to the given conductivity type, on the internal surface and forming a field-shield electrode by filling an interior space of the trench cavity and terminating a top surface of the field-shield electrode so as to be level with the upper surface of the semiconductor substrate.

The above methods of production of the device enables to achieve the high degree of integration density required for modern semiconductor devices. As an example, the methods involve the steps of making the field-shield electrode material to a height higher than the level of opening of the trench cavity, and later planarizing the deposit to be level with the substrate surface by such methods as chemical mechanical polishing, etch back and wet etching. The method leads to a much simpler and economical production approach to making the buried-type isolation device without the use of photolithography.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. 1A is a vertical cross sectional view of a first embodiment of the semiconductor device of the present invention seen through a section A—A indicated in FIG. 1B.

FIG. 1B is a plan view of the first embodiment of the semiconductor device of the present invention.

FIGS. 2A~2G are schematic illustrations to show the successive steps for making the semiconductor device of the first embodiment.

FIG. 3 is a vertical cross sectional view of a second embodiment of the semiconductor device of the present invention.

FIG. 4 is a vertical cross sectional view of a third embodiment of the semiconductor device of the present invention to particularly show the arrangement of applying voltages.

FIG. 5 is a vertical cross sectional view of a fourth embodiment of the semiconductor device of the present invention.

FIGS. 6A~6I are schematic illustrations to show the successive steps for making the semiconductor device of the fourth embodiment.

FIG. 7 is a vertical cross sectional view of a fifth embodiment of the semiconductor device of the present invention.

FIG. 8 is a vertical cross sectional view of a sixth embodiment of the semiconductor device of the present invention to particularly show the arrangement of applying voltages.

DESCRIPTION OF THE PREFERRED EMBODIMENTS

A first embodiment of the semiconductor device of the present invention will be explained with reference to drawings.

4

FIGS. 1A and 1B show a FSDI structure in a MOSLSI device comprising: an N-channel MOS transistor 1; a source diffusion layer 2; a drain diffusion layer 3; a gate-electrode 4; a field-shield insulator film 5; and a field-shield electrode 6.

As shown in FIG. 1A, the N-channel MOS transistor 1 is fabricated on an active region 8 on an upper surface of a semiconductor substrate 7. The N-channel MOS transistor 1 comprises: a gate electrode 4 formed of a polycrystalline silicon film; a gate insulator film 9 formed of a silicon dioxide (SiO₂) film of 10~14 nm thickness; an N-type source diffusion layer 2; and an N-type drain diffusion layer 3 of a lightly doped drain (LDD) structure. The regions between the active regions 8 are non-active regions 10 which are utilized for fabrication of the FSDI structure 11 for isolating the neighboring MOS transistors 1.

The FSDI structure 11 consists of a field-shield insulator film 5 and a field-shield electrode 6. Within the non-active region 10, there is a trench cavity (shortened to trench hereinbelow) 12 with its opening terminating at the surface of the substrate 7, and having a cavity depth dimension larger than the depth dimensions of the source and drain diffusion layer 2 and 3. The interior surfaces of the trench 12 are provided with the field-shield insulator film 5 fabricated along its entire interior surfaces thereby burying the field-shield electrode 6 in its interior space surrounded by the field-shield insulator film 5. The top surface of the field-shield electrode is coplanar (i.e. level) with the upper surface of the substrate 7. An interlayer insulator film 13 is provided over the field-shield electrode 6.

As shown in FIGS. 1A and 1B, electrode lines 16 and 17 are provided, respectively, for the source and drain diffusion layers 2 and 3 through corresponding contact holes 14 and 15. An electrode line 19 is provided for the field-shield electrode 6 through a contact hole 18, and a gate line 21 for the gate electrode 4 through a contact hole 20.

In the following, a method of fabricating the MOSLSI device of the configuration described above will be explained with reference to the steps illustrated in FIGS. 2A~2G.

First, as shown in FIG. 2A, the cavities for the trenches 12 are fabricated on the upper surface of a wafer W (includes a substrate 7 of a P-type monocrystalline silicon having a specific resistance 3~4 ohm-cm) by process of etching through an etching mask of a SiO₂ film 22, for protecting those active regions 8 for fabricating the N-channel MOS transistor but exposing those regions for forming the trenches 12. The process of forming the trenches 12 used in this embodiment is a dry etching process using gaseous chlorine to make a cavity measuring 0.5~1.5 μ m in depth and 0.2~0.5 μ m in width.

Next, as shown in FIG. 2B, a SiO₂ insulator film 23 having a 10~80 nm thickness is fabricated on the surface of the wafer W by means of a thermal oxidation process or a vapor deposition process. This step is followed by another vapor deposition process to form a polycrystalline silicon deposit 24 of 100~500 nm thickness on the entire surface of the wafer W. The polycrystalline silicon deposit 24 fills the entire cavity space of the trenches 12, and is made electrically conductive by doping with an impurity such as phosphorus to be incorporated therein by doping during either the deposition process or by diffusion process subsequent to the deposition process.

Next, as shown in FIG. 2C, chemical mechanical polishing (shortened to CMP hereinbelow) is carried out on the entire surface of the wafer W until the surface of the

5

substrate 7 becomes exposed, by removing the polycrystalline silicon deposit 24 deposited on the upper surface of the substrate 7. This step produces a such configuration shown in FIG. 2C that the polycrystalline silicon deposit 24 is present (buried) only within the interior boundaries of the trenches 12. CMP performs planarization by a combined action of chemical and mechanical polishing using chemicals such as alkaline solution together with polishing particles. Simultaneously with or subsequent to the CMP step, the SiO₂ films 22, 23 which have been protecting the surface of the substrate 7 to this stage are also removed. The SiO₂ film 23 thus left within the trench 12 constitutes the field-shield insulator film 5 and the polycrystalline silicon deposit 24 buried in the interior of the field-shield insulator film 5 constitutes the field-shield electrode 6.

Next, as shown in FIG. 2D, the active regions 8 are subjected to the conventional fabrication steps for making MOS transistors. That is, the regions to correspond with the active regions 8 of the substrate 7 are provided with the gate insulator film 9 of SiO₂ of 10–14 nm thickness made by a process of thermal oxidation. Using the polycrystalline silicon gate electrode 4 having a gate cap insulator thereon, fabricated on top of the gate insulator film 9 by a conventional photolithographical method, as the implantation mask for arsenic (As) ion implantation, a shallow N-type diffusion layer 25 having a low-carrier concentration of 10¹⁷ ions/cm³ and a diffusion depth of about 0.1 μm. These regions constitute respectively, the source and drain diffusion layers 2 and 3 of the N-channel MOS transistor 1.

Next, as shown in FIG. 2E, device fabrication is continued to produce these transistors having an LDD structure. An insulator film is deposited on the entire surface, etched back by a conventional anisotropic etching method and formed into the insulator film 26 as a sidewall spacer, using both the insulator films 26 fabricated on both interior side-surfaces of the gate electrode 4 of the transistor 1 and the gate electrode 4 as the implantation mask. Arsenic(As) ion implantation (N-type dopant) process is carried out to produce a deep, N-type high carrier diffusion region 27 having a relatively high depth dimension of about 0.3 μm and a carrier concentration of 10¹⁸–10²¹ ions/cm³. By disposing the high carrier N-type diffusion region 27 deeper into the substrate 7 (away from the gate electrode 4) than the low carrier N-type diffusion region 25, the short channel effect is prevented, and produces an effect of lowering the electrical resistance of the source and drain diffusion layers 2 and 3. At this time, a SiO₂ film 28 is fabricated on the upper surfaces of the field-shield electrodes 6 and those of each of the source and drain diffusion layers 2 and 3 by thermal oxidation.

Next, as shown in FIG. 2F, the same fabrication steps as in the conventional MOS device making are taken to produce an insulator film 13 made of a silicate glass containing boron and phosphorous (BPSG) on the surface of the wafer W.

Finally, as shown in FIG. 2G, after fabricating contact holes, electrode lines 16, 17 are fabricated using such materials as conductive polycrystalline silicon, titanium-tungsten and aluminum in single layer or multiple layers, thus completing the fabrication steps for the MOSLSI device of the first embodiment.

In the MOSLSI device of the first embodiment, because both the field-shield insulator film 5 and the field-shield electrode 6 are buried within their own trenches 12 having a depth dimension larger than those for the source and drain diffusion layers 2 and 3, the effective isolation distance

6

between the diffusion layers 2 and 3 is equal to the distance of the width and twice the depth dimensions of a trench 12. Therefore, compared with a conventional non-buried type device, the effective isolation dimension is increased substantially. In this case, the deeper the dimension of the trench 12 than that of the source and drain diffusion layers 2 and 3, the higher would be the insulative isolation capability of the FSDI structure 11.

Additionally, especially in the first embodiment device, the field-shield electrodes do not protrude out on the upper surface of the substrate 7 as in the T-shaped electrode in the conventional devices, and the top surface of the field-shield electrode 6 is level with the surface of the substrate 7. It follows that the surface area required for the isolation structure 11 needs to be only as large as the width dimension of the trench 12, thereby significantly reducing the area for the non-active region 10 compared with that required in the conventional devices. Therefore, it is obvious that the configuration of the FSDI structure 11 will result in achieving a higher device integration in a given space of a wafer, thus enabling to provide further densification of the highly integrated MOSLSI devices.

Furthermore, according to the method for making MOSLSI device presented above, the planarization by CMP for the wafer W is carried out after depositing the polycrystalline silicon deposit 24 on the field-shield insulator film 5 by vapor deposition process, there is no need to use any photolithographic processes for fabricating the field-shield electrode 6. This is a notable simplification in the processing routine compared with the conventional process routines requiring photomasking. This means a considerable lowering in the cost of manufacturing the device having the FSDI structure of the present invention.

A second embodiment of the FSDI structure will be presented with reference to FIG. 3.

The only difference in the isolation structure between the second embodiment and the first embodiment is that the device isolation is achieved in a multi-layer structure in the second embodiment compared with the single layer structure presented in the first embodiment. Therefore, those device structures for performing the same functions are designated by the same reference numerals, and their explanations are omitted.

As shown in FIG. 3, the second embodiment device is produced by: forming the trenches 12 on the surface of a monocrystalline silicon substrate 7; followed by fabricating a triple-layer isolation film (i.e., field-shield isolator film 5) 33 comprising a first layer of SiO₂ film 30, a second layer of silicon nitride (SiN) film 31, and a SiO₂ film 32, on the interior surface of the trench 12. The device making process is continued, by growing a layer of polycrystalline silicon deposit 24 on the overall top surface by vapor deposition process, after which the surface of the wafer W is planarized by CMP method as in the first embodiment to complete the formation of the field-shield electrode 6 terminating on the common plane with the upper surface of the substrate 7.

The three-layer insulator film 33 is made by thermal oxidation of the surface of the substrate 7 including the interior surface of the trench 12 first, to produce a SiO₂ film 30 of 2–4 nm thickness, followed by forming a SiN film 31 of 4–12 nm thickness by vapor deposition process, followed by thermal oxidation of SiN layer 31 to produce a SiO₂ film 32 of 1–4 nm thickness.

The subsequent processing steps are identical to those in the first embodiment, i.e., gate-insulator film forming step; gate electrode forming step; source and drain diffusion layer

forming step; interlayer insulation forming step; contact hole fabrication step; line fabrication step are needed to complete the fabrication of MOSLSI device as shown in FIG. 3. In this embodiment, electrode lines 16, 17 are made by filling the hole sections with successive depositions of titanium nitride and tungsten films to extend to the upper surface of the interlayer insulator film at the hole sections to make electrical contact with the electrodes of other devices by means of aluminum lines.

As in the first embodiment device, the second embodiment device has no portion of the FSDI structure 11 extending on the surface of the substrate 7, thus allowing a high density integration of active circuits, and in addition, the simple method of CMP planarization of the field-shield electrode 6 with the surface of the substrate 7 enables to manufacture highly integrated MOSLSI devices economically.

Further in this embodiment, because the field-shield insulator film 5 (as manifested by a multi-layer insulator film 33) is made up of SiO₂ films 30, 32 and a SiN film 31, the field-shield isolation effect can be achieved by utilizing thin film components to further enhance the performance. The multi-layer insulator film 33 provides a highly effective insulator film exhibiting excellent shielding properties even when the polycrystalline silicon deposit 24, constituting the field-shield electrode 6, contains phosphorus or boron. In other words, according to this embodiment, by constructing the field-shield insulator film 5 to be a multi-layered composite film, it becomes possible to provide a low-defect insulator film of a substantially thinner dimension compared with a single layered isolation film, thereby improving the yield of the device as well as the shielding performance.

In the first and second embodiments, after forming the polycrystalline silicon deposit 24, the planarization step of the wafer W was carried out by using the CMP method. However, it is also permissible to utilize dry etching involving a thick coating of a photoresist material on the surface of the wafer W to etch back the entire surface of the wafer W, or to utilize wet etching involving an etching solution mixture containing primarily hydrofluoric acid and nitric acid to etch back the coating to produce a planar surface. Even though different planarization approaches may be adopted, it is still possible to simplify manufacturing processes and achieve low cost production.

Also, it is not necessary that the entire interior space of the trench be filled to construct the field-shield electrode. It is permissible to have a hollow interior structure or a cored-interior having an insulator film made by vapor depositing polycrystalline silicon followed by another vapor growth of SiO₂. The top surfaces of the electrode and the upper surface of the substrate may be made planar using the usual CMP method.

The dimensions quoted in the embodiments are meant to be examples, and they are not limited to the exact dimensions quoted. For example, it is permissible to have a range of dimensions such as: the trench widths may range from 80 nm—several mm; the depth of the trench may be made deeper by up to 10 μm than the depth of the diffusion layers for source and drain; the film thickness of the field-shield insulator film may range 5–200 nm; and the film thickness of the polycrystalline silicon film may range 40–800 nm.

In the second embodiment, the triple-layer structure of the insulator film (SiO₂—SiN—SiO₂) may be replaced with a double-layer structure by omitting one of the SiO₂ films without affecting the shielding performance of the device of the present invention.

A third embodiment will be presented with reference to FIG. 4.

In this embodiment, the arrangement of voltage application to the field-shield electrode will be explained with reference to the cross sectional view of the MOSLSI device of this embodiment and the device connection lines shown in FIG. 4.

FIG. 4 shows a P-type monocrystalline silicon substrate 35 having an N-type region 36, the so-called “N-Well” region, fabricated on its surface. The region 36 comprises P-channel MOS transistors TRp. Adjacent to the N-well region 36, there are N-channel transistors TRN1, TRN2, thereby providing an LSI device based on a CMOS (complementary metal oxide semiconductor) structure on the surface of the substrate W.

The isolation for the N-channel MOS transistors TRN1, TRN2 is provided by the FSDI structures fabricated in the trenches formed between the transistors. As shown in FIG. 4, each of the field-shield electrodes 37 has an electrode line FSn, and the N-channel MOS transistor TRN1 has a gate line Gn from the gate electrode 38, a source line Sn from the N-type source diffusion layer 39, a drain line Dn from the N-type drain diffusion layer 40, and electrode lines SBn from the P-type substrate 35 through the P-type diffusion layer 41.

In the meanwhile, the isolation for the P-channel MOS transistor fabricated within the N-well 36 is provided by a FSDI structures similar to the case of the N-channel MOS transistors TRN1, TRN2. As shown in FIG. 4, each of the field-shield electrodes 42 has an electrode line FSp, and the P-channel MOS transistor TRp has a gate line Gp from the gate electrodes 43, a source line Sp from the P-type source diffusion layer 45, a drain line Dp from the P-type drain diffusion layer 44, and electrode lines SBp from the N-well region 36 through the N-type diffusion layers 46. These device lines extend parallel to the surface of the substrate 35 on the upper surface of the interlayer insulator film 47.

For any of the FSDI structures (separating the N-channel MOS transistors TRN1, TRN2 and P-channel MOS transistor TRp) presented in this embodiment, the field-shield insulation films 48, 49 may be a single layer structure presented in the first embodiment or a multi-layer structure presented in the second embodiment can be utilized.

The device in this embodiment is constructed so as to supply a negative voltage of −1—3 volts to the P-type substrate 35 from a substrate voltage generation circuit (not shown) connected to the electrode line SBn, as well as to the electrode lines FSn for the field-shield electrodes 37 disposed on the N-channel MOS transistors TRN1, TRN2, thereby supplying the same negative voltage to the field-shield electrodes 37.

In the meanwhile, the electrode line FSp for the field-shield electrode 42 in the P-channel MOS transistor TRp circuit is normally connected to a step-up voltage generation circuit (not shown) provided for the purpose of supplying word line driving potential or output buffer driving potential. In the device of this embodiment, a step-up voltage Vcc+2Vtn is supplied to the field-shield electrode 42, where Vtn is the threshold voltage of the N-channel MOS transistor.

It can be seen that the CMOS structure of the third embodiment device is also highly suitable for isolation of active regions of transistor devices and diffusions layers. The FSDI structures fabricated within the respective trenches belonging to each of N-channel MOS transistors and P-channel MOS transistors are therefore applicable to higher integration of MOSLSI devices.

Further, in the third embodiment device, the circuit is arranged in such a way that a negative potential is applied to the field-shield electrodes 37 for N-channel MOS transistors TRN1, TRN2, and a step-up voltage from the supply voltage is applied to the field-shield electrode 42 for the P-channel MOS transistor TRp, in contrast to the conventional field-shield devices, in which a GND potential is applied to the N-devices and the supply voltage to the P-device, and therefore, the tolerance capacity for overshooting/undershooting in the diffusion layer potential has been made comparatively larger, thereby providing a more stable isolation performance.

In other words, the third embodiment demonstrated the adaptation of the trench-type FSDI structure to a CMOSLSI device to provide effective inter-transistor isolation or inter-diffusion region isolation, thereby showing a path to realization of future ultra-high density LSI architectures.

A fourth embodiment will be explained in the following with reference to FIG. 5.

FIG. 5 is a FSDI structure in a MOSLSI comprising: a P-type semiconductor substrate 101; an N-channel MOS transistor 102; a source diffusion layer 103; a drain diffusion layer 104; a gate electrode 105; field-shield isolator film 106; field-shield electrodes 107; and high carrier P-type regions 108.

As shown in FIG. 5, an N-channel MOS transistor 102 is fabricated in active regions 109 on an upper surface of the P-type semiconductor substrate 101. The N-channel MOS transistor 102 comprises: a gate electrode 105 of a polycrystalline silicon film; and a gate insulator film 110 of SiO₂; N-type source and drain diffusion layers 103, 104 having a lightly doped drain structure (LDD-structure). Between the active regions 109 are non-active regions 111 in which the FSDI structure 112 is fabricated to isolate the N-channel MOS transistor 102.

The FSDI structure 112 comprises a field-shield insulator film 106, a field-shield electrode 107 and a high carrier P-type region 108. Inside the non-active region 111, there are trenches 113 which open to the upper surface of the P-type substrate 101 and having a depth dimension larger than the source and drain diffusion layers 103, 104. The field-shield isolator film 106 is formed on the side walls of the trench 113. A field-shield electrode 107 is buried in the interior of the trench 113 surrounded by the field-shield isolator film 106, and the top surface of the field-shield electrode 107 is level with the upper surface of the P-type substrate 101. An interlayer insulator film 114 is fabricated above the field-shield electrode 107, and a high carrier P-type region 108 (having a higher concentration of B than that in the P-type substrate 101) is fabricated at the bottom surface of the trench 113.

Additionally, electrode lines 116 are provided from the source and drain diffusion layers 103 and 104, respectively, through the contact holes 115.

A method of fabricating the above MOSLSI structure will be presented with reference to the processing steps illustrated in FIGS. 6A to 6I.

First, as shown in FIG. 6A, the trenches 113 are fabricated on the upper surface of a wafer W (including a substrate 101 of a P-type single crystal silicon having a specific resistance 3–4 ohm·cm) by process of etching through an etching mask of a SiO₂ film 117 which protects those active regions 109 for making the N-channel MOS transistor but exposes those regions for making the trenches 113.

The process of forming the trenches 113 is a dry etching process using gaseous chlorine to make cavities measuring

0.5–1.5 μm in depth and 0.2–0.5 μm in width. As illustrated in FIG. 6A, the etching process is carried out under conditions to favor etching on the side-wall surface of the cavities so that the width A of the trench 113 can be made to include an undercutting dimension C of about 0.02–0.2 μm more than the opening dimension B on the SiO₂ film 117. This undercut structure facilitates making of the subsequent fabrication of insulative isolation with trenches 113 to surround the active regions 109.

Next, as shown in FIG. 6B, a SiO₂ insulator film 118 having a 10–80 nm thickness is fabricated on the surface of the wafer W by means of a thermal oxidation process or a vapor deposition process, thereby encasing the SiO₂ film 117 deposited on the active regions 109 as well as the interior surfaces of the trenches 113 with the insulator film 118.

Next, as shown in FIG. 6C, the entire surface of the wafer W is dry etched so as to remove the insulator film 118 from the bottom surface of the trenches 113, thereby exposing the internal surface of the substrate 101 at the bottom of the trenches 113. This dry etching step is carried out under an anisotropic etching condition so as to remove the insulator film 118 from the upper surface of the active regions 109 and from the bottom surface of the trenches 113, but to leave the insulator film 118 on the side-wall surfaces of the trenches 113 untouched.

Next, as shown in FIG. 6D, boron (B) is introduced into the bottom surface of the trenches 113, which corresponds to the substrate 101, by ion-implantation to produce a P-type region 108 of a high carrier concentration of 10^{18} – 10^{20} ions/cm³. This step is followed by vapor deposition step of depositing a polycrystalline silicon deposit 119 of 100–500 nm thickness to act as the field-shield electrode. The polycrystalline silicon deposit 119 is deposited so as to fill the entire interior space of the trenches 113 as well as to cover the entire surface of the wafer W. The polycrystalline silicon deposit 119 is made conductive by doping phosphorous or boron either during the vapor deposition step or after the vapor deposition step.

Incidentally, in this embodiment, ion-implantation is used to produce the P-type high carrier region 108 followed by a vapor deposition step to form the polycrystalline silicon deposit 119. It is also permissible to first carry out forming of the field-shield electrode by filling the trenches with polycrystalline silicon film containing B (the identical doping type as the substrate) prior to fabricating the P-type regions. The next step is to thermally diffuse B from the polycrystalline silicon film to form the high carrier P-type region. The advantage is that the ion-implantation step can be eliminated.

Next, as shown in FIG. 6E, the surface of the wafer W is subjected to CMP polishing step to remove the polycrystalline silicon deposit 119 until the surface of the substrate 101 becomes exposed so that the polycrystalline silicon fills only the trenches 113. Simultaneously with or subsequent to the polishing step, the surface SiO₂ film 117 which has protected the active regions 109 on the substrate 101 to this stage is also removed. This configuration provides the field-shield insulator film 106 constituted by the SiO₂ insulator film 118 remaining on the side-wall surfaces of the trenches 113, and the field-shield electrode 107 constituted by the polycrystalline silicon filling the interior spaces of the trenches 113.

Next, as shown in FIG. 6F, the active regions 109 are subjected to the conventional fabrication steps for making MOS transistors. That is, on the regions to correspond with the active regions 109 of the substrate 101 are provided with the gate insulator film 110 of SiO₂ having a thickness of

11

10–14 nm by a process of thermal oxidation. Using the polycrystalline silicon gate electrode **105**, fabricated on top of the gate insulator film **110**, as the implantation mask for arsenic (As) ion implantation, a shallow N-type diffusion layer **120** having a low-carrier concentration of 10^{17} – 10^{10} ions/cm³ is fabricated so as to provide a diffusion depth of about 0.1 μ m. These regions constitute, respectively, the source and drain diffusion layers **103** and **104** of the N-channel MOS transistor **102**.

Next, as shown in FIG. 6G, processing steps are carried out to make these transistors to have an LDD structure. That is, using the insulator films **121** fabricated on both side-wall surfaces of the gate electrode **105** of the transistor **102** together with the gate electrode **105** as the implantation mask, As-ion (N-type dopant) implantation step is carried out to produce a deep N-type, high carrier diffusion layer region **122** having a carrier concentration of 10^{18} – 10^{21} ions/cm³ and a diffusion depth dimension of about 0.3 μ m. This high carrier N-type diffusion layer region **122** extends further deeper into the substrate away from the gate electrode **105** than the region of the N-type low carrier diffusion layer **120**, thereby preventing short channel effect, and produces an effect of lowering the resistance value of the source and drain diffusion layers **102** and **103**. Also, SiO₂ film **123** is fabricated on the upper surfaces of the field-shield electrodes **107** and each of the source and drain diffusion layers **103** and **104** by thermal oxidation.

Next, as shown in FIG. 6H, the same fabrication steps as in the conventional MOS device making are taken to produce an insulator film **114** made of a silicate glass containing boron and phosphorous (BPSG) on the surface of the wafer W, after which contact holes **115** are fabricated on the upper surface of the source and drain diffusion layers **103** and **104** using photolithography.

Finally, as shown in FIG. 6I, using such materials as conductive polycrystalline silicon, titanium-nitride, titanium-tungsten as a barrier material, electrode line **116** is fabricated using aluminum or tungsten in single layer or multiple layers, thus completing the fabrication steps for the MOSLSI device of the this embodiment.

In the MOSLSI device of the fourth embodiment, because both the field-shield insulator film **106** and the field-shield electrode **107** are buried within their own trenches **113** having a depth dimension larger than those for the source and drain diffusion layers **103** and **104**, the effective isolation distance between the diffusion layers **103** and **104** is equal to twice the total distance of the width and depth dimensions of a trench **113**. Therefore, it can be seen that, compared with the non-buried type conventional devices, the isolation dimension is substantially increased. In this case, the deeper the trench **113** than the source and drain diffusion layers **103** and **104**, the higher would be the insulative isolation capability.

Additionally, especially in the device of this embodiment, the field-shield electrode does not protrude out on the surface of the substrate **101** as in the conventional devices, and the top surface of the field-shield electrode **107** is level with the surface of the substrate **101**. It follows that the surface area required for the FSDI structure **112** needs to be only as large as the width dimension of the trench **113**, thereby significantly reducing the area for the non-active region **111** compared with the conventional field shielding devices.

Furthermore, the field-shield electrode **107** is not insulated from the substrate **101** but is in electrical contact with the internal surface of the substrate **101** through the bottom

12

surface of the trench **113**. This configuration means that a voltage can be applied to the field-shield electrode **107** from the substrate **101** side, thus eliminating the need to provide the voltage application line necessarily on the top surface of the field-shield electrode **107**. Therefore, it is obvious that the accumulation of such advantages accruing from the present configuration of the FSDI structure **112** will result in achieving higher device integration in a given space of a wafer, thus enabling to produce even more highly integrated MOSLSI devices.

Furthermore, according to the method for making MOSLSI device presented above, the planarization step for the wafer W by CMP method is carried out after the process of forming the polycrystalline film **119** by vapor deposition on the field-shield insulator film **106**, there is no need for using photolithography for fabricating the field-shield electrode **107**. This is a notable simplification in the processing steps compared with the conventional process requiring photomasking, resulting in considerable lowering in the manufacturing cost.

A fifth embodiment of the FSDI structure of the present invention will be explained with reference to FIG. 7.

There are two points of differences between the fourth embodiment device and the device of this embodiment. The first point is that the FSDI structure in the fifth embodiment is a multilayer structure, not a single layer structure presented in the fourth embodiment. The second point is that doping is carried out on the side-wall surfaces of the trenches also. Therefore, those components in FIG. 7 which are the same as those in the fourth embodiment are given the same reference numerals, and their explanations are omitted.

Subsequent to the trench-forming step shown in FIG. 6A for forming the trenches **113**, the substrate **101** of this device is subjected to a diffusion step to diffuse the boron dopant to produce a P-type region **125** having a carrier concentration of about 10^{17} – 10^{18} ions/cm³ on all the interior surfaces of the trenches **113**. Here, those areas of the interior surfaces close to the substrate **101** are replaced with N-type doped regions during a subsequent fabrication step to produce N-type source and drain regions.

Next, following the fabrication of a triple layer insulator film **129** comprising SiO₂ film **126**–SiN film **127**–SiO₂ film **128** (to act as the field-shield insulator film **106**), the bottom surfaces of the trenches **113** are exposed by anisotropic etching and are covered over with a polycrystalline silicon film **119** by vapor deposition. As in the fourth embodiment, the top surface of the field-shield electrode **107** comprised of polycrystalline silicon film **119** is planarized and made level with the upper surface of the substrate **101** by CMP method.

The triple layer insulator film **129** is made by thermal oxidation of the surface of the substrate **1** including the interior surface of the trench **113** first, to produce a SiO₂ film **126** of 2–4 nm thickness, followed by forming a SiN film **127** of 4–12 nm thickness by vapor deposition process, followed by thermal oxidation of SiN film **126** to produce a SiO₂ film **128** of 1–4 nm thickness.

The subsequent processing steps are identical to those in the fourth embodiment, i.e., gate-insulator film forming step; gate electrode forming step; source and drain forming step; interlayer insulation forming step; contact hole fabrication step; line fabrication step are needed to complete the fabrication of MOSLSI device as shown in FIG. 7. In this embodiment, electrode lines **116** comprises aluminum device lines, and are made by filling the contact holes **115** with successive depositions of titanium nitride-tungsten films to extend, through the contact holes **115**, to the upper

surface of the interlayer insulator film 114 to make contact with other devices through the aluminum device lines.

As in the case of the fourth embodiment device, the same beneficial effects accrue from the FSDI structure 112 of this embodiment. That is, the field-shield electrode 107 in this embodiment also does not extend on the upper surface of the substrate 101 as in the conventional devices, and by eliminating the need for the voltage impression lead line to be provided necessarily on the top surface of the field-shield electrode 107, higher device integration can be achieved in a given space of a wafer. Coupled with the use of simple CMP method for making the surfaces of field-shield electrode 107 level with that the substrate 101, the configuration of the device enables to produce highly integrated MOSLSI devices economically.

On the other hand, in contrast to the fourth embodiment device, the trenches 113 in the MOSLSI device of this embodiment are provided with P-type regions 125 on its side-wall surfaces as well as on its bottom surface. Therefore, the P-type region 125 at the bottom surface can be used to supply voltage to the device, whereas the P-type region 125 on the side-wall surfaces of the device also functions to prevent the formation of inversion layers connecting the N-type source diffusion layers 103 with N-type drain diffusion layers 104. Thus, it can be seen that the adoption of the FSDI structure 112 will further enhance the isolation effects and the operating performance of a MOSLSI device.

Further, in the device of this embodiment, the film for constituting the field-shield insulator film 106 comprises SiO₂ films 126, 128 and a SiN film 127. Therefore, the field-shield insulator film 106 can be effectively made from thin film components so further enhancing the isolation capability. The multilayer insulator film 129, comprising SiO₂ films 126, 128 and a SiN film 127, is able to retain high electrical isolation even when the polycrystalline silicon 119 (constituting the field-shield electrode 107) contains phosphorous or boron. In other words, by making the field-shield insulator film 106 to be a multilayer film, a highly effective insulator film of thin film thickness with lesser number of defects can be produced, thus leading to higher device yield to provide economical production while offering enhanced isolation effect.

In the fourth and fifth embodiments, the planarization step of the wafer W using the CMP method was carried out after forming the polycrystalline deposit 119, however, it is also permissible to utilize dry etching involving a thick coating of a photoresist material applied all over on the surface of the wafer W to etch back the entire surface of the wafer W, or to utilize wet etching involving an etching solution mixture containing primarily hydrofluoric acid and nitric acid to etch back the surface to produce a planar surface. Even though different planarization approach may be taken, it is still possible to simplify manufacturing processes and achieve low cost production.

Also, it is not necessary to follow the previous embodiments in which the entire interior space of the trench 113 was filled to construct the field-shield electrode 107. It is permissible to have a hollow interior structure or to fill the interior by depositing polycrystalline silicon followed by vapor deposition of SiO₂. The surface may be made planar using the usual CMP method.

It should be noted that the dimensions quoted in the embodiments are meant to be illustrative, and they are not limited to the dimensions quoted. For example, it is permissible to have ranges of dimensions such as: 80 nm—several

mm for the trench widths; the depth of the trench may be made deeper than the depth of the diffusion layers for source and drain components by up to 10 μm; the film thickness of the field-shield insulator film may range 5–200 nm; and the film thickness of the polycrystalline deposit may range 40–800 nm.

In the fifth embodiment, the triple-layer structure of the insulator film (SiO₂—SiN—SiO₂) may be replaced with a double-layer structure by omitting one of the SiO₂ films without affecting the shielding performance of the device of the present invention.

A sixth embodiment will be explained with reference to FIG. 8.

In this embodiment, the arrangement of the voltage application to the field-shield electrode will be explained with reference to the cross sectional view of the MOSLSI device and the lines shown in FIG. 8.

FIG. 8 shows a P-type single crystal silicon substrate 131 having an N-type region 132, the so-called “N-Well” region, fabricated on its surface. The N-well region 132 comprises a P-channel MOS transistor TRp. Adjacent to the N-well region 132, there are N-channel MOS transistors TRN1, TRN2, thereby providing an LSI device based on a CMOS structure on the surface of the substrate 131.

The isolation function for the N-channel MOS transistors TRN1, TRN2 is provided by the FSDI structures fabricated in the trenches formed between the transistors. As shown in FIG. 8, the N-channel MOS transistor TRN1 has an electrode line FSn from the field-shield electrodes 133, a gate line Gn from the gate electrode 134, a source line Sn from the N-type source diffusion layer 135, a drain line Dn from the N-type drain diffusion layer 136, and electrode lines SBN from the P-type substrate 131 through the bottom surface of the P-type substrate 131. Although the PN-junction is included between the P-type substrate 131 and the N-type field-shield electrode 133, the potential of the substrate electrode SBN is approximately the same as the potentials at the N-type field-shield electrode 133 and at the electrode line FSN.

In the meanwhile, the isolation function for the P-channel MOS transistor fabricated within the N-well region 132 is provided by a similar FSDI structures, and the electrode line FSp from each of the field-shield electrodes 137 is provided as necessary, a gate line Gp from the gate electrodes 138, a source line Sp from the P-type source diffusion layer 139, a drain line Dp from the P-type drain diffusion layer 140. The field-shield electrode 137 is made of an N-type polycrystalline silicon containing phosphorous (P), and the diffusion of P from the N-type polycrystalline silicon produces a high carrier N-type region 141 within the N-Well region 132, thus making the field-shield electrode 137 to be at the same potential as the N-Well region 132.

For any of the FSDI structures (separating the N-channel MOS transistors TRN1, TRN2 and P-channel MOS transistor TRp), the single layer structure presented in the fourth embodiment or the multi-layer structure presented in the fifth embodiment can be utilized. In the sixth embodiment device also, the electrode lines extend on the upper surface of the interlayer insulator film 142 parallel to the surface of the substrate 131.

The device in this embodiment includes an electrical power line electrode Vcc, Vss (not shown) for connecting to outside circuits. Vcc is supplied with a positive voltage (usually 5 volts) from an outside power source, and Vss is supplied with a reference voltage (usually 0 volt GND).

In the sixth embodiment device, the field-shield electrode 133 on the TRN1, TRN2 side of the N-channel MOS

15

transistor is supplied with the substrate potential, and the substrate **131** is maintained at a negative voltage of $-1 \sim -3$ volts which is the power circuit generation voltage of the device. The device is designed so that this voltage can be monitored through the electrode line FSN.

In the meanwhile, the potential of the electrode line FSp for the field-shield electrode **137** in the P-channel MOS transistor TRp side is positive and maintained approximately at the source potential, and the N-Well region **132** is also maintained positive at the source potential through the field-shield electrode **137**.

It can be seen that, as in the devices presented in the fourth and fifth embodiments, the FSDI structure of this embodiment fabricated within the respective trenches belonging to each of N-channel MOS transistors and the P-channel MOS transistor is also highly suitable for adaptation to CMOSLSI devices for isolation of active regions.

Further, in the device of this embodiment, because the N-type field-shield electrode **133** and the P-type substrate **131** are electrically conductively joined, the basic function of the base electrode SBN to supply a potential to the substrate **131** has been extended. The base electrode SBN can perform the role of supplying the substrate potential to the N-type field-shield electrode **133** as well as to monitor the substrate potential through the electrode line FSN provided above the N-type field-shield electrode **133**. Further, because the P-type field-shield electrode **137** and the N-Well region **132** are electrically conductively joined, the positive potential supplied to the P-type field-shield electrode **137** through the electrode line FSp is also supplied to the N-Well region **132**, thus eliminating the need for providing a separate electrode line for the N-Well region **132**.

In other words, in the design of the device presented in this embodiment, the need has been eliminated for providing individual electrode lines for different functions of the various electrodes, for example, potential supply to field-shield electrode, potential supply to the substrate or monitoring of various potentials. Therefore, it may be noted that an important consequence of the design demonstrated in the sixth embodiment device is that the elimination of the need to provide electrode lines above the different electrodes in the FSDI structure of the present invention leads logically to an overall simplification in the interconnection lines required for CMOSLSI devices.

In other words, the sixth embodiment demonstrated the application of the trench-type FSDI structure to the trench-type FSDI structure of the present invention in a CMOSLSI device to provide effective inter-transistor isolation or inter-diffusion region isolation, thereby showing a path to the future development of ultra-high density LSI circuitries.

It should be noted that the particular components and device arrangements used in the six embodiments presented above are illustrative and do not limit the scope of the principle of device design demonstrated in the present invention that the shielding effect of field-shield device isolation (FSDI) structure is enhanced by adopting a configuration of a trench-type field-shield electrode as well as trans-electrode single processing. It is clear that the FSDI structure presented is applicable to device isolation in a wide variety of semiconductor devices, such as DRAM and the like memory devices, microcomputer LSI, logic devices. It is also obvious that the application possibilities include PMOS, NMOS as well as CMOS devices.

What is claimed is:

1. A semiconductor device means having a field-shield device isolation structure fabricated in non-active regions of

16

said semiconductor device means arranged on a semiconductor substrate, said field-shield device isolation structure comprising:

a field-shield insulator film for providing inter-device electrical isolation for a plurality of devices fabricated on said semiconductor substrate;

a field-shield electrode connected to receive at least one of either a negative potential applied to a N-type device isolation region or a step-up potential of a source voltage applied to a P-type device isolation region;

wherein said field-shield insulator film is formed on interior surfaces of a trench cavity whose cavity opening faces an upper surface of said semiconductor substrate and whose depth dimension is deeper than a diffusion distance of a dopant species associated with a device of said plurality of devices; and

wherein said field-shield electrode is buried in an interior space of said trench cavity lined with said field-shield insulator film so that a top surface of said field-shield electrode is level with said upper surface of said semiconductor substrate.

2. A semiconductor device means having a field-shield device isolation structure fabricated in non-active regions of said semiconductor device means arranged on a semiconductor substrate of a given conductivity type, said field-shield device isolation structure comprising:

a field-shield insulator film for providing inter-device electrical isolation for a plurality of devices fabricated on said semiconductor substrate;

a field-shield electrode connected to receive at least one of either a negative potential applied to a N-type device isolation region or a step-up potential of a source voltage applied to a P-type device isolation region;

wherein said field-shield insulator film is formed on interior surfaces of a trench cavity whose cavity opening faces an upper surface of said semiconductor substrate and whose cavity depth dimension is deeper than a diffusion distance of a dopant species associated with a device of said plurality of devices; and

wherein said field-shield electrode is buried in an interior space of said trench cavity lined with said field-shield insulator film so that a top surface of said field-shield electrode is level with said upper surface of said semiconductor substrate and so that a bottom surface of said field-shield electrode is in electrical contact with said semiconductor substrate.

3. A semiconductor device means having a field-shield device isolation structure fabricated in non-active regions of said semiconductor device means arranged on a semiconductor substrate of a given conductivity type, said field-shield device isolation structure comprising:

a field-shield insulator film for providing inter-device electrical isolation for a plurality of devices fabricated on said semiconductor substrate;

a field-shield electrode for providing inter-device and external electrical communications, said field shield electrode connected to receive at least one of either a negative potential applied to a N-type device isolation region or a step-up potential of a source voltage applied to a P-type device isolation region;

wherein said field-shield insulator film is formed on interior surfaces of a trench cavity whose cavity opening faces an upper surface of said semiconductor substrate and whose cavity depth dimension is deeper than a diffusion distance of a dopant species associated with a device of said plurality of devices; and

17

wherein said field-shield electrode is buried in an interior space of said trench cavity lined with said field-shield insulator film so that a top surface of said field-shield electrode is level with said upper surface of said semiconductor substrate and so that a bottom surface of said field-shield electrode is in direct electrical contact with said semiconductor substrate through said bottom surface of said trench cavity and a doped region of an identical conductivity type to said given conductivity type in a region of said semiconductor substrate abutting said bottom surface of said trench cavity.

4. A semiconductor device means having a field-shield device isolation structure fabricated in non-active regions of said semiconductor device means arranged on a semiconductor substrate of a given conductivity type, said field-shield device isolation structure comprising:

- a field-shield insulator film for providing inter-device electrical isolation for a plurality of devices fabricated on said semiconductor substrate;
- a field-shield electrode for providing inter-device and external electrical communications, said field-shield electrode is connected to receive at least one of either a negative potential applied to a N-type device isolation region or a step-up potential of a source voltage applied to a P-type device isolation region;

18

wherein said field-shield insulator film is formed on interior surfaces of a trench cavity whose cavity opening faces an upper surface of said semiconductor substrate and whose cavity depth dimension is deeper than a diffusion distance of a dopant species associated with a device of said plurality of devices;

wherein said field-shield electrode is buried in an interior space of said trench cavity lined with said field-shield insulator film so that a top surface of said field-shield electrode is level with said upper surface of said semiconductor substrate and so that a bottom surface of said field-shield electrode is in direct electrical contact with said semiconductor substrate through said bottom surface of said trench cavity and a doped region of an identical conductivity type to said given conductivity type in a region of said semiconductor substrate abutting said bottom surface of said trench cavity; and

wherein further doped regions of an identical conductivity type to said given conductivity type are additionally provided in portions of said semiconductor substrate opposite to said field-shield insulator film formed on the side-wall surfaces of said trench cavity.

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