UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SMIC, AMERICAS,
Petitioner,

v.

INNOVATIVE FOUNDRY TECHNOLOGIES, LLC,
Patent Owner.

Case No. IPR2020-01003
U.S. Patent No. 6,580,122

DECLARATION OF JOHN C. BRAVMAN, PH.D.

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I, John C. Bravman, being of legal age, hereby declare affirm, and state the following:

I. INTRODUCTION

1. I have been retained on behalf of Patent Owner, Innovative Foundry Technologies, LLC, to offer opinions regarding certain aspects of U.S. Patent No. 6,580,122 and IPR2020-01003. I have personal knowledge of the facts and opinions set forth in this declaration, and, if called upon to do so, I would testify competently thereto. All of the opinions and conclusions found in this declaration are my own.

2. I am working as an independent consultant in this matter and am being compensated at my normal consulting rate of $775 per hour for my time. My compensation is in no way dependent on the outcome of this matter. I have no financial interest in the Petitioner.

II. BACKGROUND AND QUALIFICATIONS

3. My academic training was at Stanford University, where I received a Bachelor of Science degree in Materials Science and Engineering in 1979, and a Master of Science degree in 1981, also in Materials Science and Engineering. I completed my Doctor of Philosophy degree in 1984, with a dissertation that focused on the nature of silicon – silicon dioxide interfaces as found in integrated circuit devices.

4. From 1979 to 1984, while a graduate student at Stanford, I was employed part-time by Fairchild Semiconductor in their Palo Alto Advanced Research Laboratory. I worked in the Materials Characterization group. In 1985, upon completion of my doctorate, I joined the faculty at Stanford as an Assistant Professor of Materials Science and Engineering. I was promoted to Associate Professor with tenure in 1991 and achieved the rank of Professor in 1995. In 1997 I was named to the Bing Centennial Professorship. In 2001 my faculty appointment was broadened to include the Department of Electrical Engineering.

5. At Stanford I held multiple administrative and leadership roles. I was Chairman of the Department of Materials Science and Engineering from 1996 to 1999, and Director of the Center for Materials Research from 1998 to 1999. I served as Senior Associate Dean of the School of Engineering from 1992 to 2001 and the Vice Provost for Undergraduate Education from 1999 to 2010. On July 1, 2010, I retired from Stanford University and assumed the Presidency of Bucknell University, where I also became a Professor of Electrical and Computer Engineering.

6. I have worked for more than 35 years in the areas of thin film materials processing and analysis. Much of my work has involved materials for use in microelectronic interconnects and packaging, and in superconducting structures and systems. With regard to integrated circuits, I led investigations

involving aluminum, copper and tungsten metallizations, polycrystalline silicon, metal silicides, a variety of oxide and nitride dielectrics, and barrier layers such as titanium and tantalum-based nitrides. Further, my groups blended fundamental aspects of the behavior of microelectromechanical systems—specifically, compliant multilayer cantilever beams—for possible test probe and package implementations. In this work my group investigated the mechanical behavior of underfill systems as found in a variety of flip chip and other packaging systems, focusing on the relationship between microstructures, processing, and adhesion.

7. I have also led multiple development efforts of specialized equipment and methods for determining the microstructural and mechanical properties of materials and structures. My group designed and built the first high voltage SEM for in-situ studies of electromigration, the first high temperature wafer curvature system, and the first microtensile tester for micron-scale structures, amongst many others. As a graduate student I developed one of the earliest methodologies for obtaining high resolution cross section transmission electron micrographs of integrated circuit structures, pre-dating the commercialization of what has become an important component of "reverse engineering" for thin film structural and chemical analyses.

8. My work has been published extensively in more than 160 technical publications, and I have given over 50 invited talks, as well as nine keynote

lectures. My publications have been cited more than 4,500 times with an h-index of roughly 40.

9. I have taught a wide variety of courses at the undergraduate and graduate level in materials science and engineering, emphasizing both basic science and applied technology, including coursework in the areas of integrated circuit materials and processing. Some of these courses focused on processes (e.g., cleaning, etching, deposition, doping, oxidation, lithography, etc.) used in the production of integrated circuits. More than two thousand students have taken my classes, and I have trained 24 doctoral students, most of whom now work in the microelectronics industry.

10. I am a member of many professional societies, including the Materials Research Society, the Institute of Electrical and Electronic Engineers, the American Society of Metals, the Microscopy Society of America, and the American Physical Society. I was heavily involved with the Materials Research Society for more than 20 years, including service as its President in 1994.

11. A copy of my curriculum vitae is attached as Appendix A.

III. MATERIALS CONSIDERED

12. In developing my opinions, I have considered the IPR pleadings, including the Petition, Preliminary Response, Decision Granting Institution, the materials cited herein, and the following exhibits:

Exhibit	Description
Exhibit 1001	U.S. Patent No. 6,580,122 to Wristers et al. (the "**'122 patent**")
Exhibit 1002	Declaration of Dr. Sayfe Kiaei ("**Kiaei**")
Exhibit 1003	Korean Laid-Open Patent Application No. KR1998-074469 (with associated certified English translation and translator's declaration) ("**Yun**")
Exhibit 1004	U.S. Patent No. 5,859,466 ("**Wada**")
Exhibit 1005	U.S. Patent No. 6,009,023 ("**Lu**")
Exhibit 1006	U.S. Patent No. 5,960,297 ("**Saki**")

13. Other background references, of which I had been previously aware, and not cited herein, that a person of ordinary skill in the art ("POSITA") at the time of the invention would have recognized as being related to the subject matter of the '122 patent.

14. Although this Declaration refers and cites to selected portions of the cited references for the sake of brevity, it should be understood that a POSITA would have viewed the references cited herein in their entirety and in combination with other references cited herein or cited within the references themselves. The references used in this Declaration, therefore, should be viewed as being incorporated herein in their entirety.

15. This Declaration is made based on information currently available to me. I intend to continue my investigation and study, which may include a review

of documents and information that may yet be produced, as well as deposition testimony from depositions for which transcripts are not yet available or that may yet be taken in this proceeding. Therefore, I expressly reserve the right to expand or modify my opinions as my investigation and study continue, and to supplement my opinions in response to any additional information that becomes available to me, any matters raised by Patent Owner and/or other opinions provided by Patent Owner's expert(s), or in light of any relevant orders from the Patent Trial and Appeal Board or other authoritative body.

IV. PERSON OF ORDINARY SKILL IN THE ART

16. I understand that the content of the '122 patent and prior art should be interpreted the way a POSITA would have interpreted the material at the time of invention.

17. I understand that the "time of invention" for the Asserted Patent is the date that the inventor filed the earliest patent application—March 20, 2001.

18. I understand that the factors considered in determining the ordinary level of skill in the art include the level of education and experience of persons working in the field, the types of problems encountered in the field, and the sophistication of the technology.

19. Based on my analysis of the '122 patent and the prior art references, in my opinion a POSITA within the field of the '122 patent, which is the art of

designing, manufacturing, and/or fabricating semiconductor devices, components, and/or transistors, around the early 2000 time period would have a bachelor's or master's degree in electrical engineering, materials science and engineering, or related fields, and at least 2-4 years' experience working in electrical engineering or materials science and engineering, or related fields, or an equivalent amount of work experience, graduate work, or graduate education.

20. I was a person of at least ordinary skill in the art at the time of the alleged invention of the '122 patent.

V. LEGAL STANDARDS

21. In preparing and expressing my opinions and considering the subject matter of the '122 patent, I am relying on certain basic legal principles that counsel have explained to me.

22. I have been informed that a claim may be invalid as obvious if the subject matter described by the claim as a whole would have been obvious to a POSITA at the time the claimed invention was made. I understand that the standard for obviousness in an *inter partes* review proceeding is by a preponderance of the evidence.

23. I have also been informed that a determination of obviousness involves an analysis of the scope and content of the prior art, the similarities between the claimed invention and the prior art, and the level of ordinary skill in

the art. I have been informed and understand that a prior art reference should be viewed as a whole.

24. I have been informed that in considering whether an invention for a claimed combination would have been obvious, I may assess whether there are apparent reasons to combine known elements in the prior art in the manner claimed in view of interrelated teachings of multiple prior art references, the effects of demands known to the design community or present in the market place, and/or the background knowledge possessed by a POSITA. I also understand that other principles may be relied on in evaluating whether a claimed invention would have been obvious.

25. I have been informed that, in making a determination as to whether or not the claimed invention would have been obvious to a POSITA, one may consider certain objective indicators of non-obviousness if they are present, such as: commercial success of product(s) practicing the claimed invention; long-felt but unsolved need; teaching away; unexpected results; copying; and praise by others in the field. I understand that for such objective evidence to be relevant to the non-obviousness of a claim, however, there must be a causal relationship (called a "nexus") between the claim and the evidence. I also understand that this nexus must be based on a novel element of the claim rather than something available in the prior art.

26. I have also been informed and understand that when considering the obviousness of a patent claim, one should consider whether a reason or motivation existed for combining the elements of the references in the manner claimed, and that the prior art must create a reasonable expectation of success in producing the claimed subject matter.

VI. CHALLENGED CLAIMS 5, 16, AND 27: GROUNDS 3, 5, AND 7

27. Challenged claims 5, 16, and 27 require a recessed isolation structure "formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å," as exemplified by claim 5:

> 5. The transistor of claim 1, wherein said recessed isolation structure is formed in a trench having a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å.

(Ex. 1001, claim 5).

28. The Petition concedes that neither *Yun* (the primary reference in both Grounds 3 and 5) nor *Saki* (the primary reference in Ground 7) teach the "trench . . . depth ranging from approximately 4000-5000 Å" limitation, and relies on secondary reference *Wada* to cure these deficiencies in Grounds 3, 5, and 7.

29. Regarding Grounds 3 and 5, *Yun* teaches using a "conventional trench isolation process" when forming a trench in a semiconductor device. (Ex. 1003, Construction and Operation of the Present Invention, at 2-5). A channel is

"wrapped up with a silicon oxide film SiO_2 and a silicon nitride film SiN" to electrically isolate or insulate the trench in *Yun*. (Ex. 1003, Detailed Description of the Invention, at 1). The conventional trench isolation process taught in *Yun* uses etching of the silicon oxide and nitride films within the trench to create the isolation structure. (Ex. 1003, Abstract). The conventional trench isolation process taught in *Yun* is very commonly used in the industry because it is simple to manufacture and it forms circuits that have a high integration density. Trench isolation was developed as an alternative to the "LOCOS" process (Local Oxidation of Silicon) because it allowed isolation to be maintained while consuming less area and by introducing less surface topography that did LOCOS. As a result it became the standard across the industry.

30. Regarding Ground 7, *Saki* teaches using a conventional trench isolation process to form a "shallow trench isolation structure," similar to that used in *Yun*. (Ex. 1006, 2:55-59). The process uses silicon oxide and silicon nitride film to electrically isolate the shallow trench isolation structure. (Ex. 1006, 4:2-35). *Saki* is generally directed toward improvements to conventional shallow trench isolation structures to prevent the "etching away of the silicon dioxide at the corners" of the isolation structure. (Ex. 1006, 1:25-59). Furthermore, one of the stated goals of *Saki* is to "ha[ve] a small number of steps and therefore contributes to ease of device manufacture and reduced manufacturing costs." (Ex. 1006, 3:18-

21). As discussed above regarding *Yun*, the trench isolation process taught in *Saki* is very commonly used in the industry because it is simple to manufacture and it forms circuits that have a high integration density. The film material in both *Saki* and *Yun* increase electrical isolation of a trench by blocking or increasing the resistance of the shortest physical electrical pathway between the trench and any surrounding conducting structures. As such, the length of the pathway between otherwise adjacent conducting structures is increased, which in turn increases the electrical isolation provided by each trench.

31. In contrast to both *Yun* and *Saki*, *Wada* uses a field-shield device isolation structure with "an improved method for fabricating . . . a buried-type field-shielding device which is fabricated in non-active regions of the LSI circuit." (Ex. 1004, abstract). The process in *Wada* uses the field-shield isolation structure to separate:

> devices by forming a field-shield insulator film and a field-shield electrode between two active regions of a device. By fixing the field-shield electrode potential at a reference potential (e.g., GND or OV), the formation of parasitic channels on the device surface is prevented, thereby providing insulative isolation of the active regions of the devices.

(Ex. 1004, 1:29-38).

32. Wada's improved field-shield insulation structure includes buried field-shield isolation structures that are coplanar with the top surface of the substrate enabling "a higher degree of integration of circuits." (Ex. 1004, 1:64-66).

33. The field-shield electrode 6 of *Wada* is a relatively large structure having a considerable width and depth. *Wada* describes that prior art field-shield isolation structures did not attain the "degree of integration densities required in modern semiconductor devices" because the buried field-shied electrode extended up above the top surface of the semiconductor substrate to form a T-shaped cap on the trench. (Ex. 1004, 1:45-60).

34. One of the ways *Wada* proposed to solve this problem and increase integration was to make the trench deeper than in the prior art field-shield isolation structures, deep enough to contain the entire depth of the field-shield electrode so that the "top of the filed-shield electrode is coplanar (i.e. level) with the upper surface of the substrate 7." (Ex. 1004, 4:24-29). As a result, "the field-shield electrodes do not protrude out on the upper surface 7 of the substrate 7 as in the T-shaped electrode in conventional devices, and the top surface of the field shield electrode 6 is level with the surface of the substrate 7. (Ex. 1004, 6:9-22).

35. *Wada* teaches that this resulting coplanar field-shield electrode achieves the desired increased integration:

> [Because the field-shield electrode 6 is level with the surface of the substrate 7, it] follows that the surface area required for the isolation structure 11 needs to be only as large as the width dimension of the trench 12, thereby significantly reducing the area for the non-active region 10 compared with that required for conventional devices. Therefore, it is obvious that the configuration of the FSDI structure 11 will result in achieving a higher device integration in a given space of a wafer, thus enabling to provide further densification of the highly integrated MOSLSI devices.

(Ex. 1004, 6:9-22).

36. Unlike *Wada*, *Yun* and *Saki* do not feature a field-shield buried electrode, and they instead rely only on silicon oxide and silicon nitride films to insulate trenches, as discussed above. *Wada's* teaching of using a deeper trench to allow a field-shield buried electrode to be coplanar with the top of the substrate is thus inapplicable to *Yun* and *Saki*, which have no buried electrode. In fact, *Wada* explicitly distinguishes its field-shield isolation structure from the typical isolation method of "forming thick oxide films on selected local areas" as taught in *Yun* and *Saki*. (Ex. 1004, 1:15-24). The trench utilized in the buried field-shield isolation structure of *Wada* is designed to allow for a width dimension and a "depth dimension [that] is deeper than a diffusion distance of dopant species associated with a device of the plurality of devices." (Ex. 1004, 2:11-14). The width and

depth of the isolation structure as taught in *Wada* are thus based on buried electrodes within the isolated trench region and would only be applicable and desirable when using a field-shield isolation process. As explained above, neither *Yun* nor *Saki* suggest using a field-shield isolation process, and in fact, the increased manufacturing difficulty provides significant motivation to avoid a field-shield isolation process like the one taught in *Wada*.

37. Furthermore, while Petitioner does not currently argue that *Yun* and *Saki* have electrodes or that it would have been obvious to use the field-shield electrode of *Wada* in *Yun* or *Saki*, it is worth noting that any such combination would not have been obvious given the drastically different structures between the conventional trench structure in *Yun* and *Saki* and the field-shield trench structure in *Wada*.

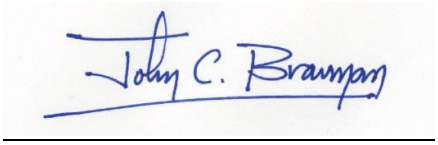
38. In that it includes both conducting and insulating structures, the field-shield isolation structure in *Wada* is significantly different from and more complex than the conventional isolation structures in both *Yun* and *Saki*. While a field-shield isolation structure can provide "a higher degree of integration of circuits," manufacturing is more complicated and time consuming than the convention approach used in both *Yun* and *Saki*. (Ex. 1004, 1:64-66). In fact, the increased complexity has limited the use of field-shield isolation structures in the field, and it

is generally more common for devices to use the conventional trench isolation processes in *Yun* and *Saki* than the field-shield isolation process of *Wada*.

39. A POSITA would thus not modify the teachings of *Yun* or *Saki* with the teachings of Wada because the depth taught in Wada is irrelevant to both Yun and Saki and because of the increased complexity involved in Wada. Any benefits achieved from the methods of *Wada*, such as reducing the surface area for the isolation structure or simplifying the processing required to form the isolation structure, are limited to forming field-shield isolation structures and would not be applicable to the conventional isolation processes of *Yun* and *Saki*. It would thus never occur to a POSITA to look to a reference like *Wada* when considering trench **dimensions** for conventional isolation trench structures, like those taught in *Yun* and *Saki*.

I declare that all statements made herein of my knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code.

Executed on March 23, 2021



By: John C. Bravman, Ph.D.