UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE PATENT TRIAL AND APPEAL BOARD
SMIC, AMERICAS,
Petitioner,
v.
INNOVATIVE FOUNDRY TECHNOLOGIES, LLC, Patent Owner.
Case No. IPR2020-01003
U.S. Patent No. 6,580,122

PATENT OWNER'S PRELIMINARY RESPONSE PURSUANT TO 37 C.F.R. § 42.107(a)

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2003	Ordering Setting Markman Hearing (ECF057)		
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I. Summary Of Arguments

For at least the following reasons, SMIC, Americas' ("SMIC") Petition fails to establish the required likelihood that it will prove that challenged claims 1-3, 5-14, 16-25, and 27-34 of Innovative Foundry Technologies LLC's ("IFT") U.S. Patent No. 6,580,122 are unpatentable.

The Board should deny the Petition for *inter partes* review of Patent Owner IFT's U.S. Patent No. 6,580,122.

As an initial matter, to simplify these proceedings, IFT has disclaimed claims 1-3, 6-14, 17-25, and 28-34. Accordingly, the requested IPR may not be instituted based on these claims because, under 37 C.F.R. § 42.107(e), "no *inter partes* review will be instituted based on disclaimed claims."

As to the remaining challenged claims 5, 16, and 27, the Board should deny the Petition for at least two independent reasons:

(1) The Petition's asserted invalidity Grounds will be resolved in a parallel district court trial **three months before** the Board's deadline for a final written decision in the requested IPR, and the Board should therefor deny

- institution under 35 U.S.C. § 314 (a) and PTAB's Precedential-designated *NKH* and *Fintiv* decisions.¹
- (2) The Petition fails to establish the required reasonable likelihood of success of proving any of the challenged claims 5, 16, and 27 unpatentable under any asserted Ground.

Section 314(a): Although the Petition was filed in the name of "SMIC, Americas," the Petition concedes that the real parties-in-interest are its parent and sister corporations that were sued by IFT for infringement of the '122 Patent in the District Court for the Western District of Texas (the "RPI Petitioners"). (Petition, 1-3).

In that pending parallel district court proceeding, the RPI Petitioners have raised the same invalidity defenses presented in their Petition here, and the Western District of Texas Court has scheduled and will complete its trial on those defenses (and other issues) three months before the final written decision deadline in the requested IPR.

In light of this earlier trial date to resolve the same issues as those presented by the Petition, all six *Fintiv* factors weigh in favor of denying the present Petition

¹ NHK Spring Co., Ltd. V. Intri-Plex Techs., Inc., IPR2018-00752, Paper 8, 20 (PTAB Sept. 12, 2018) (precedential); Apple Inc., v. Fintiv, Inc., IPR2020-00019, Paper 11 (PTAB May 13, 2020) (precedential)

to serve "the efficiency and integrity of the system." The Petition's cursory attempt at addressing *Fintiv* does not establish otherwise; it ignores most of the *Fintiv* factors and is instead based on misstatements concerning the Court's trial date and claim construction. But contrary to the Petition, the parties have in fact agreed to, and the Court has ordered, a trial date **three months before** the FWD deadline in this requested IPR. And also contrary to the Petition, the claim construction proceedings have in fact proceeded according to schedule and the Court will issue its claim construction order in two days, nearly three months **before** the institution decision deadline for this Petition. Therefore, the Board should follow its precedent set in *NHK* and *Fintiv* and deny the Petition under 35 U.S.C. § 314(a).

No Reasonable Likelihood of Success: The Petition's failure to show the required reasonable likelihood of success provides another independent reason for denying institution. In light of IFT's disclaimer of challenged claims 1-3, 6-14, 17-25, and 28-34, the only remaining Grounds are:

- Ground 3 against challenged claims 5 and 27;
- Ground 5 against challenged claim 16; and
- Ground 7 against challenged claims 5, 16, and 27.

As to these remaining Grounds, challenged claims 5, 16, and 27 all require (among other things) the recessed isolation structured formed in a trench "having a width ranging from approximately 2000-3000 Å and a depth ranging from

approximately 4000-5000 Å." The Petition concedes that *Yun* (the primary reference in Ground 3 and 5) and *Saki* (the primary reference in Ground 7) do not teach the width and depth dimensions, and instead attempts to reply on secondary reference *Wada* to cure these deficiencies in all the remaining Grounds. But the Petition's asserted basis for combining *Wada* with these references is wrong and unsupported. *Wada*'s teaching of fabrication of "field-shield device isolation structure" is a completely different type of isolation structure from the "isolation region" disclosed in *Yun* or "shallow trench isolation" taught in *Saki*. The Petition thus identifies no evidence supporting its proposed combination of *Wada* with *Yun* and *Saki*, and its remaining Grounds 3, 5, and 7 based on those combinations necessarily fail.

For each and all of the foregoing reasons, the Board should deny the Petition.

II. Inter Partes Review Cannot Be Instituted Against Disclaimed Claims 1-3, 6-14, 17-25, and 28-34

Pursuant to 37 C.F.R. § 42.107(e), a patent owner may file a statutory disclaimer under 35 U.S.C. § 253 (a), disclaiming one or more claims in a patent. "No *inter partes* review will be instituted based on disclaimed claims." 37 C.F.R. § 42.107(e).

Solely to streamline and expedite this proceeding, patent owner IFT has disclaimed challenged claims 1-3, 6-14, 17-25, and 28-34 of the '122 Patent. (*See* Ex. 2001, Disclaimer in Patent Under 37 C.F.R. 1.321). Therefore, under 37 C.F.R.

§ 42.107(e), the Board should not institute *inter partes* review against or based on those disclaimed claims.

In making this disclaimer, IFT has made no admissions concerning the validity of claims 1-3, 6-14, 17-25, and 28-34 or any other claims. No adverse inferences shall result from the disclaimer, and the disclaimer shall have no effect on other patent claims. *See, e.g., Anchor Wall Sys., v. Rockwood Retaining Walls, Inc.*, No. 99-1356, 2007 U.S. Dist. LEXIS 80583 at *3 (D. Minn. Oct. 30, 2007); 77 Fed. Reg. 48, 764 (Aug 14, 2012).

Moreover, in making this disclaimer, IFT is not requesting an adverse judgment against it. For example, pursuant to 37 C.F.R. § 42.73(b),² IFT is not disclaiming the '122 Patent and there remain non-disclaimed '122 Patent claims challenged in the Petition, specifically challenged claims 5, 16 and 27.

III. The Board Should Deny Institution Because the Parties Are Scheduled to Try the Validity of the Challenged Patent in a District Court Jury Trial Before The Requested IPR Would Conclude

The Board should deny institution on those remaining challenged claims 5, 16 and 27 under § 314(a) and PTAB's Precedent-designated *NHK* and *Fintiv* decisions because IFT and the RPI Petitioners are scheduled to try the validity of the

²An adverse judgment under 37 C.F.R. § 42.73(b) also is inapplicable and inappropriate here because, for example, the disclaimer was made prior to any institution decision and any IPR "trial."

challenged patent in a district court jury trial three months before the deadline for a Final Written Decision in the requested IPR.

In PTAB's precedential *NHK* and *Fintiv* decisions, it:

- recognized that it is inefficient and wasteful for PTAB to institute and conduct an IPR trial if the parties are already scheduled to litigate the validity of the challenged patent in an Article III district court trial set to conclude prior to the deadline for a FWD in the requested IPR; and
- therefore exercised its discretion under 35 U.S.C. § 314(a) to deny the Petitions and avoid such inefficiencies and waste.

NHK, Paper 8 at 20; *Fintiv*, Paper 11 at 3-6, Paper 15 at 7-8, 17.

As the Board stated in *Fintiv*, "NHK applies to the situation where the district court has set a trial date to occur earlier than the Board's deadline to issue a final written decision in an instituted proceeding." *Fintiv*, Paper 11, 3. That is exactly the situation here – RPI Petitioners and Patent Owner are scheduled to try the Petition's invalidity claims in a district court jury trial scheduled three months **before** the Board's deadline to issue a Final Written Decision in the requested IPR.

Fintiv also identified the following six factors that a Board should balance when determining to deny institution under 35 U.S.C § 314(a) "and NHK due to an earlier trial date:"

- 1. whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted;
- 2. proximity of the court's trial date to the Board's projected statutory deadline for a final written decision;
- 3. investment in the parallel proceedings by the court and the parties;
- 4. overlap between issues raised in the petition and in the parallel proceeding;
- 5. whether the petitioner and the defendant in the parallel proceeding are the same party; and
- 6. other circumstances that impact the Board's exercise of discretion, including the merits.

Fintiv, Paper 11, 4-5.

As established in Section B below, all six factors weigh in favor of denying the present Petition to serve "the efficiency and integrity of the system." The Petition does not present any evidence to the contrary. Indeed, the Petition does not even mention or attempt to distinguish *NHK*, nor does the Petition address all of the *Fintiv* factors. (Pet. at 8-10). Instead, the Petition relies largely on misstatements concerning the trial date and the status of claim construction in the parallel district court proceedings. (Pet. at 8-10).

A. The Parallel District Court Proceeding Between The Parties Is Scheduled For Trial Three Months Before The Final Written Decision Deadline

The RPI Petitioners are challenging the validity of the '122 Patent in a parallel district court action pending between them and Patent Owner IFT in the District

Court for the Western District of Texas: *Innovative Foundry Technologies LLC*, v. *SMIC et. al*, No. 6:19-cv-00719-ADA (the "Parallel Proceeding").

In the Parallel Proceeding, RPI Petitioners have raised the same invalidity defenses presented in their Petition here, and the Western District of Texas Court has scheduled the trial on those (and other issues) for September 2021. (Ex. 2002, Scheduling Order (ECF044); Ex. 2003, Ordering Setting *Markman* Hearing (ECF057)). This is three months before any final written decision is due in the requested IPR. Moreover, the Western District of Texas has not expressed any intent to stay this trial date, and the Petition does not argue otherwise. To the contrary, as discussed below when applying the six *Fintiv* factors, the Western District's established guidelines confirm that it typically does <u>not</u> enter a stay under the present circumstances.

To this end, by the Board's December 16, 2020 institution decision deadline for the Petition, the Parallel Proceeding will be well underway. For example, the parties have already exchanged their initial infringement and invalidity contentions, initial document productions, completed all claim construction briefing, completed all claim construction discovery, including expert deposition, completed briefing on motions to dismiss, and completed briefing on summary judgment motions. (Ex. 2002, Scheduling Order (ECF044); Ex. 2004, Proposed Scheduling Order (ECF 64); Ex. 2010, Order Re Disputed Deadlines & Scheduling (ECF 71); Ex. 2005, Case

Docket Sheet, 6-19-cv-00719). And, before the December 16, 2020 institution deadline:

- the District Court and the parties will have already conducted the *Markman* claim construction hearing;
- the Court will have issued its claim constructions;³ and
- the parties will be in the midst of fact discovery.

(Ex. 2002, Scheduling Order (ECF044)).

Thus, the circumstances here are materially the same as those in *NHK* and *Fintiv. NHK Spring Co., Ltd. V. Intri-Plex Techs., Inc.*, IPR2018-00752, Paper 8, 20 (PTAB Sept. 12, 2018); *Apple Inc., v. Fintiv, Inc.*, IPR2020-00019, Paper 15 (PTAB May 13, 2020). In each of those precedential decisions, the Board denied institutions under 35 U.S.C. § 314(a) where, as here, the district court action was set to be tried before the IPR's final written decision would have been issued, and the petitioner had raised substantially the same prior art and arguments in both proceedings.

³ Judge Albright is the presiding judge in the Parallel Proceeding and his stated practice is to issue claim constructions from the bench at the conclusion of the *Markman* hearing. (Ex. 2006, Claim Construction Order, 1:20-cv-00351-ADA; Ex. 2007, Claim Construction Order, 6:19-cv-00532-ADA; Ex. 2008, Claim Construction Order, 6:18-cv-00308-ADA).

B. All Six *Fintiv* Factors Weigh in Favor of the Board Denying Institution

Fintiv reiterated and confirmed the PTAB's earlier identification of the six factors that a Board should consider when determining "whether efficiency, fairness, and the merits support the exercise of authority to deny institution in view of an earlier trial date in the parallel proceeding." Fintiv, Paper 11, 506. The Fintiv decision also noted that "in evaluating the factors, the Board takes a holistic view." Here, however, the Board need not consider whether some factors are more important than others because all six Fintiv factors confirm that the Board should deny institution. The Petition reaches its conclusion that Fintiv factors weigh against discretionary denial without address all six factors or NHK. As discussed below, all of the Fintiv factors, both individually and as a whole, weigh in favor of the Board denying the Petition

1. "whether the court granted a stay or evidence exists that one may be granted if a proceeding is instituted"

Factor one favors denying the Petition in light of the earlier-scheduled district court trial. The Petition does not dispute that this factor weighs in factor of denying institution under 35 U.S.C. § 314(a), *Fintiv*, and *NHK*. In fact, despite referring generally to the *Fintiv* factors, the Petition does not even address or acknowledge this factor. (Pet. at 8-10).

This factor poses two questions, and the answers to those questions indisputably favor denial. First, has the Court "granted a stay"? No, it has not, and Petitioners do not argue or present evidence otherwise. Second, does "evidence exist[] that one may be granted if [the IPR] proceeding is instituted"? No, there does not, and Petitioners do not even try to identify any. Therefore, this factor fully and heavily weighs against institution.

And Petitioners could not reasonably argue that a stay would be likely because the test applied by the District Court for the Western District of Texas establishes that the Court typically does not stay trials in these circumstances, even if an IPR were instituted. The Court and presiding Judge considers three questions to assess stay requests in view of an *inter partes* review: (1) whether the stay will unduly prejudice the nonmoving party, (2) whether the case is in an advanced stage, and (3) whether a stay will likely result in simplifying the case. (*See e.g.*, Ex. 2009, Order Denying Motion to Stay Pending *Inter Partes* Review, *Multimedia Content Management v. Dish Network*, Civil No. 6:18-CV-00207 at 2 (W.D. Tex. May 30, 2019) (J. Albright) ("*Multimedia*").) All three factors confirm that the Court likely will not stay the Parallel Proceeding.

For question (1), the Court and presiding Judge have held that this question weighs against a stay where, as here, the trial date is scheduled before an anticipated final written decision. (*Id.* at 4).

Question (2)—whether the action is in an advanced stage—also weighs against any future stay. For example, the parties have already exchanged their initial infringement and invalidity contentions and their initial document productions, and they also have already completed claim construction briefing and discovery. In addition, before the December 16, 2020 institution deadline, the Court will have held its *Markman* hearing and issued its claim constructions, and the parties will be in the midst of fact discovery. (Ex. 2002, Scheduling Order (ECF044); Ex. 2004, ECF064 Proposed Scheduling Order; Ex. 2010, ECF071 Order Re Disputed Deadlines & Scheduling).

Finally, for question (3), there is no argument or evidence that a stay will likely result in simplifying the case. The Board would not issue a final written decision (and certainly, any appeal thereon would not be completed) prior to the earlier district court trial. Therefore, the requested IPR will not simplify that trial, which will need to address <u>all</u> outstanding issues, including the invalidity defenses raised by RPI Petitioners in both this Petition and the Western District of Texas.

Thus, all of the evidence shows that, under the applicable test, the Court is **not** likely to stay the prior scheduled trial in favor of an instituted IPR. Indeed, to date, Judge Albright has denied **every** opposed motion to stay pending proceedings in his

court pending resolution of an instituted IPR.⁴ Therefore, this factor heavily weighs against institution.

2. "proximity of the court's trial date to the Board's projected statutory deadline for a final written decision"

In *Fintiv*, the Board found that this factor weighed in favor of denying institution because the Parallel Proceeding trial was scheduled to begin two months before the final written decision was due. *Apple Inc.*, *v. Fintiv*, *Inc.*, IPR2020-00019, Paper 15 at 13 (PTAB May 13, 2020). This factor thus weighs against institution because the trial date in the Parallel Proceeding is set for three months before the Final Written Decision deadline for the requested IPR, one more month than in *Fintiv*.

In an attempt to avoid the effect of this earlier trial date, the Petition represents that "a trial date has not yet been set and an announcement of a trial date is not expected soon." (Pet. at 8-9). This representation is simply not true.⁵

⁴ Based on Patent Owner's research, Judge Albright has denied every opposed motion to stay he has ruled on. *See* Ex. 2009, Order Denying Motion to Stay Pending *Inter Partes* Review, *Multimedia Content Mgmt v. Dish Network*, Civil Case No. 6:18-CV-00207 (W.D. Tex. May 30, 2019); Ex. 2011, Excerpt of Case Docket Sheet, 6-19-cv-00514-ADA; Ex. 2012, Excerpt of Case Docket Sheet, 6-19-cv-00515-ADA; Ex. 2013, Excerpt of Case Docket Sheet, 7-18-cv-00147-ADA.

⁵ Petitioners' unsupported speculation that "the escalating pandemic adds uncertainty in the timing of the proceedings" is likewise baseless. Judge Albright has already confirmed, and the parties have agreed, that the Parallel Proceeding will proceed as scheduled despite the ongoing pandemic. (Ex. 2002, Scheduling Order (ECF044); Ex. 2004, ECF064 Proposed Scheduling Order; Ex. 2010, ECF071 Order

The Court's initial "Order Governing Proceedings" set a default trial date of September 17, 2021 and ordered the parties in the Parallel Proceeding to "discuss whether they believe the Court's default Scheduling Order [is] appropriate for this case" and then "submit an agreed Scheduling Order." (Ex. 2002, Scheduling Order (ECF044) at 2). As Petitioners⁶ knew when they filed their June 9, 2020 Petition (but failed to inform the Board), the parties (including the RPI Petitioners here) met and then submitted an April 4, 2020 "Joint Motion For Entry Of Scheduling Order," in which they agreed to a trial date September 17, 2021 and requested that the Court enter a scheduling order adopting that trial date. (Ex. 2004, ECF064 Proposed Scheduling Order at 15). On May 7, 2020, the Court granted the parties' Joint Motion for Entry of Scheduling Order, thereby adopting and ordering the parties' agreed trial date. (Ex. 2010, ECF071 Order Re Disputed Deadlines & Scheduling). The parties have thus agreed to, and the Court has ordered, a trial date of September 17, 2021, three months before any Final Written Decision deadline.

Re Disputed Deadlines & Scheduling).

⁶ "Petitioners" are the named Petitioner SMIC, Americas and the admitted real parties-in-interest Petitioners, which are its parent and sister companies who are the defendants in the Parallel proceeding.

3. "investment in the parallel proceeding by the court and the parties"

Also baseless are the Petition's assertions (without evidence or support) that the Parallel Proceeding is in its "early stages" and "it is unclear whether the Court will have issued its claim construction order by the institution deadline." (Pet. at 8-9). To the contrary, by the time the Board issues its decision on institution, the parties and the Court will have already expended considerable resources in advancing the Parallel Proceeding, including the Court issuing it claim construction order as scheduled. Therefore, this factor too weighs in favor of denial.

The PTAB's precedential *Fintiv* opinion does not limit Factor 3 to invalidity, but instead states that the Board should broadly consider the "investment in the parallel proceeding by the Court and the parties." *Fintiv*, Paper 11 at 6, 9-12. *Fintiv* does not limit the relevant investments to invalidity, but explains that "more work completed by the parties and court in the parallel proceeding tends to support the arguments that the parallel proceeding is more advanced, a stay may be less likely, and instituting would lead to duplicative costs." *Fintiv*, Paper 11 at 10. One example of an investment that *Fintiv* identifies as favoring denial under this factor is claim construction. *Fintiv*, Paper 11 at 10. This alone means this factor weighs in favor of denial here because the parties have already completed all claim construction discovery and briefing, and, by the time the Board issues its institution decision, the

Court will have already held its *Markman* hearing and issued its claim construction order. Indeed, the Court confirmed last week that the *Markman* hearing is proceeding as scheduled on Friday, September 18, 2020, just two days after the filing of this POPR. (Ex. 2014). Moreover, contrary to Petitioners' claimed uncertainty concerning when the Court will issue its claim constructions, the Court's stated and consistent practice is to issue claim constructions from the bench at the conclusion of the *Markman* hearing. (Ex. 2006, Claim Construction Order, 1:20-cv-00351-ADA; Ex. 2007, Claim Construction Order, 6:19-cv-00532-ADA; Ex. 2008, Claim Construction Order, 6:18-cv-00308-ADA). Thus, the Court will issue its claim constructions in just a few days at the September 18, 2020 hearing, roughly three months before the institution deadline in this manner. This alone means that this factor weighs heavily against institution.

And the Petition's conclusory assertion that the Parallel Proceedings is in its early stages not only ignores that claim construction briefing, discovery, and rulings will all be completed before any institution decision, it also ignores all of the other time and resources the parties and Court have already spent in the Parallel Proceeding and will continue to do so prior to and beyond the Board's institution decision deadline. For example, by that date, the parties will already have: exchanged their initial infringement and invalidity contentions, made their initial document productions, completed briefing on motions to dismiss, and completed

briefing on summary judgment motions, and have conducted several months of full fact discovery. (Ex. 2002, Scheduling Order (ECF044); Ex. 2004, Proposed Scheduling Order (ECF 64); Ex. 2010, Order Re Disputed Deadlines & Scheduling (ECF 71); Ex. 2005, Case Docket Sheet, 6-19-cv-00719). Moreover, before any Final Written Decision in the requested IPR, the Court and the parties will have already expended the time, money, and resources necessary to completely litigate and conduct a jury trial on the entire parallel litigation—including all invalidity issues.

For any and all of these reasons, instituting would lead to duplicative costs and this factor weighs against institution.

4. "overlap between issues raised in the petition and in the parallel proceeding"

Factor four also weighs in favor of denying institution because there is almost complete overlap between the invalidity issues raised in the remaining Grounds of the Petition and in the Parallel Proceeding in the Western District of Texas. Specifically, RPI Petitioners are asserting the substantively the same prior art references against the same exact claims in the Parallel Proceeding as they are in the remaining Grounds.

In light of IFT's disclaimer of claims, the only remaining Petition Grounds are Grounds 3, 5, and 7 against claims 5, 16, and 27. Two of these Grounds (Grounds

3 and 7) are identical to RPI Petitioners' invalidity contentions in the Parallel Proceedings. Specifically, in both the Parallel Proceedings and the Petition's Grounds 3 and 7, the RPI Petitioners assert that challenged claims 5, 16, and 26 are obvious over *Yun* and *Saki* in light of *Wada*. (Ex. 2015, Ex. A-1 of Dfts Invalidity Contentions; Ex. 2016, Ex. A-2 of Dfts Invalidity Contentions).

The references asserted in remaining Ground 5 are substantively identical to those asserted the RPI Petitioners' invalidity defenses in the Parallel Proceedings. Ground 5 asserts that claim 16 is obvious over Yun in light of Wada and Lu, relying on secondary reference Lu solely for disclosing that a gate electrode may be made of polysilicon. (E.g., Pet. at 57). In the Parallel Proceedings, the RPI Petitioners also rely on Yun and Wada as making claim 16 obvious, but rely on a numerous other references (rather than the Petition's secondary reference Lu) as teaching that a gate electrode may be made of polysilicon, ostensibly so that they can argue in the Petition that "the prior art in this Petition and the Parallel Proceeding do not overlap completely." (Pet. at 9 (emphasis added); Ex. 2015, Ex. A-1 of Dfts Invalidity Contentions; Ex. 2016, Ex. A-2 of Dfts Invalidity Contentions (relying on Tao (U.S. Pat. No. 6,037,266) as including a polysilicon gate electrode yet also identifying Pey (U.S. Pat. No. 6,180,501), Rubin (U.S. Pat. No. 6,429,062), and Perera (U.S. Pat. No. 5,786,263), which teach a polysilicon gate electrode)).

Petitioners' transparent attempt to (superficially) avoid complete identity does not somehow tip this factor towards institution. The references at issue in the Grounds and in the Parallel Proceeding are all identical except for Ground 5's secondary reference Lu, which is (according to RPI Petitioners' own assertions) substantively duplicative and cumulative of the secondary references raised in the Parallel Proceeding. RPI Petitioners identified no substantive difference between their Grounds and their invalidity contentions in the Parallel Proceedings. Petitioners' attempt to game the system in this manner should be rejected for the artificial and blatant ploy that it is.

5. "whether the petitioner and the defendant in the parallel proceeding are the same party"

Factor five also weighs in favor of a denial because RPI Petitioners are the defendants in the Parallel Proceeding. Indeed, the Petition does not address this factor or dispute that it favors denial.

For example, the Petition does not argue that the fact that it was filed in the name of "SMIC, Americas" rather than the real parties-in-interests affects this factor. Nor could it reasonably do so because PTAB and its rules regularly protect patent owners from successive challenges to those patents by "the petitioner <u>or real party</u> <u>in interest</u>." *E.g.*, 35 U.S.C. § 315 (a) (emphasis added); *see also*, 35 U.S.C. § 315 (b); *WesternGeco LLC v. ION Geophysical Corp.*, 889 F.3d 1308, 1319 (Fed. Cir.

2018) ("[I]t is important to determine whether the petitioner and the prior litigant's relationship — as it relates to the lawsuit — is sufficiently close that it can be fairly said that the petitioner had a full and fair opportunity to litigate the validity of the patent in that lawsuit. In other cases, it may be more relevant to determine whether the petitioner is simply serving as a proxy to allow another party to litigate the patent validity question that the other party raised in an earlier-filed litigation.").

6. "other circumstances that impact the Board's exercise of discretion, including the merits"

Finally, factor six also confirms that the Board should deny the Petition. As established herein, the Petition's Grounds are particularly weak and do not justify instituting on the merits. But "a full merits analysis is [not] necessary to evaluate this factor" because even "if the merits of the grounds raised in the petition are a closer call, then that fact has favored denying institution when other factors favoring denial are present." *Fintiv*, Paper 11, 15.

Here, the merits do not even present a "closer call" because, as discussed below, the Petition wholly fails to offer **any** basis for combining *Yun* or *Saki* with *Wada* to disclose the width and depth dimensions of the trench, as required for every remaining asserted Ground.

Thus, all of the *Fintiv* factors, both individually and as a whole, weigh in favor of the Board denying the Petition in light of the earlier-scheduled trial date in the Parallel Proceeding. The Petition presents no supported arguments to the contrary.

IV. The Petition Should Be Denied Because It Does Not Establish the Required Reasonable Likelihood Success Of Proving Challenged Claims 5, 16 & 27 Unpatentable

The Petition asserts eight Grounds. But in light of IFT's disclaimer of challenged claims 1-3, 6-14, 17-25, and 28-34, the only remaining Grounds at issue are Grounds 3, 5, and 7 against challenged claims 5, 16, and 27:

Ground	References	Basis	Original	Remaining Non-
			Challenged	Disclaimed,
			Claims	Challenged Claims
1	Yun	35 U.S. C. §	1–2 and 11-12	None
		102		
2	Yun	35 U.S. C. §	3, 23-25, and 33-	None
		103	34	
3	Yun in	35 U.S. C. §	5 and 27	5 and 27
	view of	103		
	Wada			
4	Yun in view	35 U.S. C. §	6-10, 13-14, 17-22	None
	of Lu	103	and 28-32	
5	Yun in	35 U.S. C. §	16	16
	view of	103		
	Wada and			
	Lu			
6	Saki	35 U.S. C. §	1-3, 6, 11-14, 21-	None
		103	25, 28 and 33-34	
7	Saki in	35 U.S. C. §	5, 16, and 27	5, 16, 27
	view of	103		
	Wada			
8	Saki in	35 U.S. C. §	7-10, 17-20 and	None
	view of Lu	103	29-32	

The Petition does not establish the required likelihood of success for any of these Grounds. For example, as established below, the Petition wholly fails to offer **any** basis for combining the asserted references in the manner required by remaining Grounds 3, 5, and 7.

The following sections address:

- the inventions and claims of the '122 Patent, including a primer on basic semiconductor components; and
- the Petition's failure to identify evidence that it was obvious to combine *Wada* with either *Yun* or *Saki* to remedy their admitted failure to teach the "trench . . . depth ranging from approximately 4000-5000 Å" limitation of challenged claims 5, 16, and 27.

A. The '122 Patent

The challenged '122 Patent has a priority date of March 20, 2001, and relates generally to improved semiconductor devices. (Ex. 1001). The following provides background on typical semiconductor devices, some of the drawbacks of prior art manufacturing methods, and how the '122 Patent describes and claims inventive solutions to those problems.

1. Typical Semiconductor Components

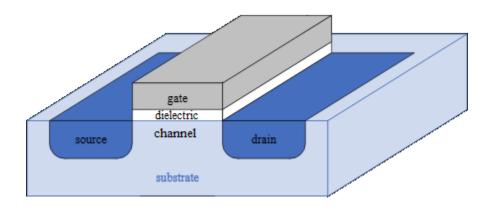
Today's semiconductor devices trace their lineage back to the first computers of the 1940s, which used vacuum tubes to perform two key electrical functions:

switching (*i.e.*, turning electrical current on and off) and amplification (increasing the amplitude of a signal while retaining its electrical characteristics). But where the earlier tubes used a vacuum to control the flow of electrons (turning electrical current on and off), today's semiconductor devices use transistors.

a. A Simple Field Effect Transistor

One type of transistor typically used in semiconductor devices is a "field effect transistor," or FET. Materials used to build such a transistor may be divided into three categories, based on their ability to allow the flow of electrical current: conductors, dielectrics, and semiconductors. In a conductor (such a metal), electric current can flow freely. A dielectric (such as silicon dioxide) is a material at the opposite end of the conductivity spectrum and has a high resistance to the free flow of electrical current. Semiconductors (such as silicon) fall between conductors and dielectrics and have some conducting (and some resisting) ability.

The simplified FET below illustrates how these materials may be used to create a semiconductor device transistor. As shown the transistor is built in and on a semiconductor substrate and comprises a source, a drain, a gate, and a channel.

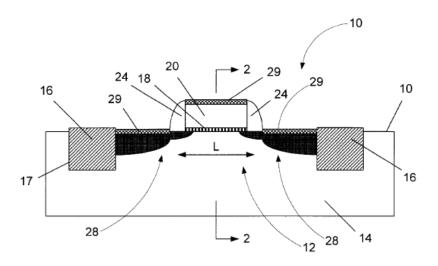


The source and drain are regions in the semiconductor substrate that are either rich in electrons (a negative, or n-type, region) or rich in electron holes (a positive, or p-type, region). The channel is a region under the gate and between the source and drain, and is the opposite type of region from the source and drain. In other words, if the source and drain are n-type regions, then the channel will be a p-type region (and vice versa).

The gate is a conductor (such as metal) located above the channel. In this simplified version of a FET, there is a dielectric between the channel and the gate. When a voltage is applied to the gate, the dielectric prevents the flow of current from the gate to the channel, but the applied voltage results in the creation of a "field effect" in the channel. This "field effect" either builds up or depletes the charges in the channel (depending on whether it is a p- or n-type channel). As a result, the field effect allows electrical current to flow from the source, through the channel, to the drain. Thus, selectively applying voltage to the gate essentially switches the transistor on and off, starting and stopping the flow of electrical current.

b. Isolation Structures

Multiple transistors may be fabricated on the same semiconductor substrate. But as multiple transistors have become tightly packed on the same substrate, it is necessary to electrically isolate adjacent regions of a semiconductor device to prevent issues such as surface leakage currents. One way to isolate these different transistors from each other, is to surround each transistor by an "isolation structure." The '122 Patent Figure 1 illustrates such as an isolation structure below, showing in cross-section an isolation structure 16 that comprises a dielectric (insulating material) and surrounds the transistor 10 to isolate it from other transition the same substrate 14. (Ex. 1001, at Fig. 1, 1:30-61).



2. Drawbacks Of The Prior Art

The '122 Patent describes that a transistor's performance may be improved by increasing the amount of current flowing from the drain to the source, which is known as the "drive current." (Ex. 1001, 1:62-66). The prior art taught that one

way of increasing the drive current is to reduce the gate's length, i.e., the distance across the channel between the source and drain. (Ex. 1001, 2:5:10).

However, this prior art approach suffered from drawbacks. For example, while reducing the gate/channel length increases drive current, it also has the negative effect of increasing off-state leakage current: "all other things being equal, the smaller the channel length, the greater the off-state leakage current." (Ex. 1001, 2:5-10). Moreover, attempts to substantially increase drive current by decreasing the length of the gate/channel exacerbated this leakage problem because "the off-state leakage current increases exponentially as the channel length of the device decreases." (Ex. 1001, 2:10).

3. The '122 Patent's Exemplary Solutions and Embodiment

Because improving drive current by reducing gate/channel length could lead to excessive "off-state leakage currents," the '122 Patent focused on an alternative approach: **increasing** the transistor's **width** rather than **reducing** its **length**. (*E.g.*, Ex. 1001, 2:10-18, 4:13-20). As the '122 Patent describes, increasing the width also increases drive current (similar to reducing the length), but introduces less off-state leakage currents than does a corresponding reduction in length. (Ex. 1001, 2:10-13).

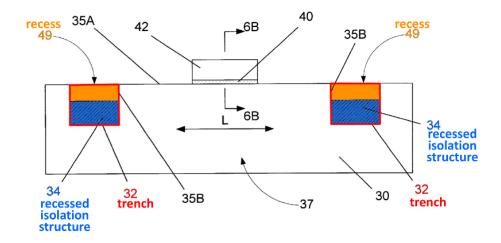
Accordingly, the '122 Patent discloses improved methods for achieving this desired increase in drive current using an increase in gate width. And these improved methods allow not only for an increase in gate width, they do so while

simultaneously (1) accommodating the continued use of recessed isolation structures yet (2) still minimizing the overall footprint of the transistor. (*E.g.*, Ex. 1001, 2:35-38, 4:13-35). To this end, one aspect of the '122 Patent's disclosed approach to increasing the width of the gate while still minimizing the overall area covered by the transistor is to have the width ends of the gate overlap with at least a portion of the recessed isolation structure, thereby increasing the width while minimizing the resultant increase in total area. (Ex. 1001, 5:41-43, 6:62-7:18).

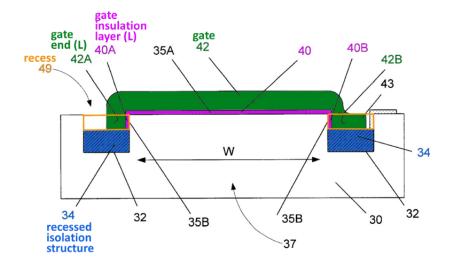
To allow for this configuration, one '122 Patent embodiment describes that a recess (trench 32) is formed within substrate 30. (Ex. 1001, 4:21-22). Then, "[a] recessed isolation material 34, comprised of materials such as silicon oxynitride, etc., is formed in the trench 32" to form the recessed isolation structure. (Ex. 1001, 4:23-25). To achieve the desired isolation while still allowing for maximum gate width in a minimum amount of space, the '122 Patent teaches and claims forming the trench with "a width ranging from approximately 2000-3000 Å and a depth ranging from approximately 4000-5000 Å." (Ex. 1001, claims 5, 16, 27; *see also id.* at 4:27-33).

The Patent further describes that once the recessed isolation structure is formed in a trench with these dimensions, some of the recessed isolation material may then be removed (e.g., etched away) to create another recess above the recessed isolation material: "this process also results in the definition of a recess 49 in the

substrate 30 above the recessed isolation material 34." (Ex. 1001, 4:34-55). Annotated Figure 6A illustrates: (1) trench 32 formed as a recess in substrate 37; (2) recessed isolation structure 34 formed within that recess/trench 32; and (3) the second recess 49 then formed above recessed isolation structure 34. (Ex. 1001, Fig. 6A).



The '122 Patent further describes that (as depicted below in annotated Figure 6B) the width ends of the gate 42 (and the ends of its gate insulation layer 40) may extend into the recess 49 above the recessed isolation structure 34, thereby increasing the gate's width without enlarging the overall footprint of the transistor and its recessed isolation structure. (Ex. 1001, 5:41-43, 6:62-7:18).



4. The Challenged Claims

Consistent with the foregoing, each of challenged claims 5, 16, and 27 is directed to a transistor that includes a gate electrode and recessed isolation structure that defines an upper space into which a portion of the gate may be positioned. (Ex. 1001, claims 1, 5, 13, 16, 23, 27).

For example, independent claims 1 and 13 (from which challenged claims 5 and 16 depend) each describes that the recessed isolation structure defines a recess above it, with a portion of the gate electrode "extending into said recess above said recessed isolation structure." Similarly, independent claim 23 (from which challenged claim 27 depends) describes that the recessed isolation structure defines "an active area having an upper surface and an exposed sidewall surface" and that the gate electrode is "positioned above a portion of said upper surface and a portion of said exposed sidewall surface."

Each of the challenged claims also specifies that the recessed isolation structure must be formed in a trench with specific dimensions, specifically "a trench having a width ranging from approximately 2000–3000 Å and a depth ranging from approximately 4000-5000 Å." (Ex. 1001, claims 5, 16, 27). As established below, this limitation required by every challenged claim is admittedly not taught by the primary references *Yun* and *Saki* and is not obvious in light of the secondary reference *Wada*.

B. <u>Challenged Claims 5, 16, and 27</u>: Grounds 3, 5, and 7 Do Not Identify Evidence Showing That The Admittedly Missing "trench . . . depth ranging from approximately 4000-5000 Å" Limitations Were Obvious

The Petition concedes that none of the asserted primary references teaches forming a recessed isolation structure in a trench having the dimensions required by each of the challenged claims. For example, the Petition concedes that neither *Yun* (the primary reference in both Grounds 3 and 5) nor *Saki* (the primary reference in Ground 7) teaches a "trench . . . depth ranging from approximately 4000-5000 Å" limitation as required by each of claims 5, 16, and 27. (Pet. at 43, 57-58, 78).

Accordingly, Grounds 3, 5, and 7 attempt to rely on secondary reference *Wada* to cure this deficiency. However, the Petition identifies no rationale or evidence supporting the proposed (and necessary) combination of *Wada* with *Yun* and *Saki*.

While *Yun* and *Saki* concern conventional "isolation regions" and "shallow trench isolation," *Wada* is directed to a more complex and specialized area of <u>field-shield device isolation</u>. Because *Yun* and *Saki* do not contemplate a structure that would be applicable to the specialized field-shield application there is no reason to combine *Wada*'s trench structure to the devices taught in *Yun* and *Saki*. Accordingly, Grounds 3, 5, and 7 based on those combinations necessarily fail.

1. Wada's Teachings Are Inapplicable to Yun and Saki

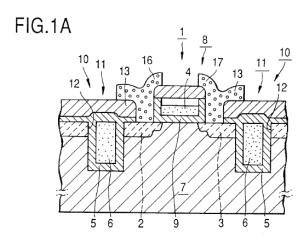
Isolation Structure And Method For Making The Same." (Ex. 1004) (emphasis added). Consistent with this title, *Wada* describes "an improved method for fabricating... a buried-type field-shielding device which is fabricated in non-active regions of the LSI circuit." (Ex. 1004, abstract). Critically, this field-shield isolation structure is materially different from and more complex than the conventional isolation structures used in the primary references *Yun* and *Saki*.

Wada describes that a field-shield isolation structure separates transistor devices by forming a field-shield insulator film and a field-shield electrode between two active regions of a device. By fixing the field-shield electrode potential at a reference potential (e.g., GND or OV), the formation of parasitic channels on the device surface is prevented, thereby providing insulative isolation of the active regions of the devices.

(Ex. 1004, 1:29-38).

The buried field-shield isolation structures that are the subject of *Wada*'s proposed improvements are formed such that a portion of the filed-shield isolation structure extends beyond the trench region, with a "T-shaped cross-section field-shield electrode [that] is exposed on the top surface of the substrate such that the width of the top of the field-shield electrode is wider than the width of the trench." (Ex. 1004, 1:46-52). This undesirable isolation structure meant that valuable surface space on the wafer was occupied with non-active regions for the purpose of device isolation. (Ex. 1004, 1:52-60).

The improved field-shield insulator method disclosed in *Wada* relates to semiconductor devices that includes buried field-shield isolation structures that are coplanar with the top surface of the substrate enabling "a higher degree of integration of circuits." (Ex. 1004, 1:64-66). These field-shield isolation structures include a field-shield insulator film and a field-shield electrode which are each formed within a trench in the semiconductor substrate, as illustrated in *Wada* Figure 1A below. (Ex. 1004, 2:5-10). This structure differs from the typical CMOS fabrication method of "forming thick oxide films on selected local areas" as taught in *Yun* and *Saki*. (Ex. 1004, 1:15-24).



The *Wada* improved method varies substantially from a convention isolation method by utilizing electrodes buried within an isolation region to provide a reference potential between active regions in the semiconductor device. (Ex. 1004, 2:5-10). The *Wada* isolation structure includes a "field-shield insulator film is formed on interior surfaces of a trench cavity whose cavity opening faces an upper surface of the semiconductor substrate . . . and the field-shield electrode is buried in an interior space of the trench cavity lined with the field-shield insulator film." (Ex. 1004, 2:9-17). The trench utilized in the buried field-shield isolation structure is designed to allow for a "depth dimension [that] is deeper than a diffusion distance of dopant species associated with a device of the plurality of devices." (Ex. 1004, 2:11-14).

Another feature of the *Wada* improved method is that this field-shield insulator is able to be formed such that "the trench cavity lined with the field-shield insulator film so that a top surface of the field-shield electrode is **level with the**

upper surface of the semiconductor substrate." (Ex. 1004, 2:15-18). This coplanar top surface of the field-shield electrode is taught as an important feature of this improved method, allowing for "the area required for the device isolation structure is only that area required for the width of the trench cavity . . . compared with the conventional buried-type field-shield device isolation structures." (Ex. 1004, 2:29-35).

In contrast to the teachings of *Wada*, neither *Yun* nor *Suki* teaches, uses, or contemplates the use of an isolation structure that is anything other than conventional, and certainly does not teach the use of a specialized and more complicated field-shield isolation structure. The depth of the isolation structure as taught in *Wada* are based on buried electrodes within the isolation region and add complexity and difficulty to the manufacturing process that would not be necessary or desirable except when used in a field-shield isolation application. Furthermore, the teaching in *Wada* relating to the placement of a field-shield isolation structure's top surface being co-planar with the top surface of the substrate teaches away from combining the isolation structure in *Wada* with *Yun* or *Suki*.

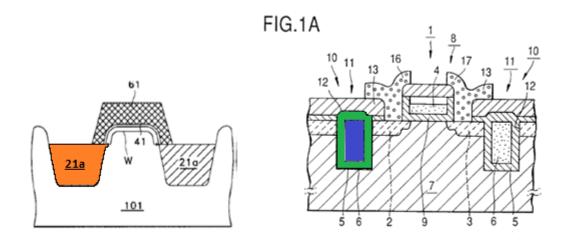
2. Grounds 3 and 5 Do Not Show That The Proposed Combination of *Yun* with *Wada* Was Obvious

Grounds 3 and 5 rely on combining *Wada* with *Yun*, but ignore that it would not be obvious to combine these references and teachings because of the

significantly different and incompatible structures and goals of *Wada* and *Yun*. Indeed, the Petition provides **no explanation** as to why it would be obvious to combine the trench associated with specialized buried field-shield isolation taught in *Wada* with the "**conventional** trench isolation process" taught in *Yun*. (Ex. 1003, Construction and Operation of the Present Invention, at 2-5).

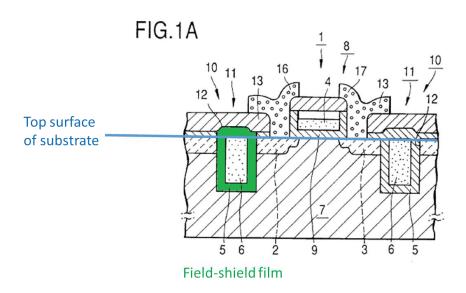
Unable to identify a reason to combine these disparate and incompatible structures, the Petition resorts to simply misstating the teaching in Wada as "reducing the surface area for the isolation structure relative to prior art structures, and simplifying the processing required to form the isolation structure." (Pet., 43-44). But Wada does **not** teach or suggest such a reduction or simplified method for forming the type of conventional trench isolation structures found in Yun; rather, Wada only teaches and suggests only a reduction and simplified method for forming field-shield isolation structures. (Ex. 1004, 6:3-5 ("The method leads to a much simpler and economical production approach to making the buried-type isolation **device** without the use of photolithography.")). The Petition does not assert that Yun features a field-shield isolation structure or that it would have been obvious to use one in Yun instead of a conventional isolation structure. Therefore, the teachings of Wada concerning the materially different and more complex field shield isolation structures is inapplicable to Yun.

The added complexity of the *Wada* isolation structure can be readily seen by comparing the isolation structures in *Yun* and *Wada*. The conventional trench isolation process taught in *Yun* includes a single oxide film material (21a) within the trench to create the isolation structure. (Ex. 1003, Fig. 3 (annotated)). Comparatively, the isolation structure taught in *Wada* requires multiple additional steps and processes to form the isolation structure, including forming a field-shield insulator film (5) and a field-shield electrode (6). (Ex. 1004, Fig. 1A (annotated)).



Furthermore, the "partial etching of a first oxide film inside the trench isolation" taught in *Yun* in not compatible with the buried field-shield isolation structure as taught in *Wada*. While *Wada* does disclose a trench with a depth "measuring 0.5~1.5µm" (5000-15,000 Å) in relation to a buried field-shied isolation structure there is no reason to believe a POSITA would apply those dimensions to a traditional isolation structure. The *Wada* isolation structure teaches a buried

electrode is "coplanar" with the stop surface of the substrate however the isolation structure's field-shield film necessarily extends <u>above</u> the top surface of the substrate, as shown below. (Ex. 1004, 4:27-29; 4:49-52).



(Ex. 1004, Fig. 1A (annotated)). If an etch were to be performed on the *Wada* buried field-shield isolation structure the electrically conductive buried electrode would be exposed allowing for shorts to occur between a gate electrode that extends into the isolation structure and the buried electrode.

For these reasons, the Petition's argument for combining *Yun* and *Wada* were not obvious and Grounds 3 and 5 are unsupported.

3. Ground 7 Does Not Show That The Proposed Combination of *Saki* with *Wada* Was Obvious

Ground's 7 attempt to combine *Wada* with *Saki* fails for similar reasons because the Petition again ignores that it would not be obvious to combine these

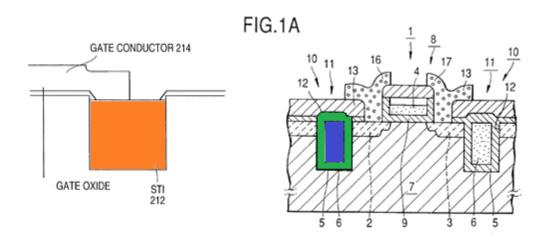
references and teachings because of the significantly different and incompatible structures and goals of *Wada* and *Saki*. Once again, the Petition provides **no explanation** as to why it would be obvious to combine the trench associated with specialized buried field-shield isolation taught in *Wada* with the **conventional** trench isolation process taught in *Saki*.

Unlike *Wada*, the *Saki* reference is generally directed toward improvements to conventional shallow trench isolation structures to prevent the "etching away of the silicon dioxide at the corners" of the isolation structure. (Ex. 1006, 1:25-59). Furthermore, one of the stated goals of *Saki* is to "ha[ve] a small number of steps and therefore contributes to ease of device manufacture and reduced manufacturing costs." (Ex. 1006, 3:18-21).

Unable to identify a reason to combine the disparate and incompatible isolation structures of *Wada* and *Saki*, the Petition again misstates that *Wada* simplifies isolation structures in general. (Petition, at 79). Again, this is incorrect, as the teachings of *Wada* are directed specifically to forming <u>field-shield</u> isolation structures and are not applicable to the conventional trench isolation structure of *Saki*. (Ex. 1004, 6:3-5 ("The method leads to a much simpler and economical production approach to making <u>the buried-type isolation device</u> without the use of photolithography.")). The Petition does not assert that *Saki* features a field-shield isolation structure or that it would have been obvious to use one in *Saki* instead of a

conventional isolation structure. Therefore, the teachings of *Wada* concerning the materially different and more complex field shield isolation structures is inapplicable to *Saki*.

Again, the added complexity of the *Wada* isolation structure can be readily seen by comparing the isolation structures in *Saki* and *Wada*. The conventional trench isolation process taught in *Saki* includes a STI material (212) within the trench to create the isolation structure. (Ex. 1006, Fig. 5(i)). Comparatively, the isolation structure taught in *Wada* requires multiple additional steps and processes to form the isolation structure, including forming a field-shield insulator film (5) and a field-shield electrode (6). (Ex. 1004, Fig. 1A).



The Petition provides no rationale for why the more complicated field-shield isolation structure taught in *Wada* would be obvious to combine with the stated goal of "ha[ving] a small number of steps and therefore contributes to ease of device

manufacture and reduced manufacturing costs" as discussed in *Saki*. For these reasons, the Petition's argument for modifying the *Saki* device to use the *Wada* isolation structure is unsupported and Ground 7 fails.

V. Conclusion

For each and any of the foregoing reasons,⁷ the Board should deny the Petition.

Dated: September 16, 2020 /William A. Meunier/

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⁷ Petitioners cannot somehow cure the foregoing failings in the Petition in some later argument or pleading, because the Supreme Court and the Federal Circuit have confirmed that an IPR cannot proceed or be decided on grounds not included in the initial petition. *SAS Inst., Inc. v. Iancu,* 138 S. Ct. 1348, 1353, 1356 (2018); *Samsung Elecs. Am., Inc. v. Prisua Eng'g Corp.*, No. 2019-1169, 2020 U.S. App. 3292, at *14 (Fed Cir. Feb. 2, 2020); *Koninklijke Phillips N.V. v. Google LLC*, No. 2019-1177,

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner hereby certifies, in reliance on the word count of the word-processing system (Microsoft Office Word 2010) used to prepare this preliminary response, that the number of words in this paper is 8,390. This word count excludes the tables of contents, tables of authorities, certificate of word count, certificate of service, and table of exhibits.

Dated: September 16, 2020 /William A. Meunier/

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CERTIFICATE OF SERVICE

I certify that a copy of Patent Owner's Preliminary Response is being served by electronic mail on the following counsel of record:

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