

714, but may be separate lines as may be appreciated by one with ordinary skill in the art. The bit lines and their complement bit lines connect to sense amplifiers, like 1309, not illustrated in this figure, like those in Fig. 13a, to read the value of the location addressed by the specific word line. The bit line and its complement may be driven to desired values when the operation
5 is to write the specific memory location selected by the word line. The Fig. 7A illustrates multiple word lines for the different memory blocks in a state block. The state block bit may comprise of an optional Mask Word line to address the optional mask memory block. The state block bit may further comprise of another word line, WL2, 705, that is used to address the SDV memory block. Thus three memory locations may be used to represent a state block in the NFA rule block in
10 PRISM. These may be contiguous locations or partitioned differently based on the similarity of the type of information being stored. Thus if an NFA or FSA supports 8 states, there may be 24 memory locations in the PRISM Memory address space that may be used to represent the memory in the state blocks. Further the NFA accept vector, start vector and optionally the tag vectors may occupy a location each in the memory space. The NFA state vector may also
15 optionally use up another location, not illustrated, in the PRISM memory space. Thus an 8-state NFA or FSA may use 28 to 30 memory address locations to store the related information of the FSA. If the symbols are wider for example when symbols are 16-bits, and the FSA states are 8, the organization of the PRISM memory may be done slightly differently, not illustrated, to maintain the modular arrays as may be appreciated by one with ordinary skill in the art. The
20 symbols may be used to occupy more than one address location addressed by separate word lines or may occupy a wider word if a single word line is used. Using the appropriate addressing and read, write operations of the memory, the PRISM NFA rule blocks may be programmed and dynamically reconfigure the realized regular expressions.

The symbol evaluate circuit, 711, generates a signal, RSx and/or CAM matchx, 704, which is
25 used to indicate when the input character matches the programmed symbol. The content symbol or character to be examined with the programmed symbol, is presented to the state block bit on the content bit lines CL, 740, and complement bit line CLn, 715 which are coupled to the symbol evaluate circuit. The symbol evaluate circuit further couples to the mask memory block bit and the symbol memory block bit through the mask circuit, 710, and evaluates if the
30 content bit presented to this state block bit matches with the programmed symbol bit. The output of the symbol evaluate circuit is the RSx / CAM matchx signal 704, which is coupled between multiple symbol evaluate circuits of all state block bits of a state block, and is asserted when all the bits of the symbol programmed in the state block match their corresponding symbol bits of

the input content to being examined. The figure illustrates separate bit lines and their complement lines for content and mask and other programming information illustrated by the lines, 740 and 707 or 714 and 715. Those with ordinary skill in the art can appreciate that the positive and complement bit lines may each be on the same signal or may each be on a separate signals. Thus all variations of these implementations are covered by the teachings of this patent. The bit lines used to store and retrieve the information to memory elements may optionally be separate from the content lines, as illustrated in the Fig. 7A for various reasons, like performance, interconnect load, die size, cost, power and the like.

Fig. 8A illustrates symbol logic bit in PRISM. This figure illustrates the circuit detail for the symbol logic, 703, of the state block bit illustrated in Fig. 7A. This figure illustrates the BL(bit line), CL (content bit line) and ML (mask bit lines) sharing the same signal as described above as a memory design choice. They may each be separate as discussed earlier, in which case the connectivity will be different to the appropriate elements of the symbol logic bit. The symbol logic bit illustrates a realization using static memory architecture for the memory bits. The transistors, 810, 825, 826, 827, 828, and 829 form a typical six transistor static memory cell which are coupled to the bit line using the line 806, and the complement of the bit line by the line 824. The transistors, 825 and 827, may optionally comprise of p-channel metal oxide semiconductor (PMOS) field effect transistor (FET) device in a complementary metal-oxide semiconductor (CMOS) process technology, while the transistors, 810, 826, 828, 829, may optionally comprise of the n-channel metal oxide semiconductor (NMOS) field effect transistor (FET) devices. These six transistors coupled together as illustrated in the Fig. 8A form a static memory cell. Memory cells comprised of other transistor devices in other process technologies like SiGe, Bipolar or the like providing similar functionality as those in this patent are all within the scope and spirit of the teachings of this patent as may be appreciated by those with ordinary skill in the art. The transistors 825, 826, 827 and 828 are setup as back to back inverters which are written to from the BL, 802, and BLn, 805, coupled to transistors 810 and 829 respectively, when word line WL, 801 is selected which activates the devices 810 and 829 and when the BL and BLn are driven by the bit line drivers with the logic value and its complement to be stored in the memory cell. This memory cell stores a symbol bit. If a logic value '1' needs to be stored, the BL is driven by '1' and BLn by '0'. If the WL is active then the logic value gets stored in the symbol memory bit. When the symbol memory bit needs to be read the BL and BLn may not be driven actively other than pre-charging. The sense amplifiers attached to the bit lines may then detect the differential in the voltage swing on BL and BLn to read the symbol memory bit. The

transistors, 812, 814, 815, 816, 817 and 818 form a similar six transistor memory cell as above, where the transistors 814 and 816 may optionally be of PMOS type, while the others may optionally be of NMOS type, for storing the symbol mask bit, which is accessed by selecting mask word line (MWL), line 803. This memory location is used to store the symbol mask bit. The

5 symbol mask bit when set enables the symbol evaluation and disables the evaluation when the mask bit is disabled. Reverse setup is also feasible, except the connectivity between the symbol memory cell and the mask memory cell would need to be changed appropriately. The device pairs 808, 809 and 821, 822 are coupled to the symbol bit, mask bit and content line, 802, and form a XOR functionality by coupling with the RSx/CAM Match x pre-charged line 804. This line

10 804, is shared between adjoining symbol logic bits of a NFA or FSA rule block. This line is pulled low, if any of the bit pairs of the content and the symbol do not match, assuming the bit is enabled using the optional mask bit. The line stays high only if all the bits of the symbol match all content bits. The mask bit is coupled to devices 808 and 809 by the signal 813. Alternatively, the mask bit signal 813a, may be coupled to another n-transistor, not illustrated, which would

15 couple to device 808 and 821 on its drain and to ground value on its source, thereby providing a similar masking functionality described below. When the mask bit is set, device 815, is turned-on which enables the path from devices 808 and 809, when the content value on CL, 802, coupled to device 809, is '1' and when the symbol bit value is '0', a value of '1' is coupled to 808 by signal 811 which enables the path from the RSx/CAM Match x, line 804, to ground, GND,

20 This causes the match signal 804 to be pulled-down or low indicating a mismatch. Similarly the transistors 821 and 822, provide are enabled when the symbol bit value is '1' and the content value is '0', coupled to device 822 through CLn, 805, which carries the complement of the content value, forming a XOR function on the RSx or CAM Match x signal, line 804. Thus, the match signal, 804, stays high or active only when all the bits of the symbol and the content input

25 match respectively. Though the symbol evaluation illustrated is a compare operation, other operations like range detect, or other ALU operations may be implemented with appropriate circuits added without digressing from the teachings of this application as may be appreciated by those with ordinary skill in the art.

Fig. 8B illustrates symbol logic bit in PRISM (DRAM based with independent Refresh port). This

30 figure illustrates the circuit detail for the symbol logic, 703, of the state block bit realized using dynamic memory like DRAM. This figure illustrates the BL(bit line), 835, CL (content bit line), 857, and ML (mask bit lines), 856, as independent signals. The symbol logic bit of Fig. 8B illustrates a realization using dynamic memory architecture for the memory bits. The transistor,

840, and the capacitor, 842 form a typical dynamic memory cell which are coupled to the bit line using the signal 839. The transistor 840 may optionally be of the NMOS type transistor. The capacitor, 842, holds the memory bit state using a dynamic charge which decays over time, and hence it needs to be refreshed with the correct state in certain time period. Typically, the capacitor may be refreshed within 8ms time period. DRAM's typically have refresh mode that is multiplexed with the normal mode of operation. In such a case, the memory banks are not usable during refresh cycles. For a high performance application this is not acceptable. The transistor, 843, is coupled with a refresh bit line, RBL, 836, which is separate from BL, 835. This device, 843, is also coupled to a refresh word line RWL, 833. Thus the dynamic memory based symbol logic of this patent has an independent port to refresh the memory cell and not affect the performance of the PRISM memory during dynamic memory cell refresh. When the word line WL, 801, is asserted, the capacitor, 842, is coupled to the bit line BL, 835, through the transistor, 840. When the BL is driven by the bit line driver, not illustrated in this figure, coupled to the bit line, the logic value on the bit line gets stored as a dynamic charge on the capacitor, 842. If a logic value '1' needs to be stored, the BL is driven to '1' and similarly if the value needs to be '0', the BL is driven to '0'. If the WL, 801, is active then the logic value gets stored in the symbol memory bit. When the symbol memory bit needs to be read the BL may not be driven actively other than pre-charging. The sense amplifiers, not illustrated in this figure, coupled to the bit line may then detect voltage swing on BL to read the symbol memory bit value. All transistor devices illustrated in Fig. 8B except transistor 858 may optionally be of NMOS type while the transistor 858 may optionally be of the PMOS type.

During normal operation of the PRISM memory being used for content inspection, the symbol bit has to be available and refreshed. To accomplish this function a refresh circuit, not illustrated, which may optionally be present in the Cluster FSA Controller, 1302, for each PRISM cluster or may be present for the entire PRISM memory as separate functional block or the like, and may be continuously operating to refresh the dynamic memory locations when the PRISM memory is comprised of dynamic memory cells. The PRISM memory may either be comprised of dynamic memory or static memory or a combination. The refresh circuit would have access to all the rows and columns of the dynamic PRISM memory through the appropriate refresh word lines like RWL, 833, and the refresh bit lines like RBL, 836. The refresh circuit may optionally comprise of refresh counter(s) that may count from 0 through optionally 2000 and use the count as a refresh word line address for each block of optionally 2000 memory rows selecting refresh word line like RWL for each row and cycling through them, refreshing all the memory locations,

at least once within the refresh time window which may typically be less than 8ms. To refresh a dynamic memory location, the refresh word line, 833, is activated coupling the refresh transistor, 843, the capacitor, 842, and the refresh bit line, 836. The sense amplifiers on the refresh bit lines detect the value stored on the capacitor. An FSA clock cycle may optionally comprise of a

5 pre-charge phase when various pre-charged signals like the RSx signals, like 837, or the Rule match signals and the like get pre-charged to Vcc or high logic level. The FSA clock cycle optionally also comprises of an evaluate phase during which all the FSA evaluations are performed and at the end of that clock cycle the state updates are stored in the state memory or flip-flops, like 508a. The refresh operation is typically performed during the pre-charge phase of

10 the FSA evaluation. During this period the refresh word line is selected and the memory bit value on the capacitor like 842, is read on to the refresh bit line, 836. The sense amplifiers, not illustrated, coupled to the refresh bit lines detect the memory value and record the value for writing it back on the capacitor to restore the memory bit state. The refresh bit lines also retain the value on the line for use during the evaluate state since the capacitor of the memory cell is

15 disturbed during the reading by the refresh operation. During this period the capacitor may be fully restored as well or may be refreshed to a sufficient level to be used in the evaluate phase without giving false mismatch. The refresh word line may optionally be kept active during the evaluate phase of the cycle as well so that the memory bit value that is retained on the refresh bit line provides the correct symbol bit value to be used during the evaluation phase of the FSA

20 clock cycle. Then during the pre-charge phase of the following FSA clock cycle the bit value recorded by the refresh sense amplifiers is fully written to the capacitor 842 through the refresh transistor 843 coupled to the refresh bit line. This phase is also called refresh restore phase in this patent. During the refresh restore phase, the refresh word line is kept active. Thus the dynamic memory cell illustrated in Fig. 8B can be refreshed and restored and be used in the

25 FSA rule block and PRISM memory saving about four transistors per memory bit location compared to the static memory based cells. The method of refresh and restoring the memory bit cells may be chosen based on the need for performance, design complexity and the like. For a lower frequency operation, the refresh read and restore operation may all be completed in the pre-charge phase of one FSA clock cycle, however for a higher frequency operation the refresh

30 read and restore operations may be performed in the pre-charge phase of two different or consecutive FSA clock cycles as described above. Thus, each memory location may be refreshed within one or two FSA clock cycles and the refresh circuitry is designed appropriately to refresh each location at least once during the dynamic memory refresh period discussed above as can be appreciated by those with ordinary skill in the art.

The transistor 849 and the capacitor 851 form the dynamic memory cell that holds the optional mask bit of the mask vector for the dynamic memory based PRISM symbol logic bit. The transistor 849 is also illustrated to be coupled to the word line 801, though it could optionally be coupled to a different word line for mask vector. This memory location is used to store the symbol mask bit. The symbol mask bit when set enables the symbol evaluation and disables the evaluation when the mask bit is disabled. Reverse setup is also feasible, except the connectivity between the symbol memory cell and the mask memory cell would need to be changed appropriately. The device pairs 845, 847 and 846, 848 are coupled to the symbol bit, mask bit, the content line (CL), 857, complement of the content line (CLn), 834, and form an XOR functionality by coupling with the RSx/CAM Match x pre-charged signal line 837. The line 837, is shared between adjoining symbol logic bits of a PRISM FSA rule block. This line is pulled low, if any of the bit pairs of the content and the symbol do not match, assuming the bit is enabled using the optional mask bit. The line stays high only if all the bits of a symbol match all content symbol bits. The mask bit is coupled to devices 845 and 846 by the signal 854. When the mask bit, capacitor 851, is set, the device 852, is turned-on which enables the path from devices 846 and 848 to ground, when the content value on CL, 857, coupled to device 848, by the signal 855 is '1' and when the symbol bit value is '0', a value of '1' is coupled to 846 by signal 860 which is an output of the inverter formed by the devices 858 and 859, which then enables the path from the RSx/CAM Match x, line 837, to ground, GND. This causes the match signal 837 to be pulled-down or low indicating a mismatch. Similarly the transistors 845 and 847, are turned on when the symbol value is '1' and the complement of the content value, CLn, 834, is '1' indicating the content value to be '0', thus forming a XOR function on the RSx or CAM Match x signal, line 837. Thus, the match signal, 837, stays high or active only when all the bits of the symbol and the content input match respectively. Though the symbol evaluation illustrated is a compare operation, other operations like range detect, or other ALU operations may be implemented with appropriate circuits added without digressing from the teachings of this application as may be appreciated by those with ordinary skill in the art.

Fig. 9 illustrates Partial State Logic Bit in PRISM. This figure illustrates a circuit for the partial state logic block, 706. The partial state logic bit comprises of a memory bit for state dependent vector. The transistors 906, 912, 913, 914, 915 and 918 form the typical six transistor static memory cell configuration to store the SDV bit. The operation of this memory bit is similar to the memory bits described above. The word line WL2, 901, selects devices 906 and 918, and the BL/CL/ML, and the complement are coupled to the memory cell from 905 and 920 respectively.

The transistors 908, 909, 910, 911, 916 and 919, form the three input NAND gate between the stored SDV bit, the input state Qy, 921 and the RSx line 902 coupled to transistor 911 using signal 904. The NAND gate generates the partial state transition control signal STxy, 917, that indicates if there is a transition from state 'x' to state 'y' activated similar to the signal 717. Even though the circuit of the NAND gate is fully static, it may be possible to use precharged circuits to realize the same function with fewer gates as may be appreciated by those with ordinary skill in the art. The transistors, 912, 914, 908, 916, 919, illustrated in Fig. 9 may optionally be of the PMOS type, while the other transistors illustrated in Fig. 9 may optionally be of NMOS type.

Fig. 9A illustrates Partial State Logic Bit in PRISM (DRAM based with refresh port). This figure illustrates a circuit for the partial state block, 706 using a dynamic memory cell. The partial state logic bit comprises of a memory bit for state dependent vector (SDV). The transistor 930 and the capacitor 932 form a typical dynamic memory cell configuration to store the SDV bit. The operation of this memory bit is similar to the memory bits described above for the symbol logic. Since this is a dynamic memory cell like the one in the dynamic symbol memory bit illustrated in Fig. 8B, this memory bit also needs to be refreshed. The transistor 933, coupled to refresh bit line, 926, and the refresh word line, 923, create an independent refresh port similar to the one for the dynamic symbol memory bit discussed above. This dynamic memory cell is also refreshed using mechanism similar to that discussed above for the symbol dynamic memory cell illustrated in Fig. 8B. The word line WL2, 901, when asserted turns the devices 930 on and enables coupling of the capacitor, 932, and the bit line BL, 925, through the signal 929. The transistors 936, 937, 938, 939, 940 and 941, form a three input NAND gate between the stored SDV bit, 932, the input state Qy, 921 and the RSx line 924 coupled to transistor 939 using signal 928 (for clarity, RSx is the same signal as the signal RSx / CAM Match x signal 837 illustrated in Fig. 8B). The NAND gate generates a partial state transition control signal STxy, 917, that indicates if there is a transition activated from state 'x' to state 'y'. Even though the circuit of the NAND gate is fully static, it is possible to use pre-charged circuits to realize the same function with fewer gates as may be appreciated by those with ordinary skill in the art. As illustrated in Fig. 9A the transistors, 936, 940 and 941 may optionally be of PMOS type while the other transistors in this figure may optionally be of NMOS type.

Fig. 10a illustrates state control block in PRISM. This figure illustrates the state control block, 604, with the appropriate elements labeled. Essentially the NAND gates, 1001(1) through 1001(n) are bit specific state transition control logic portions that logically NAND the partial state outputs from the state blocks. The blocks 1002(1) through 1002(n) are the initialization blocks

described earlier and the blocks 1003(1) through 1003(n) hold the states of the NFA or FSA rule block.

Fig. 10b illustrates local Init Detect Circuit in PRISM. This circuit may be optionally used to detect if the states of the FSA reach an error, which in this case is assumed to be all state bits to be inactive or low. The FSA is evaluating a symbol only when at least one of the states is set, otherwise the FSA may reach an error state and stop evaluating the input content. To prevent such a condition, the circuit illustrated in Fig. 10b is used to generate a local initialization signal whenever all the states of the FSA are inactive. This signal, Linit, can then be used to set the FSA to a predefined start state. The signal Linit, 1018, is pre-charged to an active high value. Whenever, at least one of the state bits, Q1 through Qn is active the transistor coupled to that state, 1007(1) through 1007(n) respectively, is turned on and the signal Linit is pulled to an active low state, however when each of the state bits is inactive, the Linit signal stays high indicating a local initialization signal which gets processed by state control block bit gates 1019 and the multiplexer, 1015, that then initializes the state bit, 1032, to the start state memory bit coupled through signal 1024 and the multiplexer 1014 and 1015 to the state memory bit, 1032. As illustrated in this Fig. 10b, all transistors may optionally be of NMOS type except transistor 1006 which may optionally be of PMOS type.

The Fig. 10c illustrates state control block bit in PRISM. This block bit stores the initialization vector or start state bit in a typical six transistor static memory configuration created using the transistors, 1008, 1010, 1012, 1011, 1013 and 1009. The start state bit is selected by the FSA controller by driving the word line ivWL, 1027, which is coupled to devices 1008 and 1009. The value on the BL and BLn is coupled through those transistors into the memory cell during write and is read onto the bit lines during a read operation. The output of the memory cell, 1024, is used as one of the inputs to a multiplexer, 1014 which may optionally be present to enable selection of the initialization vector bit. When the Load signal, 1017, is asserted, the value of signal LS_n, 1016, is coupled to the output of the multiplexer, 1022 but when Load signal is not asserted the start state bit, 1024, is coupled to 1022. The signal LS_n, may optionally be provided as a means to load a state context that was saved earlier or any other state value to be loaded into the state bit, 1032. The state bit, may alternatively be written using a memory bit and be coupled with the other initialization logic appropriately. The Load signal may be asserted by the FSA controller to indicate updating the state bit value. During normal operation the signal 1025 that acts as a select signal for the multiplexer 1015 is inactive, selecting the output of the bit location specific gate like 1001(n) which indicates the state transition of the FSA during

normal content evaluation. However, if the local initialization signal is asserted then path from the start state bit 1024, to the state bit, 1032 is enabled and the state bit gets initialized. There may also be a need to provide a global cluster wide or PRISM memory wide initialization, which is controlled by asserting global initialization signal Glnit, 1018b which again enables the path

5 from the start state bit 1024 to the state bit 1032. The state control block may generate state bit signals Qn, 1029 and optionally signal Qnb, 1030. The state bit, 1032, may be updated at synchronized interval with other parts of the memory, using a control signal, 1031, which may be a clock or an enable signal or other signal like hold or a combination. As illustrated in Fig. 10c the transistors, 1010 and 1011 may optionally be of PMOS type while the transistors, 1008,

10 1009, 1012, 1013, illustrated in this figure may optionally be of NMOS type.

The Fig. 10d illustrates state control block bit in PRISM (DRAM based). This state control block bit stores an initialization vector or start state bit in a typical dynamic memory configuration created using the transistor, 1035, and the capacitor, 1038. The start state bit is selected by the PRISM cluster FSA controller by driving the word line ivWL, 1027, which is coupled to the

15 transistor 1035. The value on the bit line BL, 1026, is coupled through this transistor, 1035, to the capacitor, 1038 which stores the memory bit value as a dynamic charge similar to the dynamic memory cells described above. Similar to the other dynamic memory cells described above, this memory cell also needs to be refreshed. The refresh transistor, 1039, couples the refresh bit line RBL, 1034 to the capacitor 1038 when the refresh word line ivRWL, 1033, is

20 asserted. The refresh mechanism for this memory cell also follows similar mechanisms and principles as described above for the other dynamic memory cells of this application like the symbol memory bit illustrated in Fig. 8B. The output of the memory cell, 1024, is used as one of the inputs to a multiplexer, 1014 which may optionally be present to enable selection of the initialization vector bit. The other elements of this illustration operate essentially in similar

25 manner as described above for the Fig. 10c. Further, various circuits of illustrated in this figure may be realized using a dynamic circuit architecture as would be appreciated by those with ordinary skill in the art. As illustrated in Fig. 10d the transistors, 1035, and 1039 may optionally be of NMOS type.

Fig. 11 illustrates Tagged match detect block bit in PRISM. As discussed earlier the FSA of

30 PRISM are optionally Tagged. The discussion below is with respect to tagged NFA or FSAs, though it is also applicable for non-tagged NFAs or FSAs where the tagging elements, are not used or not present. The tagged match detect block bit comprises of an accept state memory bit, formed by the familiar six transistor static memory bit as earlier memory bits, where the

transistors 1106, 1110, 1112, 1111, 1113 and 1114 form the accept state memory bit. The devices 1106 and 1114 are coupled to the word line AWL, 1101, which selects the accept memory bit when it needs to be read or written. These devices are also coupled to the four transistors forming the back to back inverter and the bit lines, 1104 and 1115. This memory bit

5 is read and written in a manner similar to the description for other memory bits above. The tagged Match Detect block bit may optionally comprise of a tag state memory bit which may be set to detect a sub-expression evaluation as described earlier. Additional tag state bits and state transition tag bits may be optionally present in PRISM tagged match detect block bit as discussed earlier but are not illustrated in this figure. The optional tag memory bit is again stored

10 in a typical six transistor memory cell comprising the transistors, 1124, 1125, 1126, 1127, 1128 and 1129. This memory location may be selected by asserting word line TWL, 1119. The operation of the tag memory cell is similar to other memory cells described above. The rule match detection is formed by coupling accept state bit 1107 and the FSA state Qn, 1102, through the devices 1108 and 1109. When accept state bit is set, it indicates that the particular

15 state bit is an accept state, meaning that when the FSA evaluation reaches that state a string recognized by the regular expression rule programmed in the NFA is found and hence a rule match should be signaled. The Rule Match signal, 1103, is an active low signal as illustrated. It is precharged to a high value and stays at that level as long as a state which is an accept state is not reached. However, when Qn signal is asserted and the accept state bit 1107,

20 corresponding to that state signal Qn, is set, the devices 1108 and 1109 pull the rule match signal low, indicating a match. The rule match signal is shared with the adjoining bits of the FSA, so when any of the accept state bit is matched the Rule Match signal is asserted to an active low value. The polarity of the rule match signal can be reversed by selecting appropriate bits to couple to the transistors 1109 and 1108. Similarly, if the tagging is supported, the devices

25 1130 and 1132, couple to the tag match signal, 1122 and pull it down if the tag is asserted and the FSA state is also asserted. The rule match and tag match signals from individual NFA rule blocks in a PRISM cluster array may be evaluated by the local and/or global priority encoder and the evaluation processors of PRISM memory illustrated in fig. 12 and 13 and appropriate actions taken as described above. As illustrated in Fig. 11 the transistors, 1110, 1111, 1126,

30 1127 may optionally be of PMOS type while the other transistors in this figure may optionally be of NMOS type.

Fig. 11A illustrates match detect block bit in PRISM (DRAM based). As discussed earlier the FSA of PRISM are optionally tagged. The discussion below is with respect to non-tagged NFA,

though it is also applicable for tagged NFAs where the tagging elements, are present and being utilized. The match detect block bit comprises of an accept state memory bit, formed by a typical transistor and capacitor based dynamic memory bit similar to other dynamic memory bits earlier, where the transistor 1136, and the capacitor 1138 which holds the memory value as a dynamic charge form the accept state memory bit. The device 1136 is coupled to the word line AWL, 1133, which selects the accept memory bit when it needs to be read or written. This memory bit is read and written in a manner similar to the description for other dynamic memory bits above. Similar to the other dynamic memory bits described above, this memory bit also comprises of a refresh port comprised of the refresh transistor, 1139, coupled to the refresh word line ARWL, 1134, and the refresh bit line RBL, 1147. The refresh mechanism for this dynamic memory cell follows the same principles and methods described above for the dynamic symbol memory bit illustrated in Fig. 8B and other dynamic memory bits. The rule match detection is formed by coupling accept state bit 1137 and an FSA state bit signal Qn, 1102, through the devices 1141 and 1142. When accept state bit is set, it indicates that the particular state bit is an accept state, meaning that when the FSA evaluation reaches that state a string recognized by the regular expression rule programmed in the FSA is found and hence a rule match should be signaled. The Rule Match signal, 1103, is an active low signal as illustrated. It is pre-charged to a high value and stays at that level as long as a state which is an accept state is not reached. However, when Qn signal is asserted and the accept state bit 1137 is set, the devices 1141 and 1142 pull the rule match signal low, indicating a match. The rule match signal is shared with the adjoining bits of the FSA, so when any accept state bit is matched the Rule Match signal is asserted to an active low value. As illustrated in Fig. 11A transistors, 1136, 1139, 1141, 1142 may optionally be of NMOS type.

Fig. 14 illustrates a computing device with content search memory based accelerator. The computing device may be a server, a workstation, a personal computer, a networking device like a switch or a router or other type of device. This is one type of configuration in which a content search accelerator using one version of the content search memory of this invention may be used. The figure illustrates a computing device comprising one or more CPUs, 1400 (1) through 1400 (n), at least one chipset, 1402, at least one memory component, 1401, with at least one content search accelerator, 1403, and zero or more adapters providing other functions. The content search accelerator may comprise of content search memory (PRISM), 1404. It may also comprise at least one memory component, 1405, coupled to the content search memory. There are many different system configurations that may be created with the content search memory

of this invention. Hence the examples in this patent should not be used as limiting the scope, rather they are primarily a means to explain the content search memory in a few sample usage scenarios. The content search memory of this patent may be used on line cards, network adapters or network interface controllers, storage networking cards, IO cards, motherboards, control processing cards, switching cards or other system elements of systems like networking devices such as routers, switches, management devices, security devices, gateways, virtualization devices, storage networking devices, servers, storage arrays, and the like. The content search memory or its components may also be coupled to or embedded in or a combination thereof, the microprocessors, network processors, regular expression search processors, content search processors, multi-core processors, switching chips, protocol processors, TCP/IP processors, control plane processors, chipsets, control processors or other devices, including being incorporated as a functional block on these processors or chips. The content search memory may be used to perform content inspection at high line rates in the systems in which it is incorporated to offload or assist in content processing to the main processors of such systems. There may be configurations where multiple content search memories may also be incorporated in systems to provide scaling in performance or number of rules or a combination thereof for content search. The content search memory may be incorporated on network line cards, in line with the traffic and offer line rate deep packet inspection when coupled to a networking processor or TOE or packet processor or the like.

The configuration illustrated in Fig. 14 may optionally be used for email security or instance message security or outbound security or extrusion detection or HIPAA compliance or Sarbanes-Oxley compliance or Gramm-Leach-Bliley compliance or web security or the like or a combination thereof. The security capabilities listed may comprise anti-spam, anti-virus, anti-phishing, anti-spyware, detection/prevention of directory harvest attacks, detection/prevention of worms, intrusion detection/prevention, firewalls, or the like or detection/prevention of leaks of confidential information, health care information, customer information, credit card numbers, social security numbers or the like or a combination thereof. The content search memory in such device may be configured with a set of security rules for one or more of the applications listed above and provide acceleration for content search for information incoming or outgoing from the device. Content search memory device may be deployed at any place in the network, like close to or embedded in a router or a switch or gateway of an organization's networks or at a departmental level or within a datacenter or a combination and provide high speed content inspection to incoming or outgoing traffic flow of the network.

Fig. 15 illustrates example anti-spam performance bottleneck and solution. As discussed earlier, content search performance using a DFA or NFA based search on a microprocessor results in below 100Mbps performance. Fig. 15 illustrates an anti-spam application as an example application to show the value of hardware based content search. The performance numbers are not illustrated to scale. The figure illustrates four vertical stacks of operations in four types of appliances. The first stack, 1500, is illustrated to represent an email appliance stack. An email appliance typically may comprise device drivers to drive the hardware devices on the appliance, the networking protocol stack along with other functions of the Operating System (OS) and a mail transport agent (MTA) which are all typically software components along with other application software. Today's servers, which are typically used for email appliances, are able to keep up with network line rates of up to 1Gbps, and perform the application functions due to the high performance processors. Typically a 1GHz processor is required to process 1Gbps line rate traffic for network protocol stack processing. Since the state of art processors are around 4GHz today, the servers can handle the network traffic and have processing power available to do other needs of the OS and the applications running on a server. Thus the email appliance stack, 1500, running on a high end server, should be able to keep up with a high line rate. A study by network world magazine, "Spam in the Wild: Sequel" done in December 2004, showed the performance comparison of a large number of anti-spam software and appliance vendors. Under their configuration the range of the message processing performance of the vendor products listed was from around 5 messages per second to 21 messages per second. When this performance number is translated into line rate performance using the worst case message sizes used by network world of 10,000 characters per message, the line rate performance comes to be below 2 Mbps sustained performance. All the vendors either software or appliance solutions were based on dual Xeon processor servers. Thus, a server that can handle 1Gbps network line rate traffic, when performing anti-spam application its performance drops down to below 10 Mbps. The reason for this is that one of the features used extensively by most anti-spam vendors is searching of emails against a set of rules, which are typically represented as regular expressions. The anti-spam appliance stack, 1501, illustrates the email appliance with anti-spam capability loaded on it. Anti-spam applications typically performs many complex regular expression rules based filtering along with statistical filtering, reputation based filtering and the like. The anti-spam rules are typically applied sequentially to each incoming email one after the other to find a rule that may match the content of the email. Then the anti-spam application may apply scores to the rules that match and then decide if a message is spam or not based on the total score it receives. Such an operation causes the stack performance needs

to grow substantially higher than a typical email appliance stack, where the anti-spam filters, 1505, overhead on the performance of the appliance is substantial to reduce the over all anti-spam server appliance performance to be below 10Mbps. The content search memory of this invention can be used in such anti-spam appliances to achieve significant performance

5 improvements. The hardware accelerated anti-spam appliance stack, 1502, illustrates the impact of using the search memory of this invention on the overall performance of the system. In such a case, all the anti-spam filters, 1511 thru 1513, may be configured on the search memory, 1506, which in turn may be used to inspect each incoming message. Since all rules would be searched simultaneously, the search memory based appliance can achieve well over

10 1Gbps line rate performance or more, since the host CPU is relieved from the performance intensive regular expression searches. The compute device illustrated in Fig. 14 may be one such configuration that may be used as the anti-spam appliance to achieve multiple orders of magnitude higher performance than a typical server based anti-spam appliance. The stack, 1503, illustrates a stack of an enhanced messaging appliance which may use a TCP/IP offload

15 processor for offloading the protocol processing from the host CPU along with the content search memory of this invention. Thus a significant amount of CPU bandwidth can be made available to other applications which may not have been possible to execute on the computing device without significant performance impact. The use of TCP/IP offload and content search memory may be done individually or in combination and the use of one does not require the use

20 of the other. TCP offload and content search memory could be on the same device providing network connectivity and the acceleration. Although the discussion above is with respect to anti-spam application, other critical network applications like Intrusion Detection and Prevention systems suffer from similar performance issue, where the line rate gets limited by memory access time if a composite DFA type solution is used. Typical IDS/IPS performance on a single

25 processor based solution does not scale above 1Gbps. The content search memory of this invention can be applied for IDS/IPS regular expression search performance issues and can achieve one to two orders of magnitude higher line rate inspection than any composite DFA based solutions.

Fig. 16 illustrates an anti-spam with anti-virus performance bottleneck. This figure is very similar

30 to Fig. 15, except that the anti-spam appliance whose stack is illustrated also supports anti-virus capability. Anti-virus searches are different then the anti-spam searches but they also add a significant performance overhead as illustrated by the stack, 1604. The number of filters for anti-virus is lot larger then those for anti-spam, though when a content search memory of this

invention is used the anti-virus overhead can also be substantially reduced as illustrated by 1605.

Fig. 17 illustrates application content search performance bottleneck and solution. The content search memory of this invention can be used as a search accelerator for a large number of applications that require content search but do the search on the host processor or host CPU or host microprocessor or the like. Since, the performance of these processors for content search is not very high as discussed above, a content search memory based accelerator can substantially increase the performance of these applications. The applications that require content search are many like data warehousing applications, database applications, bioinformatics related applications, genetics, proteomics, drug discovery related applications and the like. The figure illustrates three boxes, 1700, 1701 and 1702 which represent the content search based application performance in terms of host CPU load. The traditional applications run on a server or a workstation or personal computer, and perform content search interspersed with other tasks that the application needs to perform. If the applications perform a significant amount of search, then the performance need of the search portions of the application can be substantially higher than the other parts. This is illustrated by content search portions of applications app1 and appN, 1703 and 1705 respectively, compared to the other code of these applications, 1704 and 1706. The stack in 1700 is how current or prior art solution exists for content search applications. Though the stack illustrates a continuous stack for content search and other code sections, the actual execution may generally be composed of search interspersed with other code functions. When a content search memory and accelerator of this invention is used in the computing device performing this function, it may be possible to have the application leverage the search capabilities of the memory and accelerate the performance of the application substantially compared to a computing device without the search acceleration support. The stack in 1701, illustrates the impact on the CPU load and the resulting time spent by the application when converted to leverage the content search accelerator. The stacks 1703 and 1705, could take substantially less load and time as illustrated by stacks, 1707 and 1708 respectively. Similarly, the performance of the system may be further increased by offloading the TCP/IP protocol processing as illustrated by 1709. As described above, TCP/IP offload and content search offload are independent of each other and may each be done without the other in a system. However, one could also use the content search memory with the TCP/IP processor together as separate components or on the same device and achieve the performance benefits.

Fig. 18 illustrates an example content search API usage model. As discussed above, the content search memory may be used to accelerate content search portions of generic applications. To enable an ease of creation of new applications and migrate existing applications to leverage such search memory acceleration capability this invention illustrates an application programming interface (API) for content search. An example content search API is illustrated in Fig. 19 and described below. The content search API may reside in the user level or the kernel level with user level calls, or a combination. The Fig. 18 illustrates the content search API at the user layer, 1807. The content search API would provide API functions that any application can call to get the benefit of content search acceleration. There would be a convention of usage for the applications to use the content search API. For example the application may be required to setup the search rules that can be configured on the search memory using the API calls before the application is run or may be required to dynamically create the rules and set them up in the appropriate format so that they can be configured on the content search memory using the API or a combination. There would be API calling conventions that may be established dependent on the hardware system, the operating system or the search memory or a combination. The applications may then be coded to the API conventions and benefit from the search memory acceleration. The figure illustrates applications App1, 1800 through App N, 1803, working with the content search API, 1807 to get access to the content search memory/acceleration hardware, 1817, using logical interface paths illustrated as 1812, 1813 and 1814. The content search API may access the services and resources provided by the content search memory/accelerator through a port driver which may be running under a kernel. The applications may pass the content to be searched directly through this interface or put the content to be searched as well as tables to be setup as needed, in the application's buffers, 1804, 1805, and then instruct the content search memory to retrieve the information from these buffers through the content search API. The API may map these buffers to the kernel space so the port driver for the search API can provide them to the content search memory or the buffers may be made available for direct memory access by the search memory hardware. The search memory may store the content in on-chip or off-chip memory buffers, 1818, and then perform the requested search on the content. Once the search is complete the results of the search may be provided back to the application using a doorbell mechanism or a callback mechanism or data buffers or the like as allowed by the operating systems' model. The content search API may provide a polling mechanism as well which may be used by the application to check and/or retrieve the search results.

Fig. 19 illustrates an example content search API with example functions. The figure illustrates a set of functions which may be a part of the example content search API. Though, the list of functions may be more or less than those illustrated, the functions provide a basic set that would enable an application to use the content search memory hardware with the use of the API. The example functions do not illustrate the input, output or return parameters for API function calls, which may depend on the operating system, calling conventions and the like as can be appreciated by one with ordinary skill in the art. An application may use the API, by first querying the capabilities of the PRISM content search memory and then initializing it with appropriate rules, pointers, permissions and the like that may be required for the content search memory to communicate with the application and its resources through the kernel or the user mode or a combination. The application may set specific rules as tNFA rules or NFA rules which may get configured in the search memory. An application may be given access to multiple contexts that it may be able to leverage to perform context based search. The application can start performing the search against its content once the content search memory is appropriately setup with all necessary rules. The application can communicate the content to be searched directly to the search memory using the API by sending a byte stream of the content through the interface. There may be versions of an API function, not illustrated, like `sendData()` which may be used by an application to start sending data to the search memory, start the search and to indicate when the search memory should stop searching. A more efficient way of performing the search may be that the application may fill a buffer or a set of buffers to be searched, and then provide the search memory with a pointer(s) to the buffer(s) so it can then start searching the buffers with the configured rules once it receives a call to start the search using an API call like `startHWsearch()`. The search memory may have been initialized to communicate the results of the search to the application through one of many mechanisms like copying the results to a result buffer or storing the result on the memory associated with the search memory or invoking a callback function registered by the application to the operating system or the like. The search memory may also communicate to the application with a doorbell mechanism to inform it that the search is done. There are many different ways of communicating the information as described earlier and may be dependent on the operating system and the system hardware architecture as can be appreciated by one with ordinary skill in the art. There may also be polling mechanism available with an API function like `isSearchDone()`, not illustrated, which may provide the answer to a query to the search memory whether a specific search is complete. If the answer from the PRISM memory to the application is that the search is done, then the application may ask for the specific result using an API call like `getRes()`, or the application may

ask for a pointer to a buffer that may hold the result using an API call like `getResPtr()` illustrated in Fig. 19. Once the application is done with the specific search or is done using the search memory it may call the API function `stopHWsearch()` to stop PRISM memory from performing the search for this application. There may also be an API call like `removeAppContext()`, not
5 illustrated, which may be called by the application to indicate to the OS and the search memory hardware that the application is done using the search memory and hence all its associated context may be freed-up by the search memory hardware for use by another application that may need the search memory resources. There may be other hardware features specific API calls as well, like `setRuleGroup()`, `selectRuleGroup()`, `setInitGroup()` and the like, that may allow
10 an application to create groups of rules and the order of their execution using mechanisms of rule grouping using the PRISM cluster arrays that may enable rule groups. As discussed earlier there may be many more functions and variation of API functions that can be created to enable a general content search application acceleration using a hardware search memory from the teachings of this patent that will be appreciated by those with ordinary skill in the art. Thus it is
15 possible to create a content search API to provide content search capabilities to general applications. Though, the description above is given with an example where the rules to be used are setup by an application before starting the search, it may be possible to update the rule set that is configured in the search memory dynamically while the search is in progress by adding, removing and/or modifying the rules that have already been configured to start using the
20 updated rule set for any future searches by the application.

Fig. 20 illustrates an example application flow (static setup) using the search memory. The flow illustrates a static process for setting up the rules and the search memory although as discussed above a dynamic setup is also feasible as would be obvious to one with ordinary skill in the art. The flow may allow an application to add/remove/modify rules in the search memory
25 as the application executes at runtime to enable a dynamic flow. The illustration provides a mechanism where existing applications or new applications may be updated with content search rules and API calls which can enable the application to use a content search memory. An application source, 2000, may be updated, 2001 to create application source with modifications for content search where the content search rules may be setup in distinct code sections or may
30 be clearly marked, 2002, as expected by the content search compiler coding conventions, which is then compiled by a content search aware compiler, 2003. The compiler generates an object code, 2004, with content search rules compiled in sections which a loader may use to configure them in the search memory. The application object code may then be distributed to customers

or users of content search memory for accelerating the application's search performance. The application code may be distributed electronically using the internet, world wide web, enterprise network, or other network or using other means like a CD, DVD, or other computer storage that can be used to load the application. The application update, 2001, may be done manually or
5 using a tool or both as appropriate. The distributed object code, 2006, is read by the loader, 2007, or a similar function provided by an operating system to which the application is targeted, and setup for execution on the system. The loader or another function may use a set of content search API calls or a port driver or other OS function or a combination to configure the content search memory with appropriate rules that the application needs as coded in the object code as
10 illustrated by block 2008. Once the search memory hardware is setup and other resources that the application needs get reserved or setup, the application is started, 2009, by the OS. The application may execute or perform tasks, 2010, if needed before content search. The application may then setup the content, 2011, it needs to search by the search memory. Then it starts the search memory to perform search, 2013. Once the search is done it may retrieve the
15 results, 2014. While the search is being conducted by the search memory, the application may continue to perform other tasks, 2012, on the main CPU or other elements of the system. If the application is done the application may exit, otherwise the application may continue the execution where more tasks may be performed including new search if necessary. The flow diagram illustrates the execution of tasks as a loop from 2015 to 2010, though the tasks being
20 executed may be very different from one time to the next through the loop. The loop is not illustrated to mean that the same code sequence is being repeated. It is meant to illustrate that the type of tasks may be repeated. Further, not all tasks from 2010 through 2015 may need to be present in an application flow as may be appreciated by one with ordinary skill in the art. Once the application is done, it may release all the resources it uses beside those for the
25 content search memory.

Fig. 21 illustrates a PRISM search compiler flow (full and incremental rule distribution). The flow can be used for distributing search rules or security rules when the full set of rules are defined or when any updates or modifications are made to the rule set and incremental changes to the rule set need to be communicated and configured in the search memory. The search memory
30 may be used in a distributed security architecture within system nodes across a network which may be a LAN, WAN, MAN, SAN, wireless or wired LAN and the like. The rules like application layer rules, network layer rules or storage network layer rules or any other search rules may be created using manual or automated means and provided as inputs to the search compiler flow

in a predefined format. The search compiler's rule parser, 2104, parses the rules and converts them into regular expression format if the rules are not already in that form. Then the regular expression rules are converted into FSA rules compiled to the node capabilities of the node that has the content search memory and stored in the rules database. The rules from the rule

5 database are retrieved and distributed by the rules distribution engine to the appropriate node(s) with the search memory. The search or security rules may be distributed to the host processor or a control processor or a host microprocessor or a network processor or a master processor or a combination thereof as appropriate depending on the node capability. The rules may be distributed using a secure link or insecure link using proprietary or standard protocols as

10 appropriate per the specific node's capability over a network. The network may be a local area network (LAN), wide area network (WAN), internet, metro area network (MAN), wireless LAN, storage area network (SAN) or a system area network or another network type deployed or a combination thereof. The network may be Ethernet based, internet protocol based or SONET based or other protocol based or a combination thereof.

15 The PRISM memory of this invention may be manufactured into hardware products in the chosen embodiment of various possible embodiments using a manufacturing process, without limitation, broadly outlined below. The PRISM memory in its chosen embodiment may be designed and verified at various levels of chip design abstractions like RTL level, circuit/schematic/gate level, layout level etc. for functionality, timing and other design and

20 manufacturability constraints for specific target manufacturing process technology. The design would be verified at various design abstraction levels before manufacturing and may be verified in a manufactured form before being shipped. The PRISM memory design with other supporting circuitry of the chosen embodiment at the appropriate physical/layout level may be used to create mask sets to be used for manufacturing the chip in the target process technology. The

25 mask sets are then used to build the PRISM memory based chip through the steps used for the selected process technology. The PRISM memory based chip then may go through testing/packaging process as appropriate to assure the quality of the manufactured product.

Thus the inventions of this patent cover various aspects like:

30 A memory architecture comprising programmable intelligent search memory (PRISM) for content search wherein the PRISM memory provides search capability for regular expression based search.

The PRISM memory further comprises an array of search memory circuits that provide the regular expression search functions for searching content from documents, messages or packets or other data received from the network or the local host or a master processor or a network processor or TCP Offload Engine or Processor or Storage Network processor or a security processor or other processor or a combination thereof.

The PRISM memory further comprises of a plurality of clusters of the search memory circuits that provide regular expression search functions for a plurality of regular expressions. The search memory circuits comprise of memory elements to store symbols of finite state automata representing the regular expressions. The search memory circuits further comprise memory elements to store mask vectors (MV) that may be applied to the stored symbols. The mask vectors are coupled to the symbol memory elements and the content being searched through symbol evaluation circuits that detect whether the received content comprises of the symbols being searched. The search memory circuits further comprise of memory elements to store elements of state dependent vectors (SDV) which are used to decide the state traversal by the search memory for the finite state automata. The search memory circuits further comprise of match detect circuits that operate by coupling with the memory elements for symbols, MVs, SDVs, and the symbol evaluation circuits for multiple states of the FSAs to decide on the traversal of the states in the FSA based on the content being searched and the programmed symbols, SDVs, and MVs. The search memory circuits may further comprise tag and match detect circuits that operate to provide tagged FSA and regular expression search, wherein the tagged FSA is used to detect sub-string or partial regular expression match beside a full regular expression match.

The memory elements of the PRISM memory comprise of static or dynamic memory cells. The memory elements are each independently addressable in a random order. The PRISM memory further comprises of circuits to couple the content search memory with other logic to provide coupling with processors that can interface to the PRISM memory integrated circuits. The PRISM memory further comprises of a controller for interfacing with the processors to receive the content to be searched. The PRISM memory may further comprise of address decode logic circuits which decode the received address to select the specific static or dynamic memory cells location to be read or written. The memory elements of the search memory may each be uniquely addressed to read or write appropriate values in the memory elements. The address decoding logic and the controller generate control signals necessary to address the appropriate memory locations of the static or dynamic memory cells based search memory. The control

signals are coupled to the PRISM arrays as a series of word lines and bit lines that can randomly be used to access desired memory locations.

The memory elements of PRISM support detection of character pattern strings. The PRISM memory comprises of symbol detection circuits and may optionally comprise of mask vectors
5 per symbol bits, that may be used to evaluate received character string using simple XOR based compare or other logic function and create a match indication. The PRISM match signal processing circuits may logically combine multiple match signals from each symbol detection block to generate a composite match signal which would be activated only if all the symbols have a match. The composite match signal creates a match functionality like a traditional CAM
10 chip and thus enable PRISM chip to be partially or fully configured to behave like a CAM provide a pattern matching functionality beside regular expression search.

While the foregoing has been with reference to particular embodiments of the invention, it will be appreciated by those with ordinary skill in the art that changes in these embodiments may be made without departing from the principles and spirit of the invention.

CLAIMS

1. A memory architecture comprising programmable intelligent search memory for content search wherein said programmable intelligent search memory comprises dynamic random access memory circuits and performs regular expression based search.

5 2. An integrated circuit chip comprising programmable intelligent search memory for content search wherein said programmable intelligent search memory comprises dynamic random access memory circuits and performs regular expression based search.

3. A hardware processor comprising an integrated circuit chip memory said integrated circuit chip memory comprising programmable intelligent search memory for content search, wherein said programmable intelligent search memory comprises dynamic random access memory circuits and performs regular expression based search.

4. An integrated circuit chip of claim 2 comprising a processor comprising memory, said memory comprising said programmable intelligent search memory for content search, wherein said programmable intelligent search memory performs regular expression based search.

5. The programmable intelligent search memory of claim 2 for content search using one or more regular expressions, said one or more regular expressions comprising one or more symbols or characters, said one or more regular expressions converted into one or more finite state automata representing the functionality of said one or more regular expressions for programming in said programmable intelligent search memory, said one or more finite state automata comprising a plurality of states, said plurality of states derived from said one or more symbols or characters of said one or more regular expressions, said content comprising one or more input symbols provided as input to said programmable intelligent search memory, said programmable intelligent search memory comprising at least one of each of:

25 a. symbol memory circuit to store said one or more symbols;

b. symbol evaluation circuit coupled to said symbol memory circuit to evaluate match of said one or more symbols stored in said symbol memory circuit with said one or more input symbols of the said content;

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c. state dependent vector (SDV) memory circuit to store state transition controls for said one or more finite state automata;

d. current state vector (CSV) memory circuit to store said plurality of states; and

5 e. state transition circuit coupled to said symbol evaluation circuit, current state vector memory circuit and said state dependent vector memory circuit to perform state transition from one or more first states to one or more second states of said plurality of states of said one or more finite state automata.

6. The symbol memory circuit, the state dependent vector memory circuit, current state vector memory circuit of the programmable intelligent search memory of claim 5 comprises
10 dynamic random access memory circuit.

7. The programmable intelligent search memory of claim 5 further comprises at least one of:

a. memory circuit to store mask vector coupled to said one or more symbols to enable or disable evaluation of specific bits of said one or more symbols by said symbol
15 evaluation circuit;

b. received symbol vector signals generated by said symbol evaluation circuit to indicate when said content comprises said one or more symbols of said one or more finite state automata;

c. accept state vector memory circuit to store which of said one or more states
20 are accept states, said accept states used to detect when said one or more regular expressions have matched with said content;

d. tag state vector memory circuit to store which of said one or more states are tag states, said tag states used to detect when said one or more regular expressions have partially matched with said content;

25 e. start state vector memory circuit to store initialization values of said one or more states;

f. regular expression match detect circuit to detect match in said content with said one or more regular expressions;

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g. tag match detect circuit to detect tag match in said content for said one or more finite state automata that are tagged to detect partial regular expression match or to detect sub-string match or a combination thereof; or

h. Any combination of a through g above.

5 8. The programmable intelligent search memory of claim 5 further comprising circuits to couple said programmable intelligent search memory to at least one functional block or circuit or a combination.

 9. The at least one functional block of claim 8 comprises a microprocessor, multi-
core processor, network processor, graphics processor, switch processor, microcontroller, TCP
10 Offload Engine, network packet classification engine, protocol processor, regular expression
processor, security processor, content search processor, network attached storage processor,
storage area network processor, wireless processor, mainframe computer, grid computer,
server, workstation, personal computer, laptop, handheld device, cellular phone, wired or
wireless networked device, switch, router, gateway, chipset, unified threat management device,
15 and the like or any derivatives thereof or any combination thereof.

 10. The symbol evaluation circuit of claim 5 comprising one or more symbol match signals to indicate a match of said one or more stored symbols with said one or more input symbols of said content.

 11. A plurality of said one or more symbol match signals of claim 10 coupled together
20 to form a composite match signal.

 12. The composite match signal of claim 11 to indicate a composite match, said composite match signal asserted only when each of said one or more symbol match signals coupled to form said composite match signal have a match with a plurality of said one or more symbols of said content.

25 13. The one or more finite state automata of claim 5 are non deterministic finite state automata or tagged non deterministic finite state automata or deterministic finite state automata or a combination thereof.

 14. The one or more finite state automata of claim 5 are programmable finite state automata comprising said one or more states wherein each state of the said one or more states

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is coupled to at least one of said state dependent vector memory circuit to control and program which of said one or more states are coupled to said each state.

15. The one or more finite state automata of claim 5 comprising said one or more states wherein each state of said one or more states is entered from a set of said one or more states coupled to said each state using same input symbol of said content being searched.

16. The one or more finite state automata of claim 5 comprising said one or more states wherein each state of said one or more states is exited to a set of said one or more states coupled to said each state using same input symbol of said content being searched.

17. The one or more finite state automata of claim 5 comprising said one or more states wherein a set of said one or more states are programmed as accept states, said accept states for use to detect when said one or more regular expressions have matched with said content.

18. The one or more finite state automata of claim 5 comprising said one or more states wherein a set of said one or more states are programmed as tag states, said tag states for use to detect when said one or more regular expressions have partially matched with said content.

19. The symbol memory circuit of claim 6 comprising at least one symbol logic bit comprising:

- a. A symbol memory cell to store one bit of said symbol;
- b. A word line signal coupled to said symbol memory cell to select the symbol memory cell;
- c. A mask memory cell to store at least one bit of a mask vector coupled to said symbol memory cell to enable or disable said symbol logic bit and coupled to said word line signal to select mask memory cell;
- d. At least one bit line signal coupled to said symbol memory cell to read or write said at least one symbol bit to said symbol memory cell;
- e. At least one mask bit line signal coupled to said mask memory cell to read or write a mask bit to said mask memory cell;

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f. At least one content bit line signal coupled to said symbol memory cell and mask memory cell to detect a match between a bit of said input symbol and value stored in said symbol memory cell when said mask memory cell is set to an active high value; and

5 g. A received symbol vector bit signal coupled to said at least one content bit line, said symbol memory cell and said mask memory cell to detect and flag a match between said bit of input symbol and said bit of stored symbol.

20. Symbol memory cell of claim 19 comprises:

a. A first NMOS transistor device coupled to a capacitor to store a logic value as a charge on said capacitor, said first NMOS transistor device coupling a value on the said bit
10 line signal to said capacitor when said first NMOS transistor device is selected by said word line signal thereby forming a dynamic memory cell, said dynamic memory cell further comprising a second NMOS transistor device coupled to said capacitor to restore said logic value of said capacitor during a refresh cycle for said dynamic memory cell; or

b. A third NMOS transistor coupled to first PMOS transistor and fourth NMOS
15 transistor, said first PMOS transistor and fourth NMOS transistor coupled together to form a first inverter, and a fifth NMOS transistor coupled to a second PMOS transistor and a sixth NMOS transistor, said second PMOS transistor and sixth NMOS transistor coupled together to form a second inverter, said first inverter and said second inverter coupled together in a back to back configuration, said first and second inverters coupled to said third and fifth NMOS transistors
20 forming a static memory cell, said third and fifth NMOS transistors coupled to said word line signal, said at least one bit line signal and at least one signal carrying complement value of said at least one bit line to store or read said logic value of said one symbol bit to said static memory cell.

21. A memory architecture comprising programmable intelligent search memory for
25 content search wherein said programmable intelligent search memory performs regular expression based search and signature pattern based search.

22. An integrated circuit chip comprising programmable intelligent search memory for content search wherein said programmable intelligent search memory performs regular expression based search and signature pattern based search.

23. The programmable intelligent search memory of claim 22 for content search using a plurality of regular expressions and a plurality of signature patterns, said programmable intelligent search memory comprises of a plurality of programmable FSA rule search engines to perform search using said plurality of regular expressions and further comprises of one or more
 5 programmable signature search engines to perform content search using said plurality of signature patterns, said plurality of regular expressions comprising a plurality of symbols or characters, said plurality of regular expressions converted into a plurality of finite state automata representing the functionality of the said plurality of regular expressions for programming in the said programmable FSA rule search engines, said plurality of finite state automata comprising a
 10 plurality of states, said plurality of states derived from the said plurality of symbols or characters of said plurality of regular expressions, said content comprising a plurality of input symbols or characters provided as input to the said programmable intelligent search memory, said plurality of programmable FSA rule search engines comprising at least one of each of:

- a. symbol memory circuit to store said plurality of symbols;
- 15 b. symbol evaluation circuit coupled to the said symbol memory circuit to evaluate match of the said plurality of symbols stored in the said symbol memory circuit with said plurality of input symbols of said content;
- c. state dependent vector (SDV) memory circuit to store state transition controls for said plurality of finite state automata;
- 20 d. current state vector (CSV) memory circuit to store said plurality of states; and
- e. state transition circuit coupled to the said symbol evaluation circuit, current state vector memory circuit and said state dependent vector memory circuit to perform state transition from one or more first states to one or more second states of said plurality of states of said plurality of finite state automata.

25 24. Programmable signature search engines of claim 23 to perform content search using said plurality of signature patterns, said plurality of signature patterns comprising a plurality of strings of characters of variable lengths, said plurality of signature patterns compiled into a compressed signature database by performing a plurality of hash operations using a
 plurality of hash functions, said plurality of hash functions to create a plurality of hash indices
 30 from said plurality of signature patterns, said compressed signature database having a memory

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bit set for each hash index generated from said plurality of signature patterns, said plurality of signature patterns further compiled to a plurality of FSAs into an exact signature match database used for performing exact signature match operations, said programmable signature search engines comprising at least one of each of:

- 5 a. A signature search controller to control said programmable signature search engines;
- b. A content buffer to store a plurality of characters of said content;
- c. A plurality of hash engines coupled to said content buffer to perform said plurality of hash operations on said plurality of characters of said content;
- 10 d. A signature hash memory coupled to said plurality of hash engines to store said compressed signature database;
- e. A coarse match logic to perform a coarse match on a set of characters of said content using said compressed signature database coupled to said plurality of hash engines and said signature hash memory;
- 15 f. An exact match controller to perform exact signature match on said content that has a coarse match on said plurality of characters with said compressed signature database, said exact match controller to confirm a match in said content with at least one of said plurality of signature patterns; or
- g. A combination of any of a through f above
- 20 25. A programmable intelligent search memory (PRISM) compiler for compiling content search rules comprising a plurality of regular expression rules and a plurality of signature pattern rules for content search wherein said programmable intelligent search memory performs regular expression based and signature pattern based search..
26. The programmable intelligent search memory of claim 25 comprising one or
- 25 more programmable finite state automata (FSA) rule memory circuit and one or more signature search engines, said PRISM compiler for compiling said regular expression rules into one or more programmable finite state automata data structure for programming into said one or more programmable FSA rule memory circuits and said PRISM compiler for further compiling said

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signature pattern rules in data structure for programming into said one or more signature search engines.

27. The PRISM compiler of claim 26 further comprising means to compile a first set of said signature pattern rules in data structure for programming into said one or more signature search engines and further comprising means to compile a second set of said signature pattern rules into a set of programmable finite state automata for programming in the said one or more programmable FSA rule memory circuits, said second set of said signature pattern rules comprising signatures with length less than a predetermined number of characters,

28. The programmable intelligent search memory of claim 27 for content search using one or more regular expressions, said programmable intelligent search memory comprising a symbol memory circuit for storing symbols; a state dependent vector memory circuit for storing state transition controls; an initial vector memory circuit for storing initial vector; and an accept state vector memory circuit for storing an accept state vector, said PRISM memory further comprising an array of randomly accessible PRISM memory locations to access the said one or more programmable finite state automata memory circuits, said one or more regular expressions comprising one or more symbols or characters, said one or more regular expressions compiled by said PRISM compiler into said one or more programmable finite state automata data structure representing the functionality of the said one or more regular expressions for programming in the said programmable intelligent search memory, said one or more finite state automata comprising a plurality of states, said plurality of states derived from the said one or more symbols of the said one or more regular expressions, said content comprising one or more input symbols provided as input to the said programmable intelligent search memory, said programmable intelligent search memory compiler to generate said one or more programmable finite state automata comprising at least one of each of:

a. A symbol representing at least one of the said one or more symbols for programming in the said symbol memory circuit;

b. a state dependent vector representing state transition controls for programming in the said state dependent vector memory circuit;

c. an initial state vector to represent at least one initial state for programming in the said initial state vector memory circuit; and

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d. an accept state vector to represent at least one accept state for programming in the said accept state vector memory circuit.

29. The programmable intelligent search memory compiler of claim 28 further comprises:

- 5 a. a read mechanism to read said one or more regular expressions;
- b. a parse mechanism to parse said one or more regular expressions;
- c. a syntax tree generation mechanism to generate syntax tree of said one or more regular expressions;
- 10 d. an error handling mechanism to handle errors in said one or more regular expressions;
- e. a symbol extraction mechanism to extract said one or more symbols of said one or more regular expressions;
- f. a marking mechanism to mark said one or more symbols of said one or more regular expressions;
- 15 g. a FSA linearization mechanism to create a linear FSA from said one or more programmable FSA;
- h. a mechanism to find and extract first states of said linear FSA from said one or more states of said programmable FSA;
- 20 i. a mechanism to find and extract follow states of the said linear FSA from said one or more states of the said programmable FSA;
- j. a mechanism to find and extract state transition list of the said linear FSA;
- k. a mechanism to find and extract accept states of the said linear FSA from said one or more states of said programmable FSA;
- 25 l. a mechanism to create a PRISM programmable FSA data structure for said one or more regular expressions;

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m. a mechanism to generate a compiled regular expression rules data base comprising said one or more programmable FSA data structures of said one or more regular expressions;

5 n. a mechanism to store or distribute said compiled regular expression rules data base;

o. a mechanism to generate a programmable FSA rule ID for programming said linear FSA in one specific memory location of said PRISM memory locations;

10 p. A mechanism to generate specific actions associated with said one or more regular expression rules when a particular regular expression of said one or more regular expression rules that is programmed in the PRISM FSA rule blocks is matched; or

q. any combination of the above.

30. The FSA linearization mechanism of claim 29 further comprising marking said one or more symbols of said one or more programmable FSAs with unique integers.

15 31. The FSA linearization mechanism of claim 29 further comprising a mechanism to create determinants of said linear FSA to detect presence or absence of an empty string in a language defined by said one or more regular expressions.

32. The content search rules of claim 25 comprise rules that are

20 a. Application layer rules to detect content from an application layer of an OSI stack;

b. Network layer rules to detect content from a network layer of an OSI stack;

c. Storage area networking rules to detect content in a storage area network; or

d. A combination of the foregoing.

25 33. The content search rules of the claim 32 further comprise rules that are

a. Anti-spam rules for detecting spam messages in the said content;

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- b. Anti-virus rules for detecting viruses in the said content;
 - c. Anti-spyware rules for detecting spyware in the said content;
 - d. Digital rights management rules for detecting digital rights compliance or violation in the said content;
 - 5 e. Anti-phishing rules for detecting information indicating phishing attempts in the said content;
 - f. Intrusion detection rules for detecting information indicating intrusions from the said content;
 - g. Extrusion detection rules for detecting information indicating extrusions from
10 the said content;
 - h. Legal compliance detection rules for detecting information that may violate legal compliance rules from the said content;
 - i. Worm detection rules for detecting computer worms from the said content;
 - j. Instant message inspection rules for detecting malware in the said content
15 which is an instant messaging content;
 - k. XML security rules for detecting security compliance or violation of the said content which is a XML content;
 - l. VOIP rules for detecting VOIP security violation from the said content; or
 - m. a combination of any of the foregoing.
- 20
34. The storage area networking rules of the claim 32 comprising:
- a. Logical unit number (LUN) masking rules for controlling storage area network traffic to allow or deny access to specific LUNs;
 - b. Zoning rules for enforcing zones in a storage area network;
 - 25 c. Frame filtering rules to filter frames in a storage area network;

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d. Logical block addressing rules for controlling access to specific logical block addresses in a storage area network; or

e. a combination of any of the foregoing.

35. The network layer rules of the claim 32 comprising:

5 a. Access control rules for controlling access to a network;

b. Network address rules for controlling access to or from specific network addresses of a network;

c. Port specific rules for controlling access to specific network ports of a network;

10 d. Protocol specific rules for checking protocol violations of a network protocol operating on a network; or

e. a combination of any of the foregoing.

36. The programmable intelligent search memory compiler of claim 27 further comprises:

15 a. a read mechanism to read said plurality of signature patterns;

b. a signature length detection mechanism to determine the length of each of the said plurality of signature patterns;

20 c. said signature length mechanism separating out the said plurality of signature patterns into said first set of signature patterns to be compiled into data structure for programming into said one or more signature search engines and further separating the said plurality of signature patterns into said second set of signature patterns for programming into said one or more finite state automata rule memory;

d. hash index generation mechanism to generate a plurality of hash indices for each of the said first set of signature patterns using a plurality of hash functions;

25 e. a compressed signature database generation mechanism coupled to said hash index generation mechanism to set said compressed signature database entries at said

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hash indices to an active value used to indicate presence of a potential coarse signature match during said content search;

5 f. a Aho-corasick Finite Automata (ACFA) or Deterministic FSA (DFA) generation mechanism to generate a plurality of composite ACFA or composite DFA from all of said second set of signature patterns wherein each of said plurality of composite ACFA or composite DFA are generated for all signature patterns that have the same first hash index of said plurality of hash indices, said plurality of composite ACFA or composite DFA for use in exact signature match during said content search forming an exact match signature database;

10 g. a mechanism to generate a compiled signature pattern database comprising said compressed signature database and said exact match signature database;

h. a mechanism to store or distribute the said compiled signature pattern database for programming into said one or more signature search engines;

i. any combination of the above.

15 37. In programmable intelligent search memory of claim 24, the process of performing said content search on a stream of content presented to the said programmable intelligent search memory using said plurality of signature patterns, said process comprising:

a. Said signature search controller reading or receiving or a combination the said stream of content for said content search;

20 b. Said signature search controller writing said stream of content to said content buffer;

c. Said plurality of hash engines retrieving a plurality of characters from said content buffer and generating a plurality of hash indices from said plurality of characters using a plurality of hash functions;

25 d. Said plurality of hash engines retrieving content of memory locations corresponding to said plurality of hash indices from said signature hash memory and providing said content of memory locations to said coarse match logic;

e. Said coarse match logic detecting each of said content from memory locations corresponding to said plurality of hash indices are set active and asserting a coarse

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match signal indicating a coarse match of said content stream with at least one signature of said compressed signature database;

5 f. Said exact match controller coupled to said coarse match signal to detect said coarse match and perform an exact signature match detection using Aho-corasick Finite Automata (ACFA) or Deterministic FSA (DFA) walk of said exact signature match database comprised of said ACFA or DFA data structure to confirm using said exact signature match detection a signature match in said content with at least one of said plurality of signature patterns; or

g. any combination of the above

10 38. Integrated circuit chip of claim 22 embedded in a hardware processor system for accelerating at least one content search application, said hardware processor system comprising at least one integrated circuit microprocessor as a central processing unit to run an operating system comprising kernel layer services and application layer services, said application layer services comprising a application programming interface to couple said content
15 search application to said programmable intelligent search memory, content search operations of said content search application offloaded from said integrated circuit microprocessor to said integrated circuit chip comprising said programmable intelligent search memory, said programmable intelligent search memory further comprising a plurality of regular expression programmable search engines for accelerating regular expression search and further
20 comprising at least one programmable signature search engine to accelerate signature search, said content search application requiring search using a set of variable length signatures or search using a set of regular expressions or a combination thereof..

25 39. Content search application of claim 38 comprises one of the applications from anti-spam, anti-virus, anti-spyware, anti-phishing, intrusion detection, extrusion detection, digital rights management, legal compliance, worm detection, instant message inspection, VOIP security, XML document security and search, genetics, proteomics, XML, XML based protocols like XMPP, web search, database search, bioinformatics, signature recognition, speech recognition, or web indexing application.

30 40. Content search application of claim 39 adapted for running on said hardware processor to use said regular expression acceleration or said signature pattern acceleration

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capabilities of said programmable intelligent search memory, said content search application adaptation comprising:

a. Updating application source code by marking said content search operation code in distinct section; and

5 b. Compiling said updated application source code using a PRISM content search acceleration aware compiler to generate a content search acceleration aware object code;

10 Said object code for loading on said integrated circuit microprocessor for use by a loader of said operating system, said operating system loader setting up said PRISM with application content search operations like regular expressions or signatures or a combination and said content search application sending content to be searched to said PRISM content search acceleration integration circuit chip to accelerate said content search application.

15 41. A memory architecture comprising programmable intelligent search memory for content search wherein said programmable intelligent search memory performs regular expression based search.

42. An integrated circuit chip comprising programmable intelligent search memory for content search wherein said programmable intelligent search memory performs regular expression based search.

20 43. A hardware processor comprising an integrated circuit chip memory said integrated circuit chip memory comprising programmable intelligent search memory for content search, wherein said programmable intelligent search memory performs regular expression based search.

25 44. The programmable search engine of claim 5 further comprises of a fixed number of said symbol memory circuits to store the same number of said symbols, and further comprises of said current state vector memory to store said plurality of states corresponding to said fixed number of symbols of said at least one finite state automaton.

45. The programmable intelligent search memory of claim 44 further comprising a FSA extension architecture to support regular expressions that result in finite state automata

with number of symbols more than said fixed number of symbol memory circuits to store said symbols.

46. The programmable intelligent search memory of claim 45 further comprising one or more PRISM memory clusters comprising said plurality of programmable search engines, wherein said plurality of programmable search engines are organized in an array of rows and columns such that each said plurality of programmable search engines is addressable using a row address and a column address.

47. The FSA extension architecture of claim 46 further comprising row-wise FSA extension architecture to couple two or more of said plurality of programmable search engines in at least one said row of one of said PRISM memory clusters to support a regular expression that results in a finite state automaton with number of symbols greater than said fixed number of symbol memory circuits of one of said programmable search engines.

48. The FSA extension architecture of claim 46 further comprising column-wise FSA extension architecture to couple two or more of said plurality of programmable search engines in at least one said column of one of said PRISM memory clusters to support a regular expression that results in a finite state automaton with number of symbols greater than said fixed number of symbol memory circuits of one of said programmable search engines.

49. The FSA extension architecture of claim 46 further comprising row-wise and column-wise extension architecture to couple two or more of said plurality of programmable search engines in at least one said column or at least one said row or a combination of one said row and one said column of one of said PRISM memory clusters to support a regular expression that results in a finite state automaton with number of symbols greater than said fixed number of symbol circuits of one of said programmable search engines

50. The FSA extension architecture of claim 49 further comprising at least one of each of:

a. A group forward signal input to transfer a first state from one of said two or more FSAs;

b. A group forward signal output to transfer a second state out of one of said two or more FSAs;

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c. Global forwarding vector memory circuit to store column-wise state forwarding control coupled to said group forward input signal;

d. Local forwarding vector memory circuit to store a local FSA state forwarding control, said local FSA state forwarding control to enable the transfer of a local FSA state;

5 e. Up or down control vector memory circuit to store a transition enable control to enable a transfer of said group forward signal input for said first state to said local FSA state; and

f. Column state transition circuit coupling said global forwarding vector memory circuit, said local forwarding vector memory circuit, said local FSA state and said group forward
10 signal input to generate said group forward signal output.

g. Global state dependent vector memory circuit to store global state transition controls for enabling transition into a first state within one of said two or more programmable search engines from a second state external to said one of said two or more programmable search engines;

15 h. Global control vector memory circuit to store global out state transition control for enabling transition out of a third state within one of said two or more programmable search engines to a fourth state external to said one of said two or more programmable search engines;

i. Global transition logic circuit to couple said global control vector memory
20 circuit and at least one state of one of said two or more programmable search engines to at least one state external to said one of said two or more programmable search engines; and

j. Global control network circuit to couple said global transition logic circuit and said global state dependent vector memory circuit to perform transition into said first state or the fourth state of said one of said two or more programmable search engines from said second
25 state or said third state within a second programmable search engine of said two or more programmable search engines.

51. The FSA extension architecture of claim 49 further comprising rule group FSA extension architecture to enable creation of a plurality of groups of regular expression rules from said plurality of regular expressions and to perform state transition from one regular expression

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of a first group to at least one regular expression of a second group of said plurality of regular expressions.

52. The rule group FSA extension architecture of claim 51 further comprising at least one of each of:

5 a. rule group transition logic to perform transition into one of said second group of said regular expressions ;

b. rule group control vector to control transition into one of said second group of said regular expressions;

10 c. external state vector out to transfer a state of said second group of regular expressions and

d. external state vector to couple the state of said first group of regular expressions to said second group of said regular expressions;

53. A memory architecture comprising programmable intelligent search memory for content search wherein said programmable intelligent search memory performs regular
15 expression based and signature pattern based search and said programmable intelligent search memory is embedded in a processor.

54. A hardware processor comprising at least one integrated circuit chip processor, said integrated circuit chip processor comprising programmable intelligent search memory for content search, wherein said programmable intelligent search memory performs regular
20 expression based search and signature pattern based.

55. A multi-processor system comprising at least one integrated circuit chip processor and further comprising at least one other integrated circuit chip comprising programmable intelligent search memory for content search, wherein said programmable intelligent search memory performs regular expression based search and signature pattern
25 based.

56. Hardware processor of claim 54 further comprising

a. At least one integrated circuit microprocessor for central processing unit function of said hardware processor;

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b. At least one chipset integrated circuit chip coupled to a memory chip, said chipset for controlling the flow of data in said hardware processor and said memory chip for system memory use of said hardware processor;

5 c. At least one adapter card for coupling said hardware processor to at least one system other than said hardware processor wherein said at least one adapter card is coupled to said at least one chipset; and

d. At least one content search accelerator card to accelerate content search applications running on said hardware processor, said at least one content search accelerator card comprising said integrated circuit chip processor comprising said programmable intelligent search memory to offload and accelerate content search functions from said at least one integrated circuit microprocessor.

57. A memory architecture comprising programmable intelligent search memory for content search wherein said programmable intelligent search memory comprises a context switch architecture and performs regular expression based search, said content comprising a plurality of sessions or flows or streams or the like forming a plurality of content search contexts for said programmable intelligent search memory, said context switch architecture to load or store at least one of said plurality of content search contexts to or from said programmable intelligent search memory.

58. An integrated circuit chip comprising programmable intelligent search memory for content search wherein said programmable intelligent search memory comprises a context switch architecture and performs regular expression based search, said content comprising a plurality of sessions or flows or streams or the like forming a plurality of content search contexts for said programmable intelligent search memory, said context switch architecture to load or store at least one of said plurality of content search contexts to or from said programmable intelligent search memory.

59. In a hardware processor comprising an integrated circuit chip memory said integrated circuit chip memory comprising programmable intelligent search memory for content search, wherein said programmable intelligent search memory comprises a context switch architecture and performs regular expression based search, said programmable intelligent search memory (PRISM) further comprising: a) a PRISM controller to control the flow of said content through PRISM; b) a plurality of programmable search engines to perform search using

- a plurality of regular expressions; c) at least one context memory to store a plurality of contexts of said programmable search engines; d) a cluster FSA controller to control a group of said plurality of programmable search engines; and e) an external memory controller coupled to a memory external to said integrated circuit chip; said plurality of regular expressions converted
- 5 into plurality of finite state automata to program in said plurality of programmable search engines, said content comprising a plurality of sessions or flows or streams or the like forming a plurality of content search contexts for said programmable intelligent search memory, said context switch architecture to load or store at least one of said plurality of content search contexts to or from said programmable intelligent search memory, the process of performing
- 10 content search on said content and further performing context switch for inspecting first data stream from said content belonging to a first flow or session or stream different from a second data stream from said content belonging to a second flow or session or stream with its context loaded in said plurality of programmable search engines, said process comprising:
- a. said PRISM controller receiving said first data stream of said content
 - 15 belonging to said first flow or session or stream;
 - b. said PRISM controller identifying the session or flow or stream of said first data stream;
 - c. said PRISM controller identifying if the context of said first data stream is different from the context of said second data stream;
 - 20 d. if said first data stream and said second data stream are from different contexts said PRISM controller coupled to said cluster FSA controller determining the location of the context of said first data stream in said at least one context memory or said external memory and retrieving said context for said first data stream;
 - e. said cluster FSA controller coupled to said programmable search engines
 - 25 storing the context for said second data stream present in said programmable search engines that have a plurality of states that need to be stored;
 - f. said cluster FSA controller loading said retrieved context for said first data stream in said plurality of programmable search engines; or
 - g. said cluster FSA controller coupling with said PRISM controller directing the
 - 30 flow of said first data stream to said plurality of programmable search engines for content

inspection once said plurality of programmable search engines are loaded with the context of said first data stream;

5 60. An integrated circuit chip comprising programmable intelligent search memory for content search wherein said programmable intelligent search memory performs regular expression based search and comprises of a plurality of programmable memory clusters for programming rules for said content search, said programmable memory clusters further comprising plurality of programmable search engines to perform search using a plurality of regular expressions on input content, said plurality of regular expressions converted into functionally equivalent plurality of finite state automata to program in said plurality of
10 programmable search engines.

 61. The PRISM memory clusters of claim 60 further comprising FSA controller to program said plurality of regular expressions in said plurality of programmable search engines, wherein at least two groups of said PRISM memory clusters are programmed with said content search rules for at least one application for examining said input content, said input content
15 comprising plurality of packets or flows or data streams to be examined, at least one of said packets or flows or data streams presented to first set of said two groups of PRISM memory clusters and at least one additional of said packets or flows or data streams presented to second set of said group of PRISM memory clusters for content examination using said content search rules for said at least one application achieving an increase in the content search
20 performance by a multiple of the number of sets of said PRISM memory clusters programmed with the same said content search rules used to perform said content search.

 62. The PRISM memory clusters of claim 60 further comprising FSA controller to program said plurality of regular expressions in said plurality of programmable search engines, wherein a first PRISM memory cluster is programmed with content search rules for one
25 application and a second PRISM memory cluster is programmed with content search rules for a second application, said programmable intelligent search memory further comprising circuits to put said PRISM memory clusters in a power down mode, said power down mode for putting at least one of said PRISM memory clusters in a low power consumption mode when said input content comprises of data for said first application while rules for said second application are
30 programmed in said at least one of PRISM memory cluster, said power down mode used for creating a low power programmable intelligent search memory.

Regular Expression: $(xy + y)*yx$

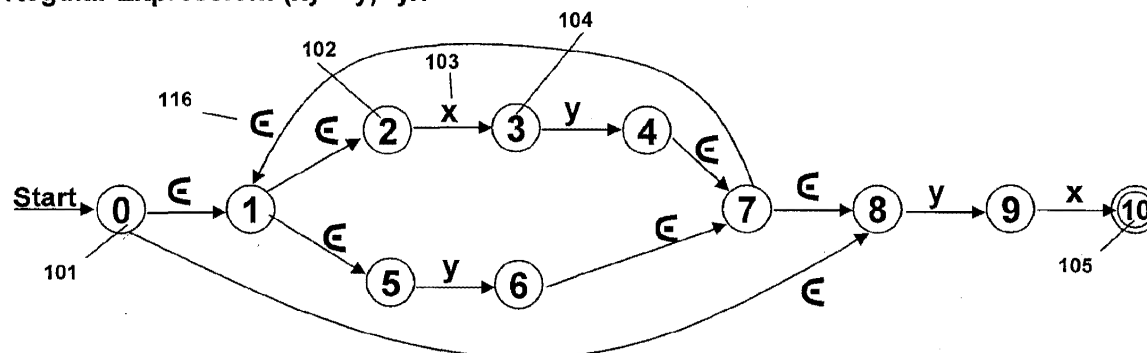


Fig. 1a Thompson's NFA (Prior Art)

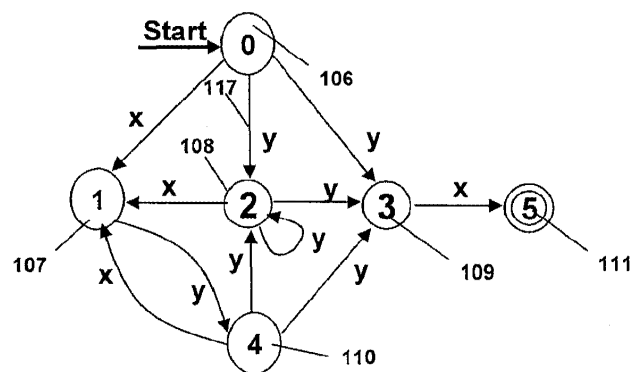
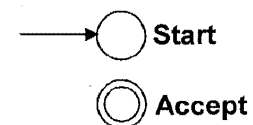


Fig. 1b Berry-Sethi NFA (Prior Art)

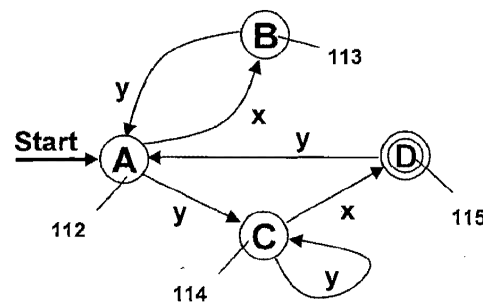


Fig. 1c DFA (Prior Art)

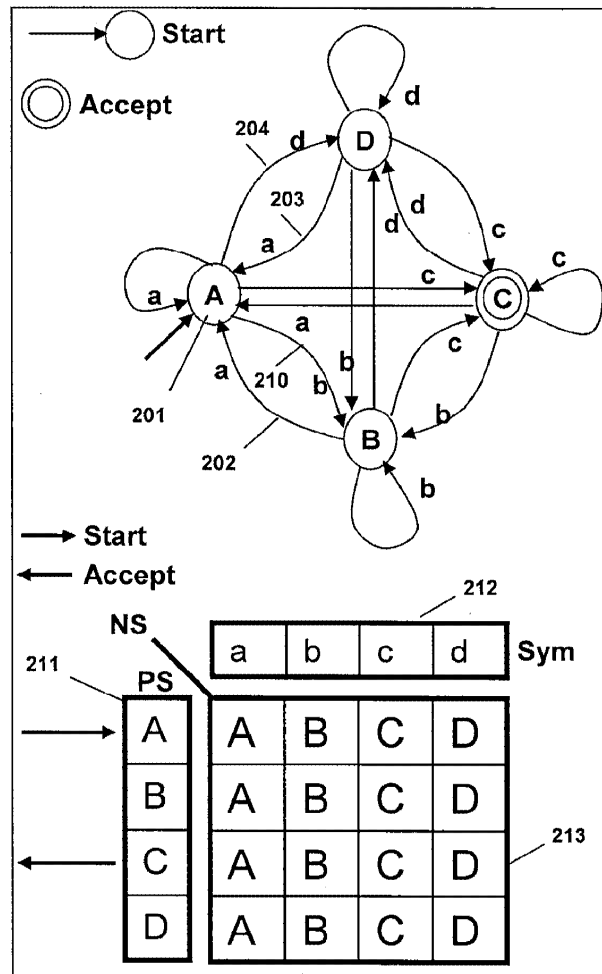


Fig. 2a A Left-biased NFA & State Transition Table (Prior Art)

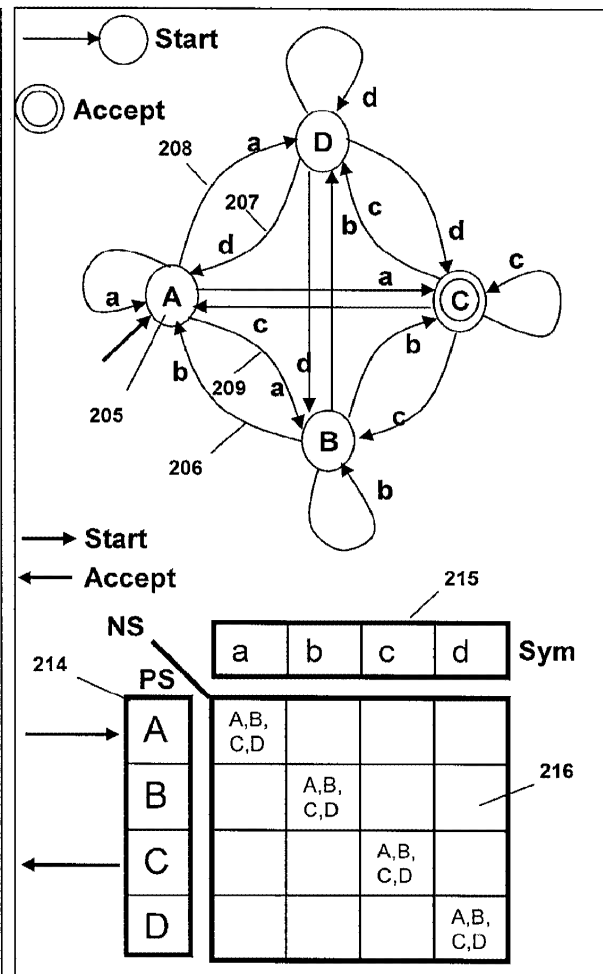


Fig. 2b A Right-biased NFA & State Transition Table (Prior Art)

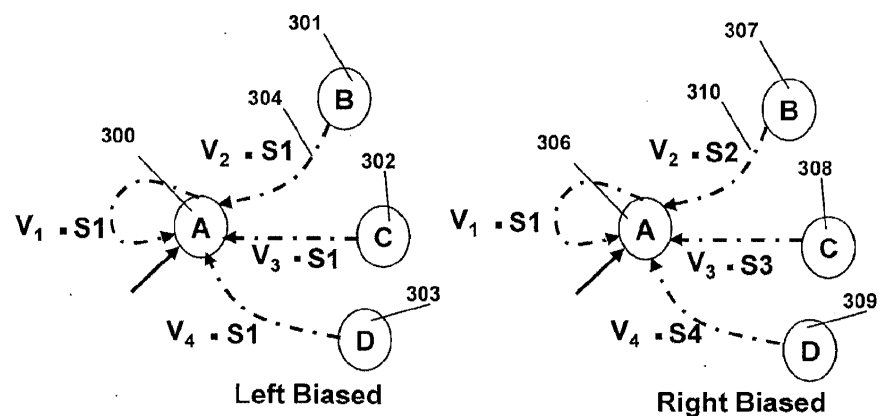


Fig. 3a State Transition Controls

NS = A	PS	Sym	SDV
311	A	S1	V_1
	B	S1	V_2
	C	S1	V_3
	D	S1	V_4
	Left Biased		

NS = A	PS	Sym	SDV
312	A	S1	V_1
	B	S2	V_2
	C	S3	V_3
	D	S4	V_4
	Right Biased		

State Prop: LB, RB, SDV, Start, Accept, Action
Fig. 3b Configurable Next State Table per State

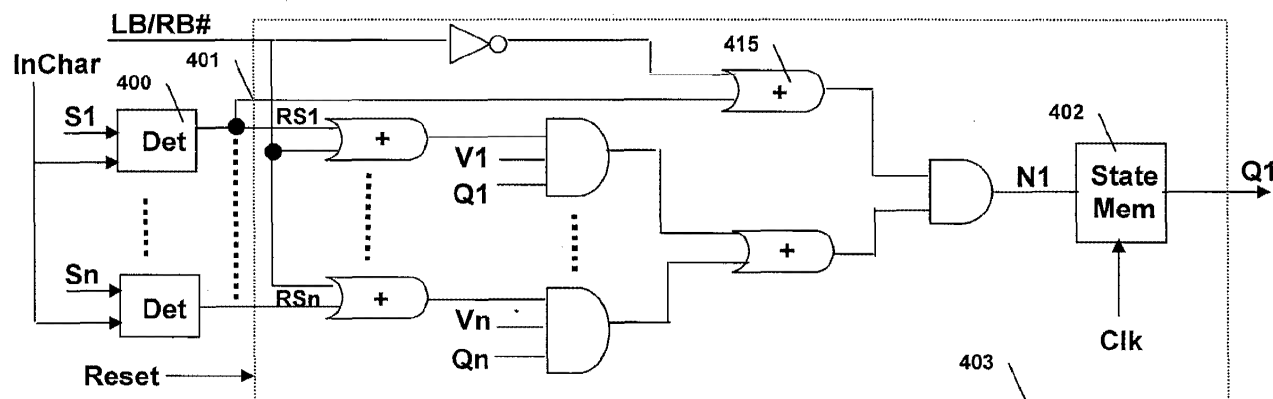


Fig. 4a State transition logic (STL) for a state

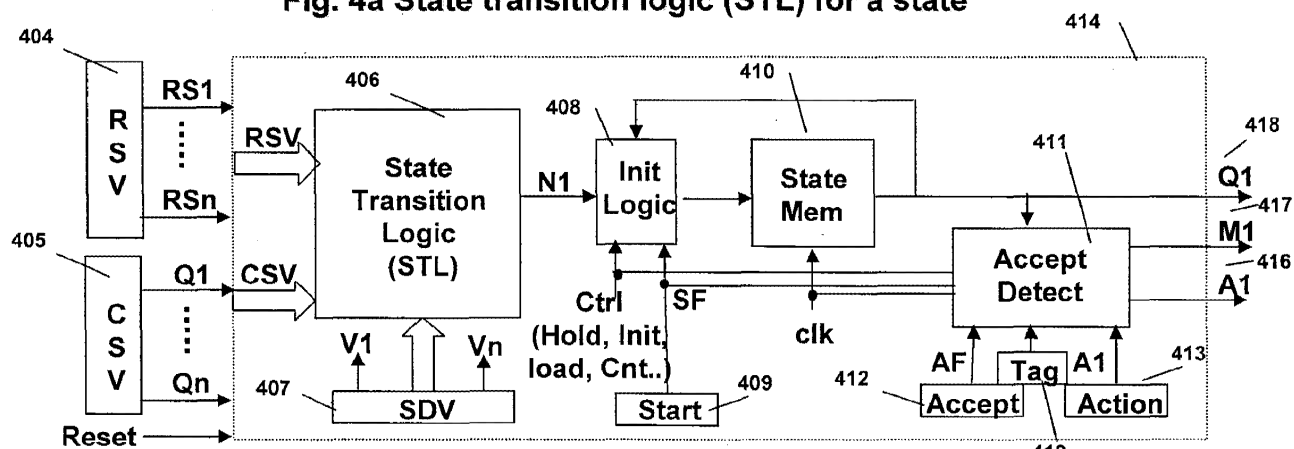


Fig. 4b A State Logic Block

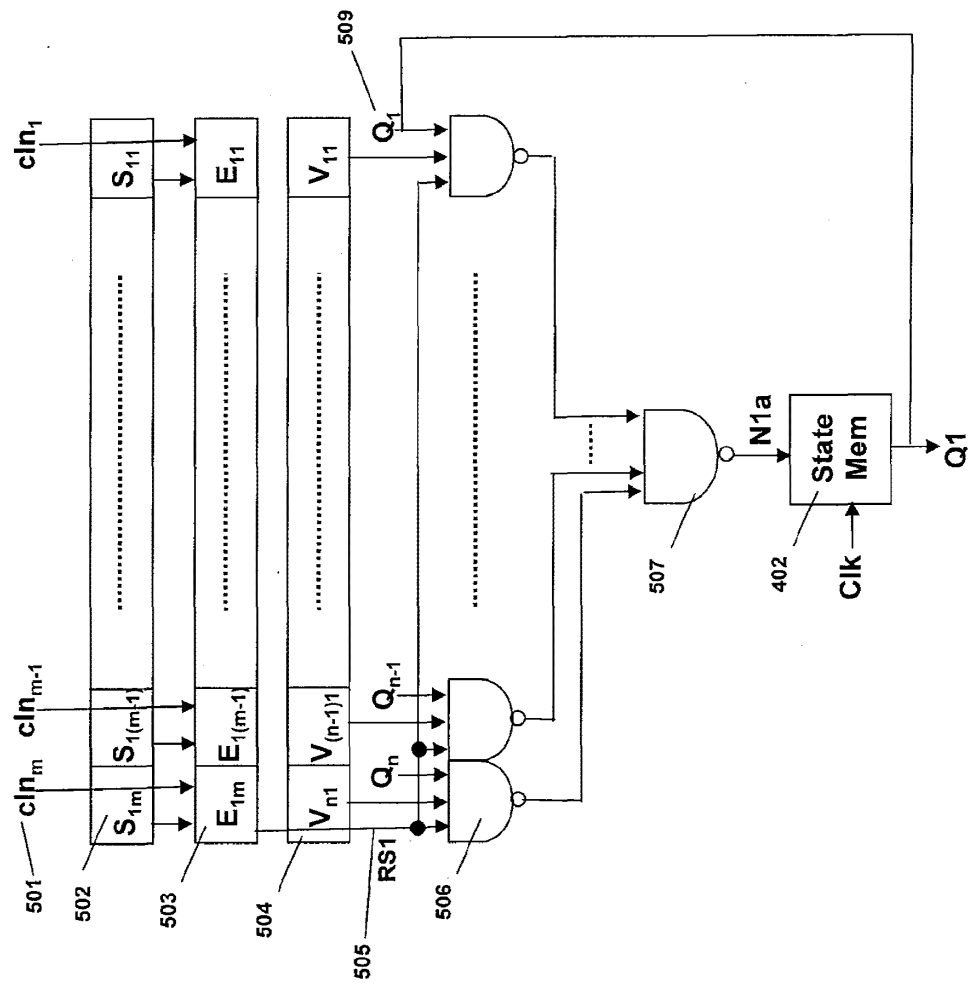


Fig. 5a State transition logic (STL) for a state in Left-biased FSA

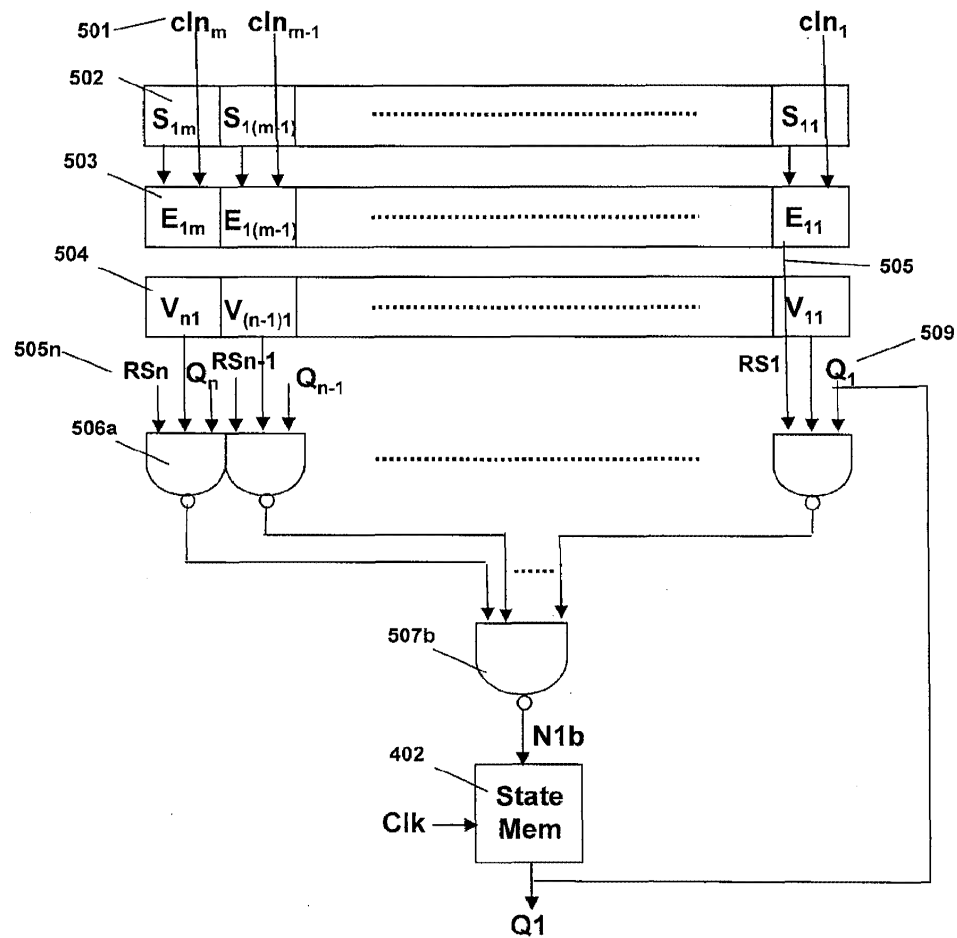
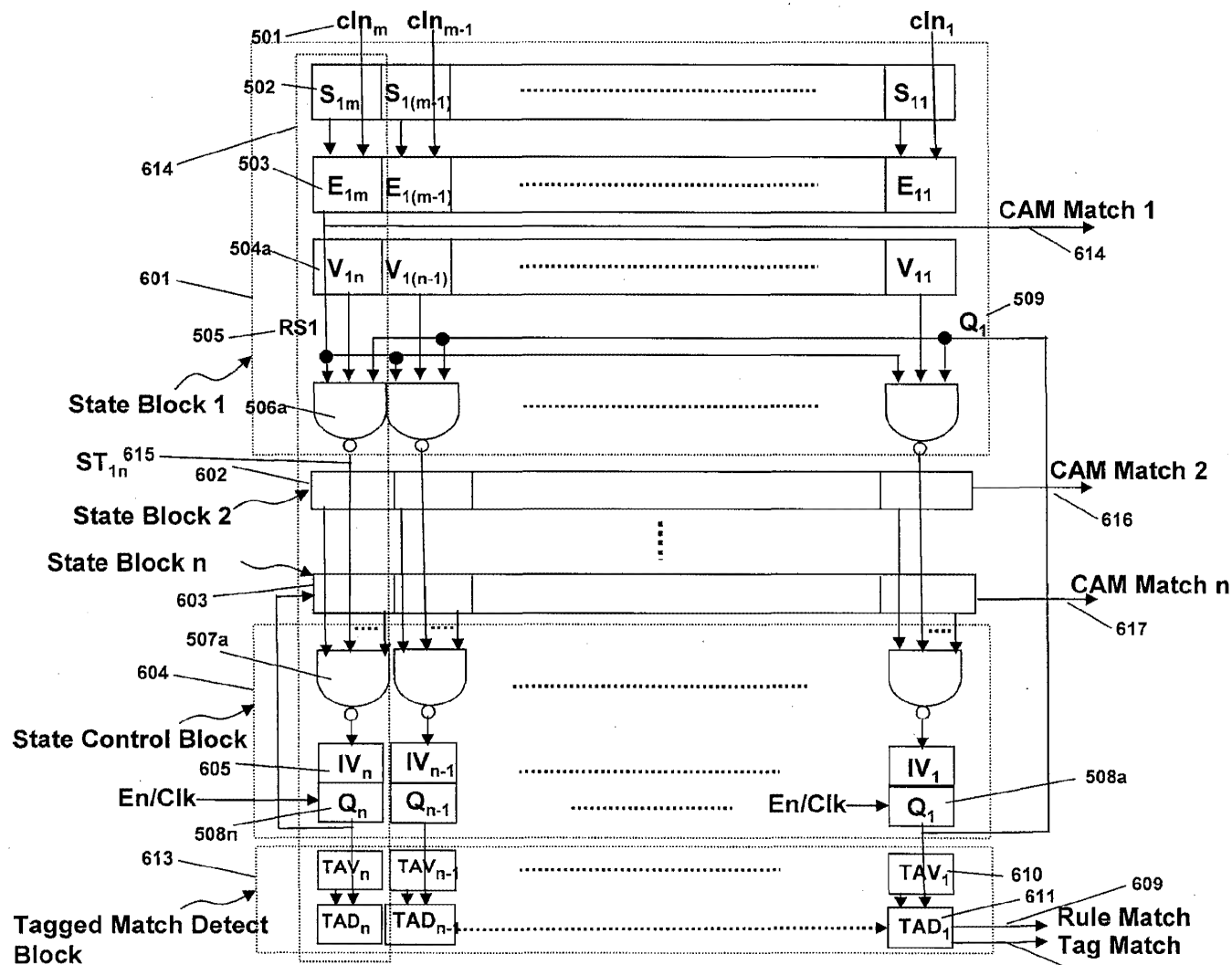
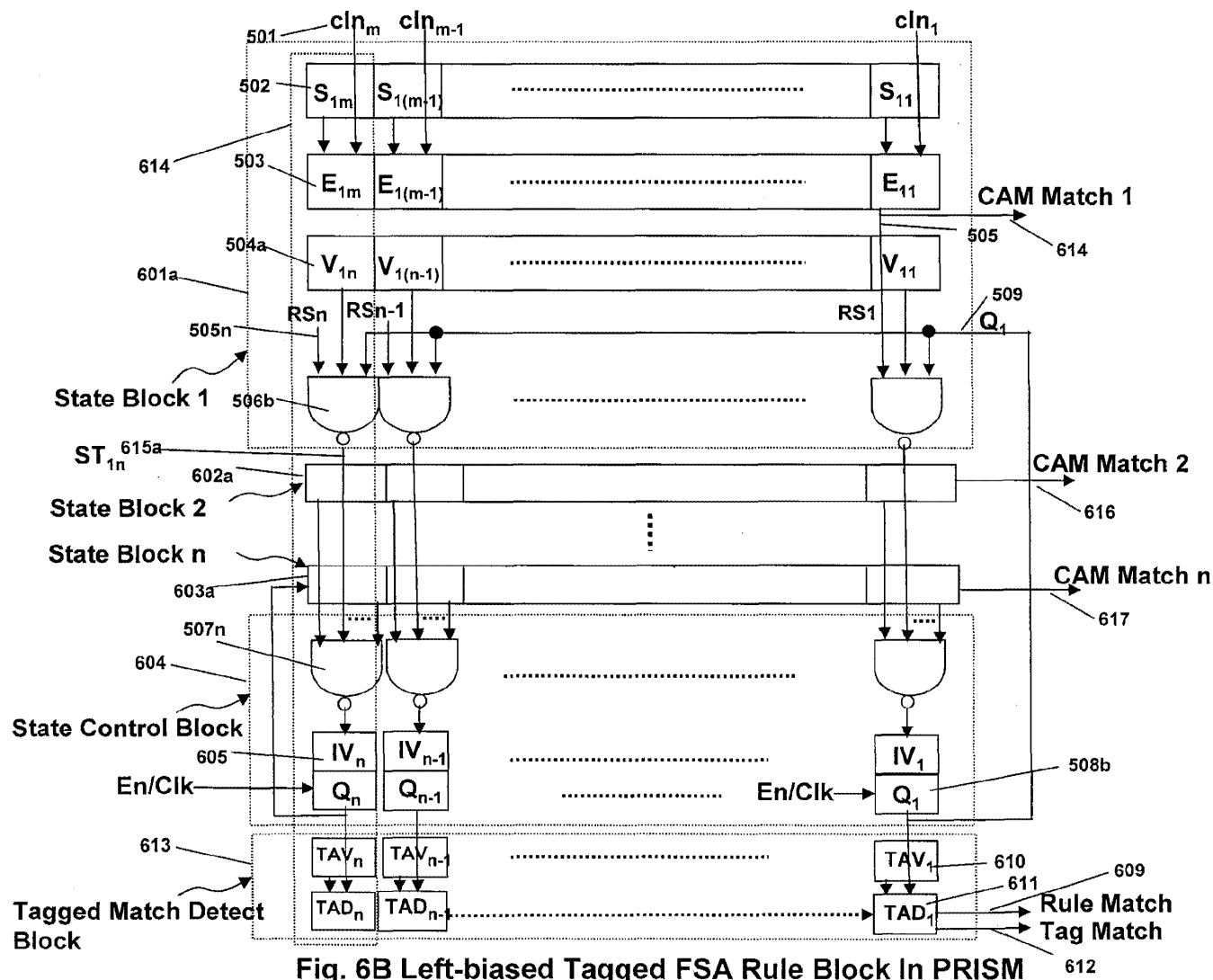


Fig. 5b State transition logic (STL) for a state in Right-biased FSA





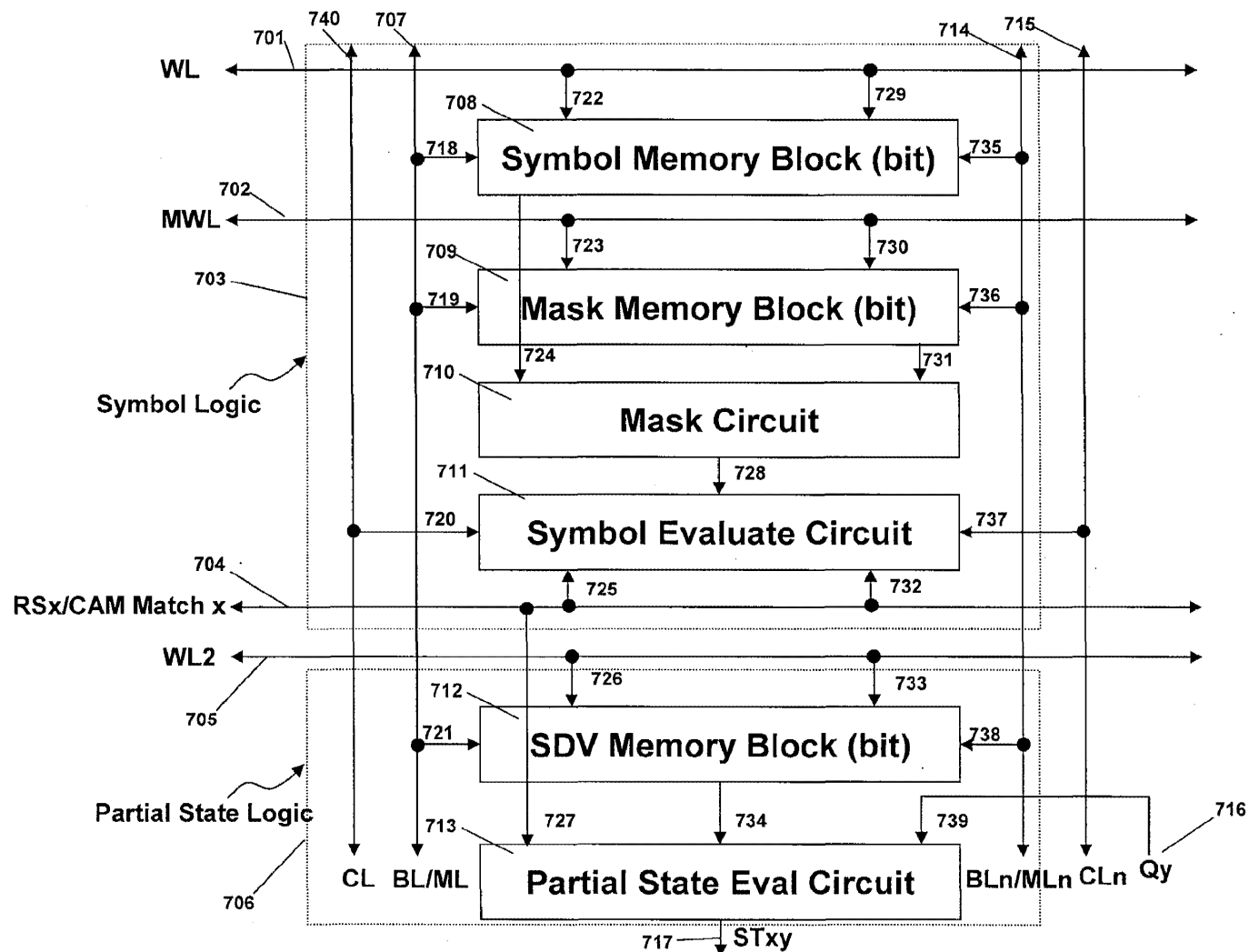


Fig. 7A State Block Bit In PRISM

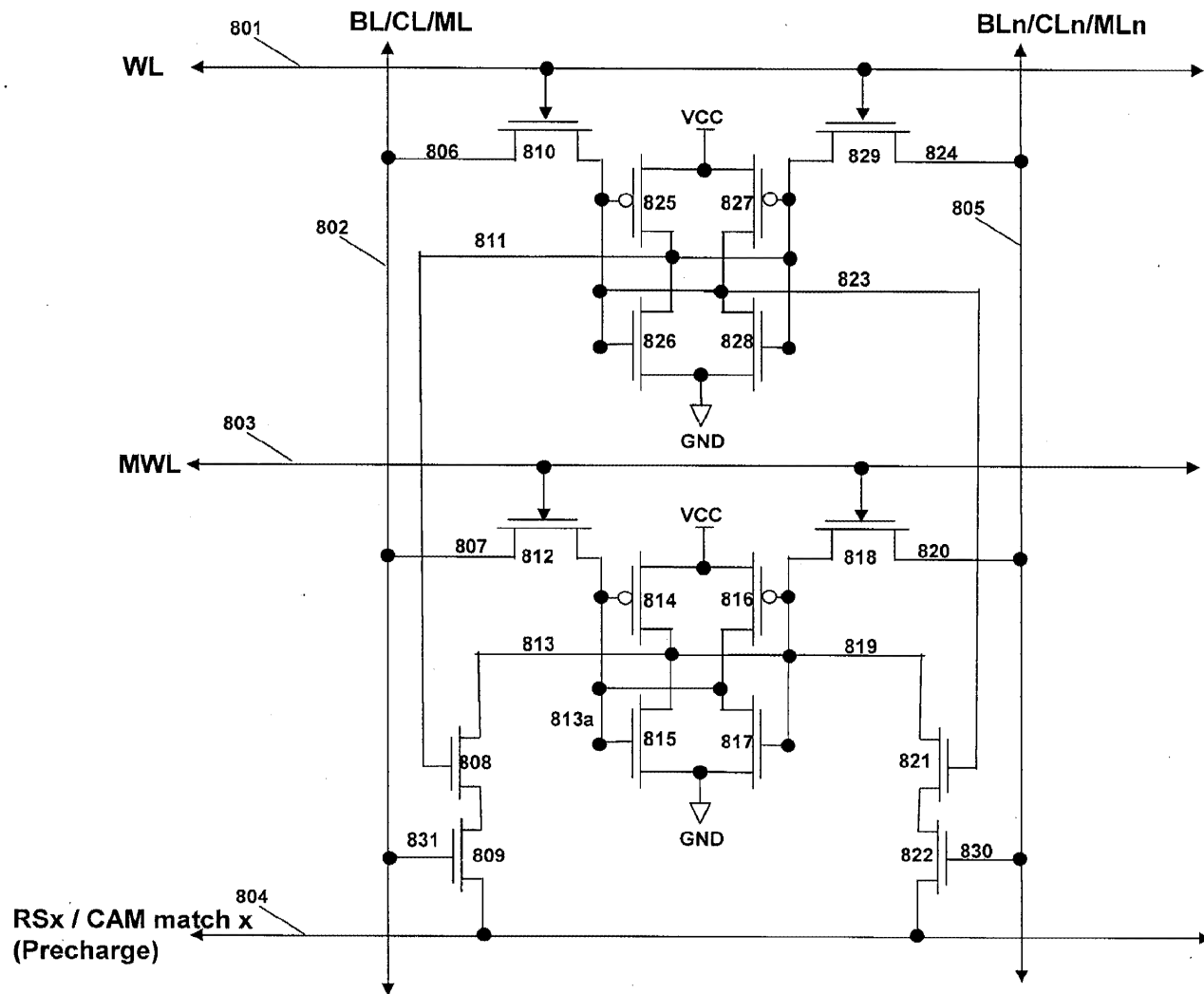


Fig. 8A Symbol Logic Bit in PRISM

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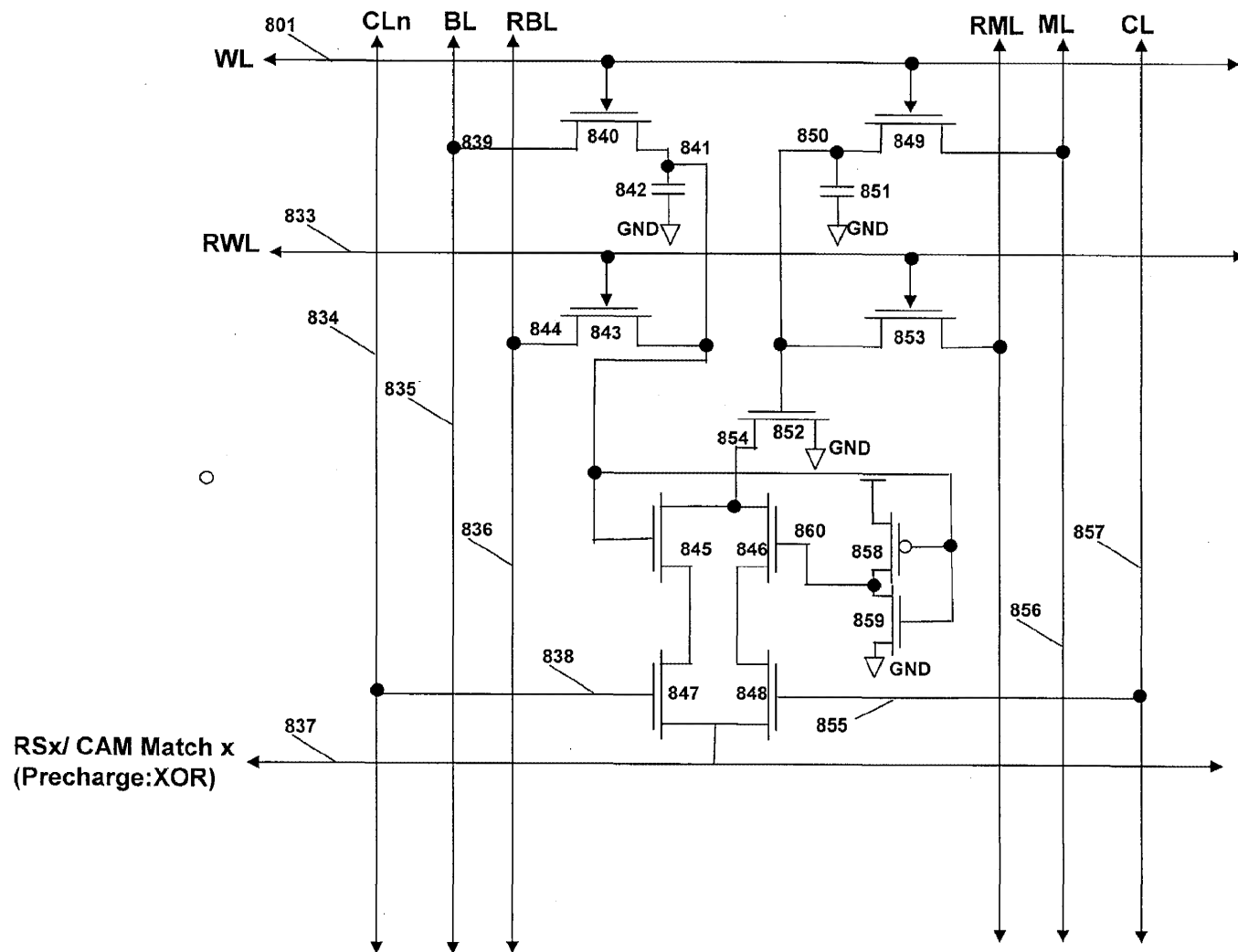


Fig. 8B Symbol Logic Bit in PRISM (DRAM based with independent Refresh port)

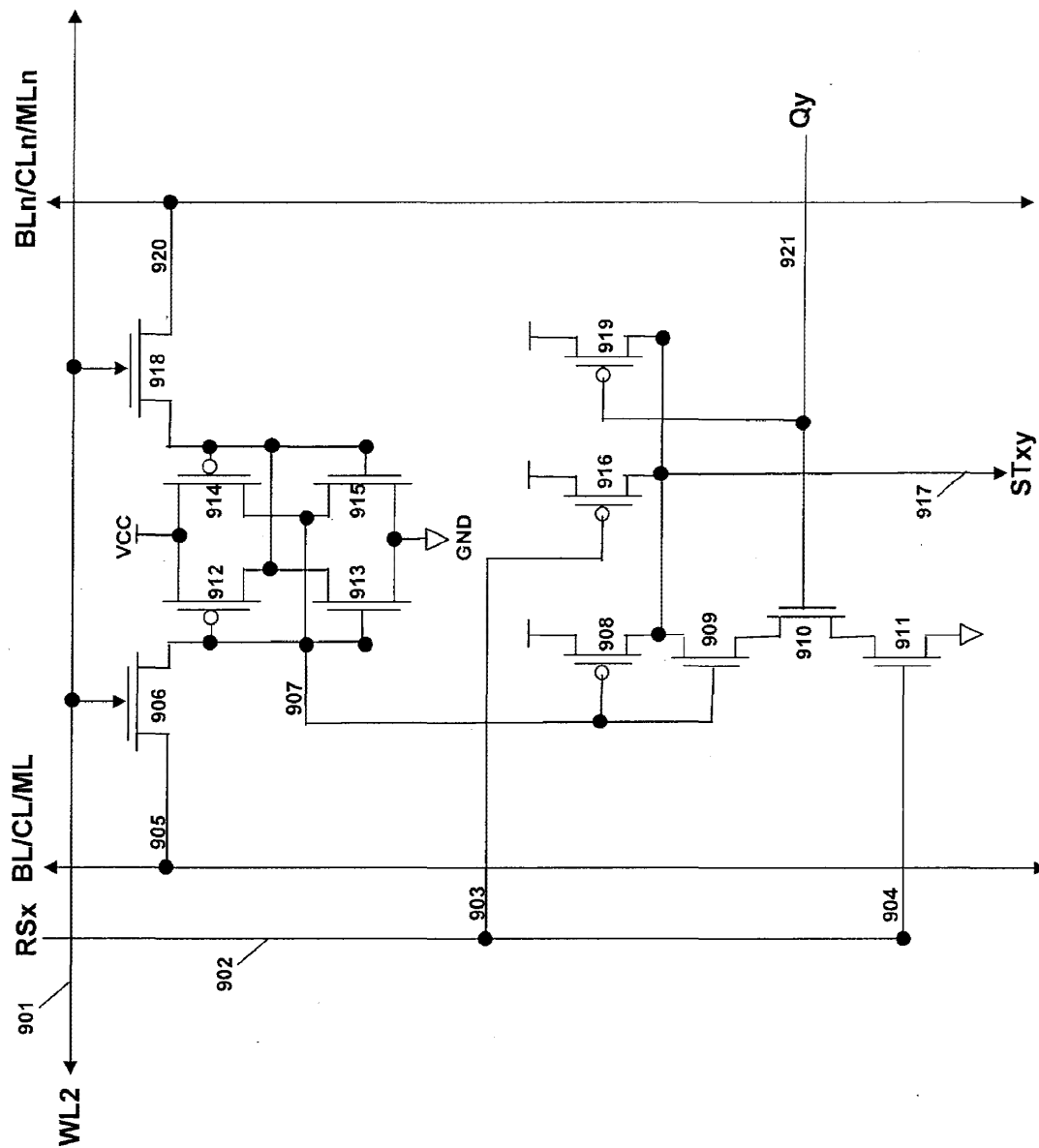


Fig. 9 Partial State Logic Bit in PRISM

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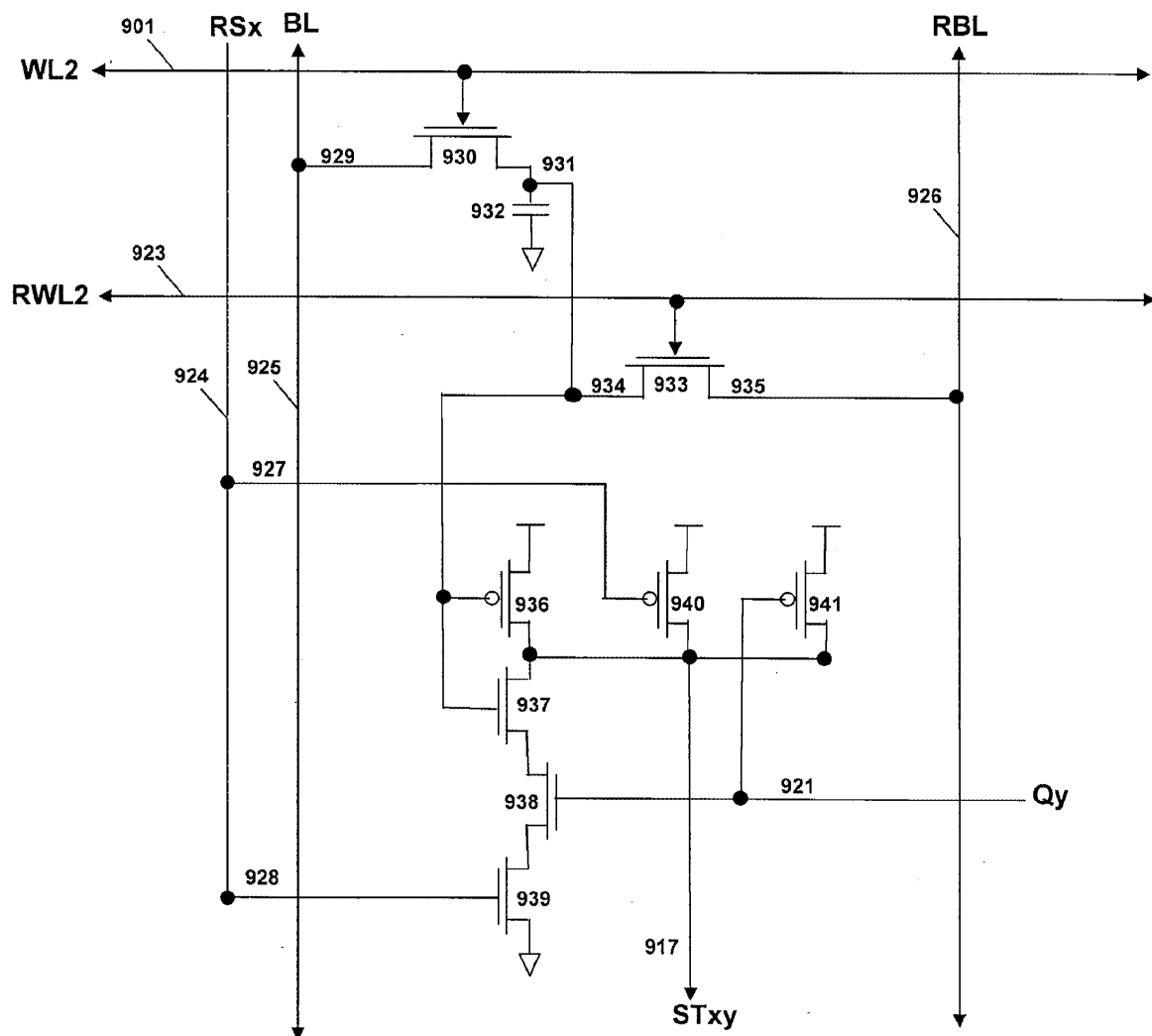


Fig. 9A Partial State Logic Bit in PRISM (DRAM based with refresh port)

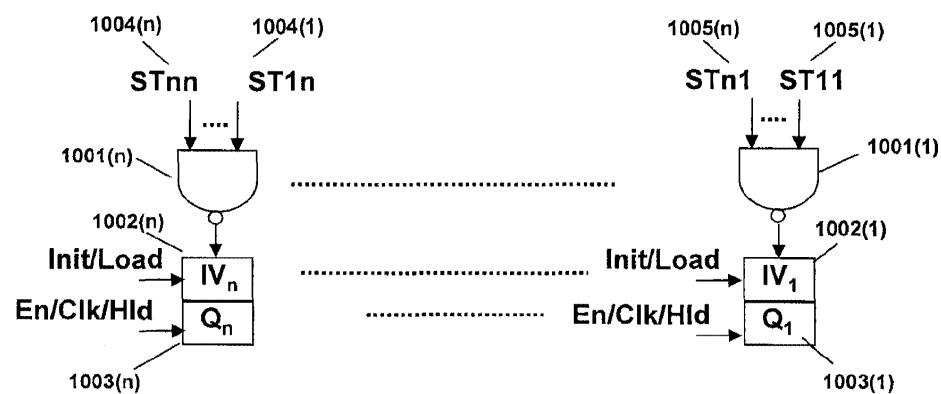


Fig. 10a State Control Block in PRISM

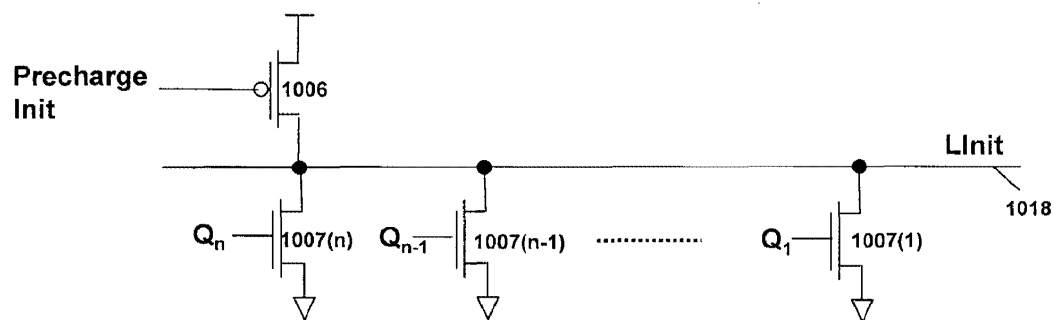


Fig. 10b Local Init Detect Circuit in PRISM

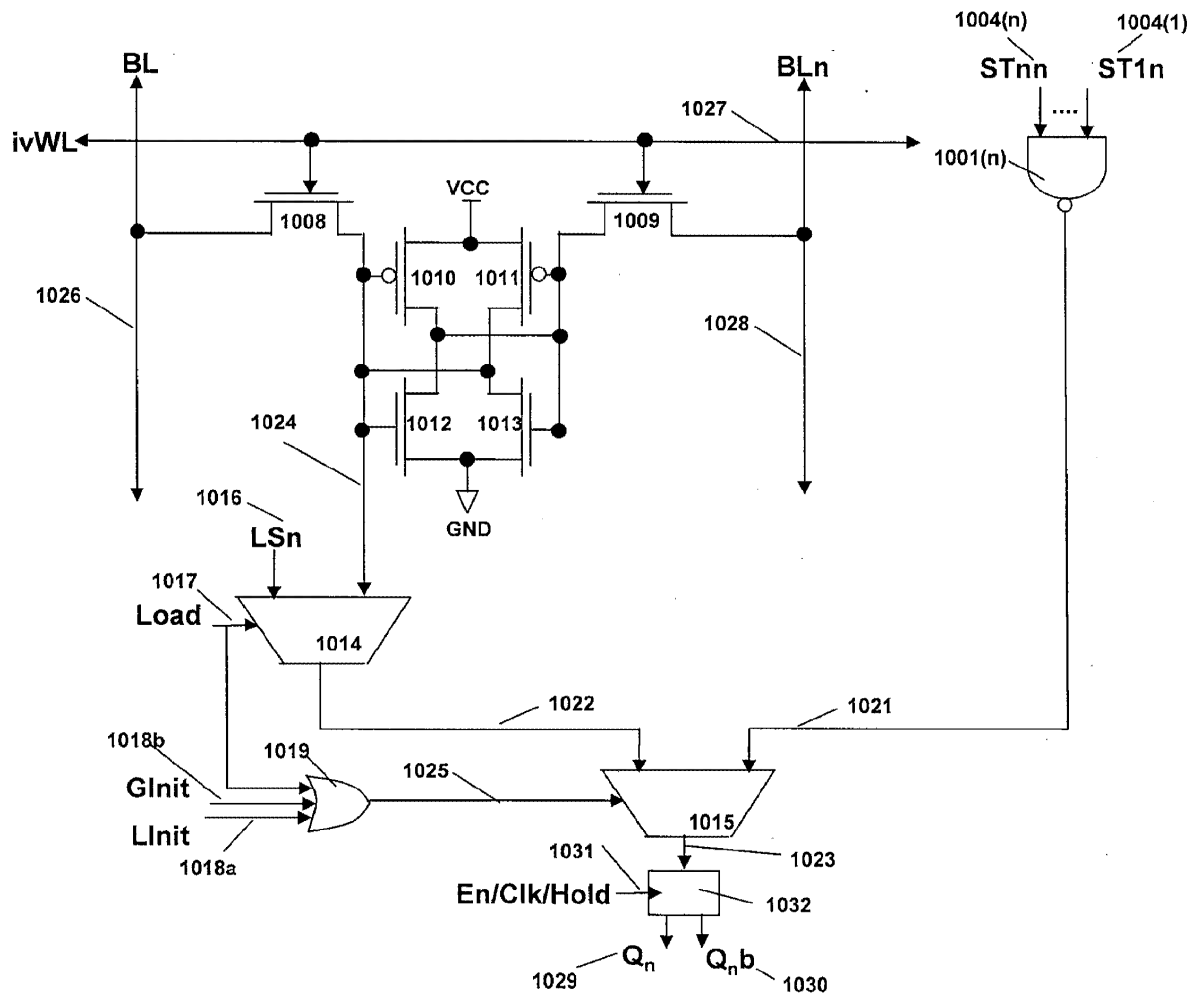


Fig. 10c State Control Block Bit in PRISM

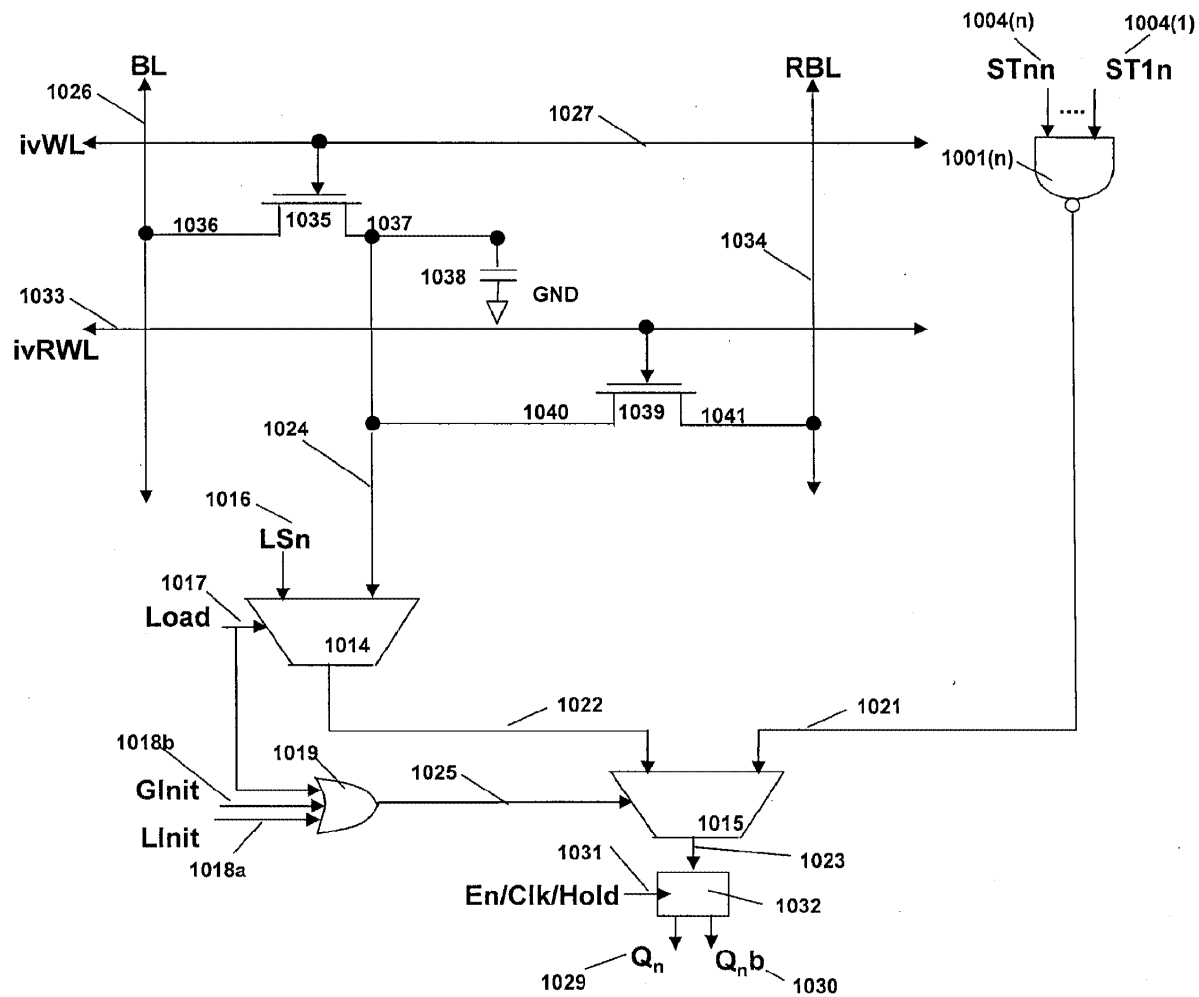
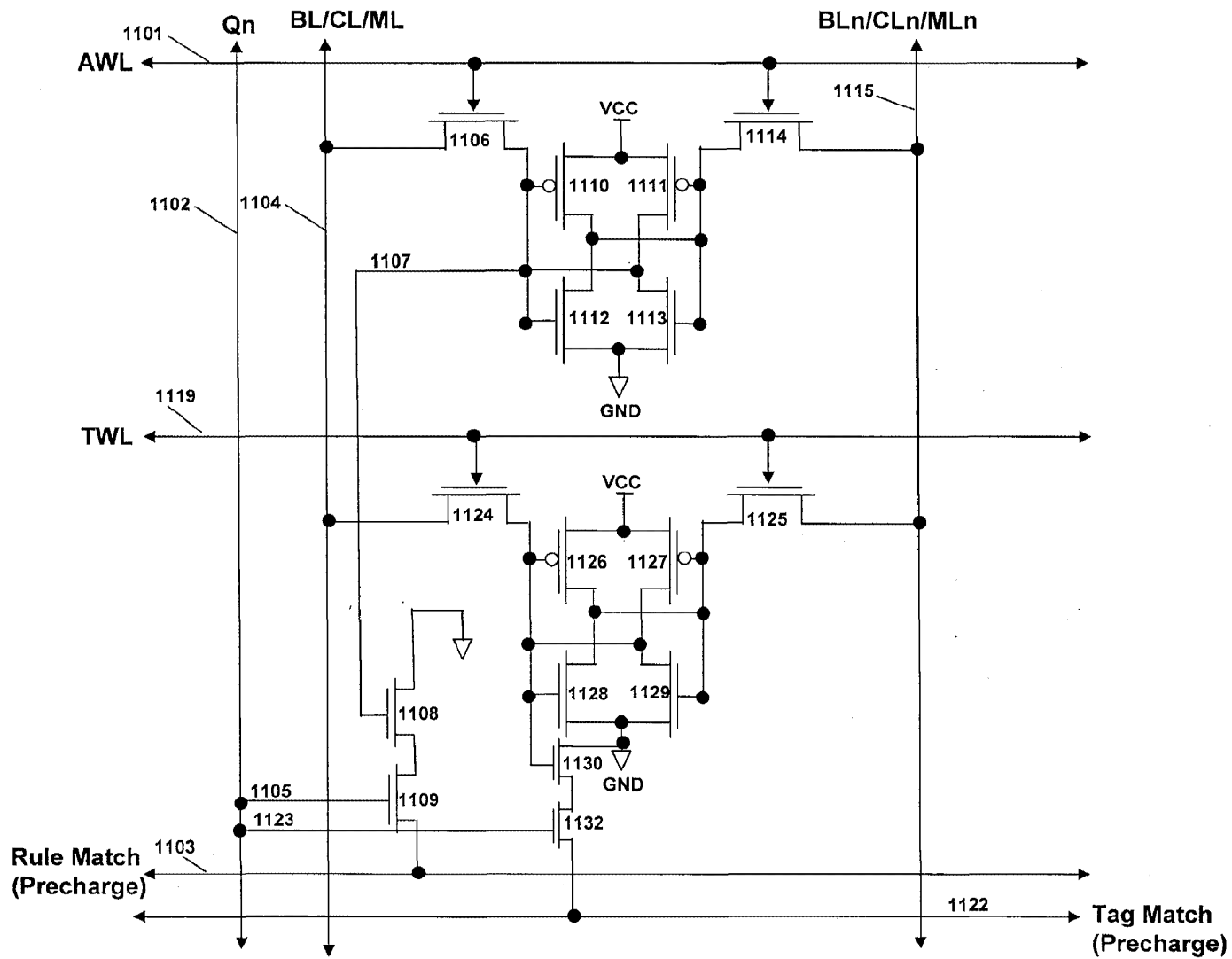


Fig. 10d State Control Block Bit in PRISM (DRAM based)



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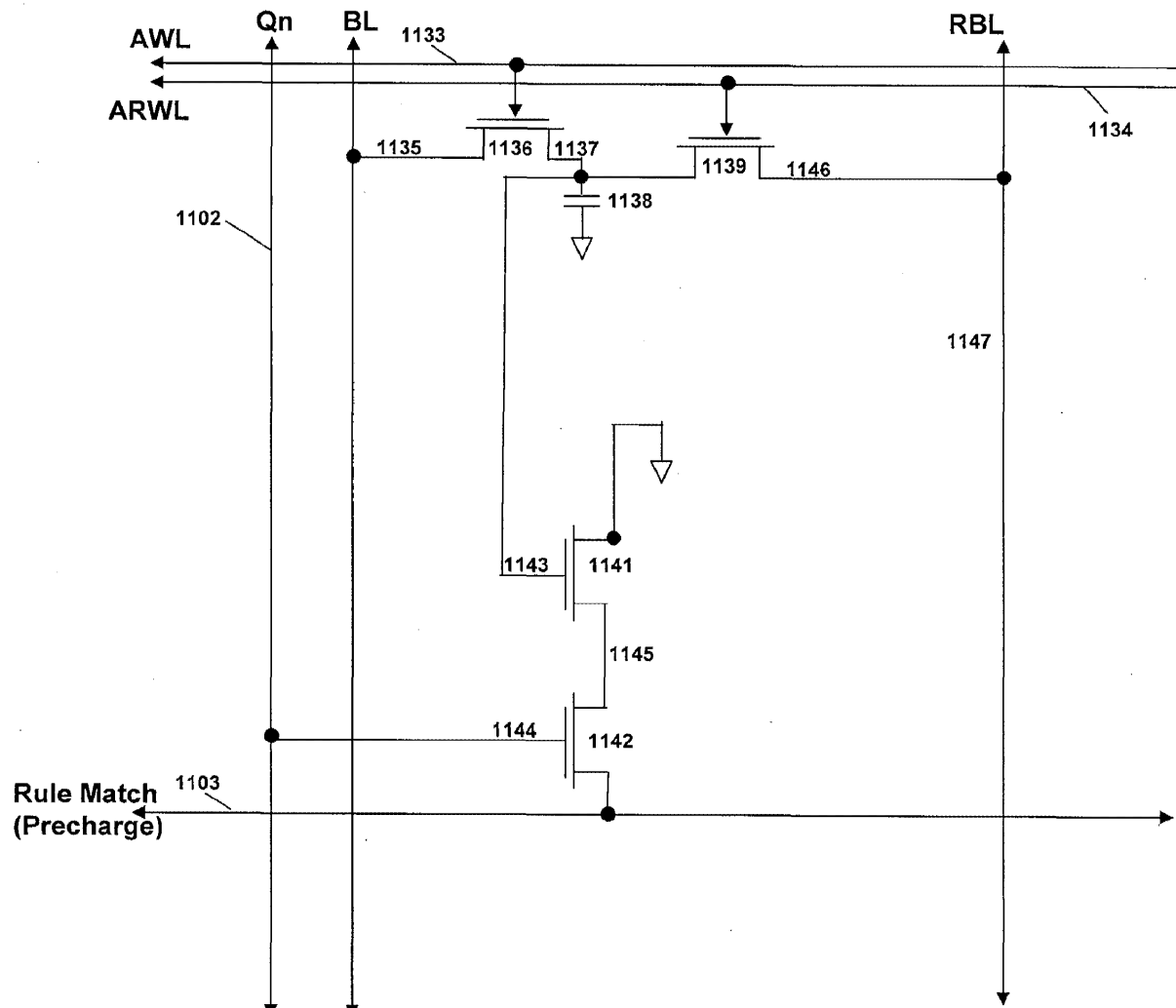


Fig. 11A Match Detect Block bit in PRISM (DRAM based)

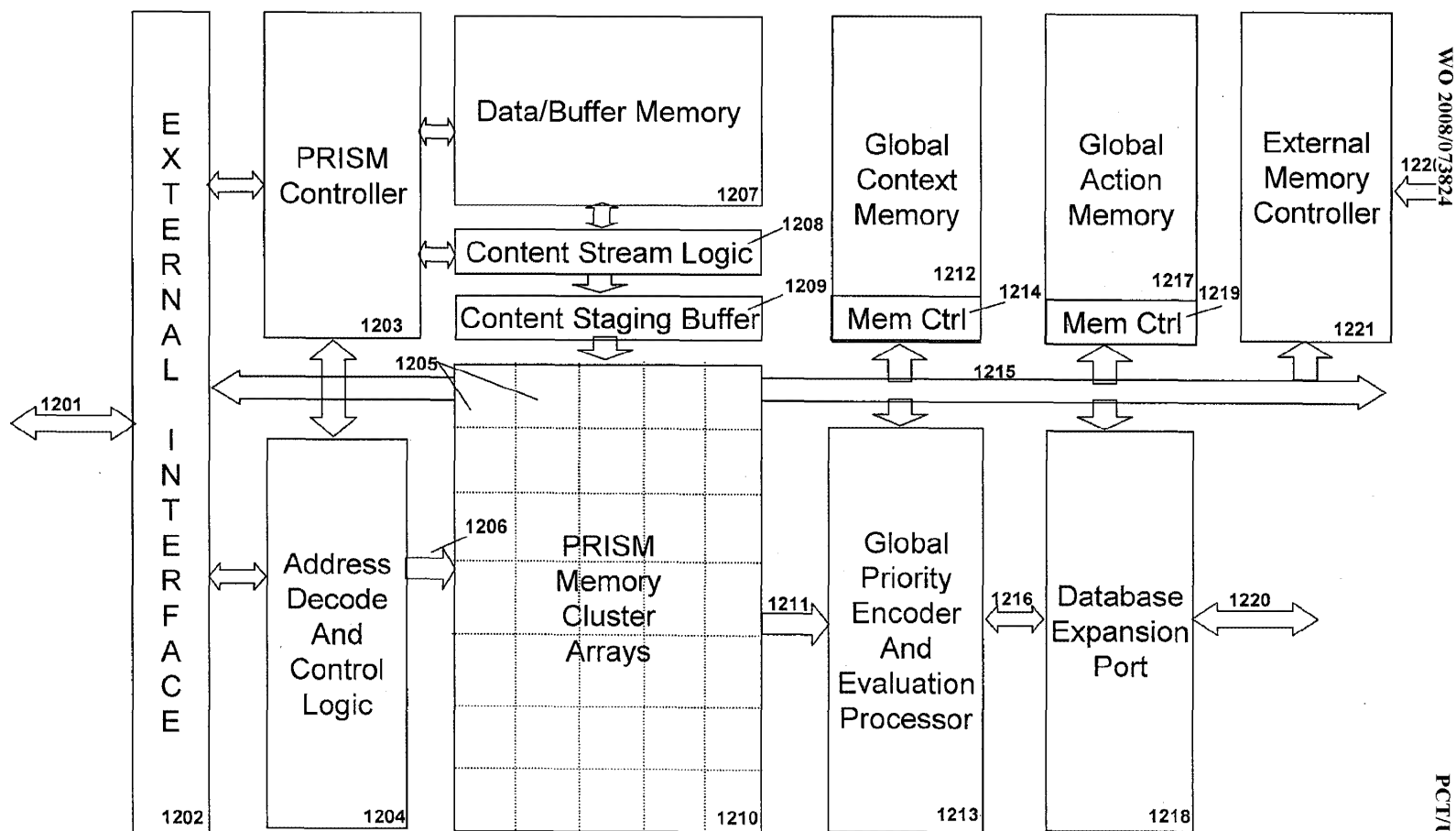


Fig. 12 PRISM Block Diagram

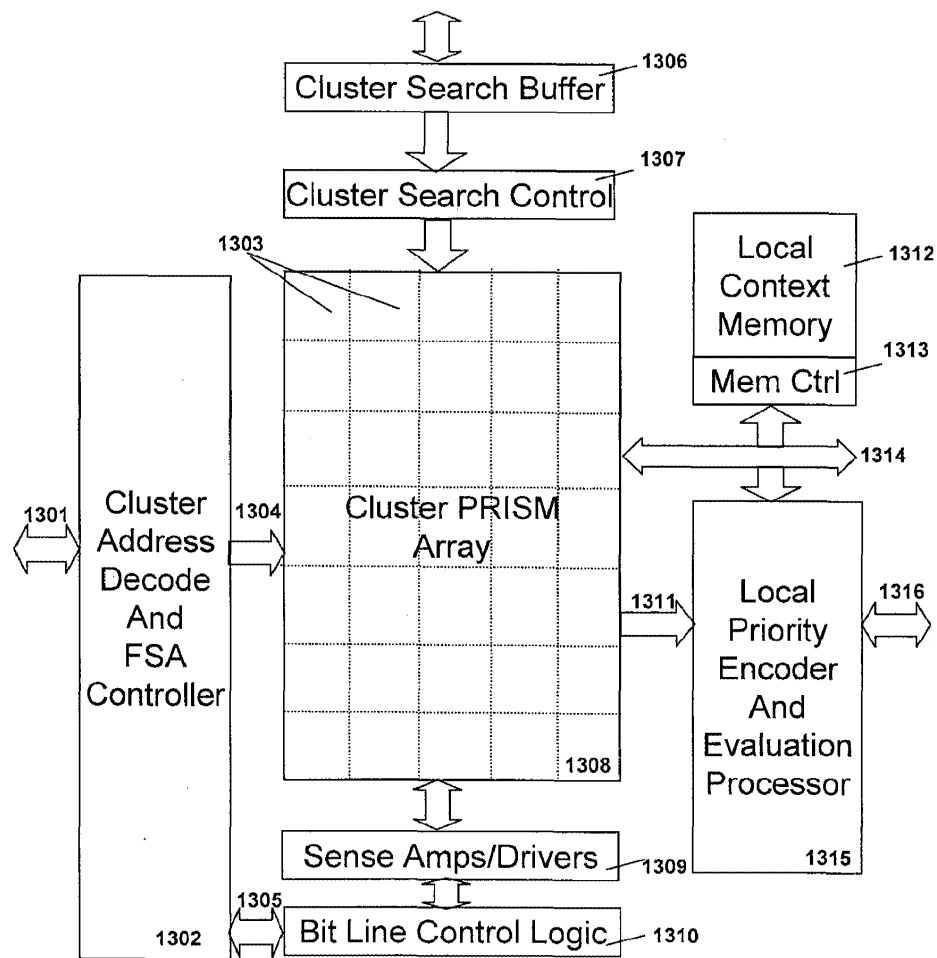
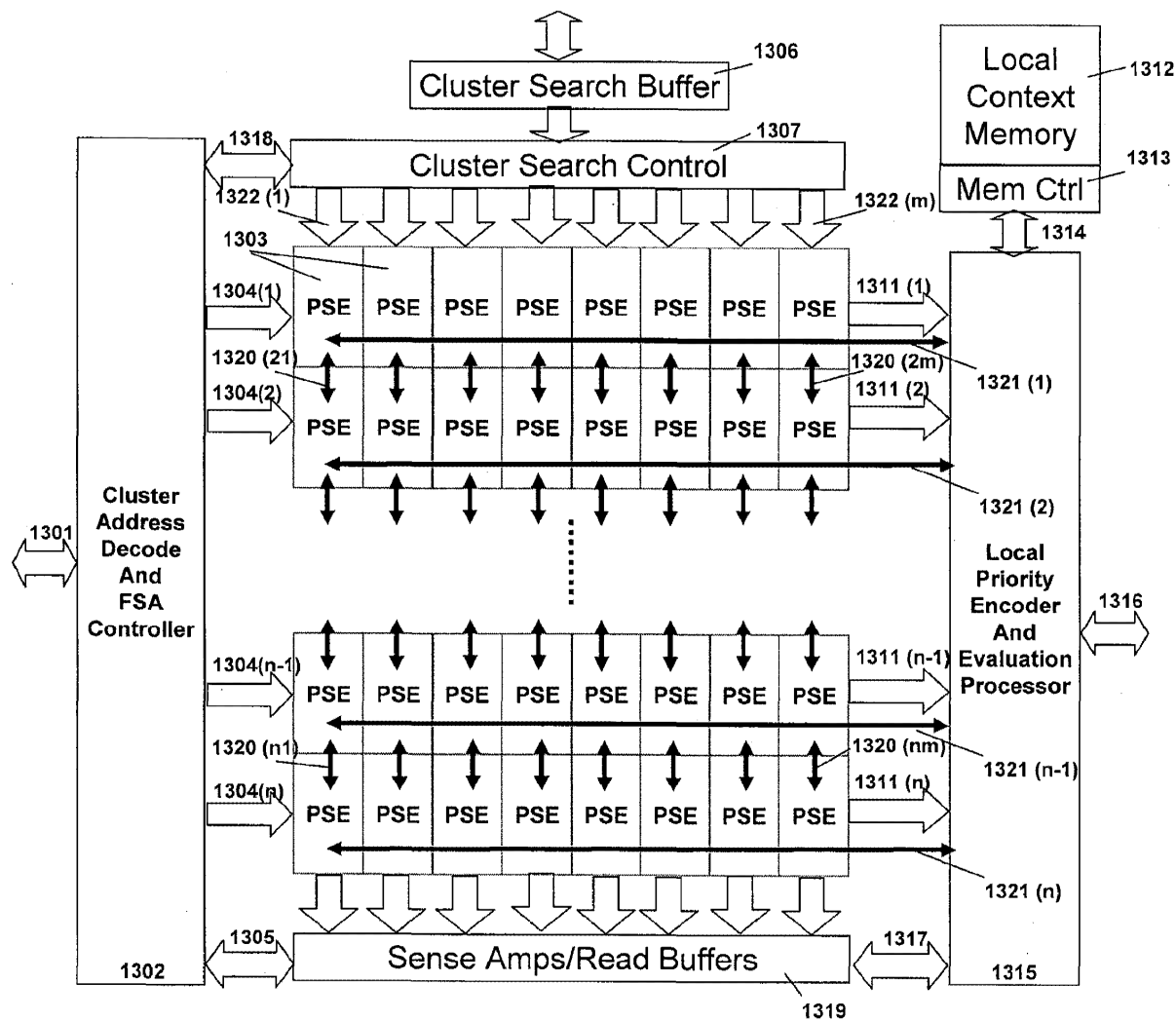


Fig. 13a PRISM Memory Cluster Block Diagram



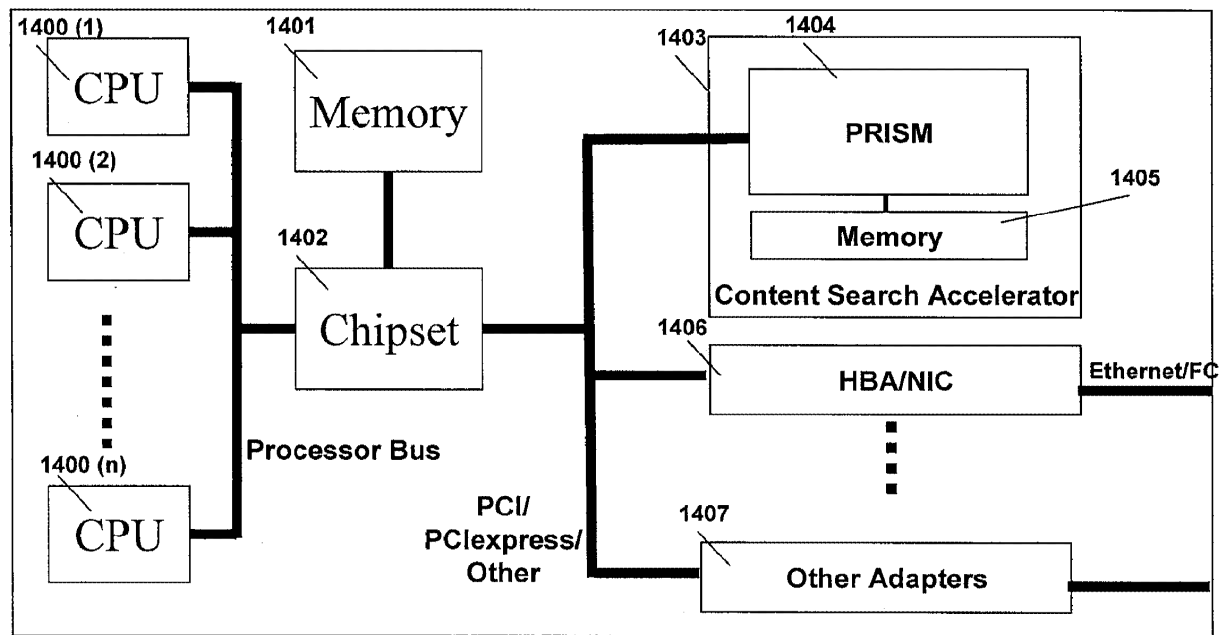


Fig. 14 Computing Device with Content Search Memory Based Accelerator

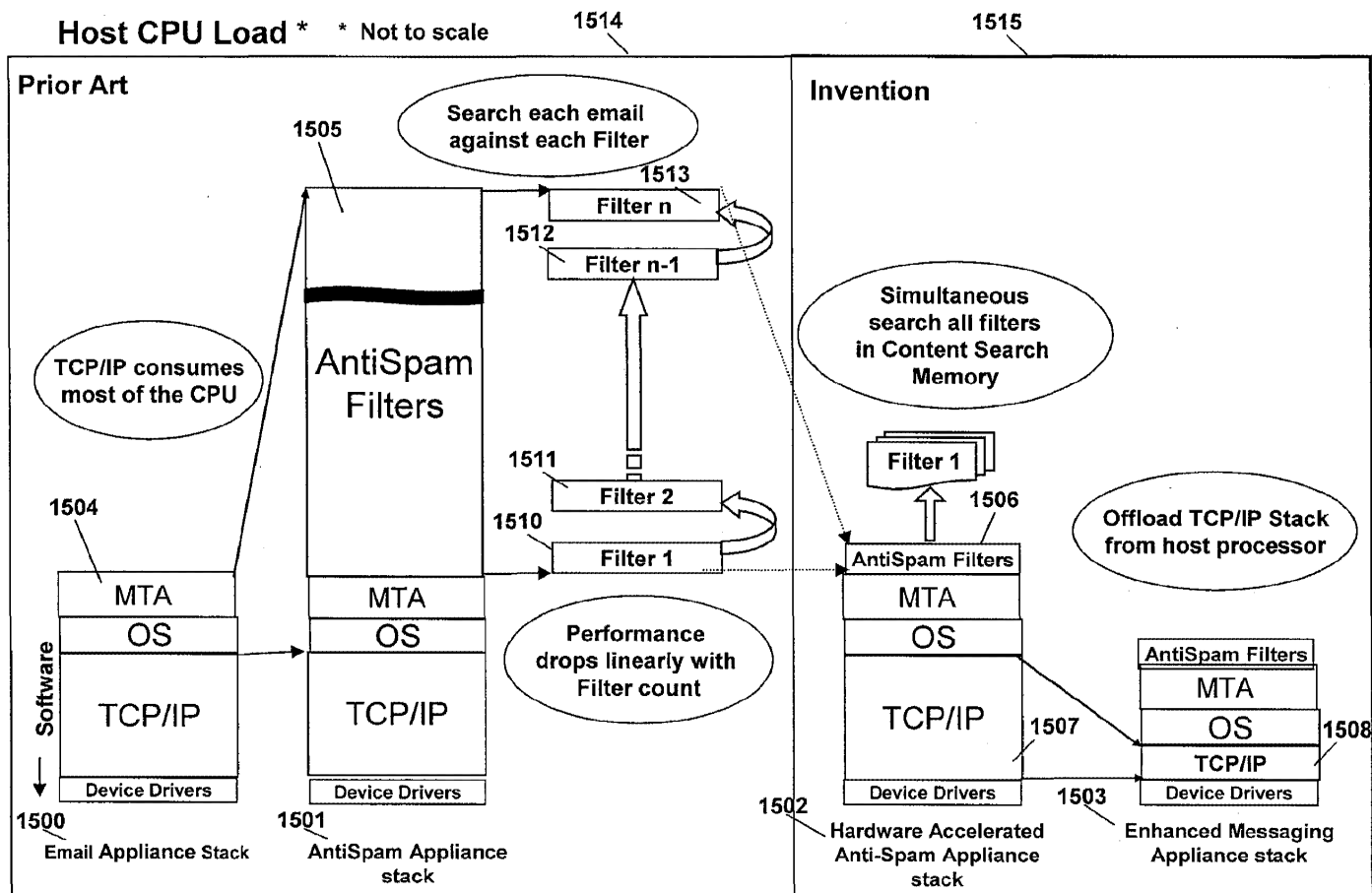


Fig. 15 Example Anti-spam Performance* Bottleneck and Solution

* Performance not to scale

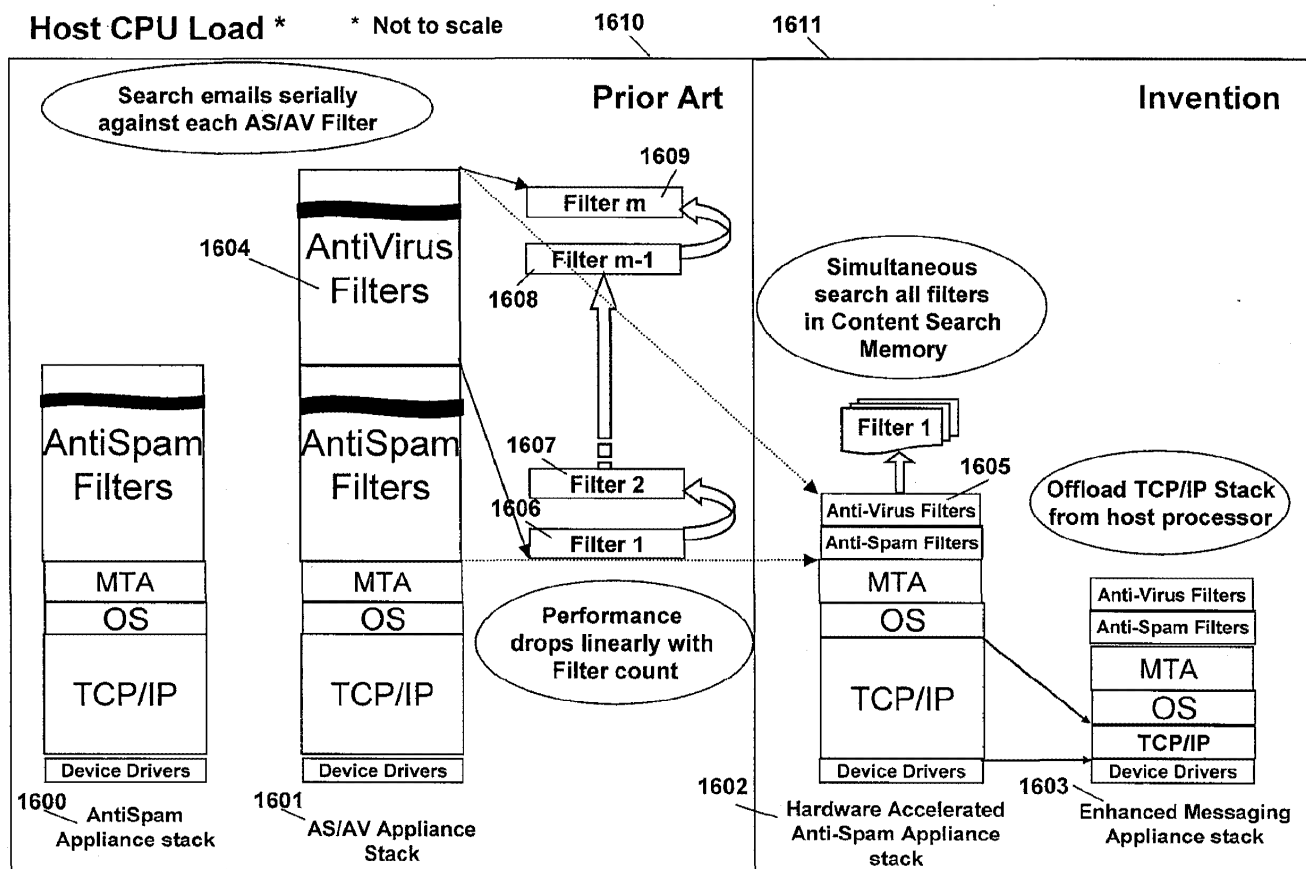


Fig. 16 Anti-spam with Anti-virus Performance* Bottleneck

* Performance not to scale

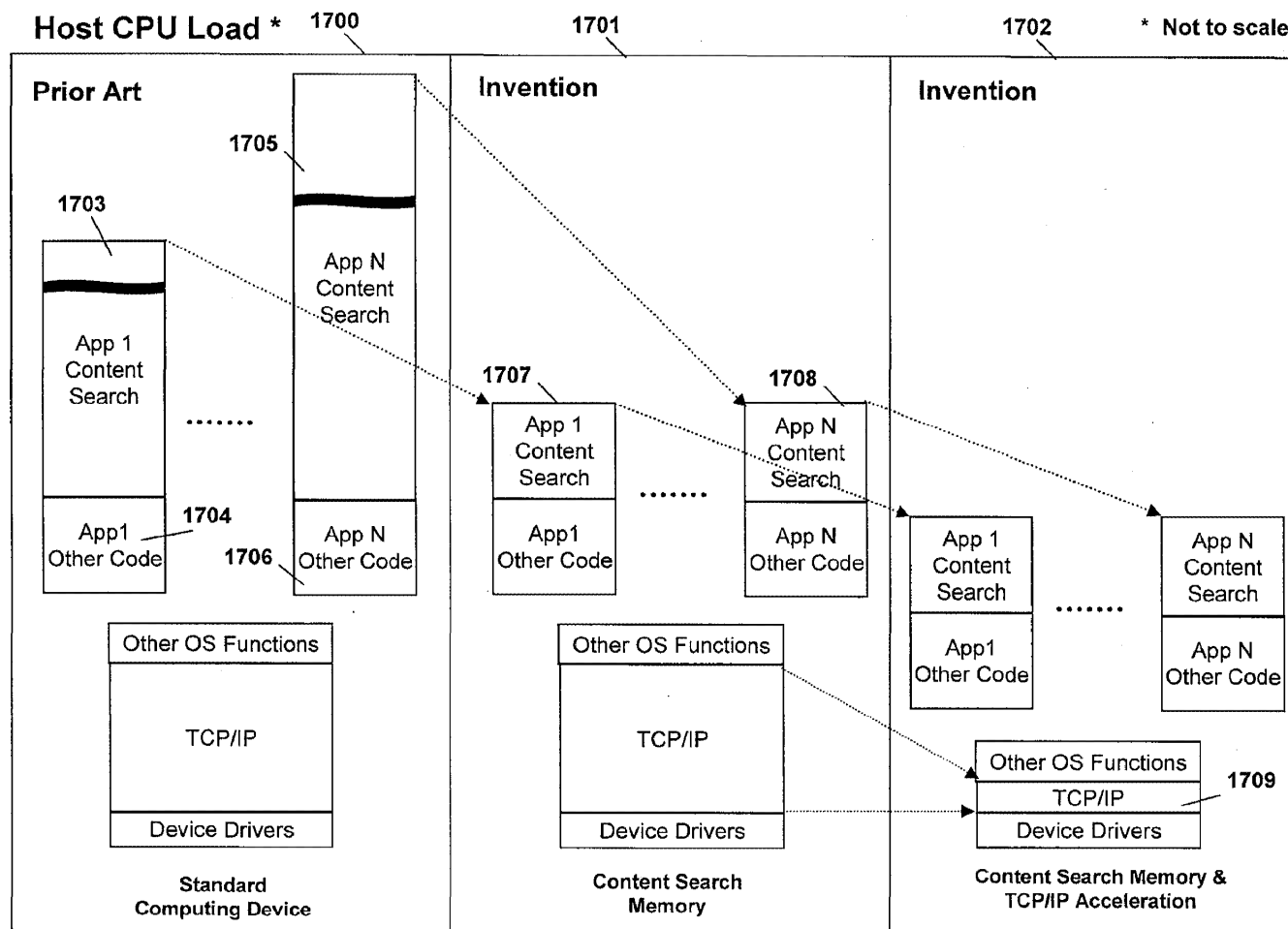


Fig. 17 Application Content Search Performance* Bottleneck and Solution

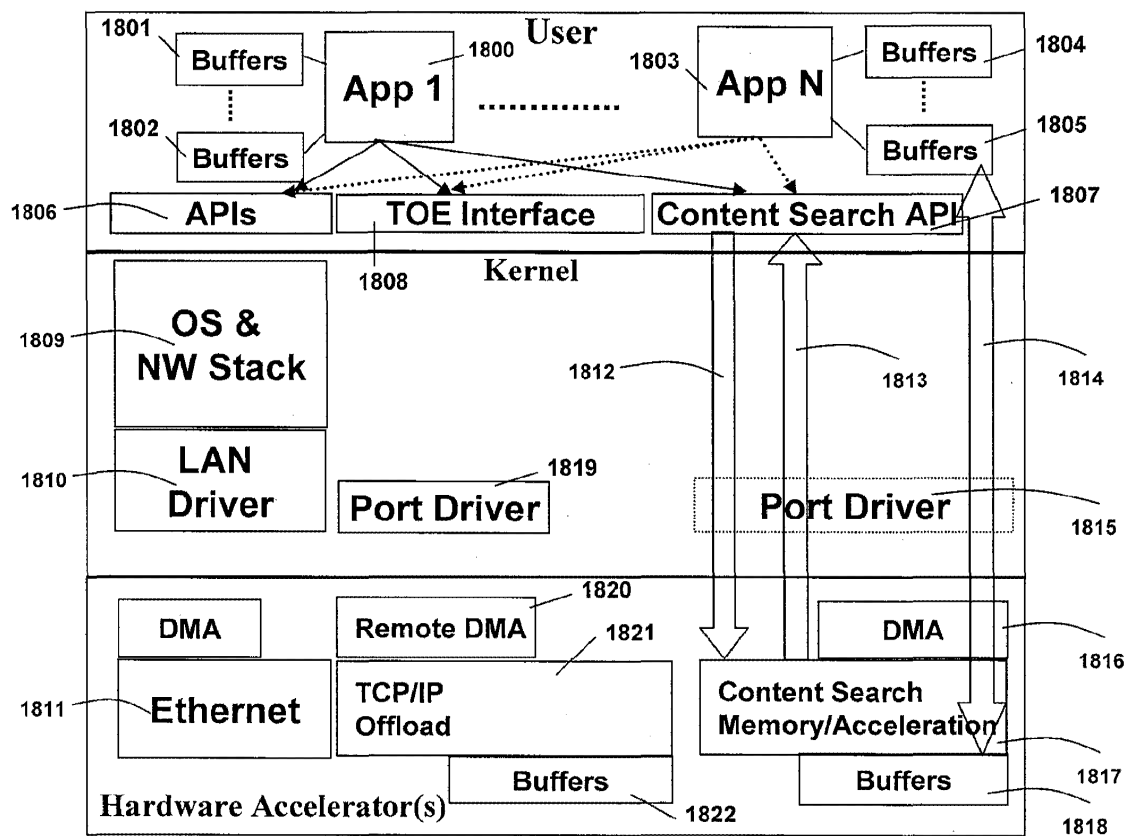


Fig. 18 An example content search API usage model

API *	Description
(*parameters are not illustrated)	
Initialize()	Initialize the hardware
getCapabilities()	Query the capabilities of the current hardware
setNFARule()	set an NFA rule in PRISM
Set_tNFA_Rule()	set a tagged NFA rule in PRISM
setContext()	set the context for PRISM
sndDataPtr()	send the pointer of the data buffer that needs to be searched
getRes()	retrieve the result from PRISM
getResPtr()	retrieve the pointer to the memory buffer that holds the results
switchContext()	Switch the current active context of the FSA blocks
setRuleGroup()	set the rule group that a specific rule belongs
selectRuleGroup()	select a specific rule group for access
setInitGroup()	set the initial group that is active for a given flow
startHWSearch()	start the hardware search
stopHWSearch()	stop the hardware search

Fig. 19 An example Content Search API with example functions

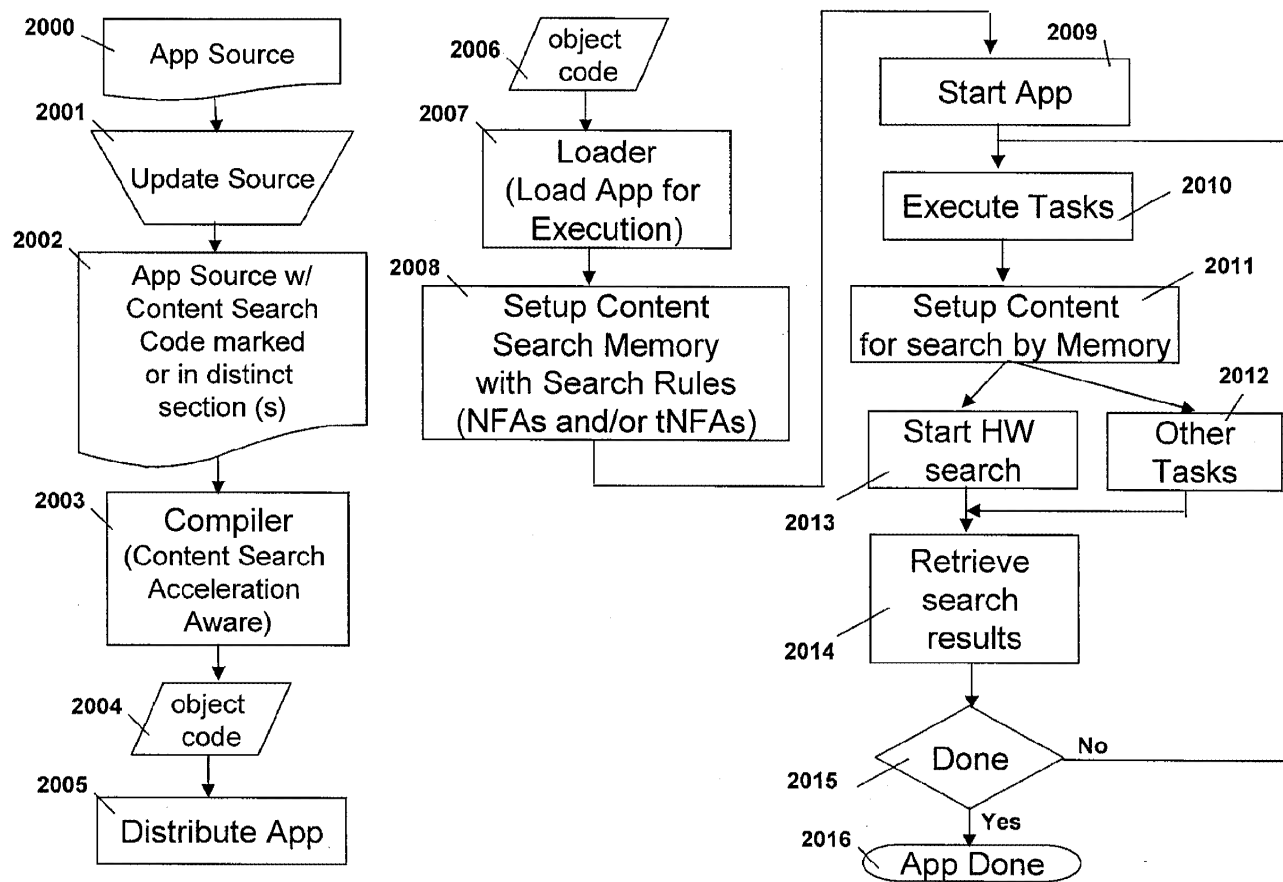
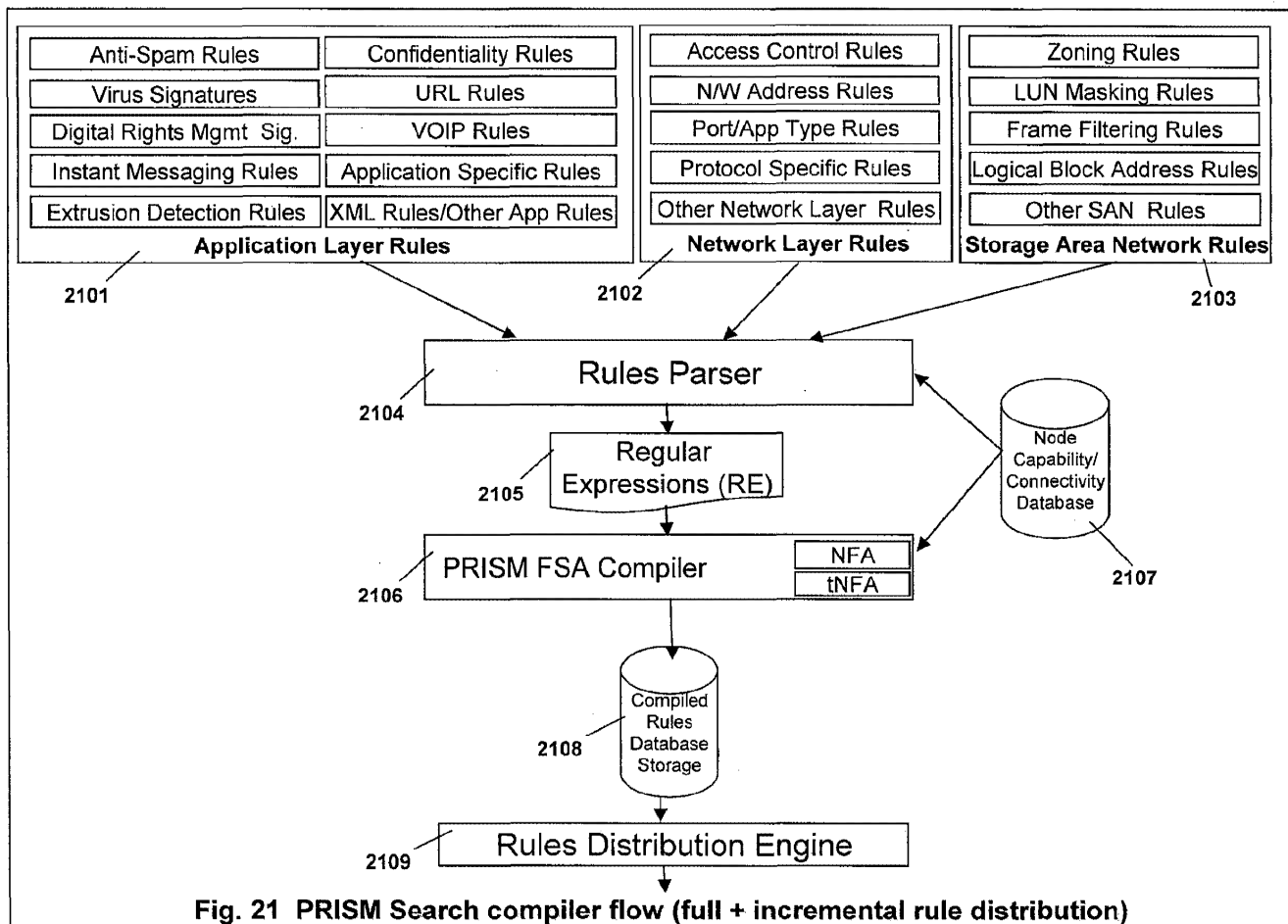


Fig. 20 An example application flow (static setup) for PRISM



INTERNATIONAL SEARCH REPORT

International application No.
PCT/US 07/86785

A. CLASSIFICATION OF SUBJECT MATTER

IPC(8) - G06F 12/00 (2008.04)

USPC - 711/105

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
USPC: 711/105Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched
USPC: 711/100, 105, 108; 707/3, 4, 10; 712/1, 36, 37

Electronic data base consulted during the international search (name of data base and, where practicable, search terms used)

USPTO WEST (PGPB, USPT, EPAB, JPAB); Google Scholar

Search Terms: Content search memory, architecture or circuit or chip, regular expression, finite state automata or FSA or NFA or DFA, search string, processor, intelligent search, current state vector, state dependent vector, dynamic or static etc.

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X ---	US 2004/0215593 A1 (SHARANGPANI et al.) 28 October 2004 (28.10.2006), entire document	21-22, 41-43, 53-58
Y		1-20, 23-40, 44-52, 59-62
Y	US 2006/0136570 A1 (PANDYA) 22 June 2006 (22.06.2006), entire document	1-20, 23-40, 44-52, 59-62
Y	US 2005/0052934 A1 (TRAN et al.) 10 March 2005 (10.03.2005), Fig. 13, para [0091]-[0092], [0100]	20
A	US 2006/0085533 A1 (HUSSAIN et al.) 20 April 2006 (20.04.2006)	1-62

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Date of the actual completion of the international search

06 April 2008 (06.04.2008)

Date of mailing of the international search report

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EFS ID:	24047283
Application Number:	14315571
International Application Number:	
Confirmation Number:	1085
Title of Invention:	Method and Apparatus for High-Speed Processing of Financial Market Depth Data
First Named Inventor/Applicant Name:	David E. Taylor
Customer Number:	21888
Filer:	Benjamin Lowell Volk/Michelle Woods
Filer Authorized By:	Benjamin Lowell Volk
Attorney Docket Number:	57451-133596
Receipt Date:	11-NOV-2015
Filing Date:	26-JUN-2014
Time Stamp:	10:44:40
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	no

File Listing:

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	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3693
	Examiner Name	Merchant, Shahid R
	Attorney Docket Number	57451-133596

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	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3693
	Examiner Name	Merchant, Shahid R
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Name/Print	Benjamin L. Volk, Jr.	Registration Number	48017

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Application Number:	14315571
International Application Number:	
Confirmation Number:	1085
Title of Invention:	Method and Apparatus for High-Speed Processing of Financial Market Depth Data
First Named Inventor/Applicant Name:	David E. Taylor
Customer Number:	21888
Filer:	Benjamin Lowell Volk/Laurie Poss
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Attorney Docket Number:	57451-133596
Receipt Date:	19-FEB-2016
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14315571
	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3692
	Examiner Name	Johnson, Gregory L
	Attorney Docket Number	57451-133596

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14315571
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Name/Print	Benjamin L. Volk, Jr.	Registration Number	48017

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International Application Number:	
Confirmation Number:	1085
Title of Invention:	Method and Apparatus for High-Speed Processing of Financial Market Depth Data
First Named Inventor/Applicant Name:	David E. Taylor
Customer Number:	21888
Filer:	Benjamin Lowell Volk/Linda Grace
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Attorney Docket Number:	57451-133596
Receipt Date:	22-JUN-2016
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Application Type:	Utility under 35 USC 111(a)

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	Filing Date	2014-06-26
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Signature	/Benjamin L. Volk, Jr./	Date (YYYY-MM-DD)	2016-10-21
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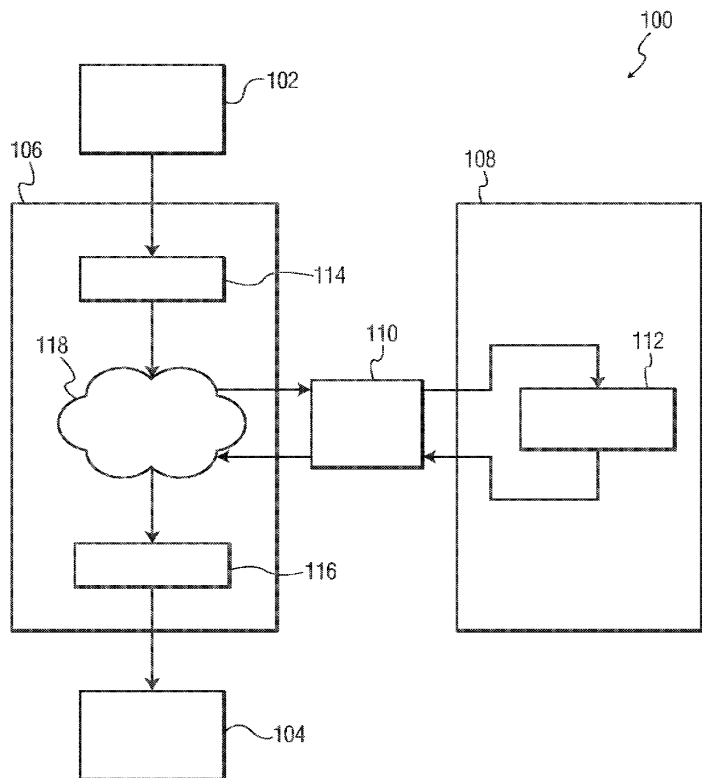
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[Continued on next page]

(54) Title: DATA PROCESSING WITH CIRCUIT MODELING



(57) Abstract: Various aspects of the present invention are directed to design modeling and/or processing of streaming data. According to an example embodiment, a system to model a hardware specification includes a platform (106) arranged to receive an input data stream and transmit an output data stream. The system also includes a source (102) for a streaming application adapted to provide the input data stream at a source data rate, a destination (104) for the streaming application adapted to consume the output data stream at a destination data rate, and a data channel (110) coupling the platform and a computer (108). The computer uses the hardware specification to generate intermediate data streams, which, in turn, are used to streamline the modeling for the platform.

WO 2006/059312 A2



FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

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DATA PROCESSING WITH CIRCUIT MODELING

The present invention is directed generally to modeling for streaming applications. More particularly, the present invention relates to methods and arrangements for real-time, or near real-time, modeling for streaming applications.

The electronics industry continues to strive for high-powered, high functioning circuits. Significant achievements in this regard have been realized through the fabrication of very large-scale integration of circuits on small areas of silicon wafer. Integrated circuits of this type are developed through a series of steps carried out in a particular order. The main objective in designing such devices is to obtain a device that conforms to geographical features of a particular design for the device. To obtain this objective, steps in the designing process are closely controlled to insure that rigid requirements are realized.

Semiconductor devices are used in large numbers to construct most modern electronic devices. In order to increase the capability of such electronic devices, it is necessary to integrate even larger numbers of such devices into a single silicon wafer. As the semiconductor devices are scaled down (i.e., made smaller) to form a larger number of devices on a given surface area, the structure of the devices and the fabrication techniques used to make such devices become more refined. This increased ability to refine such semiconductor devices has lead to an ever-increasing proliferation of customized chips, with each chip serving a unique function and application. This, in turn, has lead to various techniques to design and successfully test chips efficiently and inexpensively.

For many chip designs, customized chips are made by describing their functionality using a hardware-description language (HDL), such as Verilog or VHDL. The hardware description is often written to characterize the design in terms of a set of functional macros. The design is computer simulated to ensure that the custom design criteria are satisfied. For highly-complex custom chip designs, the above process can be burdensome and costly. The highly integrated structure of such chips leads to unexpected problems, such as signal timing, noise-coupling, and signal-level issues. Consequently, such complex custom chip designs involve extensive validation. This validation is generally performed at different stages using a Verilog or VHDL simulator. Once validated at this level, the Verilog or VHDL HDL code is synthesized, for example, using "Synopsys," to a netlist that is supplied to an ASIC (Application Specific Integrated Circuit) foundry for prototype fabrication. The ASIC prototype is then tested in silicon. Even after such validation with the Verilog or

VHDL simulator, unexpected problems are typical. Overcoming these problems involves more iterations of the above process, with testing and validation at both the simulation and prototype stages. Such repetition significantly increases the design time and cost to such a degree that this practice is often intolerable in today's time-sensitive market.

5 Similar problems manifest in semi-custom designs such as programmable logic devices. Also known as "PLDs", programmable logic devices are a well-known type of integrated circuit that can be programmed to perform specified logic functions. One of the more commons types of PLD is the field programmable gate array (FPGA) which has a number of different circuit tiles, each of which permits certain flexibility for programming
10 its functionality. Although programming most PLDs would be significantly faster than most complex custom chip designs, such efforts still involve significant delays.

As illustrated and described in U.S. Patent No. 6,347,395 issued February 12, 2002, and entitled, "Method and Arrangement for Rapid Silicon Prototyping", a typical development period (from initial design to new product) can be reduced by more that fifty
15 percent by way of a rapid silicon prototyping process and arrangement. However, even with rapid silicon prototyping, substantial delay can be required to compile a design that is modified to evaluate new algorithms or to address problems discovered during validation.

These chip-development problems are accentuated when attempting to process streaming data in real time or in near real time where the degree of delay is tolerable on an
20 application-by-application basis.

Accordingly, there is a need for a way to develop customized (including semi-customized) chips that overcomes the above-mentioned deficiencies. The present invention addresses this need, and other needs, by way of design modeling per the examples disclosed herein.

25 Various aspects of the present invention are directed to design modeling and/or processing of streaming data in a manner that addresses and overcomes the above-mentioned issues. Consistent with one example embodiment, a system to model a hardware specification includes a platform arranged to receive an input data stream and transmit an output data stream. The system also includes a source for a streaming application adapted
30 to provide the input data stream at a source data rate, a destination for the streaming application adapted to consume the output data stream at a destination data rate, and a data channel coupling the platform and a general purpose computer. The general purpose computer is adapted to generate, according to at least a portion of the hardware

specification, from a first intermediate data stream, which is received from the platform via the data channel, a second intermediate data stream, which is sent to the platform via the data channel, wherein the first intermediate data stream is based on the input data stream and the output data stream is based on the second intermediate data stream.

5 Another embodiment of the present invention discloses a method for modeling an electronic design. The method includes separating the electronic design for a streaming application into a start portion receiving an input data stream for the streaming application, an intermediate portion, and an end portion transmitting an output data stream for the streaming application, based on the streaming data flow through the electronic design. The
10 method also includes producing a hardware specification for the start portion and the end portion, producing an abstract software model for the intermediate portion, and generating configuration data for a programmable logic device (PLD) implementation from the hardware specification, wherein the PLD includes configurable logic and configurable routing that are programmed by the configuration data. The method further includes
15 generating an executable program from the abstract software model and operating the PLD using the configuration data and a general purpose computer using the executable program, wherein the electronic design is modeled by the operation of the PLD and the general purpose computer.

The invention may be more completely understood in consideration of the following
20 detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

Figure 1 is a block diagram of an example system for real-time abstract modeling of a streaming application, according to the present invention;

Figure 2 is a block diagram of another example system for real-time abstract
25 modeling of a streaming application, according to the present invention; and

Figure 3 is a flow diagram of an example process for real-time abstract modeling of a streaming application, according to the present invention.

While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described
30 in detail. It should be understood, however, that the intention is not to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

The present invention is believed to be generally applicable to methods and arrangements for processing data using circuits that require or benefit from fast compilations of circuit-configuration data. The invention has been found to be particularly advantageous for processing of streaming data in real time or in near real time where the degree of delay is tolerable on an application-by-application basis. While the present invention is not necessarily limited to such applications, an appreciation of various aspects of the invention is best gained through a discussion of examples in such an environment.

According to one example embodiment of the present invention, a system to model a hardware specification includes a platform arranged to receive an input data stream and transmit an output data stream. The system also includes a source for a streaming application adapted to provide the input data stream at a source data rate, a destination for the streaming application adapted to consume the output data stream at a destination data rate, and a data channel coupling the platform and a general purpose computer. The general purpose computer is adapted to generate, according to at least a portion of the hardware specification, from a first intermediate data stream, which is received from the platform via the data channel, a second intermediate data stream, which is sent to the platform via the data channel, wherein the first intermediate data stream is based on the input data stream and the output data stream is based on the second intermediate data stream.

Referring to Figure 1, a block diagram is shown of a system 100 for real-time abstract modeling of a streaming application, according to the present invention. The streaming application has a source 102 of streaming data, for example, a streaming video or audio source, such as a video tape player, video disk player, or music audio player. The streaming application has a destination 104 for streaming data, such as a video display device or audio speakers. The data from the source 102 is processed by the combination of the platform 106 and the general purpose computer 108, according to the hardware specification of the streaming application, before delivery of the processed data to the destination 104. The platform 106 and the computer 108 communicate via channel 110.

The platform 106 can be a PLD based platform or other device that is programmed to perform a portion of the streaming application. Alternatively, the platform 106 may be a SOC based platform that includes a system-on-a-chip (SOC). Example platforms 106 for Philips Semiconductors include Rapid Silicon Prototyping and the Nexperia platform together with the Nexperia Advanced Prototyping Architecture.

An example SOC for a platform 106 may include a wide variety of building blocks, such one or more digital signal processing blocks, which are typically used in the design of streaming applications. Certain portions of the hardware specification of the streaming application may include instances for a subset of the available building blocks, and the remaining portions of the hardware specification may be modeled by computer 108. For example, a streaming application may include various standard blocks and an innovative custom block. The streaming application may be modeled by system 100 with the standard blocks modeled by the platform 106 and the custom block modeled by a software processing function 112 on computer 108. Various alternative designs for the custom block may be quickly evaluated by system 100, because the custom block modeled by software processing function 112 may be rapidly modified and recompiled.

The platform 106 typically includes a receiver 114 to receive streaming data from the application data source 102. The receiver 114 may include processing functions, such as the conversion of analog signals from a video tape player 102 into a digital video stream. The platform 106 typically includes a transmitter 116 to provide processed streaming data to the application data destination 104. The transmitter 116 may include processing functions, such as the conversion of a processed digital video stream into analog signals for a video display unit 104. It will be appreciated that the receiver 114 and transmitter 116 may either be included within or be separate from the PLD or SOC on which platform 106 is based.

Hardware processing function 118 may perform a portion of the processing for the streaming application. Hardware processing function 118 implements an interface to channel 110. Examples for channel 110 include a parallel bus, such as PCI X, and a serial or parallel communications link, such as PCI Express. Typically, channel 110 provides high bandwidth in accordance with the particular streaming application. Channel 110 may be a communication protocol directly supported by computer 108 or an adapter between a communication protocol supported by computer 108 and another communication protocol, such as a proprietary communication protocol.

Hardware processing 118 typically sends a partially processed version of the streaming data received from application data source 102 to computer 108 via channel 110. It will be appreciated that hardware processing 118 may send only a portion of the streaming data, such as the data for one color component of color video data, to the computer 108. It will be appreciated that hardware processing 118 may send streaming data

to computer 108 without prior processing. Hardware processing 118 also receives streaming data from computer 108 via channel 110 that has been processed by processing function 112. Hardware processing 118 sends streaming data to application data destination 104 that is based on the streaming data received from computer 108. Hardware processing 118 may perform additional processing of the streaming data before providing the streaming data to application data destination 104.

Software processing function 112 may be a compiled software function on the general purpose computer 108. The streaming data received from platform 106 by function 112 and the streaming data sent to platform 106 by function 112 may be abstract data types, such as a sequence of numbers each representing an intensity value for a pixel of streaming video data. The available abstract data manipulation functions provided by computer 108, such as multiplication and addition, may be used to abstractly process the streaming data that is abstractly represented. An example function 112 scales the orientation of a video image vertically and/or horizontally.

It should be understood that the elements described in the figures are for description only, to aid in the understanding of the present invention. As is known in the art, elements described as hardware may equivalently be implemented in software. Reference to specific electronic circuitry is also only to aid in the understanding of the present invention, and any circuit to perform essentially the same function is to be considered an equivalent circuit.

Referring to Figure 2, a block diagram is shown for another example system 200 for real-time abstract modeling of a streaming application, according to the present invention. Data for the streaming application from source 202 is processed by the combination of PLD based platform 204, channel 206, and computer 208, and the processed data for the streaming application is delivered to destination 210.

The platform 204 may include a receiver 212 that receives the streaming data from the application data source 202 and provides the streaming data to an FPGA 214. FPGA 214 may include a memory 216 and FPGA 214 may be programmed to implement a DMA block 218 that interfaces with memory 216. DMA block 218 may provide four independent DMA channels to memory 216. A first DMA channel may be used to write data received from source 202 via receiver 212 into memory 216, a second DMA channel may be used to read data from memory 216 for delivery to application data destination 210 via transmitter 220, a third DMA channel may be used to read streaming data from memory 216 for

delivery to computer 208 via channel 206, and a fourth DMA channel may be used to write streaming data received from computer 208 via channel 206 to memory 216.

Memory 216 may be a dual port memory with the DMA block 218 connected to one port and the FPGA 214 programmed to implement a processing block 222 that is connected to the other port. The processing block 222 may perform processing of the streaming data received from source 202 before the processed data is delivered to computer 208 and the processing block 222 may perform processing of the streaming data received from computer 208 before the processed data is delivered to destination 210. Thus, the streaming data from source 202 may undergo three sequential processing operations, by the processing block 222, the computer 208, and again the processing block 222, before delivery to the destination 210. It will be appreciated that either or both of these processing operations by processing block 222 may be omitted, according to the specification of the streaming application. In one embodiment, processing block 222 may include a processor.

In one embodiment, channel 206 is a PCI-X card that is plugged into a server computer 208. The PCI-X card 206 includes another FPGA 224 that is programmed to implement an adapter function between the PCI-X protocol of the PCI-X bus on line 226 and a proprietary communication protocol on line 228 that is based on low level differential signaling supported by FPGA 214 and FPGA 224. The adapter function of FPGA 224 includes a PCI-X core 230, a memory-mapped DMA controller 232, a memory-mapped bridge 234 for I/O transactions, a memory mapped bridge 236 for memory transactions, an interrupt controller 238 and a channel controller 239. The PCI-X core 230 may implement the PCI-X protocol for the PCI-X bus on line 226. The memory-mapped DMA controller 232 may be controlled by the computer 208 to read burst data transfers from memory 216 to deliver streaming data to memory 240 of computer 208 via PCI-X controller 242. The computer 208 may generate burst data transfers causing PCI-X controller 242 to send streaming data to memory 216 via memory-mapped bridge 236.

The streaming data from the platform 204 may be stored in a buffer in memory 240. In one embodiment, the streaming data is broken into data blocks and multiple buffers are provided for the data blocks, such that one buffer may be receiving a block streaming data from platform 204, while another buffer is simultaneously being processed by processing function 244 executing on processor 246 of computer 208, and a block of streaming data is simultaneously being sent to platform 204 from yet another buffer. With a greater number of buffers, the various data transfer and data processing function may be further decoupled.

In one embodiment, on completing the evaluation of various design options for a processing function 244, the abstract implementation of the processing function 244 may be translated into a hardware specification that is implemented in FPGA 214, such that channel 206 and computer 208 are no longer needed to perform the streaming application.

5 Referring to Figure 3, a flow diagram is shown as an example of one process for real-time abstract modeling of a streaming application, according to the present invention. The streaming application delivers to a destination processed streaming data from a source.

At step 302, a hardware platform receives streaming data from an application data source, such as a source of a video and/or audio stream. At step 304, the hardware platform
10 optionally performs a processing of the streaming data from the data source. At step 306, streaming data is transferred from the hardware platform to a general purpose computer. If the hardware platform performed processing at step 304, then the streaming data transferred at step 306 is the streaming data after the processing of step 304, otherwise the streaming data transferred at step 306 is the data received from the source at step 302.

15 At step 308, software on the general purpose computer creates a processed data stream from the data stream transferred at step 306. Various design options for the processing of step 308 may be quickly evaluated at an abstract level by modifying and recompiling the software, allowing a particular design option to be selected according to the evaluation criteria.

20 At step 310, the processed data stream from step 308 is transferred from the general purpose computer to the hardware platform. At step 312, the processed data stream from step 308 is optionally further processed by the hardware platform, with the result sent from the hardware platform to an application data destination.

Accordingly, various embodiments have been described by way of the figures and/or
25 discussion as example implementations of the present invention involving abstract modeling of streaming data applications. The present invention should not be considered limited to these particular example implementations. Various modifications, equivalent processes, as well as numerous structures to which the present invention may be applicable fall within the scope of the present invention. Such variations may be considered as part of the claimed
30 invention, as fairly set forth in the appended claims.

CLAIMS

What is claimed is:

1. A system to model a hardware specification, comprising: a platform (106) arranged to receive an input data stream and transmit an output data stream; a source (102) for a streaming application adapted to provide the input data stream at a source data rate; a destination (104) for the streaming application adapted to consume the output data stream at a destination data rate; a data channel (110) coupling the platform and a general purpose computer (108); and the general purpose computer adapted to generate according to at least a portion of the hardware specification, from a first intermediate data stream, which is received from the platform via the data channel, a second intermediate data stream, which is sent to the platform via the data channel, wherein the first intermediate data stream is based on the input data stream, the output data stream is based on the second intermediate data stream.
2. The system of claim 1, wherein the platform is based on a programmable logic device (PLD).
3. The system of claim 2, wherein the PLD-based platform includes at least one memory arranged to store a moving interval of the input data stream, the first intermediate data stream, the second intermediate data stream, and the output data stream.
4. The system of claim 2, wherein the PLD-based platform is adapted to generate according to at least a portion of the hardware specification, the first intermediate data stream from the input data stream.
5. The system of claim 2, wherein the PLD-based platform is adapted to generate according to at least a portion of the hardware specification, the output data stream from the second intermediate data stream.
6. The system of claim 2, wherein the PLD-based platform includes a PLD that includes configurable logic and configurable routing.
7. The system of claim 1, wherein the first intermediate data stream is a copy of the input stream, the output data stream is a copy of the second intermediate data stream, and the general purpose computer is adapted to generate the second intermediate data stream from the first intermediate data stream according to the hardware specification.
8. A method for modeling an electronic design, comprising: separating the electronic design for a streaming application into a start portion receiving an input data

stream for the streaming application, an intermediate portion (112), and an end portion transmitting an output data stream for the streaming application, based on the streaming data flow through the electronic design; producing a hardware specification for the start portion and the end portion; producing an abstract software model for the intermediate portion; generating configuration data for a programmable logic device (PLD) implementation from the hardware specification, wherein the PLD (118) includes configurable logic and configurable routing that are programmed by the configuration data; generating an executable program from the abstract software model; and operating the PLD using the configuration data and a general purpose computer (108) using the executable program, wherein the operating models the electronic design.

9. The method of claim 8, further comprising validating the electronic design based on the operating.

10. The method of claim 8, further comprising: generating a derived hardware specification from the abstract software model; generating another configuration data for a PLD implementation from the hardware specification and the derived hardware specification; and operating the PLD using the another configuration data, wherein the operating implements the electronic design.

1/3

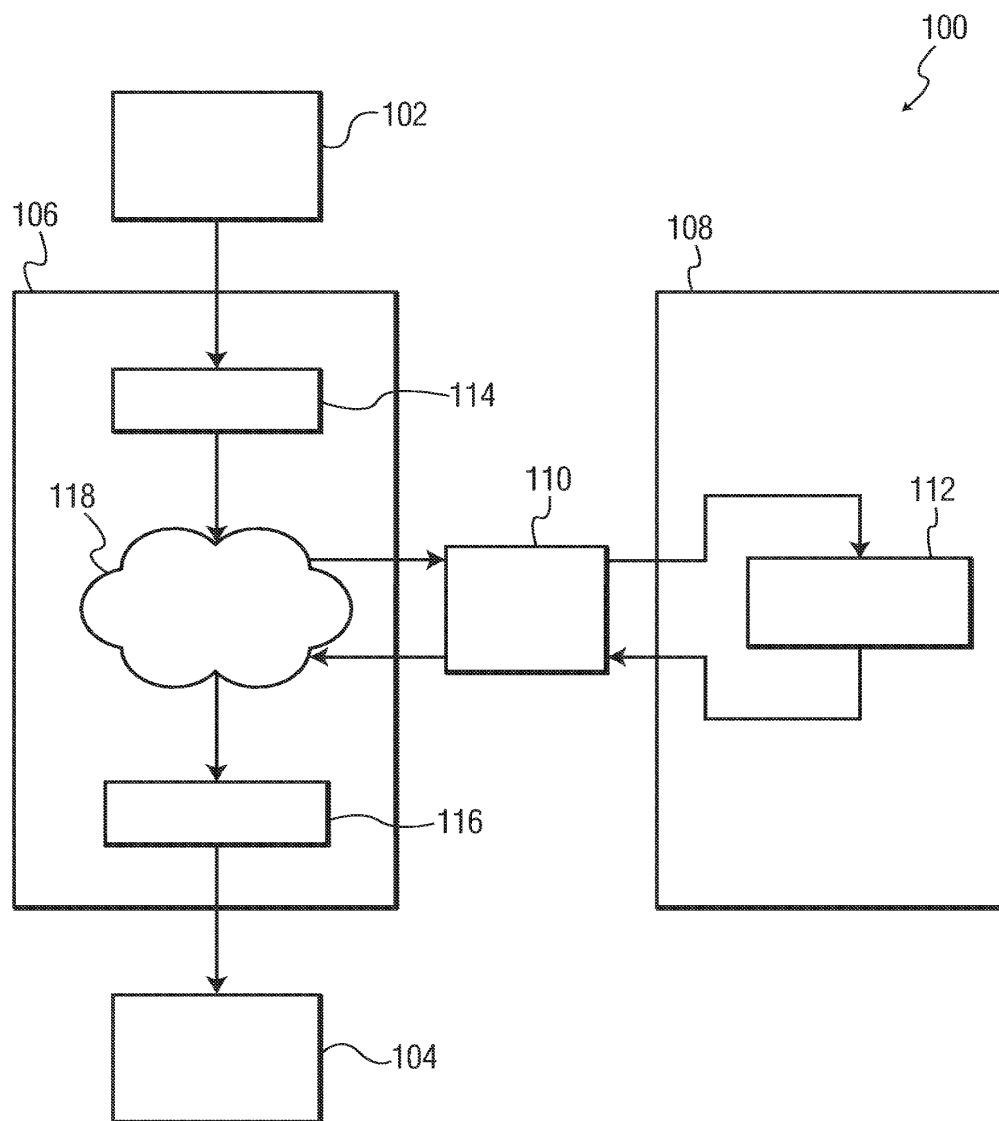


FIG. 1

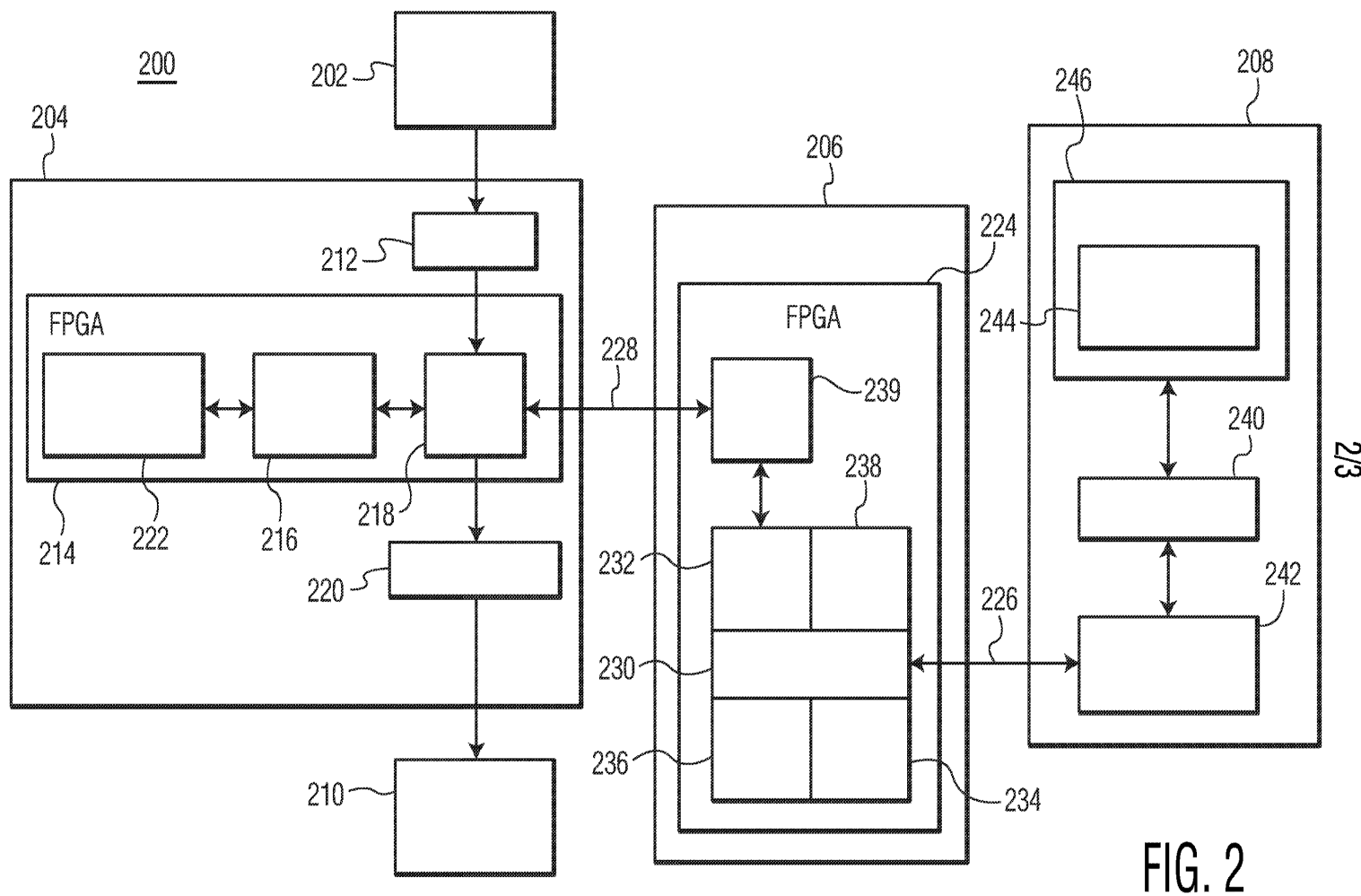


FIG. 2

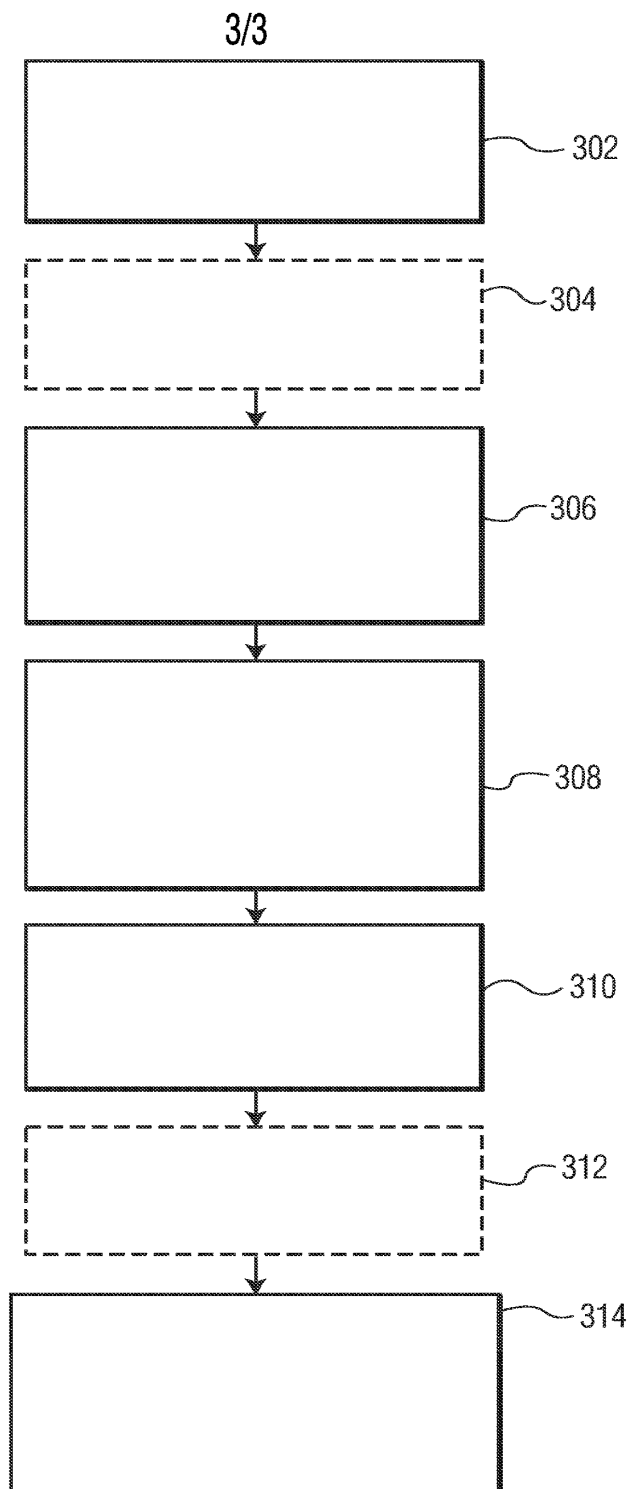


FIG. 3

Electronic Acknowledgement Receipt	
EFS ID:	27281862
Application Number:	14315571
International Application Number:	
Confirmation Number:	1085
Title of Invention:	Method and Apparatus for High-Speed Processing of Financial Market Depth Data
First Named Inventor/Applicant Name:	David E. Taylor
Customer Number:	21888
Filer:	Benjamin Lowell Volk/Linda Grace
Filer Authorized By:	Benjamin Lowell Volk
Attorney Docket Number:	57451-133596
Receipt Date:	21-OCT-2016
Filing Date:	26-JUN-2014
Time Stamp:	10:06:38
Application Type:	Utility under 35 USC 111(a)

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File Listing:

Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Information Disclosure Statement (IDS) Form (SB08)	IDS.pdf	1034946	no	4
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2	Foreign Reference	WO2006059312A2.pdf	787038	no	15
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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14315571
	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3695
	Examiner Name	Robinson, Kito R.
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	Examiner Name	Robinson, Kito R.
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	3	20040073703	A1	2004-04-15	Boucher et al.	
	4	20050190787	A1	2005-09-01	Kuik et al.	
	5	20090019219	A1	2009-01-15	Magklis et al.	
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	1	CORBET ET AL., "Linux Device Drivers: Where the Kernel Meets the Hardware, O'Reilly, February 2005, pp. 19-20, 412-414, and 441, 3rd Edition	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14315571
	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3695
	Examiner Name	Robinson, Kito R.
	Attorney Docket Number	57451-133596

2	CURRID, "TCP Offload to the Rescue", Networks, June 14, 2004, 16 pages, Vol. 2, No. 3
3	Office Action for CA Application 2744746 dated March 10, 2017

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14315571
	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3695
	Examiner Name	Robinson, Kito R.
	Attorney Docket Number	57451-133596

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Benjamin L. Volk, Jr./	Date (YYYY-MM-DD)	2017-05-26
Name/Print	Benjamin L. Volk, Jr.	Registration Number	48,017

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EFS ID:	29327459
Application Number:	14315571
International Application Number:	
Confirmation Number:	1085
Title of Invention:	Method and Apparatus for High-Speed Processing of Financial Market Depth Data
First Named Inventor/Applicant Name:	David E. Taylor
Customer Number:	21888
Filer:	Benjamin Lowell Volk/Greg Drennen
Filer Authorized By:	Benjamin Lowell Volk
Attorney Docket Number:	57451-133596
Receipt Date:	26-MAY-2017
Filing Date:	26-JUN-2014
Time Stamp:	15:10:47
Application Type:	Utility under 35 USC 111(a)

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1	Information Disclosure Statement (IDS) Form (SB08)	IDS.pdf	1035571	no	5
			9fb686f94011d53a7b453043e526ff76f6a2b910		

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/315,571	06/26/2014	David E. Taylor	57451-133596	1085
21888 7590 07/07/2017 THOMPSON COBURN LLP ONE US BANK PLAZA SUITE 3500 ST LOUIS, MO 63101			EXAMINER ROBINSON, KITO R	
			ART UNIT 3695	PAPER NUMBER
			NOTIFICATION DATE 07/07/2017	DELIVERY MODE ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No. 14/315,571	Applicant(s) TAYLOR ET AL.	
	Examiner KITO R. ROBINSON	Art Unit 3695	AIA (First Inventor to File) Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTHS FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 26 June 2014.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on ____.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on ____; the restriction requirement and election have been incorporated into this action.
- 4) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims*

- 5) ☒ Claim(s) 1-46 is/are pending in the application.
5a) Of the above claim(s) ____ is/are withdrawn from consideration.
- 6) ☐ Claim(s) ____ is/are allowed.
- 7) ☒ Claim(s) 1-46 is/are rejected.
- 8) ☐ Claim(s) ____ is/are objected to.
- 9) ☐ Claim(s) ____ are subject to restriction and/or election requirement.

* If any claims have been determined allowable, you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to PPHfeedback@uspto.gov.

Application Papers

- 10) ☒ The specification is objected to by the Examiner.
- 11) ☒ The drawing(s) filed on 26 June 2014 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

Certified copies:

- a) ☐ All b) ☐ Some** c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. ____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

** See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☒ Information Disclosure Statement(s) (PTO/SB/08a and/or PTO/SB/08b)
Paper No(s)/Mail Date See Continuation Sheet.
- 3) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. ____.
- 4) ☐ Other: ____.

Continuation of Attachment(s) 2). Information Disclosure Statement(s) (PTO/SB/08), Paper No(s)/Mail Date :11/11/2014; 02/19/2016; 06/22/2016; 10/21/2016 & 05/26/2017.

DETAILED ACTION

Status of Claims

1. This action is in reply to the application filed on 26 June 2014.
2. Claims 1-46 are currently pending and have been examined.
3. The present application is being examined under the pre-AIA first to invent provisions.
4. Claims 23-41 & 44-46 are allowable.

Specification

5. The disclosure is objected to because of the following informalities: Paragraph 0001 and 0003 contains missing U.S. Patent Numbers.

Appropriate correction is required.

Claim Rejections - 35 USC § 101

6. 35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

7. Claims 1-46 are rejected under 35 U.S.C. 101 because the claimed invention is directed to a judicial exception (i.e., a law of nature, a natural phenomenon, or an abstract idea) without significantly more. Claim(s) 1-46 is/are directed to managing limit orders. Claim 1 discloses streaming data representative of a plurality of limit order events pertaining to a plurality of financial instruments, processing the streaming data to determine order book data associated with the limit order events; generating a stream of enriched limit order events wherein the enriched limit order events are enriched with data indicative of the determined order book data. Thus, the focus of the claim and its character as a whole is on the idea of managing limit orders, which is implemented by a system that uses a coprocessor.

Managing limit orders is according to the court a “method of organizing human behavior” that is similar to other concepts that have been identified as abstract by the courts, such as Collecting, displaying, and manipulating data (*Int. Ventures v. Cap One Financial*); 1) collecting data, 2) recognizing certain data within the collected data set, and 3) storing that recognized data in a memory in *Content Extraction*; Obtaining and comparing intangible data (*CyberSource*) and organizing information through mathematical correlations in *Digitech*. Therefore, it is reasonable to conclude based on the similarity of the idea described in this claim to several abstract ideas found by the courts that claim 1 is directed to an abstract idea (*Step 2A: Yes*).

This conclusion is not altered by *Enfish*, where the Federal Circuit stated that certain claims directed to improvements in computer-related technology, including claims directed to software, are not necessarily abstract (*Step 2A*). Unlike the claims in *Enfish*, claim 1 is not clearly directed to an improvement in computer-related technology (*e.g.*, computer functionality). Thus, because it is not readily apparent that claim 1 is directed to a non-abstract idea under *Step 2A*, it is necessary to analyze the additional elements in claim 1 under *Step 2B*.

8. The claim(s) does/do not include additional elements that are sufficient to amount to significantly more than the judicial exception because the claim recites the additional limitations of a coprocessor receive, processes and transmit data wherein the coprocessor comprises a member of the group consisting of a chip-multi-processor (CMP) and a graphics processing unit (GPU). A chip-multi-processor (CMP) and a graphics processing unit (GPU) for receiving and processing data are well-understood, routine, conventional computer components, which in this claim are recited at a high level of generality and perform generic computer functions (*e.g.*, receiving and processing information). Generic computer components performing generic computer functions, alone, do not amount to significantly more than the abstract idea.

9. Viewing the limitations in combination also fails to amount to significantly more than the abstract idea. The claimed invention seeks to receive, process, and manipulate data simply, fast, and in such a way that the information may be easily tracked (*i.e.* order limit events), but these functions reflect ordinary usage typically performed by a generic computer, as would be recognized by those of ordinary skill in the

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field of data processing. For example, as noted in *TLI Communications*, using a computer to attach classification data, such as dates and times, to images for purposes of storing those images in an organized manner does not add significantly more to a judicial exception. The recitation of conventional processing technology performing well-understood, routine, conventional functions such as receiving and processing and manipulating data does not reflect an "inventive concept." Thus, whether viewed individually or in combination, the additional limitations do not amount to a claim as a whole that is significantly more than the abstract idea (*Step 2B: No*). The claim is not patent eligible.

Claim Rejections - 35 USC § 103

10. The following is a quotation of pre-AIA 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under pre-AIA 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

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12. Claims 1, 2, 41 & 43 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Hamati et al. US 8,175,946 B2, hereafter Hamati in view of Kelleher US 7,598,958 B1.

Claim 1, 42

Hamati discloses:

- *streaming data representative of a plurality of limit order events pertaining to a plurality of financial instruments into a processor (column 3, lines 41-44);*
- *processing the streaming data with the processor to determine order book data associated with the limit order events (column 3, lines 45-55);*
- *generating a stream of enriched limit order events with the coprocessor wherein the enriched limit order events are enriched with data indicative of the determined order book data (column 3, lines 45-55 & column 3, lines 56-63);.*

Hamati does not disclose the following, however Kelleher does:

- *Coprocessor (Abstract & column 2, lines 6-17)*

It would have been obvious to one of ordinary skill in the art at the time of the invention to [combine/modify] the method of Hamati with the technique of Kelleher because it is an easy and convenient way to improved processing performance.

Claim 2 & 43

Hamati & Kelleher discloses the limitations as shown in the rejection of Claim 1 & 42 above. Hamati does not disclose the limitation of *wherein the coprocessor comprises a member of the group consisting of a chip-multi-processor (CMP) and a graphics processing unit (GPU)*. However, Kelleher, in at least Column 2 Line 6-17 discloses "A graphics processing unit chip is disclosed that may be used as an individual processor or packaged as a multi-chip module having a master/slave pair with improved processing performance. A packaged multi-chip master/slave pair includes a high bandwidth interlink for transferring data from the master chip to the slave chip and returning processed data from the slave chip to the master chip. The master chip receives a graphics command string and generates a graphics

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output. The master chip utilizes the slave chip to process, in parallel, data for one or more stages of the graphics pipeline of the master chip.”

It would have been obvious to one of ordinary skill in the art at the time of the invention to [combine/modify] the method of Hamati with the technique of Kelleher because it is an easy and convenient way to improved processing performance.

13. Claims 3-22 is/are rejected under pre-AIA 35 U.S.C. 103(a) as being unpatentable over Hamati in view of Kelleher and in further view of Parsons et al. US 7,921,046 B2, hereafter Parsons.

Claim 3-6

Hamati & Kelleher discloses the limitations as shown in the rejection of Claim 1 above. Hamati & Kelleher do not disclose the limitation of *wherein the generating step comprises appending a plurality of data fields to a plurality of limit order events to generate the enriched limit order events, wherein the appending step comprises appending at least one price volume field to a limit order event, wherein the at least one price volume field comprises a regional price volume field, and wherein the at least one price volume field comprises a composite price volume field*. However, Parsons, in at least Column 22 Line 47-63 discloses “Record fields may include but are not limited to: last trade price, last trade size, last trade time, best bid price, best bid size, best bid time, best ask price, best ask size, best ask time, total trade volume, daily change, tick direction, price direction, high trade price, high price time, low trade price, low price time, and close price. In a preferred embodiment, record fields also include derived fields such as: total trade volume at bid, total trade volume at ask, traded value, traded value at bid, traded value at ask, and volume-weighted average price (VWAP). As reflected in FIGS. 15(a) and (b), a preferred embodiment of the LVC Update FAM maintains a composite record and a set of regional records for every financial instrument observed on the input feeds. A composite record reflects the current state of the financial instrument across all exchanges upon which it trades. A regional record reflects the current state of the financial instrument on a given exchange.”

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It would have been obvious to one of ordinary skill in the art at the time of the invention to [combine/modify] the method of Hamati and Kelleher with the technique of Parsons because it is an easy and convenient way to improved processing performance.

Claim 7-9

Hamati & Kelleher discloses the limitations as shown in the rejection of Claim 3 & 7 above. Hamati & Kelleher do not disclose the limitation of *wherein the appending step comprises appending at least one price order count field to a limit order event, wherein the at least one price order count field comprises a regional price order count field and wherein the at least one price order count field comprises a composite price order count field*. However, Parsons, in at least Column 15 Line 62-67 discloses "The OBC includes the ability to generate various views of the book for a financial instrument including but not limited to a price-aggregated view and a composite view. A composite view is a sort order of the price or order entries for a financial instrument across multiple exchanges." Column 22 Line 47-63 discloses "Record fields may include but are not limited to: last trade price, last trade size, last trade time, best bid price, best bid size, best bid time, best ask price, best ask size, best ask time, total trade volume, daily change, tick direction, price direction, high trade price, high price time, low trade price, low price time, and close price. In a preferred embodiment, record fields also include derived fields such as: total trade volume at bid, total trade volume at ask, traded value, traded value at bid, traded value at ask, and volume-weighted average price (VWAP). As reflected in FIGS. 15(a) and (b), a preferred embodiment of the LVC Update FAM maintains a composite record and a set of regional records for every financial instrument observed on the input feeds. A composite record reflects the current state of the financial instrument across all exchanges upon which it trades. A regional record reflects the current state of the financial instrument on a given exchange

It would have been obvious to one of ordinary skill in the art at the time of the invention to [combine/modify] the method of Hamati and Kelleher with the technique of Parsons because it is an easy and convenient way to improved processing performance.

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Claim 10-13

Hamati & Kelleher discloses the limitations as shown in the rejection of Claim 3 & 11 above. Hamati & Kelleher do not disclose the limitation of *wherein the appending step comprises appending at least one order attribute vector field to a limit order event, the order attribute vector indicative of an impact of an attribute on an order book associated with the limit order event, wherein the appending step comprises appending at least one price attribute vector field to a limit order event, the price attribute vector indicative of an impact of an attribute on a price point order book associated with the limit order event, wherein the at least one price attribute vector field comprises a regional price attribute vector field and wherein the at least one price attribute vector field comprises a regional price attribute vector field*. However, Parsons, in at least column 11, lines 61-65 discloses “a price aggregate view where orders at the same price point are aggregated together to create entries that are indicative of the total number of orders available at each price point; and an ordinary view with specific trading venues (which are the source of orders) excluded.” Column 15 Line 62-67 discloses “The OBC includes the ability to generate various views of the book for a financial instrument including but not limited to a price-aggregated view and a composite view. A composite view is a sort order of the price or order entries for a financial instrument across multiple exchanges.” Column 22 Line 47-63 discloses “Record fields may include but are not limited to: last trade price, last trade size, last trade time, best bid price, best bid size, best bid time, best ask price, best ask size, best ask time, total trade volume, daily change, tick direction, price direction, high trade price, high price time, low trade price, low price time, and close price. In a preferred embodiment, record fields also include derived fields such as: total trade volume at bid, total trade volume at ask, traded value, traded value at bid, traded value at ask, and volume-weighted average price (VWAP). As reflected in FIGS. 15(a) and (b), a preferred embodiment of the LVC Update FAM maintains a composite record and a set of regional records for every financial instrument observed on the input feeds. A composite record reflects the current state of the financial instrument across all exchanges upon which it trades. A regional record reflects the current state of the financial instrument on a given exchange. Column 24, lines 19-30 discloses “In a preferred embodiment, the set of user identifiers is specified using a bit vector where each bit position in the vector corresponds to a user identifier. For

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example, a 4-bit vector with the value 1010 represents the set of user identifiers [3,1]. The size of the interest list in bits is equal to the total number of user subscriptions allowed by the Ticker Plant. In a preferred embodiment, each record contains an interest list that is updated in response to user subscribe and unsubscribe events. By maintaining an interest list in the composite record, the Ticker Plant allows a subscription to include all transactions for a given financial instrument on every exchange upon which it trades."

It would have been obvious to one of ordinary skill in the art at the time of the invention to [combine/modify] the method of Hamati and Kelleher with the technique of Parsons because it is an easy and convenient way to improved processing performance.

Claim 14-16

Hamati & Kelleher discloses the limitations as shown in the rejection of Claim 3 & 14 above. Hamati & Kelleher do not disclose the limitation of *wherein the appending step comprises appending at least one sort order field to a limit order event, the sort order field being indicative of a relative position of the limit order event within an associated order book, wherein the sort order field is indicative of a relative position of the limit order event within an associated price aggregated order book, wherein the sort order field is indicative of a relative position of the limit order event within an associated composite price aggregated order book*. However, Parsons, in at least column 11, lines 46-56 discloses "For each record, the order book server preferably maintains a sorted list of the bids and offers associated with all outstanding orders for that instrument. This list is known as the "book" for that instrument. The order information for each instrument is received from a variety of different trading venues in stream 106 and is aggregated together to form one holistic view of the market for that particular instrument. The order book server is configured to respond to requests from workstation 104 users or application programs 150 to present the book in a number of different ways." Column 15, lines 62-67 discloses "The OBC includes the ability to generate various views of the book for a financial instrument including but not limited to a price-aggregated view and a composite view. A composite view is a sort order of the price or order entries for a financial instrument across multiple exchanges."

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It would have been obvious to one of ordinary skill in the art at the time of the invention to [combine/modify] the method of Hamati and Kelleher with the technique of Parsons because it is an easy and convenient way to improved processing performance.

Claim 17 & 18

Hamati & Kelleher discloses the limitations as shown in the rejection of Claim 3 & 14 above. Hamati & Kelleher do not disclose the limitation of *wherein the appending step comprises appending at least one interest vector field to a limit order event, the interest vector field being indicative of which of a plurality of client applications are interested in receiving the enriched limit order event and wherein the interest vector field is further indicative of which fields of the enriched limit order event each of the plurality of client applications are interested in receiving.* However, Parsons, in at least column 2, lines 7-11 discloses "In an attempt to promptly deliver financial information to interested parties such as traders, a variety of market data platforms have been developed for the purpose of ostensible "real time" delivery of streaming bid, offer, and trade information for financial instruments to traders." Column 14, lines 52-60 discloses "With interest and entitlement filtering, a stream of messages coming from a module such as one of the caching modules described below (e.g., price summary LVC, order book OBC, or generic GVC) is filtered based upon a set of entitlement data and interest data that is stored for each record in the cache. This entitlement and interest data defines a set of users (or applications) that are both entitled to receive the messages associated with the record and have expressed an interest in receiving them." Column 24, lines 15-19 discloses "The LVC message/record updater passes updated message fields and interest lists to the Interest Entitlement Filter FAM 1108. An interest list contains a set of unique identifiers for users/applications that registered interest in receiving updates for the financial instrument." Column 24, lines 27-32 discloses "By maintaining an interest list in the composite record, the Ticker Plant allows a subscription to include all transactions for a given financial instrument on every exchange upon which it trades. Preferably, each interest list for a given record is stored with that record in the record storage memory."

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It would have been obvious to one of ordinary skill in the art at the time of the invention to [combine/modify] the method of Hamati and Kelleher with the technique of Parsons because it is an easy and convenient way to improved processing performance.

Claim 19

Hamati & Kelleher discloses the limitations as shown in the rejection of Claim 2 above. Hamati & Kelleher do not disclose the limitation of *wherein the processing step comprises: resolving each of a plurality of limit order events to at least one record associated with an order book in a data structure; and updating the records based on the content of the plurality of limit order events*. However, Parsons, in at least column 25, lines 20-34 discloses "Another sub-block may process the stream of returned list blocks to resolve regional record addresses. The last sub-block of the address resolution block passes the regional and composite record addresses to the cache determination block. By tracking the sequence of record addresses, this block determines the physical location of the "current" (most up-to-date) records: in the record cache or in the record storage memory. The cache determination block passes the physical record pointers to the record retrieval block. The record retrieval block fetches the records from the specified locations, loads them into the processing buffers for updating, then signals the processors to begin processing."

It would have been obvious to one of ordinary skill in the art at the time of the invention to [combine/modify] the method of Hamati and Kelleher with the technique of Parsons because it is an easy and convenient way to improved processing performance.

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Claim 20

Hamati & Kelleher discloses the limitations as shown in the rejection of Claim 2 above. Hamati & Kelleher do not disclose the limitation of *wherein the enriched limit order events comprises a stream view of a plurality of order books associated with the limit order events*. However, Parsons, in at least column 11, lines 50-56 discloses "The order information for each instrument is received from a variety of different trading venues in stream 106 and is aggregated together to form one holistic view of the market for that particular instrument. The order book server is configured to respond to requests from workstation 104 users or application programs 150 to present the book in a number of different ways. There are a variety of different "views"...."

It would have been obvious to one of ordinary skill in the art at the time of the invention to [combine/modify] the method of Hamati and Kelleher with the technique of Parsons because it is an easy and convenient way to improved processing performance.

Claim 21

Hamati & Kelleher discloses the limitations as shown in the rejection of Claim 2 above. Hamati & Kelleher do not disclose the limitation of *wherein the enriched limit order events comprises a summary view of a plurality of order books associated with the limit order events*. However, Parsons, in at least column 11, lines 56-65 discloses "There are a variety of different "views", including but not limited to: a "top slice" of the book that returns orders whose prices are considered to be within a specified number of price points of the best price available in the market (the best price being considered to be the "top" of the book); a price aggregate view where orders at the same price point are aggregated together to create entries that are indicative of the total number of orders available at each price point; and an ordinary view with specific trading venues (which are the source of orders) excluded."

It would have been obvious to one of ordinary skill in the art at the time of the invention to [combine/modify] the method of Hamati and Kelleher with the technique of Parsons because it is an easy and convenient way to improved processing performance.

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Claim 22

Hamati & Kelleher discloses the limitations as shown in the rejection of Claim 2 above. Kelleher discloses a coprocessor in the Abstract. Hamati & Kelleher do not disclose the limitation of *a ticker plant*. However, Parsons, in at least column 4, lines 22-42 discloses "Also disclosed as an embodiment of the invention is a ticker plant that is configured to process financial market data with a combination of software logic and firmware logic. Through firmware pipelines deployed on the ticker plant and efficient software control and management over data flows to and from the firmware pipelines, the inventors herein believe that the ticker plant of the preferred embodiment is capable of greatly accelerating the speed with which financial market data is processed. In a preferred embodiment, financial market data is first processed within the ticker plant by software logic. The software logic controls and manages the flow of received financial market data into and out of the firmware logic deployed on the reconfigurable logic device(s), preferably in a manner such that each financial market data message travels only once from the software logic to the firmware logic and only once from the firmware logic back to the software logic. As used herein, the term "ticker plant" refers to a plurality of functional units, such as functional units 102 depicted in FIG. 1, that are arranged together to operate on a financial market data stream 106 or data derived therefrom."

It would have been obvious to one of ordinary skill in the art at the time of the invention to [combine/modify] the method of Hamati and Kelleher with the technique of Parsons because it is an easy and convenient way to improved processing performance.

Double Patenting

14. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the “right to exclude” granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); *In re Thornton*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on nonstatutory double patenting provided the reference application or patent either is shown to be commonly owned with the examined application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement. See MPEP § 717.02 for applications subject to examination under the first inventor to file provisions of the AIA as explained in MPEP § 2159. See MPEP §§ 706.02(I)(1) - 706.02(I)(3) for applications not subject to examination under the first inventor to file provisions of the AIA. A terminal disclaimer must be signed in compliance with 37 CFR 1.321(b).

The USPTO Internet website contains terminal disclaimer forms which may be used. Please visit www.uspto.gov/patent/patents-forms. The filing date of the application in which the form is filed determines what form (e.g., PTO/SB/25, PTO/SB/26, PTO/AIA/25, or PTO/AIA/26) should be used. A web-based eTerminal Disclaimer may be filled out completely online using web-screens. An eTerminal Disclaimer that meets all requirements is auto-processed and approved immediately upon submission. For more information about eTerminal Disclaimers, refer to www.uspto.gov/patents/process/file/efs/guidance/eTD-info-I.jsp.

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15. Claims 44-46 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 81 & 82 of U.S. Patent No. 8,768,805 B2. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 44-46 is generic to all that is recited in claim claims 81 & 82 of U.S. Patent No. 8,768,805 B2. That is, claims 81 & 82 of U.S. Patent No. 8,768,805 B2 falls entirely within the scope of claim 44-46 or, in other words, claim 44-46 is anticipated by claims 81 & 82 of U.S. Patent No. 8,768,805 B2.

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Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KITO R. ROBINSON whose telephone number is (571)270-3921. The examiner can normally be reached on Monday-Friday 7:30am-5:00pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, RYAN DONLON can be reached on (571) 270-3602. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KITO R ROBINSON/
Primary Examiner, Art Unit 3695

30 June 2017

Notice of References Cited	Application/Control No. 14/315,571	Applicant(s)/Patent Under Reexamination TAYLOR ET AL.	
	Examiner KITO R. ROBINSON	Art Unit 3695	Page 1 of 1

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-7,598,958 B1	10-2009	Kelleher; Brian M.	G06F9/3877	345/502
*	B	US-7,921,046 B2	04-2011	Parsons; Scott	G06Q40/00	705/35
*	C	US-8,175,946 B2	05-2012	Hamati; Gheis Henri	G06Q30/0202	705/36R
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Receipt date: 10/21/2016

14315571 - GAU: 3695

Doc code: IDS

PTO/SB/08a (03-15)

Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14315571
	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3692
	Examiner Name	Johnson, Gregory L.
	Attorney Docket Number	57451-133596

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	1	20050203938	A1	2005-09-15	Hoelt et al.			
	2	20060075404	A1	2006-04-06	Rosu et al.			
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	1	2006/059312	WO	A2	2006-06-08	Koninkl Philips Electronics Nv		
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Examiner Signature	/KITO R ROBINSON/	Date Considered	06/28/2017

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CERTIFICATION STATEMENT

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See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Benjamin L. Volk, Jr./	Date (YYYY-MM-DD)	2016-10-21
Name/Print	Benjamin L. Volk, Jr.	Registration Number	48,017

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7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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Receipt date: 05/26/2017

14315571 - GAU: 3695

Doc code: IDS

PTO/SB/08a (03-15)

Doc description: Information Disclosure Statement (IDS) Filed

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	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3695
	Examiner Name	Robinson, Kito R.
	Attorney Docket Number	57451-133596

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	6247060	B1	2001-06-12	Boucher et al.	
	2	6591302	B2	2003-07-08	Boucher et al.	
	3	7089326	B2	2006-08-08	Boucher et al.	
	4	9582831	B2	2017-02-28	Parsons et al.	

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	1	20020095519	A1	2002-07-18	Philbrick et al.	
	2	20030217306	A1	2003-11-20	Harthcock et al.	

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Signature	/Benjamin L. Volk, Jr./	Date (YYYY-MM-DD)	2017-05-26
Name/Print	Benjamin L. Volk, Jr.	Registration Number	48,017

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14315571 - GAU: 3695

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	Art Unit	3693		
	Examiner Name	Merchant, Shahid R.		
	Attorney Docket Number	57451-133596		

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
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	2	3082402		1963-03-19	Scantlin	
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43	5267148		1993-11-30	Kosaka et al.	
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22	WOOSTER et al., "HTTPDUMP Network HTTP Packet Snooper", April 25, 1996	☐

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14315571
	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3693
	Examiner Name	Merchant, Shahid R.
	Attorney Docket Number	57451-133596

23	WORBOYS, "GIS: A Computing Perspective", 1995, pp. 245-247, 287, Taylor & Francis Ltd.	☐
24	YAMAGUCHI ET AL., "High Speed Homology Search with FPGAs", Proceedings Pacific Symposium on Biocomputing, January 3-7, 2002, pp 271-282, Vol. 7, Online, Lihue, Hawaii, USA	☐
25	YAN et al., "Enhancing Collaborative Spam Detection with Bloom Filters", 2006, IEEE, pages 414-425	☐
26	YOSHITANI ET AL., "Performance Evaluation of Parallel Volume Rendering Machine Re Volver/C40", Study Report of Information Processing Society, March 5, 1999, pp. 79-84, Vol. 99, No. 21	☐
27	ZIV ET AL., " A Universal Algorithm for Sequential Data Compression", IEEE Trans. Inform. Theory, IT-23(3): 337-343 (1997)	☐
28	US Patent Application Serial No. 61/570670 filed December 14, 2011 (Taylor et al.)	☐

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	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
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	Examiner Name	Merchant, Shahid R.
	Attorney Docket Number	57451-133596

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

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☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

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A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Benjamin L. Volk, Jr./	Date (YYYY-MM-DD)	2014-11-11
Name/Print	Benjamin L. Volk, Jr.	Registration Number	48017

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3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
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Receipt date: 02/19/2016

14315571 - GAU: 3695

Doc code: IDS

PTO/SB/08a (03-15)

Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14315571
	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3693
	Examiner Name	Merchant, Shahid R
	Attorney Docket Number	57451-133596

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear	
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Application Number	14315571
Filing Date	2014-06-26
First Named Inventor	David E. Taylor
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	1	Office Action for CA Application 2744746 dated February 5, 2016	
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Signature	/Benjamin L. Volk, Jr./	Date (YYYY-MM-DD)	2016-02-19
Name/Print	Benjamin L. Volk, Jr.	Registration Number	48017

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SERIAL NUMBER	FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.		
14/315,571	06/26/2014	705	3695	57451-133596		
APPLICANTS IP Reservoir, LLC, St. Louis, MO; INVENTORS David E. Taylor, St. Louis, MO; Scott Parsons, St. Charles, MO; Jeremy Walter Whatley, Ballwin, MO; Richard Bradley, St. Louis, MO; Kwame Gyang, St. Louis, MO; Michael DeWulf, St. Louis, MO; ** CONTINUING DATA ***** This application is a DIV of 13/154,804 06/07/2011 PAT 8768805 which is a DIV of PCT/US2009/067935 12/14/2009 which claims benefit of 61/122,673 12/15/2008 ** FOREIGN APPLICATIONS ***** ** IF REQUIRED, FOREIGN FILING LICENSE GRANTED ** ** SMALL ENTITY ** 07/08/2014						
Foreign Priority claimed ☐ Yes ☒ No 35 USC 119(a-d) conditions met ☐ Yes ☒ No Verified and Acknowledged <u>/KITO R ROBINSON/</u> Examiner's Signature		☐ Met after Allowance Initials	STATE OR COUNTRY MO	SHEETS DRAWINGS 17	TOTAL CLAIMS 46	INDEPENDENT CLAIMS 3
ADDRESS THOMPSON COBURN LLP ONE US BANK PLAZA SUITE 3500 ST LOUIS, MO 63101 UNITED STATES						
TITLE Method and Apparatus for High-Speed Processing of Financial Market Depth Data						
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EAST Search History**EAST Search History (Prior Art)**

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	159	Parsons-Scott\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:34
L2	0	l1 with (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:34
L3	11	Whatley-Jeremy-Walter\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:35
L4	0	l3 with (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:35
L5	427	Bradley-Richard\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:35
L6	0	l5 with (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:36
L7	25	Gyang-Kwame\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:36
L8	0	l7 with (enriched or ephemeral)	US-PGPUB;	OR	ON	2017/06/30

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L9	11	DeWulf-Michael\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:36
L10	0	19 with (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:36
L11	142	Taylor-David-E\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:37
L12	0	111 with (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:37
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L14	1200206	13 ans (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:38
L15	6	13 and (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:38
L16	6	15 and (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/06/30 15:38

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L18	12	111 and (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:39
S1	73	Taylor-David-E\$.inv.	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/27 15:22
S2	1	("8768805").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/06/27 15:22
S3	6	S1 and (stream\$4 same (limit near2 order))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/27 15:25
S4	7	S1 and ((limit near2 order))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/27 15:25
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S6	7	705/36 and (stream\$4 same (limit near2 order))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/27 16:42
S7	3	705/36 and ((stream\$4 near2 (data or information or price)) same (limit near2 order))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/27 17:07
S8	80	705/36 and ((stream\$4 near2 (data or information or price)) and (limit near2 order))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/27 17:08
S9	30	705/36 and ((stream\$4 near2 (data or information or price)) and (limit near2 order) and (order near2 book))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/27 17:08
S10	0	705/36 and ((stream\$4 near2 (data or information or price)) and (limit near2 order) and (order near2 book) and enrich\$3)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/27 17:08
S11	13	705/36 and ((stream\$4 near2 (data or information or price)) and (limit near2 order) same (order near2 book))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 09:22
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		"20070237327" "20080114725" "20080275805" "20090182683" "20090287628" "20110178911" "20110178919" "20110231446" "20110246353" "4385393" "4550436" "4823306" "5101353" "5101424" "5140692" "5375055" "5396253" "5500793" "5517642" "5802290" "5884286" "6028939" "6044407" "6263321" "6321258" "6415269" "6624761" "6691301" "7089206" "7103569" "7167980" "7181608" "7487327" "7603303" "7668849" "RE36946" "20040010612" "20050108518" "20080162378" "20140310717" "8055601" "9020928" "20020198813" "20090037514" "9176775" "20030217306" "20090019219" "6247060" "20010042040" "20020023010" "20020080871" "20020129140" "20020199173" "20030037321" "20030065607" "20030187662" "20030191876" "20030221013" "20040015502" "20050187846" "20050187847" "20050240510" "20060059083" "20060282369" "20070067108" "20070118457" "20070244859" "20070294157" "20070294162" "20080133453" "20110199243").PN.				
S13	0	S12 and (chip-processor)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:16
S14	0	S12 and (chip-multi-processor and (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:17
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S23	1	705/35 and (chip-multi-processor and (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:22

S24	0	705/36 and (chip-multi-processor and (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:22
S25	2	705/\$\$ and (chip-multi-processor and (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:23
S26	11	705/\$\$ and ((chip near2 multi near2 processor) and (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:23
S27	1	streaming same ((chip near2 multi near2 processor) and (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:24
S28	542	((chip near2 multi near2 processor) and (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:25
S29	363	((chip near2 multi near2 processor) same (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:25
S30	3	(regional and composite) near2 price near2 volume	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:38
S31	3	(regional and composite) near6 price near2 volume	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:40
S32	6	(regional and composite) same price near2 volume	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:40
S33	5	(S12 or S15 or S17 or S19 or S21) and ((regional and composite) same price near2 volume)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:41
S34	42	(S12 or S15 or S17 or S19 or S21) and (price near2 volume)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:41
S35	30	(S12 or S15 or S17 or S19 or S21) and (regional and composite)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:42
S36	72	(ephemeral near2 order)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/29 17:01
S37	5	705/35 and (ephemeral near2 order)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/29 17:01
S38	0	705/36 and (ephemeral near2 order)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/29 17:01
S39	12	705/\$\$ and (ephemeral near2 order)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/29 17:01
S40	9	705/36 and (ephemeral)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:13
S41	53	705/35 and (ephemeral)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:15
S42	7	(limit near2 order) with mapping same identifier	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:20

S43	17	(limit near2 order) same mapping same identifier	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:20
S44	372	(limit near2 order) with identifier	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:21
S45	192	(limit near2 order) near4 identifier	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:21
S46	388	(limit near2 order) near4 event	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:22
S47	15	705/35 and ((limit near2 order) near4 event)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:22
S48	8	705/36 and ((limit near2 order) near4 event)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:23
S49	5	705/36 and ((limit near2 order) near4 identifier)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:24
S50	15	705/35 and ((limit near2 order) near4 identifier)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:25
S51	1	705/35 and ((ephemeral) near4 identifier)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:41
S52	13	705/\$\$ and ((ephemeral) near4 identifier)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:41
S53	10	705/\$\$ and (identif\$4 near4 ephemeral near4 (order or transaction))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:43
S54	10	705/\$\$ and (identif\$4 near6 ephemeral near6 (order or transaction))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:43
S55	11	705/\$\$ and (identif\$4 near8 ephemeral near8 (order or transaction))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:44
S56	10	705/\$\$ and (identif\$4 with ephemeral near8 (order or transaction))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:44
S57	14	705/\$\$ and (identif\$4 with ephemeral with (order or transaction))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:44
S58	14	705/\$\$ and (identif\$4 with ephemer\$3 with (order or transaction))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:47
S59	14	705/\$\$ and (identif\$4 with ephemer\$3 with (order or transaction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 11:47
S60	0	705/\$\$ and (identif\$4 with ephemer\$3 with (commodit\$3))	US-PGPUB; USPAT; USOCR;	OR	ON	2017/06/30 11:48

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S61	93	705/\$\$ and (identif\$4 near4 ephemer\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 11:48

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Receipt date: 06/22/2016

14315571 - GAU: 3695

Doc code: IDS

Doc description: Information Disclosure Statement (IDS) Filed

PTO/SB/08a (03-15)

Approved for use through 07/31/2016. OMB 0651-0031

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	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3692
	Examiner Name	Johnson, Gregory L
	Attorney Docket Number	57451-133596

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	1	6243753	B1	2001-06-05	Machin et al.			
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	1	20010003193	A1	2001-06-07	WOODRING et al.			
	2	20070025351	A1	2007-02-01	Cohen			
	3	20100306479	A1	2010-12-02	Ezzat			
	4	20160070583	A1	2016-03-10	Chamberlain et al.			
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

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Filing Date	2014-06-26
First Named Inventor	David E. Taylor
Art Unit	3692
Examiner Name	Johnson, Gregory L
Attorney Docket Number	57451-133596

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Examiner Signature	/KITO R ROBINSON/	Date Considered	06/28/2017

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¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	14315571
Filing Date	2014-06-26
First Named Inventor	David E. Taylor
Art Unit	3692
Examiner Name	Johnson, Gregory L
Attorney Docket Number	57451-133596

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Benjamin L. Volk, Jr./	Date (YYYY-MM-DD)	2016-06-22
Name/Print	Benjamin L. Volk, Jr.	Registration Number	48017

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Receipt date: 11/11/2014

14315571 - GAU: 3695

Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0651-0031

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14315571	
	Filing Date		2014-06-26	
	First Named Inventor	David E. Taylor		
	Art Unit	3693		
	Examiner Name	Merchant, Shahid R.		
	Attorney Docket Number	57451-133596		

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Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	5826075		1998-10-20	Bealkowski et al.	
	2	5845266		1998-12-01	Lupien et al.	
	3	5857176		1999-01-05	Ginsberg	
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36	International Preliminary Report on Patentability (Chapter I) for PCT/US2009/067935 issued June 30, 2011	☐

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STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	14315571
Filing Date	2014-06-26
First Named Inventor	David E. Taylor
Art Unit	3693
Examiner Name	Merchant, Shahid R.
Attorney Docket Number	57451-133596

37	International Search Report and Written Opinion for PCT/US2009/067935 dated April 30, 2010	☐
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42	KEUTZER ET AL., "A Survey of Programmable Platforms - Network Proc", University of California-Berkeley, pp. 1-29	☐
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49	LOCKWOOD ET AL., "Field Programmable Port Extender (FPX) for Distributed Routing and Queuing", ACM International Symposium on Field Programmable Gate Arrays (FPGA 2000), Monterey, CA, February 2000, pp. 137-144	☐
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Signature	/Benjamin L. Volk, Jr./	Date (YYYY-MM-DD)	2014-11-11
Name/Print	Benjamin L. Volk, Jr.	Registration Number	48017

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14315571 - GAU: 3695

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32	Prosecution History for US Application 13/077,036 filed March 31, 2011 (Parsons et al.)	☐
33	Prosecution History for US Application 13/132408 filed December 21, 2011 (Taylor et al.)	☐

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US CLASSIFICATION SEARCHED			
Class	Subclass	Date	Examiner
705	35	06/30/2017	KR

SEARCH NOTES		
Search Notes	Date	Examiner
EAST: INVENTOR SEARCH	06/30/2017	KR

INTERFERENCE SEARCH			
US Class/ CPC Symbol	US Subclass / CPC Group	Date	Examiner

<i>Index of Claims</i> 	Application/Control No. 14315571	Applicant(s)/Patent Under Reexamination TAYLOR ET AL.
	Examiner KITO R ROBINSON	Art Unit 3695

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant			☐ CPA			☐ T.D.			☐ R.1.47		
CLAIM		DATE									
Final	Original	06/30/2017									
	1	✓									
	2	✓									
	3	✓									
	4	✓									
	5	✓									
	6	✓									
	7	✓									
	8	✓									
	9	✓									
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	11	✓									
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	30	✓									
	31	✓									
	32	✓									
	33	✓									
	34	✓									
	35	✓									
	36	✓									

<i>Index of Claims</i> 	Application/Control No. 14315571	Applicant(s)/Patent Under Reexamination TAYLOR ET AL.
	Examiner KITO R ROBINSON	Art Unit 3695

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☐ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	06/30/2017								
	37	✓								
	38	✓								
	39	✓								
	40	✓								
	41	✓								
	42	✓								
	43	✓								
	44	✓								
	45	✓								
	46	✓								

Receipt date: 11/11/2015

14315571 - GAU: 3695

Doc code: IDS

PTO/SB/08a (03-15)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2016. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14315571	
	Filing Date		2014-06-26	
	First Named Inventor	David E. Taylor		
	Art Unit		3693	
	Examiner Name	Merchant, Shahid R		
	Attorney Docket Number		57451-133596	

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	7376755		2008-05-20	Pandya	
	2	7415723		2008-08-19	Pandya	
	3	7487264		2009-02-03	Pandya	
	4	7536462		2009-05-19	Pandya	
	5	7627693		2009-12-01	Pandya	
	6	7631107		2009-12-08	Pandya	
	7	7827190		2010-11-02	Pandya	
	8	7831606		2010-11-09	Pandya	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
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Application Number	14315571
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First Named Inventor	David E. Taylor
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Attorney Docket Number	57451-133596

9	7831607		2010-11-09	Pandya	
10	7870217		2011-01-11	Pandya	
11	7890692		2011-02-15	Pandya	
12	7899976		2011-03-01	Pandya	
13	7899977		2011-03-01	Pandya	
14	7899978		2011-03-01	Pandya	
15	7912808		2011-03-22	Pandya	
16	7944920		2011-05-17	Pandya	
17	7996348		2011-08-09	Pandya	
18	8005966		2011-08-23	Pandya	
19	8030888		2011-10-04	Pandya et al.	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
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20	8051022		2011-11-01	Pandya	
21	8055601		2011-11-08	Pandya	
22	8181239		2012-05-15	Pandya	
23	8200599		2012-06-12	Pandya	
24	8374986		2013-02-12	Indeck et al.	
25	8601086		2013-12-03	Pandya	
26	8762249	B2	2014-06-24	Taylor et al.	
27	8768805	B2	2014-07-01	Taylor et al.	
28	8768888	B2	2014-07-01	Chamberlain et al.	
29	8843408	B2	2014-09-23	Singla et al.	
30	8879727	B2	2014-11-04	Taylor et al.	

**INFORMATION DISCLOSURE
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31	8880501	B2	2014-11-04	Indeck et al.	
32	8983063	B1	2015-03-17	Taylor et al.	
33	9020928	B2	2015-04-28	Indeck et al.	
34	9047243	B2	2015-06-02	Taylor et al.	

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Examiner Initial*	Cite No	Publication Number	Kind Code ¹	Publication Date	Name of Patentee or Applicant of cited Document	Pages, Columns, Lines where Relevant Passages or Relevant Figures Appear
	1	20020038276	A1	2002-03-28	Buhannic et al.	
	2	20040010612		2004-01-15	Pandya	
	3	20050108518		2005-05-19	Pandya	
	4	20050228735	A1	2005-10-13	Duquette	
	5	20060282281	A1	2006-12-14	Egetoft	

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

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Filing Date	2014-06-26
First Named Inventor	David E. Taylor
Art Unit	3693
Examiner Name	Merchant, Shahid R
Attorney Docket Number	57451-133596

6	20080077793	A1	2008-03-27	Tan et al.	
7	20080162378	A1	2008-07-03	Levine et al.	
8	20080253395		2008-10-16	Pandya	
9	20100106976	A1	2010-04-29	ACIICMEZ et al.	
10	20100174770		2010-07-08	Pandya	
11	20110291615		2011-12-01	Pandya et al.	
12	20120089496		2012-04-12	Taylor et al.	
13	20120117610		2012-05-10	Pandya	
14	20130018835		2013-01-17	PANDYA	
15	20130151458		2013-06-13	Indeck et al.	
16	20140180903	A1	2014-06-26	Parsons et al.	

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14315571	
	Filing Date		2014-06-26	
	First Named Inventor	David E. Taylor		
	Art Unit	3693		
	Examiner Name	Merchant, Shahid R		
	Attorney Docket Number	57451-133596		

	17	20140180904	A1	2014-06-26	Parsons et al.	
	18	20140180905	A1	2014-06-26	Parsons et al.	
	19	20140181133	A1	2014-06-26	Parsons et al.	
	20	20140310717	A1	2014-10-16	Chamberlain et al.	
	21	20150023501	A1	2015-01-22	Taylor et al.	
	22	20150052148	A1	2015-02-19	Indeck et al.	
	23	20150055776	A1	2015-02-26	Taylor et al.	

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	1	09-269901	JP	A	1997-10-14	Hitachi Ltd.		☐
	2	2002117232	JP	A	2002-04-19	Konami Co Ltd		☐

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
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Art Unit	3693
Examiner Name	Merchant, Shahid R
Attorney Docket Number	57451-133596

3	2002352070	JP	A	2002-12-06	Good Lots Kk		☐
4	2006293852	JP	A	2006-10-26	Hitachi Ltd		☐
5	2003104943	WO	A2	2003-12-18	Pandya Ashish A		☐
6	2005081855	WO	A2	2005-09-09	Pandya Ashish A		☐
7	2005114339	WO	A2	2005-12-01	Pandya Ashish A		☐
8	2006060571	WO	A2	2006-06-08	Pandya Ashish A		☐
9	2007/016078	WO	A2	2007-02-08	CFPH, LLC		☐
10	2007/149378	WO	A2	2007-12-27	ITG Software Solutions, Inc.		☐
11	2007079095	WO	A2	2007-07-12	Pandya Ashish A		☐
12	2008/036197	WO	A2	2008-03-27	Reuters Limited,		☐
13	2008073824	WO	A1	2008-06-19	Pandya Ashish A		☐

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	Filing Date		2014-06-26
	First Named Inventor	David E. Taylor	
	Art Unit	3693	
	Examiner Name	Merchant, Shahid R	
Attorney Docket Number		57451-133596	

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	1	COMPTON ET AL., "Reconfigurable Computing: A Survey of Systems and Software", University of Washington, ACM Computing Surveys, Jun. 2, 2002, pp. 171-210, Vol. 34 No. 2, <http://www.idi.ntnu.no/emner/tdt22/2011/reconfig.pdf>	☐	
	2	KUNITOMO, Database First Edition, Jun. 28, 2008, pp. 174-175, Juse Press, Ltd., Japan	☐	
	3	SUGAWARA ET AL., "Over 10Gbps String Matching Mechanism for Multi-Stream Packet Scanning Systems", Field Programmable Logic and Application Lecture Notes in Computer Science, 2004, pp. 484-493, Vol. 3203	☐	
	4	Prosecution History for US Application 13/154,804, now USPN 8,768,805, filed June 7, 2011 (Taylor et al.)	☐	
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Examiner Signature	/KITO R ROBINSON/		Date Considered	06/28/2017
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¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.				

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14315571
	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3693
	Examiner Name	Merchant, Shahid R
	Attorney Docket Number	57451-133596

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

☐ That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

☐ See attached certification statement.

☐ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Benjamin L. Volk, Jr./	Date (YYYY-MM-DD)	2015-11-11
Name/Print	Benjamin L. Volk, Jr.	Registration Number	48017

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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Electronic Petition Request	TERMINAL DISCLAIMER TO OBVIATE A DOUBLE PATENTING REJECTION OVER A "PRIOR" PATENT	
Application Number	14315571	
Filing Date	26-Jun-2014	
First Named Inventor	David Taylor	
Attorney Docket Number	57451-133596	
Title of Invention	Method and Apparatus for High-Speed Processing of Financial Market Depth Data	
☒ Filing of terminal disclaimer does not obviate requirement for response under 37 CFR 1.111 to outstanding Office Action ☒ This electronic Terminal Disclaimer is not being used for a Joint Research Agreement.		
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Applicant claims the following fee status: ☒ Small Entity ☐ Micro Entity ☐ Regular Undiscounted	
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Signature	/Benjamin L. Volk, Jr./
Name	Benjamin L. Volk, Jr.

*Statement under 37 CFR 3.73(b) is required if terminal disclaimer is signed by the assignee (owner).
 Form PTO/SB/96 may be used for making this certification. See MPEP § 324.

Electronic Patent Application Fee Transmittal				
Application Number:		14315571		
Filing Date:		26-Jun-2014		
Title of Invention:		Method and Apparatus for High-Speed Processing of Financial Market Depth Data		
First Named Inventor/Applicant Name:		David E. Taylor		
Filer:		Benjamin Lowell Volk/Laurie Poss		
Attorney Docket Number:		57451-133596		
Filed as Small Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
STATUTORY OR TERMINAL DISCLAIMER	2814	1	160	160
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				160

Doc Code: DISQ.E.FILE

Document Description: Electronic Terminal Disclaimer – Approved

Application No.: 14315571

Filing Date: 26-Jun-2014

Applicant/Patent under Reexamination: Taylor

Electronic Terminal Disclaimer filed on January 3, 2018

☒ APPROVED

This patent is subject to a terminal disclaimer

☐ DISAPPROVED

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Electronic Acknowledgement Receipt	
EFS ID:	31395316
Application Number:	14315571
International Application Number:	
Confirmation Number:	1085
Title of Invention:	Method and Apparatus for High-Speed Processing of Financial Market Depth Data
First Named Inventor/Applicant Name:	David E. Taylor
Customer Number:	21888
Filer:	Benjamin Lowell Volk/Laurie Poss
Filer Authorized By:	Benjamin Lowell Volk
Attorney Docket Number:	57451-133596
Receipt Date:	03-JAN-2018
Filing Date:	26-JUN-2014
Time Stamp:	15:44:30
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$160
RAM confirmation Number	010418INTEFSW00002129200823
Deposit Account	200823
Authorized User	Laurie Poss
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.17 (Patent application and reexamination processing fees) 37 CFR 1.21 (Miscellaneous fees and charges)	

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1	Terminal Disclaimer-Filed (Electronic)	eTerminal-Disclaimer.pdf	33433	no	2
			17ef192635797f7208edb70c73986d49544f44f8		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	31001	no	2
			dcf6ae5c43d4eefd1d3c0b1918e4144362bdc1d3		
Warnings:					
Information:					
Total Files Size (in bytes):			64434		
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Application No. 14/315,571
Attorney Docket No. 57451-133596

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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I hereby certify that this correspondence has been e-filed with the U.S. Patent and Trademark Office on January 3, 2018.

/Benjamin L. Volk, Jr./
Benjamin L. Volk, Jr.
Reg. No. 48,017

In re application of:	:	
Taylor et al.	:	
	:	
Serial No.: 14/315,571	:	Examiner: Robinson, Kito R.
	:	
Filing Date: June 26, 2014	:	Group Art Unit: 3695
	:	
For: Method and Apparatus for High-	:	
Speed Processing of Financial	:	
Market Depth Data	:	

Amendment and Response A

In response to the outstanding Office Action, Applicant submits the following amendment and remarks.

Amendments to the Specification are presented on pages 2-3.

Amendments to the Claims are reflected in the listing of claims which begins on page 4 of this paper.

Remarks begin on page 22 of this paper.

Amendments to the Specification:

Please replace the “Cross-Reference and Priority Claim to Related Patent Applications” section with the following replacement section (additions underlined; deletions struck-through or double-bracketed).

This application is a divisional of U.S. patent application 13/154,804, filed June 7, 2011, now U.S. Pat. No. [[____]] 8,768,805, which is a divisional of International Patent Application No. PCT/US2009/067935, filed December 14, 2009, and designating the U.S., which claims priority to U.S. patent application 61/122,673, filed December 15, 2008, entitled “Method and Apparatus for High-Speed Processing of Financial Market Depth Data”, the entire disclosures of each of which are incorporated herein by reference.

This application is related to (1) U.S. patent application 12/013,302, filed January 11, 2008, entitled “Method and System for Low Latency Basket Calculation”, published as U.S. Patent Application Publication 2009/0182683, (2) U.S. patent application 11/765,306, filed June 19, 2007, entitled “High Speed Processing of Financial Information Using FPGA Devices”, published as U.S. Patent Application Publication 2008/0243675, (3) U.S. patent application 11/760,211, filed June 8, 2007, entitled “Method and System for High Speed Options Pricing”, published as U.S. Patent Application Publication 2007/0294157, and (4) U.S. patent application 11/561,615, filed November 20, 2006, entitled “Method and Apparatus for Processing Financial Information at Hardware Speeds Using FPGA Devices”, published as U.S. Patent Application Publication 2007/0078837, the entire disclosures of each of which are incorporated herein by reference.

This application is also related to (1) U.S. patent application 13/154,824, filed June 7, 2011, now U.S. Pat. No. [[____]] 8,762,249, which is a divisional of International Patent Application No. PCT/US2009/067935 and claims priority to U.S. patent application 61/122,673, and (2) U.S. patent application 13/132,408,

Application No. 14/315,571
Attorney Docket No. 57451-133596

which is a national phase entry of International Patent Application No.
PCT/US2009/067935 and claims priority to U.S. patent application 61/122,673.

Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (currently amended) A method for applying specific computer technology to reduce latency and increase throughput with respect to streaming data enrichment, the method comprising:

streaming data representative of a plurality of limit order events pertaining to a plurality of financial instruments into a coprocessor, the coprocessor including an order engine and a price engine;

the order engine accessing a plurality of limit order records based on the streaming limit order event data;

the order engine generating updated limit order data based on the accessed limit order records and processing the streaming limit order event data with the coprocessor to determine order book data associated with the limit order events;

the price engine accessing a plurality of price point records based on the streaming limit order event data;

the price engine generating updated price point data based on the accessed price point records and the streaming limit order event data; and

the coprocessor generating a stream of enriched limit order events with the coprocessor, wherein the enriched limit order events are enriched with the updated limit order and price point data indicative of the determined order book data; and

wherein the order engine and the price engine perform their steps in parallel with each other as the limit order event data streams through the coprocessor.

2. (currently amended) The method of claim 1 wherein the coprocessor comprises a member of the group consisting of a reconfigurable logic device, a chip-multi-processor

(CMP), and a graphics processing unit (GPU), and wherein the order engine and the price engine are deployed on the member.

3. (currently amended) The method of claim 2 wherein the stream generating step comprises the coprocessor appending a plurality of data fields corresponding to the updated limit order and price point data to a plurality of limit order events to generate the enriched limit order events.

4. (currently amended) The method of claim 3 wherein the appending step comprises the coprocessor appending at least one price volume field to a limit order event.

5. (original) The method of claim 4 wherein the at least one price volume field comprises a regional price volume field.

6. (original) The method of claim 4 wherein the at least one price volume field comprises a composite price volume field.

7. (currently amended) The method of claim 3 wherein the appending step comprises the coprocessor appending at least one price order count field to a limit order event.

8. (original) The method of claim 7 wherein the at least one price order count field comprises a regional price order count field.

9. (original) The method of claim 7 wherein the at least one price order count field comprises a composite price order count field.

10. (currently amended) The method of claim 3 wherein the appending step comprises the coprocessor appending at least one order attribute vector field to a limit

order event, the order attribute vector indicative of an impact of an attribute on an order book associated with the limit order event.

11. (currently amended) The method of claim 3 wherein the appending step comprises the coprocessor appending at least one price attribute vector field to a limit order event, the price attribute vector indicative of an impact of an attribute on a price point order book associated with the limit order event.

12. (original) The method of claim 11 wherein the at least one price attribute vector field comprises a regional price attribute vector field.

13. (original) The method of claim 11 wherein the at least one price attribute vector field comprises a composite price attribute vector field.

14. (currently amended) The method of claim 3 wherein the appending step comprises the coprocessor appending at least one sort order field to a limit order event, the sort order field being indicative of a relative position of the limit order event within an associated order book.

15. (original) The method of claim 14 wherein the sort order field is indicative of a relative position of the limit order event within an associated price aggregated order book.

16. (original) The method of claim 14 wherein the sort order field is indicative of a relative position of the limit order event within an associated composite price aggregated order book.

17. (currently amended) The method of claim 3 wherein the appending step comprises the coprocessor appending at least one interest vector field to a limit order event, the interest vector field being indicative of which of a plurality of client applications are interested in receiving the enriched limit order event.
18. (original) The method of claim 17 wherein the interest vector field is further indicative of which fields of the enriched limit order event each of the plurality of client applications are interested in receiving.
19. (currently amended) The method of claim 2 wherein the ~~processing~~ order engine accessing step comprises:
 the order engine resolving each of a plurality of limit order events in the streaming limit order event data to at least one limit order record associated with an order book in a limit order records data structure; and
 the method further comprising the order engine updating the accessed limit order records based on the content of the plurality of limit order events.
20. (original) The method of claim 2 wherein the enriched limit order events comprises a stream view of a plurality of order books associated with the limit order events.
21. (original) The method of claim 2 wherein the enriched limit order events comprises a summary view of a plurality of order books associated with the limit order events.
22. (original) The method of claim 2 wherein the coprocessor is resident within a ticker plant.

23. (currently amended) The method of claim 2 wherein each of the limit order events is associated with a limit order for the financial instrument to which it pertains, ~~the method further comprising:~~

~~—accessing the order book data in a memory, the order book data comprising (1) a plurality of limit order records corresponding to a plurality of limit orders for a plurality of financial instruments and (2) a plurality of price point records corresponding to financial instruments for which there are limit order records, wherein the limit order records comprising comprise a plurality of limit order record fields, and wherein the price point records comprising comprise a plurality of price point record fields;~~

~~wherein the order engine accessing ~~processing~~ step comprises the ~~coprocessor~~ (1) order engine mapping a plurality of the limit order events to the limit order records corresponding to their associated limit orders;~~

~~—wherein the price engine accessing step comprises the price engine[[, (2)]] mapping a plurality of the limit order events to the price point records corresponding to the financial instruments for their associated limit orders, and (3) updating the mapped limit order records and the mapped price point records based on the limit order events~~

~~—the method further comprising (1) the order engine updating the limit order records based on the updated limit order data, and (2) the price engine updating the price point records based on the updated price point data; and~~

wherein the stream generating step comprises the coprocessor, for those limit order events that are mapped to limit order records and price point records, appending at least one limit order record field from the updated limit order records and at least one price point record field from the updated price point records to those limit order events to generate enriched limit order events.

24. CANCELED

25. (original) The method of claim 23 wherein the mapped limit order record for at least one of the limit order events includes a limit order record field that comprises an identifier for an attribute with respect to the determined limit order record; and

wherein the appending step comprises the coprocessor appending the attribute identifier to the at least one limit order event.

26. (original) The method of claim 25 wherein the attribute identifier is indicative of whether the determined limit order record pertains to an ephemeral regional order.

27. (original) The method of claim 25 wherein the attribute identifier is indicative of whether the determined limit order record relates to an implied liquidity.

28. (original) The method of claim 23 wherein the mapped limit order record for at least one of the limit order events includes a limit order record field that comprises an attribute identifier indicative of whether the mapped limit order record pertains to an ephemeral regional order and a limit order record field that comprises an attribute identifier indicative of whether the mapped limit order record relates to an implied liquidity, the ephemeral regional order attribute identifier and the implied liquidity attribute identifier serving as an attribute vector; and

wherein the appending step comprises the coprocessor appending the attribute vector to the at least one limit order event.

29. (original) The method of claim 23 wherein the mapped price point record for at least one of the limit order events includes a price point record field that comprises an identifier for an attribute with respect to the mapped price point record; and

wherein the appending step comprises the coprocessor appending the attribute identifier to the at least one limit order event.

30. (original) The method of claim 29 wherein the attribute identifier is indicative of whether the mapped price point record includes price data pertaining to one or more ephemeral regional orders;

wherein the mapped price point record for the at least one limit order event further includes a price point record field that comprises a volume for the one or more ephemeral regional orders and a price point record field that comprises a count for the one or more ephemeral regional orders; and

wherein the appending step further comprises the coprocessor appending the ephemeral regional order volume and the ephemeral regional order count to the at least one limit order event.

31. (original) The method of claim 29 wherein the attribute identifier is indicative of whether the mapped price point record includes price data that relates to implied liquidity;

wherein the mapped price point record for the at least one limit order event further includes a price point record field that comprises a volume for the implied liquidity and a price point record field that comprises a count for the implied liquidity; and

wherein the appending step further comprises the coprocessor appending the implied liquidity volume and the implied liquidity count to the at least one limit order event.

32. (original) The method of claim 23 wherein the mapped price point record for at least one of the limit order events includes (1) a price point record field that comprises an attribute identifier indicative of whether the mapped price point record includes price data pertaining to one or more ephemeral regional orders, (2) a price point record field that comprises a volume for the one or more ephemeral regional orders, (3) a price point record field that comprises a count for the one or more ephemeral regional orders,

(4) a price point record field that comprises an attribute identifier indicative of whether the mapped price point record includes price data that relates to implied liquidity, (5) a price point record field that comprises a volume for the implied liquidity and (6) a price point record field that comprises a count for the implied liquidity;

wherein the ephemeral regional order attribute identifier, the ephemeral regional order volume, the ephemeral regional order count, the implied liquidity attribute identifier, the implied liquidity volume, and the implied liquidity count serve as an attribute vector; and

wherein the appending step comprises the coprocessor appending the attribute vector to the at least one limit order event.

33. (currently amended) The method of claim 23 wherein the mapped price point record for at least one of the limit order events includes a price point record field that comprises a price volume and a price point record field that comprises a price count;

wherein the ~~price engine generating updating~~ step comprises the ~~coprocessor (1)~~ the price engine computing an updated price volume and an updated price count for the mapped price point record based on the at least one limit order event; ~~and (2)~~

wherein the price engine updating step comprises the price engine updating the mapped price point record with the updated price volume and the updated price count; and

wherein the appending step comprises the coprocessor appending the updated price volume and the updated price count to the at least one limit order event.

34. (currently amended) The method of claim 23 wherein the price point records comprise a plurality of regional price point records and a plurality of composite price point records;

wherein the price point records mapping step comprises the ~~coprocessor~~ price engine mapping a plurality of the limit order events to the regional and composite price

point records corresponding to the financial instruments for their associated limit orders;

wherein the price engine updating step comprises the ~~coprocessor~~ price engine updating ~~the determined limit order records~~, the determined regional price point records[[,]] and the determined composite price point records based on the limit order events; and

wherein the appending step comprises the coprocessor, for those limit order events that are mapped to limit order records, regional price point records, and composite price point records, appending at least one limit order record field from the updated limit order records, at least one price point record field from the updated regional price point records, and at least one price point record field from the updated composite price point records to the limit order events to generate the enriched limit order events.

35. (currently amended) The method of claim 34 wherein the mapped regional price point record for at least one of the limit order events includes a regional price point record field that comprises a regional price volume and a regional price point record field that comprises a regional price count;

wherein the mapped composite price point record for the at least one limit order event includes a composite price point record field that comprises a composite price volume and a composite price point record field that comprises a composite price count;

wherein the price engine generating updating step comprises the ~~coprocessor~~ price engine (1) computing an updated regional price volume and an updated regional price count for the mapped regional price point record based on the at least one limit order event, and (2) computing an updated composite price volume and an updated composite price count for the mapped composite price point record based on the at least one limit order event;[[, (3)]]

wherein the price engine updating step comprises the price engine (1) updating the mapped regional price point record with the updated regional price volume and the updated regional price count, and [(4)] (2) updating the mapped composite price point record with the updated composite price volume and the updated composite price count; and

wherein the appending step comprises the coprocessor appending the updated regional price volume, the updated regional price count, the updated composite price volume, and the updated composite price count to the at least one limit order event.

36. (currently amended) The method of claim 23 wherein the mapped limit order record for at least one of the limit order events includes a limit order record field that comprises an interest vector indicative of which of a plurality of subscribers are interested in the mapped limit order record, and wherein the mapped price point record for the at least one limit order event includes a price point record field that comprises an interest vector indicative of which of the subscribers are interested in the mapped price point record;

wherein the stream generating processing step further comprises the coprocessor combining the interest vectors from the mapped limit order record and the mapped price point record into a consolidated interest vector; and

wherein the appending step comprises the coprocessor appending the consolidated interest vector to the at least one limit order event.

37. (original) The method of claim 36 further comprising selectively communicating the streaming enriched limit order events to a plurality of downstream subscribers in accordance with their appended consolidated interest vectors.

38. CANCELED

39. (original) The method of claim 23 wherein at least one of limit order events includes data indicative of whether the at least one limit order event is an addition, modification, or deletion event; and

wherein the appending step comprises the coprocessor appending data from the mapped limit order record for the at least one limit order event based on the data indicative of whether the limit order event is an addition, modification, or deletion event.

40. (currently amended) The method of claim 23 wherein the stream generating step further comprises the coprocessor normalizing the enriched limit order event, the method further comprising:

communicating the streaming normalized enriched limit order events to a plurality of downstream subscribers.

41. (currently amended) The method of claim 2[[3]] further comprising:

storing the limit order records in wherein the memory comprises a first physical memory in which the limit order records are stored; and

storing the price point records in a second physical memory in which the price point records are stored.

42. (currently amended) An apparatus for applying specific computer technology to reduce latency and increase throughput with respect to streaming data enrichment, the apparatus comprising:

a coprocessor that includes an order engine and a price engine;

wherein the coprocessor is configured to [[(1)]] receive streaming data representative of a plurality of limit order events pertaining to a plurality of financial instruments;[[, (2)]]

wherein the order engine is configured to (1) access a plurality of limit order records based on ~~process~~ the streaming limit order event data, and (2) compute updated limit order data based on the accessed limit order records and ~~to determine order book data associated with the streaming limit order event~~[[s]] data;

wherein the price engine is configured to (1) access a plurality of price point records based on the streaming limit order event data, and (2) compute updated price point data based on the accessed price point records and the streaming limit order event data; ~~and (3)~~

wherein the coprocessor is further configured to ~~generate a stream of enrich~~[[ed]] the streaming limit order events with financial market depth data based on the computed updated limit order data and price point data, ~~wherein the enriched limit order events are enriched with data indicative of the determined order book data; and~~

wherein the order engine and the price engine are configured to perform their respective operations in parallel with each other as the limit order event data streams through the coprocessor.

43. (currently amended) The apparatus of claim 42 wherein the coprocessor comprises a member of the group consisting of a reconfigurable logic device, a chip-multi-processor (CMP), and a graphics processing unit (GPU), and wherein the order engine and the price engine are deployed on the member.

44. (currently amended) A method for applying specific computer technology to reduce latency and increase throughput with respect to streaming data enrichment, the method comprising:

streaming data representative of a plurality of limit order events into a coprocessor, wherein each of the limit order events is associated with a limit order for a financial instrument, the coprocessor including an order hash engine, an order engine, a price hash engine, and a price engine;

~~storing~~ ~~accessing~~ order book data in a memory, the order book data comprising (1) a plurality of limit order records corresponding to a plurality of limit orders for a plurality of financial instruments and (2) a plurality of price point records corresponding to financial instruments for which there are limit order records, the limit order records comprising a plurality of limit order record fields, and the price point records comprising a plurality of price point record fields;

the ~~coprocessor~~ order hash engine mapping a plurality of the limit order events to the limit order records corresponding to their associated limit orders;

the ~~coprocessor~~ price hash engine mapping a plurality of the limit order events to the price point records corresponding to the financial instruments for their associated limit orders;

the ~~coprocessor~~ order engine updating the mapped limit order records ~~and the mapped price point records~~ based on the limit order events;

the price engine updating the mapped limit order records based on the limit order events;

the coprocessor, for those limit order events that are mapped to limit order records and price point records, appending at least one limit order record field from the updated limit order records and at least one price point record field from the updated price point records to those limit order events to directly generate a plurality of enriched limit order events from the streaming data; and

the coprocessor sending the enriched limit order events downstream; and
wherein the order hash engine, the price hash engine, the order engine, and the price engine perform their respective steps in parallel as the limit order event data streams through the coprocessor.

45. (currently amended) The method of claim 44 wherein the coprocessor comprises a member of the group consisting of a reconfigurable logic device, a chip-multi-processor

(CMP), and a graphics processing unit (GPU), and wherein the order engine and the price engine are deployed on the member.

46. (original) The method of claim 45 further comprising:

the coprocessor, for each limit order event that does not map to any limit order record and does not map to any price point record, creating and storing a limit order record and a price point record in the memory for that limit order event; and

the coprocessor, for each limit order event that maps to a limit order record and does not map to any price point record, (1) creating and storing a price point record in the memory for that limit order event, and (2) appending at least one limit order record field from the updated limit order record for that limit order event to directly generate an enriched limit order event from the streaming data for that limit order event.

47. (new) The method of claim 2 wherein the streaming limit order event data comprises symbol identifiers, exchange identifiers, order reference identifiers, and prices for the limit order events, wherein the limit order records and the price point records are stored in at least one memory, wherein the coprocessor comprises a processing pipeline deployed on the member, the pipeline comprising an order hash engine, the order engine, a price hash engine, and the price engine, wherein the order engine is downstream from the order hash engine, wherein the price hash engine is downstream from the order engine, and wherein the price engine is downstream from the price hash engine, the method further comprising:

the order hash engine hashing the symbol identifiers, exchange identifiers, and the order reference identifiers in the streaming limit order event data to identify memory addresses for a plurality of limit order records pertaining to the streaming limit order event data; and

the price hash engine hashing the symbol identifiers, exchange identifiers, and the prices in the streaming limit order event data to identify memory addresses for a plurality of price point records pertaining to the streaming limit order event data;

wherein the order engine accessing step comprises the order engine accessing the limit order records based on the identified limit order record memory addresses;

wherein the price engine accessing step comprises the price engine accessing the price point records based on the identified limit order record memory addresses; and

wherein the order hash engine, the order engine, the price hash engine, and the price engine perform their steps in parallel with each other as the limit order event data streams through the coprocessor.

48. (new) The method of claim 47 further comprising:

 caching the accessed limit order records in a first cache memory;

 caching the accessed price point records in a second cache memory;

 the order engine (1) accessing limit order records from the first cache memory if available from the first cache memory, and (2) accessing limit order records from the at least one memory if not available from the first cache memory; and

 the price engine (1) accessing price point records from the second cache memory if available from the second cache memory, and (2) accessing price point records from the at least one memory if not available from the second cache memory.

49. (new) The method of claim 47 wherein the at least one memory comprises (1) a first physical memory in which the limit order records are stored, and (2) a second physical memory in which the price point records are stored.

50. (new) The apparatus of claim 43 wherein the streaming limit order event data comprises symbol identifiers, exchange identifiers, order reference identifiers, and prices for the limit order events, the apparatus further comprising:

at least one memory configured to store the limit order records and the price point records as different data structures;

wherein the coprocessor comprises a processing pipeline deployed on the member, the pipeline comprising an order hash engine, the order engine, a price hash engine, and the price engine, wherein the order engine is downstream from the order hash engine, wherein the price hash engine is downstream from the order engine, and wherein the price engine is downstream from the price hash engine;

wherein the order hash engine is configured to hash the symbol identifiers, exchange identifiers, and the order reference identifiers in the streaming limit order event data to identify memory addresses for a plurality of limit order records pertaining to the streaming limit order event data;

wherein the price hash engine is configured to hash the symbol identifiers, exchange identifiers, and the prices in the streaming limit order event data to identify memory addresses for a plurality of price point records pertaining to the streaming limit order event data;

wherein the order engine is further configured to access the limit order records based on the identified limit order record memory addresses;

wherein the price engine is further configured to access the price point records based on the identified limit order record memory addresses; and

wherein the order hash engine, the order engine, the price hash engine, and the price engine are configured to perform their respective operations in parallel with each other as the limit order event data streams through the coprocessor.

51. (new) The apparatus of claim 50 further comprising:

a first cache memory configured to cache the accessed limit order records;

a second cache memory configured to cache the accessed price point records;

wherein the order engine is further configured to (1) access limit order records from the first cache memory if available from the first cache memory, and (2) access

limit order records from the at least one memory if not available from the first cache memory; and

wherein the price engine is further configured to (1) access price point records from the second cache memory if available from the second cache memory, and (2) access price point records from the at least one memory if not available from the second cache memory.

52. (new) The apparatus of claim 50 wherein the at least one memory comprises:
a first physical memory configured to store the limit order records; and
a second physical memory configured to store the price point records.

53. (new) The method of claim 45 wherein the streaming limit order event data comprises symbol identifiers, exchange identifiers, order reference identifiers, and prices for the limit order events, wherein the coprocessor comprises a processing pipeline deployed on the member, the pipeline comprising the order hash engine, the order engine downstream from the order hash engine, the price hash engine downstream from the order engine, and the price engine downstream from the price hash engine;

wherein the order hash engine mapping step comprises the order hash engine hashing the symbol identifiers, exchange identifiers, and the order reference identifiers in the streaming limit order event data to identify memory addresses for a plurality of limit order records pertaining to the streaming limit order event data; and

wherein the price hash engine mapping step comprises the price hash engine hashing the symbol identifiers, exchange identifiers, and the prices in the streaming limit order event data to identify memory addresses for a plurality of price point records pertaining to the streaming limit order event data;

the method further comprising:

the order engine accessing the limit order records based on the identified limit order record memory addresses; and

the price engine accessing the price point records based on the identified limit order record memory addresses.

54. (new) The method of claim 53 further comprising:

 caching the accessed limit order records in a first cache memory;

 caching the accessed price point records in a second cache memory;

 the order engine (1) accessing limit order records from the first cache memory if available from the first cache memory, and (2) accessing limit order records from the memory if not available from the first cache memory; and

 the price engine (1) accessing price point records from the second cache memory if available from the second cache memory, and (2) accessing price point records from the memory if not available from the second cache memory.

55. (new) The method of claim 53 wherein the memory comprises (1) a first physical memory in which the limit order records are stored, and (2) a second physical memory in which the price point records are stored.

Remarks:

The pending claims at the time of the outstanding Office Action were claims 1-46, of which claims 1, 42, and 44 were independent. By this response, Applicant (1) amends claims 1-4, 7, 10, 11, 14, 17, 19, 23, 33-36, and 40-45 as shown herein, (2) cancels claims 24 and 38 without prejudice, and (3) adds new dependent claims 47-55. Applicant has also amended the specification to insert the patent numbers that are now available for related patent applications. No new matter is present. Examples of support for the claim amendments can be found at paragraphs 22 and 149 of the patent application (with reference to this patent application's published version, US Pat App Pub 2014/0310148). The pending claims are now claims 1-23, 25-37, and 39-52, of which claims 1, 42, and 44 remain the independent claims.

The outstanding Office Action (1) rejected the pending claims for an alleged lack of patent eligibility under 35 USC 101, (2) rejected claims 1-22 and 41-43 for alleged obviousness under 35 USC 103, and (3) rejected claims 44-46 for alleged obviousness-type double patenting. Applicant respectfully disagrees with these rejections as explained below.

35 USC 101:

The Office Action rejected all pending claims under 35 USC 101 based on an allegation that the claims are merely directed toward an abstract idea, where the alleged abstract idea is identified as "managing limit orders". Applicant respectfully disagrees.

Applicant respectfully submits that the pending claims are directed toward a specific arrangement of computer technology that improves how streaming data is enriched by reducing latency and increasing throughput relative to conventional computer systems for streaming data enrichment. Because the claims are directed toward such a technical innovation in the art, Applicant respectfully submits that the claims are non-abstract and thus patent-eligible under 35 USC 101.

More particularly, Applicant is not asserting that the claimed invention is patent-eligible because of a use of computers in a generic sense; instead Applicant is asserting that the claimed invention is patent-eligible because of a specific manner of HOW computer technology is applied to improve latency and throughput relative to conventional computer solutions in the art. This is the essence of patent-eligible innovation. Conventional computer systems in the art do not offload the enrichment of streaming limit order event data to a coprocessor as required by the claimed invention. Moreover, the claimed invention recites more than just the combination of a coprocessor with the task of enriching streaming limit order event data because the claimed invention recites a specific arrangement for how a parallel arrangement of an order engine and a price engine deployed on the coprocessor are configured to accelerate how limit order records and price point records are accessed and leveraged to enrich the streaming limit order event data. This is a significant improvement over conventional solutions in the art that employ a conventional CPU executing software to build order books and augment streaming limit order events with information from the order books. Because the claims recite a specific technological arrangement for applying specific computer technology to improve the latency and throughput performance for a computer system that enriches streaming limit order event data with financial market depth data relative to conventional computer systems in the art, the claims recite patent-eligible subject matter.

The *McRO* case demonstrates the patent-eligibility of the claims. See *McRO, Inc. v. Bandai Namco Games America, Inc.*, No. 2015-1080, 2016 WL 4896481 (Fed. Cir. 2016). As explained in *McRO*, “[t]he abstract idea exception prevents patenting a result where ‘it matters not by what process or machinery the result is accomplished.’” (See *McRO*, 2016 WL 4896481 at *6 (emphasis added) (quoting and citing *O’Reilly v. Morse*, 5 US 62, 113 (1854))). **With claim 1, it very much matters by what process or machinery the result is accomplished.** For example, once again, claim 1 recites a specific technical arrangement for achieving reduced latency and higher throughput via

the use of order and price engines (deployed on a coprocessor) that are configured to operate **in parallel with each other** in order to access limit order records and the price point records and generate updated limit order data and price point data based on the accessed records. Because these arrangements “allow for the improvement realized by the invention” (see *McRO*, 2016 WL 4896481 at *7), the claims are patent-eligible as were the claims in the *McRO* case.

Applicant further notes that the Federal Circuit decision in *Amdocs (Israel) Limited v. Openet Telecom, Inc.* (Fed. Cir. 2016) establishes that the use of a distributed computing architecture to enhance how data records are processed qualifies as non-abstract subject matter. Thus, the Federal Circuit has concluded that the use of specific computer technology to improve how records are processed is patent-eligible subject matter. In reaching its decision, the Federal Circuit found that the claim reproduced below from the *Amdocs* case was non-abstract and thus patent-eligible:

1. A computer program product embodied on a computer readable storage medium for processing network accounting information comprising:

computer code for receiving from a first source a first network accounting record;

computer code for correlating the first network accounting record with accounting information available from a second source; and

computer code for using the accounting information with which the first network accounting record is correlated to enhance the first network accounting record.

Of note, the court interpreted “enhance” in this claim to mean “**to apply a number of field enhancements in a distributed fashion**” (see reproductions from *Amdocs* below).

In *Amdocs I*, we construed “enhance” as being dependent upon the invention’s distributed architecture. 761 F.3d at 1338–40 (quoting ‘065 patent at 7:51–57, 10:45–50, 7:7–8). We construed “enhance” as meaning “to apply a number of field enhancements in a distributed fashion.” *Id.* at

...
In other words, this claim entails an unconventional technological solution (enhancing data in a distributed fashion) to a technological problem (massive record flows which previously required massive databases). The solution requires arguably generic components, including network devices and “gatherers” which “gather” information. However, the claim’s enhancing limitation necessarily requires that these generic components operate in an unconventional manner to achieve an improvement in computer functionality.

Thus, given that the enhancement that arises from applying field enhancements “in a distributed fashion” is that the distributed computing architecture is **bringing different compute resources to bear on the problem of record correlation**, *Amdocs* establishes that a claim which specifies how different compute resources are used to improve how records are processed qualifies as a non-abstract and patent-eligible technological solution. Given that the claims recite how specific tasks involved in record accessing and stream enrichment are distributed across different engines on the coprocessor to improve performance, where these engines operate in parallel, the claims are thus patent-eligible for the same reason that the claims were found to be patent-eligible in *Amdocs*.

Accordingly, because claim 1 practically applies specific technology to define a specific technical solution to the problems of latency and throughput in enriching streaming limit order event data, Applicant respectfully submits that claim 1 “is **necessarily rooted in computer technology in order to overcome a problem specifically arising in the realm of computer networks**” (quoting *DDR Holdings*), which is a category of innovation recognized by the Federal Circuit in *DDR Holdings* as

being eligible for patent protection. Applicant respectfully submits that claims 42 and 44 are patent-eligible for these reasons as well.

Applicant further notes that additional reasons exist for concluding that claims 2, 43, and 45 are non-abstract and patent-eligible because these claims further recite non-generic computer technology for the coprocessor in the form of a reconfigurable logic device, graphics processing unit (GPU), or chip multi-processor (CMP).

Further still, Applicant notes that additional reasons exist for concluding that claims 47, 50, and 53 are non-abstract and patent-eligible because these claims further recite specific hashing features where parallel order hash and price hash engines perform hashing operations on portions of the streaming limit order event data to identify memory addresses for relevant records. Moreover, claims 48, 51, and 54 are also non-abstract and patent-eligible because they further recite various caching features to improve latency and throughput performance.

Accordingly, Applicant respectfully requests withdrawal of the 35 USC 101 rejection of the pending claims.

35 USC 103:

The Office Action rejected claims 1, 2, 41-43 for alleged obviousness based on Hamati (USPN 8,175,946) in combination with Kelleher (USPN 7,598,958). Applicant respectfully submits that this obviousness rejection is improper and must be withdrawn. Independent claim 1 recites:

1. A method for applying specific computer technology to reduce latency and increase throughput with respect to streaming data enrichment, the method comprising:
streaming data representative of a plurality of limit order events pertaining to a plurality of financial instruments into a coprocessor, **the coprocessor including an order engine and a price engine;**
the **order engine accessing a plurality of limit order records based on the streaming limit order event data;**

the order engine generating updated limit order data based on the accessed limit order records and the streaming limit order event data;
the **price engine accessing a plurality of price point records based on the streaming limit order event data;**
the price engine generating updated price point data based on the accessed price point records and the streaming limit order event data; and
the coprocessor generating a stream of enriched limit order events, wherein the enriched limit order events are enriched with the updated limit order and price point data; and
wherein the order engine and the price engine perform their steps in parallel with each other as the limit order event data streams through the coprocessor. (Emphases Added).

The cited Hamati reference fails to describe the use of separate engines for accessing limit order records and price point records to generate updated limit order data and price point data respectively, as recited by claim 1. As such, Hamati also fails to disclose an arrangement "wherein the order engine and the price engine perform their steps in parallel with each other as the limit order event data streams through the coprocessor" as recited by claim 1. Moreover, the Kelleher reference fails to bridge these gaps between claim 1 and Hamati. Kelleher merely describes a multi-chip GPU design, with no teachings regarding how a skilled person could apply such a design to the problem of stream enrichment. As such, even if one assumed for the sake of argument that a skilled person would have had a reason to combine Hamati with Kelleher, Applicant notes that such a combination would still fail to yield the elements of claim 1 because Hamati and Kelleher are silent about distributing tasks between an order engine and price engine in parallel as recited by claim 1 to improve how streaming limit order events are enriched with information derived from limit order records and price point records.

Given these shortcomings in the Hamati and Kelleher references, Applicant respectfully submits that claim 1 is non-obvious over the Hamati/Kelleher combination. Applicant further submits that claim 42 is non-obvious over the Hamati/Kelleher combination for similar reasons.

Double Patenting:

The Office Action rejected claims 44-46 for alleged obviousness-type double patenting (OTDP) based on various claims of parent U.S. patent 8,768,805. Applicant submits herewith a Terminal Disclaimer relative to the '805 patent, which obviates the OTDP rejection. As such, Applicant respectfully requests withdrawal of the OTDP rejection.

Conclusion:

For the foregoing reasons, Applicant respectfully submits that the pending claims are in condition for allowance.

If the Examiner believes, for any reason, that personal communication will expedite prosecution of this application, the Examiner is invited to telephone the undersigned at the number provided below.

Furthermore, Applicant believes that this amendment and remarks are sufficient for overcoming the rejection raised by this Office Action. However, should Applicant later need to further respond to this or new claim rejections, Applicant reserves the right to fully respond to this and any other new rejections, including but not limited to amending the claim and/or adding new claims, submitting evidence in favor of the patentability of the claim(s), disputing the alleged prior art status of the cited references if warranted, and raising new arguments in favor of patentability. Moreover, in submitting this response, Applicant does not acquiesce to any characterizations of the claim or art (including any characterizations about what is allegedly known in the art) made in the outstanding Office Action.

Application No. 14/315,571
Attorney Docket No. 57451-133596

Favorable action is respectfully requested.

Respectfully submitted,

/Benjamin L. Volk, Jr./

Benjamin L. Volk, Jr.

Reg. No. 48,017

Thompson Coburn LLP

One US Bank Plaza

St. Louis, Missouri 63101-9928

(314) 552-6352 (ph)

(314-)552-7000 (fax)

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14315571
	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3695
	Examiner Name	Robinson, Kito R.
	Attorney Docket Number	57451-133596

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14315571
	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3695
	Examiner Name	Robinson, Kito R.
	Attorney Docket Number	57451-133596

1	Office Action for US Application 13/132408 dated June 26, 2017
2	Response to Office Action for US Application 13/132408 dated June 26, 2017

If you wish to add additional non-patent literature document citation information please click the Add button

EXAMINER SIGNATURE

Examiner Signature		Date Considered	

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14315571
	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3695
	Examiner Name	Robinson, Kito R.
	Attorney Docket Number	57451-133596

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

☐ That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.

☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Benjamin L. Volk, Jr./	Date (YYYY-MM-DD)	2018-01-03
Name/Print	Benjamin L. Volk, Jr.	Registration Number	48,017

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

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5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Electronic Patent Application Fee Transmittal				
Application Number:		14315571		
Filing Date:		26-Jun-2014		
Title of Invention:		Method and Apparatus for High-Speed Processing of Financial Market Depth Data		
First Named Inventor/Applicant Name:		David E. Taylor		
Filer:		Benjamin Lowell Volk/Laurie Poss		
Attorney Docket Number:		57451-133596		
Filed as Small Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
CLAIMS IN EXCESS OF 20	2202	7	40	280
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Extension - 3 months with \$0 paid	2253	1	700	700
Miscellaneous:				
SUBMISSION- INFORMATION DISCLOSURE STMT	2806	1	90	90
Total in USD (\$)				1070

Electronic Acknowledgement Receipt	
EFS ID:	31395591
Application Number:	14315571
International Application Number:	
Confirmation Number:	1085
Title of Invention:	Method and Apparatus for High-Speed Processing of Financial Market Depth Data
First Named Inventor/Applicant Name:	David E. Taylor
Customer Number:	21888
Filer:	Benjamin Lowell Volk/Laurie Poss
Filer Authorized By:	Benjamin Lowell Volk
Attorney Docket Number:	57451-133596
Receipt Date:	03-JAN-2018
Filing Date:	26-JUN-2014
Time Stamp:	15:51:55
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$1070
RAM confirmation Number	010418INTEFSW00002292200823
Deposit Account	200823
Authorized User	Laurie Poss
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.17 (Patent application and reexamination processing fees) 37 CFR 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		Amendment_A.pdf	506258	yes	29
			1fd6c70681feb001b3691caf7e19377cc9ce4acb		
	Multipart Description/PDF files in .zip description				
	Document Description		Start	End	
	Amendment/Req. Reconsideration-After Non-Final Reject		1	1	
	Specification		2	3	
	Claims		4	21	
	Applicant Arguments/Remarks Made in an Amendment		22	29	
Warnings:					
Information:					
2	Information Disclosure Statement (IDS) Form (SB08)	IDS-133596.pdf	1034891	no	4
			a9ad1578ca21585e2d47f65b7706ca2e8b5c5c4b		
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3	Non Patent Literature	OAUS13132408.pdf	735254	no	20
			5007c295cfc6256e10e03fc02e706c09b2734f91		
Warnings:					
Information:					
4	Non Patent Literature	ResponseUS13132408.pdf	732097	no	28
			0a49cc42ff3ebabe3ed8a166581a471f30387dbc		

Warnings:					
Information:					
5	Fee Worksheet (SB06)	fee-info.pdf	34317	no	2
			98743f9b879a4b2162bf7623e9eeac8aff7b1b6c		
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Total Files Size (in bytes):			3042817		
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PATENT APPLICATION FEE DETERMINATION RECORD				Application or Docket Number		Filing Date		☐ To be Mailed	
Substitute for Form PTO-875				14/315,571		06/26/2014			
ENTITY: ☐ LARGE ☒ SMALL ☐ MICRO									
APPLICATION AS FILED – PART I									
(Column 1)		(Column 2)							
FOR	NUMBER FILED	NUMBER EXTRA		RATE (\$)		FEE (\$)			
☐ BASIC FEE (37 CFR 1.16(a), (b), or (c))	N/A	N/A		N/A					
☐ SEARCH FEE (37 CFR 1.16(k), (i), or (m))	N/A	N/A		N/A					
☐ EXAMINATION FEE (37 CFR 1.16(o), (p), or (q))	N/A	N/A		N/A					
TOTAL CLAIMS (37 CFR 1.16(j))	minus 20 =	*		X \$ =					
INDEPENDENT CLAIMS (37 CFR 1.16(h))	minus 3 =	*		X \$ =					
☐ APPLICATION SIZE FEE (37 CFR 1.16(s))	If the specification and drawings exceed 100 sheets of paper, the application size fee due is \$310 (\$155 for small entity) for each additional 50 sheets or fraction thereof. See 35 U.S.C. 41(a)(1)(G) and 37 CFR 1.16(s).								
☐ MULTIPLE DEPENDENT CLAIM PRESENT (37 CFR 1.16(j))									
* If the difference in column 1 is less than zero, enter "0" in column 2.				TOTAL					
APPLICATION AS AMENDED – PART II									
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT	01/03/2018	CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	* 52	Minus	** 52	= 0	X \$40 =		0	
	Independent (37 CFR 1.16(h))	* 3	Minus	***3	= 0	X \$210 =		0	
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE		0	
(Column 1)		(Column 2)		(Column 3)					
AMENDMENT		CLAIMS REMAINING AFTER AMENDMENT		HIGHEST NUMBER PREVIOUSLY PAID FOR	PRESENT EXTRA	RATE (\$)		ADDITIONAL FEE (\$)	
	Total (37 CFR 1.16(i))	*	Minus	**	=	X \$ =			
	Independent (37 CFR 1.16(h))	*	Minus	***	=	X \$ =			
	☐ Application Size Fee (37 CFR 1.16(s))								
	☐ FIRST PRESENTATION OF MULTIPLE DEPENDENT CLAIM (37 CFR 1.16(j))								
						TOTAL ADD'L FEE			
* If the entry in column 1 is less than the entry in column 2, write "0" in column 3. ** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 20, enter "20". *** If the "Highest Number Previously Paid For" IN THIS SPACE is less than 3, enter "3". The "Highest Number Previously Paid For" (Total or Independent) is the highest number found in the appropriate box in column 1.									

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NOTICE OF ALLOWANCE AND FEE(S) DUE

21888 7590 05/01/2018
THOMPSON COBURN LLP
ONE US BANK PLAZA
SUITE 3500
ST LOUIS, MISSOURI 63101
UNITED STATES OF AMERICA

EXAMINER

ROBINSON, KITO R

ART UNIT

PAPER NUMBER

3695

DATE MAILED: 05/01/2018

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/315,571	06/26/2014	David E. Taylor	57451-133596	1085

TITLE OF INVENTION: Method and Apparatus for High-Speed Processing of Financial Market Depth Data

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$500	\$0.00	\$0.00	\$500	08/01/2018

THE APPLICATION IDENTIFIED ABOVE HAS BEEN EXAMINED AND IS ALLOWED FOR ISSUANCE AS A PATENT. PROSECUTION ON THE MERITS IS CLOSED. THIS NOTICE OF ALLOWANCE IS NOT A GRANT OF PATENT RIGHTS. THIS APPLICATION IS SUBJECT TO WITHDRAWAL FROM ISSUE AT THE INITIATIVE OF THE OFFICE OR UPON PETITION BY THE APPLICANT. SEE 37 CFR 1.313 AND MPEP 1308.

THE ISSUE FEE AND PUBLICATION FEE (IF REQUIRED) MUST BE PAID WITHIN THREE MONTHS FROM THE MAILING DATE OF THIS NOTICE OR THIS APPLICATION SHALL BE REGARDED AS ABANDONED. THIS STATUTORY PERIOD CANNOT BE EXTENDED. SEE 35 U.S.C. 151. THE ISSUE FEE DUE INDICATED ABOVE DOES NOT REFLECT A CREDIT FOR ANY PREVIOUSLY PAID ISSUE FEE IN THIS APPLICATION. IF AN ISSUE FEE HAS PREVIOUSLY BEEN PAID IN THIS APPLICATION (AS SHOWN ABOVE), THE RETURN OF PART B OF THIS FORM WILL BE CONSIDERED A REQUEST TO REAPPLY THE PREVIOUSLY PAID ISSUE FEE TOWARD THE ISSUE FEE NOW DUE.

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If the ENTITY STATUS is the same as shown above, pay the TOTAL FEE(S) DUE shown above.

If the ENTITY STATUS is changed from that shown above, on PART B - FEE(S) TRANSMITTAL, complete section number 5 titled "Change in Entity Status (from status indicated above)".

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III. All communications regarding this application must give the application number. Please direct all communications prior to issuance to Mail Stop ISSUE FEE unless advised to the contrary.

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PART B - FEE(S) TRANSMITTAL

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Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address)

21888 7590 05/01/2018
THOMPSON COBURN LLP
ONE US BANK PLAZA
SUITE 3500
ST LOUIS, MISSOURI 63101
UNITED STATES OF AMERICA

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/315,571	06/26/2014	David E. Taylor	57451-133596	1085

TITLE OF INVENTION: Method and Apparatus for High-Speed Processing of Financial Market Depth Data

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$500	\$0.00	\$0.00	\$500	08/01/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
ROBINSON, KITO R	3695	705-035000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363). ☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached. ☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. Use of a Customer Number is required.	2. For printing on the patent front page, list (1) The names of up to 3 registered patent attorneys or agents OR, alternatively, (2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed. 1 _____ 2 _____ 3 _____

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☐ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☐ Issue Fee
- ☐ Publication Fee (No small entity discount permitted)
- ☐ Advance Order - # of Copies _____

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
- ☐ Payment by credit card. Form PTO-2038 is attached.
- ☐ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number _____ (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
- ☐ Applicant asserting small entity status. See 37 CFR 1.27
- ☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.

NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.

NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature _____ Date _____

Typed or printed name _____ Registration No. _____



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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/315,571	06/26/2014	David E. Taylor	57451-133596	1085
21888 7590 05/01/2018 THOMPSON COBURN LLP ONE US BANK PLAZA SUITE 3500 ST LOUIS, MISSOURI 63101 UNITED STATES OF AMERICA			EXAMINER ROBINSON, KITO R	
			ART UNIT	PAPER NUMBER
			3695	

DATE MAILED: 05/01/2018

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (Applications filed on or after May 29, 2000)

The Office has discontinued providing a Patent Term Adjustment (PTA) calculation with the Notice of Allowance.

Section 1(h)(2) of the AIA Technical Corrections Act amended 35 U.S.C. 154(b)(3)(B)(i) to eliminate the requirement that the Office provide a patent term adjustment determination with the notice of allowance. See Revisions to Patent Term Adjustment, 78 Fed. Reg. 19416, 19417 (Apr. 1, 2013). Therefore, the Office is no longer providing an initial patent term adjustment determination with the notice of allowance. The Office will continue to provide a patent term adjustment determination with the Issue Notification Letter that is mailed to applicant approximately three weeks prior to the issue date of the patent, and will include the patent term adjustment on the patent. Any request for reconsideration of the patent term adjustment determination (or reinstatement of patent term adjustment) should follow the process outlined in 37 CFR 1.705.

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Customer Service Center of the Office of Patent Publication at 1-(888)-786-0101 or (571)-272-4200.

OMB Clearance and PRA Burden Statement for PTOL-85 Part B

The Paperwork Reduction Act (PRA) of 1995 requires Federal agencies to obtain Office of Management and Budget approval before requesting most types of information from the public. When OMB approves an agency request to collect information from the public, OMB (i) provides a valid OMB Control Number and expiration date for the agency to display on the instrument that will be used to collect the information and (ii) requires the agency to inform the public about the OMB Control Number's legal significance in accordance with 5 CFR 1320.5(b).

The information collected by PTOL-85 Part B is required by 37 CFR 1.311. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, Virginia 22313-1450. **DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, Virginia 22313-1450.** Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

Privacy Act Statement

The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether disclosure of these records is required by the Freedom of Information Act.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspection or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

Notice of Allowability	Application No. 14/315,571	Applicant(s) Taylor et al.	
	Examiner KITO R ROBINSON	Art Unit 3695	AIA Status No

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to amendments filed on 03 January 2018.
☐ A declaration(s)/affidavit(s) under **37 CFR 1.130(b)** was/were filed on _____.

2. ☐ An election was made by the applicant in response to a restriction requirement set forth during the interview on _____; the restriction requirement and election have been incorporated into this action.

3. ☒ The allowed claim(s) is/are See Continuation Sheet. As a result of the allowed claim(s), you may be eligible to benefit from the **Patent Prosecution Highway** program at a participating intellectual property office for the corresponding application. For more information, please see http://www.uspto.gov/patents/init_events/pph/index.jsp or send an inquiry to **PPHfeedback@uspto.gov**.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
Certified copies:
a) ☐ All b) ☐ Some *c) ☐ None of the:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).
* Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file areply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892) 2. ☒ Information Disclosure Statements (PTO/SB/08), Paper No./Mail Date <u>01/03/2018</u> . 3. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material _____. 4. ☐ Interview Summary (PTO-413), Paper No./Mail Date. _____.	5. ☐ Examiner's Amendment/Comment 6. ☒ Examiner's Statement of Reasons for Allowance 7. ☐ Other _____.

/KITO R ROBINSON/ Primary Examiner, Art Unit 3695	

Continuation of 3. The allowed claim(s) is/are: 1-23,25-37 and 39-55

DETAILED ACTION

Status of Claims

1. This action is in reply to the amendments filed on 03 January 2018.
2. Claims 24 and 38 have been cancelled.
3. Claims 1-4, 7-, 10, 11, 14, 17, 19, 23, 33, 34-36, and 40-45 have been amended.
4. Claims 47-55 are new.
5. Claims 1-23, 25-37 and 39-55 are currently pending and have been examined.
6. The present application is being examined under the pre-AIA first to invent provisions.
7. The Examiner respectfully rescinds the objection to the specification in view of the amendments.
8. The Examiner respectfully rescinds the pre-AIA 35 U.S.C. 103(a) rejection in view of the claimed amendments and arguments on page 28 & 27.
9. The Examiner respectfully rescinds the 35 U.S.C. 101 rejection in view of the claimed amendments. The claimed method recites specific steps that accomplish a result that realizes an improvement in computer functionality. In particular, parallel engines update and maintain the order and price aggregation data structures in parallel and the data structures are maintained in the same

physical memory. Therefore, the one or more order engines and one or more price engines interleave their accesses to memory, masking the memory access latency of the memory technology and maximizing throughput of the system. This is an improvement over traditional streaming data systems.

10. The information disclosure statement (IDS) submitted on 01/03/2018 was considered by the examiner.

Allowable Subject Matter

11. The following is an examiner's statement of reasons for allowance: The instant application is directed towards high speed processing of financial market depth data. More specifically, the Applicants claim a system and method for applying specific computer technology to reduce latency and increase throughput with respect to streaming data enrichment, the method comprising: streaming data representative of a plurality of limit order events pertaining to a plurality of financial instruments into a coprocessor, the coprocessor including an order engine and a price engine; the order engine accessing a plurality of limit order records based on the streaming limit order event data; the order engine generating updated limit order data based on the accessed limit order records and the streaming limit order event data; the price engine accessing a plurality of price point records based on the streaming limit order event data; the price engine generating updated price point data based on the accessed price point records and the streaming limit order event data; and the coprocessor generating a stream of enriched limit order

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events, wherein the enriched limit order events are enriched with the updated limit order and price point data; and wherein the order engine and the price engine perform their steps in parallel with each other as the limit order event data streams through the coprocessor.

Furthermore, Humati et al. [US 8,175,946] discloses “A system, method and computer program product are described for providing the execution probability of a limit order within a given time period based on historical and current information and for adaptively and dynamically adjusting to intra-day trade data. For a given financial interest, the frequency of trade execution, the time evolution of the price, the time evolution of the trade volume, and the current state of the market, among other parameters, are captured and/or calculated. A probability function is generated based on the parameters corresponding to various time spans, and the execution probability of a limit order within a given time period is provided. Embodiments of the invention can be employed to estimate the probability of a limit order being executed within a given time period in the future, e.g., the next two minutes, based on the parameter data of a given time period in the past, e.g., the previous five minutes.” Kelleher [US 7,598,958 B1] discloses “A multi-chip graphics system includes a master chip and a slave chip coupled by an interlink. The slave chip performs a graphics processing operation in parallel with the master chip, improving the performance of the master chip. In one embodiment, an individual graphics processing unit (GPU) chip includes a normal operational

Art Unit: 3695

mode, a master mode, and a slave mode to permit an individual GPU chip to be used as individual processor or to be packaged as part of a master/slave pair.”

12. However, in the instant application none of the prior arts of record either individually or in combination teach or suggest a coprocessor including an order engine and a price engine; the order engine accessing a plurality of limit order records based on the streaming limit order event data; the order engine generating updated limit order data based on the accessed limit order records and the streaming limit order event data; the price engine accessing a plurality of price point records based on the streaming limit order event data; the price engine generating updated price point data based on the accessed price point records and the streaming limit order event data; and the coprocessor generating a stream of enriched limit order events, wherein the enriched limit order events are enriched with the updated limit order and price point data; and wherein the order engine and the price engine perform their steps in parallel with each other as the limit order event data streams through the coprocessor.

For these reasons claims 1, 42 & 44 are deemed to be allowable over the prior art of record, and claims 2-23, 25-37, 39-41, 43 and 45-55 are allowed by dependency on an allowed claim.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure is listed on the enclosed PTO-892.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to KITO R ROBINSON whose telephone number is (571)270-3921. The examiner can normally be reached on M-F 8:30am-5:30pm.

Examiner interviews are available via telephone, in-person, and video conferencing using a USPTO supplied web-based collaboration tool. To schedule an interview, applicant is encouraged to use the USPTO Automated Interview Request (AIR) at <http://www.uspto.gov/interviewpractice>.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ryan Donlon can be reached on (571) 270-36023602. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/KITO R ROBINSON/
Primary Examiner, Art Unit 3695

Notice of References Cited	Application/Control No. 14/315,571		Applicant(s)/Patent Under Reexamination Taylor et al.	
	Examiner KITO R ROBINSON		Art Unit 3695	Page 1 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-4811210-A	03-1989	McAulay; Alastair D.	G06E1/02	385/17
*	B	US-5375055-A	12-1994	Togher; Michael	G06Q40/025	340/4.5
*	C	US-6278982-B1	08-2001	Korhammer; Richard A.	G06Q40/04	705/36R
*	D	US-20010041012-A1	11-2001	Hsieh, Jeff	G06F7/76	382/234
*	E	US-20020038279-A1	03-2002	Samuelson, Ralph	G06Q10/06	705/37
*	F	US-6493682-B1	12-2002	Horrigan; Holly T.	G06Q40/00	705/35
*	G	US-20030009411-A1	01-2003	Ram, Pranil	G06F17/246	705/37
*	H	US-6801938-B1	10-2004	Bookman; Lawrence A.	G06F17/2258	707/999.201
*	I	US-20050216384-A1	09-2005	Partlow, Daniel	G06Q40/00	705/35
*	J	US-20060292292-A1	12-2006	Brightman; Thomas B.	H04L49/10	427/66
*	K	US-7565315-B2	07-2009	West; Robert A.	G06Q40/00	705/37
*	L	US-7598958-B1	10-2009	Kelleher; Brian M.	G06F9/3877	345/502
*	M	US-7840482-B2	11-2010	Singla; Naveen	G06Q40/06	705/36R

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
	O					
	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	Gaughan, P. T. (1995). Data streaming: Very low overhead communication for fine-grained multicomputing doi:http://dx.doi.org/10.1109/SPDP.1995.530727 (Year: 1995)
	V	Babz. (2005). Empower your virtual instruments. Electronic Musician, 10(21), NA. Retrieved from https://dialog.proquest.com/professional/docview/668423692?accountid=142257 (Year: 2005)
	W	Srini, V. P. (1995). DFS-SuperMPx: Low-cost parallel processing system for machine vision and image processing Retrieved from https://dialog.proquest.com/professional/docview/828015663?accountid=142257 (Year: 1995)
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office
PTO-892 (Rev. 01-2001)

Notice of References Cited

Part of Paper No. 20180413

Notice of References Cited	Application/Control No. 14/315,571		Applicant(s)/Patent Under Reexamination Taylor et al.	
	Examiner KITO R ROBINSON		Art Unit 3695	Page 2 of 2

U.S. PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Name	CPC Classification	US Classification
*	A	US-8843408-B2	09-2014	Singla; Naveen	G06Q40/06	705/36R
*	B	US-7921046-B2	04-2011	Parsons; Scott	G06Q40/00	705/35
*	C	US-8175946-B2	05-2012	Hamati; Gheis Henri	G06Q30/0202	705/36R
*	D	US-8213518-B1	07-2012	Wang; Jason N.	H04N19/44	348/721
*	E	US-20120216019-A1	08-2012	Bower; Jacob Alexis	G06F17/5054	712/201
*	F	US-20120246052-A1	09-2012	Taylor; David	G06Q40/04	705/37
*	G	US-8332829-B2	12-2012	Mattson; Peter	G06F8/453	712/225
*	H	US-20150317277-A1	11-2015	Wang; Hao	G06F13/161	710/307
*	I	US-20160154867-A1	06-2016	Chen; Qiming	G06F9/4843	707/756
*	J	US-9813976-B2	11-2017	Velusamy; Senthil Kumar Mullupadi	H04W48/16	1/1
	K					
	L					
	M					

FOREIGN PATENT DOCUMENTS

*		Document Number Country Code-Number-Kind Code	Date MM-YYYY	Country	Name	CPC Classification
	N					
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	P					
	Q					
	R					
	S					
	T					

NON-PATENT DOCUMENTS

*		Include as applicable: Author, Title Date, Publisher, Edition or Volume, Pertinent Pages)
	U	
	V	
	W	
	X	

*A copy of this reference is not being furnished with this Office action. (See MPEP § 707.05(a).)
Dates in MM-YYYY format are publication dates. Classifications may be US or foreign.

U.S. Patent and Trademark Office
PTO-892 (Rev. 01-2001)

Notice of References Cited

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<i>Index of Claims</i> 	Application/Control No. 14/315,571	Applicant(s)/Patent Under Reexamination Taylor et al.
	Examiner KITO R ROBINSON	Art Unit 3695

✓	Rejected	-	Cancelled	N	Non-Elected	A	Appeal
=	Allowed	÷	Restricted	I	Interference	O	Objected

CLAIMS										
☐ Claims renumbered in the same order as presented by applicant ☐ CPA ☒ T.D. ☐ R.1.47										
CLAIM		DATE								
Final	Original	06/30/2017	04/13/2018							
1	1	✓	=							
2	2	✓	=							
3	3	✓	=							
4	4	✓	=							
5	5	✓	=							
6	6	✓	=							
7	7	✓	=							
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31	32	✓	=							
32	33	✓	=							
33	34	✓	=							
34	35	✓	=							
35	36	✓	=							
36	37	✓	=							
	38	✓	-							
37	39	✓	=							
38	40	✓	=							
39	41	✓	=							
43	42	✓	=							

<i>Index of Claims</i> 	Application/Control No. 14/315,571	Applicant(s)/Patent Under Reexamination Taylor et al.
	Examiner KITO R ROBINSON	Art Unit 3695

CLAIM		DATE								
Final	Original	06/30/2017	04/13/2018							
44	43	✓	=							
48	44	✓	=							
49	45	✓	=							
50	46	✓	=							
40	47		=							
41	48		=							
42	49		=							
45	50		=							
46	51		=							
47	52		=							
51	53		=							
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53	55		=							

<i>Search Notes</i> 	Application/Control No. 14/315,571	Applicant(s)/Patent Under Reexamination Taylor et al.
	Examiner KITO R ROBINSON	Art Unit 3695

CPC - Searched*		
Symbol	Date	Examiner
G06Q 40/04	04/14/2018	KR
G06Q 40/00	04/14/2018	KR

CPC Combination Sets - Searched*		
Symbol	Date	Examiner

US Classification - Searched*			
Class	Subclass	Date	Examiner
705	35	04/14/2018	KR

* See search history printout included with this form or the SEARCH NOTES box below to determine the scope of the search.

Search Notes		
Search Notes	Date	Examiner
EAST: INVENTOR SEARCH, BACKWARD/FORWARD SEARCH	04/14/2018	KR

Interference Search			
US Class/CPC Symbol	US Subclass/CPC Group	Date	Examiner
705	35	04/14/2018	KR

Issue Classification 	Application/Control No. 14/315,571	Applicant(s)/Patent Under Reexamination Taylor et al.
	Examiner KITO R ROBINSON	Art Unit 3695

CPC						
Symbol					Type	Version
G06Q		40		04	F	2013-01-01
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CPC Combination Sets						
Symbol				Type	Set	Ranking

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	53	
/KITO R ROBINSON/ Primary Examiner, Art Unit 3695	13 April 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	23

Issue Classification 	Application/Control No. 14/315,571	Applicant(s)/Patent Under Reexamination Taylor et al.
	Examiner KITO R ROBINSON	Art Unit 3695

INTERNATIONAL CLASSIFICATION			
CLAIMED			
G06Q		40	00
NON-CLAIMED			

US ORIGINAL CLASSIFICATION	
CLASS	SUBCLASS
705	35

CROSS REFERENCES(S)						
CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)					

NONE		Total Claims Allowed:	
(Assistant Examiner)	(Date)	53	
/KITO R ROBINSON/ Primary Examiner, Art Unit 3695	13 April 2018	O.G. Print Claim(s)	O.G. Print Figure
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Issue Classification 	Application/Control No. 14/315,571	Applicant(s)/Patent Under Reexamination Taylor et al.
	Examiner KITO R ROBINSON	Art Unit 3695

☐ Claims renumbered in the same order as presented by applicant
 ☐ CPA
 ☒ T.D.
 ☐ R.1.47

CLAIMS															
Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original	Final	Original
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6	6	15	15		24	32	33	43	42	46	51				
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NONE		Total Claims Allowed:	
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/KITO R ROBINSON/ Primary Examiner, Art Unit 3695	13 April 2018	O.G. Print Claim(s)	O.G. Print Figure
(Primary Examiner)	(Date)	1	23

U.S. Patent and Trademark Office

Part of Paper No.: 20180413

EAST Search History

EAST Search History (Prior Art)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	18	((stream\$4 near2 data) and (parallel near4 processor) and latency).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 16:30
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L16	3	"l15" and ((stream\$4 near2 data) and (parallel near4 processor) and (redu\$4 near4 latency))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 16:42
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L18	1	705/35 and ((stream\$4 near2 data) and (parallel near4 processor) and (redu\$4 near4 latency))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 16:43
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L36	15	((stream\$4 near2 data) and (parallel near4 processor) and (redu\$4 near4 latency) and rice)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 16:48
L37	287	((stream\$4 near2 data) and (parallel near4 processor) and (redu\$4 near4 latency) and price)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 16:48
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S2	1	("8768805").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2017/06/27 15:22
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S4	7	S1 and ((limit near2 order))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/27 15:25
S5	1759	(stream\$4 same (limit near2 order))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/27 16:42
S6	7	705/36 and (stream\$4 same (limit near2 order))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/27 16:42
S7	3	705/36 and ((stream\$4 near2 (data or information or price)) same (limit near2 order))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/27 17:07
S8	80	705/36 and ((stream\$4 near2 (data or information or price)) and (limit near2 order))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/27 17:08
S9	30	705/36 and ((stream\$4 near2 (data or information or price)) and (limit near2 order) and (order near2 book))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/27 17:08
S10	0	705/36 and ((stream\$4 near2 (data or information or price)) and (limit near2	US-PGPUB; USPAT;	OR	ON	2017/06/27 17:08

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S23	1	705/35 and (chip-multi-processor and (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:22
S24	0	705/36 and (chip-multi-processor and (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:22
S25	2	705/\$\$ and (chip-multi-processor and (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:23
S26	11	705/\$\$ and ((chip near2 multi near2 processor) and (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:23
S27	1	streaming same ((chip near2 multi near2 processor) and (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:24
S28	542	((chip near2 multi near2 processor) and (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:25
S29	363	((chip near2 multi near2 processor) same (graphics near2 processing near2 unit))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:25
S30	3	(regional and composite) near2 price near2 volume	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:38
S31	3	(regional and composite) near6 price near2 volume	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:40
S32	6	(regional and composite) same price near2 volume	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:40
S33	5	(S12 or S15 or S17 or S19 or S21) and ((regional and composite) same price near2 volume)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:41
S34	42	(S12 or S15 or S17 or S19 or S21) and (price near2 volume)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:41
S35	30	(S12 or S15 or S17 or S19 or S21) and (regional and composite)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/28 15:42
S36	72	(ephemeral near2 order)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/29 17:01
S37	5	705/35 and (ephemeral near2 order)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/29 17:01

S38	0	705/36 and (ephemeral near2 order)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/29 17:01
S39	12	705/\$\$ and (ephemeral near2 order)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/29 17:01
S40	9	705/36 and (ephemeral)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:13
S41	53	705/35 and (ephemeral)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:15
S42	7	(limit near2 order) with mapping same identifier	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:20
S43	17	(limit near2 order) same mapping same identifier	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:20
S44	372	(limit near2 order) with identifier	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:21
S45	192	(limit near2 order) near4 identifier	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:21
S46	388	(limit near2 order) near4 event	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:22
S47	15	705/35 and ((limit near2 order) near4 event)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:22
S48	8	705/36 and ((limit near2 order) near4 event)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:23
S49	5	705/36 and ((limit near2 order) near4 identifier)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:24
S50	15	705/35 and ((limit near2 order) near4 identifier)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 09:25
S51	1	705/35 and ((ephemeral) near4 identifier)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:41
S52	13	705/\$\$ and ((ephemeral) near4 identifier)	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:41
S53	10	705/\$\$ and (identif\$4 near4 ephemeral near4 (order or transaction))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:43
S54	10	705/\$\$ and (identif\$4 near6 ephemeral near6 (order or transaction))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:43
S55	11	705/\$\$ and (identif\$4 near8 ephemeral near8 (order or transaction))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:44
S56	10	705/\$\$ and (identif\$4 with ephemeral near8 (order or transaction))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:44

S57	14	705/\$\$ and (identif\$4 with ephemeral with (order or transaction))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:44
S58	14	705/\$\$ and (identif\$4 with ephemer\$3 with (order or transaction))	US-PGPUB; USPAT; USOCR	OR	ON	2017/06/30 11:47
S59	14	705/\$\$ and (identif\$4 with ephemer\$3 with (order or transaction))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 11:47
S60	0	705/\$\$ and (identif\$4 with ephemer\$3 with (commodit\$3))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 11:48
S61	93	705/\$\$ and (identif\$4 near4 ephemer\$3)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 11:48
S62	159	Parsons-Scott\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:34
S63	0	S62 with (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:34
S64	11	Whatley-Jeremy-Walter\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:35
S65	0	S64 with (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:35
S66	427	Bradley-Richard\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2017/06/30 15:35

			IBM_TDB			
S67	0	S66 with (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:36
S68	25	Gyang-Kwame\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:36
S69	0	S68 with (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:36
S70	11	DeWulf-Michael\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:36
S71	0	S70 with (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:36
S72	142	Taylor-David-E\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:37
S73	0	S72 with (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:37
S74	8	S62 and (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:37
S75	1200206	S64 ans (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS;	OR	ON	2017/06/30 15:38

			EPO; JPO; DERWENT; IBM_TDB			
S76	6	S64 and (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:38
S77	6	S66 and (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:38
S78	6	S70 and (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:38
S79	12	S72 and (enriched or ephemeral)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2017/06/30 15:39
S80	9	"8768805"	US-PGPUB; USPAT; USOCR	OR	ON	2018/04/13 10:56
S81	10	("20030182224" "20060259381" "20070100722" "20070233593" "20070294162" "20080077521" "6343278" "6493682" "7177833" "7251629").PN. OR ("8175946").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/04/13 18:16
S82	43	("20030164830" "20030164834" "20040012934" "20050041031" "20050088445" "20050190190" "5157765" "5392394" "5757385" "5794016" "5995121" "6088043" "6178180" "6473086" "6627531" "6630936" "6903278" "7158140").PN. OR ("7598958").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/04/13 18:18
S83	43	("20030164830" "20030164834" "20040012934" "20050041031" "20050088445" "20050190190" "5157765" "5392394" "5757385" "5794016" "5995121" "6088043" "6178180" "6473086" "6627531" "6630936" "6903278" "7158140").PN. OR ("7598958").URPN.	US-PGPUB; USPAT; USOCR	OR	ON	2018/04/13 18:18
S84	146	Taylor-David-E\$.inv.	US-PGPUB; USPAT; USOCR;	OR	ON	2018/04/14 15:13

			FPRS; EPO; JPO; DERWENT; IBM_TDB			
S85	166	Parsons-Scott\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:13
S86	0	hatley-Jeremy-Walter\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:13
S87	11	whatley-Jeremy-Walter\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:13
S88	443	Bradley-Richard\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:14
S89	25	Gyang-Kwame\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:14
S90	11	DeWulf-Michael\$.inv.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:14
S91	1775	(stream\$4 near2 data) same (parallel near4 processor)	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:16
S92	0	70/35 and ((stream\$4 near2 data) same (parallel near4 processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:16
S93	0	705./35 and ((stream\$4 near2 data)	US-PGPUB;	OR	ON	2018/04/14;

		same (parallel near4 processor))	USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB			15:17
S94	2	705/35 and ((stream\$4 near2 data) same (parallel near4 processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:17
S95	1775	705/\$\$and ((stream\$4 near2 data) same (parallel near4 processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:17
S96	25	705/\$\$ and ((stream\$4 near2 data) same (parallel near4 processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:18
S97	0	S84 and ((stream\$4 near2 data) same (parallel near4 processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:18
S98	0	S85 and ((stream\$4 near2 data) same (parallel near4 processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:18
S99	0	S87 and ((stream\$4 near2 data) same (parallel near4 processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:18
S100	0	S87 and ((stream\$4 near2 data) and (parallel near4 processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:18
S101	0	S88 and ((stream\$4 near2 data) and (parallel near4 processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT;	OR	ON	2018/04/14 15:18

			IBM_TDB			
S102	0	S89 and ((stream\$4 near2 data) and (parallel near4 processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:19
S103	0	S90 and ((stream\$4 near2 data) and (parallel near4 processor))	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:19
S104	371	((stream\$4 near2 data) and (parallel near4 processor)).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:19
S105	93	((stream\$4 near2 data) and (parallel near4 processor) and access).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:19
S106	0	((stream\$4 near2 data) and (parallel near4 processor) and access and price and limit).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:19
S107	0	((stream\$4 near2 data) and (parallel near4 processor) and price and limit).clm.	US-PGPUB; USPAT; USOCR; FPRS; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2018/04/14 15:20

EAST Search History (Interference)

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L20	1	705/35 and ((stream\$4 near2 data) and (parallel near4 processor) and (redu\$4 near4 latency))	US-PGPUB; USPAT	OR	ON	2018/04/14 16:43
L21	0	((stream\$4 near2 data) and (parallel near4 processor) and price and limit).clm.	US-PGPUB; USPAT	OR	ON	2018/04/14 16:44
L22	93	((stream\$4 near2 data) and (parallel near4 processor) and access).clm.	US-PGPUB; USPAT	OR	ON	2018/04/14 16:44
L23	73	Taylor-David-E\$.inv.	US-PGPUB; USPAT	OR	ON	2018/04/14 16:44

L24	6	whatley-Jeremy-Walter\$.inv.	US-PGPUB; USPAT	OR	ON	2018/04/14 16:44
L25	0	hatley-Jeremy-Walter\$.inv.	US-PGPUB; USPAT	OR	ON	2018/04/14 16:44
L26	94	Bradley-Richard\$.inv.	US-PGPUB; USPAT	OR	ON	2018/04/14 16:44
L27	13	Gyang-Kwame\$.inv.	US-PGPUB; USPAT	OR	ON	2018/04/14 16:44
L28	6	DeWulf-Michael\$.inv.	US-PGPUB; USPAT	OR	ON	2018/04/14 16:45
L29	9	23 and ((stream\$4 near2 data) and (parallel near4 processor) and (redu\$4 near4 latency))	US-PGPUB; USPAT	OR	ON	2018/04/14 16:45
L30	1845	234and ((stream\$4 near2 data) and (parallel near4 processor) and (redu\$4 near4 latency))	US-PGPUB; USPAT	OR	ON	2018/04/14 16:45
L31	0	24 and ((stream\$4 near2 data) and (parallel near4 processor) and (redu\$4 near4 latency))	US-PGPUB; USPAT	OR	ON	2018/04/14 16:45
L32	0	25 and ((stream\$4 near2 data) and (parallel near4 processor) and (redu\$4 near4 latency))	US-PGPUB; USPAT	OR	ON	2018/04/14 16:45
L33	0	26 and ((stream\$4 near2 data) and (parallel near4 processor) and (redu\$4 near4 latency))	US-PGPUB; USPAT	OR	ON	2018/04/14 16:45
L34	0	27 and ((stream\$4 near2 data) and (parallel near4 processor) and (redu\$4 near4 latency))	US-PGPUB; USPAT	OR	ON	2018/04/14 16:45

4/14/2018 4:52:29 PM

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April 16 2018 10:22

Search Strategy

Databases: AdisInsight: Drugs, AdisInsight: Safety Reports, AdisInsight: Trials, Adis Pharmacoeconomics & Outcomes News, Allied & Complementary Medicine™, Analytical Abstracts, Aqualine, Aquatic Science & Fisheries Abstracts (ASFA), BIOSIS Previews®, CAB ABSTRACTS, Chemical Engineering & Biotechnology Abstracts, EconLit, Ei Compendex®, Embase®, Foodline®: MARKET, Foodline®: PRODUCT, Foodline®: SCIENCE, FSTA®, Gale Group Health Periodicals Database, Gale Group PharmaBiomed Business Journals, Gale Group PROMT®, GeoRef, Global Health, Inspec®, KOSMET: Cosmetic Science, MEDLINE®, Meteorological & Geostrophysical Abstracts, NTIS: National Technical Information Service, Oceanic Abstracts, Polymer Library, ProQuest Technology Research Professional, SciSearch®: a Cited Reference Science Database, ToxFile®, TULSA™ (Petroleum Abstracts)

Set#	Searched for	Results
S1	((streaming near data) AND (limit near order) AND latency AND (parallel near procesor)) and (pd(<20081215))	0°
S2	((streaming near data) AND (limit near order) AND (parallel near procesor)) and (pd(<20081215))	0°
S3	((streaming near data) AND (parallel near procesor)) and (pd(<20081215))	0°
S4	(streaming AND (parallel near procesor)) and (pd(<20081215))	0°
S5	((streaming near data) AND latency AND processor) and (pd(<20081215))	196°
S6	((streaming near data) AND (reduc* near latency) AND processor) and (pd(<20081215))	33°
S7	((streaming near data) AND (reduc* near latency) AND processor) and (pd(<20081215))	33°
S8	((streaming near data) AND (reduc* near latency) AND parallel) and (pd(<20081215))	23°
S9	((data near stream*) AND (reduc* near latency) AND parallel) and (pd(<20081215))	81°
S10	((data near stream*) AND (reduc* near latency) AND (parallel near processor)) and (pd(<20081215))	8°

° Duplicates are removed from the search and from the result count.

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Bibliographic Data

Application No: 14315571

Foreign Priority claimed: ☐ Yes ☒ No

35 USC 119 (a-d) conditions met: ☐ Yes ☒ No ☐ Met After Allowance

Verified and Acknowledged:

/KITO R ROBINSON/

Examiner's Signature

Initials

Title:

Method and Apparatus for High-Speed Processing of Financial Market
Depth Data

FILING or 371(c) DATE	CLASS	GROUP ART UNIT	ATTORNEY DOCKET NO.
06/26/2014	705	3695	57451-133596
RULE			

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CONTINUING DATA

This application is a DIV of 13154804 06/07/2011 PAT 87688058

13154804 is a DIV of PCT/US2009/067935 12/14/2009

PCT/US2009/067935 has PRO of 61122673 12/15/2008

FOREIGN APPLICATIONS

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Doc code: IDS

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Doc description: Information Disclosure Statement (IDS) Filed

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INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number	14315571
	Filing Date	2014-06-26
	First Named Inventor	David E. Taylor
	Art Unit	3695
	Examiner Name	Robinson, Kito R.
	Attorney Docket Number	57451-133596

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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	14315571
Filing Date	2014-06-26
First Named Inventor	David E. Taylor
Art Unit	3695
Examiner Name	Robinson, Kito R.
Attorney Docket Number	57451-133596

1	Office Action for US Application 13/132408 dated June 26, 2017
2	Response to Office Action for US Application 13/132408 dated June 26, 2017

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EXAMINER SIGNATURE

Examiner Signature	/KITO R ROBINSON/	Date Considered	04/13/2018

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through a citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ See Kind Codes of USPTO Patent Documents at www.USPTO.GOV or MPEP 901.04. ² Enter office that issued the document, by the two-letter code (WIPO Standard ST.3). ³ For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁴ Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST.16 if possible. ⁵ Applicant is to place a check mark here if English language translation is attached.

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**
(Not for submission under 37 CFR 1.99)

Application Number	14315571
Filing Date	2014-06-26
First Named Inventor	David E. Taylor
Art Unit	3695
Examiner Name	Robinson, Kito R.
Attorney Docket Number	57451-133596

CERTIFICATION STATEMENT

Please see 37 CFR 1.97 and 1.98 to make the appropriate selection(s):

That each item of information contained in the information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(1).

OR

That no item of information contained in the information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application, and, to the knowledge of the person signing the certification after making reasonable inquiry, no item of information contained in the information disclosure statement was known to any individual designated in 37 CFR 1.56(c) more than three months prior to the filing of the information disclosure statement. See 37 CFR 1.97(e)(2).

See attached certification statement.

- ☒ The fee set forth in 37 CFR 1.17 (p) has been submitted herewith.
☒ A certification statement is not submitted herewith.

SIGNATURE

A signature of the applicant or representative is required in accordance with CFR 1.33, 10.18. Please see CFR 1.4(d) for the form of the signature.

Signature	/Benjamin L. Volk, Jr./	Date (YYYY-MM-DD)	2018-01-03
Name/Print	Benjamin L. Volk, Jr.	Registration Number	48,017

This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1 hour to complete, including gathering, preparing and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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The Privacy Act of 1974 (P.L. 93-579) requires that you be given certain information in connection with your submission of the attached form related to a patent application or patent. Accordingly, pursuant to the requirements of the Act, please be advised that: (1) the general authority for the collection of this information is 35 U.S.C. 2(b)(2); (2) furnishing of the information solicited is voluntary; and (3) the principal purpose for which the information is used by the U.S. Patent and Trademark Office is to process and/or examine your submission related to a patent application or patent. If you do not furnish the requested information, the U.S. Patent and Trademark Office may not be able to process and/or examine your submission, which may result in termination of proceedings or abandonment of the application or expiration of the patent.

The information provided by you in this form will be subject to the following routine uses:

1. The information on this form will be treated confidentially to the extent allowed under the Freedom of Information Act (5 U.S.C. 552) and the Privacy Act (5 U.S.C. 552a). Records from this system of records may be disclosed to the Department of Justice to determine whether the Freedom of Information Act requires disclosure of these records.
2. A record from this system of records may be disclosed, as a routine use, in the course of presenting evidence to a court, magistrate, or administrative tribunal, including disclosures to opposing counsel in the course of settlement negotiations.
3. A record in this system of records may be disclosed, as a routine use, to a Member of Congress submitting a request involving an individual, to whom the record pertains, when the individual has requested assistance from the Member with respect to the subject matter of the record.
4. A record in this system of records may be disclosed, as a routine use, to a contractor of the Agency having need for the information in order to perform a contract. Recipients of information shall be required to comply with the requirements of the Privacy Act of 1974, as amended, pursuant to 5 U.S.C. 552a(m).
5. A record related to an International Application filed under the Patent Cooperation Treaty in this system of records may be disclosed, as a routine use, to the International Bureau of the World Intellectual Property Organization, pursuant to the Patent Cooperation Treaty.
6. A record in this system of records may be disclosed, as a routine use, to another federal agency for purposes of National Security review (35 U.S.C. 181) and for review pursuant to the Atomic Energy Act (42 U.S.C. 218(c)).
7. A record from this system of records may be disclosed, as a routine use, to the Administrator, General Services, or his/her designee, during an inspection of records conducted by GSA as part of that agency's responsibility to recommend improvements in records management practices and programs, under authority of 44 U.S.C. 2904 and 2906. Such disclosure shall be made in accordance with the GSA regulations governing inspection of records for this purpose, and any other relevant (i.e., GSA or Commerce) directive. Such disclosure shall not be used to make determinations about individuals.
8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

PART B - FEE(S) TRANSMITTAL

**Complete and send this form, together with applicable fee(s), to: Mail Mail Stop ISSUE FEE
Commissioner for Patents
P.O. Box 1450
Alexandria, Virginia 22313-1450
or Fax (571)-273-2885**

INSTRUCTIONS: This form should be used for transmitting the ISSUE FEE and PUBLICATION FEE (if required). Blocks 1 through 5 should be completed where appropriate. All further correspondence including the Patent, advance orders and notification of maintenance fees will be mailed to the current correspondence address as indicated unless corrected below or directed otherwise in Block 1, by (a) specifying a new correspondence address; and/or (b) indicating a separate "FEE ADDRESS" for maintenance fee notifications.

CURRENT CORRESPONDENCE ADDRESS (Note: Use Block 1 for any change of address):

21888 7590 05/01/2018
THOMPSON COBURN LLP
ONE US BANK PLAZA
SUITE 3500
ST LOUIS, MISSOURI 63101
UNITED STATES OF AMERICA

Note: A certificate of mailing can only be used for domestic mailings of the Fee(s) Transmittal. This certificate cannot be used for any other accompanying papers. Each additional paper, such as an assignment or formal drawing, must have its own certificate of mailing or transmission.

Certificate of Mailing or Transmission

I hereby certify that this Fee(s) Transmittal is being deposited with the United States Postal Service with sufficient postage for first class mail in an envelope addressed to the Mail Stop ISSUE FEE address above, or being facsimile transmitted to the USPTO (571) 273-2885, on the date indicated below.

(Depositor's name)
(Signature)
(Date)

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/315,571	06/26/2014	David E. Taylor	57451-133596	1085

TITLE OF INVENTION: Method and Apparatus for High-Speed Processing of Financial Market Depth Data

APPLN. TYPE	ENTITY STATUS	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	SMALL	\$500	\$0.00	\$0.00	\$500	08/01/2018

EXAMINER	ART UNIT	CLASS-SUBCLASS
ROBINSON, KITO R	3695	705-035000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).

☐ Change of correspondence address (or Change of Correspondence Address form PTO/SB/122) attached.

☐ "Fee Address" indication (or "Fee Address" Indication form PTO/SB/47; Rev 03-02 or more recent) attached. **Use of a Customer Number is required.**

2. For printing on the patent front page, list
(1) The names of up to 3 registered patent attorneys or agents OR, alternatively,
(2) The name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.

1. Thompson Coburn LLP
2.
3.

3. ASSIGNEE NAME AND RESIDENCE DATA TO BE PRINTED ON THE PATENT (print or type)

PLEASE NOTE: Unless an assignee is identified below, no assignee data will appear on the patent. If an assignee is identified below, the document has been filed for recordation as set forth in 37 CFR 3.11. Completion of this form is NOT a substitute for filing an assignment.

(A) NAME OF ASSIGNEE

IP Reservoir, LLC

(B) RESIDENCE: (CITY AND STATE OR COUNTRY)

St. Louis, Missouri

Please check the appropriate assignee category or categories (will not be printed on the patent): ☐ Individual ☒ Corporation or other private group entity ☐ Government

4a. The following fee(s) are submitted:

- ☒ Issue Fee
☐ Publication Fee (No small entity discount permitted)
☐ Advance Order - # of Copies

4b. Payment of Fee(s): (Please first reapply any previously paid issue fee shown above)

- ☐ A check is enclosed.
☐ Payment by credit card. Form PTO-2038 is attached.
☒ The director is hereby authorized to charge the required fee(s), any deficiency, or credits any overpayment, to Deposit Account Number 26-0823 (enclose an extra copy of this form).

5. Change in Entity Status (from status indicated above)

- ☐ Applicant certifying micro entity status. See 37 CFR 1.29
☐ Applicant asserting small entity status. See 37 CFR 1.27
☐ Applicant changing to regular undiscounted fee status.

NOTE: Absent a valid certification of Micro Entity Status (see forms PTO/SB/15A and 15B), issue fee payment in the micro entity amount will not be accepted at the risk of application abandonment.
NOTE: If the application was previously under micro entity status, checking this box will be taken to be a notification of loss of entitlement to micro entity status.
NOTE: Checking this box will be taken to be a notification of loss of entitlement to small or micro entity status, as applicable.

NOTE: This form must be signed in accordance with 37 CFR 1.31 and 1.33. See 37 CFR 1.4 for signature requirements and certifications.

Authorized Signature /Benjamin L. Volk, Jr./ Date July 25, 2018
Typed or printed name Benjamin L. Volk, Jr. Registration No. 48,017

Electronic Patent Application Fee Transmittal				
Application Number:		14315571		
Filing Date:		26-Jun-2014		
Title of Invention:		Method and Apparatus for High-Speed Processing of Financial Market Depth Data		
First Named Inventor/Applicant Name:		David E. Taylor		
Filer:		Benjamin Lowell Volk/Deanna Woll		
Attorney Docket Number:		57451-133596		
Filed as Small Entity				
Filing Fees for Utility under 35 USC 111(a)				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
UTILITY APPL ISSUE FEE	2501	1	500	500

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension-of-Time:				
Miscellaneous:				
Total in USD (\$)				500

Electronic Acknowledgement Receipt	
EFS ID:	33282122
Application Number:	14315571
International Application Number:	
Confirmation Number:	1085
Title of Invention:	Method and Apparatus for High-Speed Processing of Financial Market Depth Data
First Named Inventor/Applicant Name:	David E. Taylor
Customer Number:	21888
Filer:	Benjamin Lowell Volk/Deanna Woll
Filer Authorized By:	Benjamin Lowell Volk
Attorney Docket Number:	57451-133596
Receipt Date:	25-JUL-2018
Filing Date:	26-JUN-2014
Time Stamp:	16:00:34
Application Type:	Utility under 35 USC 111(a)

Payment information:

Submitted with Payment	yes
Payment Type	DA
Payment was successfully received in RAM	\$ 500
RAM confirmation Number	072618INTEFSW00002483200823
Deposit Account	200823
Authorized User	Deanna Woll
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: 37 CFR 1.20 (Post Issuance fees) 37 CFR 1.21 (Miscellaneous fees and charges)	

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Issue Fee Payment (PTO-85B)	Issue_Fee_Transmittal.pdf	958032	no	1
			9a5e4ada3a674bc4e192085772af41d73d110819		
Warnings:					
Information:					
2	Fee Worksheet (SB06)	fee-info.pdf	30523	no	2
			1226ca8f14d39247fc6591052dae49e9adec1baaf		
Warnings:					
Information:					
Total Files Size (in bytes):			988555		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Receipt date: 11/11/2014

14315571 - GAU: 3695

Doc code: IDS

PTO/SB/08a (01-10)

Doc description: Information Disclosure Statement (IDS) Filed

Approved for use through 07/31/2012. OMB 0651-0031

U.S. Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Not for submission under 37 CFR 1.99)	Application Number		14315571	
	Filing Date		2014-06-26	
	First Named Inventor	David E. Taylor		
	Art Unit	3693		
	Examiner Name	Merchant, Shahid R.		
	Attorney Docket Number	57451-133596		

U.S.PATENTS						Remove
Examiner Initial*	Cite No	Patent Number	Kind Code ¹	Issue Date	Name of Patentee or Applicant of cited Document	Pages,Columns,Lines where Relevant Passages or Relevant Figures Appear
	1	2046381		1936-07-07	Hicks et al.	
	2	3082402		1963-03-19	Scantlin	
Change(s) applied to document, /G.R.P./ 5/4/2018	3	3296597		~~01-1967~~ ~~1971-01-03~~	Scantlin et al.	
	4	3573747		1971-04-06	Adams et al.	
	5	3581072		1971-05-25	Nymeyer	
	6	3601808		1971-08-24	Vlack	
	7	3611314	A	1971-10-05	Pritchard, Jr., et al.	
	8	3729712	A	1973-04-24	Glassman	



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Alexandria, Virginia 22313-1450
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APPLICATION NO.	ISSUE DATE	PATENT NO.	ATTORNEY DOCKET NO.	CONFIRMATION NO.
14/315,571	08/28/2018	10062115	57451-133596	1085

21888 7590 08/08/2018
THOMPSON COBURN LLP
ONE US BANK PLAZA
SUITE 3500
ST LOUIS, MO 63101

ISSUE NOTIFICATION

The projected patent number and issue date are specified above.

Determination of Patent Term Adjustment under 35 U.S.C. 154 (b) (application filed on or after May 29, 2000)

The Patent Term Adjustment is 1014 day(s). Any patent to issue from the above-identified application will include an indication of the adjustment on the front page.

If a Continued Prosecution Application (CPA) was filed in the above-identified application, the filing date that determines Patent Term Adjustment is the filing date of the most recent CPA.

Applicant will be able to obtain more detailed information by accessing the Patent Application Information Retrieval (PAIR) WEB site (<http://pair.uspto.gov>).

Any questions regarding the Patent Term Extension or Adjustment determination should be directed to the Office of Patent Legal Administration at (571)-272-7702. Questions relating to issue and publication fee payments should be directed to the Application Assistance Unit (AAU) of the Office of Data Management (ODM) at (571)-272-4200.

APPLICANT(s) (Please see PAIR WEB site <http://pair.uspto.gov> for additional applicants):

David E. Taylor, St. Louis, MO;
IP Reservoir, LLC, St. Louis, MO;
Scott Parsons, St. Charles, MO;
Jeremy Walter Whatley, Ballwin, MO;
Richard Bradley, St. Louis, MO;
Kwame Gyang, St. Louis, MO;
Michael DeWulf, St. Louis, MO;

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