

**UNITED STATES PATENT AND TRADEMARK OFFICE**

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**BEFORE THE PATENT TRIAL AND APPEAL BOARD**

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SK HYNIX INC. and SK HYNIX AMERICA INC.,  
Petitioners,

v.

NETLIST, INC.  
Patent Owner

Patent No. 9,858,218

Issued: January 2, 2018

Filed: April 1, 2016

Inventors: Hyun Lee

Title: Memory Module And Methods For Handshaking With A Memory  
Controller

*Inter Partes* Review No. IPR2020-01044

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**PETITION FOR *INTER PARTES* REVIEW OF  
U.S. PATENT NO. 9,858,218**

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Petition for *Inter Partes* Review of U.S. Patent No. 9,858,218

**Attachment A. Proof of Service of the Petition**

**Attachment B. List of Evidence and Exhibits Relied Upon in Petition**

**Attachment C. Table of Claims and Elements**

## **I. INTRODUCTION**

Petitioners respectfully request trial on claims 1-22 of U.S. Patent 9,858,218 (“218 Patent”)(EX1001) based on the obvious combination of Hazelzet with either JEDEC or Buchmann. JEDEC is a ballot on a draft proposal (with the proposal included) distributed to members of a JEDEC standards committee in November 2009. It discloses the exact technique the 218 Patent asserts as its advance over the prior art – the use by a memory module of a single open drain output to provide parity error information in an operational mode and status information in a training mode. Combined with Hazelzet, a detailed description of a memory module that employs the same open drain output in two different operational modes, it satisfies every element of all the claims. As demonstrated below, JEDEC is prior art here because the claims of the 218 Patent are not entitled to their provisional application priority date.

Regardless of priority date, however, the combination of Hazelzet and Buchmann also renders the claims unpatentable. A panel of the Board recently found all claims of a related patent, having the same specification and claiming the same open drain signaling technique as the 218 Patent, to be unpatentable based on this combination. IPR2018-00303, Paper 42 (EX1034, 22). That same combination renders the 218 claims unpatentable as well.

## **II. COMPLIANCE WITH REQUIREMENTS FOR A PETITION FOR INTER PARTES REVIEW**

### **A. Certification the 218 Patent May Be Contested by Petitioners**

Petitioners certify they are not barred or estopped from requesting *inter partes* review of the 218 Patent. Neither Petitioners, nor any party in privity with Petitioners, has filed a civil action challenging the validity of any claim of the 218 Patent. The 218 Patent has not been the subject of a prior *inter partes* review by either Petitioners or a privy of Petitioners. Petitioners also certify this petition for *inter partes* review is filed within one year of the date of service of a complaint alleging infringement of the patent and that this patent is available for *inter partes* review.

### **B. Fee for Inter Partes Review (§ 42.15(a))**

The Director is authorized to charge the fee specified by 37 CFR § 42.15(a) to Deposit Account No. 50-1597.

### **C. Mandatory Notices (37 CFR § 42.8(b))**

The real parties in interest are the Petitioners and their respective corporate parents: SK hynix Inc. and SK hynix America Inc.

The 218 Patent is involved in the following legal proceedings:

- *Netlist, Inc. v. SK Hynix Inc. et al.*, Case No. 6:20-CV-00194 (W.D. Tex.)

The 218 Patent is related to the following legal proceedings:

Petition for *Inter Partes* Review of U.S. Patent No. 9,858,218

- *SK Hynix Inc., et al. v Netlist, Inc.*, IPR2020-01042
- *Netlist, Inc. v. SK Hynix Inc., et al.*, Case No. 8:17-cv-01030 (C.D. Ca.)
- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1089 (International Trade Commission)
- *SK Hynix Inc., et al. v Netlist, Inc.*, IPR2018-00303
- *Netlist, Inc. v. SK Hynix Inc., et al.*, Case No. 8:16-cv-01605 (C.D. Ca.)
- *In the Matter of Certain Memory Modules and Components Thereof, and Products Containing Same*, Inv. No. 337-TA-1023 (International Trade Commission)
- *SK Hynix Inc., et al. v Netlist, Inc.*, IPR2017-00548

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Service on Petitioner may be made by mail or hand delivery to: Sidley Austin LLP, 1501 K Street, N.W., Washington, D.C. 20005. The fax number for lead and backup counsel is (202) 736-8711.

**D. Proof of Service (§§ 42.6(e) and 42.105(a))**

Proof of service of this petition is provided in **Attachment A**.

**III. IDENTIFICATION OF CLAIMS BEING CHALLENGED  
(§ 42.104(B))**

Claims 1-22 of the 218 Patent are unpatentable as follows:

- (i) Claims 1-22 are obvious in view of Hazelzet and JEDEC;
- (ii) Claims 1-22 are obvious in view of Hazelzet and Buchmann;
- (ii) Claims 3-6, 10-12, and 17-20 are obvious in view of Hazelzet, JEDEC or Buchmann, and Kim.

Petitioners' proposed claim constructions, the evidence relied upon, and the precise reasons why the claims are unpatentable are provided below. The evidence relied upon in this petition is listed in **Attachment B**.

**IV. RELEVANT INFORMATION CONCERNING THE  
CONTESTED PATENT**

**A. Effective Filing Date of the 218 Patent**

The 218 Patent is a continuation of, *inter alia*, a utility application filed June 14, 2010, and also claims priority to U.S. Provisional Application No. 61/186,799 (EX1008), filed June 12, 2009. EX1001, Face. The claims of the 218 Patent are **not**, however, entitled to the June 2009 date, for multiple reasons:

**1. Unsupported Negative Limitation – Claims 7, 9, 15**

Each of independent claims 9 and 15 (and claim 7 that depends from claim 1) include a negative limitation requiring “train[ing] with one or more training sequences *while the first edge connections [i.e., for data] are **not** active.*” *E.g.*,



EX1001, 15:60-61 (claim 9), 16:48-50 (claim 15), 15:31-34 (claim 7); EX1003, ¶44.

For the claims of the 218 Patent to be entitled to the benefit of the provisional's filing date, the provisional must provide written description support for those claims, including for that negative limitation. 35 U.S.C. §§ 119(e), 112(a). To meet that standard, Patent Owner must show from the disclosure of the provisional that the inventor was in "possession" of the invention, which means that "the written description must include all of the limitations of the [claims], or the applicant must show that any absent text **is necessarily comprehended** in the description provided and would have been so understood at the time the patent application was filed." *Hyatt v. Boone*, 146 F.3d 1348, 1354-55 (Fed.Cir. 1998).<sup>1</sup>

Patent Owner cannot do so. There is no disclosure in the provisional of training "while the first edge connections are not active." As Dr. Alpert explains, the single sentence fragment of the provisional referencing training – "Error-Out pin: Low during MB training (high signal indicates that training is done)" – never describes such a relationship between "training" and edge connections, either explicitly or implicitly. EX1003, ¶45. Indeed, edge connections are not even mentioned in the provisional application, let alone associated with "training."

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<sup>1</sup> All emphasis in bold in this document has been added.

Moreover, it was known before the 2009 provisional filing date that some training included sending data over the data edge connections, while other training did not. Specifically, a Skilled Artisan would understand the provisional's "MB training" as a generic reference to "training" in the context of memory buffers. To the extent one might argue it refers to something more specific, a Skilled Artisan would, at most, understand the phrase in this context (where the provisional refers to the then current LRDIMMs under development/standardization, DDR3 LRDIMM) as referring to training of the interfaces to/from and/or operations of the type of register/buffer used in DDR3 LRDIMMs. EX1036, 4; EX1003, ¶45.

It was known, however, that such buffers employed memory read and write operations instituted by the memory controller that transferred data over the edge connections with the data pins ("*first edge connections*") during some training modes. For instance, JEDEC, a ballot on a draft DDR3 LRDIMM standard, discloses a Host-MB training mode that employs memory read and write operations instituted by the memory controller that transferred data over the edge connections with the data pins ("*first edge connections*") during the training mode. EX1015, 8-9 ( "The host performs normal writes to DRAM for write DQ/DQS margining ...[t]he host performs read DQ/DQS margining by using normal reads from DRAM ..."); EX1039, 10-11 (disclosing "Host-MB Training" before June 12, 2009 provisional filing date); EX1022, ¶¶[0039],[0043],[0053] (employing

read/write operations transferring data to module during training); EX1003, ¶47.

Thus, Patent Owner cannot show from the provisional's disclosure that the negative limitation that "*the first edge connections [i.e., for data] are not active*" during training "is necessarily comprehended" in that disclosure because it was known that some types of "MB training" did in fact include active first edge connections on which data was being transferred.

## **2. Unsupported Negative Limitation – Claim 1**

Claim 1 requires that its memory module be "configured to perform one or more memory read or write operations *not associated with the one or more training sequences* by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections." EX1001, 14:57-62. However, the terms "read operation," "write operation" (or just "write"), "data signals" (or just "data"), "edge connections" (or just "edge"), "address signals" (or just "address"), and "command signals" appear nowhere in the provisional. There are two passing references to "normal operation" in the provisional, and perhaps Patent Owner will argue that necessarily provides support for all the aforementioned terms and their interrelations during "normal operation." But nothing in the provisional says that its "training" is necessarily excluded from its "normal operation." In fact, as Dr. Alpert explains, a Skilled Artisan would understand training could occur during normal operation.

For instance, Buchmann discloses the options of utilizing either “memory channel repair and re-initialization” or “fast repair and re-initialization,” both of which employ some of Buchmann’s training and which may (though not necessarily) occur during “functional mode,” which Buchmann describes as “normal, run-time operation.” EX1016, 12:60-13:41. During that “functional mode” when errors are encountered, either “repair” or “fast repair” is utilized before a “retry command,” and occurs so fast “other system components will not time-out during the repair and re-init process.” *Id.*, 13:29-34; EX1003, ¶48. Thus, the provisional should have disclosed how its reads/writes (which it does not explicitly disclose in any event) are unassociated with its training (which is just a generic reference to “MB training”), if Patent Owner wanted to provide support for this negative limitation. EX1003, ¶49.

### **3. “One or More” Training “Sequences”**

Each independent claim of the 218 Patent also requires its memory module to be “configured to be trained with one or more training sequences” or “training with one or more training sequences.” EX1001, 14:55-56 (claim 1), 15:60 (claim 9), 16:48-49 (claim 15); EX1003, ¶50. The provisional, however, only discloses “MB training”, that a Skilled Artisan would understand as a generic disclosure of “training” a memory buffer in some way. It does not disclose any training “sequences,” and particularly not “one or more” training sequences. EX1003, ¶51.

The claims of the 218 Patent are accordingly entitled to a priority date no earlier than **June 14, 2010**.

**B. Person of Ordinary Skill in the Art**

A person of ordinary skill in the art in the field of the 218 Patent in the 2009-10 time frame (“a Skilled Artisan”) would have had a bachelor’s degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. She would have been familiar with computer memory systems and basic CPU architecture documented in the literature, including standards, and generally available in commercial systems, including how computer components access a computer’s memory, the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system. EX1003, ¶52.

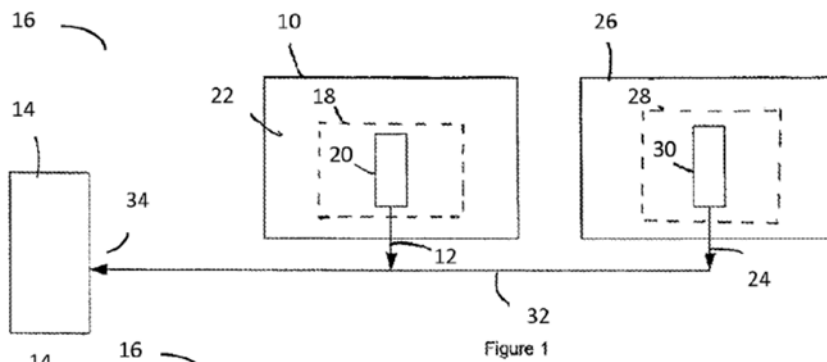
**C. The 218 Patent**

**1. Technical Overview**

The 218 Patent describes “a method of establishing a handshake mechanism based on notification signaling” that “can be implemented by adding a new interface (notifying) signal between the MCH [*i.e.*, system memory controller] and the memory subsystem controller,” and that this interface “can be an open drain signaling from the memory subsystem controller to the MCH.” EX1001, 4:1-12; EX1003, ¶53.

According to the 218 Patent, “there [was] no existing method of handshaking between the MCH (*e.g.*, system memory controller) and a memory subsystem (*e.g.*, memory module) during initialization.” EX1001, 2:59-62. And that “in conventional systems, the system memory controller does not monitor the error-out signal from the memory subsystem.” *Id.* at 2:62-3:2. The 218 Patent states that “typical” servers of the prior art would instead, after commencing memory module initialization, simply wait a predetermined amount of time and then assume the memory subsystem had completed initialization. EX1001, 3:3-17; EX1003, ¶54.

Figure 1 shows a computer system including memory module 10 coupled to a memory controller 14 via “output 12” which is driven by notification circuit 20 of controller circuit 18.



EX1001, 4:19-37, FIG. 1. Memory module 26 is also shown, and has essentially the same structure as module 14, having “output 24” driven by notification circuit 30 of controller circuit 28. *Id.* at 6:23-44; EX1003, ¶56.

In one specific example of handshaking, the interface between the memory controller (MCH) and memory subsystem controller is implemented using a technique called open drain signaling. EX1001, 4:12-16, 9:47-53, FIGs. 2-3. Specifically, output 12 of module 10 and output 24 of module 26 are both tied to the same bus 32 using an open drain configured transistor. EX1001, 4:12-23, 9:51-67, FIGs. 2-3; EX1003, ¶57.

In that configuration, when starting an initialization procedure, each memory module will drive the gate of the transistor of its open drain output high, placing a logic level low (low impedance) signal on bus 32. When the initialization is complete, the memory module can drive the gate of the transistor, placing a logic level high (high impedance) signal on bus 32. However, because all of the outputs of multiple memory modules are tied to the same bus 32 in an open drain configuration, the state of bus 32 will remain logic level low (low impedance) until each memory module drives the gate of the transistor of its open drain output low, placing a logic level high (high impedance) on its output, which then allows “the bus 32 [to] be pulled high by the internal pull-up configuration 40 of the system memory controller 14.” EX1001, 9:47-10:50. In this manner, the system memory controller may be provided the status of an initialization procedure (*e.g.*, either that it is currently executing or complete) using only a single bus line from multiple memory modules. *Id.*; EX1003, ¶58.

The 218 Patent further states that bus 32 could be tied to a standard-defined (such as JEDEC) error output pin that is not required by the standard to be used during initialization. EX1001, 8:4-33. The patent states that output 12 can be operatively coupled to the error-out pin of memory module 10, which is connected to a multiplexor 42 driving the transistor 36 with either of a `task_in_progress` signal 44 or an error signal 46 (*e.g.*, parity error signal). EX1001, 11:16-20, FIG. 3. According to the 218 Patent, “the memory module 10 can be advantageously configured to both perform the standard (*e.g.*, JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode.” EX1001, 11:26-31; EX1003, ¶59.

## **2. Prosecution History**

### **a) 218 Patent**

The 218 Patent issued from U.S. Patent Application Serial No. 15/088,115 (“115 Application”), filed on April 1, 2016, and claims priority to two utility and one provisional applications. EX1001, 1-2. The 115 Application originally presented 20 claims, which were cancelled after rejection and replaced with new



claims 21-42. EX1002, 30-33, 68-81.<sup>2</sup> Importantly, the original claims included no limitation directed to “training.. EX1002, 30-33.

The new claims were drawn to a memory module, or method of operating one, that required an open drain output for **both** a parity error signal during normal operation and a notification signal while carrying out *training sequences* outside of normal operation. *See e.g.* EX1002, 70.

These new claims were finally rejected over the combination of Moshayedi (EX1011, U.S. 2010/0202240) in view of Fahr (EX1012, U.S. 2008/0256281). EX1002, 100-107. The examiner cited Moshayedi for the training sequence limitations, including the output of a training sequence notification signal over the same open-drain output used for parity error during normal mode. EX1002, 103. Oddly, Fahr was cited only for disclosing “**two** open-drain outputs,” even though none of the claims required two open-drain outputs. *Id.*

In an after-final response, the Applicant argued that neither Moshayedi nor Fahr disclosed the open-drain and training sequence limitations of the claims, EX1002, 139-143. After that response was not entered, *id.*, 151, the Applicant filed an RCE and repeated the arguments., *id.*, 167, 174-78.

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<sup>2</sup> The Applicant also filed a terminal disclaimer. EX1002, 60-67.

The claims were rejected again based on the same prior art, with the examiner again citing Moshayedi as satisfying the “training sequence” and open-drain limitations of the claims and Fahr cited for its two open drain outputs. *Id.*, 187-88. In response, the Applicant amended the claims to require a “first mode” during which the recited training sequence would occur and which was different from a “second mode” not associated with the training sequence, and also to specify that the training sequence notification signal be output “while the memory module is in the first mode.” *Id.*, 204-05. It argued, among other things, that the “paragraphs cited by the Examiner do not even come close to disclosing or teaching ‘wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences.’” *Id.*, 215. The claims were then allowed. EX1002, 228-232.

**b) Related 623 Patent**

U.S. Patent No. 9,535,623 is a continuation of the 218 Patent. EX1031, Face. The 623 Patent claims the same technique of using a single open drain output to send two different signals, one for parity error in a “first mode” and one for a notification signal related to “training sequences” in a “second mode.” EX1031, 15:26-58. In IPR2018-00303, the Board found all claims of the 623

Patent to be unpatentable over the obvious combination of Hazelzet and Buchmann, EX1034, the same combination asserted in this petition.<sup>3</sup>

**3. 35 U.S.C. 314(a)**

Patent Owner may argue that institution should be denied based on the existence of a parallel district court proceeding involving the patent at issue here, pursuant to *NHK Spring Co. v. Intri-Plex Tech*, IPR2018-00752, Paper 8 (precedential). But the facts of *NHK* were very different from here, where a discretionary denial is not supported. In *NHK*, the institution decision issued a mere six months before trial in district court on the same patent and prior art was scheduled. The panel denied institution based on Section 325(d), but noted as an additional factor supporting denial that “the district court proceeding will analyze

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<sup>3</sup> The 218 Patent is a continuation of U.S. Patent No. 8,489,837, EX1001, 1-2, which claimed the same handshake technique described in the 218 Patent. EX1019, 3:24-4:2, 14:5-20. And while those claims do not mention training, the terminal disclaimer filed during prosecution of the 218 Patent disclaimed any term beyond that of the 837 Patent. EX1002, 61. The Board found all claims of the 837 Patent to be unpatentable in IPR2017-00548, EX1035, a finding Patent Owner did not appeal.

the same issues and will be resolved before any trial on the Petition concludes.” *Id.*, 19-20. That is simply not the situation here.

Here, Petitioners were sued on the 218 Patent in the Western District of Texas on March 17, 2020, but have not yet answered the complaint and by stipulation need not answer or otherwise respond to the complaint until July 21, 2020. The Court has scheduled a case management conference for June 19, and by practice appears to schedule trial 18 months or so after such a conference. However, the judge (recently appointed) to which the case has been assigned has not yet held any patent jury trials, so there is no record on which to gage the likelihood of that schedule not changing. On the other hand, since 2008, the average time to trial for patent jury trials in that district is almost 32 months. EX1030, 2. Indeed, considering the disruption in court scheduling caused by the COVID19 pandemic, it would be unreasonable to assume any court could improve upon its time to trial in the next few years. EX1028, 1-5. To the contrary, the only reasonable conclusion here is that the issues raised in the Texas case will not be resolved until long after this IPR has concluded, meaning the estoppel of Section 315(e) will apply and no duplication of effort will occur.

Moreover, Petitioners have moved to transfer that Texas case to the Central District of California, where Patent Owner had previously sued Petitioners on both the 837 Patent (grand-parent of 218 Patent) and the 623 Patent (parent of 218

Patent). In those cases, which are presently pending but stayed, Patent Owner asserts the 837 and 623 patents against the same products against which the 218 Patent is asserted, and Petitioners raise the same, or similar, RAND issues that will be at issue in Texas, including issues regarding what constitutes a RAND royalty rate for any Netlist essential patents. Thus, at a minimum, Petitioners' transfer motion is well-founded, and may very well take any trial scheduled in Texas off calendar.

This case is therefore wholly distinguishable from *NHK*, and the Board should not deny institution on that basis.

**4. 35 U.S.C. 325(d)**

The prior art analyzed and arguments asserted in this petition are not the same or substantially the same as those before the examiner of the 218 Patent, and the examiner clearly erred in issuing the 218 Patent. The Board should therefore not deny institution based on Section 325(d).

***a) This Petition Presents Substantially Different Prior Art***

This petition is based on the obvious combination of Hazelzet with either JEDEC or Buchmann.

JEDEC, however, was not before the examiner and discloses precisely the supposed advance over the prior art, *i.e.*, use of single open drain output to output parity error during normal operations and training notification signals during a

training mode. §§IV.C.2 (prosecution history), V.B (JEDEC). There was nothing remotely similar to that before the examiner. Indeed, nothing before the examiner disclosed the use of an open drain output in a training mode at all, let alone its use in a separate mode as well. The prior art and JEDEC-based arguments advanced here are therefore not substantially the same as those before the examiner.

Buchmann, also, was *not* before the examiner of the 218 Patent; nor was any other reference like Buchmann. Specifically, over the course of six columns Buchmann provides an expansive disclosure of eight different memory module training sequences, labelled TS0 through TS7, and the signaling associated with them. EX1016, 5:40-11:47. Importantly, as the Board in IPR2018-00303 found, Buchmann's disclosed signaling includes notification signals relating to training sequences. EX1034, 12 (“In other words, Buchmann discloses a memory controller connected to a memory module that operates in a mode in which the memory module executes a training sequence and notifies the memory controller of the status of the training sequence (e.g., successful).”) As explained above, the 218 Patent explicitly distinguishes between such notification signals and prior art polling signals, which the patent disparages. EX1001, 3:38-58. Thus, as the Board found in IPR2018-00303, Buchmann discloses exactly the type of signaling at the heart of the claims here and identified in the specification as a distinguishing feature of the invention.

The examiner of the 218 Patent had nothing of the sort before him either. The examiner relied mainly on Moshayedi for training-related claim limitations, EX1002, 103-105, 188-190, but that reference has nothing to do with training sequences in memory modules, let alone the use of notification signals during training. It does not even use the word “train,” or any form of it.

Moreover, as Dr. Alpert testifies, he has reviewed the prior art before the examiner and can confirm that it does not include anything remotely similar to the dual use of an open drain output for parity error and notification signals, as JEDEC discloses, or the broad disclosure regarding training sequences found in Buchmann, or anything about training sequences at all. EX1003, ¶.

The differences between JEDEC and Buchmann, on the one hand, and the prior art before the examiner, on the other, are therefore substantial. Indeed, as demonstrated above, the principal argument for patentability made during prosecution was that the claims required using the same open-drain output normally used for parity error for a notification regarding training, and the art of record did not disclose that technique. Thus, the additional subject matter brought by JEDEC and Buchmann goes to the precise reason the claims were allowed.

*b) This Petition Presents Substantially Different*

***Arguments***

Because JEDEC and Buchmann constitutes such different prior art than what was before the examiner, the arguments advanced here are substantially different from those asserted during prosecution.

Moreover, the examiner cited Fahr solely for its disclosure of two open-drain outputs, EX1002, 103, a feature not even required by the 218 Patent claims. As demonstrated below, in this petition Hazelzet – which shares some disclosure with Fahr -- is relied on for the disclosure of using *the same* open-drain output *for two different purposes*, as well as for numerous other details of the claims. The use of two open-drain outputs, and the use of the same open-drain output for two dissimilar purposes, are two very different things. The examiner's citation to Fahr was essentially irrelevant to the claims; the analysis of Hazelzet below goes to several core aspects of the claims, and represents a substantially different argument than those made during prosecution.

***c) The Examiner Erred***

Finally, the examiner of the 218 Patent clearly erred in issuing the claims, at least because he did not have before him prior art relating to the open drain signaling limitations that form the heart of these claims. Moreover, he plainly misunderstood the claim requirements relating to an open-drain output, as his



citation to Fahr for the disclosure of two such outputs, when the claim required one used for two purposes, demonstrates. EX1003, ¶91.

The examiner's error has been confirmed by the Board's decision in IPR2018-00303, finding all claims of the 623 Patent unpatentable over the obvious combination of Hazelzet and Buchmann. EX1034. As noted above, the 623 Patent is a continuation of the 218 Patent. The claims of both are strikingly similar. Just by way of example, claim 1 of both patents is directed to a memory module on a printed circuit board having various edge connections, including an error edge connection. EX1001 at claim 1; EX1031 at claim 1. Both require that the module operate in two modes, one for normal operation and one for training. *Id.* And both require an open drain output that is used both for parity error during normal operation and for a notification signal during training. *Id.*; EX1003, ¶¶85-86.

The petition in IPR2018-00303 challenging the claims of the 623 Patent was based primarily on the combination of Hazelzet and Buchmann. EX1032, 3-4. The petition argued, as this one does, that it would have been obvious to combine Hazelzet and Buchmann such that a single open drain output of Hazelzet would be used for a parity error signal during normal operations, as disclosed in Hazelzet, and for a training sequence notification signal, per Buchmann, EX1033, ¶¶164-174; EX1003, ¶87. The petition also argued, as this one does too, that a Skilled Artisan would have been motivated to make this combination because it would

have improved overall system reliability, EX1032, 63-64, would have complimented Hazelzet's existing initialization sequence, EX1032, 64, and "would have been merely a use of prior art techniques for prior art purposes with only expected results," EX1032, 56. Moreover, as with the present petition, the petition arguments in IPR2018-00303 were supported by detailed citations to numerous prior art references and the thorough analysis of Dr. Alpert, a long time expert in the field. EX1033, ¶¶165-175; EX1003, ¶¶87-88.

In its Final Written Decision in IPR2018-00303, the Board agreed with these arguments, expressly stating that "we agree with Petitioner's showing that the combination of Hazelzet and any one of Buchmann or Talbot teaches every limitation of claims 1, 12, and 21 of the '623 patent and that a Skilled Artisan would have had reason, with rational underpinning, to combine the references." EX1034, 13. The Board stated "[f]urther, we credit Dr. Alpert's supporting testimony (EX1003, ¶¶121-150, 158-186), as it is consistent with the prior art disclosures." EX1034, 13; EX1003, ¶89.

The examiner of the 218 Patent never saw the analysis, evidence or conclusions of the Board in IPR2018-00303, as the Final Written Decision in that proceeding issued more than a year after the 218 Patent issued, and none of the submissions from that IPR were disclosed to the examiner of the 218 Patent. Given the striking similarity between the claims of the 218 patent and the

unpatentable claims of the 623 Patent, the only reasonable conclusion that can be drawn is that the examiner of the 218 Patent erred. EX1003, ¶90.

**D. Construction of Terms Used in the Claims**

Claim terms are generally given their ordinary meaning in the context of the patent as understood by a Skilled Artisan. 37 CFR § 42.100(b); *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312-13 (Fed.Cir. 2005) (*en banc*). If Patent Owner contends claim terms should have a special meaning, those contentions should be disregarded unless Patent Owner successfully amends the claims compliant with 35 U.S.C. § 112 to make them expressly correspond to those contentions. 77 Fed. Reg. 48,764 at II.B.6 (August 14, 2012); *cf. In re Youman*, 679 F.3d 1335, 1343 (Fed.Cir. 2012).

**1. “memory read or write operations”**

In the context of the 218 Patent, a Skilled Artisan would understand the ordinary meaning of “*memory read and write operations*” to be operations used to communicate data between the memory module and the memory controller in response to commands from the memory controller. EX1003, ¶95.

In the claims this phrase refers to operations used to read or write DRAMs in response to address and control signals received from the system memory controller. EX1001, 14:63-15:1; EX1003, ¶96. Similarly, the 218 Patent explains that “[d]uring the read/write operations, the memory module **communicates data**

with the memory controller via the data signal pins **in response to second memory commands received via the address and control signal pins.**”

EX1001, 1:52-56. It further states that, during such operations, the module controller will transmit the command and address signals received from the system memory controller to the memory devices. EX1001, 5:40-47. The intrinsic record therefore confirms that this phrase refers to operations used to read from or write to memory devices in response to commands from the memory controller. EX1003, ¶97.

## 2. “mode”

During the 837 Patent IPR, Patent Owner sought to have the term “mode” interpreted to mean “a distinct behavioral state that a system may be switched to.” EX1035, 7. Petitioners objected for several reasons, including because it became clear that Patent Owner sought to use the word “distinct” to inject several unwarranted concepts and ambiguities into the claims, such as that different “modes” must necessarily include mutually exclusive operations, EX1041, 6, which was inconsistent with the disclosure of the 837 Patent (and of the 218 Patent) that the disclosed memory operations may be used in both an operational mode and an initialization mode. EX1001, 6:46-52. The Board accordingly declined to construe the word “mode.” EX1035, 7. Indeed, the intrinsic record

never defines the term “mode” or uses it in any special sense, so the Board should take the same approach here. EX1003, ¶¶98-102.

**3. “training sequence”**

In the context of the 218 Patent, a Skilled Artisan would understand the ordinary meaning of “*training sequence*” to be a set of operations occurring in a particular order and used for training. EX1003, ¶103.

Generally, a “sequence” is “a set of related events, movements, or things that follow each other in a particular order.” EX1042, 1; EX1003, ¶104.

The 218 Patent provides no details concerning the disclosed “training sequences,” except that they are controlled by the memory module, a module may carry out more than one, and that they may be part of the module’s “initialization sequence.” EX1001, 3:28-31, 6:15-19; EX1003, ¶105.

During the 623 Patent IPR, the Board found Buchmann’s TS3 training operations satisfied the “training sequence” claimed in the 623 Patent. EX1034, 11-12. The TS3 operations are a set of operations carried out in a particular order to perform upstream lane training and repair. EX1016, 5:40-44. Indeed, Buchmann explicitly describes his different sets of training operations as “training sequences.” EX1016, 3:49-52, 14:38-41; EX1003, ¶106

Accordingly, the phrase “*training sequence*” should be construed to mean a set of operations occurring in a particular order and used for training. EX1003, ¶107.

## V. OVERVIEW OF THE PRIOR ART

### A. Hazelzet (EX1014)

U.S. Patent Publication No. 2008/0098277 to Hazelzet (“Hazelzet”) (EX1014) was filed on October 23, 2006 and published on April 24, 2008. Hazelzet is prior art under 35 U.S.C. §§102(a), (b), and (e).

Hazelzet discloses a system having multiple memory modules that operate in an “ECC mode” or a “parity mode.” EX1014, ¶¶[0064],[0069]-[0070]; EX1003, ¶109. Hazelzet explains that the “ECC mode” is a mode that allows the host system to detect and/or correct “correctable errors” or “uncorrectable errors.” EX1014, ¶[0069]. In ECC mode, the detected correctable errors are reported through an “/Error (CE)” output pin and uncorrectable errors are reported through an “/Error (UE)” output pin 121 (hereinafter “UE 121”). *Id.* Hazelzet explains that these two outputs are “open-drain outputs.” EX1014, ¶¶[0072],[0109]; EX1003, ¶110.

Hazelzet further explains that the “parity operating mode” allows the host system to “interrogate the device to determine the error condition” of the memory module. EX1014, ¶¶[0064],[0070]. In “parity mode” the “error condition” is

reported to the host “via the Uncorrectable Error (UE) line” (*i.e.*, UE 121), EX1014, ¶¶[0070],[0072],[0109]; EX1003, ¶¶111.

**B. JEDEC Proposal (EX1015)**

EX1015, entitled “LRDIMM DDR3 Memory Initialization Chapter Proposal” and referred to herein as “JEDEC,” is a proposal to the JEDEC JC-40.4 committee for ballot approval. EX1050, ¶7, Ex.A (also EX1015). As Julie Carlson, a former Manager of Standards and Publications at JEDEC, testifies, the JEDEC organization “maintains business records to document when standards are modified, balloted, and approved, and when its standards are published,” processes with which she is familiar given her twenty-three year association with the organization. EX1050, ¶¶1-3,6. Ms. Carlson testifies that JEDEC (a copy of which is attached to the Carlson Declaration, EX1050, Ex.A) is a true and correct copy of the LRDIMM DDR3 Memory Initialization Chapter Proposal. EX1050, ¶7.

Citing the JEDEC business records attached to her declaration, Ms. Carlson explains that on November 9, 2009 JEDEC “was approved by DDR3 MB TG (‘Task Group’) and referred to JC-40.4 to vote for ballot approval,” and that a letter ballot was distributed to the members of the relevant committee on November 11, 2009. EX1050 ¶7, Ex. B (also EX1051). Ms. Carlson explains that the letter ballot included a link to JEDEC, and therefore that the “Letter Ballot for

[JEDEC] itself distributes [JEDEC] to JC-40.4.’” *Id.* JEDEC was therefore distributed to the members of the JC-40.4 committee on November 11, 2009.

Ms Carlson also explains that the distribution of JEDEC on that date is confirmed by the tally of votes on that proposal recorded in the JEDEC organization’s files. In particular, Ms. Carlson attaches a printout from those files, showing that twenty-three of the most important companies in the field of computer memories voted on the proposal between November 13, 2009 and December 3, 2009. EX1050, ¶8, Ex.C, 21 (also EX1037). Ms. Carlson explains that “[t]hose companies include Advanced Micro Devices Inc. (AMD), Cray Inc., Dell Inc., Elpida Memory Inc., Hynix Semiconductor, IBM Corp., Inphi Corp., Integrated Device Technology Inc., Intel Corp, Kingston Technology Co. Inc., Legacy Electronics Inc., Micron Technology Inc., Netlist Inc., Nvidia Corp., NXP Semiconductors, Samsung Semiconductor, Silego Technology, Smart Modular Technologies, Inc., Sun Microsystems Inc., and Texas Instruments Inc.” EX1050, ¶¶8-9, Ex.C, 21-22. Thus, numerous interested members of the relevant public were directly provided JEDEC in November 2009.<sup>4</sup>

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<sup>4</sup> IDT, a member of the relevant committee, confirms that they received the ballot and proposal on or about November 11, 2009. EX1055, ¶7.



Ms. Carlson testifies that “the compilation of votes was generated on December 4, 2009, one day after the expiration date of the ballots” and that JEDEC maintains all vote tallies, such as Exhibit C, as business records, and it is the general practice of JEDEC employees and members to generate them at or around the time of the event they describe, and to keep them.” EX1050, ¶9, Ex. C, 1 (also EX1037).

Further, the members of the JC-40.4 committee to whom JEDEC was distributed were under no obligation to maintain that document as confidential when it was distributed. The relevant rules of the JEDEC organization in force at the time include no such obligation, though they specifically address how JEDEC documents are to be treated. EX1048, 19-20 (chapter on “JEDEC Documents”); EX1049 (same).

This is confirmed by the testimony of Dr. Halbert, who was involved with JEDEC standards processes during that period, contributed to several memory-related JEDEC standards, and was even given an award for his work. EX1054, ¶¶3, 6, 9-11. In addition to various other roles he played with the JEDEC organization, Dr. Halbert testifies that he has “received, reviewed, and voted on proposals regarding JEDEC standards.” EX1054, ¶9. He further testifies that, in his experience,

[T]here was no rule or other requirement that members treat ballots, technology presentations, or meeting minutes as confidential. Rather, these documents were freely disclosed and distributed within JEDEC's committees and subcommittees between JEDEC members manufacturing memory related products. JEDEC members are expected to discuss proposed technology, such as in ballots, technology presentations or meeting minutes, **within their company and among all third-parties interested in interoperability of memory related products.**

EX1054, ¶11. Thus, in November 2009, JEDEC was directly distributed to twenty-three of the largest and most important members of the interested public, with no obligation of confidentiality, and with the expectation it would be freely discussed with others, including parties who were not members of the JEDEC organization. JEDEC was therefore publically accessible as of November 11, 2009, or at least before June 13, 2010. *GoPro, Inc. v. Contour IP Holding LLC*, 908 F.3d 690, 694 (Fed.Cir. 2018).<sup>5</sup>

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<sup>5</sup> Moreover, Ms. Carlson also testifies that JEDEC membership is open to any company or organization, or one of its related entities, that manufactures electronic equipment or electronic-related products or related services, that the organization

JEDEC was therefore publically accessible by November 11, 2009, and at least before June 13, 2010. It is therefore prior art to the 218 Patent as a printed publication under 35 U.S.C. §102(a).

JEDEC discloses a proposed modification to the Memory Buffer functionality of a DDR3 LRDIMM memory module, the standards for which were being developed, to add the output of signals providing the status of certain training sequences. One disclosed training mode constituted MB-DRAM Training that entailed at least two training sequences, Write Leveling Training and Read Enable Training, both between the Memory Buffer and the DRAMs of the module. EX1015, 8 (§6.7). JEDEC also states that “[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete....” *Id.*; EX1003, ¶113.

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can be joined online, and that once a party joins it is given access JEDEC documents such as JEDEC and the other documents cited above. EX1050, ¶5. Thus, JEDEC was publically accessible as of November 11, 2009, or at least before June 13, 2010, in this additional way. *Constant v. Advanced Micro-Devices, Inc.*, 848 F.2d 1560, 1569 (Fed.Cir. 1988).

In the same description of MB-DRAM Training, JEDEC states that “training completion can be signaled by the assertion of ERROUT#.” *Id.*, 3, 8. A Skilled Artisan would understand that “ERROUT#” refers to the parity error out pin on a JEDEC standard LRDIMM module of the time, which was used to notify the memory controller of parity errors during normal operation, a pin referred to as ErrOut\_n in other JEDEC documents defining DDR3 LRDIMMs of the time. EX1036, 1, 4 (“Product Description”), 8 (penultimate entry in table on page re ErrOut\_n); EX1003, ¶¶114

**C. Buchmann (EX1016)**

U.S. Patent No. 8,139,430 to Buchmann (“Buchmann”), the application for which was filed on July 1, 2008, is prior art under 35 U.S.C. §102(e). EX1003, ¶116.

Buchmann discloses two modes of operation (*i.e.*, “SBC mode” and “high-speed mode”), EX1016, Abstract, 1:39-44; EX1003, ¶117, and also discloses executing training sequences in SBC mode. EX1016, 4:51-12:59; EX1003, ¶118.

As an example, training sequence TS0 involves “clock detection and repair,” EX1016, 5:51-53, which is training of the clock signal. EX1016, 5:66-6:50. During the TS0 training sequence, Buchmann’s memory module generates and outputs various notification signals to the memory controller of the host system, including the status of the TS0 training sequence (*e.g.*, “TS\_done,” which notifies

the host that the TS0 training is “done.”). EX1016, FIG. 4, 5:51-7:2. EX1003, ¶119.

As another example, training sequence TS3 involves “upstream lane training” and is “used to perform upstream data lane training.” EX1016, 8:24-47; EX1003, ¶120. During this sequence, the memory module generates and outputs notification signals to the system memory controller, including the status of the TS3 training sequence, such as “TS3\_ack,” which indicates that all downstream MBs have returned the TS3a\_ack SBC, and “TS\_done,” which notifies the host that the TS3 training sequence is “done.” EX1016, FIG. 6, 8:24-9:18; EX1003, ¶¶120.

Buchmann’s implementation involves a daisy chain arrangement among the various modules of his system, resulting in training sequence-complete signals from the memory module reaching the host only after all modules had completed the sequence. EX1016, 3:49-52, 14:41-43, 16:47-50, 28:23-26. However, Buchmann also explains that “one or more other bus structure(s) or a combination of bus structures” may be used, including “point-to-point bus(es),” “multi-drop bus(es),” and/or “other shared or parallel bus(es).” *Id.*, 28:26-31; EX1003, ¶122.

#### **D. The Combinations Relied on Here**

As Dr. Alpert explains, the combinations analyzed here – Hazelzet/JEDEC and Hazelzet/Buchmann – are exceedingly straightforward. In each, Hazelzet’s

memory modules would be modified to add a training mode (“*first mode/operation*”) into which each module could be switched and which includes training sequences and which reports completion of those training sequences by a status signal output over an open drain output (*i.e.*, UE 121) of Hazelzet. EX1003, ¶131.

In the JEDEC combination, the training sequences would be like those described as MB-DRAM Training in JEDEC (*e.g.*, Write Leveling and Read Enable Training), EX1015, 8, and the open drain output signal would be similar to the signal output on the ERROUT# pin as described in JEDEC, *id.*, 8; EX1036, 8 (is open-drain output for parity errors during normal operation). During those training sequences, the memory controller communicates no data with the module and performs no operations to read or write to the memory devices; the training is carried out by memory buffer (module controller) itself. EX1015, 8; EX1003, ¶132.

In the Buchmann combination, the training sequences would be like those described as TS0, EX1016, FIG. 4, 5:51-7:2, or alternatively, like those described as TS3, EX1016, FIG. 6, 8:24-9:18. The open drain output signals would be TS0\_done, in the former case, EX1016, FIG. 4, 5:51-7:2, and TS3\_ack or TS3\_done, in the latter case, EX1016, FIG. 6, 8:24-9:18. Buchmann does not disclose the memory controller communicating any data with the module or

performing operations to read or write to the memory devices during either TS0 or TS3 sequences. EX1003, ¶133.

In either combination, the circuitry of Hazelzet's module, in particular the ECC/Parity register, would be modified to implement the training as part of an additional mode to run, for example, at initialization, to switch among modes when appropriate, and to use the UE 121 open drain output of Hazelzet to communicate the new notification signals. EX1014, ¶[0123] (initialization operations); EX1015, 3 (training occurs during initialization); EX1016, 3:49-60 (same). As explained in more detail below, Hazelzet already uses his UE 121 open drain output for two different signals in two different modes. Thus, this ECC/Parity register necessarily includes circuitry for selecting which signal to drive on the UE 121 output depending on the mode of the module. It was well within the level of ordinary skill to modify such circuitry such that it instead selected among three different signals, depending on mode/operation, and a Skilled Artisan could have made that modification without undue experimentation and with a reasonable expectation of success. EX1003, ¶134.

Finally, these combinations would employ known open drain signaling circuitry, which necessarily included a field effect transistor having its source coupled to ground and its drain as the output. EX1017, FIGs 4&5. A Skilled Artisan would have known that in order to use open drain signaling to indicate

training completion among multiple modules, as here, the open drain output would have to be configured such that the transistor output is driven low (ground) while training is still occurring and driven high upon completion. This is because, with an open drain configuration shared by multiple modules, any module can individually drive the output low, but it takes the collective action of all connected modules to drive the output high. Moreover, a Skilled Artisan would also understand that to drive the output low (which would be a low impedance state), the gate of the transistor must be high, causing the transistor to conduct and connect the drain to ground. Conversely, to drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off. This is how an open drain output works. EX1014, ¶[0099]; EX1017, FIGs. 4-5, 5:65-6:18; EX1003, ¶135.

#### **E. Reasons to Combine**

The prior art relied on here is analogous to the 218 Patent because all are in the same field of invention – memory module design, including error detection and correction, initialization, training and the use of pins/paths for multiple purposes during different operations/modes, EX1001, Abstract, 5:66-6:14, 8:4-48; EX1014, Abstract, ¶¶[0007],[0069]-[0070],[0123]; EX1015, 1, 3, 8; EX1016, 1:7-9, 3:49-60, 4:51-5:50, 12:60-13:41, 14:1-63, 20:20-21:19, 33:45-67; EX1022, ¶¶[0004]-[0005],[0032]-[0033],[0052]; EX1025, 15-18; EX1027, 1:61-2:19, 6:24-25, 10:24-



45; EX1017, 1:16-22, 5:49-57, 6:8-18, 11:20-34, 12:36-53, and each is reasonably pertinent to the problem addressed by that patent – increasing memory module capacity, performance, and/or reliability by sharing an output pin/path to perform multiple functions during multiple operations/modes, including initialization/training, EX1001, Abstract, 5:66-6:14, 8:4-48; EX1014, Abstract, ¶¶[0007],[0069]-[0070],[0123]; EX1015, 1, 3, 8; EX1016, 1:7-9, 3:49-60, 4:51-5:50, 12:60-13:41, 14:1-63, 20:20-21:19, 33:45-67; EX1022, ¶¶[0004]-[0005],[0032]-[0033],[0052]; EX1025, 15-18; EX1027, 1:61-2:19, 6:24-25, 10:24-45; EX1017, 1:16-22, 5:49-57, 6:8-18, 11:20-34, 12:36-53. EX1003, ¶136.

Also, a Skilled Artisan would have considered each of the combinations analyzed here to be merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement. Combining the Hazelzet, JEDEC, Buchmann and Kim disclosures would have been well within the level of ordinary skill in the art, would not have resulted in any unpredictable results. EX1003, ¶137. A Skilled Artisan would have been motivated to make these combinations for at least the following reasons. EX1003, ¶138.

### **1. Motivation to Add Training**

Hazelzet emphasizes the need for “improved overall system reliability.” EX1014, ¶¶[0001]-[0004],[0007],[0042],[0044]. Given that emphasis, a Skilled

Artisan would have been motivated to add training to Hazelzet because it was known that training improved memory module reliability. EX1027, 1:35-2:12; EX1025, 15-18; EX1014, ¶[0123]; EX1017, 12:36-53; EX1003, ¶139.

Further, JEDEC explains that, during training, “[t]he MB performs ‘Write Leveling’ to the DRAMs **to ensure successful writes**, and ‘Read Enable Training’ **to ensure it can capture read data from the DRAMs correctly**, as part of the DRAM interface training,” and discloses that “MB DRAM interface training must be completed before any MB host interface read or write training **to ensure that the MB DRAM interface is configured optimally for DRAM reads and writes.**” EX1015, 3, 8-9. These statements would have motivated a Skilled Artisan to add training to systems such as Hazelzet to ensure optimal and correct operation. EX1003, ¶140.

Also, Buchmann discloses a “training phase that allows more flexibility and improved control data exchange during start-up,” *id.*, 3:64-67, to establish “reliable communication” on the bus, *id.* at 14:28-35, 14:5-8. A Skilled Artisan would have been motivated by these disclosures to look to systems such as JEDEC’s and Buchman’s to improve reliability. EX1003, ¶141.

## **2. Motivation to Add Training as a Mode Separate from Normal Operations**

As Dr. Alpert explains, a Skilled Artisan would have been motivated to combine these references by adding training in a mode/operation separate from

normal operation because it was known that training before normal operation was necessary to minimize errors, by “ensur[ing] successful writes,” and “ensur[ing] [the register on the DIMM] can capture read data from the DRAMs correctly.”

EX1015, 3, 8; EX1025, 15-18; EX1022, Fig. 4, ¶¶[0032],[0052],[0088-89];

EX1056, 18, 22, 25-26, 42-44, EX1057, Fig. 5, Abstract, 2:13-34, 2:60-3:3, 9:11-10:44. Likewise, Buchmann’s invention is an “initialization training sequence” completed at “power-on,” EX1016, Abstract, which would suggest to a Skilled Artisan that training before normal operation is important. EX1003, ¶142.

Because Hazelzet is initialized upon power-on, EX1014, ¶[0123]; EX1025, 15-18; EX1027, 1:61-2:19, 6:24-25, 10:24-45, JEDEC’s and Buchmann’s training that occurs at initialization would have complimented Hazelzet’s initialization, and a Skilled Artisan would have accordingly been motivated to combine these references such that the training mode occurred separate from normal operating modes/operations. EX1003, ¶143.

### **3. Motivation to Use Hazelzet’s Open Drain Signaling for Training Notifications**

It would have been further obvious to communicate training status in the new mode/operation using the same open drain output used in other modes/operations. EX1003, ¶¶144-146.

Hazelzet uses the same open drain output, UE 121, to indicate an “uncorrectable error” in ECC mode and parity error in parity mode, depending on

the mode. EX1014, FIGs. 4B, 7A, ¶¶[0044],[0049],[0059],[0064],[0069],[0072],[0109]; EX1003, ¶146. JEDEC also discloses using the same open drain output in two different modes, one for parity error and one for training status. EX1015, 8; EX1036, 8. These disclosures would have motivated a Skilled Artisan to use that same output in the added training mode/operation, particularly when the training mode/operation was implemented separate from, and before, the parity and ECC modes, as here, because those modes would not be using the open drain outputs while the training mode/operation was running during initialization. EX1003, ¶147.

A Skilled Artisan would also have been so motivated because such multiple use of a pin was known, and would have been considered an efficient use of the limited number of output pins on integrated circuits. For instance, Kim, EX1017, discloses additional details regarding the use of an open-drain output on a memory module during multiple modes, EX1017, 1:16-22, 5:49-57, 6:8-16, and discloses that, in addition to sharing ECC and parity on the error out pin, “[i]n alternate exemplary embodiments, other functions also share the error feedback pin,” *id.* at 6:16-18. EX1003, ¶148. As another example, Talbot discloses memory modules which use the same output to communicate error information during normal mode and training information during a training mode. EX1022, ¶¶[0004]-[0005],[0032]-[0033],[0052]. Such disclosures would have motivated a Skilled

Artisan to use Hazelzet's UE 121 open-drain output to notify the memory controller that the training was in progress or done. EX1003, ¶149.

Moreover, as Dr. Alpert explains, a Skilled Artisan would have been motivated to arrange the modified Hazelzet to communicate signals indicating training completion only when all memory modules have completed that training, in order to ensure that the entire memory system had been trained before proceeding to normal operation. This would permit training to be completed in an orderly and systematic manner, limiting the complexity of the control circuitry needed to implement the training, while using a known, efficient way to do so. *Id.*; EX1043, 7:30-51; EX1017, FIG. 4, 5:65-6:12; EX1014, ¶¶[0018],[0109]; EX1003, ¶150.

A Skilled Artisan would have been further motivated to modify Hazelzet as described above because Hazelzet's memory system includes multiple memory modules in need of training. EX1014, ¶¶[0018],[0109]; EX1017, FIG. 4, 5:65-6:12; EX1043, 7:30-51. The combinations analyzed here would therefore allow any module in the system to pull the open drain pin to “low” (*i.e.* to ground) while still executing its training sequence, regardless of whether other modules in the system have completed training and were no longer pulling that pin low, thereby delaying normal operations until the system is completely ready. *Id.*; EX1003, ¶151.

## VI. PRECISE REASONS FOR RELIEF REQUESTED

As set forth below, the combinations analyzed here – Hazelzet/JEDEC and Hazelzet/Buchmann – satisfy the claim elements set forth in the attached claim listing (**Attachment C**).<sup>6</sup> Additional grounds, building on and incorporating that basic combinations and addressing arguments Patent Owner may raise, are also included below.

Moreover, the Board’s Final Written Decision in IPR2018-00303, finding claims that are nearly identical to the 218 Patent claims unpatentable based on Hazelzet and Buchmann, is an adverse judgment precluding Patent Owner from taking action inconsistent with that judgment. 37 C.F.R. § 42.73(d)(3). Indeed, during prosecution of the 623 Patent, Patent Owner filed a terminal disclaimer with respect to patent application no., “15088115 filed on 04/01/2016,” the application from which the 218 Patent issued, EX1038, 79-80, thereby admitting the claims of the 218 Patent are not patentably distinct from the claims of the 623 Patent. As the Federal Circuit has explained, “[t]he purpose of [§ 42.73(d)(3)] is to ‘provide[ ] estoppel against claims that are patentably indistinct from those claims that were lost.’” *Arthrex, Inc. v. Smith & Nephew, Inc.*, 880 F.3d 1345, 1350 (Fed.Cir. 2018). Thus, Patent Owner should not even be heard to contest the arguments

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<sup>6</sup> Specific claim elements are identified in brackets below.

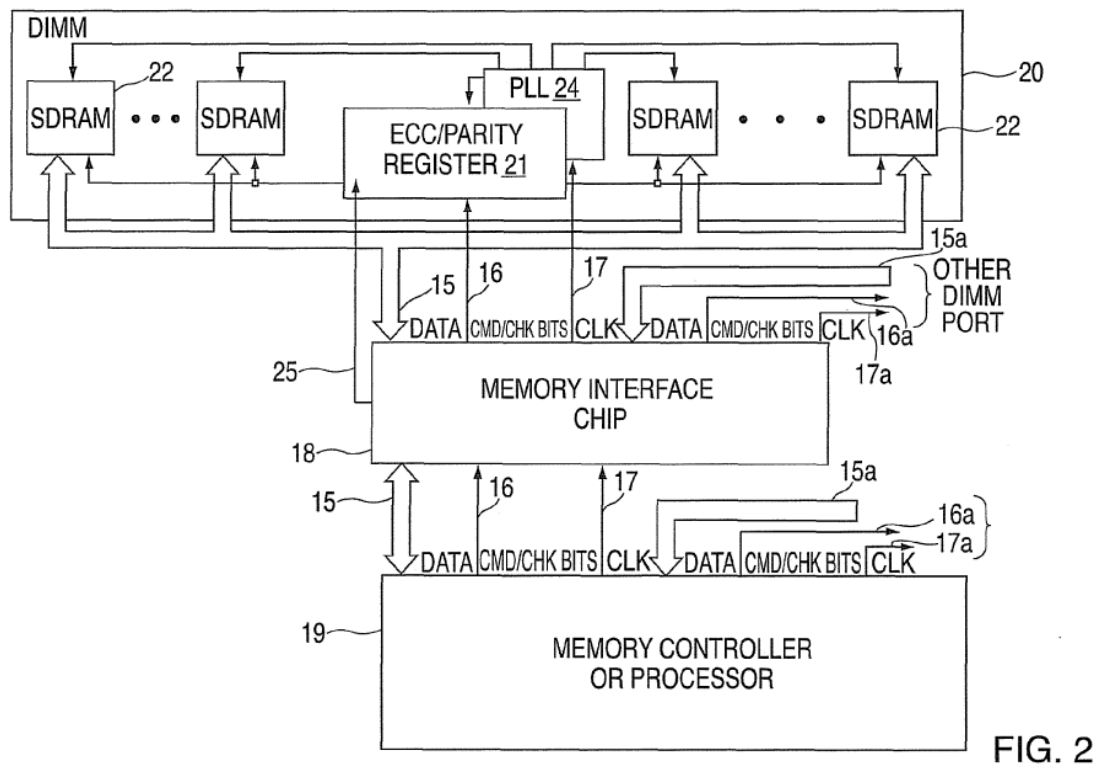
below, unless it can show that its positions are not inconsistent with the Board's decision in IPR2018-00303.

**A. Claims 1-22 Are Obvious Over Hazelzet In View Of JEDEC, or Buchmann**

**1. Claim 1**

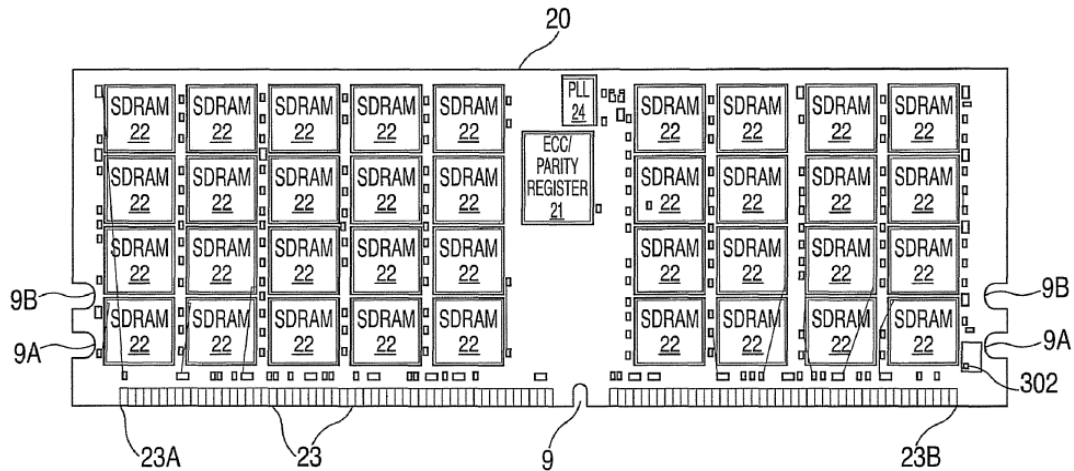
**a) [1.a] Preamble**

Hazelzet discloses dual inline memory modules (“DIMMs”) configured to operate with the “memory controller” of the host system. EX1014, FIGs. 2, 3A-3D, ¶¶[0036]-[0039]; EX1003, ¶154.



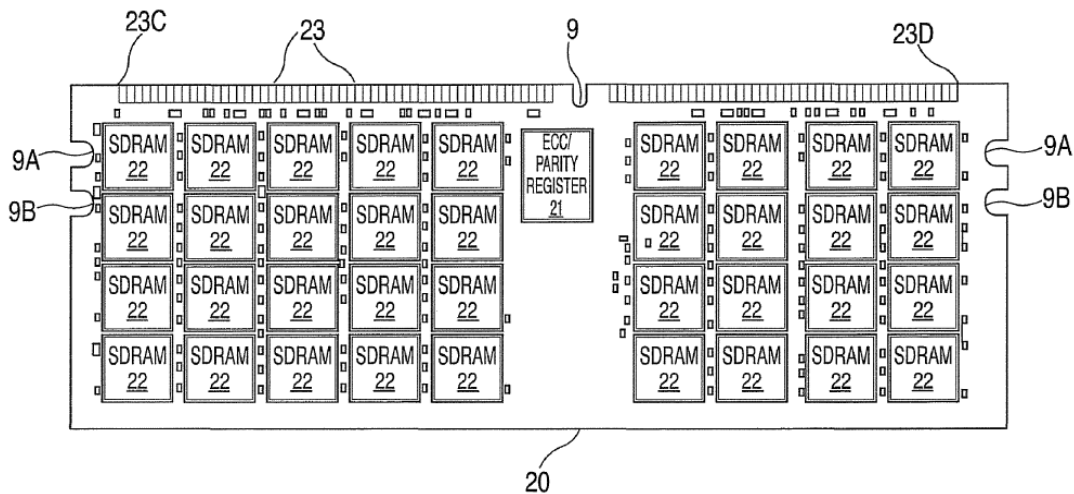
b) **[1.b] Printed Circuit Board**

Hazelzet explains the DIMM is “comprised of a printed circuit board having a front side and a back side.” EX1014, ¶[0015], FIGS. 2, 3A-3D, ¶¶[0037], [0039]; EX1003, ¶157.



FRONT SIDE OF DIMM - 72 PLANAR

FIG. 3A



BACK SIDE OF DIMM - 72 PLANAR

FIG. 3B



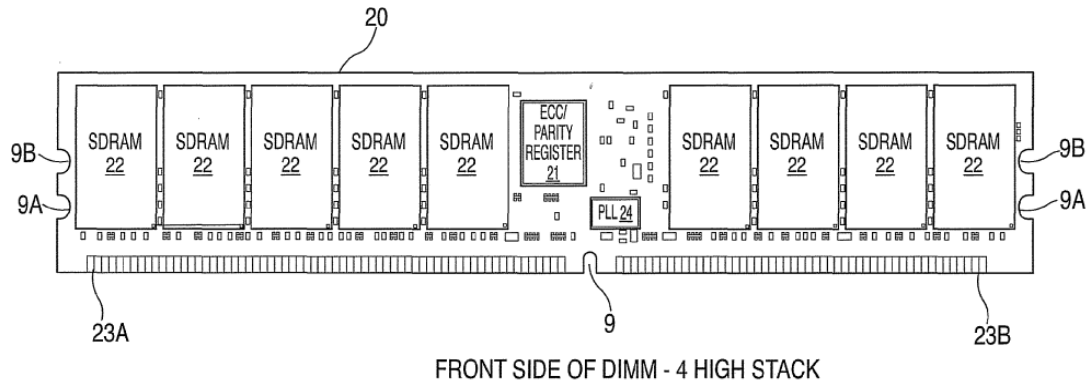


FIG. 3C

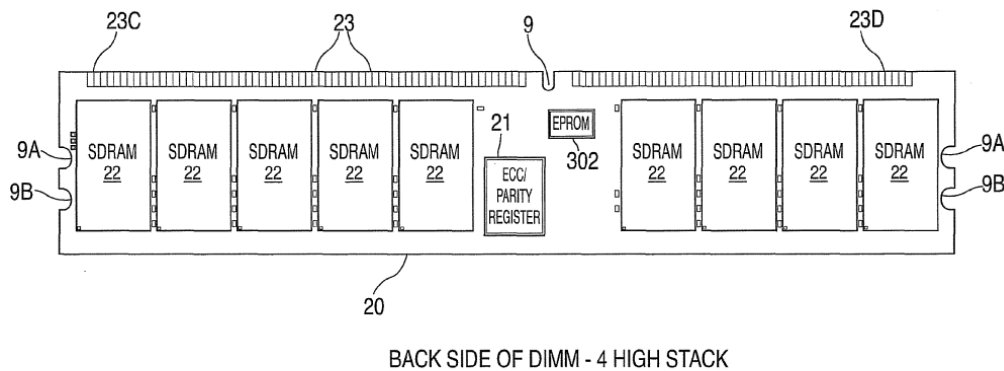
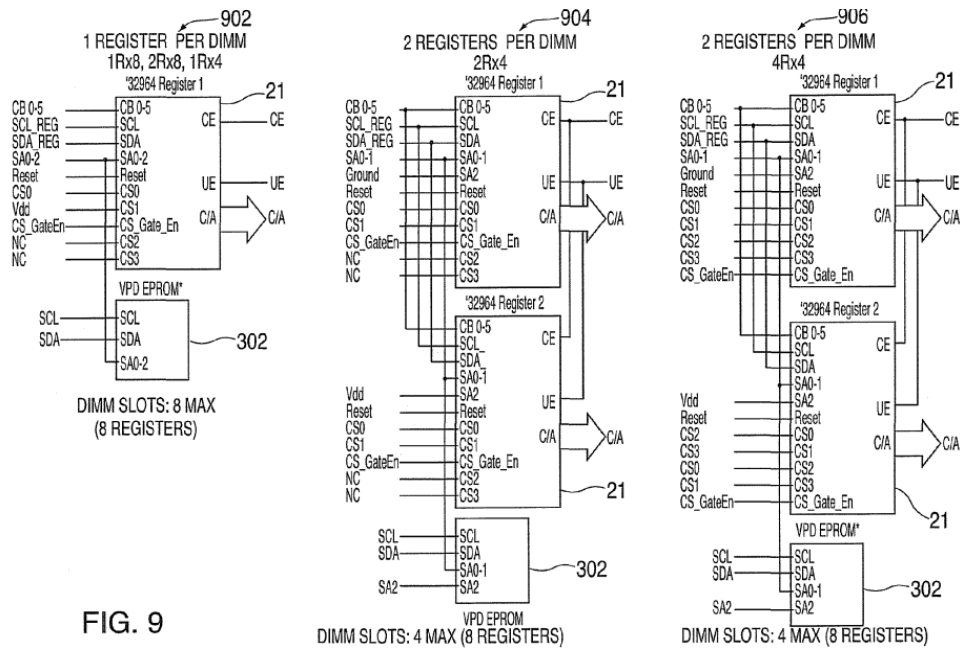


FIG. 3D

Hazelzet explains the memory modules include “connectors 23 along the edge of both the back and front sides,” which are provided to form connections to the memory controller when the module is inserted into a corresponding “slot” of the host system. EX1014, FIGs. 9, 11, ¶¶[0039],[0097]; EX1003, ¶158.



Hazelzet therefore discloses “a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller.” EX1003, ¶159.

Hazelzet discloses that the printed circuit board has a first set of edge connections for communicating data signals between the module and the memory controller, EX1014, FIGs. 7A-7C, ¶¶[0015],[0035],[0038],[0041]; EX1003, ¶160, and a second set of edge connections for communicating address and control signals from the memory controller, EX1014, FIGs 7A-7C, ¶¶[0015],[0035],[0038],[0041]; EX1003, ¶161. Hazelzet further discloses that the printed circuit board has an error edge connection coupled to the open drain output of the module controller. EX1014, FIGs 4B, 7A, ¶¶[0072],[0109]; EX1003, ¶162.

c) ***[1.c] DRAMs***

Hazelzet's memory module includes a plurality of "*DRAMs*" on the "*printed circuit board*," EX1014, ¶¶[0015], FIGs. 2, 3A-3D; EX1003, ¶165.

d) ***[1.d] Module Controller ... Having An Open Drain Output***

Hazelzet discloses an ECC/Parity register ("*module controller*") having an output for uncorrectable errors shown in FIG. 4B as "/ERROR (UE) 121" (*i.e.*, UE 121), which is an "*open drain output*." EX1014, FIGs. 3A-3D, 4A-4B, ¶¶[0044],[0059],[0072]. The ECC/Parity register is on the "*printed circuit board*" and coupled to the DRAMs. EX1014, FIGs. 3A-3D, ¶¶[0039],[0042]; EX1003, ¶168. The output UE 121 is "*coupled to the error edge connection*" of the module. EX1014, FIGs. 4B, 7A (pin 142), ¶¶[0059],[0072]; EX1003, ¶169-172.

e) ***[1.e] First Wherein Clause***

(1) ***[1.e.i] First and Second Modes / Operations in First Mode***

Hazelzet discloses the module is configurable to operate in (1) a "parity mode," which is the claimed "*second mode*," and (2) an "ECC mode." EX1014, FIG. 8, ¶¶[0064],[0069]-[0072]. As demonstrated above, §V.D, the combination of Hazelzet and JEDEC or, alternatively, Hazelzet and Buchmann, include a "*first mode*" in which training is carried out, and the combined module would be configurable to operate in either mode. EX1003, ¶174.

(2) ***[1.e.ii] Training Sequences***

As explained above, §V.D, the combinations analyzed here include a separate training mode (“*first mode*”) into which the module can be placed and in which the module can implement (“*configured to be trained*”) various training sequences (*e.g.*, Write Leveling and Read Enable Training per JEDEC/TS0 and TS3 per Buchmann) (“*with one or more training sequences*”). Each of those operations includes a set of operations occurring in a particular order, used for training the memory module. EX1015, 8; EX1039, 8-9; EX1016, FIGs. 4, 6, 5:51-7, 8:24-9:18; EX1040, 14:1-15:3; EX1018, Fig. 4; EX1003, ¶175.

*f) [1.f] Second Wherein Clause: Read or Write Not Associated with Training*

Hazelzet discloses that “as shown in this FIG. 2, the memory interface chip 18 sends and receives data from the DIMMs via the data line 15 and sends address and commands via line 16.” EX1014, ¶[0038]; FIG. 2. The figure shows line 15 coupling the memory controller and the DRAMs, and line 16 coupling the memory controller and the register 21. *Id.* A Skilled Artisan would understand from Figure 2 that lines 15 and 16 are coupled to edge connectors for data and address/control, respectively, since those lines couple the DIMM to the memory controller. EX1014, FIGs. 2, 7A-7B, ¶¶[0015],[0035],[0038],[0041]. Hazelzet therefore discloses that the module is configurable to receive address and control signals via the edge connections included on the module for that purpose. EX1003, ¶177.

A Skilled Artisan would also understand that such operations – communicating data with DRAMs while communicating address and command information with the register – to constitute “*one or more memory read or write operations*” because they follow the standard configuration for such operations with a JEDEC compliant device, EX1014, ¶[0044], including sending address and control to the register and data to the DRAMs. EX1024, 1, 14, 16; EX1003, ¶178.

Indeed, Hazelzet explains that its “parity mode” is an “operating mode,” EX1014, ¶¶[0064],[0070]; EX1003, ¶179, in which “the memory interface chip or controller would generate a single parity bit in conjunction with providing **the full address and command field to the module.**” EX1014, ¶[0075]; EX1003, ¶¶179-180. A Skilled Artisan would understand the use of the phrase “operating mode” and the phrase “full address and command field” in this context refers to the signals sent to a memory module during a memory read or write operation. *Id.*; EX1024, 1, 14, 16; EX1014, ¶[0038]. Moreover, Figure 8 of Hazelzet depicts a timing diagram used with his invention and explicitly discloses “Data In” and “Data Out” in parity mode, which movement of data is known to occur in the context of memory read and write operations. EX1014, FIG. 8. Hazelzet therefore discloses that the address and control signals received by the module over the address/control edge connections are “*configured to perform one or more memory read or write operations.*” EX1003, ¶181, 182.

Moreover, Hazelzet relates this configuration to both his ECC and parity mode, EX1014, ¶[0038], so a Skilled Artisan would understand these operations occur in parity mode (“*second mode*”). EX1003, ¶¶183-185.

To the extent one might argue that Hazelzet does not sufficiently disclose memory read and write operations in the parity mode, it would have been obvious to include that in the system of Hazelzet. The use of such operations in an operational mode employing parity checking was known in the prior art. EX1017, 6:19-34. Hazelzet describes how its “parity mode” is an “operating mode,” EX1014, ¶¶[0064],[0070], and discloses that in that mode the module is provided “the full address and command field,” EX1014, ¶[0075], suggesting the use of read and write operations that were known in the prior art, EX1024, 14, 16. A Skilled Artisan would have therefore been motivated to modify Hazelzet’s “parity mode” into the claimed “*second mode*” involving a read and write operations over the recited edge connections because to do so would have permitted memory operations using existing and convenient connections disclosed in Hazelzet and because it would have been common sense to do so. EX1024, 14, 16. This is confirmed by the passage’s reference to a third mode without ECC or parity where the register would simply be “operat[ing] the memory” which a Skilled Artisan would also understand to refer to the usual memory operations such as reading and writing. EX1014, ¶[0075]; EX1003, ¶187.

Further, as demonstrated above, §V.D, the combinations analyzed here include JEDEC or Buchmann training sequences in a training mode (“*first mode*”) separate from any mode that includes memory read and write operations in response to memory controller commands, thereby satisfying this limitation. Moreover, none of the portions of Hazelzet, JEDEC, and Buchmann relied upon for the combinations analyzed disclose training operations occurring during the memory read and write operations in response to memory controller commands, EX1003, ¶191, so their silence additionally satisfies this limitation. *Süd-Chemie, Inc. v. Multisorb Technologies, Inc.*, 554 F.3d 1001, 1004-05 (Fed. Cir. 2009).

*g) [1.g] Third Wherein Clause*

*(1) [1.g.i] Receive Address and Control Signals*

As explained for claim elements [1.b] and [1.f], Hazelzet’s module can be placed into a parity mode, which is a mode in which the module is provided, over the edge connections identified for that purpose, address and control signals for performing “*one or more memory read or write operations.*” EX1014, FIGs. 2, 7A-7B, ¶¶[0015],[0035],[0038],[0041],[0064],[0070]; EX1024, 13-14, 16; EX1003, ¶193.

*(2) [1.g.ii] Configured to Control*

As explained for claim elements [1.b] and [1.f], Hazelzet discloses that the printed circuit board has a first set of edge connections for communicating data

signals between the DRAM and the system memory controller, EX1014, FIGs 7A-7C, ¶¶[0015],[0035],[0038],[0041], while the memory module is in the “parity mode” and in accordance with the received address and control signals, *id.* at FIGs. 2, 8, ¶¶[0015],[0035],[0038],[0041],[0064],[0070]. Further, as explained in claim element [1.f], data communication between the memory module and the memory controller is “*in accordance with the address and command signals.*” EX1014, FIGs. 2, 7A-7C, 8, ¶¶[0015],[0035],[0038],[0041],[0064],[0070]; EX1024, 13; EX1003, ¶¶177-185, 194.

*h) [1.h] Fourth Wherein Clause: Output Parity Error*

As explained in claim elements [1.b.] and [1.d.], the error edge connection (pin 142) is coupled to the open drain output (UE 121) of the ECC/Parity register (“*module controller*”). EX1014, FIGs. 4B, 7A (pin 142), ¶¶[0059],[0072]; EX1003, ¶196. In particular, Hazelzet’s ECC/Parity register includes an “SEC/DED ECC” 90. EX1014, FIG. 4B. Figure 5 of Hazelzet, which is a block diagram of the “SEC/DED ECC” 90 in Figure 4B, includes a “parity generator/checker circuit 231.” EX1014, ¶¶[0028],[0076]; EX1003, ¶197. When the memory module is in the parity mode (“*second mode*”), the “parity generator/checker circuit 231” generates and sends the “parity error signal (PERR)” to the “error logic circuit” 100, EX1014, FIGs. 4-5, ¶¶[0070],[0076]; EX1003, ¶198, and outputs it to the memory controller through the output line UE



121, EX1014, ¶[0059]; EX1003, ¶199, which is an open-drain output, EX1014, ¶¶[0072], coupled to the memory controller using pin number 142, EX1014, FIG. 7A (pin 142), ¶¶[0038],[0070],[0072]; EX1003, ¶¶200-202.

*i) [1.i] Fifth Wherein Clause: Notification Signal*

As demonstrated above, §V.D, in the combinations analyzed here, the Hazelzet module would be modified to be configurable to enter a training mode and output JEDEC or Buchmann training status signals (“*notification signals*”) to the system memory controller via open drain output UE 121. *Id.* Each of the status signals analyzed above (ERROUT#, TS0\_done, TS3\_ack, TS3\_done,) are “*associated with the one or more training sequences*” because each provides status about the related sequences, such as whether it has been completed or whether all memory buffers have returned an acknowledgement. *Id.* Each of these combinations therefore alternatively satisfies “*wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences.*” EX1003, ¶¶205.

Moreover, Hazelzet’s memory system involves sharing the open drain output so that the memory controller can receive notification signals from multiple modules using the open drain output. EX1014, ¶¶[0018],[0072],[0109]; EX1003, ¶206. A Skilled Artisan would understand that, in this combination, the added training status signals would be at a low logic level (because the gate signals of the

transistors in the open drain circuits in all the modules in which the training is ongoing are high) over a Hazelzet open drain output (UE 121) until the related operations are completed for all modules of the system and the gate signals to the transistors of all the open drain circuits in all the modules are low, at which time the signals would be at a high impedance state, indicating completion. EX1017, FIG. 4; 5:65-6:12 (illustrating and describing how such a system as is in Hazelzet operates); EX1001, 9:47-10:50 (explaining in same way as Kim functioning of open-drain outputs in memory systems). The high and low gate signals to the transistors represent “*driv[ing] a notification signal...to the error edge connection via the open drain output while the memory module is in the first mode,*” respectively or vice versa. EX1003, ¶207.

## **2. Claims 2 and 16**

Hazelzet’s ECC/Parity register (“*module controller*”) “*comprises an integrated circuit.*” It is also referred to as a “buffer device” or a “buffer chip.” EX1014, ¶[0038]. Hazelzet explains that the module support devices, including “buffers”, “registers,” and “PLL’s” may be comprised of “multiple separate chips” or may be “combined onto a single package or even integrated onto a single device.” EX1014, ¶[0115], FIG. 3A-3D, ¶¶[0039],[0042]; EX1003, ¶¶209-211,311.

**3. Claims 3 and 17**

As explained in claim element [1.d.], Hazelzet discloses that the ECC/Parity register has “open drain output[s].” Hazelzet further explains that the ECC/Parity register has an “error correction code circuit ECC segment 21b,” which is a “*notification circuit*” because it outputs signals notifying the system memory controller of correctable, uncorrectable, and parity errors. EX1014, ¶[0044]. Such “error correction code circuit ECC segment 21b” (within the ECC/Parity register) includes the circuitry for determining whether the errors occurred, SEC/DED ECC circuit 90, and error logic circuit 100 that receives error signals from SEC/DED ECC circuit 90, such as UE 110 and PERR 111, and provides the above-mentioned “open-drain output(s),” such as UE 121. EX1014, FIG 4B, ¶¶[0059],[0072]; EX1003, ¶213.

As noted above, §V.D, the combinations analyzed here include, and a Skilled Artisan would understand an open drain output to necessarily include, a field effect transistor having gate, source, and drain. A Skilled Artisan would have also understood that the disclosed “open drain” output is an output of “*one or more transistors each having an open drain coupled to the open drain output*” while the source of that transistor is coupled to the ground. EX1017, FIGs. 4-5, 5:65-6:18; EX1020, Face (Title), 4:28-37; EX1003, ¶¶125-130, 214-216.

**4. Claims 4 and 18**

As demonstrated above, §V.D, in the combinations analyzed here the open drain output is configured such that the transistor output is driven low (ground) while training is still occurring and driven high upon completion. Moreover, to drive the output low (i.e., ground or “*provide a low impedance path*”), the gate of the transistor must be high, causing the transistor to conduct and connect the drain to ground. On the other hand, to drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off. EX1003, ¶¶233,234.

Thus, in the combinations analyzed here, the ECC/Parity register is configured (for example, by placing it in the training mode) “*to drive the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.,*” and thereby outputting “*notification signals.*” EX1003, ¶235.

**5. Claims 5, 11 and 19**

Hazelzet explains that its ECC/Parity register has “open-drain output[s]” capable of utilizing “parity error signals” (PERR) to output signal UE 121 to the host indicating a parity error. EX1014, ¶¶[0059],[0070],[0072],[0076]. Further, when the memory module is in the parity mode (“*second mode*”), the “parity generator/checker circuit 231” (within SEC/DED ECC circuit 90) generates and

sends the “parity error signal (PERR)” to the “error logic circuit” 100. EX1014, FIGs. 4B-5, ¶¶[0059],[0070],[0072],[0076]; EX1003, ¶239. Hazelzet explains that in the parity mode the parity error “will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses).” EX1014, ¶¶[0070],[0018]; EX1003, ¶240.

Further, as explained for claims 3-4, Hazelzet discloses that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (*i.e.*, gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” EX1014, ¶[0099]; EX1003, ¶241.

Accordingly, Hazelzet discloses that its “error correction code circuit ECC segment 21b” (“*notification circuit*”) driving the open-drain output UE 121 is configured “*to drive the parity error signal by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.*”. EX1017, FIGs. 4-5, 5:65-6:18; EX1003, ¶¶125-130,, 242-243,282,317.

## **6. Claims 6, 12 and 20**

Hazelzet’s “*notification circuit*” includes an “Error Logic 100,” EX1014, FIG. 4B, ¶¶[0044],[0059]; EX1003, ¶246; which receives the “US [sic] 110” signal and the “PERR 111” signal, and outputs one of these signals to the same “/ERROR

(UE)” pin depending on which mode the memory module is in. EX1014, FIG. 4B, ¶¶[0044],[0059],[0069-72]. In the combinations analyzed here, that circuitry would be modified to implement the additional training mode, in which the UE 121 open drain output would, when the module is in training mode, be used to send the notification/status signals identified above. EX1003, ¶¶134,246-247.

As Dr. Alpert explains, a Skilled Artisan would necessarily understand that the UE 121 open drain output is driven by a transistor in an open drain configuration, and that such a transistor necessarily has “*a gate*” that can be driven to assert the open drain output. EX1003, ¶248. Because in the combinations analyzed here Error Logic 100 receives “U[E] 110” signal and the “PERR 111” signal and the training mode notification signals, but uses only one such signal to drive the UE 121 output, depending on mode, a Skilled Artisan would also understand that Error Logic 100 would necessarily include “one or more OR logic elements,” such as a three-input OR gate, to determine which signal should be used to drive the transistor, thus the circuit would be “*configured to drive the notification signal using one or more OR logic elements.*” EX1017, FIGs. 4-5, 5:65-6:18 (depicting in FIG. 5 OR logic gate used for such purpose); EX1003, ¶¶249,284,319.

**7. Claim 7**

As Dr. Alpert explains, JEDEC discloses that during the MB-DRAM training, “[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low,” EX1015, 8. Accordingly, during such training the address/control pins would remain inactive as those are pins used to provide “DRAM commands or control word writes” and no data signals would be communicated on the data pins (“*first edge connections*”), so they would be inactive as well. *Id.*; EX1003, ¶¶253-254. That satisfies the limitations of claim 7.

Additionally, in a Buchmann combination, in which only the TS0 training operations are carried out in the training mode (“*first mode*”), the address/control and data pins (data pins are the “*first edge connections*”) of the module edge connections would not be active during that training because TS0 training involves training of the “clock” itself, and no address/control or data signals are transmitted between the host and the memory module during such training. EX1016, 5:51-7:2; EX1003, ¶¶255. That also satisfies the limitations of claim 7.

Moreover, neither Hazelzet nor JEDEC or Buchmann disclose address/control or data pins being active while the memory module is in a MB-DRAM Training or TS0 training mode during initialization/power-on. Because

these claims each recite a negative limitation, that silence also satisfies these claims. *Süd-Chemie, Inc. v. Multisorb Technologies, Inc.*, 554 F.3d 1001, 1004-05 (Fed.Cir. 2009). EX1003, ¶257.

To the extent one might argue otherwise, it would have been obvious not to send any data or address/control signals while the clock is being trained because a Skilled Artisan would have been motivated to keep the pin(s) for those signals inactive to conserve power and/or avoid unreliable operation during periods that the clock may be unstable. EX1003, ¶256.

#### **8. Claims 8, 14 and 22**

As demonstrated above, §V.D, in the combinations analyzed here, the Hazelzet module would be modified to be configurable to enter a training mode and output JEDEC or Buchmann training status signals (“*notification signals*”) to the system memory controller via open drain output UE 121. *Id.* Each of the status signals analyzed above (ERROUT#, TS0\_done, TS3\_ack, TS3\_done) “*indicate a status of the one or more training sequences*” because each provides status about the related sequences, such as whether it has been completed or whether all memory buffers have returned an acknowledgement. *Id.* Each of these combinations therefore alternatively satisfies “*wherein the module controller is configured to drive a notification signal indicating status of the one or more training sequences.*” EX1003, ¶¶260,289,323



**9. Claim 9**

***a) [9.a] Preamble***

This limitation is satisfied by the operation of the combined system analyzed in connection with claim [1.a].

***b) [9.b] DRAMs on PCB***

This limitation is satisfied for the reasons set forth for claim element [1.c].

***c) [9.c] Printed Circuit Board***

This limitation is satisfied for the reasons set forth for claim elements [1.b] (identifying PCB and edge connections) and [1.f] (explaining coupling of edge connections to DRAMs and module controller).

***d) [9.d] Receiving***

This limitation is satisfied for the reasons set forth for claim element [1.g]. Specifically, Hazelzet discloses memory operations that entail the module receiving address and control signals from a system memory controller via the respective address and control edge connections. EX1003, ¶269.

***e) [9.e] Controlling***

This limitation is satisfied for the reasons set forth for claim element [1.g]. Specifically, Hazelzet discloses memory operations that entail the module receiving address and control signals from a system memory controller via the respective address and control edge connections, and in response communicating

data between the system memory controller and the module DRAMs via the data edge connections under the control of the module controller. EX1003, ¶271.

***f) [9.f] Outputting***

This limitation is satisfied for the reasons set forth for claim element [1.h]. Hazelzet discloses the module outputting, in the “*second mode*,” a parity error signal via an open drain output (UE 121) in connection with memory read and write operations accessing the module. EX1003, ¶273.

***g) [9.g] Training***

This limitation is satisfied for the same reasons set for in claim elements [1.e.] (explaining training that occurs) and claim 7 (explaining that “first edge connections are not active” during that training). EX1003, ¶¶192-203, 275.

***h) [9.h] Driving***

This limitation is satisfied for the same reasons set forth in claim element [1.g]. Specifically, as demonstrated above, §V.D, the combinations analyzed here include a module that performs training sequence operations and outputs to the system memory controller training notification signals (*e.g.*, ERROUT#, TS0\_done, TS3\_ack, TS3\_done) via an open drain output (UE 121). EX1003, ¶277.

**10. Claim 10**

This claim is satisfied for the same reasons set for in claims 3 and 4. Specifically, the analysis above for claim 3 satisfies “*wherein driving the*

*notification signal comprises driving ... one or more transistors ... the one or more transistors each having an open drain coupled to the open drain output.”* The analysis above for claim 4 satisfies “*driving a gate of each of [the] one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground.*” EX1003, ¶279.

## **11. Claims 13 and 21**

In the combinations analyzed here, it would have been obvious to train the memory module with one or more training sequences that initiates in response to a request by the memory controller, given that JEDEC explains that, for MB-DRAM training, “the host triggers the DRAM interface training by setting the control bit DA4 in F0RC12,” EX1015, 8, and that Buchmann explains that “[t]he memory system includes a memory controller that includes logic for initiating ... initialization training sequence for the memory system,” EX1016, 1:56-59. Buchman further explains that “the memory buffer [in the memory module] includes logic for executing a power-on and initialization training sequence initiated by the memory controller.” EX1016, 2:39-42, 6:51-7:2, 8:24-29; EX1015, 3 (noting it provides “an overview of the power-up initialization of the Memory Buffer”); EX1003, ¶¶286,321.

## **12. Claim 15**

### ***a) [15.a] Preamble***

This limitation is satisfied for the reasons set forth in claim element [1.a].

***b) [15.b] Printed Circuit Board Having Edge Connections***

This limitation is satisfied for the reasons set forth for claim elements [1.b] (identifying PCB and edge connections) and [1.f] (explaining coupling of edge connections to DRAMs and module controller).

***c) [15.c] DRAMs***

This limitation is satisfied for the reasons set forth in claim elements [1.c.] (identifying DRAMs on PCB) and [1.f.] (explaining coupling of edge connections to DRAMs).

***d) [15.d] Module Controller ... Having An Open Drain Output***

This limitation is satisfied for the reasons set forth in claim element [1.d.].

***e) [15.e] A First Operation And A Second Operation***

This limitation is satisfied for the reasons set forth in claim elements [1.e.i]. The claimed “*first operation*” corresponds to the “*second mode*” of claim 1 and the claimed “*second operation*” corresponds to the “*first mode*” of claim 1.

***f) [15.f] First Wherein Clause***

***(1) [15.f.i] Receive Via Second Edge Connections***

This limitation is satisfied for the reasons set forth for claim element [1.g]. Specifically, Hazelzet discloses memory operations that entail the module receiving address and control signals from a system memory controller via the respective address and control edge connections. EX1003, ¶301.

**(2) [15.f.ii] Control the DRAM**

This limitation is satisfied for the reasons set forth for claim element [1.g]. Specifically, Hazelzet discloses memory operations that entail the module receiving address and control signals from a system memory controller via the respective address and control edge connections, and in response communicating data between the system memory controller and the module DRAMs via the data edge connections under the control of the module controller. EX1003, ¶303.

**g) [15.g] Second Wherein Clause: Output a Parity Error**

This limitation is satisfied for the reasons set forth for claim element [1.h]. Hazelzet discloses the module outputting, in the “*second mode*,” corresponding to the “first operation” in this claim, a parity error signal via an open drain output (UE 121) in connection with memory read and write operations accessing the module. EX1003, ¶305.

**h) [15.h] Third Wherein Clause: Trained**

This limitation is satisfied for the same reasons set for in claim elements [1.e.] (explaining training that occurs) and claim 7 (explaining that “first edge connections are not active” during that training. EX1003, ¶307.

**i) [15.i] Fourth Wherein Clause: Notification Signal**

This limitation is satisfied for the same reasons set forth in claim element [1.g]. Specifically, as demonstrated above, §V.D, the combinations analyzed here

include a module that performs training sequence operations and outputs to the system memory controller training notification signals (*e.g.*, ERRROUT#, TS0\_done, TS3\_ack, TS3\_done, TS3\_ack) via an open drain output (UE 121) of the module controller. EX1003, ¶309.

**B. Claims 3-6, 10-12, and 17-20 Are Obvious Over the Combinations Analyzed Above, And Kim**

To the extent one might argue that the Hazelzet/JEDEC or Hazelzet/Buchmann combinations do not satisfy the limitations in claims 3-6, 10-124, or 17-20, these claims would have been obvious in view of those combinations further combined with Kim.

Kim discloses an “open drain output” with an output pin coupled to the drain of a transistor, which includes a gate, a source, and a drain. EX1017, FIG. 4. FIG. 4 of Kim shows an open drain output coupled to a pull-up resistor (*i.e.*, connected to a high voltage via a pull-up resistor), the source of the transistor coupled to ground, and the gate coupled to “ERR.” EX1003, ¶217.

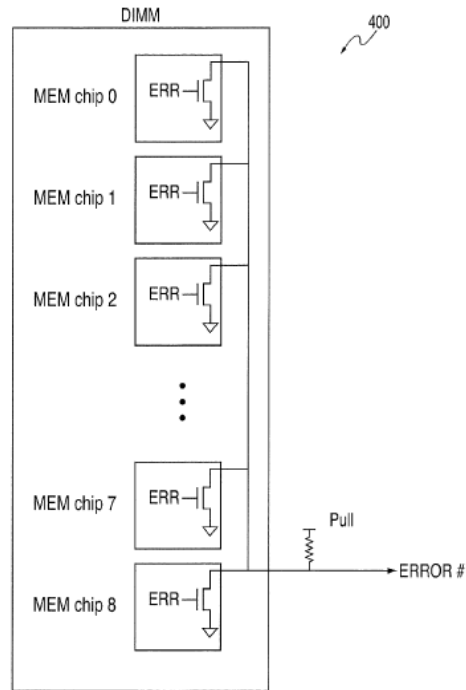


FIG. 4

Kim also discloses in Figure 5 using a logic element (an OR gate) such that multiple error signals could drive the gate of the open-drain transistor. EX1017, FIG. 5, 6:13-6:18.

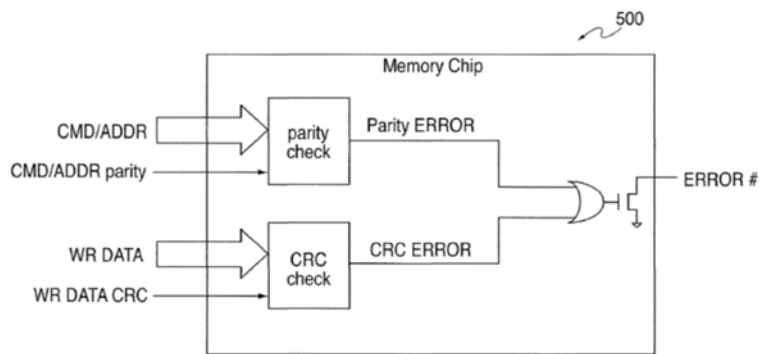
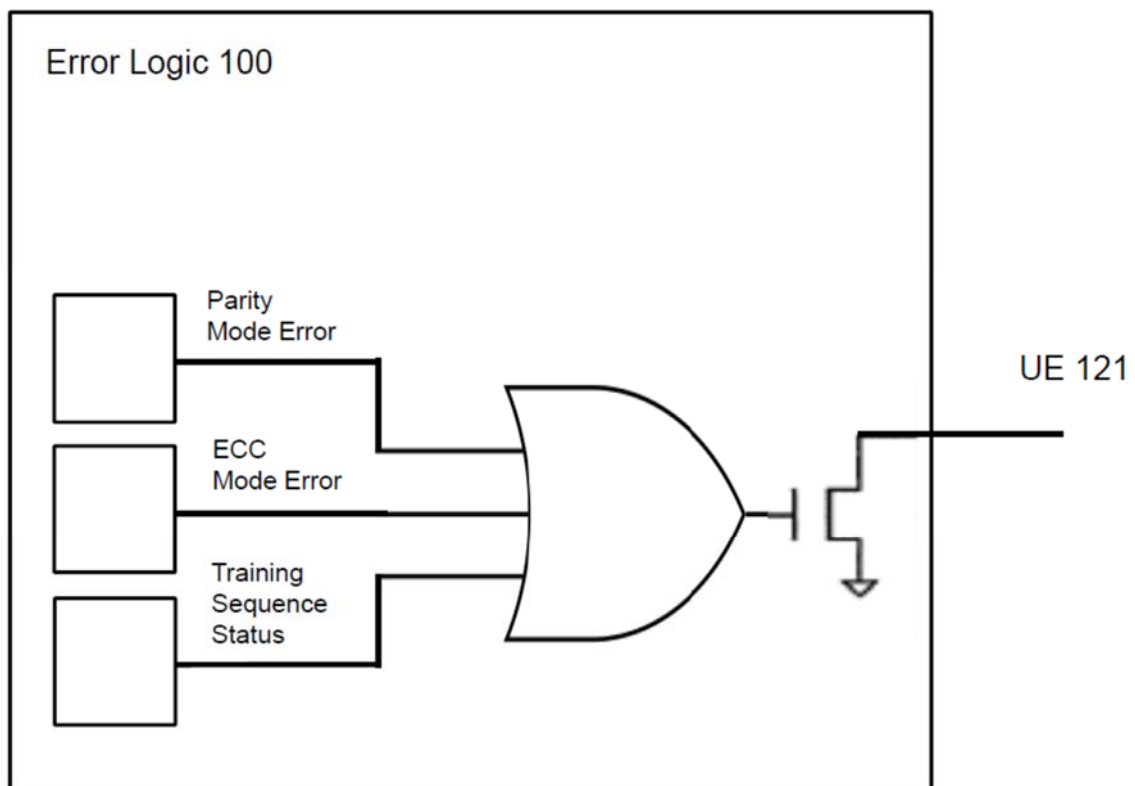


FIG. 5

EX1003, ¶218.

In the combinations analyzed here, Kim's open drain transistor configuration would be included within Hazelzet's error logic 100 (which is part of the ECC

segment 21b – a “*notification circuit*” as claimed) such that signals indicating parity mode error, ECC mode error and training status would be provided to a logic gate, such as an OR gate, as in Kim, which would select among them based on the mode of the module, as in Hazelzet. The output of the OR gate would be coupled to, and would drive, the gate of an open drain transistor, which itself drives UE 121, as shown in the annotation below:



EX1003, ¶219.

In this combination, each signal input to the OR gate would remain low when the module was not in its associated mode/operation, and the signal whose mode/operation was active could be high to indicate the occurrence of the event to



be signaled (error in Parity Mode or ECC Mode; ongoing training in Training Mode), or low to indicate that the event is not occurring (Parity/ECC) or acknowledged/completed (training). The signal whose mode was active would then be passed through the OR gate to drive the gate of the transistor. EX1003, ¶222.

As Dr. Alpert explains, *see* ¶¶223-224, a Skilled Artisan would have understood that an open drain output as set forth in the figure above would be pulled to a high logic level when the gate of the transistor is low, because the transistor would be off. EX1017 at FIG. 4. The output would then be in an undriven, high impedance, state. EX1014, ¶[0099]. On the other hand, the open drain output would switch to a low logic level (*e.g.*, ground), and be put in a low impedance state, when the gate of the transistor is high, because the transistor would be on. *Id.* EX1003, ¶225.

This combined circuit would therefore include the transistor configurations and signaling recited in claims 3-5, 10, and 17-19, EX1003, ¶215, and the OR logic elements as recited in claims 6, 12 and 20, EX1003, ¶251.

A Skilled Artisan would have been motivated to combine Kim into the obviousness combinations of Hazelzet and JEDEC or Buchmann. Kim is assigned to the same company as Hazelzet, includes some of the same disclosures, and discloses additional details regarding the use of an open-drain output to notify the

memory controller of errors during parity and ECC normal operating modes.

EX1017, 1:16-22, 5:49-57, 6:8-16. A Skilled Artisan would therefore have been motivated to consider them together. To use the output-pin scheme of Kim in the system of Hazelzet would also have been only the use of known techniques for their known purposes to achieve predictable results, i.e., using an open-drain output to provide error or status information from multiple components. EX1003, ¶227.

Kim and Hazelzet/JEDEC/Buchmann are analogous art to the 218 Patent for the reasons stated above. EX1003, ¶228; §V.E.

A Skilled Artisan would have been motivated to use the open-drain techniques of Kim in the combinations analyzed here because it represented a well-known (and therefore reliable) and simple technique to provide error and/or status information from a number of components and in different modes. EX1014, ¶¶ [0072],[0122]; EX1017, FIGs. 4-5, 5:65-6:18, 12:18-23; EX1003, ¶229.

The open-drain technique of Kim permitted a single signal line with an “*OR logic element*” to indicate error or status information, thus simplifying the design of the system and saving pins on the various integrated circuits connected to the bus, which necessarily can have only a finite number of pins. Thus, a person of ordinary skill in the art could readily have modified Hazelzet’s open-drain output

with the teachings of Kim and would have been motivated to do so. EX1003, ¶¶230-231.

## II. CONCLUSION

Petitioner therefore respectfully requests that Trial be instituted and that claims 1-22 be canceled as unpatentable.

Dated: June 8, 2020

Respectfully Submitted,

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Petition for *Inter Partes* Review of U.S. Patent No. 9,858,218

**PETITION FOR INTER PARTES REVIEW  
OF U.S. PATENT NO. 9,858,218**

**Attachment A:**

**Proof of Service of the Petition**

**CERTIFICATE OF COMPLIANCE**

I hereby certify that this brief complies with the type-volume limitations of 37 C.F.R. § 42.24, because it contains 13,714 words (as determined by the Microsoft Word word-processing system used to prepare the brief), excluding the parts of the brief exempted by 37 C.F.R. § 42.24.

Dated: June 8, 2020

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**CERTIFICATE OF SERVICE**

I hereby certify that on this 8th day of June, 2020, a copy of this Petition, including all attachments, appendices and exhibits, has been served in its entirety by overnight mail on the following counsel of record for patent owner:

Jamie J. Zheng, Ph.D., Esq.  
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**Attachment B:**

**List of Evidence and Exhibits Relied Upon in Petition**

Petition for *Inter Partes* Review of U.S. Patent No. 9,858,218

Exhibit #	Reference Name
1001	U.S. Patent No. 9,858,218
1002	File History of U.S. Patent No. 9,858,218
1003	Declaration of Donald Alpert
1004	Curriculum Vitae of Donald Alpert
1005	File History of U.S. Patent Application No. 15/857,553 ( <i>i.e.</i> , U.S. Patent No. 10,474,595)
1006	File History of U.S. Patent Application No. 13/942,721 ( <i>i.e.</i> , U.S. Patent No. 9,311,116)
1007	File History of U.S. Patent Application No. 12/815,339 ( <i>i.e.</i> , U.S. Patent No. 8,489,837)
1008	U.S. Provisional App. No. 61/186,799
1009	U.S. Patent Publication No. 2010/0042778 to Tanguay <i>et al.</i>
1010	U.S. Patent Publication No. 2003/0115427 to Roohparvar
1011	U.S. Patent Publication No. 2010/0202240 to Moshayedi <i>et al.</i>
1012	U.S. Patent Publication No. 2008/0256281 to Fahr <i>et al.</i>
1013	U.S. Patent Publication No. 2010/0142383 to Goishi <i>et al.</i>
1014	U.S. Patent Publication No. 2008/0098277 to <u>Hazelzet</u>
1015	JEDEC COMMITTEE LETTER BALLOT, LRDIMM DDR3 Memory Initialization Chapter Proposal (Dec. 2009) (“JEDEC”)
1016	U.S. Patent No. 8,139,430 to <u>Buchmann</u> <i>et al.</i>
1017	U.S. Patent No. 8,359,521 to <u>Kim</u> <i>et al.</i>
1018	U.S. Patent No. 8,407,441 to Giovannini <i>et al.</i>
1019	U.S. Patent No. 8,489,837 to Lee



Petition for *Inter Partes* Review of U.S. Patent No. 9,858,218

Exhibit #	Reference Name
1020	U.S. Patent No. 3,414,781 to Dill
1021	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Exhibit 1021, (PTAB December 11, 2017) (Deposition of Robert J. Murphy in 837 Patent IPR)
1022	U.S. Patent Application Pub. 2008/0147897 to Talbot
1023	U.S. Patent Application Pub. 2008/0155378 to Amidi
1024	JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) (“JESD79”)
1025	JEDEC Standard, FBDIMM: Architecture and Protocol (January 2007) (“JESD206”)
1026	JEDEC Standard, FBDIMM Advanced Memory Buffer (AMB) (March 2007)(“JESD82-20A”)
1027	U.S. Patent No. 7,411,862 to Hein et al.
1028	Chan, Melissa, ‘ <i>It Will Have Effects for Months and Years.</i> ’ <i>From Jury Duty to Trials, Coronavirus is Wreaking Havoc on Courts</i> , Time (March 16, 2020) <a href="https://time.com/5803037/coronavirus-courts-jury-duty/">https://time.com/5803037/coronavirus-courts-jury-duty/</a>
1029	JEDEC Standard, Low Power Double Data Rate (LPDDR) SDRAM Specification (August 2007) (“JESD209”)
1030	<a href="https://compass.docketnavigator.com/patent/binder/0/0">https://compass.docketnavigator.com/patent/binder/0/0</a> (Time to Trial for W.D. Tex. Patent cases since 2008)
1031	U.S. Patent No. 9,535,623 (623 Patent)
1032	<i>SK hynix, Inc. et al. v. Netlist, Inc.</i> , IPR2018-00303, Paper No. 1 (PTAB December 14, 2017) (623 Patent IPR Petition)
1033	<i>SK hynix, Inc. et al. v. Netlist, Inc.</i> , IPR2018-00303, Exhibit 1003 (PTAB December 14, 2017) (Alpert Declaration in 623 Patent IPR)

Petition for *Inter Partes* Review of U.S. Patent No. 9,858,218

Exhibit #	Reference Name
1034	<i>SK hynix, Inc. et al. v. Netlist, Inc.</i> , IPR2018-00303, Paper No. 42 (PTAB March 21, 2019) (623 Patent Final Written Decision)
1035	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Paper No. 25 (PTAB May 3, 2018) (837 Patent Final Written Decision)
1036	JEDEC COMMITTEE LETTER BALLOT, DDR3 LRDIMM Design Specification Body (Dec. 2009)
1037	JEDEC, Compilation of Tallies for JC-40 CMOS Digital Logic and point committees (Dec. 4, 2009)
1038	File History of U.S. Patent Application No. 15/169,745 (i.e., U.S. Patent No. 9,535,623)
1039	Inphi Corporation, “MB Initialization sequence Item 142.35,” June 4, 2009
1040	U.S. Patent No. 8,386,737 to Jeon et al.
1041	<i>SK hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Paper 14 (PTAB December 11, 2017).
1042	“Sequence,” <a href="https://www.lexico.com/en/definition/sequence">https://www.lexico.com/en/definition/sequence</a>
1043	U.S. Patent No. 7,222,213 to James
1044	“28-Bit to 56-Bit Registered Buffer with Address Parity Test One Pair to Four Pair Differential Clock PLL Driver” Texas Instruments (October 2008)
1045	“High-Speed DRAM Controller Design” Micron (2008)
1046	“Minutes of Meeting No. 158 JC-40 Digital Logic Committee” JEDEC (June 4, 2009)
1047	<i>SK Hynix Inc. et al. v. Netlist, Inc.</i> , IPR2017-00548, Exhibit 2009, (PTAB September 6, 2017)

Petition for *Inter Partes* Review of U.S. Patent No. 9,858,218

<b>Exhibit #</b>	<b>Reference Name</b>
1048	JEDEC, JEDEC Manual of Organization and Procedure, JM21P (Rev. of JM21N, May, 2008), (May, 2010)
1049	JEDEC, JEDEC Manual of Organization and Procedure, JM21N (Rev. of JM21M, December, 2006), (May, 2008)
1050	Declaration of Julie Carlson
1051	JEDEC, “Committee Letter Ballot, JC-40.4-09-320, Item 142.35,” (Dec. 2009)
1052	JEDEC, “Committee Letter Ballot, JC-45.4-09-321, Item 2192.44,” (Dec. 2009)
1053	JEDEC, “Tally of Votes, Committee Letter Ballot, JC-45.4-09-321, 2192.44” (Dec. 9, 2009)
1054	Declaration of John Halbert
1055	Declaration of Roland Knaack
1056	JEDEC Stanard, DDR3 SDRAM, JESD79-3C (November 2008) (“JESD79-3C”)
1057	U.S. Patent No. 7,647,467 to Hutsell et al.

**PETITION FOR INTER PARTES REVIEW  
OF U.S. PATENT NO. 9,858,218**

**Attachment C:  
Listing of The Claims of 9,858,218**

Claim	Claim Language
1.a	1. A memory module operable with a memory controller of a host system, comprising:
1.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;
1.c	dynamic random access memory elements on the printed circuit board;
1.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and
1.e	[i] wherein the memory module is operable in at least a first mode and a second mode,  [ii] wherein the memory module in the first mode is configured to be trained with one or more training sequences;
1.f	wherein the memory module in the second mode is configured to perform one or more memory read or write operations not

Claim	Claim Language
	associated with the one or more training sequences by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections;
1.g	<p>[i] wherein the module controller is configured to receive via the second edge connections the address and command signals associated with the one or more memory read or write operations and</p> <p>[ii] to control the dynamic random access memory elements in accordance with the address and command signals, and</p>
1.h	wherein the module controller is further configured to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the second mode;
1.i	wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output while the memory module is in the first mode.
2	2. The memory module of claim 1, wherein the module controller comprises an integrated circuit.

Claim	Claim Language
3	3. The memory module of claim 1, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.
4	4. The memory module of claim 3, wherein the notification circuit is configured to drive the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
5	5. The memory module of claim 4, wherein the notification circuit is configured to drive the parity error signal by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
6	6. The memory module of claim 4, wherein the notification circuit is configured to drive the notification signal using one or more OR logic elements.
7	7. The memory module of claim 1, wherein the first edge connections are not active when the memory module is in the first mode and configured to be trained with the one or more training sequences.

Claim	Claim Language
8	8. The memory module of claim 1, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences.
9.a	9. A method performed by a memory module operating with a memory controller of the host system,
9.b	the memory module including dynamic random access memory elements on a printed circuit board,
9.c	the printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections via which the dynamic random access memory devices communicate data with the memory controller, second edge connections via which the memory module receives address and command signals from the memory controller, and an error edge connection in addition to the first edge connections and the second edge connections, the method comprising:
9.d	receiving from the memory controller address and command signals associated with one or more memory read or write operations;
9.e	controlling the dynamic random access memory elements in accordance with the address and command signals;



Claim	Claim Language
9.f	outputting to the memory controller via an open-drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module; and
9.g	training with one or more training sequences while the first edge connections are not active, and
9.h	driving a notification signal associated with the one or more training sequences to the memory controller via the open drain output and the error edge connection.
10	10. The method of claim 9, wherein driving the notification signal comprises driving a gate of each of one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground, the one or more transistors each having an open drain coupled to the open drain output.
11	11. The method of claim 10, wherein driving the signal indicating the parity error comprises driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground.
12	12. The method of claim 10, wherein driving the notification signal comprises using one or more OR logic elements.

Claim	Claim Language
13	13. The method of claim 9, wherein the memory module is configured to be trained with the one or more training sequences in response to a request by the memory controller.
14	14. The method of claim 9, wherein the notification signal indicates a status of the one or more training sequences.
15.a	15. A memory module operable with a memory controller of a host system, comprising:
15.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and command signals, and an error edge connection in addition to the first edge connections and the second edge connections;

Claim	Claim Language
15.c	dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the first edge connections; and
15.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection;
15.e	wherein the memory module is configurable to perform at least a first operation and a second operation;
15.f	<p>[i] wherein the module controller in the first operation is configured to receive via the second edge connections address and command signals associated with one or more memory read or write operations and</p> <p>[ii] to control the dynamic random access memory elements in accordance with the address and command signals,</p>
15.g	wherein the module controller in the first operation is further configured to output to the memory controller a signal indicating a parity error having occurred in the memory module; and

Claim	Claim Language
15.h	wherein the memory module in the second operation is configured to be trained with one or more training sequences while the first edge connections are not active, and
15.i	wherein the module controller in the second operation is configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output of the module controller.
16	16. The memory module of claim 15, wherein the module controller comprises an integrated circuit.
17	17. The memory module of claim 15, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.
18	18. The memory module of claim 17, wherein the notification circuit is configured to generate the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
19	19. The memory module of claim 18, wherein the notification circuit is configured to drive the signal indicating the parity error by

Claim	Claim Language
	driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
20.	20. The memory module of claim 18, wherein the notification circuit is configured to drive the notification signal using one or more OR logic elements.
21	21. The memory module of claim 15, wherein the memory module is configured to perform the second operation in response to a command from the memory controller.
22	22. The memory module of claim 15, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences.