

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC. and SK HYNIX AMERICA INC.,
Petitioners,

v.

NETLIST, INC.
Patent Owner.

Case No. IPR2020-01044
U.S. Patent No. 9,858,218

**PATENT OWNER'S RESPONSE
UNDER 37 C.F.R. §42.120**

TABLE OF CONTENTS

I.	Introduction.....	1
II.	Identification of Claims Being Challenged	1
III.	Relevant Information Concerning the '218 Patent.....	2
A.	The Correct Priority Date of the '218 Patent is June 12, 2009	2
1.	The Petition Applies the Wrong Legal Standard	2
2.	The '218 Patent Claims Reciting That the First Edge Connections Are not Active Are Supported By the Priority Application	4
a.	The priority application provides written description support for this claim	5
3.	The Provisional Application Supports the '218 Patent Claims Reciting Performance of One or More Memory Read or Write Operations Not Associated With the One or More Training Sequences	8
a.	The priority application provides written description support for this claim	8
b.	Petitioners and Petitioners' expert corroborate that written description support exists for this claim	10
4.	The Provisional Application Supports the '218 Patent Claims Reciting "One or More" Training "Sequences"	11
B.	General Overview of the '218 Patent.....	13
IV.	Overview of the References	14
A.	Hazelzet	14
B.	Buchmann.....	15
C.	JEDEC	15

V.	Grounds 1-3 Fail for Numerous, Reasons	16
A.	Ground 1 Fails Because Petitioners Have Failed to Demonstrate that JEDEC is Prior Art.....	18
1.	Petitioners fail to show that distributing JEDEC to committee members rendered the reference publicly available	19
a.	Petitioners fail to show that documents available on the JEDEC website were in fact available to anyone not already a participant in JEDEC.....	19
b.	Petitioners fail to identify evidence that a person of skill and interest in the art could reasonably be expected to find the JEDEC reference in the JEDEC repository.	23
2.	Petitioners fail to show that the absence of confidentiality provision and that there was an expectation to distribute JEDEC to others rendered the reference publicly available	26
B.	Grounds 1-3 Fail Because There is No Motivation to Add Buchmann’s or JEDEC’s Alleged Training to Hazelzet.....	27
1.	Problem and Solution Taught in Hazelzet	27
2.	General Overview of ECC	29
3.	General Overview of Training	31
4.	General Differences Between ECC and Training.....	33
5.	There is No Motivation to Add Buchmann’s or JEDEC’s Alleged Training to Hazelzet for Multiple Reasons	34
a.	Petitioners’ Motivation to Combine is Conclusory and Logically Inconsistent.....	34
b.	Petitioners’ Motivation to Combine is the Result of Impermissible Hindsight.....	37

c.	Petitioners’ Motivation to Combine is Based on What a POSITA Could Have Done; Not what a POSITA Would Have Done	40
d.	Hazelzet, Buchmann and JEDEC Disclose Teachings that Diverge from One Another	42
C.	There is No Motivation to Create a Separate Training Mode in Hazelzet	43
D.	There is No Motivation to Use Hazelzet’s Open Drain Signaling Training Notifications	46
E.	Claims 1-22 are not obvious over Hazelzet in view of Buchmann for Additional Reasons	49
F.	Claims 1-22 are not obvious over Hazelzet in view of JEDEC for Additional Reasons	52
VI.	Conclusion	55

TABLE OF AUTHORITIES

	Page(s)
Cases	
<i>Ariad Pharm., Inc. v. Eli Lilly & Co.</i> , 598 F.3d 1336, 1351 (Fed. Cir. 2010)	3
<i>Arris Int’l PLC v. Sony Corp.</i> , IPR2016-00828, Paper 10 at 15-16 (PTAB Oct. 7, 2016).....	36
<i>ATD Corp. v. Lydall, Inc.</i> , 159 F.3d 534,546 (Fed. Cir. 1998)	39
<i>Black & Decker, Inc. v. Positec USA, Inc.</i> , 646 Fed. Appx. 1019, 1027 (Fed. Cir. 2016).....	41, 45
<i>Blue Calypso, LLC v. Groupon, Inc.</i> , 815 F.3d 1331, 1349 (Fed. Cir. 2016)	20, 22
<i>Cardiac Pacemakers, Inc. v. St. Jude Medical, Inc.</i> , 381 F.3d 1371 (Fed. Cir. 2004)	36
<i>Contrast Medtronic, Inc., v. AGA Medical Corp.</i> , 618 F.Supp.2d 1191, 1193 (N.D. Cal., April 28, 2009)	21
<i>Costco Wholesale Corp. v. Robert Bosch LLC</i> , IPR2016-00035, Paper 23 at 8.....	41
<i>DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.</i> , 567 F.3d 1314, 1326 (Fed. Cir. 2009)	42, 52
<i>EnOcean GmbH v. Face Int’l Corp.</i> , 742 F.3d 955, 960 (Fed. Cir. 2014)	3
<i>Ex parte Parks</i> , 30 USPQ2d 1234, 1236 (Bd. Pat. App. & Inter. 1993)	4
<i>Front Row Techs. v. MLB Advanced Media, L.P.</i> , IPR2015-01932, Paper 7 at 17 (PTAB Mar. 25, 2016). (Ex. 2032 at ¶ 71)	36

<i>Graham v. John Deere Co. of Kan. City</i> , 383 U.S. 1, 36 (1966). (Ex. 2032 at ¶ 72).....	37
<i>In re Enhanced Security Research, LLC</i> , 739 F.3d 1347, 1355 (Fed. Cir. 2014)	39
<i>In re Fine</i> , 837 F.2d 1071,1075 (Fed. Cir. 1988)	39
<i>In re Gorman</i> , 983 F.2d 982, 987 (Fed. Cir. 1991)	39
<i>In re Gurley</i> , 27 F.2d 551, 553, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994)	42, 52
<i>In re Ratti</i> , 270 F.2d 810, 813 (CCPA 1959)	46
<i>Inphi Corp. v. Netlist, Inc.</i> , 805 F.3d 1350, 1356 (Fed. Cir. 2015)	4, 8
<i>Kao Corp. v. Unilever United States, Inc.</i> , 441 F.3d 963 (Fed. Cir. 2006)	3
<i>KSR Int'l Co. v. Teleflex Inc.</i> , 550 U.S. 538, 416, 82 USPQ2d 1385, 1395 (2007)	35, 40, 46
<i>Mobilemedia Ideas LLC v. Apple Inc.</i> , 780 F.3d 1159, 1172 (Fed. Cir. 2015)	37
<i>Pandrol USA, LP v. Airboss Ry. Prods.</i> , 424 F.3d 1161, 1165 (Fed. Cir. 2005)	3
<i>Samsung Elecs. Co. v. Infobridge Pte. Ltd.</i> , 929 F.3d 1363, 1370-73 (Fed. Cir. 2019).....	20, 22
<i>Samsung Electronics Co. Ltd. v. Rembrandt Wireless Technologies</i> , <i>LP</i> , IPR2014-00514, Paper 18, at 4 (P.T.A.B. Sept. 9, 2014).....	19, 20, 21
<i>Seabery N. Am., Inc. v. Lincoln, Global, Inc.</i> , IPR2016-00904, Paper 12 at 11-12	41

<i>SRI International, Inc. v. Internet Security Systems, Inc.</i> , 511 F.3d 1186, 1194 (2008).....	<i>passim</i>
<i>TQ Delta, LLC v. Cisco Sys.</i> , 942 F.3d 1352, 1359 (Fed. Cir. 2019)	37, 40
<i>Van Os</i> 844 F.3d at 1361	35, 40

Statutes and Rules

U.S.C § 102(a)	27
35 U.S. C. § 103.....	2, 46
35 U.S.C. § 311(b)	18

TABLE OF EXHIBITS

Exhibit	Description
2001	Scheduling Order, <i>Netlist, Inc. v. SK hynix Inc. and SK hynix America Inc.</i> , Civil No. 6:20-cv-00194-ADA (W.D. Tex, Jul. 8, 2020), ECF No. 46
2002	Order Setting Markman Hearing, <i>Netlist, Inc. v. SK hynix Inc. and SK hynix America Inc.</i> , Civil No. 6:20-cv-00194-ADA (W.D. Tex. Jun. 26, 2020), ECF No. 41.
2003	Jointly Proposed Scheduling Order, <i>Netlist, Inc. v. SK hynix Inc. and SK hynix America Inc.</i> , Civil No. 6:20-cv-00194-ADA (W.D. Tex. Jul. 6, 2020), ECF No. 045-1.
2004	Order Denying Motion to Stay Pending IPR, <i>Multimedia Content Management v. Dish Network</i> , Civil No. 6:18-CV-00207 (W.D. Tex. May 30, 2019) (J. Albright).
2005	Claim Construction Order, <i>STC.UNM v. Apple Inc.</i> , Civil No. 1:20-cv-00351-ADA (W.D. Tex. Jun 8, 2020).
2006	Claim Construction Order, <i>Uniloc 2017 LLC v. Apple Inc.</i> , Civil No. 6:19-cv-00532-ADA (W.D. Tex. Jun 8, 2020).
2007	Claim Construction Order, <i>MV3 Partners LLC v. Roku Inc.</i> , Civil No. 6:18-cv-00308-ADA (W.D. Tex. Oct. 19, 2019).
2008	Docket Report, <i>Diamondback Industries, Inc. v. Repeat Precision, LLC, et al</i> , Civil No. 6:19-cv-00034-ADA (W.D. Tex. Sep. 16, 2020).
2009	Exhibit A1 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020.
2010	Exhibit A21 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020.
2011	Exhibit A19 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020.
2012	Exhibit A36 of SK hynix's Invalidity Contentions, dated Aug. 7, 2020.
2013	SK hynix's Invalidity Contentions, dated Aug. 7, 2020.
2014	<i>Reserved</i>
2015	Petition For IPR of U.S. Patent No. 9,535,623, <i>Sk Hynix, et al v. Netlist Inc.</i> , IPR2018-00303, Paper No. 1 (PTAB Dec. 14, 2017).
2016	Final Written Decision, <i>Sk Hynix, et al v. Netlist Inc.</i> , IPR2018-00303, Paper No. 42 (PTAB Mar. 21, 2019).
2017	Decl. of Dr. Alpert Regarding U.S. Patent No. 9,535,623, <i>Sk Hynix, et al v. Netlist Inc.</i> , IPR2018-00303, Ex. 1003 (PTAB Dec. 13, 2017).
2018	Excerpt of Case Docket Sheet, <i>Solas OLED Ltd. v. Dell Technologies Inc.</i> , Civil No. 6-19-cv-00514-ADA (W.D. Tex. Aug. 6, 2020)

Exhibit	Description
2019	Excerpt of Case Docket Sheet, <i>Solas OLED Ltd. v. Google Inc.</i> , Civil No. 6-19-cv-00515-ADA (W.D. Tex. Aug. 6, 2020)
2020	Excerpt of Case Docket Sheet, <i>Continental Intermodal Group-Trucking LLC v. Sand Revolution LLC et al</i> , Civil No. 7-18-cv-00147-ADA (W.D. Tex. Aug. 6, 2020)
2021	Email from Judge Albright's Clerk to the Parties, dated Oct. 13, 2020.
2022	Procedures Regarding Technology Tutorials, Claim Construction, Discovery Disputes, and Trial Date for the Honorable Alan D Albright
2023	Amended Scheduling Order Governing the '525 and '194 Cases, <i>Netlist, Inc. v. SK hynix Inc. and SK hynix America Inc.</i> , Civil No. 6:20-cv-00194-ADA (W.D. Tex. Nov. 18, 2020), ECF No. 73
2024	Declaration of Matthew S. Galica in Support of Pro Hac Vice Motion, dated March 8, 2021
2025	Declaration of Andrew H. DeVoogd in Support of Pro Hac Vice Motion, dated March 8, 2021
2026	Deposition Transcript of Dr. Donald Alpert, dated March 10, 2021
2027	Micron DDR3 SDRAM LRDIMM Product Sheet
2028	JEDEC Membership Details
2026	Deposition Transcript of Dr. Donald Alpert, dated March 10, 2021
2027	Micron DDR3 SDRAM LRDIMM Product Sheet
2028	JEDEC Membership Details
2029	Excerpt of DRAM Circuit Design, Fundamental and High-Speed Topics (2008)
2030	Excerpt of Semiconductor Memories, A Handbook of Design, Manufacture, and Application Second Edition (1997)
2031	Deposition of Dr. Donald Alpert, IPR2018-00303, <i>SK hynix, Inc., et al. v. Netlist, Inc.</i> , dated July 20, 2018
2032	Declaration of Robert J. Murphy dated March 11, 2021

I. Introduction

On June 9, 2020, SK hynix Inc. and SK hynix America Inc. (collectively, “Hynix” or “Petitioners”) submitted a Petition to institute *inter partes* review of U.S. Patent No. 9,858,218 (the “’218 patent”), and the Petition was accompanied by an expert declaration by Dr. Donald Alpert (Ex. 1003, “Alpert Declaration” or “Alpert Decl.”). Netlist, Inc. (“Netlist” or “Patent Owner”) submitted a Preliminary Response in response to the Petition. On December 17, 2020, the Board instituted review in an institution decision (Paper 13, “Decision”). The Board instituted review on the three grounds set forth in the Petition.

Netlist submits this Patent Owner Response in response to the Decision. This Patent Owner Response is accompanied by, *inter alia*, the Declaration of Robert J. Murphy (Ex. 2032), the cross-examination testimony of Dr. Alpert (Ex. 2026).

The Board should find the challenged claims patentable because the instituted grounds fail to demonstrate that a person of ordinary skill in the art would be motivated to (1) add Buchmann’s or JEDEC’s alleged training to Hazelzet, (2) create a new mode of operation in Hazelzet for Buchmann’s or JEDEC’s alleged training, or (3) use Hazelzet’s UE line for communicating training related information.

II. Identification of Claims Being Challenged

The Board instituted *inter partes* review on the following Grounds:

Ground	References	Basis	Challenged Claims
1	<i>Hazelzet and JEDEC</i>	35 U.S. C. § 103	1 – 22
2	<i>Hazelzet and Buchmann</i>	35 U.S. C. § 103	1 – 22
3	<i>Hazelzet, JEDEC or Buchmann, and Kim</i>	35 U.S. C. § 103	3 – 6, 10-12, and 17-20

III. Relevant Information Concerning the '218 Patent

A. The Correct Priority Date of the '218 Patent is June 12, 2009

The Petition erroneously argues that the '218 Patent is not entitled to this priority date because certain claim elements are not disclosed in the Provisional Application. (Pet. at 4-9). Contrary to the Petition, the '218 Patent is entitled to its stated priority date of June 12, 2009. (Ex. 2032 at ¶ 25).

1. The Petition Applies the Wrong Legal Standard

The Petition relies on the wrong legal standard for determining whether priority application adequately discloses the claims. There is no “necessarily comprehended” standard, as the Petition argues (Pet. at 5), in determining whether the claims are supported by a written description.¹ Instead, “[t]o obtain the benefit of the filing date of a parent application, the claims of the later-filed application must be supported by the written description in the parent in sufficient detail that one

¹ The legal standards set forth in the petition are in tension with regard to negative limitations. The Petition also states negative limitations need no disclosure at all because “silence additionally satisfies” such limitations. (Pet. at 51, 60 (citing *Süd-Chemie, Inc. v. Multisorb Technologies, Inc.*, 554 F.3d 1001, 1004-05 (Fed.Cir. 2009))).

skilled in the art can clearly conclude that the inventor invented the claimed invention as of the filing date sought.” *EnOcean GmbH v. Face Int’l Corp.*, 742 F.3d 955, 960 (Fed. Cir. 2014) (quoting *Anascape, Ltd. v. Nintendo of Am. Inc.*, 601 F.3d 1333, 1335 (Fed. Cir. 2010)) (internal quotations omitted). Contrary to the Petition, the standard requires that the “description must clearly allow persons of ordinary skill in the art to recognize that the inventor invented what is claimed.” *Ariad Pharm., Inc. v. Eli Lilly & Co.*, 598 F.3d 1336, 1351 (Fed. Cir. 2010). Thus, the question is whether the priority application “**reasonably conveys** to those skilled in the art that the inventor has possession of the claimed subject matter as of the filing date. *Id.* (emphasis added).

In addition, “[t]he written description requirement does not require the applicant ‘to describe exactly the subject matter claimed, [instead] the description must clearly allow persons of ordinary skill in the art to recognize that [the inventor] invented what is claimed.’” *Pandrol USA, LP v. Airboss Ry. Prods.*, 424 F.3d 1161, 1165 (Fed. Cir. 2005) (quoting *Union Oil Co. of Cal. v. Atl. Richfield Co.*, 208 F.3d 989, 997 (Fed. Cir. 2000)) (citation omitted); *see also Kao Corp. v. Unilever United States, Inc.*, 441 F.3d 963 (Fed. Cir. 2006) (“We have cautioned, however, that ‘the disclosure as originally filed does not . . . have to provide in *haec verba* support for the claimed subject matter at issue.’”) (citation omitted).

Under the correct standard, the Provisional Application reasonably conveys to a POSITA each claim of the '218 patent.

2. The '218 Patent Claims Reciting That the First Edge Connections Are not Active Are Supported By the Priority Application

The Petition incorrectly asserts that the claim element “train[ing] with one or more training sequences while the first edge connections are not active,” is not sufficiently disclosed in the Provisional Application. (Pet. at 4-7; Ex. 2032 at ¶ 26).

There is not a “heightened standard” for demonstrating that negative limitations have written description support. *Inphi Corp. v. Netlist, Inc.*, 805 F.3d 1350, 1356 (Fed. Cir. 2015). Instead, a specification satisfies the written description requirement when “the essence of the original disclosure” conveys the necessary information—“regardless of how it” conveys such information, and regardless of whether the disclosure's “words [a]re open to different interpretation[s]. *Id.* (citing *In re Wright*, 866 F.2d 422, 424-25 (Fed. Cir. 1989)). Also, “a lack of literal basis in the specification for a negative limitation may **not** be sufficient to establish a prima facie case for lack of descriptive support. *Ex parte Parks*, 30 USPQ2d 1234, 1236 (Bd. Pat. App. & Inter. 1993) (emphasis added).

a. The priority application provides written description support for this claim

The Priority Application discloses that that the MCH is idle while then-current LRDIMMs complete their tasks (e.g., training). (Ex. 1008 at 22) (“Although the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller, the LR-DIMM proposal requires the MCH to insert a waiting period. The shortcoming of the current the LR-DIMM proposal is that, instead of adopting the notification, the proposal requires the MCH to be in standby (idle, or wait) while the memory subsystem controller completes its task.”). (Ex. 2032 at ¶ 27).

Among its other disclosures, the Priority Application discloses the use of a notification signal to allow the MCH to execute independent commands instead of idling while the memory module performs training. (Ex. 1008 at 22) (“In the notifying method, the memory subsystem controller sends a signal to the MCH when it completes the required or requested operation. This method allows the MCH to execute independent command while it is waiting for a notification signaling for the memory subsystem controller.”). (Ex. 2032 at ¶ 28).

Allowing the MCH to execute independent commands means allowing the MCH to perform other tasks unrelated to the memory module undergoing training. (Ex. 1008 at 23) (“In certain embodiments in which more than one memory

subsystem is connected to the MCH, each controller that associates with each memory subsystem drives the notifying signal pin to the high impedance state from the low impedance state when it completes the required operation. Thus, it provides the condition that the MCH can only pull the notifying signal high when all memory subsystem controllers are done with the required operation. This method allows the MCH to work with a non-homogenous memory subsystem, such as mixing of DIMMs with different DIMM density, ranks, DRAM density, speed, DRAM configuration, etc.”). (Ex. 2032 at ¶ 29).

The Priority Application further discloses that, when the memory module is undergoing training, the Error-Out pin is pulled Low, and when the memory module is in normal operation, the Error-Out pin is pulled High. (Ex. 1008 at 23 and Fig. 3 (stating that the error-out pin is “Low during MB training” and “High during normal operation unless parity error occurs”)). Therefore, the memory module undergoing training is not accessed for normal read or write operation. (Ex. 1008 at 23); (Ex. 2032 at ¶ 30).

Before the MCH receives a notification signal from a memory subsystem performing training operations, it can perform independent operations that are unrelated to the memory subsystem. When the MCH is performing these independent operations, it is **not** performing operations with the memory module that is performing training. *Id.* The priority application further discloses that “the

notification of completion of the required or requested task from the memory subsystem controller would generate an interrupt to the system **during the initialization period** as error occurrence generates an interrupt to the system **during the normal operation**” (emphasis added). Thus, the priority application draws a clear boundary between initialization and normal operation. (Ex. 2032 at ¶ 31).

The passages above provide the “necessary information” to a POSITA that the ’595 patent claims reciting that the priority application provides written description support for the ’595 claims reciting that a memory controller not access the module for memory read and write operations in the second mode. (Ex. 2032 at ¶ 32).

The Petition corroborates this. (Pet. at 6 (“Moreover, it was known before the 2009 provisional filing date that **some training** included sending data over the data edge connections, while **other training did not.**”); *id.* (“It was known, however, that such buffers employed memory read and write operations instituted by the memory controller that transferred data over the edge connections with the data pins (“*first edge connections*”) during **some** training modes.”)). Setting aside the fact that Petitioners and Dr. Alpert cite no evidence for their speculation, the statement actually proves Patent Owner’s point. The Petition confirms that a POSITA would have clearly known that some training may have involved active data pins, while other types of training clearly would not. *Id.* (Ex. 2032 at ¶ 33).

Thus, the Provisional Application reasonably conveys to a POSITA that the first edge connections include one or more pins that are inactive during training. Having been disclosed, it is proper to claim. *Inphi Corp. v. Netlist, Inc.*, 805 F.3d 1350, 1356 (Fed. Cir. 2015).

3. The Provisional Application Supports the '218 Patent Claims Reciting Performance of One or More Memory Read or Write Operations Not Associated With the One or More Training Sequences

The Petition incorrectly asserts that “configured to perform one or more memory read or write operations not associated with the one or more training sequences,” as recited in each claim 1 of the '218 patent, is not sufficiently disclosed in the Provisional Application. (Pet. at 7-8; Ex. 2032 at ¶ 34).

a. The priority application provides written description support for this claim

The priority application explicitly discloses two modes of operation: training and normal. (Ex. 1008 at Fig 3. and pp. 22-23). The priority application then explains that memory modules performing MB training can output a low signal during MB training and that a high signal can indicate that **training is done**. (Ex. 1008 at Fig. 3). This unambiguously conveys to a POSITA that when training is **done**, the module will be in normal operation without training. (Ex. 2032 at ¶ 36).

Further, the priority application starts with the sentence: “Certain embodiments described herein provide a method of providing a feedback path from

a memory subsystem to the MCH (Memory Controller Hub, e.g., system memory controller) **during initialization**” (Ex. 1008 at 22), and then goes on to state that, “[i]n general, there is no method of handshaking between the MCH and a memory subsystem **during initialization...**” (Ex. 1008 at 22) (emphasis added). The priority application is clear that the method of providing a feedback path in certain embodiments is performed “during initialization.” A POSITA undoubtedly recognizes that when the memory subsystem is being initialized, it is **not** ready for memory operation, and thus is **not** accessed by the MCH for read or write operations. (Ex. 2032 at ¶ 37).

The priority application also discloses that “the notification of completion of the required or requested task from the memory subsystem controller would generate an interrupt to the system **during the initialization period** as error occurrence generates an interrupt to the system **during the normal operation**” (Ex. 1008 at 24) (emphasis added). Thus, the priority application draws a clear boundary between initialization and normal operation. (Ex. 2032 at ¶ 38).

In view of these disclosures, a POSITA would clearly understand that, when a memory module is performing training, it is **not** accessed by the MCH for read or write operations. This, alone, provides written description support, because a POSITA would understand that the priority application discloses the performance of

normal read or write operations that are not associated with training. (Ex. 2032 at ¶ 39).

b. Petitioners and Petitioners' expert corroborate that written description support exists for this claim

Petitioners and their expert corroborate that all the parts of that claim element would have been known to a POSITA when reading the Provisional Application. Petitioners' only argument is that training ***could*** occur during normal operation. (Pet. at 7 (“In fact, as Dr. Alpert explains, a Skilled Artisan would understand training ***could*** occur during normal operation.”)) (emphasis added). Petitioners' expert testified similarly. Ex. 2026 at 31:10-32:4 (explaining that it is not the case that training can never be done in normal operation). Setting aside the fact that Petitioners' argument is ***not*** disclosed in the priority application and they cite no evidence to substantiate their speculation, it actually proves Patent Owner's point. Through their statements, Petitioners and their expert tacitly concede that a POSITA would understand that training typically does not occur during normal operation—it just is not the case that training can never occur during normal operation. *Id.* This serves as an explicit message to a POSITA that the Provisional Application discloses normal read or write operations that are not associated with training. (Ex. 2032 at ¶ 40).

4. The Provisional Application Supports the '218 Patent Claims Reciting “One or More” Training “Sequences”

The Petition incorrectly asserts that “one or more” training “sequences,” as recited in each independent claim of the '218 patent, is not sufficiently disclosed in the Provisional Application. (Pet. at 8-9). Petitioners’ argument as to why “one or more training sequences” is not disclosed is that the provisional application “only discloses ‘MB Training.’” (Pet. at 8-9). Petitioners’ argument fails. (Ex. 2032 at ¶ 41)

To start, Petitioners’ expert admitted that a POSITA would understand that the provisional application discloses “multiple different types of training.” (Ex. 2026 at 33:17-20). That, alone, confirms that a POSITA would understand that the provision application discloses “one or more training sequences.” (Ex. 2032 at ¶ 42).

Additionally and separately, Dr. Alpert explains that the Provisional Application discloses “MB training” in the context of “then current LRDIMMs under development / standardization, DDR3 LRDIMM,” which a POSITA would understand refers to “training of interfaces to/from and/or operations of a Memory Buffer.” (Ex. 1003, ¶46). The Petition includes nearly identical admissions. (See Pet. at 6.) In that same context, the Provisional Application also discloses initialization sequences when describing that newly developed LR-DIMMs memory modules require “the MCH to hand over *one or more parts of the initialization*

operation sequences to the memory subsystem controller” as an issue to be addressed by the invention. (Ex. 1008 at 22 (emphasis added); Ex. 2032 at ¶ 43).

Here, the Provisional Application reasonably conveys operation sequences (e.g., sequences of operations) that would occur during the initialization of a memory subsystem (e.g., “initialization operation sequences”). MB training is exactly that—a sequence of training operations that could occur during the overall initialization period. It is explicitly disclosed by the Provisional Application. Petitioners’ expert went a step further and stated that, in addition to MB training, a POSITA would understand that the provisional application discloses “multiple different types of training.” (Ex. 2026 at 33:17-20; Ex. 2032 at ¶ 44).

Even in the context of just MB training, one or more training sequences are disclosed. This is because the Provisional Application explains that memory modules performing MB training has its notifying signal pin at a low impedance state during MB training and can drive its notifying signal pin to a high impedance state to indicate that training is done. (Ex. 1008 at 22 and Fig. 3 (stating that the error-out pin is “low during MB training”); Ex. 1032 ¶ 45).

The Provisional Application explicitly states that the low impedance state can be asserted for different sections of the overall initialization step. (Ex. 1008 at 23) (“Figure 3 shows the operation of the notifying signal in accordance with an example embodiment. The output of *the notifying signal is low* impedance while the memory

subsystem controller executing *each section of the initialization step*, thus the notifying signal is pulled low by the memory subsystem controller. *As the memory controller completes each step, it drives the notifying signal pin to the high impedance state.*”) (emphasis added). Collectively, multiple training operations are performed, and multiple notifying signals in relation to training operations are disclosed. This clearly discloses “one or more” training sequences. Therefore, the Provisional Application sufficiently discloses, and the patent owner properly claims, one or more training sequences. (Ex. 2032 at ¶ 46).

B. General Overview of the '218 Patent

The '218 patent has a priority date of June 12, 2009, and relates generally to the operation of memory modules. (Ex. 1001). Specifically, the '218 patent discloses a memory module that can function in two different modes communicating with a host system. (Ex. 1001, Abstract; Ex. 2032 at ¶ 47).

As described in the '218 patent, memory modules operate in two distinct modes of operation. (Ex. 1001, 1:42-52, 1:63-2:8, 2:9-14, 4:24-28, 5:61-64, 7:58-65, 9:20-24, 11:47-51, 12:13-17, 12:44-48). The first mode of operation mode in which the memory module executes a training sequence, during which the memory module may transmit to the memory controller a notification signal associated with the training sequence, but during which the memory module is not accessed by the host for normal memory read or write operations. (Ex. 1001, 1:45-49, 2:17-24, 4:24-

31, 5:61-6:10, 6:15-30, 7:3-18, 9:20-27, 11:46-54, 11:55-63). The second mode of operation is a normal operational mode, in which the memory module performs standard read-write, pre-charge, refresh, and similar other standard operations, during which the memory devices are generally accessible by the host system. (Ex. 1001, 1:49-58, 2:2-6, 6:41-48, 12:4-8; Ex. 2032 at ¶ 48).

The memory module includes a notification circuit which outputs a notification signal associated with the training sequences to the host system. (Ex. 1001, 1:45-49, 1:66-2:2, 2:20-24, 4:31-37, 7:2-14; Ex. 2032 at ¶ 49).

IV. Overview of the References

A. Hazelzet

U.S. Patent App. Pub. No. 2008/0098277 to Hazelzet (“Hazelzet”) is U.S. Patent Publication that was filed on October 23, 2006. Hazelzet discloses a memory module including error correction code (ECC) logic “to identify and correct single bit errors on the command or address bus.” (Ex. 1014 at [0008]). The invention disclosed in Hazelzet further includes an error reporting mode during which the system can interrogate the module regarding its error status. (Ex. 1014 at [0009]). The invention implements these features in a register “having error correction code (ECC), parity checking, a multi-byte fault reporting register, read via an independent bus, and real time error lines for both correctable errors and uncorrectable error conditions.” (Ex. 1014 at [0016]). Thus, Hazelzet’s invention discloses a hybrid

device utilizing error detection, error correction, and parity. It does not discuss or mention training. (Ex. 2032 at ¶ 50).

B. Buchmann

U.S. Patent No. 8,139,430 to Buchmann (“Buchmann”) discloses a power-on initialization test for a cascade interconnect system. Buchmann discloses a memory buffer that includes a bus interface to links in a high-speed channel for communicating with a memory controller via a direct connection or via a cascade interconnection and another memory buffer. (Ex. 1016 at 1:39-43). The interface is operable in a static bit communication (SBC) mode and a high-speed mode. (Ex. 1016 at 1:43-44). The memory buffer includes logic for executing a power-on and initialization training sequence initiated by the memory controller. (Ex. 1016 at 1:44-48). The sequence includes initializing the links to the high-speed channel. (Ex. 1016 at 1:48-50; Ex. 2032 at ¶ 51).

C. JEDEC

The JEDEC reference which Petitioners rely on (Ex. 1015) is not prior art to the '218 Patent because it post-dates the priority date of the '218 Patent. *See*, Sections III.A.1 - 4, *supra*; *see also* Section V.A, *infra*. The '218 Patent claims priority to Provisional Application No. 61/186,799 (Ex. 1008 at 12) (the “Provisional Application”) which has a filing date of June 12, 2009. (Ex. 1001, Cover). Nonetheless, JEDEC discloses Write Leveling and Read Enable Training Ex. 1015

at 4. JEDEC states that the MB performs ‘Write Leveling’ to the DRAMs to ensure successful writes, and ‘Read Enable Training’ to ensure it can capture read data from the DRAMs correctly, as part of the DRAM interface training. (Ex. 1015 at 8; (Ex. 2032 at ¶ 52).

V. Grounds 1-3 Fail for Numerous, Reasons

Petitioners rely on two combinations to challenge all independent claims in the ’218 patent: (1) Hazelzet with JEDEC (“Ground 1”) and (2) Hazelzet with Buchmann (“Ground 2”).² Section II, *supra*. (Ex. 2032 at ¶ 53).

In Ground 1, Petitioners allege that Hazelzet could be combined with JEDEC. Pet. at 33-36. More specifically, Petitioners allege that the combination of Hazelzet and JEDEC “include a ‘*first mode*’ in which training is carried out.” (Pet. at 47). Petitioners rely on JEDEC’s Write Leveling and Read Enable Training function to satisfy the “training sequences” limitation of Claim 1. (Pet. at 48). Petitioners allege that JEDEC’s ERROUT# signal “are ‘*associated with the one or more training sequences*’ and could be transmitted via an open drain output. (Pet. at 53-54; Ex. 2032 at ¶ 54).

² Petitioners’ Ground 3 (“Claims 3-6, 10-12, 20, and 17-20 are obvious over the combinations analyzed above, and Kim”) (Pet. at 66-71) only challenges dependent claims of the ’218 patent. For the same reasons that Petitioners’ Grounds 1 and 2 fail, Petitioners’ Ground 3 also fail.

In Ground 2, Petitioners allege that Hazelzet could be combined with Buchman. (Pet. at 33-36). Specifically, Petitioners allege that the combination of Hazelzet and Buchman “include a ‘*first mode*’ in which training is carried out.” Pet. at 47. Petitioners rely on Buchmann’s TS0 and TS3 function to satisfy the “training sequences” limitation of Claim 1. (Pet. at 48). Petitioners allege that Buchmann’s TS0_done, TS3_ack, or TS3_done signals “are ‘*associated with the one or more training sequences*’” and could be transmitted via an open drain output. (Pet. at 50-52; Ex. 2032 at ¶ 55).

All Grounds need to demonstrate that a POSITA would find it obvious (1) to add the kind of alleged training in JEDEC or Buchmann to Hazelzet (2) in an entirely new mode that is separate from Hazelzet’s normal mode of operation and (3) utilize a single output to communicate parity errors and information related to training. As explained below, Ground 1 fails because JEDEC is not prior art. Further, all Grounds fail because there is (1) no motivation to add the type of training in JEDEC or Buchmann to Hazelzet, (2) no motivation to combine Hazelzet with Buchmann or JEDEC in a way that Hazelzet is reconstructed to have a training mode separate from its ECC mode of operation, and (3) no motivation to combine Hazelzet with Buchmann or JEDEC such that Hazelzet is reconstructed to output signals related to training sequences over its UE line while in a training mode, and, separately, output

parity errors via its open drain line during a normal mode of operation. (Ex. 2032 at ¶ 56).

A. Ground 1 Fails Because Petitioners Have Failed to Demonstrate that JEDEC is Prior Art

Ground 1 of the Petition fails because Petitioners have failed to demonstrate that JEDEC is prior art. To prevail on this issue, Petitioners must first prove that JEDEC was sufficiently “publicly accessible” and therefore is a printed publication under 35 U.S.C. § 311(b). This requires Petitioners to prove that JEDEC has “been disseminated or otherwise made available to the extent that persons interested and ordinarily skilled in the subject matter or art exercising reasonable diligence, can locate it.” (*SRI International, Inc. v. Internet Security Systems, Inc.*, 511 F.3d 1186, 1194 (2008), *quoting Bruckelmyer v. Ground Heaters, Inc.*, 445 F.3d 1374, 1378 (Fed. Circ. 2006); Ex. 2032 at ¶ 57).

Petitioners advance two related arguments that JEDEC meets the threshold for sufficient public accessibility, none of which are sufficient to meet Petitioners’ burden: (1) JEDEC was distributed to committee members as a link on November 11, 2009 which represented “interested members of the relevant public”; and (2) the rules of JEDEC did not require an obligation to maintain documents confidential, and there was an expectation to distribute it to others. (Pet. at 27-30). Each of these

arguments, individually or collectively, fail to demonstrate that JEDEC was publicly accessible.

1. Petitioners fail to show that distributing JEDEC to committee members rendered the reference publicly available

Petitioners' first argument is that JEDEC was sufficiently publicly accessible once it was distributed to committee members on November 11, 2009. To prevail on this argument, Petitioners must prove:

- (1) the electronic JEDEC reference was available to those interested and skilled in the art and not simply those already members or participants in the organization maintaining the repository, *see Samsung Electronics Co. Ltd. v. Rembrandt Wireless Technologies, LP*, IPR2014-00514, Paper 18, at 4 (P.T.A.B. Sept. 9, 2014)) (“*Rembrandt* Final Written Decision”); and
- (2) one interested and skilled in the art could reasonably have found the electronic JEDEC reference. (*SRI International, Inc.*, 511 F.3d at 1195).

Failure on either of these elements is fatal to Petitioners' argument, but Petitioners failed to present evidence on both.

a. Petitioners fail to show that documents available on the JEDEC website were in fact available to anyone not already a participant in JEDEC.

As to the first element, Petitioners attempt to prove the JEDEC was available to participants in JEDEC, but fail to meet their burden of demonstrating that the

reference was available to persons of ordinary skill and interest outside that organization. Indeed, Petitioners do not even argue that the reference was available to persons of ordinary skill outside of JEDEC, much less prove it.

Showing that a reference in an electronic repository was sufficiently available to persons of skill and interest outside the organization controlling that repository typically requires evidence of efforts to apprise the public—and not merely those already a part of the organization making a reference available—of a reference’s availability. *See Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1349 (Fed. Cir. 2016); *see also Samsung Elecs. Co. v. Infobridge Pte. Ltd.*, 929 F.3d 1363, 1370-73 (Fed. Cir. 2019).

Petitioners have presented no such evidence here, and this Petition is defective for a reason identical to the reason the Board found dispositive in denying institution in *Samsung v. Rembrandt*, where institution of the petition turned on whether a “[d]raft [s]tandard, on which both of Petitioner’s asserted grounds of unpatentability rely, is a printed publication.” (*Rembrandt* Final Written Decision at 4). Samsung presented extrinsic evidence that the reference, a draft iteration of the IEEE standard 802.11, was uploaded to the server of the IEEE working group on the subject and available to its members. (*Id.* at 5). Samsung also presented evidence that, while the reference was password-protected on the server, the password was disseminated throughout the working group, and membership in that group was granted to “any

interested parties[.]” (*Id.* at 7). An announcement of the reference’s availability for download was even mailed to the listserv for the working group, subscription to which was open to the public and automatically granted upon request. (*Id.* at 5-6). Collectively, however, this evidence demonstrated only that the reference available as of the date of upload to “members of the 802.11 Working Group and those who already knew about [reference] or the ... meeting of the 802.11 Working Group [where the reference was discussed][.]” (*Id.* at 7) The Board therefore rejected Samsung’s *Rembrandt* Petition for failure to establish the required public accessibility.

Here, the same holds true: Petitioners fail to present evidence sufficient to prove that JEDEC was available to one of skill and interest in the art not already a member of JEDEC. Petitioners proffer no extrinsic evidence that anyone of skill and interest in the art not already a member of JEDEC actually accessed JEDEC. *Contrast Medtronic, Inc., v. AGA Medical Corp.*, 618 F.Supp.2d 1191, 1193 (N.D. Cal., April 28, 2009) (evidence that “anyone outside of the institution in which the asserted reference was housed had located the reference” created issue of fact as to whether the reference was a printed publication). Nor do Petitioners present evidence that the JEDEC website, an electronic repository, where the linked reference was housed, was advertised outside of that organization or that persons of skill and interest in the art who were not part of JEDEC were apprised of the

reference's or even repository's availability. See *Blue Calypso, LLC v. Groupon, Inc.*, 815 F.3d 1331, 1349 (Fed. Cir. 2016); see also *Samsung Elecs. Co. v. Infobridge Pte. Ltd.*, 929 F.3d 1363, 1370-73 (Fed. Cir. 2019).

Moreover, Petitioners fail to proffer evidence that one of skill and interest in the art, as they define such a person, would have known of JEDEC and known to check its online repository for information pertinent to the art. According to Petitioners, a person of ordinary skill in the art simply has “a bachelor’s degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems,” and “would have been familiar with computer memory systems and basic CPU architecture documented in the literature, including standards, and generally available in commercial systems, including how computer components access a computer’s memory, the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system.” (Pet. at 9). Familiarity with the JEDEC organization is not, by Petitioners’ definition, required for a person of ordinary skill in the art.

Petitioners nonetheless simply assume that a person of ordinary skill would know to check the JEDEC site for information of relevance to the art. Petitioners present no competent evidence to support that assumption, and instead relies solely on conclusory and unsupported statements from its declarants. (Ex. 1054 at ¶ 11;

Ex. 1055 at ¶ 7). No evidence was provided in support of the proposition that JEDEC was publicly available, aside from JEDEC members. Consequently, Petitioners have not met their burden of demonstrating JEDEC was publicly available to persons of ordinary skill outside of the JEDEC organization.

b. Petitioners fail to identify evidence that a person of skill and interest in the art could reasonably be expected to find the JEDEC reference in the JEDEC repository.

Petitioners likewise fail to present evidence sufficient to establish a reasonable likelihood of success on the second element of public accessibility, that a person of skill and interest in the art could reasonably be expected to find the reference within the JEDEC repository. Again, Petitioners do not ever assert this required element, much less identify evidence sufficient to prove it.

Evidence that a reference was publicly available in an electronic repository to persons of ordinary skill outside of the repository's organization must be coupled with evidence that such persons could reasonably have found it within that repository. In *SRI International, Inc.*, the Federal Circuit held that evidence that reference was uploaded to the publicly-available file-transfer protocol ("FTP") site of a consortium of parties interested in the art did not establish the references as a printed publication because, for an electronic reference to be publicly accessible, the manner by which it was stored or disseminated must have provided something akin

to a “roadmap that would have allowed one skilled in the art to locate” the reference. (*SRI International, Inc.*, at 1195-96, *quoting Bruckelmyer*, 445 F.3d at 1379).

Petitioners have presented no evidence that persons of skill and interest in the art looking at the JEDEC website could reasonably have found JEDEC therein. That is because JEDEC’s website could only be accessed by members. In an attempt to demonstrate that JEDEC was accessible by anyone, Petitioners simply state in a footnote that “Ms. Carlson testifies that ‘JEDEC membership is open,’ and access to documents such as JEDEC provided to those who join. (Pet. at 30-31, Footnote 7). But Petitioners fail to capture Ms. Carlson’s full quote that “JEDEC membership is open to ***any company or organization, or one of its related entities***, that manufactures electronic equipment or electronic-related products or related services,” which is in accordance with the JEDIC’s membership webpage, which was accessed using the Wayback Machine from its archive on April 10, 2009. (Ex. 1050, ¶ 5 (emphasis added); Ex. 2028).

Membership to JEDEC was not available to all persons of skill and interest in the art, and instead only to companies that met JEDEC’s requirements for membership. For example, on JEDEC’s membership webpage, the requirements for membership are delineated. The webpage explains that membership is not open to individuals, which Petitioners’ definition of a POSITA contemplates, and instead

membership is only open to companies that “manufacture semiconductor products, or provide related services or equipment.” (Ex. 2028). The webpage further explains that “[m]embership is company based, not by individual.” *Id.*

Further, in order to obtain membership and access JEDEC materials, qualifying companies needed to pay an annual dues in order to maintain their membership. Membership entitled a company “to appoint ***one principal member*** and alternate members to the committee or committee(s) of choice.” *Id.* (emphasis added). And in order to appoint a principal member to a committee, a company had to pay an annual dues commensurate with the number of committees it wished to appoint a member. For example, the membership webpage lists the annual dues for different levels of access:

Annual Dues are calculated on a calendar year basis (January-December).*

- One committee and subcommittees \$4,000
- Two committees and subcommittees \$6,500
- Three committees and subcommittees \$9,000
- Four or more committees and subcommittees \$12,000

(Ex. 2028). Paying annual dues in order for exclusive access to JEDEC materials runs counter the idea of public accessibility. It is akin to paying a yearly membership at a private country club to keep the public from accessing it.

2. Petitioners fail to show that the absence of confidentiality provision and that there was an expectation to distribute JEDEC to others rendered the reference publicly available

Petitioners' final prior art theory is an apparent attempt to cure the first fatal defect of their initial theory, *i.e.*, that it was only distributed to members of JEDEC which did not render the reference publicly accessible because there is no evidence demonstrating that it was available to persons of ordinary skill outside the JEDEC organization. To that end, Petitioners' final theory is that JEDEC should be considered prior art because there was no obligation to keep it confidential and there was an expectation that it would be distributed to others. (Pet. at 29-30). But this theory fails to render JEDEC as prior art as well.

Petitioners point to JEDEC documents that allegedly do not contain an obligation to keep documents confidential, to the testimony of their declarant that testified that "there was an expectation of distribution to others," then state that "JEDEC was distributed to twenty-three key members of the interested public, with no obligation of confidentiality, and with the expectation it would be freely discussed with others, including parties who were not members of JEDEC. (Pet. at 29-30). First, twenty-three members of a private organization are not "key members of the interested public." Further, Petitioners have offered no evidence that demonstrates that JEDIC was distributed to any people who were not members of JEDEC.

Finally, Petitioners' admission that only twenty-three committee members were distributed JEDEC is an explicit admission by Petitioners that JEDEC was only distributed to committee members, which were representatives of paying companies, and not the "relevant public."

Thus, JEDEC was not publicly accessible, and therefore, is not prior art under 35. U.S.C § 102(a).

B. Grounds 1-3 Fail Because There is No Motivation to Add Buchmann's or JEDEC's Alleged Training to Hazelzet

1. Problem and Solution Taught in Hazelzet

The Petition identifies an alleged problem with Hazelzet related to errors in data caused by unreliable or noisy communications between a host system and a memory module. (Pet. at 26). This is not correct. In reality, Hazelzet focused on providing a cost-sensitive solution for optimizing performance and reliability. (Ex. 1014 at [0001]-[0006]). Unlike Petitioners' characterization, Hazelzet did not focus myopically on a system's reliability to the detriment of its performance or cost considerations. Instead, Hazelzet sought a solution that would strike a balance, for low end and midrange systems ("reduced function" systems having an "adequate level of asset-protection"), between performance, reliability, and cost. *Id.* Hazelzet identified this as being a problem overlooked by the industry. *Id.* (Ex. 2032 at ¶ 58).

Hazelzet contemplated numerous, different solutions to this problem including: “memory mirroring, symbol slicing and extensive forms of fault rejection and redundancy” as well as “error detection and/or correction methods such as CRC (Cyclic Redundancy Code), EDC (Error Detection and Correction), parity or other encoding/decoding methods suited for this purpose” and “further reliability enhancements [that] may include operation re-try (to overcome intermittent faults such as those associated with the transfer of information), the use of one or more alternate or replacement communication paths to replace failing paths and/or lines, complement-re- complement techniques” and “the use of bus termination, on busses as simple as point-to-point links or as complex as multi-drop structures,” which “is becoming more common consistent with increased performance demands.” (Ex. 1014 at [0005], [0127], [0128]). Ultimately, based on performance, cost, and reliability considerations, Hazelzet chose to implement a hybrid solution focused on error code correction (“ECC”) functionality that allows a memory module system to perform normal operations in conjunction with parity. Hazelzet at [0016]. Hazelzet relied on parity to enhance a system’s performance and ECC to enhance its reliability. (Ex. 2031 (Alpert Deposition) at 65:13-19). Hazelzet makes no mention of training—even in its contemplated alternative solutions to the problem it identified (i.e., the appropriate balance of performance and reliability for low end memory systems). (Ex. 1014 at [0005], [0127], [0128]). Notwithstanding,

Petitioners allege that a POSITA would be motivated to add training—specifically, the alleged training disclosed in Buchmann and JEDEC—to Hazelzet. (Pet. at 33-38; Ex. 2032 at ¶ 59).

A POSITA would not be motivated to add Buchmann’s or JEDEC’s alleged training to Hazelzet. Buchmann’s and JEDEC’s alleged training, in contrast to Hazelzet’s chosen solution of ECC, are fundamentally different solutions to distinct problems in memory modules. As explained in further detail below, ECC uses an algorithm to correct errors in received data packets after the data has been transmitted. Buchmann’s alleged training seeks to synchronize the timing of memory module communication to ensure error-free transmission of data packets via a high-speed link before the data is sent, while JEDEC’s alleged training is meant to solve the timing issues related to the memory buffers in LR-DIMM, which are not present in Hazelzet. Put simply, ECC corrects data errors once they have occurred, and, in contrast, Buchmann’s or JEDEC’s alleged training is used to prevent timing errors from occurring before they do. (Ex. 2032 at ¶ 60).

2. General Overview of ECC

A system implementing ECC leverages redundancies encoded in data packets to detect errors in transmitted data, and to apply a correcting algorithm to the corrupted data. Redundancy is used primarily for correcting “hard” errors in memory circuits to improve production yield. (Ex. 2030 at 764). With error correction it is

possible to detect and correct errors occurring either in manufacturing or in the field to “improve the reliability of the memory device in the system” as well as the yield. (Ex. 2030 at 765). Detecting and correcting errors can be used to give improvement in long term in-system yield. (Ex. 2030 at 765; Ex. 2032 at ¶ 61).

Generally, error correction involves two simple steps: first, an error must be detected, and, second, the error must be corrected. (Ex. 2030 at 765). The simplest method of error correction is a simple duplication of every bit in the array. (Ex. 2030 at 765). The drawback to this is that the chip size is increased. Different techniques can be deployed which take less area on the chip, though. (Ex. 2030 at 765). Hamming codes are frequently used for this purpose. (Ex. 2030 at 765). With Hamming codes, error correction can be performed on many different bit field sizes with the assistance of additional parity bits in the array. (Ex. 2030 at 765). There is a trade-off in that small bit fields allow fast error detection but require a large number of extra parity bits in the memory matrix. (Ex. 2030 at 766). Large bit fields permit use of a smaller amount of extra matrix for the parity cells but error detection is slower. (Ex. 2030 at 766; Ex. 2032 at ¶ 62).

With single error correction, a memory word with one bad bit can be corrected to recover the original information, whereas two bad bits can be detected, but not corrected. (Ex. 2030 at 766). Error correction is useful in system not only to correct soft errors due to noise or alpha particle hits, but also for hard error correction. (Ex.

2030 at 766). A soft error can be corrected by reprogramming the bit. (Ex. 2030 at 766). A hard error is a “stuck at” failure. Since only one error in a word can be corrected, a system failure with error correction present occurs only if two errors occur in the same word. (Ex. 2030 at 766). This occurrence can be lessened by clearing the soft errors more frequently and by regularly replacing parts with hard errors. (Ex. 2030 at 766). For these reasons, ECC is an effective way to reduce and eliminate soft and hard errors in memory systems in order to improve the reliability of data being communicated. (Ex. 2032 at ¶ 63).

3. General Overview of Training

Timing uncertainty is a challenge—separate from the existence of soft and hard errors in memory systems which are resolved via ECC—related to data capture and processing in memory systems. (Ex. 2029 at 195). This would exist in Buchmann’s high speed link or JEDEC’s memory buffers. It is related to data capture and processing, which is a different problem than Hazelzet attempted to resolve. In operation, a clock path that runs between the clock pads and capture latches may include a clock receiver, timing adjust circuits, and a clock distribution network (or clock tree). (Ex. 2029 at 195). Data, command, and address paths, on the other hand, may be much shorter and only include input buffers. (Ex. 2029 at 195). With different electrical lengths, the input paths are no longer source synchronous internally. (Ex. 2029 at 195). Furthermore, process, voltage and

temperature (PVT) variations introduce excessive jitter, and even post-production trimming may not be sufficient as the timing margin shrinks. (Ex. 2029 at 195). Aligning the clock with data, command and address helps ensure synchronous communication. One way to retain the clock and data relationship is by matching the routing all the way from the pads to the capture points. (Ex. 2029 at 195). On-chip, closed-loop synchronization or input path “de-skewing” is another approach. (Ex. 2029 at 195). For instance, data training, either in relation to a host memory controller or conducted inside the DRAM itself, can improve the capture timing or ensure reliable data capture over PVT variations. (Ex. 2029 at 195; Ex. 2032 at ¶ 64).

Based on various design choices that a POSITA would consider, synchronization circuitry can be implemented using digital or analog, open or closed loop methodologies or any combination thereof. (Ex. 2029 at 252). The two most common synchronization circuits used are the delay-locked loop (DLL) and the phase-locked loop (PLL). (Ex. 2029 at 252). The DLL is widely used in memory interfaces for its simplicity and good jitter performance. (Ex. 2029 at 252). An alternative approach is the PLL, which is usually found in communication systems and microprocessors for clock data recovery and frequency synthesis. (Ex. 2029 at 252; Ex. 2032 at ¶ 65).

4. General Differences Between ECC and Training

Training is a solution to a different problem than that addressed by ECC. Training seeks to pre-emptively ensure reliable performance of a memory module. From the perspective of the memory controller, each component on a memory module is a slightly different distance away, and each component takes a slightly different amount of time to perform an operation. Conventional memory modules include predetermined constants for timing that balance these concerns by erring on the side of allowing more time, and thus result in inefficiency. (Ex. 2032 at ¶ 66).

ECC cannot, and does not, seek to optimize the timing of signals between memory controller and components on the memory module. ECC is used to correct errors in data packets by including redundant information in each data packet. Upon receipt of the data packets, an algorithm compares all the data to determine whether there are any errors, and if so, to use the redundant information to correct the errors. (Ex. 2032 at ¶ 67).

At a high level, the shipment of a package from a shipping company to a recipient is a useful analogy to highlight the differences between ECC and training. Training is used to determine when a package should be sent and received to ensure that the intended recipient is available to receive it. If it is sent too early or late, the intended recipient will not be home to receive it. Training makes sure that the shipping company sends the package at a time when the recipient is home. ECC, on

the other hand, seeks to ensure that the right content is sent in the package, and, if not, resending the correct content. This is done without regard for when the package is sent. ECC ensures that, if a basketball is intended to be shipped, a basketball is ultimately shipped. If, instead, a football is shipped, ECC will correct the mistake and resend a package that includes a basketball. (Ex. 2032 at ¶ 68).

5. There is No Motivation to Add Buchmann’s or JEDEC’s Alleged Training to Hazelzet for Multiple Reasons

All of Petitioners’ Grounds require Buchmann’s or JEDEC’s alleged training to be added to Hazelzet. (Pet. at 4). Petitioners allege that a POSITA “would have been motivated to add training to Hazelzet because it was known that training improved memory module reliability.” (Pet. at 38). That is the only reason Petitioners give for why a POSITA would specifically—and to the exclusion of other choices—add Buchmann’s or JEDEC’s alleged training to Hazelzet. This single, conclusory statement fails to establish, with any particularity, why a POSITA would have specifically chosen Buchmann’s or JEDEC’s alleged training—as opposed to any other technique to improve memory module reliability—to add to Hazelzet, without hindsight teachings from the ’218 patent. (Ex. 2032 at ¶ 69).

a. Petitioners’ Motivation to Combine is Conclusory and Logically Inconsistent

Petitioners do not explain why a POSITA would be motivated to add training to Hazelzet beyond the generic, conclusory statement that all the references relate to

“reliability.” (Pet. at 37-38). Legally, this fails to satisfy a motivation to combine the references. The Supreme Court has stated that “a patent composed of several elements is not proved obvious merely by demonstrating that each of its elements was, independently, known in the prior art.” *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 398, 418-19 (2007). Instead, “a range of real-world facts to determine ‘whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue’” must be considered. *Intercontinental Great Brands LLC v. Kellogg N. Am. Co.*, 869 F.d 1336, 1344 (Fed. Cir. 2017). Petitioners do not even attempt to analyze why a POSITA would be motivated to add training—to the exclusion of any other technique—to Hazelzet in order to “improve overall system reliability.” (Ex. 2032 at ¶ 70).

Hazelzet, itself, presents a different memory module from that of Buchmann or JEDEC, and aims to solve a different problem. Specifically, Hazelzet uses ECC to improve system reliability. This demonstrates that a POSITA would not be motivated to add training, because there is no teaching or suggestion of any other problems to be solved using training besides the alleged problem of “system reliability” which has already been resolved by ECC. As the Federal Circuit has determined, “recognition of a need does not render obvious the achievement that meets that need. There is an important distinction between the general motivation to cure an uncured disease..., and the motivation to create a particular cure...

Recognition of an unsolved problem does not render the solution obvious.” *Cardiac Pacemakers, Inc. v. St. Jude Medical, Inc.*, 381 F.3d 1371 (Fed. Cir. 2004). Here, like *Cardiac Pacemakers*, Petitioners offer a cure (training) to a problem (reliability) that has already been resolved (Hazelzet’s ECC). This does not demonstrate obviousness or a motivation to add training to Hazelzet, let alone the specific type of training alleged to be disclosed in Buchmann or JEDEC. In fact, Hazelzet’s choice to use ECC to solve the only problem it presents, is further indicia of non-obviousness. *Arris Int’l PLC v. Sony Corp.*, IPR2016-00828, Paper 10 at 15-16 (PTAB Oct. 7, 2016)(denying institution and rejecting petitioner’s obviousness rationale that “fails to acknowledge that [the primary prior art reference] already provides a different solution to the problem identified by Petitioner”); *see also Front Row Techs. v. MLB Advanced Media, L.P.*, IPR2015-01932, Paper 7 at 17 (PTAB Mar. 25, 2016)(denying institution and rejecting petitioner’s basis for combining the prior art “to utilize a ticket selling device in place of a ticket seller” as “not persuasive reasoning or even a motivation to combine” since the primary prior art reference “already utilizes various ticket selling devices”). (Ex. 2032 at ¶ 71).

Despite a myriad of options available to improve the “reliability” of a memory system—many of which are identified in Hazelzet (Ex. 1014 at [0005], [0127] and [0128]) and do not include training—Petitioners state that training, alone, would be the obvious choice. Such a conclusory, unsupported statement “fail[s] to provide any

meaningful explanation for why one of ordinary skill in the art would be motivated to combine these references at the time of this invention” and “fail[s] to explain why a person of ordinary skill in the art would have combined elements from specific references in the way the claimed invention does.” *Graham v. John Deere Co. of Kan. City*, 383 U.S. 1, 36 (1966). (Ex. 2032 at ¶ 72).

The conclusory testimony of Petitioners’ expert does not provide an articulated motivation to add Buchmann’s or JEDEC’s alleged training to Hazelzet either. (Ex. 1003 at ¶¶ 139-141). Instead, the expert declaration parrots, nearly verbatim, the Petition. *Id.* These conclusory statements do not amount to substantial evidence. *Mobilemedia Ideas LLC v. Apple Inc.*, 780 F.3d 1159, 1172 (Fed. Cir. 2015); *TQ Delta, LLC v. Cisco Sys., Inc.*, Nos. 2018-1766, 2018-1767 (Fed. Cir. Nov. 22, 2019); (Ex. 2032 at ¶ 73).

b. Petitioners’ Motivation to Combine is the Result of Impermissible Hindsight

Petitioners’ unsupported contention to add training to Hazelzet is irreconcilable with their previous positions, and is the result of improper hindsight. (Ex. 2032 at ¶ 74).

For example, in an earlier IPR between the two parties, Petitioners and Dr. Alpert argued that Hazelzet includes training. IPR2018-00303, Paper 1 at 28-32; IPR2018-00303, Ex. 1003 at ¶¶ 139-151. In his deposition for that IPR, Dr. Alpert

even stated that “a training sequence for Hazelzet would be the sequence of retrying memory accesses in the ECC mode.” IPR2018-00303, Ex. 2006, at 89:19-23. Dr. Alpert went on to contend that a POSITA would understand the ECC mode of Hazelzet to be training. (Ex. 2031 at 92:23-93:5). It is inarguable that Petitioners’ expert has already alleged that Hazelzet’s ECC mode is training. If Hazelzet already has training, why would a POSITA be motivated to add training? The rhetorical answer is: a POSITA would not. (Ex. 2032 at ¶ 75).

However, now Petitioners’ expert emphatically states that Hazelzet does **not** have training. (Ex. 2026 at 52:17-22; 53:13-18). In similar contradictory fashion, Petitioners and their expert previously said that training would be obvious to add to Hazelzet’s ECC (normal) mode, but now say it would be obvious to add a whole new training mode of operation in Hazelzet that is separate from its ECC (normal) mode. *See* Section V.C, *infra*. Put another way, depending on the claims that Petitioners and their expert are challenging, they interpret and map references differently. This is backwards. What Hazelzet discloses has to be the same no matter what. Likewise, how a POSITA would be motivated to combine it with other references does not change depending on the claims being challenged. Hazelzet either discloses training or does not. Both cannot be true. And it would either be obvious to add training to Hazelzet’s ECC mode or not. Again, both cannot be true. (Ex. 2032 at ¶ 76).

The only explanation for Petitioners’ dramatic shift in positions is that they are using the claims as a guide to reconstruct a system based on cherry-picked passages of disparate references. This is textbook impermissible hindsight. One cannot “stitch together an obviousness finding from discrete portions of prior art references without considering the references as a whole.” *In re Enhanced Security Research, LLC*, 739 F.3d 1347, 1355 (Fed. Cir. 2014). Courts are clear on this point. The “[d]etermination of obviousness cannot be based on the hindsight combination of components selectively culled from the prior art to fit the parameters of the patented invention.” *ATD Corp. v. Lydall, Inc.*, 159 F.3d 534, 546 (Fed. Cir. 1998). “One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to deprecate the claimed invention.” *In re Fine*, 837 F.2d 1071, 1075 (Fed. Cir. 1988). Most importantly, it is improper to backtrack from the claims to try to find something related in the prior art. Indeed, “[i]t is impermissible, however, simply to engage in a hindsight reconstruction of the claimed invention, using the applicant’s structure as a template and selecting elements from the references to fill the gaps.” *In re Gorman*, 983 F.2d 982, 987 (Fed. Cir. 1991). Petitioners’ arguments are built on a foundation of impermissible hindsight. For this reason alone, all Grounds fail. (Ex. 2032 at ¶ 77).

In addition to engaging in impermissible hindsight, Dr. Alpert’s blatantly contradictory opinions are unable to support an obviousness contention. Indeed, the

Federal Circuit has repeatedly held that conclusory expert testimony is inadequate to support an obviousness determination on substantial evidence review. *TQ Delta, LLC v. Cisco Sys.*, 942 F.3d 1352, 1359 (Fed. Cir. 2019). The Federal Circuit has noted that allowing unsubstantiated expert testimony “risks allowing the challenger to use the challenged patent as a roadmap to reconstruct the claimed invention using disparate elements from the prior art—i.e., the impermissible *ex post* reasoning and hindsight bias that *KSR* warned against. *TQ Delta, LLC v. Cisco Sys.*, 942 F.3d 1352, 1361 (Fed. Cir. 2019) (citing *Van Os*, 844 F.3d at 1361 (citing *KSR*, 550 U.S. at 418, 421). This is exactly what Dr. Alpert has done. Not only are his opinions conclusory, they are also contradictory. For this reason, his opinions are inadequate to support an obviousness determination.

c. Petitioners’ Motivation to Combine is Based on What a POSITA Could Have Done; Not what a POSITA Would Have Done

As previously stated, Petitioners allege that “a Skilled Artisan would have been motivated to add training to Hazelzet because it was known that training improved memory module reliability.” (Pet. at 38). This statement provides no reason for why a POSITA would be motivated to add Buchmann’s or JEDEC’s alleged training to Hazelzet. It simply states that training can improve memory module reliability. This is tantamount to saying that a POSITA would add Buchmann’s or JEDEC’s alleged training to Hazelzet because they could add

training to Hazelzet. However, Hazelzet identifies numerous, different improvements that a POSITA could implement to improve the “reliability” of its specific memory module including: “memory mirroring, symbol slicing and extensive forms of fault rejection and redundancy” as well as “error detection and/or correction methods such as CRC (Cyclic Redundancy Code), EDC (Error Detection and Correction), parity or other encoding/decoding methods suited for this purpose” and” “further reliability enhancements [that] may include operation re-try (to overcome intermittent faults such as those associated with the transfer of information), the use of one or more alternate or replacement communication paths to replace failing paths and/or lines, complement-re- complement techniques” and “the use of bus termination, on busses as simple as point-to-point links or as complex as multi-drop structures,” which “is becoming more common consistent with increased performance demands.” (Ex. 1014 at [0005], [0127], [0128]). But, what a POSITA could have done does not satisfy the legal requirement of demonstrating, with evidence, what a POSITA would have done. *Black & Decker, Inc. v. Positec USA, Inc.*, 646 Fed. Appx. 1019, 1027 (Fed. Cir. 2016); *Seabery N. Am., Inc. v. Lincoln, Global, Inc.*, IPR2016-00904, Paper 12 at 11-12; *Costco Wholesale Corp. v. Robert Bosch LLC*, IPR2016-00035, Paper 23 at 8; (Ex. 2032 at ¶ 78).

d. Hazelzet, Buchmann and JEDEC Disclose Teachings that Diverge from One Another

Petitioners ignore the fact that the teachings of Hazelzet diverge from Buchmann's and JEDEC's alleged training. As explained above, ECC and training are different solutions to a different problem. *See* Sections V.B.1 - 4, *supra*. Moreover, Hazelzet identifies numerous, different improvements that a POSITA could implement to improve "reliability" of its system—none of which include training. (Ex. 1014 at [0005], [0127], [0128]). The Federal Circuit confirms that a reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant. *In re Gurley*, 27 F.2d 551, 553, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994); *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1326 (Fed. Cir. 2009). Unlike the '218 patent, which chose training as a method to improve system reliability, Hazelzet chose ECC after contemplating numerous other techniques—none of which involved training. Accordingly, Hazelzet's teaching would lead a POSITA on a path that diverges from the one taken by the '218 patent. (Ex. 2032 at ¶ 79).

C. There is No Motivation to Create a Separate Training Mode in Hazelzet

All of Petitioners' Grounds require Buchmann's or JEDEC's alleged training to be added to Hazelzet as a new mode that is distinct from Hazelzet's normal mode of operation. (Pet. at 4, 38-39). Specifically, Petitioners argue, in a section titled "Motivation to Add Training as a Mode Separate from Normal Operations," that a POSITA "would have been motivated to combine the[] references by adding training in a mode/operation separate from normal operation" in Hazelzet. (Pet. at 38-39). However, Petitioners previously argued, and the Board agreed, that a POSITA would add training to Hazelzet's ECC mode of operation, which is a normal mode of operation. This is the exact opposite of what Petitioners currently argue. (Ex. 2032 at ¶ 80).

Specifically, Petitioners previously took the position that a POSITA would have found it obvious to add Buchmann's training to Hazelzet.

One skilled in the art would have found it obvious to implement the notification techniques of Hazelzet in the "training" schemes of Buchmann that make use of the "SBC mode" (i.e., error correcting mode). EX1017, 8:24-9:17; EX1003¶¶165, 171.

(Ex. 2015 at 62, IPR2018-00303 Petition). Petitioners' expert explained that a POSITA would find it obvious to add training into Hazelzet's ECC mode of operation (i.e., a normal mode of operation):

Because the “SBC mode” is a mode of operation where “error correcting code” is provided, Ex. 1017 (Buchmann) at 14:25-28, one skilled in the art would have found it obvious to combine the “training” schemes (e.g., “TS3: upstream lane training and repair”) described in Buchmann with the notification scheme of Hazelzet in the “ECC mode” (i.e., “second mode,” as claimed).

(Ex. 2017 at ¶171, Dr. Alpert’s IPR2018-00303 Declaration). Petitioners aver in their present petition that Hazelzet’s ECC mode is, in fact, a normal mode of operation. (Pet. at 70 (stating that Hazelzet has “parity and ECC normal operating modes”); (Ex. 2032 at ¶ 81).

The Board agreed with Petitioners’ prior position that the ECC mode of Hazelzet was a “second mode.” (Ex. 2016 at 20 (finding Hazelzet’s ECC mode to be a “second mode”) and 12 (finding that Buchmann’s training mode would be implemented in Hazelzet’s ECC mode), IPR2018-00303 FWD). The Board further credited the opinion of Petitioners’ expert as being “consistent with the prior art disclosures.” (*Id.* at 13 (citing Ex. 1003 at ¶¶121-150, 158-186)). Accordingly, Petitioners and their expert successfully argued that a POSITA would find it obvious to add training to Hazelzet’s **normal** (i.e., ECC mode) mode of operation. (Ex. 2032 at ¶ 82).

Now, in stark contrast, Petitioners and their expert attempt to argue that it would be obvious to add training as a separate mode of operation, outside Hazelzet’s normal mode of operation. (Pet. at 38-39). But, if a POSITA would have been

motivated to add training into Hazelzet's normal mode of operation (i.e., ECC mode), they could not now be motivated to do the exact opposite by adding training to Hazelzet as a separate mode from the normal mode of operation. The two options are incongruent to one another. Choosing one makes it non-obvious to choose the other. It is disingenuous for Petitioners to argue, and impossible for the Board to find, that it would now be obvious to add training as a mode distinct from Hazelzet's normal mode of operation when the exact opposite was argued and found previously. (Ex. 2032 at ¶ 83).

At best, a potential justification for Petitioners' otherwise illogical position is that Petitioners are suggesting a POSITA could have implemented training into Hazelzet in any manner. But, it is black letter law that what a POSITA **could** have done does not satisfy the legal requirement of demonstrating, with evidence, what a POSITA **would** have done. *Black & Decker, Inc. v. Positec USA, Inc.*, 646 Fed. Appx. 1019, 1027 (Fed. Cir. 2016). Petitioners clearly fail to do the latter. The more likely justification for Petitioners' and their expert's conflicting positions is that they have engaged in impermissible hindsight. See Section V.B.5.b, *supra*.

Setting aside the logical inconsistency with Petitioners' present argument that is fundamentally inconsistent with their prior view of the world, which alone is fatal to the Grounds in the petition, Petitioners gloss over the discordant reconstruction of Hazelzet that would be required to add an entirely new mode of operation to that

system. Indeed, Petitioners provide no evidence or explanation as to why the addition of an entirely new mode of operation would be obvious and straightforward. (Pet. at 38-39). The opposite is true. Adding an entirely new mode of operation would require substantial reconstruction and redesign of Hazelzet. Doing so is therefore not obvious. *In re Ratti*, 270 F.2d 810, 813 (CCPA 1959) (holding the suggested combination of references improper under §103 because it “would require a substantial reconstruction and redesign of the elements shown in [a prior art reference] as well as a change in the basic principles under which [that reference’s] construction was designed to operate”). There would not be a reasonable likelihood of success in doing this. *KSR Int’l Co. v. Teleflex Inc.*, 550 U.S. 538, 416, 82 USPQ2d 1385, 1395 (2007). This is a separate, independent reason as to why a POSITA would not be motivated, or understand how, to add training in Hazelzet as a new separate and distinct mode from Hazelzet’s normal mode of operation. (Ex. 2032 at ¶¶ 84-87).

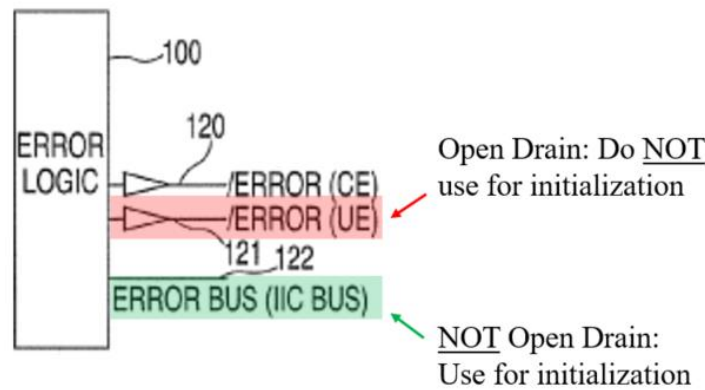
For these reasons, all of Petitioners’ Grounds fail.

D. There is No Motivation to Use Hazelzet’s Open Drain Signaling Training Notifications

All of Petitioners’ Grounds require Buchmann’s or JEDEC’s alleged training to (1) be added to Hazelzet (2) as a new mode that is distinct from Hazelzet’s normal mode of operation *and* (3) to utilize Hazelzet’s UE line. (Pet. at 4, 39-41). Petitioners

allege “it would have been further obvious to communicate training status in the new mode/operation using the same open drain output used in other modes/operations.” (Pet. at 39). However, Petitioners provide no articulated reason why a POSITA would have been motivated to do so. (Pet. at 39-41). Instead, Petitioners make a number of generic statements related to a POSITA’s ability to utilize an open drain output for multiple purposes. *Id.* This amounts to a contention that a POSITA **could** have, not **would** have, used an open drain for multiple purposes. It is legally insufficient for Petitioner to simply allege that a POSITA could use an open drain for multiple reasons. A POSITA could just as easily have reused a different pin than Hazelzet’s open drain. Why would a POSITA have been motivated to use the open drain signal—as opposed to other pins—in Hazelzet? Petitioners did not even attempt to answer the question. For good reason, Petitioners cannot. (Ex. 2032 at ¶ 88).

Hazelzet discourages use of its UE (open drain) pin during initialization. Instead, Hazelzet discloses initialization that utilizes a bus that is distinct from the UE. Specifically, Hazelzet suggests that a POSITA would use “a distinct bus, such as a presence detect bus [], an IIC bus [] and/or the SMBUS, which has been widely utilized and documented in computer systems using such memory modules.” (Ex. 1014 at [0124]). Accordingly, Hazelzet prefers use of its IIC bus instead of its UE pin.



(Ex. 1014 at Figure 4B) (annotated); Ex. 2032 at ¶ 89).

Hazelzet prefers “the use of a separate bus” because it “offers the advantage of providing an independent means for both initialization and uses other than initialization...including changes to the subsystem operational characteristics on-the-fly and for the reporting of and response to operational subsystem information such as utilization, temperature data, failure information or other purposes.” (Ex. 1014 at [0125]). In other words, Hazelzet prefers to reuse its IIC bus (not UE) for different functions—including initialization—while in its normal mode of operation. Using the IIC bus allows Hazelzet to perform initialization “on-the-fly.” (Ex. 1014 at [0125]; Ex. 2032 at ¶ 90).

Not only do Petitioners fail to muster an argument as to why a POSITA would be motivated to use Hazelzet’s UE line for training outputs, such an argument would be contrary to the teachings of Hazelzet because Hazelzet discloses utilizing the IIC bus during initialization for numerous perceived benefits and advantages. (Ex. 1014 at [0124]-[0125]). Accordingly, a POSITA would not be motivated to use Hazelzet’s

UE to communicate training status as Petitioners suggest in conclusory fashion. A POSITA would be motivated to reuse Hazelzet's IIC bus in order to improve performance, efficiency, and reliability. (Ex. 2032 at ¶ 91).

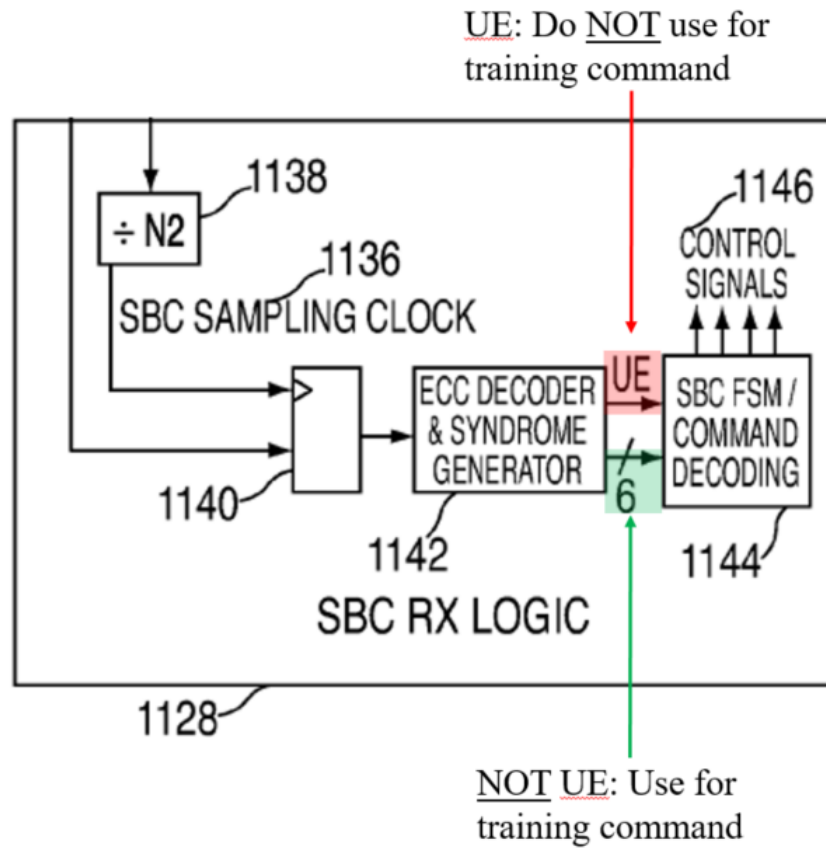
E. Claims 1-22 are not obvious over Hazelzet in view of Buchmann for Additional Reasons

For the reasons detailed above, there is no motivation to (1) add Buchmann's training to Hazelzet, (2) add Buchmann's training as a separate mode to Hazelzet, or (3) use Hazelzet's open drain signaling for Buchmann's alleged training notifications. See Sections V.B - D, *supra*. In addition to these reasons, the '218 claims are not obvious over Hazelzet in view of Buchmann for two separate reasons. More specifically, Petitioners allege that it would be obvious to output Buchmann's TS commands via Hazelzet's UE line. (Pet. at 34-36). It would not be obvious for two reasons. (Ex. 2032 at ¶ 95).

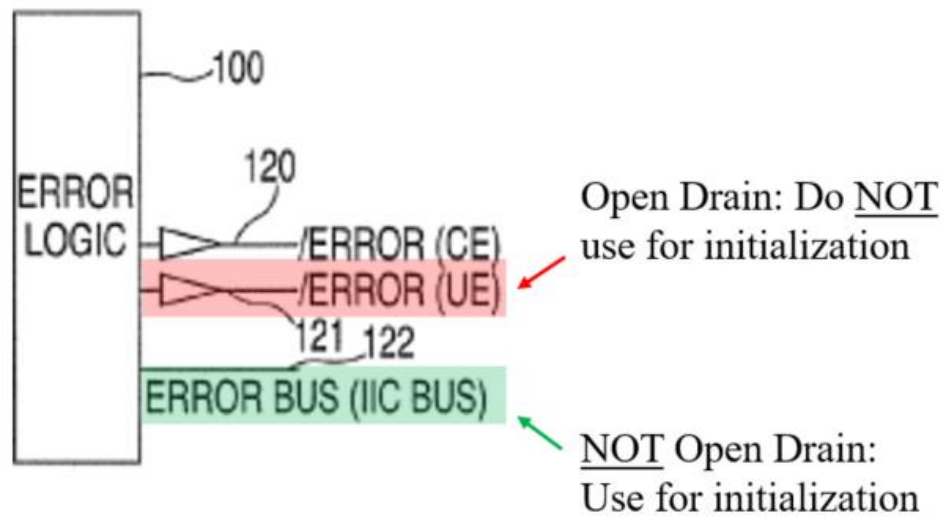
First, Petitioners rely on Buchmann's TS3 commands as being incorporated into Hazelzet. However, Petitioners' expert previously stated that Buchmann's TS3 commands "wouldn't necessarily be a very appropriate command" for Hazelzet. (Ex. 2031 at 121:6-15). Petitioners make no attempt to explain why TS3 commands would be a good fit now, and make no attempt to explain why Buchmann's TS0 commands—or any other TS command for that matter—are actually appropriate for inclusion in Hazelzet. In fact, Petitioners' expert does not even know the significance

of Buchmann's TS3 commands. (Ex. 2031 at 103:3-11). Lastly, Petitioners' expert previously testified that there are many ways Buchmann's 6-bit message could be implemented in Hazelzet, and his rationale for adding it to Hazelzet's UE line was that he did not "see a reason why the UE line couldn't be used for that purpose." (Ex. 2031 at 126:15-24). But, this is not the standard. Petitioners' and their expert's contentions amount to conclusory, unsupported, prognostication. (Ex. 2032 at ¶ 96).

Second, Petitioners allege that Buchmann's TS commands (specifically, TS0_done, TS3_ack, and TS3_done) would be obvious to output via Hazelzet's UE line in order to satisfy the claimed "associated with the one or more training sequences." (Pet. at 53). However, Buchmann includes the same UE line as Hazelzet and does not send its TS commands over it. Instead, Buchmann sends its TS commands via separate bus (annotated in green below).



(Ex. 1016 at Figure 11) (annotated). Indeed, Buchmann confirms that its TS commands are output via a different pin than its UE, and Petitioners' expert agrees that Buchmann's UE line does not communicate Buchmann's commands. (Ex. 2031 at 106:20-107:11; 108:6-14; 124:17-19). Similarly, Hazelzet teaches the use of an IIC bus—not UE—for initialization.



(Ex. 1014 at Figure 4B) (annotated); Ex. 2032 at ¶ 97).

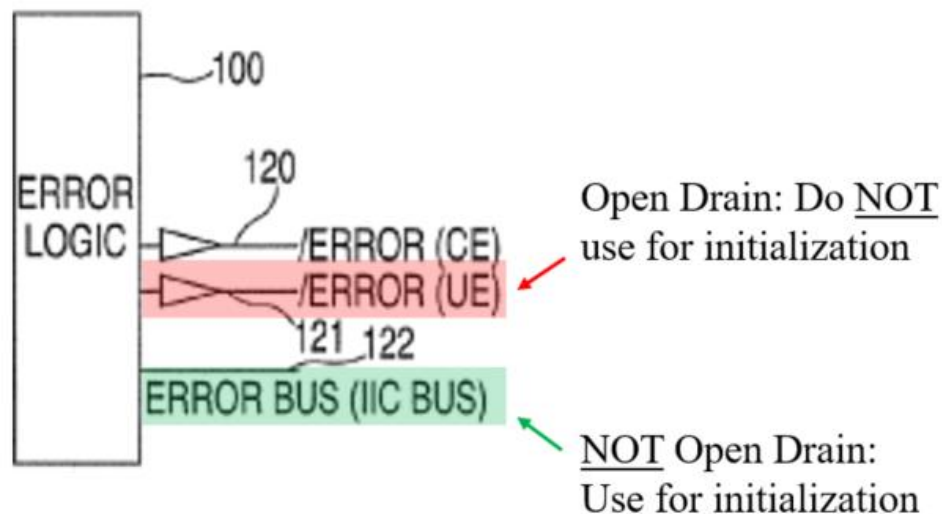
Accordingly, both Buchmann and Hazelzet disclose teachings that diverge from the '218 claims. The modification and combination proposed by the Petition do not make the '218 claims obvious; they actually teach away from the '218 claims. In re Gurley, 27 F.2d 551, 553, 31 USPQ2d 1130, 1131 (Fed. Cir. 1994); DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc., 567 F.3d 1314, 1326 (Fed. Cir. 2009); Ex. 2032 at ¶ 98).

F. Claims 1-22 are not obvious over Hazelzet in view of JEDEC for Additional Reasons

As a preliminary matter, JEDEC is not prior art to the '218 patent. See Sections III.A.1 - 4, *supra*. Further, for the reasons detailed above, there is no motivation to (1) add JEDEC's training to Hazelzet, (2) add JEDEC's training as a separate mode to Hazelzet, or (3) use Hazelzet's open drain signaling for JEDEC's alleged training notifications. See Sections V.B - D, *supra*. In addition to these

reasons, the '218 claims are not obvious over Hazelzet in view of JEDEC for two separate reasons. (Ex. 2032 at ¶ 92).

First, Petitioners allege that a POSITA would use Hazelzet's UE line to output JEDEC's alleged training notifications. (Pet. at 33-36). However, Hazelzet teaches away from doing this. Specifically, Hazelzet prefers to perform initialization via a separate, distinct bus, like "an IIC bus (such as defined in published JEDEC standards such as the 168 Pin DIMM family in publication 21-C revision 7R8). (Ex. 1014 at [0124]). Even if it were obvious to add JEDEC's training to Hazelzet—and it is not—Hazelzet specifically teaches that JEDEC's IIC bus should be used. Hazelzet also includes an IIC bus that is different than its UE line.



(Ex. 1014 at Figure 4B) (annotated). Because Hazelzet and JEDEC both include an IIC bus, and Hazelzet specifically discloses that JEDEC's IIC bus should be used for initialization, a POSITA would not be motivated to implement JEDEC's

alleged training via Hazelzet's UE line. Hazelzet has a good reason for utilizing the IIC bus:

The use of a separate bus, such as described in the embodiment above, also offers the advantage of providing an independent means for both initialization and uses other than initialization, such as described in U.S. Pat. No. 6,381,685 to Dell et al., of common assignment herewith, including changes to the subsystem operational characteristics on-the-fly and for the reporting of and response to operational subsystem information such as utilization, temperature data, failure information or other purposes.

(Ex. 1014 at [0125]).

There is no reason to use Hazelzet's UE line. (Ex. 2032 at ¶ 93).

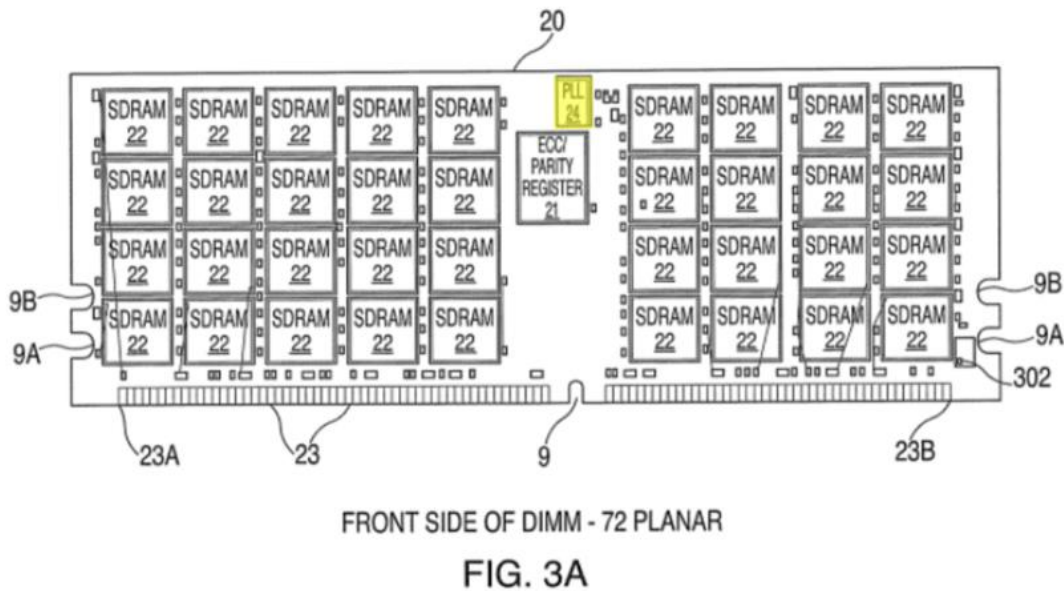
Second, Hazelzet's memory module does not have memory buffers, which would cause timing issues and which hides the memory devices from the memory bus, a problem JEDEC's alleged training aims to address. Thus, a POSITA would not be motivated to add JEDEC's training to Hazelzet in the first place, let alone trying to perform JEDEC's training in Hazelzet's ECC/Parity register, which is where Hazelzet's UE line resides. Hazelzet at Figure 4A and 4B. Instead, a POSITA would understand that a PLL or DLL component was the most obvious choice to perform training.

Based on various design choices that a POSITA would consider, synchronization circuitry can be implemented using digital or analog, open or closed loop methodologies or any combination thereof. The two most common synchronization circuits used are the delay-locked loop (DLL) and the phase-locked loop (PLL). The DLL is widely used in memory interfaces for its simplicity and good jitter performance.

An alternative approach is the PLL, which is usually found in communication systems and microprocessors for clock data recovery and frequency synthesis.

(Ex. 2029 at 252).

Since Hazelzet includes a DLL, that component would be the logical component to perform training, not the ECC/Parity register.



(Ex. 1014 at Figure 4B) (annotated). For at least these reasons, a POSITA would not be motivated to implement JEDEC's training on Hazelzet's UE line. (Ex. 2032 at ¶ 94).

VI. Conclusion

For the foregoing reasons, the Board should find the challenged claims patentable.

Dated: March 11, 2021

Respectfully submitted,

Netlist, Inc.,
By its attorneys,

/ William A. Meunier /

William A. Meunier (Reg. No. 41,193)
Serge Subach (Reg. No. 74,652)
Matthew S. Galica (*pro hac vice* filed)
Andrew H. DeVoogd (*pro hac vice* filed)
MINTZ, LEVIN, COHN, FERRIS,
GLOVSKY AND POPEO, P.C.
One Financial Center
Boston, MA 02111
Telephone: 617-542-6000
Facsimile: 617-542-2241
E-mails: WAMeunier@mintz.com
SSubach@mintz.com
MSGalica@mintz.com
AHDeVoogd@mintz.com

CERTIFICATE OF WORD COUNT

Pursuant to 37 C.F.R. §42.24(d), Patent Owner hereby certifies, in reliance on the word count of the word-processing system (Microsoft Office Word 2016) used to prepare this response, that the number of words in this paper is 12,206. This word count excludes the tables of contents, tables of authorities, certificate of word count, certificate of service, and table of exhibits.

Dated: March 11, 2021

/William A. Meunier/

William A. Meunier (Reg. No. 41,193)

CERTIFICATE OF SERVICE

I certify that a copy of Patent Owner's Response is being served by
electronic mail on the following counsel of record:

Lead Counsel

Joseph A. Micallef
jmicallef@sidley.com
Reg. No. 39,772
Sidley Austin LLP
1501 K Street, N.W.
Washington, D.C. 20005
Telephone: 202-736-8492
Facsimile: 202-736-8711

Backup Lead Counsel

Michael D. Hatcher
mhatcher@sidley.com
Reg. No. 47,636
Sidley Austin LLP
2021 McKinney Ave #2000
Dallas, TX 75201
Telephone: 214-981-3428
Facsimile: 214-981-3400

Dated: March 11, 2021

/William A. Meunier/

William A. Meunier (Reg. No. 41,193)
MINTZ, LEVIN, COHN, FERRIS, GLOVSKY
& POPEO, P.C.