

1 UNITED STATES PATENT AND TRADEMARK OFFICE
2 BEFORE THE PATENT TRIAL AND APPEAL BOARD
3 CASE NO. IPR2020-01044
PATENT 9,858,218

4 SK HYNIX INC., and SK HYNIX
5 AMERICA INC.,

6 Petitioner(s),

7 vs.

8 NETLIST INC.,

9 Respondent(s).

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15 REMOTE DEPOSITION UNDER ORAL EXAMINATION OF

16 DR. DONALD ALPERT

17 DATE: March 10, 2021

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25 REPORTED BY: MICHAEL FRIEDMAN, CCR

1 TRANSCRIPT of the remote deposition of
2 the witness, called for Oral Examination in the
3 above-captioned matter, said deposition being taken
4 by and before MICHAEL FRIEDMAN, a Notary Public and
5 Certified Court Reporter of the State of New Jersey,
6 at WEBEX VTC, ALL PARTIES REMOTE, on March 10, 2021,
7 commencing at approximately 11:27 in the morning.

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1 A P P E A R A N C E S:

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3 MINTZ LEVIN
4 One Financial Center
5 Boston, MA 02111
6 BY: SERGE SUBACH, ESQ.
7 Attorneys for Respondent

8 SIDLEY AUSTIN
9 1501 K Street, NW
10 Washington, DC 20005
11 BY: MICHAEL D. HATCHER, ESQ.
12 BRIAN NESTER, ESQ.
13 Attorneys for Petitioner

14

15 ALSO PRESENT: JOSE RIVERA, Videographer

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I N D E X

WITNESS NAME	PAGE
DR. DONALD ALPERT	
By Mr. Subach	8

* * * * *

E X H I B I T S

EXHIBIT NO.		PAGE
1	US Provisional App 61186799	15
2 – 3	Alpert Declaration 218, Alpert Declaration 595	40
4	US Patent Publication 20080098277	48

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Deposition Support Index

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5 Direction to Witness Not to Answer

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None

9 Request for Production of Documents

Page	Line	Page	Line	Page	Line
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None

13 Stipulations

Page	Line	Page	Line	Page	Line
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None

17 Questions Marked

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None

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1 THE COURT REPORTER: My name is
2 Michael Friedman, a Certified Shorthand
3 Reporter. This deposition is being held
4 via videoconferencing equipment.

5 The witness and reporter are not in
6 the same room. The witness will be
7 sworn in remotely pursuant to agreement
8 of all parties. The parties stipulate
9 that the testimony is being given as if
10 the witness was sworn in person.

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1 THE VIDEOGRAPHER: We are now on
2 record. This is the remote video
3 recorded deposition of Dr. Donald
4 Alpert. Today is Wednesday, March 10,
5 2021. The time is now 11:27 a.m. in the
6 Eastern time zone.

7 We are here in the matter of
8 SK Hynix, Inc. versus SK Hynix America,
9 Inc. versus Netlist, Inc.

10 My name is Jose Rivera, remote
11 video technician on behalf of Gregory
12 Edwards LLC.

13 At this time, will the reporter
14 Michael Friedman, on behalf of Gregory
15 Edwards LLC, please swear in the
16 witness.

17 ///

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1 D R. D O N A L D A L P E R T,

2 called as a witness, having been first
3 duly sworn according to law, testifies as follows:

4

5 EXAMINATION BY MR. SUBACH:

6 Q Good morning, Dr. Alpert?

7 A Good morning.

8 Q My name is Serge Subach. I'm from
9 the law firm of Mintz Levin.

10 How are you today?

11 A Oh, I'm good over here, thank you.
12 Hope you're fine, too.

13 Q Great. I am.

14 I understand you've been deposed
15 before.

16 Is that correct?

17 A Yes, that's correct, it is.

18 Q About how many times?

19 A You know, just off the top of my
20 head, I'd say potentially 20 times, probably
21 somewhere around that number.

22 Q All right. So you're a veteran.

23 So you're likely familiar with the basics.

24 But nonetheless, I would like to run through
25 just some ground rules to make sure that

1 we're on the same page.

2 Is that all right?

3 A Oh, for sure, yes.

4 Q As you know, your testimony today
5 is under oath as if it were being taken
6 before a judge or judges who will preside
7 over this proceeding.

8 Do you understand that?

9 A Yes.

10 Q And it's likely your testimony
11 today will be presented to the judge or
12 judges.

13 Do you understand that?

14 A Yes.

15 Q So is there any reason that you are
16 unable to testify truthfully and to the best
17 of your ability today?

18 A No, there's no reason that would
19 prevent me from testifying as you mentioned.

20 Q I'm going to ask you a series of
21 questions today.

22 If you don't understand the
23 question, can you please ask me to clarify?

24 A Yes, I will.

25 Q If you do answer the question, I'll

1 assume that you understood my question.

2 Does that sound good?

3 A I understand that's the way the
4 process works, so I will ask for
5 clarification if I have any doubts.

6 Q Perfect. If you need to take a
7 break, just let me know. If we have a
8 question pending, I would ask that we wrap up
9 that question and then we can take a break.

10 Is that all right?

11 A Yes, that's fine.

12 Q And because the deposition today is
13 being transcribed, it's important that all
14 answers are verbal and there are no gestures.

15 Does that sound okay?

16 A Yes. I'm familiar with that.

17 Q Your attorney may object from time
18 to time today, but you're still obligated to
19 answer the question unless you're
20 specifically instructed by your counsel not
21 to answer.

22 Do you understand that?

23 A Yes. I think that sounds fine.

24 MR. HATCHER: Serge, I don't know
25 when you're going to finish with the

1 prelims and then get into the substance.

2 Before you are get into the substance,

3 can you go over what is on the screen

4 now and how to switch back and forth?

5 It looks like there's a way, at least

6 for me, to say Exhibit 1, Exhibit 2,

7 Exhibit 3. And when I change it, I

8 don't know if it's changing the view on

9 everybody else's screen or if it's just

10 mine. So if you can just walk both the

11 witness and me through how it works, I

12 would appreciate that. I haven't done a

13 depo yet on WebEx before. I've used

14 other platforms, but not this one.

15 MR. SUBACH: When I get to the

16 exhibits, we'll go off the record and we

17 can do a tutorial for you, Mike.

18 MR. HATCHER: Okay. Not just me

19 too, but Donald.

20 A And I do have a second screen, but

21 we can talk about it at that point.

22 MR. HATCHER: Okay. Thank you.

23 Q Dr. Alpert, are you serving as an

24 expert for petitioners in the present IPRs?

25 A Yes, I am.

1 Q And you're here today to discuss
2 certain opinions that you've rendered in the
3 form of an expert declaration submitted in
4 support of petitioners for interparty review
5 of U.S. Patent Number 9,858,218 and U.S.
6 Patent Number 10,474,595.

7 Is that correct?

8 A Well, yes. I'm here, and in terms
9 of the patent numbers, I can read the first
10 one on screen, and I don't remember the
11 second.

12 But the '595, I'm familiar with.

13 Q Okay. Just for ease of our
14 conversation today, will you understand that
15 if I say the '218 patent, I'm referring to
16 patent number 9,858,218?

17 A Yes, I will.

18 Q And likewise, if I say the '595
19 patent, I'm referring to patent number
20 10,474,595?

21 A Yes, I will.

22 Q Thanks. And are you fully prepared
23 to discuss those opinions from your
24 declarations today?

25 A Yes, I am.

1 Q Do you have any opinions relating
2 to the patentability of the '218 or the '595
3 patents that are not contained in your expert
4 declarations?

5 A No, none that I can -- you know,
6 that I formed and I can think of as I'm
7 sitting here now.

8 Q Are there any relevant facts or
9 analysis that you relied on in forming the
10 opinions in your expert declarations that are
11 not referenced or contained within your
12 expert declarations?

13 A I just want to avoid getting
14 confused with a double negative, but -- so
15 let me just say that all the facts that I
16 relied upon are explained or referred to in
17 the declarations.

18 Q Okay. Thank you.

19 So, to clarify, are there any
20 documents that you relied on in forming your
21 opinions with respect to the patentability of
22 the '218 or '595 patents that are not cited
23 in your expert declaration?

24 A No, there are none.

25 Q Approximately what percentage of

1 your expert declaration did you write
2 yourself?

3 A Well, I think -- I think that would
4 be hard for me to say at this point. There
5 was certainly portions where I made a first
6 draft, where the attorneys made a first
7 draft, and then a considerable amount of
8 editing.

9 So I don't think I can give you an
10 informed number.

11 Q Would you say it's greater than
12 50 percent or less than 50 percent?

13 A I would have to say, you know, at
14 this point, I certainly don't recall. It was
15 drafted, I think, about nine months ago, if I
16 remember.

17 So I don't remember quantitatively.

18 Q Sitting here today, do you have any
19 concerns about the accuracy of your expert
20 declarations?

21 A No, no concerns.

22 Q Are there any aspects of the
23 declarations that you consider to be
24 incomplete?

25 A No, nothing. Nothing I'm aware of

1 that's incomplete.

2 Q So is it correct that sitting here
3 today, there are no changes that you would
4 make with respect to your analysis or
5 conclusions that are in your expert
6 declarations?

7 A Yes, that's correct. I have no
8 changes to make.

9 Q Okay. Let's go off the record for
10 a few minutes to do the demo.

11 THE VIDEOGRAPHER: Stand by. The
12 time is 11:36 a.m. and we're going off
13 the record.

14 (Brief recess taken.)

15 THE VIDEOGRAPHER: Stand by. The
16 time is 11:41 a.m. and we're back on
17 record.

18 Q I'm going to introduce what has
19 been labeled as Exhibit 1.

20 (Whereupon the above mentioned was
21 marked for Identification.)

22 Q It should be on your screen,
23 Dr. Alpert.

24 Do you see it?

25 A I see something on the screen. I

1 don't recognize what it is yet.

2 Q Sure. Take a moment to flip
3 through it.

4 A Oh, yeah, okay. Thank you. It's
5 obvious, but thank you for reminding me.

6 Q I can say that this is Exhibit 1008

7 --

8 A Okay.

9 Q -- that is attached to the
10 petition?

11 A I do have a paper copy of that
12 here, so that's -- I mean, I assume we're
13 going to ask questions about this, so I will
14 grab that and put it at hand.

15 Okay. So I do recognize this.

16 Q Great. And is this the provisional
17 application to both the '218 and '595 patents
18 which was cited as Exhibit 1008 throughout
19 your declaration?

20 A Yes.

21 Q I'm going to turn your attention to
22 Page 22 of this exhibit. Please let me know
23 when you're there.

24 A Okay. I am. I'm looking at the
25 paper copy in case that's relevant, but I am.

1 Q That's fine.

2 A Yeah, I'm there. Sorry.

3 Q Thank you.

4 Towards the bottom of the page, in
5 the second-to-last paragraph, the last couple
6 of sentences in there, is a passage that I
7 would like to point you to.

8 It reads, "In the notifying method,
9 the memory subsystem controller sends a
10 signal to the MCH when it completes the
11 required or requested operation. This method
12 allows the MCH to execute independent command
13 while it is waiting for a notification signal
14 for the memory subsystem controller."

15 Do you see that passage?

16 A Yes.

17 Q Did I read that accurately?

18 A Yes.

19 Q What does that passage mean to you?

20 A (Witness reviewing.)

21 Well, it's -- it starts out, it's
22 describing something that's in the patent
23 called a "notifying method." And it says
24 that the memory system, subsystem controller
25 that sends the signal to the MCH would be the

1 memory controller hub when it completes the
2 required or requested operation.

3 So that's indicating that there's a
4 signal, a notifying signal that's sent from
5 the memory subsystem controller to the MCH
6 when there's an operation that's completed.
7 And it does explain that the method allows
8 the MCH to execute other commands -- it says
9 "independent command" -- while it's waiting
10 for the notification signal.

11 So it's explaining one -- one
12 method of communication between the memory
13 subsystem controller and the MCH.

14 Q Okay. And I'd like to focus you
15 specifically on that last sentence that
16 recites, "This method allows the MCH to
17 execute independent command while it's
18 waiting for a notification signal for the
19 memory subsystem controller."

20 Do you see that sentence?

21 A Yes.

22 Q What does it mean when it says "the
23 MCH is allowed to execute independent
24 commands?"

25 A Well, what it says is the MCH has

1 sent a command to a memory subsystem
2 controller, and that while it's waiting for a
3 response from that controller, the MCH can
4 perform other operations, including executing
5 unrelated commands.

6 Q What other operations could it be
7 performing?

8 A Well, it could be performing other
9 operations to the same memory system
10 controller for the memory subsystem
11 controller, or it could certainly be
12 performing various operations to a different
13 memory subsystem controller.

14 Q So it's your understanding that,
15 based on this disclosure, it means that the
16 MCH is allowed to execute commands
17 independent from the memory subsystem
18 performing the required or requested
19 operations.

20 Is that correct?

21 A Yes. And in particular, you know,
22 I understand you're asking how this would be
23 interpreted by a person of ordinary skill in
24 the art at the time of the disclosure.
25 That's the context in which I was answering.

1 That's just, you know, how I interpret it.

2 But I'm trying to look at it from the vantage
3 of a person of ordinary skill in the art.

4 But I do agree with what you said.

5 Q Thanks. I understand that
6 clarification.

7 So the MCH would be performing
8 those independent commands with another
9 memory module that is not the memory module
10 performing the required or requested
11 operation.

12 Is that correct?

13 A Yes. That's one example, I think,
14 that falls under what's disclosed here.

15 Q And when the MCH is performing
16 those commands independent from the memory
17 subsystem performing the required or
18 requested operations, it would not be
19 performing commands with the memory subsystem
20 that it is performing the required or
21 requested -- scratch that question, actually.

22 MR. HATCHER: I was about to
23 object.

24 Q So in one of the scenarios that is
25 disclosed here in this passage, the MCH is

1 executing required and requested operations
2 for a first module, for example.

3 Are you with me still? Do you
4 agree?

5 A (Witness reviewing.)

6 Yeah, I believe that's covered by
7 the first sentence you pointed me to, that
8 the memory system -- but that would be what
9 initiates the operation by the memory
10 subsystem controller that's going to send a
11 signal to the MCH.

12 Q Right. I think I might have
13 misspoken in that -- in that last question.

14 So the memory subsystem controller
15 is performing the required and the requested
16 operations. And when it's complete, it sends
17 a signal to the MCH.

18 Is that right?

19 A Yes. That's what's disclosed here.

20 Q And during that time while the MCH
21 is waiting, the MCH may execute independent
22 commands on another memory module, for
23 example.

24 Is that correct?

25 A Yes. For example, on another

1 memory module or potentially to the same
2 memory module.

3 Q And while it is waiting for that
4 signal from the memory subsystem controller,
5 it is not performing commands with that
6 memory subsystem controller.

7 Is that correct?

8 A I would disagree. I don't -- I
9 don't believe that's disclosed here.

10 Q How would the MCH perform commands
11 independent from the memory subsystem which
12 is performing the required or requested
13 operations if the memory subsystem in that
14 moment is performing the required or
15 requested operation?

16 A Well, in general, the operations
17 that are requested by the MCH, you know, can
18 be pipelined. So it would be actually quite
19 common to send one command to the memory
20 controller, and before that command is
21 complete, to be sending the next command to
22 the controller.

23 Q But that isn't disclosed in this
24 passage that we have on Page 22 of
25 Exhibit 1008.

1 Right?

2 A No, it's -- it's not disclosed
3 there. But that would be certainly within
4 the general knowledge and understanding of a
5 person of skill in the art for any SD-RAM and
6 even going way back to certain of the
7 asynchronous D-RAMs that came before.

8 Q So you're saying, based on the
9 disclosure here, when the memory subsystem
10 controller is performing the required or
11 requested operations, and during that time
12 while the MCH is waiting for the signal that
13 the required or requested operations are
14 complete, during that time while the MCH is
15 waiting, it could also be performing
16 operations for that same memory subsystem
17 controller?

18 A I just want a little clarification.
19 I was following the whole thing, and talking
20 about both the MCH and the memory subsystem
21 controller. And at some point in the
22 question you said "it." And if -- you can
23 probably read it back.

24 It was just a little bit unclear to
25 me what "it" referred to. So if you wouldn't

1 mind, if you want to continue with the
2 question, just to clarify that a little more?

3 Q Sure. Let me try again.

4 Based on the disclosure here, when
5 the memory subsystem controller is performing
6 the required or requested operations, and
7 during that time while the MCH is waiting for
8 the signal that the required or requested
9 operations are complete, during that time
10 while the MCH is waiting, it can also be
11 performing operations -- scratch that. I
12 said "it" again.

13 A Uh-huh.

14 Q Let me try one more time.

15 A Sure.

16 Q Based on the disclosure here, when
17 the memory subsystem controller is performing
18 the required or requested operations, and
19 during that time while the MCH is waiting for
20 the signal that the required or requested
21 operations are complete, during that time
22 while the MCH is waiting, the MCH could also
23 be performing operations for that same memory
24 subsystem controller.

25 Is that correct?

1 A Yes, that's correct. That would
2 be -- that would certainly be the knowledge
3 of a person of ordinary skill in the art and
4 it's consistent with the disclosure here.

5 Q And how would the MCH be doing that
6 while it's waiting?

7 A Well, as I mentioned, in general,
8 the commands can be pipelined. And so, there
9 can be, you know, a second independent
10 command that would be sent from the MCH to
11 that same memory subsystem controller, and
12 that could be executed either, like I said,
13 in a pipeline fashion or in parallel with the
14 first command.

15 Q Okay. Let's take a look at
16 Exhibit 1.

17 A Actually, I hate to shut you off,
18 but we talked about this specific, you know,
19 couple of sentence. And I did want to
20 mention that I have worked on this
21 same -- well, actually, this is the
22 provisional.

23 But in general, it's talking about
24 three different methods of what they
25 call -- I don't know, "handshaking" or

1 something, but actually one without
2 "handshaking" where the MCH waits for a
3 specific amount of time to note if the
4 operation is complete.

5 Another where the MCH would be
6 doing something called "polling," or going
7 out and, for example, reading a status
8 register to determine whether the operation
9 is complete, or in the case that's described
10 here, of sending a signal.

11 And I did just want to mention that
12 in my experience, and I think also as a
13 person of ordinary skill in the art looking
14 at this would -- would, in fact, understand
15 that in any of those three methods, it is
16 possible for the MCH to execute independent
17 commands while the first command was still in
18 execution.

19 Q Okay. Thank you.

20 Let's take a look at the same
21 exhibit, Exhibit 1, which is Exhibit 1008.

22 A Oh, yes. Sorry. Okay.

23 Q Let's take a look at Figure 3.,
24 which is on Page 25.

25 Please let me know when you're

1 there.

2 A Oh, yeah, I'm there.

3 Q Do you see the description on the
4 bottom of the figure?

5 A I see there's some text at the
6 bottom, yes.

7 Q Do you see where it says, "error
8 out pin load during MB training, high signal
9 indicates that training is done."

10 Do you see that part of it,
11 Dr. Alpert?

12 A Yes.

13 Q And then it goes on to say, "High
14 during normal operation unless a parity error
15 occurs."

16 Do you see that?

17 A Yes, I do.

18 Q All right. So focusing on just the
19 first part, do you agree that the error out
20 pin will be high when training is done?

21 A Yes. It says that the error out
22 signal will be high when the training is
23 done.

24 Q And so what does that mean to you?

25 A I'm a little bit at a -- at a loss,

1 only just because it seems to be, you know,
2 clear in its statement.

3 I don't know if there's any more
4 specific question you have?

5 Q Yes. Based on this disclosure,
6 what happens when training is done?

7 A When training is done, that the
8 signal on the error out pin would go from low
9 to high.

10 Q And if training is done, does that
11 mean that the module enters normal operation?

12 A (Witness reviewing.)

13 You know, at the moment, sitting
14 here right now, I don't recall whether
15 the -- the specification discloses that it
16 necessarily enters normal mode of operation
17 when the training is done.

18 Q Well, let's take a look at the
19 second line. It says that -- or rather, do
20 you agree that the error out pin will be high
21 during normal operation?

22 A Well, it says "unless a parity
23 error occurs."

24 Q Correct. So do you agree that
25 unless a parity error occurs, the error out

1 pin will be high during normal operation?

2 A Yes. That's what it says.

3 Q So, then, when the memory subsystem
4 is in normal operation, the high signal only
5 provides information related to the normal
6 operation.

7 Is that correct?

8 A It would provide information about
9 the memory reads and writes or other commands
10 that were occurring in normal mode. I
11 think -- is that -- does that address your
12 question?

13 Q I'm referring specifically to
14 the -- to the error out pin, which we agreed
15 is high during normal operation unless a
16 parity error occurs.

17 Are you still with me on that?

18 A Yes.

19 Q Okay. So when the memory subsystem
20 is in normal operation, the high signal from
21 the error out pin only provides information
22 related to normal operations.

23 Is that correct?

24 A (Witness reviewing.)

25 I'm just sitting here thinking and

1 the concern that I have -- let me just put it
2 out there, maybe there's a follow-up
3 question -- is the error out signal is
4 actually shared between -- as shown in
5 Figure 3 is shared between two DIMMs.

6 And so, you know, the patent talks
7 about and a person of ordinary skill would
8 understand that you know, a DIMM could either
9 be in a normal operating mode or in an
10 initialization mode. Those are the two modes
11 that the patent talks about.

12 And so, you know, I think that the
13 person of ordinary skill in the art would
14 understand that it's possible the two DIMMs
15 could be in those two different modes. And
16 so, therefore, if one of them is in normal
17 operating mode and the other one is in the
18 initialization mode, then it's -- it's not
19 necessarily, you know, clear what exactly the
20 error out would be indicating.

21 Q So I think I'm -- I'm asking
22 specifically with respect to a single DIMM.
23 The single DIMM depicted here, any of the
24 two, the single DIMM depicted here has an
25 error out pin.

1 Is that right?

2 A Yes.

3 Q And according to the disclosure
4 here, that error out pin will be high during
5 normal operation unless a parity error
6 occurs.

7 Do you agree?

8 A Yes. That's what it clearly says
9 here.

10 Q So, then, when a -- when a DIMM is
11 in a normal operation, the high signal on the
12 error out pin only provides information
13 related to normal operations.

14 Is that correct?

15 MR. HATCHER: Objection, form.

16 A I would say yes, for a particular
17 DIMM, when it's operating in the normal mode,
18 then the error out is indicating whether a
19 parity error occurred in the normal mode.

20 Q So, in the normal mode, the high
21 signal over the error out pin does not relate
22 to training.

23 Is that correct?

24 MR. HATCHER: Objection, form.

25 A I would say it's possible to do

1 certain types of training in normal -- normal
2 operating mode. So I don't -- I don't think
3 I can say it never refers to training, even
4 if you're in normal operating mode.

5 Q Okay. Specifically looking at the
6 disclosure here, we have that on a -- on an
7 individual DIMM, during training, the high
8 signal over the error out pin indicates that
9 training is done.

10 Do you agree with that?

11 A Yes, it does indicate that the
12 training is done.

13 Q And after training is done as to an
14 individual DIMM, the error out pin -- or
15 rather, the high signal over the error out
16 pin during the normal operation -- scratch
17 that last part -- as to an individual DIMM,
18 the error out pin has a high signal during
19 normal operation unless a parity error
20 occurs.

21 Do you agree with that?

22 A Yes. That's what it says here.

23 Q So as to an individual DIMM, during
24 normal operation, a high signal over the
25 error out pin does not relate to training.

1 Is that correct?

2 MR. HATCHER: Objection, form.

3 Asked and answered, misstates testimony.

4 A Yeah, I -- you know, I think a
5 person of ordinary skill in the art looking
6 at the statements that you've been pointing
7 to would not understand that the -- that the
8 MB training is -- that in the first
9 statement, that necessarily includes all of
10 the MB or memory buffer training, nor does it
11 indicate that -- that there's no memory
12 buffer training.

13 And similarly, it doesn't indicate
14 to a person of ordinary skill in the art that
15 there's no training that occurs during the
16 normal operating mode.

17 Q So a person of ordinary skill in
18 the art might read this and understand there
19 are multiple different types of training?

20 A Yes.

21 MR. HATCHER: Objection, form.

22 Q Let's try to come at this a
23 slightly different way.

24 Going back to the first line of
25 that error out pin disclosure here under

1 Figure 3, it says that "the error out pin is
2 low during MB training. High signal
3 indicates that training is done."

4 Do you see that part?

5 A Yes.

6 Q Does this mean that the memory
7 modules performing MB training can output a
8 low signal during the MB training?

9 Is that correct?

10 A Yes, it can.

11 Q And that, then, a high signal can
12 indicate that training is done.

13 Is that correct?

14 A Yes. It indicates that the
15 training is done, and I -- I actually kind of
16 want to add one clarification to that, going
17 back to an earlier question I believe you'd
18 asked, whether when the training is done, it
19 transitions to the normal operating mode.

20 And as we're going through this, I
21 was recalling that, in fact, the patent
22 identifies two operating modes; a normal
23 operating mode and an initialization mode.

24 And so, in particular, I think that
25 when the DIMM indicates that training is

1 done, it may still continue in the
2 initialization mode and not necessarily
3 transition to the normal operating mode.

4 Q Understood. But as disclosed here,
5 during MB training, the high signal can
6 indicate that the training is done.

7 Is that correct?

8 A Yes.

9 Q Let's flip to Page 23 of this
10 exhibit, Exhibit 1 of this deposition, and
11 Exhibit 1008 to the petition.

12 Please let me know when you're
13 there.

14 A I am there, yes.

15 Q I'd like to focus you on a
16 paragraph that looks to be right in the
17 middle of the page. It begins with Figure 3.

18 Do you see that?

19 A Yes.

20 Q And this passage describes the
21 figure we were just looking at.

22 Is that right?

23 A Yes, Figure 3.

24 Q I want to focus you on the second
25 sentence of that paragraph, which recites,

1 "The output of the notifying signal is low
2 impedance while the memory subsystem
3 controller executing each section of the
4 initialization step."

5 Did I read that correctly?

6 A Yes.

7 Q What does that passage mean to you
8 as a person of ordinary skill in the art?

9 A (Witness reviewing.)

10 Well, it's saying that during
11 initialization, in the entirety of the
12 initialization, that the -- that the signal
13 is low impedance, which would mean that the
14 transistor is on and it's pulling that signal
15 to a low level.

16 Q In reading that passage, do you
17 understand that the output of the notifying
18 signal is low for each section of the
19 initialization step?

20 A Yes. That's what it says here.

21 Q So does that mean, in relation to
22 some MB training operations, the notifying
23 signal will be low?

24 A If that training occurs during
25 initialization.

1 Q Let's look at the next sentence,
2 the second-to-last sentence of that same
3 paragraph, which recites, "As the memory
4 controller completes each step, it drives the
5 notifying signal pin to the high impedance
6 state."

7 Did I read that correctly?

8 A Yes, that's right.

9 Q What does that passage mean to you
10 as a person of ordinary skill in the art?

11 A Well, it indicates that as each
12 step is completed, it says it drives the pin
13 to a high impedance state, meaning the
14 transistor that's shown in Figure 3 for one
15 of the DIMMs would be turned off.

16 Q So does that mean that in relation
17 to other MB training operations, the
18 notifying signal will be high?

19 MR. HATCHER: Objection, form.

20 A Yeah, I'm not -- I'm not sure I
21 understand the question.

22 Maybe you can rephrase it or give
23 it a little more context?

24 Q So if we look at Figure 3 again,
25 the disclosure directly underneath Figure 3

1 states that "the error out pin is low during
2 MB training."

3 Do you see that?

4 A Yes.

5 Q According to this disclosure, can
6 the signal be high during MB training?

7 A (Witness reviewing.)

8 I don't see that it precludes, you
9 know, certain type of training,
10 where -- where it was high. But I don't -- I
11 don't see -- I don't see that alternative
12 operation disclosed here.

13 Q So as it's disclosed here, if the
14 first DIMM is in training, it's error out pin
15 will have a low signal.

16 Is that correct?

17 A It will have a low signal, at least
18 during some MB training. I think you're
19 asking me whether it's under all MB training,
20 is that, perhaps -- or maybe I'm
21 misunderstanding the question?

22 Q I'm saying during MB training as
23 it's disclosed here, the signal from that
24 particular DIMM over the error out pin will
25 be low.

1 Is that correct?

2 A I would say it's true during some
3 MB training. It certainly -- I believe
4 that's the way a person of ordinary skill in
5 the art would understand that.

6 Q And so while the first LR
7 DIMM -- sorry. Scratch that.

8 While the first DIMM is in
9 MB training, and the second one is in normal
10 mode, or normal operation, the error out
11 signal from the one that's in normal
12 operation will be high relative to the error
13 out signal from the DIMM which is in
14 MB training.

15 Is that correct?

16 A No. I wouldn't describe it exactly
17 that way.

18 Q How would you describe it?

19 A Well, the -- first of all, I
20 believe a person of ordinary skill in the art
21 would understand that if error out is a
22 digital signal, it would either be high or
23 low, and that it would be high when neither
24 of the DIMMs is in the so-called low
25 impedance state or has the transistor on.

1 It would be low when either of them
2 has the transistor on, and it would be high
3 when neither of them has the transistor on.

4 And so, therefore, if one of the
5 DIMMs were in training and driving the error
6 out low, then it would be impossible for the
7 other DIMM to drive the signal high.

8 Q Your answer is from the perspective
9 of the MCH.

10 Is that correct?

11 A No. More generally, it would be
12 just a matter of -- you know, there's a
13 signal called "error out" that connects to
14 each of the pins on the DIMMs. And any place
15 that you looked at that signal, you'd expect
16 to find a low or high value, other than a
17 very short period during the transition.

18 Q Okay. I'm going to introduce
19 Exhibits 2 and 3.

20 MR. SUBACH: Mark 2 and 3.

21 (Whereupon the above mentioned was
22 marked for Identification.)

23 MR. HATCHER: Is this a good
24 point -- we've been going for about an
25 hour -- for a five-minute break?

1 MR. SUBACH: Yeah, let's take a
2 five-minute break.

3 THE VIDEOGRAPHER: Stand by. The
4 time is 12:25 p.m. and we're going off
5 the record.

6 (Brief recess taken.)

7 THE VIDEOGRAPHER: Stand by. The
8 time is 12:32 p.m. and we're back on
9 record.

10 Q I'm going to introduce what's going
11 to be numbered Exhibit 2, which is the
12 declaration of Dr. Donald Alpert regarding
13 U.S. Patent Number 9,858, 218.

14 Do you see this, Dr. Alpert?

15 A Yes, I do, and I do have a paper
16 copy of that next to me.

17 Q Great. And this is your
18 declaration for the '218 patent.

19 Is that correct?

20 A Yes, it is.

21 Q Okay.

22 MR. HATCHER: Just to be
23 complete -- to be complete, can we
24 identify what the exhibit number is in
25 the IPR?

1 MR. SUBACH: Sure. This is
2 Exhibit 1003 for the IPR 2020-01044.
3 I'm going to also introduce what
4 will be numbered Exhibit 3, which is
5 titled "Declaration of Dr. Donald Alpert
6 Regarding U.S. Patent Number
7 10,474,595," which is Exhibit 1003 to
8 IPR 2020-01042.

9 Do you see this in front of you,
10 Dr. Alpert?

11 A I do, and I also have a paper copy,
12 clean paper copy of that.

13 Q Thank you. This is your
14 declaration for the '595 patent.

15 Is that correct?

16 A Yes, that's what it is.

17 Q Let's flip to Exhibit 2, to start,
18 which is your declaration for the '218
19 patent. I want to draw your attention to
20 Paragraph Number 168.

21 Please let me know when you're
22 there.

23 MR. HATCHER: What page is that on?

24 MR. SUBACH: Page 89.

25 MR. HATCHER: Thank you.

1 A Okay. I've got the paper copy
2 there.

3 Q In this paragraph, you state that
4 "Hazelzet discloses an ECC/parity register
5 which has an output for uncorrectable
6 errors."

7 Is that correct?

8 A That's correct, yes.

9 Q And for this statement, you cite,
10 "Hazelzet's at Figures 3-A through 3-D, 4-A,
11 4-B, 5."

12 Is that correct?

13 A That's what it says in
14 Paragraph 168. I haven't opened up the -- I
15 have a paper copy of the Hazelzet one, when
16 and if it's necessary to refer to that.

17 But it definitely does say that
18 here.

19 Q Thanks.

20 MR. HATCHER: Can we -- I
21 apologize. Are we in the '218 or the
22 '595? I apologize.

23 MR. SUBACH: We're in the
24 declaration for the '218 which is
25 Exhibit Number 2.

1 MR. HATCHER: Okay. Thank you.

2 Q And you also cite to Paragraphs 44,
3 59, and 72 of Hazelzet.

4 Is that correct?

5 A Yes, that's correct.

6 Q Let's look at Paragraph 174 in your
7 declaration, which is Exhibit 2 to this
8 deposition. It's on Page 93.

9 Please let me know when you're
10 there.

11 A Okay. I'm there.

12 Q In this paragraph, you state that
13 "Hazelzet discloses two loads."

14 Is that correct?

15 A (Witness reviewing.)

16 Yes, that's correct. That's what
17 it says here.

18 Q Specifically, you state that
19 "Hazelzet's memory modules are configurable
20 to operate in a parity mode and an ECC mode."

21 Is that correct?

22 A Yes, it is.

23 Q And you cite to Paragraphs 20, 22,
24 49, 59 through 62, 64, 69 through 70, 72, and
25 75 as support for this.

1 Is that right?

2 A Yes. And additionally, to
3 Figure 8.

4 Q Yes, thank you. And I can
5 represent to you that they may be the exact
6 same statements and relied on the same
7 material in support of those statements in
8 the '595 declaration.

9 But for the sake of completeness,
10 let's walk through that as well. So let's
11 turn to Exhibit 3, which is your '595
12 declaration.

13 A And to where?

14 Q Yes, one second. Bear with me.

15 First, let's go to Paragraph 190,
16 which is on Page 103 of Exhibit 3 to this
17 deposition.

18 A Okay. I'm there.

19 Q In this paragraph, you state that
20 "Hazelzet discloses an ECC/parity register,
21 which has an output for uncorrectable
22 errors."

23 Is that correct?

24 A Yes.

25 Q And for that, you cite to Hazelzet

1 Figures 3-A through 3-D, 4-A, 4-B, 5, and
2 Paragraphs 44, 59, and 72.

3 Is that correct?

4 A That's what it says here, yes.

5 Q And turning to Paragraph 196, which
6 is a few pages later on Page 107, please let
7 me know when you're there.

8 A Yes, I see Paragraph 196 here.

9 Q In this paragraph, you state that
10 "Hazelzet discloses two modes."

11 Is that correct?

12 A That's correct, yes.

13 Q And specifically, you state that
14 "Hazelzet's memory modules are configurable
15 to operate in a parity mode and an ECC mode."

16 Is that correct?

17 A Yes.

18 Q And you cite to Hazelzet Figure 8
19 and Paragraphs 20, 22, 49, 59 through 62, 64,
20 69 through 70, 72, and 75 for support.

21 Is that correct?

22 A Yes. And again, also to Figure 8.

23 Q Yes. So if we compare Exhibits 2
24 and 3, which are your declarations for the
25 '218 and '595 patent, you agree that in

1 Paragraph 168 of Exhibit 2, and Paragraph 190
2 of Exhibit 3, you rely on the same portions
3 of Hazelzet in support of your statement that
4 "Hazelzet discloses an ECC/parity register."

5 Is that correct?

6 A You know, I wanted to look at them
7 side by side. Is that -- do you want me to
8 do that in order to be able to answer
9 whether --

10 Q Yes, please do.

11 A -- it's the same or not?

12 So from Exhibit 2, looking
13 at -- did you say Paragraph 168?

14 Q Correct. Paragraph 168 of
15 Exhibit 2 and Paragraph 190 of Exhibit 3.

16 A Okay. And then -- now, what's the
17 question? I've got both of those open, left
18 hand, right hand.

19 Q Do you agree that you rely on the
20 same portions of Hazelzet in support of your
21 statements that "Hazelzet discloses an
22 ECC/parity register which has an output for
23 uncorrectable errors?"

24 A (Witness reviewing.)

25 Yeah, it looks identical.

1 Q And please turn to Paragraph 174 in
2 Exhibit 2, and Paragraph 196 in Exhibit 3.
3 And we'll have a similar comparison.

4 A Okay. I'm there. And I know you
5 said "a similar comparison," but I think I
6 would like to hear the specific question.

7 Q Sure. Yes.
8 Do you agree that in Paragraph 174
9 of Exhibit 2 and Paragraph 196 in Exhibit 3,
10 you rely on the same portions of Hazelzet as
11 support for your statement that "Hazelzet
12 discloses a parity mode and ECC mode?"

13 A Yeah, that looks to be the same.

14 Q Thank you. I'm going to introduce
15 Exhibit 4.

16 MR. SUBACH: Mark this Exhibit 4.

17 (Whereupon the above mentioned was
18 marked for Identification.)

19 Q Which is -- Exhibit 4 is
20 Exhibit 1014 to the petition and it's
21 U.S. Patent Publication Number U.S.
22 2008/0098277 to inventor Hazelzet.

23 Do you see this in front of you?

24 A I do.

25 Q And I understand you have a paper

1 copy of this as well.

2 Is that correct?

3 A Yes. So I see it on the screen and
4 I see it on the paper.

5 Q This is the Hazelzet reference
6 which you cited as Exhibit 1014 in your
7 declarations.

8 Is that correct?

9 A Yes.

10 Q I want to focus on the behavior of
11 Hazelzet's ECC/parity register in each of
12 Hazelzet's parity and ECC modes, separately.

13 Does that sound okay?

14 A Sure. You're asking the questions,
15 so.

16 Q What does Hazelzet's ECC parity
17 register do in Hazelzet's parity mode?

18 A Well, generally, the register
19 receives command address and control
20 information as well as a bit that covers the
21 parity for that information. Receives that
22 from the system memory controller and it will
23 buffer that information and send it, meaning
24 address command control, along to the DRAMs.

25 And it will also check whether the

1 received parity of that information matches
2 the -- of the parity that was sent from the
3 system memory controller, and if there's
4 discrepancy in the parity, it will indicate
5 an error and send that information back to
6 the system memory controller.

7 Q Thank you.

8 What's the purpose of Hazelzet's
9 parity mode?

10 A (Witness reviewing.)

11 Well, there may be a number of
12 purposes. But certainly one is to ensure the
13 reliable communication between the MCH and
14 the DIMM of the address command and control
15 signals.

16 Q Earlier, you said it will also
17 check whether the received parity of that
18 information of the parity that was sent from
19 the system memory controller -- sorry.
20 Scratch that.

21 Earlier, you said it will check
22 whether the received parity of that
23 information matches the -- the parity that
24 was sent from the system memory controller.

25 Do I have that correct?

1 A Well, you've got the record there,
2 but maybe -- you know, as I'm hearing that
3 back, I believe what I was saying is that
4 the -- the register that we're talking about
5 will, in fact, compute a parity on the
6 information that it receives.

7 And so, it will check that
8 the -- the parity of the information it
9 receives matches the parity that the MCH
10 computed when that information was sent.

11 Q And what's the purpose of this
12 parity functionality in Hazelzet's parity
13 mode?

14 A Well, if there are had been a
15 single bit error, or, in fact, any -- an odd
16 number of bit errors in the communication
17 between the MCH and the DIMM, then that would
18 be detected as some type of error in the
19 communication.

20 The parity would also cover a
21 portion of the register, for example,
22 information that was received might have
23 been -- you know, at the DIMM might have been
24 correct, but that there was some error or
25 stuck at fault or some other problem within

1 the front end of that register.

2 It would also detect those types of
3 errors.

4 Q Okay. Perhaps I should have asked
5 earlier, but what is "parity?"

6 A Parity would be, generally, in
7 the -- in this context, it's usually kind of
8 one bit that indicates whether
9 there's -- whether, in a number of bits that
10 you're checking, whether there's an odd
11 number of ones or an even number of ones.

12 And a parity would provide a single
13 bit indicating.

14 Q Do normal read and write operations
15 occur in Hazelzet's parity mode?

16 A Yes, they do.

17 Q Does training occur in Hazelzet's
18 parity mode?

19 A Again, going by -- by recollection,
20 but I don't -- I believe that -- that
21 Hazelzet doesn't expressly disclose the
22 training.

23 Q So because you're saying that
24 Hazelzet doesn't expressly disclose training,
25 does that mean, according to Hazelzet,

1 training does not occur in Hazelzet's parity
2 mode?

3 A No. I believe a person of ordinary
4 skill in the art would understand it's
5 possible for the training to occur in the
6 parity mode.

7 Q According to Hazelzet, how would
8 training be performed?

9 A Well, as I mentioned, Hazelzet
10 doesn't explain how training is performed.
11 It only refers to some type of an
12 initialization that would occur.

13 Q Does Hazelzet disclose what would
14 be trained?

15 MR. HATCHER: Objection, form,
16 asked and answered.

17 A No. Hazelzet doesn't disclose
18 training.

19 Q So, according to Hazelzet, training
20 does not occur in Hazelzet's parity mode.

21 Is that correct?

22 A No.

23 Q Why do you believe a person of
24 ordinary skill in the art would believe that
25 training is being performed in Hazelzet's

1 parity mode?

2 MR. HATCHER: Objection, form.

3 Misstates, asked and answered.

4 A Well, I believe a person of
5 ordinary skill in the art would understand
6 that it's -- it's possible to perform
7 training in the -- in the parity mode.

8 Q Right. I guess I'm asking you, why
9 do you believe that a person of ordinary
10 skill in the art would understand that it's
11 possible to perform training in a parity
12 mode?

13 A Well, a person of ordinary skill in
14 the art would be aware that it's common, for
15 example, to perform certain types of training
16 periodically during the -- the normal
17 operation, which would be the parity mode.
18 The training would be in particular to be
19 able to compensate for any changes in
20 temperature voltage, other environmental
21 conditions that might vary, you know,
22 during -- during the operation of the system,
23 depending on -- at least on the environment.

24 Q But as you said earlier, Hazelzet
25 doesn't say anything about how training is

1 performed or what is being trained.

2 Is that correct?

3 A Yes. I mean, to the best of my
4 recollection, there's no reference to
5 training in Hazelzet.

6 Q What is "training?"

7 A I think a person of ordinary skill
8 in the art in the context of -- of the
9 patents talking about memory modules would
10 understand that training is exercising the
11 module for the purpose of adjusting
12 parameters in order to improve or optimize
13 the performance and reliability.

14 Q What parameters?

15 A Some of the common parameters would
16 be associated with the circuitry for driving
17 and receiving signals. It might be adjusting
18 the ways or it might be adjusting the
19 so-called impedance of the signals of the
20 paths.

21 Q Okay. Let's discuss Hazelzet's ECC
22 mode.

23 What does Hazelzet's ECC parity
24 register do in Hazelzet's ECC mode?

25 A The general operation would be

1 similar to the parity mode in that it
2 receives the address manned and controlled
3 signals. And it also receives something
4 called an ECC or error correcting code, so
5 that's a -- the number of bits that it
6 receives, together with the information
7 address command and control that's sent from
8 the MCH.

9 And the register in Hazelzet will
10 receive that information, it will perform the
11 error correction code computation on
12 the -- on the information, and it will
13 compare that with the error correcting code
14 that was received from the MCH. And if those
15 codes are different, then there's a way to
16 determine something called a "syndrome" that
17 can be used to correct, in this case -- well,
18 to correct certain errors. I can go into a
19 little more detail if I looked at the specs
20 some more.

21 Q So, what is the purpose of
22 Hazelzet's ECC mode?

23 A Okay. So the purpose of the ECC
24 mode is similar to what we saw for parity.
25 You can detect errors in the address

1 information -- sorry -- the address command
2 and control information that's received.

3 And furthermore, specifically, you
4 can detect up to -- all double bit errors.

5 And for the signal bit errors, the parity can
6 detect -- ECC can actually do a correction of
7 the information.

8 And so, in fact, it does signal
9 back to the memory controller about
10 information about whether it identified a
11 correctable error or an uncorrectable error.

12 Q So is the purpose of the ECC
13 function in Hazelzet's ECC mode to detect and
14 correct errors?

15 A Yes. I would say that it is, yes.

16 Q What is "ECC," generally?

17 A ECC stands for "Error Correcting
18 Code," and it would be a code. It would be
19 information -- in addition to whatever is the
20 actual content that's being communicated, it
21 would be some additional information or
22 additional bits that would be used to
23 determine whether the content that was being
24 communicated was correctly received.

25 And it also provides enough

1 information to correct certain errors that
2 might occur.

3 Q Why is ECC used?

4 A Generally, ECC would -- would be
5 used so that certain errors could be
6 corrected. And in particular, if you can't
7 correct the errors, then -- in fact, you may
8 have -- it may well be a kind of fatal flaw
9 or, you know, a problem that would be
10 unrecoverable, might require the whole system
11 to be brought down and brought back up, for
12 example.

13 Q Do normal read and write operations
14 occur in Hazelzet's ECC mode?

15 A Yes, they do.

16 Q So is ECC a normal mode of
17 operation?

18 A You know, I'm -- I'm just thinking
19 about it now. I don't believe I've thought
20 about that before, at least in the context of
21 these patents.

22 So just sitting here right now, you
23 know, I think it would be fair to say that
24 ECC is a normal mode of operation.

25 But as I mentioned, I haven't

1 thought through carefully whether there's any
2 reason it might not be considered to be
3 normal mode.

4 Q Okay. Is training performed in
5 Hazelzet's ECC mode?

6 A Well, Hazelzet doesn't disclose
7 training. So a person of ordinary skill in
8 the art would understand that training could
9 be performed in the ECC mode.

10 But that would be from general
11 knowledge. It's not a specific disclosure or
12 teaching of Hazelzet.

13 Q So let me try asking that question
14 again.

15 According to Hazelzet, is training
16 performed in Hazelzet's ECC mode?

17 A Hazelzet doesn't have any
18 disclosure about that point.

19 Q Let's go back to Exhibit 2.

20 A Which -- can you remind me which
21 that was?

22 Q Yes. That's your declaration as to
23 the '218 patent.

24 A Okay. I've got that here.

25 Q I want to direct your attention to

1 Paragraph 131, which is on Page 63.

2 Please let me know when you're
3 there.

4 A Okay. I'm there.

5 Q In this paragraph, you state that
6 "Hazelzet's memory module would be modified
7 to add a training mode."

8 Is that correct?

9 A Yes.

10 Q Just for completeness, let's turn
11 to Exhibit 3, which is your declaration for
12 the '595 patent. You can leave Exhibit 2
13 open to that same page for now.

14 And there, I want to direct you to
15 Paragraph 15 -- sorry -- Paragraph 153 of
16 Exhibit 3.

17 MR. HATCHER: What page?

18 MR. SUBACH: I'm finding
19 it -- which is Page 76 of Exhibit 3.

20 Q Please let me know when you're
21 there.

22 A Yes. Paragraph 153, you said,
23 right?

24 Q Yes.

25 A Okay. I'm here or I'm there.

1 Q And here, similarly, you state that
2 "Hazelzet's memory module would be modified
3 to add a training mode."

4 Is that correct?

5 A Yes.

6 Q And looking at those two
7 paragraphs, Exhibit 2, Paragraph 131,
8 Exhibit 3, Paragraph 153, the training mode
9 you mentioned is a whole new mode.

10 Is that correct?

11 A It is -- it's a new mode in the
12 sense that it's not disclosed by Hazelzet.

13 Q So, to Hazelzet, it's a new mode.

14 Is that correct?

15 A Yes. It would be an additional
16 mode for Hazelzet.

17 Q And that new mode is different from
18 the parity and ECC modes disclosed in
19 Hazelzet.

20 Is that correct?

21 A Yes. The training mode is
22 different from both parity and ECC modes.

23 Q What does a person of ordinary
24 skill in the art need to consider when adding
25 a new mode of operation to a memory module?

1 MR. HATCHER: Objection, form.

2 A Well, generally, a new mode would
3 mean a state of the memory module, and so you
4 would need to have some storage to indicate
5 what state it's operating in. And then there
6 would be different operations, or at least
7 the operations would be performed differently
8 in -- or at least some operations would be
9 performed differently in the two modes.

10 Q Is there anything else a person of
11 ordinary skill in the art would need to
12 consider when adding a new mode of operation
13 to a memory module?

14 A I would think that would generally
15 cover it. Obviously, in any specific case,
16 you know, you'd look at -- you would need to
17 look at more -- you know, at the details.

18 But generally, that's what a person
19 of ordinary skill in the art would look for.

20 Q What kind of details?

21 A I think you'd want to look at what
22 were the additional or different operations
23 that were being performed.

24 Q What modifications would need to be
25 made to the memory module to ensure that it

1 operates for its intended purpose with the
2 new mode?

3 MR. HATCHER: Objection, form.

4 A I'm not sure that I -- I think I
5 don't fully understand what you're asking me.
6 Maybe you can rephrase or give it a little
7 more context?

8 I may understand, but I want to
9 make sure I'm clear on what the question is.

10 Q Sure. We're talking about adding a
11 new mode to Hazelzet.

12 Right?

13 A Yeah. In particular, we're talking
14 about Paragraph -- sticking with the '218
15 declaration now, Paragraph 131 does identify
16 that as a training mode, to
17 be -- corresponding to the first mode of the
18 claims in '218.

19 Q Okay. So do you agree that adding
20 a new mode to Hazelzet would require some
21 modifications?

22 A Yes. It would require
23 modifications such as explained in the -- both
24 in the JEDEC -- yeah, sorry. So it's
25 J-E-D-E-C, all capitals, and Buchmann, which

1 is B-U-C-H-M-A-N, or N-N. I don't remember.

2 N-N, yeah. B-U-C-H-M-A-N-N.

3 Those references do disclose what
4 needs to be -- what needs to be done in order
5 to perform the training.

6 Q So what modifications would need to
7 be done to the memory module to ensure that
8 it operates for its intended purpose with the
9 new mode?

10 A (Witness reviewing.)

11 So anyway, rather than just answer
12 off the top of my head, I found what I've
13 written in the declaration, which was
14 consistent with my -- you know, with the
15 recollection off the top of my head as well.

16 But in the declaration, and we're
17 talking about the '218 declaration now, at
18 the bottom of page 64, there's a
19 Paragraph 134. And it says, "over there, in
20 either combination."

21 So that's either combination of
22 Hazelzet -- you were saying Hazelzet --
23 Hazelzet with JEDEC or Hazelzet with
24 Buchmann.

25 The circuitry of Hazelzet's module,

1 in particular the ECC parity register, would
2 be modified to implement the training as part
3 of an additional mode to run. And the
4 training there refers to the training that's
5 taught by JEDEC and Buchmann.

6 And it says, for example, "at
7 initialization with Hazelzet's other
8 disclosed initialization operations." So
9 that's one modification that's identified
10 here is implementing the training.

11 And the second is to use an open
12 grain output of Hazelzet's to communicate a
13 new notification signal.

14 Q Right. But that's -- so thank you
15 for identifying that paragraph. I agree that
16 this discloses that the modification would be
17 to add training.

18 I'm asking more specifically, what
19 steps would you need to take to make that
20 modification?

21 A (Witness reviewing.)

22 Okay. I was just looking through
23 the declaration and some other documents.
24 And I would -- I think I'm prepared to answer
25 the question if I can hear it again.

1 Q Yes. I said: What steps would you
2 need to take to make that modification?

3 A Okay. And so what -- yeah,
4 but -- I'm sorry.

5 What I've explained in
6 Paragraph 132 is that with the JEDEC
7 reference, the combination of the JEDEC
8 reference would be like those described for
9 MB-DRAM training in JEDEC. And that was
10 Exhibit 1015.

11 So it's stated with the petition
12 and the declaration. And on Page 8, it does
13 describe what would be involved even in doing
14 the training, of having the MB or memory
15 buffer do training for the module.

16 And so, some of the things that it
17 explains there are that the memory
18 buffer -- so in this case Hazelzet's
19 register -- buffer register would receive a
20 command indicating it would be going into
21 this training.

22 Once enabled -- and I'm reading
23 sections or summarizing from that Page 8 of
24 Exhibit 1015.

25 And it says, "Once that training is

1 enabled, the memory buffer assumes autonomous
2 control of the command adverse control and
3 data/strobe signals to the DRAMs without any
4 further assistance from the host. And then
5 the memory buffer performs right leveling,
6 read enable training to ensure that it can
7 capture read data, successful writes, and
8 read data from the DRAMs correctly as part of
9 the DRAM interface training. "

10 And then it further goes on to say
11 that -- that the MCH "and determine when
12 training is complete, either by going for a
13 fixed amount of time or by polling over the
14 so-called SM bus." And in particular, it
15 does indicate that -- it says, "In addition,
16 training completion can be signaled by the
17 assertion of error out, capital ERROUT
18 pound. "

19 And it says, "This is not power of
20 default, but it can be enabled by setting
21 particular bit in a particular training
22 completion word of the memory buffer. "

23 So I believe a person of ordinary
24 skill in the art would look at this and
25 understand that there's certain -- certain

1 modifications involved providing this
2 function and signals, and as well that in
3 this case that there's a mode that's
4 programmed in this training completion word
5 in order to get the functionality of
6 asserting the training completion on the
7 error out pin.

8 So that was for JEDEC. I could go
9 on to Hazelzet or maybe let me just talk for
10 a long time in response to one question.

11 Q Well, yeah. Let me try to reframe
12 it a little bit.

13 I agree that there are certain
14 functions and signals that are described
15 there that you're referring to. And
16 as -- you know, as you said, that there would
17 be certain modifications involved in
18 providing those functions and signals.

19 So I'm not asking what are the
20 functions and signals of this new mode. I'm
21 saying, "What would be the steps to add this
22 new mode? What are the steps to make that
23 modification?"

24 If I'm starting with the memory
25 module disclosed in Hazelzet, you know, I

1 need to take out the soldering iron, I need
2 to take out, you know, my -- my multimeter,
3 maybe.

4 And what do I do to add training?
5 What are the steps?

6 A Well, first of all, I would say my
7 general understanding is that in determining
8 whether these modifications are appropriate
9 for an obviousness analysis, that what we're
10 really looking at is whether -- whether and
11 how a person of ordinary skill in the art
12 would combine the teachings.

13 So my understanding as I've done
14 the analysis, it's not concerned with the
15 physical embodiments and how they
16 might -- those structures might be physically
17 modified.

18 And so I -- I haven't considered
19 what -- you know, exactly how those changes
20 would be made. But I am familiar with the
21 skill of a person of ordinary skill in the
22 art and implementing those changes, you know,
23 first in a high-level description language,
24 and ultimately through synthesizing or custom
25 designing an integrated circuit is within the

1 skill of a person of ordinary skill in the
2 art.

3 Q So let's go through those steps.

4 As a person of ordinary skill in
5 the art, what would be the first step in
6 modifying a memory module to add this new
7 mode?

8 A Well, there's a lot of ways to
9 proceed. But generally, I would think the
10 first thing that you would do would be to
11 take a high-level model corresponding to
12 Hazelzet and to make the changes first there
13 that would involve any interfaces.

14 Q Other than changes to the
15 interfaces, are there any other changes that
16 you would need to make to the high-level
17 model of Hazelzet?

18 A Yeah. After you did that, I think
19 you would want to identify how the state of
20 the training mode would be represented.

21 Generally, one or two or a certain
22 number of bits. The combination that's
23 inscribed here only uses the parity mode of
24 Hazelzet.

25 But you would want either the

1 parity mode or a training mode, and that
2 would be represented as a particular bit in a
3 control register, or multiple bits.

4 And then you would go ahead and
5 design, again, the high -- at an HDL level,
6 the logic that would sequence through
7 these -- for these training sequences, such
8 as the right leveling and the read enable
9 training.

10 And then you would test that
11 extensively versus a -- some type of model or
12 test suites that were available. And
13 eventually, after you're convinced that the
14 logic level was appropriately accurate in
15 terms of the functions that were being
16 performed, you would develop the circuit
17 level, circuit -- physical design level,
18 circuit and layout of the logic elements and
19 of the interfaces, you know, simulate that as
20 well, in particular for the performance
21 requirements and the voltage ranges, voltage
22 and temperature ranges.

23 And ultimately, once you had a
24 design that was well-validated -- the
25 function is correct, the circuitry is

1 correct, the logic function and the circuitry
2 match each other, it's a process called
3 "logic validation" -- then you would create
4 the masks, you would fabricate the circuit.

5 And you would go about and test
6 that integrated circuit according to the
7 specifications to ensure that the design was
8 operating correctly as you intended, and
9 within the -- and it's characterized to be
10 working within the specified voltage
11 temperature, frequency, and so on.

12 Q So let's go back to the high-level
13 design.

14 You said, after considering the
15 interfaces, you would want to identify how
16 the state of the training mode would be
17 represented.

18 After you do that, would that
19 necessitate any other alterations to other
20 components on Hazelzet?

21 A Well, it would ultimately be
22 providing an alternate source for the address
23 command and control information. From
24 Hazelzet, that comes from the MCH, and it's
25 internally registered, and there's certain

1 bypasses that select which version of those
2 signals to use and to drive out to the DRAMs.

3 And so you would -- for the
4 purposes of training, you would need another
5 source for those address command and control
6 signals to be provided for the training
7 sequences.

8 Q So you would need to add another
9 source for those command and control signals.

10 Is there anything else that you
11 would need to add?

12 A Maybe can you ask that question a
13 little bit more in context?

14 We talked about adding a lot of
15 things, such as like the state machines that
16 are sequencing through the training sequences
17 of what -- which would be something that's
18 not in -- in Hazelzet. And as I recall, I
19 was answering a question about what -- what
20 you would change that's in Hazelzet as
21 opposed to adding new circuitry.

22 Q Well, do you agree that when you
23 add new circuitry, it needs to -- it would
24 need to be connected to something that's
25 already there?

1 A I don't -- I don't think it
2 necessarily would, no. Not all the new
3 circuitry needs to be added to something
4 that's there.

5 Q So if it's not going to be
6 connected to something that's already there,
7 then the new circuitry would have to be
8 connected to something new.

9 Is that correct?

10 A Something -- I have to admit, I
11 don't know.

12 Maybe if you rephrase the question,
13 I might be able to answer it?

14 Q Sure. Earlier, we talked about
15 changes to the interfaces that would need to
16 be made to Hazelzet.

17 Do you recall?

18 A Yes. That's the one --
19 the -- probably for the first -- where the
20 first changes would begin.

21 Q Could you talk about those changes
22 a little bit more?

23 MR. HATCHER: Objection, form. If
24 you have a question, ask it. Ask it.

25 A Well, for example, over here, for

1 JEDEC, it does indicate that once the
2 training -- once the training is enabled,
3 that the memory buffer, it says, "assumes
4 autonomous control of the command address,
5 control, and data/strobe signals of the DRAMs
6 without any further assistance from the
7 host."

8 And looking at Hazelzet -- let me
9 just look here. Yes.

10 I'm looking at Hazelzet and it's
11 consistent with my recollection. Hazelzet
12 does not have an interface to the data/strobe
13 signals of the DRAMs or of the connector.

14 So that was certainly part of the
15 interface that would be -- that would be
16 added to Hazelzet in order to be able to
17 perform the -- the training sequences that
18 are identified.

19 Q How would you add that interface to
20 Hazelzet?

21 A Well, again, at the -- at the HDL
22 level, the high-level design language, you
23 would define some structures, what signals
24 they were connected to at the interface.
25 Basically, the pins that go -- in this case,

1 it would be going to the edge connector and
2 to the DRAMs, much as the address and command
3 are already -- had those signals to receive
4 and drive between the connector and the
5 DRAMs.

6 But the physical circuit design
7 level, you would have certain buffers, buffer
8 circuits that would be connected to the pins,
9 or whatever was the other physical interface,
10 to the -- to the board.

11 MR. HATCHER: We've been going for
12 about an hour and ten. You know,
13 whenever you get to a point, we can take
14 another five minutes.

15 THE WITNESS: I think that's a good
16 idea. I was --

17 MR. SUBACH: I don't have much
18 left. So if you just bear with me, I
19 think we'll be done soon.

20 THE WITNESS: Yeah, I'll be fine.
21 My point was that, you know, just look
22 for a breaking point.

23 Q So you said this new interface
24 would go between the pins on the memory
25 module on the edge connector to the DRAMs.

1 That means the DRAMs have to have a
2 corresponding input.

3 Is that correct?

4 A Yes. The DRAMs, yeah, have the
5 data and strobe connections.

6 Q But the DRAMs disclosed by
7 Hazelzet, as you said, they don't have an
8 interface for the data and strobe signals.

9 Is that right?

10 A No, that's not correct.

11 Q Hazelzet does disclose an interface
12 for data strobe signals?

13 A It -- it does, yes.

14 Q Okay. Perhaps I misunderstood,
15 then. I thought earlier you said Hazelzet
16 does not have an interface for data/strobe
17 signals of the DRAMs or the connector
18 interface?

19 A Okay. If I said that, that wasn't
20 totally correct.

21 What I meant to say, and I thought
22 I was answering, was what were the
23 modifications to the buffer register in
24 Hazelzet, the strobes and -- in Hazelzet, the
25 data strobes and the data signals that I was

1 talking about in that embodiment, they go
2 directly from the edge connector to the
3 DRAMs.

4 But they're not connected to
5 Hazelzet's memory buffer.

6 Q I see. So to -- one of the changes
7 that you would need to make is to connect
8 those signals through a -- through a buffer.

9 Is that correct?

10 A Yeah, I -- let me answer and then
11 you can tell me if that was responsive
12 enough.

13 So just like Hazelzet
14 has -- receives the address command and
15 control signals -- the buffer,
16 sorry -- receives those from the edge
17 connector and drives them to the DRAMs,
18 similarly, Hazelzet's buffer would be
19 modified so that it connects to the edge
20 connector data strobe and data signals, as
21 well as to the DRAM data strobe and data
22 signals.

23 And those are bidirectional, so it
24 might be driven in either direction. Sorry.

25 The data is bidirectional, not the

1 strokes.

2 Q So if I'm understanding correctly,
3 Hazelzet receives the address and command
4 control signals from the edge connector and
5 drives them directly to the DRAMs.

6 To make the modification you're
7 proposing, one of the things that you would
8 need to do is drive those signals through a
9 data buffer.

10 Is that correct?

11 A Yes. And that's what the -- that's
12 what the -- the JEDEC document tells us that.

13 Q Okay. And to make that
14 modification, you would need to add new
15 interfaces.

16 Is that correct?

17 A Yes, you would need to add
18 interfaces, for the strobe and data signals,
19 both to the edge connector and to the DRAMs.

20 Q What other modifications would you
21 need to make?

22 A Make besides the ones that we've
23 gone over? Or I don't know if it's a more
24 specific question on what we've talked about?

25 MR. HATCHER: Yeah, it's been

1 another five minutes since the last time
2 I suggested a break. Now we're at an
3 hour and 15. If you just have another
4 question, then okay. But if not, let's
5 take a break, and then you can continue
6 on.

7 THE WITNESS: Sounds good to me.

8 MR. SUBACH: Just a few more
9 questions.

10 MR. HATCHER: No, not a few. I
11 told you. I've got my son, I need to go
12 check on him. It's been an hour and 15
13 minutes.

14 If you have another question, okay.
15 If you got multiple more questions, then
16 we're taking a break.

17 Which is it?

18 MR. SUBACH: At the beginning of
19 this deposition, we -- the agreement was
20 we would end the line of questioning.
21 I'm going to continue.

22 MR. HATCHER: No, no. We're going
23 to take a break. Thank you. Go off the
24 record.

25 MR. SUBACH: Mike, this isn't your

1 decision to make.

2 MR. HATCHER: Yeah, it is. Off the
3 record.

4 MR. SUBACH: We're going to have a
5 standing objection to an improper
6 interruption by defense counsel.

7 MR. HATCHER: Fine.

8 MR. SUBACH: And wasting time with
9 long-speaking objections.

10 MR. HATCHER: Okay. Whatever.

11 THE VIDEOGRAPHER: Stand by. The
12 time is 1:46 p.m. and we're going off
13 the record.

14 (Brief recess taken.)

15 THE VIDEOGRAPHER: Stand by. The
16 time is 1:56 p.m. and we're back on
17 record.

18 Q Hi, Dr. Alpert.

19 So earlier, we were talking about
20 modifications that would need to be made to
21 Hazelzet to implement the new mode.

22 Do you recall that?

23 A Yes, I mean generally. I'll wait
24 for the next question.

25 Q One of the changes we talked about

1 was there would need to be a data buffer
2 added between the edge connections and the
3 DRAMs.

4 Do I have that right?

5 MR. HATCHER: Objection, form.

6 Objection, form.

7 A Yes, I do recall talking about
8 that, and yes, there would be --
9 the -- Hazelzet would be modified to extend
10 the buffering to include the data and
11 strokes.

12 Q And I believe, earlier, you also
13 mentioned there would need to be some logic
14 elements added to Hazelzet in this
15 modification?

16 A Yes, that sounds correct.

17 Q Is there anything else that would
18 need to be added to Hazelzet to make this
19 modification?

20 A No. You know, I can't think of
21 anything else, you know, other than any
22 issues that would be covered in the -- just
23 the common practice of design.

24 Q Okay. And then you said the
25 modified design would then need to be tested.

1 Is that right?

2 A Yeah. In terms of making
3 modifications and, you know, following that
4 through into production or real circuit, yes,
5 it would be tested.

6 Q Okay.

7 MR. SUBACH: I have no further
8 questions.

9 MR. HATCHER: That was it, like for
10 the whole thing? Perhaps if we had
11 communicated better, I would have
12 understood and that's on me. That's
13 just as much on me. I didn't realize
14 that you only had a few more questions
15 until the end of the entire questioning
16 as opposed to your next break. Okay.

17 So no more questions. Do I have
18 any questions? I do not have any
19 questions, so I believe we're done.

20 THE VIDEOGRAPHER: Stand by. The
21 time is 1:59 p.m. and we're going off
22 the record.

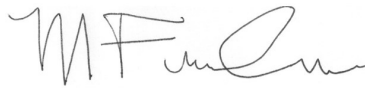
23 (Witness was excused.)
24
25

C E R T I F I C A T E

I, MICHAEL FRIEDMAN, a Certified Court Reporter and Notary Public, qualified in and for the State of New Jersey do hereby certify that prior to the commencement of the examination DR. DONALD ALPERT was duly sworn by me to testify to the truth the whole truth and nothing but the truth.

I DO FURTHER CERTIFY that the foregoing is a true and accurate transcript of the testimony as taken stenographically by and before me at the time, place and on the date hereinbefore set forth.

I DO FURTHER certify that I am neither a relative of nor employee nor attorney nor counsel for any of the parties to this action, and that I am neither a relative nor employee of such attorney or counsel, and that I am not financially interested in the action.



MICHAEL FRIEDMAN, CCR of the
State of New Jersey
License No: 30XI00228600
Date: March 10, 2021

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DEPOSITION ERRATA SHEET

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I declare under penalty of perjury
that I have read the entire transcript of
my Deposition taken in the captioned matter
or the same has been read to me, and
the same is true and accurate, save and
except for changes and/or corrections, if
any, as indicated by me on the DEPOSITION
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Signed on the _____ day of
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DR. DONALD ALPERT

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25 DR. DONALD ALPERT

DR. DONALD
ALPERT

EXHIBIT 1

03 - 10 - 2021



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APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
61/186,799	06/12/2009		270	NETL.062PR		

CONFIRMATION NO. 1666

UPDATED FILING RECEIPT



0C000000037947580

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Date Mailed: 09/25/2009

Receipt is acknowledged of this provisional patent application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Hyun Lee, Ladera Ranch, CA;

Power of Attorney:

Bruce Itchkawitz--47677

If Required, Foreign Filing License Granted: 06/17/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/186,799**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

Title

METHOD OF PROVIDING HANDSHAKING BETWEEN A MEMORY CONTROLLER HUB AND A
MEMORY SUBSYSTEM

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international

page 1 of 3

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1008, p. 1

patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

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page 2 of 3

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Ex. 1008, p. 2

Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

page 3 of 3

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1008, p. 3

Please Direct All Correspondence to Customer Number 20995

TRANSMITTAL LETTER
PROVISIONAL APPLICATION MISSING PARTS

Applicant : Hyun Lee
App. No : 61/186799
Filed : June 12, 2009
For : METHOD OF PROVIDING
HANDSHAKING BETWEEN A
MEMORY CONTROLLER HUB
AND A MEMORY SUBSYSTEM

CERTIFICATE OF EFS WEB TRANSMISSION

I hereby certify that this correspondence, and any other attachment noted on the automated Acknowledgement Receipt, is being transmitted from within the Pacific Time zone to the Commissioner for Patents via the EFS Web server on:

September 22, 2009

(Date)

Bruce S. Itchkawitz, Reg. No. 47,677

Mail Stop MISSING PARTS

Commissioner For Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

In response to the Notice to File Missing Parts of Provisional Application, which was mailed by the Office on June 22, 2009, enclosed are:

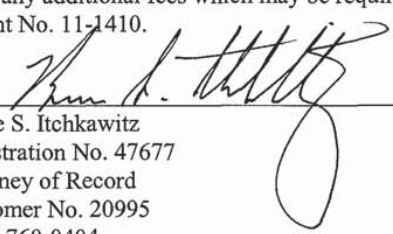
(X) A Supplemental Application Data Sheet in 3 pages.

FEE CALCULATION:

FEE CALCULATION				
FEE TYPE		FEE CODE	CALCULATION	TOTAL
Late Fee or Cover Sheet	1.16(g)	1052 (\$50)		\$50
1 Month Extension	1.17(a)(1)	1251 (\$130)		\$130
			TOTAL FEE DUE	\$180

(X) Fees will be paid via EFS Web. Extension of time is requested by payment of any extension fee.

The Commissioner is hereby authorized to charge any additional fees which may be required, now or in the future, or credit any overpayment, to Account No. 11-1410.


 Bruce S. Itchkawitz
 Registration No. 47677
 Attorney of Record
 Customer No. 20995
 (949) 760-0404

7840897
092209

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1008, p. 4

SUPPLEMENTAL APPLICATION DATA SHEET**Application Information**

Application Number:: 61/186,799
Filing Date:: June 12, 2009
Application Type:: Provisional
Subject Matter:: Utility

Suggested Classification::

Suggested Group Art Unit::

CD-ROM or CD-R?::

Number of CD disks::

Number of copies of CDs::

Sequence Submission?:: No

Computer Readable Form (CRF)?::

Number of copies of CRF::

Title:: METHOD OF PROVIDING HANDSHAKING
BETWEEN A MEMORY CONTROLLER HUB AND A MEMORY SUBSYSTEM

Attorney Docket Number:: NETL.062PR

Request for Early Publication?:: No

Request for Non-Publication?:: No

Suggested Drawing Figure::

Total Drawing Sheets:: 1

Small Entity?:: No

Latin Name::

Variety Denomination Name::

Petition Included?::

Petition Type::

Licensed US Govt. Agency::

Contract or Grant Numbers::

1

Supplemental 61/186799 June 12, 2009 9/22/09

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1008, p. 5

Secrecy Order in Parent Appl.?: No

Inventor Information

Applicant Authority Type:: Inventor
Primary Citizenship Country:: U.S.
Status:: US Residency
Given Name:: Hyun
Family Name:: Lee
City of Residence:: Ladera Ranch CA
State or Prov. of Residence:: CA
Country of Residence:: United States
Street:: 21 Thalia Street
City:: Ladera Ranch
State or Province:: CA
Country:: United States
Postal or Zip Code:: 92694

Correspondence Information

Correspondence Customer Number:: 20995
Phone Number:: (949) 760-0404
Fax Number:: (949) 760-9502
E-Mail Address:: efiling@kmob.com

Representative Information

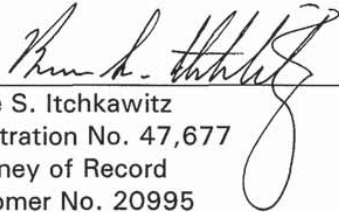
Representative Customer Number:: 20995

Assignment Information

Assignee Name:: NETLIST, Inc.
Street:: 51 Discovery, Suite #150
City:: Irvine
State or Province:: CA
Country:: United States
Postal or Zip Code:: 92618

Dated: September 22, 2009

By: _____


Bruce S. Itchkawitz
Registration No. 47,677
Attorney of Record
Customer No. 20995
(949) 760-0404

7840925
092209

Electronic Patent Application Fee Transmittal				
Application Number:		61186799		
Filing Date:		12-Jun-2009		
Title of Invention:		METHOD OF PROVIDING HANDSHAKING BETWEEN A MEMORY CONTROLLER HUB AND A MEMORY SUBSYSTEM		
First Named Inventor/Applicant Name:				
Filer:		Bruce S. Itchkawitz/Nadin Hamoui		
Attorney Docket Number:		NETL.062PR		
Filed as Large Entity				
Provisional Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Pages:				
Claims:				
Miscellaneous-Filing:				
Late provisional filing fee/cover sheet	1052	1	50	50
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1008, p. 8

Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Extension - 1 month with \$0 paid	1251	1	130	130
Miscellaneous:				
Total in USD (\$)				180

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1008, p. 9

Electronic Acknowledgement Receipt	
EFS ID:	6122939
Application Number:	61186799
International Application Number:	
Confirmation Number:	1666
Title of Invention:	METHOD OF PROVIDING HANDSHAKING BETWEEN A MEMORY CONTROLLER HUB AND A MEMORY SUBSYSTEM
First Named Inventor/Applicant Name:	
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Chelsea Pearsall
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.062PR
Receipt Date:	22-SEP-2009
Filing Date:	12-JUN-2009
Time Stamp:	18:35:58
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 180
RAM confirmation Number	4951
Deposit Account	111410
Authorized User	KNOBBE MARTENS OLSON AND BEAR
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1008, p. 10

File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1		NETL062PRMPResponse.pdf	125965 c5f139fe8c3fb1f161851273e86364c5cd9b775	yes	4
Multipart Description/PDF files in .zip description					
	Document Description		Start	End	
	Applicant Response to Pre-Exam Formalities Notice		1	1	
	Application Data Sheet		2	4	
Warnings:					
Information:					
2	Fee Worksheet (PTO-875)	fee-info.pdf	32621 6ddbf8f92d2aab6e158c0c64e64b622ecb4b42d	no	2
Warnings:					
Information:					
Total Files Size (in bytes):			158586		
This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503. <u>New Applications Under 35 U.S.C. 111</u> If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application. <u>National Stage of an International Application under 35 U.S.C. 371</u> If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course. <u>New International Application Filed with the USPTO as a Receiving Office</u> If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.					

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
 Ex. 1008, p. 11



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING or 371(c) DATE	GRP ART UNIT	FIL FEE REC'D	ATTY. DOCKET NO	TOT CLAIMS	IND CLAIMS
61/186,799	06/12/2009		220	NETL.062PR		

CONFIRMATION NO. 1666

FILING RECEIPT



OC000000036529137

20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Date Mailed: 06/22/2009

Receipt is acknowledged of this provisional patent application. It will not be examined for patentability and will become abandoned not later than twelve months after its filing date. Any correspondence concerning the application must include the following identification information: the U.S. APPLICATION NUMBER, FILING DATE, NAME OF APPLICANT, and TITLE OF INVENTION. Fees transmitted by check or draft are subject to collection. Please verify the accuracy of the data presented on this receipt. **If an error is noted on this Filing Receipt, please submit a written request for a Filing Receipt Correction. Please provide a copy of this Filing Receipt with the changes noted thereon. If you received a "Notice to File Missing Parts" for this application, please submit any corrections to this Filing Receipt with your reply to the Notice. When the USPTO processes the reply to the Notice, the USPTO will generate another Filing Receipt incorporating the requested corrections**

Applicant(s)

Power of Attorney:

Bruce Itchkawitz--47677

If Required, Foreign Filing License Granted: 06/17/2009

The country code and number of your priority application, to be used for filing abroad under the Paris Convention, is **US 61/186,799**

Projected Publication Date: None, application is not eligible for pre-grant publication

Non-Publication Request: No

Early Publication Request: No

Title

METHOD OF PROVIDING HANDSHAKING BETWEEN A MEMORY CONTROLLER HUB AND A
MEMORY SUBSYSTEM

PROTECTING YOUR INVENTION OUTSIDE THE UNITED STATES

Since the rights granted by a U.S. patent extend only throughout the territory of the United States and have no effect in a foreign country, an inventor who wishes patent protection in another country must apply for a patent in a specific country or in regional patent offices. Applicants may wish to consider the filing of an international application under the Patent Cooperation Treaty (PCT). An international (PCT) application generally has the same effect as a regular national patent application in each PCT-member country. The PCT process **simplifies** the filing of patent applications on the same invention in member countries, but **does not result** in a grant of "an international

page 1 of 3

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1008, p. 12

patent" and does not eliminate the need of applicants to file additional documents and fees in countries where patent protection is desired.

Almost every country has its own patent law, and a person desiring a patent in a particular country must make an application for patent in that country in accordance with its particular laws. Since the laws of many countries differ in various respects from the patent law of the United States, applicants are advised to seek guidance from specific foreign countries to ensure that patent rights are not lost prematurely.

Applicants also are advised that in the case of inventions made in the United States, the Director of the USPTO must issue a license before applicants can apply for a patent in a foreign country. The filing of a U.S. patent application serves as a request for a foreign filing license. The application's filing receipt contains further information and guidance as to the status of applicant's license for foreign filing.

Applicants may wish to consult the USPTO booklet, "General Information Concerning Patents" (specifically, the section entitled "Treaties and Foreign Patents") for more information on timeframes and deadlines for filing foreign patent applications. The guide is available either by contacting the USPTO Contact Center at 800-786-9199, or it can be viewed on the USPTO website at <http://www.uspto.gov/web/offices/pac/doc/general/index.html>.

For information on preventing theft of your intellectual property (patents, trademarks and copyrights), you may wish to consult the U.S. Government website, <http://www.stopfakes.gov>. Part of a Department of Commerce initiative, this website includes self-help "toolkits" giving innovators guidance on how to protect intellectual property in specific countries such as China, Korea and Mexico. For questions regarding patent enforcement issues, applicants may call the U.S. Government hotline at 1-866-999-HALT (1-866-999-4158).

LICENSE FOR FOREIGN FILING UNDER
Title 35, United States Code, Section 184
Title 37, Code of Federal Regulations, 5.11 & 5.15

GRANTED

The applicant has been granted a license under 35 U.S.C. 184, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" followed by a date appears on this form. Such licenses are issued in all applications where the conditions for issuance of a license have been met, regardless of whether or not a license may be required as set forth in 37 CFR 5.15. The scope and limitations of this license are set forth in 37 CFR 5.15(a) unless an earlier license has been issued under 37 CFR 5.15(b). The license is subject to revocation upon written notification. The date indicated is the effective date of the license, unless an earlier license of similar scope has been granted under 37 CFR 5.13 or 5.14.

This license is to be retained by the licensee and may be used at any time on or after the effective date thereof unless it is revoked. This license is automatically transferred to any related applications(s) filed under 37 CFR 1.53(d). This license is not retroactive.

The grant of a license does not in any way lessen the responsibility of a licensee for the security of the subject matter as imposed by any Government contract or the provisions of existing laws relating to espionage and the national security or the export of technical data. Licensees should apprise themselves of current regulations especially with respect to certain countries, of other agencies, particularly the Office of Defense Trade Controls, Department of State (with respect to Arms, Munitions and Implements of War (22 CFR 121-128)); the Bureau of Industry and

page 2 of 3

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1008, p. 13

Security, Department of Commerce (15 CFR parts 730-774); the Office of Foreign Assets Control, Department of Treasury (31 CFR Parts 500+) and the Department of Energy.

NOT GRANTED

No license under 35 U.S.C. 184 has been granted at this time, if the phrase "IF REQUIRED, FOREIGN FILING LICENSE GRANTED" DOES NOT appear on this form. Applicant may still petition for a license under 37 CFR 5.12, if a license is desired before the expiration of 6 months from the filing date of the application. If 6 months has lapsed from the filing date of this application and the licensee has not received any indication of a secrecy order under 35 U.S.C. 181, the licensee may foreign file the application pursuant to 37 CFR 5.15(b).

page 3 of 3

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1008, p. 14



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NUMBER	FILING OR 371(C) DATE	FIRST NAMED APPLICANT	ATTY. DOCKET NO./TITLE
61/186,799	06/12/2009		NETL.062PR

CONFIRMATION NO. 1666

FORMALITIES LETTER



20995
KNOBBE MARTENS OLSON & BEAR LLP
2040 MAIN STREET
FOURTEENTH FLOOR
IRVINE, CA 92614

Date Mailed: 06/22/2009

NOTICE TO FILE MISSING PARTS OF PROVISIONAL APPLICATION

FILED UNDER 37 CFR 1.53(c)

Filing Date Granted

An application number and filing date have been accorded to this provisional application. The items indicated below, however, are missing. Applicant is given **TWO MONTHS** from the date of this Notice within which to file all required items and pay any fees required below to avoid abandonment. Extensions of time may be obtained by filing a petition accompanied by the extension fee under the provisions of 37 CFR 1.136(a).

- The provisional application cover sheet under 37 CFR 1.51(c)(1), which may be an application data sheet (37 CFR 1.76), is required identifying:
 - the name(s) of the inventor(s).
 - either city and state, or city and foreign country, of the residence of each inventor.

The applicant needs to satisfy supplemental fees problems indicated below.

The required item(s) identified below must be timely submitted to avoid abandonment:

- To avoid abandonment, a surcharge (for late submission of filing fee or cover sheet) as set forth in 37 CFR 1.16(g) of **\$50** for a non-small entity, must be submitted with the missing items identified in this notice.

SUMMARY OF FEES DUE:

Total additional fee(s) required for this application is **\$50** for a non-small entity

- **\$50** Surcharge.

Replies should be mailed to:

Mail Stop Missing Parts
Commissioner for Patents
P.O. Box 1450
Alexandria VA 22313-1450

Registered users of EFS-Web may alternatively submit their reply to this notice via EFS-Web.
<https://portal.uspto.gov/authenticate/AuthenticateUserLocalEPF.html>

For more information about EFS-Web please call the USPTO Electronic Business Center at **1-866-217-9197** or visit our website at <http://www.uspto.gov/ebc>.

If you are not using EFS-Web to submit your reply, you must include a copy of this notice.

/schin/

Office of Data Management, Application Assistance Unit (571) 272-4000, or (571) 272-4200, or 1-888-786-0101

page 2 of 2

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1008, p. 16

Provisional Application COVER SHEET	Attorney Docket No.: NETL.062PR First Named Inventor: Unknown Title: METHOD OF PROVIDING HANDSHAKING BETWEEN A MEMORY CONTROLLER HUB AND A MEMORY SUBSYSTEM
	Date: June 12, 2009 Page 1 of 1
Direct all correspondence to Customer No.: 20995	

Commissioner for Patents
 P.O. Box 1450
 Alexandria, VA 22313-1450

The following enclosures are transmitted herewith to be filed in the Provisional Patent Application of:

APPLICATION ELEMENTS:

- (X) Specification in 3 pages.
- (X) Drawings in 1 sheet.

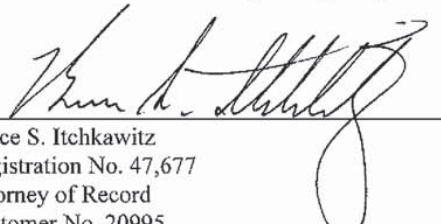
FILING FEES:

FEE CALCULATION				
FEE TYPE		LARGE FEE	CALCULATION	TOTAL
Basic Filing	37 CFR § 1.16(d)	1005 (\$220)		\$220
			TOTAL FEE DUE	\$220

- (X) The amount of \$220 will be paid via EFS web.

This invention WAS NOT made by an agency of the United States Government or under a contract with an agency of the United States Government.

Commissioner is hereby authorized to charge any additional fees which may be required, or credit any overpayment to Account No. 11-1410.


 Bruce S. Itchkawitz
 Registration No. 47,677
 Attorney of Record
 Customer No. 20995
 (949) 760-0404

7283384
 061209

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062PR
		Application Number	
Title of Invention	METHOD OF PROVIDING HANDSHAKING BETWEEN A MEMORY CONTROLLER HUB AND A MEMORY SUBSYSTEM		
The application data sheet is part of the provisional or nonprovisional application for which it is being submitted. The following form contains the bibliographic data arranged in a format specified by the United States Patent and Trademark Office as outlined in 37 CFR 1.76. This document may be completed electronically and submitted to the Office in electronic format using the Electronic Filing System (EFS) or the document may be printed and included in a paper filed application.			

Secrecy Order 37 CFR 5.2

☐ Portions or all of the application associated with this Application Data Sheet may fall under a Secrecy Order pursuant to 37 CFR 5.2 (Paper filers only. Applications that fall under Secrecy Order may not be filed electronically.)

Applicant Information:

Applicant 1				
Applicant Authority		☒ Inventor ☐ Legal Representative under 35 U.S.C. 117 ☐ Party of Interest under 35 U.S.C. 118		
Prefix	Given Name	Middle Name	Family Name	Suffix
Residence Information (Select One) ☒ US Residency ☐ Non US Residency ☐ Active US Military Service				
City		State/Province	Country of Residence	
Citizenship under 37 CFR 1.41(b)				
Mailing Address of Applicant:				
Address 1				
Address 2				
City		State/Province		
Postal Code		Country		
All Inventors Must Be Listed - Additional Inventor Information blocks may be generated within this form by selecting the Add button. Add				

Correspondence Information:

Enter either Customer Number or complete the Correspondence Information section below. For further information see 37 CFR 1.33(a).	
☐ An Address is being provided for the correspondence information of this application.	
Customer Number	20995
Email Address	efiling@kmob.com Add Email Remove Email

Application Information:

Title of the Invention	METHOD OF PROVIDING HANDSHAKING BETWEEN A MEMORY CONTROLLER HUB AND A MEMORY SUBSYSTEM		
Attorney Docket Number	NETL.062PR	Small Entity Status Claimed ☐	
Application Type	Provisional		
Subject Matter	Utility		
Suggested Class (if any)		Sub Class (if any)	
Suggested Technology Center (if any)			
Total Number of Drawing Sheets (if any)	1	Suggested Figure for Publication (if any)	

EFS Web 2.2.2

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1008, p. 18

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062PR
		Application Number	
Title of Invention	METHOD OF PROVIDING HANDSHAKING BETWEEN A MEMORY CONTROLLER HUB AND A MEMORY SUBSYSTEM		

Publication Information:
☐ Request Early Publication (Fee required at time of Request 37 CFR 1.219)

Request Not to Publish. I hereby request that the attached application not be published under 35 U.S.C. 122(b) and certify that the invention disclosed in the attached application **has not and will not** be the subject of an application filed in another country, or under a multilateral international agreement, that requires publication at eighteen months after filing.

Representative Information:

Representative information should be provided for all practitioners having a power of attorney in the application. Providing this information in the Application Data Sheet does not constitute a power of attorney in the application (see 37 CFR 1.32). Enter either Customer Number or complete the Representative Name section below. If both sections are completed the Customer Number will be used for the Representative Information during processing.

Please Select One: ☒ Customer Number ☐ US Patent Practitioner ☐ Limited Recognition (37 CFR 11.9)

Customer Number 20995

Domestic Benefit/National Stage Information:

This section allows for the applicant to either claim benefit under 35 U.S.C. 119(e), 120, 121, or 365(c) or indicate National Stage entry from a PCT application. Providing this information in the application data sheet constitutes the specific reference required by 35 U.S.C. 119(e) or 120, and 37 CFR 1.78(a)(2) or CFR 1.78(a)(4), and need not otherwise be made part of the specification.

Prior Application Status		Remove	
Application Number	Continuity Type	Prior Application Number	Filing Date (YYYY-MM-DD)

Additional Domestic Benefit/National Stage Data may be generated within this form by selecting the **Add** button.

Foreign Priority Information:

This section allows for the applicant to claim benefit of foreign priority and to identify any prior foreign application for which priority is not claimed. Providing this information in the application data sheet constitutes the claim for priority as required by 35 U.S.C. 119(b) and 37 CFR 1.55(a).

Remove			
Application Number	Country ¹	Parent Filing Date (YYYY-MM-DD)	Priority Claimed
			☒ Yes ☐ No

Additional Foreign Priority Data may be generated within this form by selecting the **Add** button.

Assignee Information:

Providing this information in the application data sheet does not substitute for compliance with any requirement of part 3 of Title 37 of the CFR to have an assignment recorded in the Office.

Assignee 1

Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it contains a valid OMB control number.

Application Data Sheet 37 CFR 1.76		Attorney Docket Number	NETL.062PR
		Application Number	
Title of Invention	METHOD OF PROVIDING HANDSHAKING BETWEEN A MEMORY CONTROLLER HUB AND A MEMORY SUBSYSTEM		

If the Assignee is an Organization check here. ☐

Prefix	Given Name	Middle Name	Family Name	Suffix

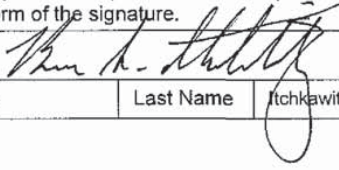
Mailing Address Information:

Address 1			
Address 2			
City		State/Province	
Country		Postal Code	
Phone Number		Fax Number	
Email Address			

Additional Assignee Data may be generated within this form by selecting the Add button.

Signature:

A signature of the applicant or representative is required in accordance with 37 CFR 1.33 and 10.18. Please see 37 CFR 1.4(d) for the form of the signature.

Signature			Date (YYYY-MM-DD)	2009-06-12	
First Name	Bruce	Last Name	Itchkawitz	Registration Number	47677

This collection of information is required by 37 CFR 1.76. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 23 minutes to complete, including gathering, preparing, and submitting the completed application data sheet form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. **SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.**

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8. A record from this system of records may be disclosed, as a routine use, to the public after either publication of the application pursuant to 35 U.S.C. 122(b) or issuance of a patent pursuant to 35 U.S.C. 151. Further, a record may be disclosed, subject to the limitations of 37 CFR 1.14, as a routine use, to the public if the record was filed in an application which became abandoned or in which the proceedings were terminated and which application is referenced by either a published application, an application open to public inspections or an issued patent.
9. A record from this system of records may be disclosed, as a routine use, to a Federal, State, or local law enforcement agency, if the USPTO becomes aware of a violation or potential violation of law or regulation.

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METHOD OF PROVIDING HANDSHAKING BETWEEN A MEMORY
CONTROLLER HUB AND A MEMORY SUBSYSTEM

Certain embodiments described herein provide a method of providing a feedback path from a memory subsystem to the MCH (Memory Controller Hub, e.g., system memory controller) during initialization.

In general, there is no method of handshaking between the MCH and a memory subsystem during initialization since the MCH does not monitor the error-out signal from the memory subsystem. This causes the MCH to perform blind execution. In a standard server (e.g., Intel or AMD or other chipset based), the lack of any handshaking between the MCH and the memory subsystem during the server initialization period has not been a serious issue since the MCH has a complete control over the initialization procedure. However, the recent proposal in JEDEC for LD-DIMM (Load Reduced DIMM) requires the MCH to hand over one or more parts of the initialization operation sequences to the memory subsystem controller, which raises an unprecedented issue to the MCH, and in such configurations, it needs a way of handshaking with the memory subsystem controller.

In general, handshaking can be implemented in two methods; polling and notifying. In the polling method, the MCH reads a status register in the memory subsystem controller to find out if the memory subsystem controller has completed the required operation. However, since the standard DDR2/3 specification does not provide a way to read any registers in the memory subsystem controller, this is not an implementable method. In the notifying method, the memory subsystem controller sends a signal to the MCH when it completes the required or requested operation. This method allows the MCH to execute independent command while it is waiting for a notification signaling for the memory subsystem controller.

Although the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller, the LR-DIMM proposal requires the MCH to insert a waiting period. The shortcoming of the current the LR-DIMM proposal is that, instead of adopting the notification, the proposal requires the MCH to be in

standby (idle, or wait) while the memory subsystem controller completes its task. Under this arrangement, since the standby duration is dependent on the density, speed and configuration of the memory subsystem, the MCH has to insert undefined standby period. In addition, if there are multiple occasions that the MCH needs to hand off its control to the memory subsystem controller, the required MCH wait periods can be different from one occasion to another, and it complicates the correlation between the MCH and the memory subsystem controller.

Certain embodiments described herein provide a method of establishing a handshake mechanism based on the notification signaling. This mechanism can be implemented by adding a new interface (notifying) signal between the MCH and the memory subsystem controller or by adding an additional functionality to an exiting, non-timing critical, signal without altering the memory subsystem hardware (refer to Figure 1). In either case, the interface of certain embodiments is an open drain signaling from the memory subsystem controller to the MCH (refer to Figure 2).

Figure 3 shows the operation of the notifying signal in accordance with an example embodiment. The output of the notifying signal is low impedance while the memory subsystem controller executing each section of the initialization step, thus the notifying signal is pulled low by the memory subsystem controller. As the memory controller completes each step, it drives the notifying signal pin to the high impedance state. This causes the signal to be pulled high by the MCH.

In certain embodiments in which more than one memory subsystem is connected to the MCH, each controller that associates with each memory subsystem drives the notifying signal pin to the high impedance state from the low impedance state when it completes the required operation. Thus, it provides the condition that the MCH can only pull the notifying signal high when all memory subsystem controllers are done with the required operation. This method allows the MCH to work with a non-homogenous memory subsystem, such as mixing of DIMMs with different DIMM density, ranks, DRAM density, speed, DRAM configuration, etc.

Although this method can be easily implemented by adding a pin to the MCH and to the memory subsystem controller, certain such embodiments would require change in hardware or the chipset, which, in many cases, is not feasible to do so. Thus, certain other

embodiments present another method of implementing this function without changing any hardware, but modifying the BIOS.

In the system point of view in accordance with certain embodiments, since the notification of completion of the required or requested task from the memory subsystem controller would generate an interrupt to the system during the initialization period as an error occurrence generates an interrupt to the system during the normal operation, the error-out signal in the current memory subsystem can be used to support the notifying function. Figure 4 shows an example of interrupt handling procedure for the error-handling routine vs. the notifying routine.

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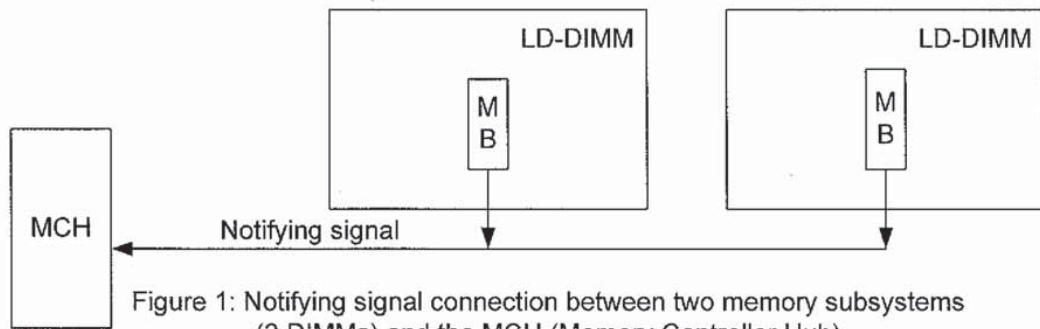


Figure 1: Notifying signal connection between two memory subsystems (2 DIMMs) and the MCH (Memory Controller Hub)

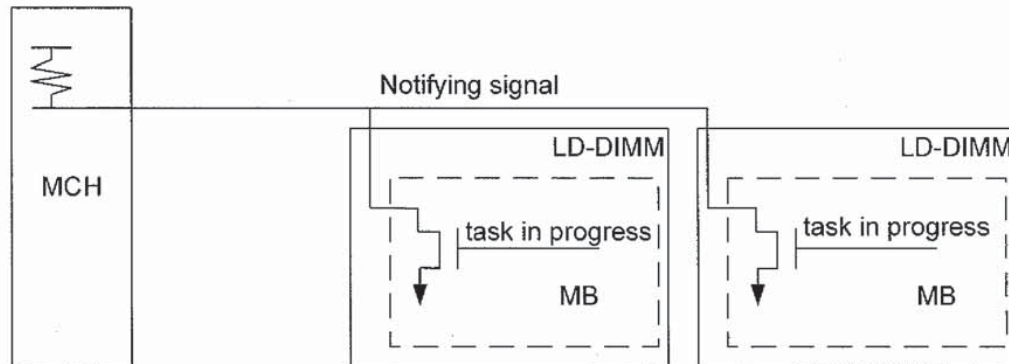


Figure 2: Notifying signal connection between two memory subsystems (2 DIMMs) using Open-Drain method

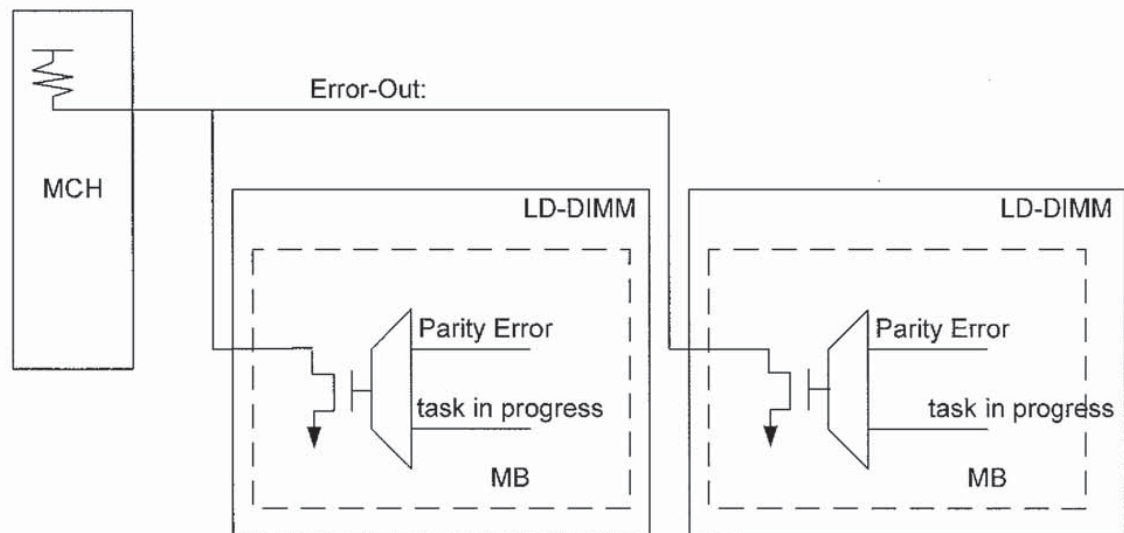


Figure 3: Sharing a pin between the Error-out and Notifying signal

Error-Out pin: Low during MB training (high signal indicates that training is done)
High during normal operation unless a parity error occurs

Electronic Patent Application Fee Transmittal				
Application Number:				
Filing Date:				
Title of Invention:		METHOD OF PROVIDING HANDSHAKING BETWEEN A MEMORY CONTROLLER HUB AND A MEMORY SUBSYSTEM		
First Named Inventor/Applicant Name:		Unknown Unknown		
Filer:		Bruce S. Itchkawitz		
Attorney Docket Number:		NETL.062PR		
Filed as Large Entity				
Provisional Filing Fees				
Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Basic Filing:				
Provisional application filing	1005	1	220	220
Pages:				
Claims:				
Miscellaneous-Filing:				
Petition:				
Patent-Appeals-and-Interference:				
Post-Allowance-and-Post-Issuance:				
Extension-of-Time:				

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Description	Fee Code	Quantity	Amount	Sub-Total in USD(\$)
Miscellaneous:				
Total in USD (\$)				220

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Electronic Acknowledgement Receipt	
EFS ID:	5510898
Application Number:	61186799
International Application Number:	
Confirmation Number:	1666
Title of Invention:	METHOD OF PROVIDING HANDSHAKING BETWEEN A MEMORY CONTROLLER HUB AND A MEMORY SUBSYSTEM
First Named Inventor/Applicant Name:	Unknown Unknown
Customer Number:	20995
Filer:	Bruce S. Itchkawitz/Shirley Martinez
Filer Authorized By:	Bruce S. Itchkawitz
Attorney Docket Number:	NETL.062PR
Receipt Date:	12-JUN-2009
Filing Date:	
Time Stamp:	20:42:50
Application Type:	Provisional

Payment information:

Submitted with Payment	yes
Payment Type	Credit Card
Payment was successfully received in RAM	\$ 220
RAM confirmation Number	5076
Deposit Account	111410
Authorized User	KNOBBE MARTENS OLSON AND BEAR
The Director of the USPTO is hereby authorized to charge indicated fees and credit any overpayment as follows: Charge any Additional Fees required under 37 C.F.R. Section 1.16 (National application filing, search, and examination fees) Charge any Additional Fees required under 37 C.F.R. Section 1.17 (Patent application and reexamination processing fees)	

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File Listing:					
Document Number	Document Description	File Name	File Size(Bytes)/ Message Digest	Multi Part /.zip	Pages (if appl.)
1	Transmittal of New Application	transmittal.pdf	29082	no	1
			e23c91a3149ac20e64ea99b286ec84e041a59ff		
Warnings:					
Information:					
2	Application Data Sheet	ads.pdf	169974	no	4
			3bac741c1d57d88c529f7674c2749ed5fb9db72		
Warnings:					
Information:					
This is not an USPTO supplied ADS fillable form					
3	Specification	specification.pdf	105158	no	3
			b382e365de4630a329d501bd5a77dcd5a4dc7a3d		
Warnings:					
Information:					
4	Drawings-only black and white line drawings	drawings.pdf	24280	no	1
			b1c597c2f3f8ea6302ea28745919e4a392b31f10		
Warnings:					
Information:					
5	Fee Worksheet (PTO-875)	fee-info.pdf	29806	no	2
			d4e60206793478be997258642eeb408d138b35d5		
Warnings:					
Information:					
Total Files Size (in bytes):			358300		

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This Acknowledgement Receipt evidences receipt on the noted date by the USPTO of the indicated documents, characterized by the applicant, and including page counts, where applicable. It serves as evidence of receipt similar to a Post Card, as described in MPEP 503.

New Applications Under 35 U.S.C. 111

If a new application is being filed and the application includes the necessary components for a filing date (see 37 CFR 1.53(b)-(d) and MPEP 506), a Filing Receipt (37 CFR 1.54) will be issued in due course and the date shown on this Acknowledgement Receipt will establish the filing date of the application.

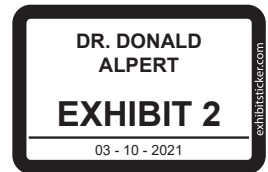
National Stage of an International Application under 35 U.S.C. 371

If a timely submission to enter the national stage of an international application is compliant with the conditions of 35 U.S.C. 371 and other applicable requirements a Form PCT/DO/EO/903 indicating acceptance of the application as a national stage submission under 35 U.S.C. 371 will be issued in addition to the Filing Receipt, in due course.

New International Application Filed with the USPTO as a Receiving Office

If a new international application is being filed and the international application includes the necessary components for an international filing date (see PCT Article 11 and MPEP 1810), a Notification of the International Application Number and of the International Filing Date (Form PCT/RO/105) will be issued in due course, subject to prescriptions concerning national security, and the date shown on this Acknowledgement Receipt will establish the international filing date of the application.

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC. and SK HYNIX AMERICA INC.,
Petitioners,

v.

NETLIST, INC.
Patent Owner

Patent No. 9,858,218

Issued: January 2, 2018

Filed: April 1, 2016

Inventors: Hyun Lee

Title: Memory Module And Methods For Handshaking With A Memory
Controller

Inter Partes Review No. IPR2020-01044

**DECLARATION OF DR. DONALD ALPERT REGARDING U.S. PATENT
NO. 9,858,218**

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
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I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for SK hynix as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent No. 9,858,218 (“the 218 Patent”) (EX1001) and on the patentability of the claims of this patent. The following is my written declaration on these topics.

B. Background and Qualifications

2. I am an independent consultant with Camelback Computer Architecture, LLC. My residence and place of business is at 2020 21st Street, Sacramento, CA 95818. I am over the age of eighteen, and I am a citizen of the United States.

3. I have 45 years of academic and industrial experience in applying, designing, studying, teaching, and writing about microprocessors and computer systems. I received an Electrical Engineering Ph.D. degree in 1984 from Stanford University. I earlier received an Electrical Engineering B.S. degree from MIT in 1973 and an Electrical Engineering M.S. degree from Stanford University in 1978. I have taught classes in computer architecture at Stanford, Tel Aviv, and Arizona State Universities.

4. From 1976 to 1977, I worked at Burroughs Corporation, where I designed peripheral interface controllers, including those for serial data

communications based on Intel 8080 microprocessor components. From 1980 to 1989, I was the lead architect for the design of three high-performance microprocessors at Zilog and National Semiconductor. Later, at Intel, I was the lead architect of the Pentium® Processor from 1989 to 1992 and of the 815 chipset from 1999 to 2000, both of which became the most widely used PC components of their time. The 815 chipset comprised two components: (1) a memory controller hub (MCH) that included a graphics controller and memory controller with interfaces to the CPU, 133 MHz SDRAM system memory modules, an optional, external graphics controller and (2) an I/O controller hub (ICH) that included various I/O controllers (e.g., network, hard drive, USB) for system peripheral devices. Additionally, I served as co-manager for the Itanium processor design from 1993-1997.

5. I am a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE), and served as the chair of the IEEE Technical Committee on Microprocessors and Microcomputers from 1999 to 2000. I was the keynote speaker at the first Cool Chips conference, dedicated to the study of low-power microprocessors and systems. I have given invited lectures at several universities, and published ten papers in various professional journals and conference proceedings. My paper entitled “Architecture of the Pentium Processor,” was selected as best paper in IEEE Micro for 1993. I am a named inventor on over 30

U.S. patents that pertain to microprocessors, computer systems, and related technology.

6. I have reviewed the 218 Patent, and I am familiar with the patent's subject matter, which is within the scope of my education and professional experience. Based at least on my background in academia, industry, and consulting, I am familiar with the issues and technology relating to processors, chipsets, memory, and peripheral devices for computer systems. I have personally analyzed, developed, and tested such computer components and systems. More specifically, the Pentium® Processor and 815 chipset for which I was the lead architect at Intel implemented various features for initializing, calibrating, and testing the memory system, which comprised cache memory, a memory controller, and standard SDRAM modules.

7. My Curriculum Vitae, including my publications and patents, is submitted herewith as EX1004.

C. Compensation and Prior Testimony

8. I am being compensated at a rate of \$550.00 per hour for my study and testimony in this matter. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this investigation. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

9. I have previously submitted declarations in seven IPR proceedings, namely IPR2020-01042, IPR2014-00970, IPR2014-00971, IPR2015-00148, IPR2015-00191, IPR2017-00548, and IPR2018-00303. Additionally I have testified as an expert witness in Federal Court and the ITC, as summarized in EX1004 at 6-7.

D. Information Considered

10. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this report and those listed in the Petition's Attachment B.

11. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions — including documents that may not yet have been provided to me.

12. My analysis of the materials produced in this investigation is ongoing and I will continue to review any new material as it is provided. This report represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. LEGAL STANDARDS FOR PATENTABILITY

13. In expressing my opinions and considering the subject matter of the claims of the 218 Patent, I am relying upon certain basic legal principles that have been explained to me.

14. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made.

15. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as “prior art” and generally includes patents and printed publications (*e.g.*, books, journal publications, articles on websites, product manuals, *etc.*).

16. I understand that in this proceeding the Petitioner has the burden of proving that the claims of the 218 Patent are anticipated by or obvious from the prior art by a preponderance of the evidence. I understand that “a preponderance of the evidence” is evidence sufficient to show that a fact is more likely true than it is not.

17. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. The claims after being construed in this manner are then to be compared to the information in the prior art.

18. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

19. I understand that there are various ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to “anticipate” the claim. Second, the prior art can be shown to have made the claim “obvious” to a person of ordinary skill in the art. Third, I understand that a patent claim may be invalid where the specification of the patent fails to provide a written description adequate to support the claim. Fourth, I understand that a patent claim may be invalid when the claim fails to particularly point out and distinctly claim the subject matter of what the inventor regards as the invention. My understanding of the legal standards is set forth below.

A. Anticipation

20. I understand that the following standards govern the determination of whether a patent claim is “anticipated” by the prior art.

21. I have applied these standards in my evaluation of whether the claims of the 218 Patent would have been anticipated by the prior art.

22. I understand that the “prior art” includes patents and printed publications that existed before the earliest filing date (the “effective filing date”)

of the claim in the patent. I also understand that a patent will be prior art if it was filed before the effective filing date of the claimed invention, while a printed publication will be prior art if it was publicly available before that date.

23. I understand that, for a patent claim to be “anticipated” by the prior art, each and every requirement of the claim must be found, expressly or inherently, in a single prior art reference as recited in the claim. I understand that claim limitations that are not expressly described in a prior art reference may still be there if they are “inherent” to the thing or process being described in the prior art. For example, an indication in a prior art reference that a particular process complies with a published standard would indicate that the process must inherently perform certain steps or use certain data structures that are necessary to comply with the published standard.

24. I understand that if a reference incorporates other documents by reference, the incorporating reference and the incorporated reference(s) should be treated as a single prior art reference for purposes of analyzing anticipation.

25. I understand that it is acceptable to consider evidence other than the information in a particular prior art document to determine if a feature is necessarily present in or inherently described by that reference.

B. Obviousness

26. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

27. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

28. A patent may not be obtained although the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be denied by the manner in which the invention was made.

29. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the asserted claims of the 218 Patent would have been considered obvious as of the priority date of the patent.

30. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I

understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

31. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

32. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of “objective factors”

suggesting the claimed methods are not obvious, and reserve my right to address any such evidence if it is identified in the future.

33. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

34. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a Skilled Artisan would recognize that it would improve similar devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

35. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the “ordinary innovation” and experimentation that

does no more than yield predictable results, which are inferences and creative steps that a Skilled Artisan would employ.

36. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

37. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words “teaching, suggestion, and motivation.” I understand that in 2007, the Supreme Court issued its decision in *KSR Int’l Co. v. Teleflex, Inc.*, 550 U.S. 398 (2007), where the Court rejected the previous requirement of a “teaching, suggestion, or motivation to combine” known elements of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that *KSR* confirms that any motivation that would have been known to a person of skill in the art, including common sense, or derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

38. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the

same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond the particular application being described in a reference, that if something can be done once it is obvious to do it multiple times, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

39. I understand that obviousness does not require that the features of a secondary reference be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to a Skilled Artisan. The disclosures of the prior art references need not be physically combinable. Combining the teachings of references should be the focus of the analysis.

40. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or lead away from the line of inquiry

disclosed in the reference(s). A reference does not “teach away” from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

41. I understand that a person of ordinary skill is also a person of ordinary creativity.

42. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was “obvious to try” may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or

leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

III. THE 218 PATENT

A. Effective Filing Date of the 218 Patent

43. The 218 Patent is a continuation of, inter alia, a utility application filed June 14, 2010, and also claims priority to U.S. Provisional Application No. 61/186,799 (EX1008), filed June 12, 2009. EX1001, Face. I have been asked to give my opinion as to whether, from the perspective of a Skilled Artisan, the provisional application shows that the inventor actually invented what is claimed in each of the claims of the 218 patent, and possessed the claimed subject matter, as of the provisional filing date. When considering that question, I have considered whether the provisional explicitly or inherently discloses the elements of the claims. To determine whether the provisional inherently discloses an element, I considered whether any element not explicitly disclosed would be necessarily comprehended in the description provided by a Skilled Artisan. I conclude that certain elements of some claims are not adequately disclosed in the provisional.

1. Unsupported Negative Limitation – Claims 7, 9, 15

44. Each of independent claims 9 and 15 (and claim 7 that depends from claim 1) include a negative limitation requiring “train[ing] with one or more training sequences *while the first edge connections [i.e., for data] are **not** active.*” *E.g.*, EX1001, 15:60-61 (claim 9), 16:48-50 (claim 15), 15:31-34 (claim 7).

45. There is no disclosure in the provisional of training “while the first edge connections are not active.” The single sentence fragment of the provisional referencing training – “Error-Out pin: Low during MB training (high signal indicates that training is done)” (EX1008, 25) – never describes such a relationship between “training” and edge connections, either explicitly or implicitly. Indeed, edge connections are not even mentioned in the provisional application, let alone associated with “training.” Moreover, it does say: “This method allows the MCH to execute independent command while it is waiting for a notification signaling for the memory subsystem controller.” EX1008, 22. If anything, this suggests read and write operations very much may be occurring during the disclosed “MB training.”

46. Moreover, it was known before the 2009 provisional filing date that some training included sending data over the data edge connections, while other training did not. Specifically, a Skilled Artisan would understand the provisional’s “MB training” as a generic reference to “training” in the context of memory buffers. To the extent one might argue it refers to something more specific, a Skilled Artisan would, at most, understand the phrase in this context (where the provisional refers to the then current LRDIMMs under development/standardization, DDR3 LRDIMM) as referring to training of the

interfaces to/from and/or operations of the type of register/buffer used in DDR3 LRDIMMs. EX1036, 4.

47. It was known, however, that such buffers employed memory read and write operations instituted by the memory controller that transferred data over the edge connections with the data pins (“*first edge connections*”) during some training modes. For instance, JEDEC, a ballot on a draft DDR3 LRDIMM standard, discloses training modes for the MB that employ memory read and write operations instituted by the system memory controller that transferred data over the edge connections with the data pins (“*first edge connections*”) during the training mode and some that do not. EX1015, 8-9 (“Host-MB Training” employing memory read and write operations), 8 (“MB-DRAM Training” not employing memory read or write operations); *see also* EX1039, 7-9, 11 (presentation dated June 4, 2009 disclosing “Host-MB Training” and “MB-DRAM Training” before June 12, 2009 provisional filing date); *see also* EX1046, 1-2, 21 (June 4, 2009 meeting minutes noting EX1045 presentation discussed). I note that, in MB-DRAM Training, at least one JEDEC document (EX1039, 7-9) at the time suggests the memory buffer performs operations such as pre-charge, but those would not be considered “memory read or write operations” per the claims because they are not performed by the system memory controller (rather the memory buffer performed them). As another example, Talbot discloses that during normal operations read

and writes are stored in FIFO 220 in the buffer, and are then passed on to DRAM. EX1022, ¶¶ [0039], [0043]. Additionally, during training, the controller may write data, which is also stored in FIFO 220; however, in this case, the data is not passed to DRAM. EX1022, ¶[0053]. Thus, it is my opinion that Patent Owner cannot show from the provisional's disclosure that the negative limitation that "*the first edge connections [i.e., for data] are not active*" during training "is necessarily comprehended" in that disclosure because it was known that some types of "MB training" did in fact include active first edge connections on which data was being transferred.

2. Unsupported Negative Limitation – Claim 1

48. Claim 1 requires that its memory module be "configured to perform one or more memory read or write operations *not associated with the one or more training sequences* by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections." EX1001, 14:57-62. However, the terms "read operation," "write operation" (or just "write"), "data signals" (or just "data"), "edge connections" (or just "edge"), "address signals" (or just "address"), and "command signals" appear nowhere in the provisional. There are, however, two passing references to "normal operation" in the provisional, and perhaps Patent Owner will argue that necessarily provides support for all the aforementioned terms and their interrelations during

“normal operation.” But nothing in the provisional says that its “training” is necessarily excluded from its “normal operation.” In fact, it is my opinion that a Skilled Artisan would understand training could occur during normal operation. For instance, Buchmann discloses the options of utilizing either “memory channel repair and re-initialization” or “fast repair and re-initialization,” both of which employ some of Buchmann’s training and which may (though not necessarily) occur during “functional mode,” which Buchmann describes as “normal, run-time operation.” EX1016, 12:60-13:41. During that “functional mode” when errors are encountered, either “repair” or “fast repair” is utilized before a “retry command,” and occurs so fast “other system components will not time-out during the repair and re-init process.” *Id.*, 13:29-34.

49. It is my opinion that the provisional should have disclosed how its reads/writes (which it does not explicitly disclose in any event) are unassociated with its training (which is just a generic reference to “MB training”), if Patent Owner wanted to provide a written description of this negative limitation.

3. “One or More” Training “Sequences”

50. Each independent claim of the 218 Patent also requires its memory module to be “configured to be trained with one or more training sequences” or “training with one or more training sequences.” EX1001, 14:55-56 (claim 1), 15:60 (claim 9), 16:48-49 (claim 15).

51. The provisional, however, only discloses a single “MB training”, that a Skilled Artisan would understand as a generic disclosure of “training” a memory buffer in some way. It does not disclose any training “sequences,” and particularly not “one or more” training sequences. Indeed, the phrases “train sequence” and “training sequences” are completely absent from the provisional. A Skilled Artisan would not “necessarily comprehend” “one or more training sequences” from the bare disclosure of “MB training” as of June 12, 2009.

B. Person Of Ordinary Skill in the Art

52. Based on my experience and the prior art I discuss herein, I believe a person of ordinary skill in the art in the field of the 218 Patent would be someone who was familiar with computer memory systems and basic CPU architecture documented in the computer/memory architecture literature and generally available in commercial systems as of 2009-10. Such literature and commercial systems would have included techniques related to how computer components access a computer’s memory, including the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system. They would also include schemes for initialization of computer systems, including initialization/training of memory components. Such a person would also have been familiar with the standards that govern the operation of memory devices. The person of ordinary

skill in the art would have had a bachelor's degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. Alternatively, such a person could have had equivalent combinations with more or less education and less or more experience.

C. Overview of The 218 Patent

53. The 218 Patent states that it describes “a method of establishing a handshake mechanism based on notification signaling.” EX1001 (218 Patent) at 4:1-3. The 218 Patent explains that “this [handshake] mechanism can be implemented by adding a new interface (notifying) signal between the MCH [i.e., system memory controller] and the memory subsystem controller, or by adding an additional functionality to an existing, non-timing critical signal without altering the memory subsystem hardware.” EX1001 (218 Patent) at 4:3-8. The 218 Patent further explains that this interface “can be an open drain signaling from the memory subsystem controller to the MCH [i.e., system memory controller].” EX1001 (218 Patent) at 4:8-12.

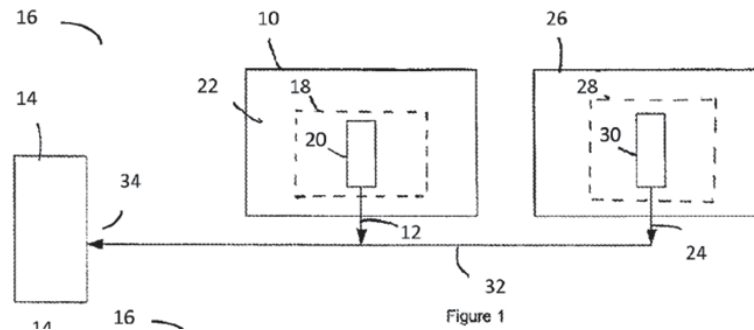
54. According to the 218 Patent, before the patent “[i]n general, there [was] *no existing method of handshaking* between the MCH (e.g., system memory controller) and a memory subsystem (e.g., memory module) during initialization.” EX1001 (218 Patent) at 2:59-62 (emphasis added). The patent states that “in conventional systems, the system memory controller does not monitor the error-out

signal from the memory subsystem.” *Id.*, 2:62-64. The 218 Patent states that “typical” servers of the prior art would instead, after commencing an initialization function in a memory module, simply wait a predetermined amount of time and then assume the memory subsystem had completed initialization. EX1001 (218 Patent) at 2:65-3:17.

55. The 218 Patent suggests that use of “handshaking” between memory controller and memory module (i.e., exchanging information about the completion of the initialization procedure) would be a better idea. EX1001 (218 Patent) at 2:53-62. It states that, generally, “handshaking can be implemented in at least two ways; polling and notifying.” EX1001 (218 Patent) at 3:38-39. The 218 Patent claims that polling is “generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation,” thus causing the controller to “wait longer than necessary to poll the memory subsystem, thereby delaying the overall initialization process.” EX1001 (218 Patent) at 3:44-50. It further states that “the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller.” EX1001 (218 Patent) at 3:51-61.

56. The 218 Patent provides only limited detail on what it purports to be the inventive system. Figure 1, for example (below), depicts the preferred embodiment. That figure shows a computer system including memory module 10

coupled to a memory controller 14 via “output 12” which is driven by notification circuit 20 of controller circuit 18.



EX1001 (218 Patent) at 4:19-37, FIG. 1. Memory module 26 is also shown, and has essentially in the same structure as module 14, having “output 24” driven by notification circuit 30 of controller circuit 28. *Id.*, 6:11-40.

57. In one specific example of handshaking described in the 218 Patent, the interface between the memory controller (MCH) and memory subsystem controller (of the memory module) is implemented using a technique called open drain signaling. EX1001 (218 Patent) at 4:8-12; *see also id.*, 9:43-49, FIGs. 2-3. Specifically, output 12 of module 10 and output 24 of module 26 are both tied to the same bus 32 using an open drain configured transistor. EX1001 (218 Patent) at 4:19-37, 9:43-67, FIGs. 2-3.

58. In that configuration, when starting an initialization procedure, each memory module will drive high the gate of the transistor with the open drain output, placing a logic level low (low impedance) signal on bus 32. When the

initialization is complete, the memory module can drive low the gate of the transistor with the open drain output, placing a logic level high (high impedance) signal on bus 32. However, because all of the outputs of multiple memory modules are tied to the same bus 32 in an open drain configuration, the state of bus 32 will remain logic level low (low impedance) until each memory module drives low the gate of the transistor of its open drain output, placing a logic level high (high impedance) on its output, which then allows “the bus 32 [to] be pulled high by the internal pull-up configuration 40 of the system memory controller 14.” EX1001 (218 Patent) at 9:43-10:46. In this manner, the system memory controller may be provided the status of an initialization procedure (*e.g.*, either that it is currently executing or complete) using only a single bus line from multiple memory modules. *Id.* The 218 Patent further states that bus 32 could be tied to a standard-defined (such as JEDEC) error output pin that is not required by the standard to be used during initialization. EX1001 (218 Patent) at 7:66-8:29.

59. The patent further states that output 12 can be operatively coupled to the error-out pin of the memory module 10, which is connected to a multiplexor 42 driving the transistor 36 with either of a task_in_progress signal 44 or an error signal 46 (*e.g.*, parity error signal). EX1001 (218 Patent) at 11:16-20, FIG. 3. According to the 218 Patent, “the memory module 10 can be advantageously configured to both perform the standard (*e.g.*, JEDEC-specified) error reporting

functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode.” EX1001 (218 Patent) at 11:26-31.

D. The Prosecution History of The 218 Patent

1. 115 Application (The 218 Patent)

60. The 218 Patent issued from the 115 Application. The 115 Application presented 20 claims, 1-20. EX1002 (115 Application File History) at 30-33 (Application at 20-23). On May 20, 2016, the examiner rejected claims 1-20 on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 9,311,116 and claims 1-18 of U.S. Patent No. 8,489,837. EX1002 (115 Application File History) at 49-57. Claims 1-20 were rejected also under 35 U.S.C. 103(a) as being unpatentable over Tanguay (Ex. 1009, US 2010/0042778) in view of Roohparvar (Ex. 1010, US 2003/0115427). *Id.*

61. In response, the applicants of the 115 Application cancelled claims 1-20, and added new claims 21-42. EX1002 at 68-81. The applicants also filed a terminal disclaimer to overcome the nonstatutory double patenting rejections. *Id.*

62. On November 25, 2016, the examiner rejected claims 21-42 as being unpatentable over Moshayedi (Ex. 1011, U.S. 2010/0202240) in view of Fahr (Ex. 1012, U.S. 2008/0256281). EX1002 (115 Application File History) at 100-107.

63. On April 25, 2017, the applicants of the 115 Application filed a Response. EX1002 (115 Application File History) at 132-144. In the Response, the applicants amended claims 21 and 35 to “address issues with antecedent basis and for better clarity.” *Id.* at 138.

64. The applicants further argued that the Applicant is left to guess what the Examiner’s rationale is in rejecting the claims under Moshayedi in view of Fahr, because Moshayedi shows several outputs including “CACHE_DIRTY, DRAM_AVAILABLE, NVDIMM_READY, TEST_TX, and VBACK_RESET,” that cannot be “an open drain output” outputting “a signal indicating a parity error.” EX1002 at 139-141. The applicants further argue that Moshayedi fails to disclose “configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory read, write, pre-charge, or refresh operations and to control the memory elements in accordance with the address and command signals,” *id.* at 142, and “wherein the module controller is further configured to process one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation, and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection.” *Id.* at 143.

65. The applicants further argued that Fahr does not make up for the deficiency of Moshayedi, because the Fahr describes “two open-drain outputs for two different error signals, /Error (CE) 120 and /Error (UE) 121, respectively,” while the claim requires “that the module controller ‘outputs to the memory controller a signal indicating a parity error’ AND ‘is further configured to drive a notification signal associated with the one or more training sequences to the memory controller’ **via the same open-drain output.**” EX1002 (115 Application File History) at 143.

66. On May 25, 2017, the applicants of the 115 Application further filed an Amendment, amending claims 21, 22, 28-29, 34-36, and 42, responding to the Final Office Action dated November 25, 2016. EX1002 (115 Application File History) at 167-179. In this Amendment, the applicants made similar arguments as in its April 25, 2017 Response. *Id.*

67. On May 31, 2017, the applicants of the 115 Application conducted an interview with the Examiner, discussing “the AFCP 2.0 filed 04/25/17 and potential claim amendments to overcome the art of record.” EX1002 (115 Application File History) at 182.

68. On June 16, 2017, the examiner rejected claims 21-42. EX1002 (115 Application File History) at 184-191. In particular, the examiner rejected claims 21-42 under 35 U.S.C. 112(a), as failing to comply with the written description

requirement, because the newly added limitations to claims 21, 29, and 35 (*i.e.*, “wherein the one or more training sequences are not associated with any memory read or write operation,” “while the memory module is not performing any memory read or write operation,” “while the memory module is not performing any memory read or write operation,” respectively) are not supported by the original disclosure and constitute new matter. EX1002 (115 Application File History) at 186-187. The examiner further rejected claims 21-42 as being unpatentable over Moshayedi (Ex. 1011, U.S. 2010/0202240) in view of Fahr (Ex. 1012, U.S. 2008/0256281) and Goishi (Ex. 1013, U.S. 2010/0142383). EX1002 (115 Application File History) at 188-190.

69. On July 14, 2017, the applicants of the 115 Application conducted an interview with the Examiner, discussing “the rejection of claims 21-42 under 35 USC 112 first paragraph and 35 USC 103 over Moshayedi (20100202240), Fahr (20080256281), and Goishi (20100142383), as well as potential claim amendments to overcome the pending rejections.” EX1002 (115 Application File History) at 201.

70. On September 18, 2017, the applicants of the 115 Application filed an Amendment, amending claims 21, 27-29, 33-35, and 41-42, responding to the Non-Final Office Action dated June 16, 2017. EX1002 (115 Application File History) at 203-216. In this Amendment, the applicants made similar arguments as

in its April 25, 2017 Response with respect to Mosheyedi and Fahr. EX1002 (115 Application File History) at 210-216. The applicants further argued that Goishi does not make up for the deficiencies of Moshayedi and Fahr without any substance. EX1002 (115 Application File History) at 216.

71. On October 12, 2017, the examiner issued a notice of allowance, allowing claims 21-42 of the 115 Application. EX1002 (115 Application File History) at 228-232.

2. 745 Application (The 623 Patent)

72. The 623 Patent issued from U.S. Patent Application 15/169,745. The 745 application presented 37 claims. The 745 application was accorded a filing date of June 1, 2016.

73. On July 29, 2016, the claims were rejected “on the ground of nonstatutory double patenting as being unpatentable over claims 1-20” of the 116 Patent, requiring Patent Owner to file a terminal disclaimer to overcome the rejection:

Although the claims at issue are not identical, they are not patentably distinct from each other because the [pending] claims ... make obvious the claims of the issued patents and vice versa.

EX1038, 57, ¶3. Patent Owner likewise had to file a terminal disclaimer over the 837 Patent when prosecuting the application that became the 623

Patent. EX1038, 79 (disclaiming over application that issued as '218 patent, which disclaims over the '837 patent); EX1005, 61.

3. 721 Application (The 116 Patent)

74. The 116 Patent issued from the 721 Application. The 721 Application presented 15 claims, 1-15. Ex. 1006 (721 Application File History) at 27-29.

75. On August 5, 2014, the applicants of the 721 Application filed a Preliminary Amendment amending claims 1 and 11-15, canceling claims 4 and 8-10, and adding new claims 16-24. Ex. 1006 (721 Application File History) at 54-60.

76. On May 22, 2015, the examiner rejected claims 1-7 and 11-24 on the ground of nonstatutory double patenting as being unpatentable over claims 1-18 of U.S. Patent No. 8,489,837. Ex. 1006 (721 Application File History) at 64-69.

77. On August 24, 2015, the applicants of the 721 Application filed a terminal disclaimer to overcome the double patenting rejection. Ex. 1006 (721 Application File History) at 74-80, 86.

78. On November 16, 2015, the examiner issued a Final Office Action maintaining the double patenting rejection noting that “[t]he person who signed the terminal disclaimer is not an attorney or agent of record, is not recognized as an officer of the assignee, and has not been established as being authorized to act on behalf of the assignee.” Ex. 1006 (721 Application File History) at 92.

79. On January 21, 2016, the applicants of the 721 Application filed a “properly signed terminal disclaimer” to overcome the double patenting rejection. Ex. 1006 (721 Application File History) at 97, 99-104.

80. On February 24, 2016, the examiner issued a Notice of Allowance, allowing claims 1-3, 5-7, and 11-24 of the 721 Application. Ex. 1006 (721 Application File History) at 115-119.

4. 339 Application (The 837 Patent)

81. The 837 Patent issued from the 339 Application. The 339 Application presented 20 claims, 1-20. Ex. 1007 (339 Application File History) at 28-31 (Application at 21-24). On September 14, 2012, the examiner rejected claims 1-3, 5, 7, 11, 14, and 19, and allowed claims 4, 6, 8-10, 12, 13, 15-18, and 20. Ex. 1007 (339 Application File History) at 57-69. Claims 5 and 11 were rejected under 35 U.S.C. 112, first paragraph. Ex. 1007 (339 Application File History) at 60-61. Claims 1-3, 5, 7, 11, 14, and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tanguay (Ex. 1009, US 2010/0042778) in view of Roohparvar (Ex. 1010, US 2003/0115427). Ex. 1007 (339 Application File History) at 61-67.

82. In response, the applicants of the 339 Application noted that the examiner’s 112 rejection must have referred to claims 5 and 14 not 5 and 11, and cancelled claims 5 and 14. EX1007, 90.

83. The applicants of the 339 Application also amended claims 1, 4, 11, and 19. Claim 1 was amended to add “wherein the at least one notification signal triggers the memory controller to execute an interrupt routine,” claim 4 was amended to remove “and the memory controller is responsive the at least one notification signal indicating completion of the at least one initialization sequence by triggering execution of an interrupt routine by the memory controller.” Ex. 1007 at 85. According to the applicants, the amendment to claim 1 rendered claims 1-3 patentable over Tanguay in view of Roohparvar. EX1007, 91.

84. On April 29, 2013, the examiner issued a notice of allowance, allowing claims 1-4, 6-13, and 15-20 of the 339 Application. EX1007, 121.

5. IPR2018-00303

85. U.S. Patent No. 9,535,623 (“623 Patent”) is related to the 218 Patent. Both the 623 Patent and the 218 Patent claims priority to and share the specification of the same parents (*e.g.*, 218 Patent and 837 Patent). The claims of both 218 Patent and 623 Patent are strikingly similar. Just by way of example, claim 1 of both patents arise directed to a memory module on a printed circuit board having various edge connections, including an error edge connection. Ex. 1001 at claim 1; Ex. 1031 at claim 1. Both require that the module operate in two modes, one for normal operation and one for training. *Id.* And both require an

open drain output that is used both for parity error during normal operation and for a notification signal during training. *Id.*

86. SK hynix filed a petition for inter partes review of the 623 Patent based primarily on US Patent Publication 2008/0098277, dated April 24, 2008 (“Hazelzet”) combined separately with several different references, most important for purposes of my analysis here US Patent 8,139,430, issued March 20, 2012 (“Buchmann”). Ex. 1032 (623 IPR Petition) at 61-67.

87. SK hynix’s petition also relied on my analysis and testimony concerning the obvious combination of Hazelzet and Buchman. In particular, I demonstrated in my direct testimony that Hazelzet, Buchmann and the 623 Patent were analogous art, Ex. 1033 (623 Patent IPR Declaration) at ¶172, and that Hazelzet and Buchman could be combined such that the same open drain output of Hazelzet could be used for a parity error signal during normal operations, as disclosed in Hazelzet, and also for a training sequence notification signal, such as “TS0_done,” “TS3_ack,” and “TS3_done,” as disclosed in Buchmann, Ex. 1033 (623 Patent IPR Declaration) at ¶167, 170; *see also id.* at ¶¶164-174.

88. I further demonstrated that a person of ordinary skill in the art would have been motivated to make this combination because, among other things, it would have improved overall system reliability, EX1033, ¶173, would have complemented Hazelzet’s existing initialization sequence, *id.* at ¶174, and “would

have been merely a use of prior art techniques for prior art purposes with only expected results,” *id.* at ¶175.

89. The Board issued a Final Written Decision in IPR2018-00303 on March 21, 2019, finding all claims of the 623 Patent unpatentable based on, among other grounds, the obvious combination of Hazelzet and Buchmann. Ex. 1034 (623 Patent IPR, Final Written Decision) at 21. In coming to that conclusion, the Board stated that “we agree with Petitioner’s showing that the combination of Hazelzet and any one of Buchmann or Talbot teaches every limitation of claims 1, 12, and 21 of the ’623 patent and that a person of ordinary skill in the art would have had reason, with rational underpinning, to combine the references.” Ex. 1034 (623 Patent IPR, Final Written Decision) at 13. In support of that conclusion, the Board stated “[f]urther, we credit Dr. Alpert’s supporting testimony (Ex. 1003 ¶¶ 121–150, 158–186), as it is consistent with the prior art disclosures.” Ex. 1034 (623 Patent IPR, Final Written Decision) at 13.

90. The Board’s Final Written Decision in IPR2018-00303 was not provided to the examiner of the 218 Patent, as IPR2018-00303 largely occurred after the 218 Patent issued.

91. I have been asked to consider whether the examiner erred in a manner material to the patentability of claims challenged here. In my opinion, the examiner of the 218 Patent erred in permitting the 218 Patent to issue, given that

the claims of both 218 Patent and 623 Patent are strikingly similar. The only arguable distinction is that the 623 Patent requires “a notification signal indicating ... status of one or more training sequences” while the 218 Patent requires “a notification signal associated with the one or more training sequences.” Ex. 1001 at claim 1; Ex. 1031 at claim 1. However, that distinction cannot justify the examiner’s decision to allow the 218 Patent, because “*a notification signal indicating ... status of one or more training sequences*” is within the scope of “*a notification signal associated with the one or more training sequences.*”

92. Below, in §§IV-**Error! Reference source not found.**, I repeat my analysis demonstrating that a Skilled Artisan would have found the combination of Hazelzet and Buchmann to be obvious, and motivated by the prior art knowledge of such a person, as evidence by multiple exhibits not discussed by the examiner of the 218 Patent. I also point out that the Board has already found such evidence to be credible during the IPR on the 623 Patent.

E. Challenged Claims of the 218 Patent

93. This declaration relates to claims 1-22 of the 218 Patent. Those claims read as follows:

Claim	Claim Language
1.a	1. A memory module operable with a memory controller of a host system, comprising:
1.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;
1.c	dynamic random access memory elements on the printed circuit board;
1.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and
1.e	[i] wherein the memory module is operable in at least a first mode and a second mode, [ii] wherein the memory module in the first mode is configured to be trained with one or more training sequences;

1.f	wherein the memory module in the second mode is configured to perform one or more memory read or write operations not associated with the one or more training sequences by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections;
1.g	[i] wherein the module controller is configured to receive via the second edge connections the address and command signals associated with the one or more memory read or write operations and [ii] to control the dynamic random access memory elements in accordance with the address and command signals, and
1.h	wherein the module controller is further configured to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the second mode;
1.i	wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output while the memory module is in the first mode.

2	2. The memory module of claim 1, wherein the module controller comprises an integrated circuit.
3	3. The memory module of claim 1, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.
4	4. The memory module of claim 3, wherein the notification circuit is configured to drive the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
5	5. The memory module of claim 4, wherein the notification circuit is configured to drive the parity error signal by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
6	6. The memory module of claim 4, wherein the notification circuit is configured to drive the notification signal using one or more OR logic elements.

7	7. The memory module of claim 1, wherein the first edge connections are not active when the memory module is in the first mode and configured to be trained with the one or more training sequences.
8	8. The memory module of claim 1, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences.
9.a	9. A method performed by a memory module operating with a memory controller of the host system,
9.b	the memory module including dynamic random access memory elements on a printed circuit board,
9.c	the printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections via which the dynamic random access memory devices communicate data with the memory controller, second edge connections via which the memory module receives address and command signals from the memory controller, and an error edge connection in addition to the first edge connections and the second edge connections, the method comprising:

9.d	receiving from the memory controller address and command signals associated with one or more memory read or write operations;
9.e	controlling the dynamic random access memory elements in accordance with the address and command signals;
9.f	outputting to the memory controller via an open-drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module; and
9.g	training with one or more training sequences while the first edge connections are not active, and
9.h	driving a notification signal associated with the one or more training sequences to the memory controller via the open drain output and the error edge connection.
10	10. The method of claim 9, wherein driving the notification signal comprises driving a gate of each of one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground, the one or more transistors each having an open drain coupled to the open drain output.

11	11. The method of claim 10, wherein driving the signal indicating the parity error comprises driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground.
12	12. The method of claim 10, wherein driving the notification signal comprises using one or more OR logic elements.
13	13. The method of claim 9, wherein the memory module is configured to be trained with the one or more training sequences in response to a request by the memory controller.
14	14. The method of claim 9, wherein the notification signal indicates a status of the one or more training sequences.
15.a	15. A memory module operable with a memory controller of a host system, comprising:

15.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and command signals, and an error edge connection in addition to the first edge connections and the second edge connections;
15.c	dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the first edge connections; and
15.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection;
15.e	wherein the memory module is configurable to perform at least a first operation and a second operation;

15.f	[i] wherein the module controller in the first operation is configured to receive via the second edge connections address and command signals associated with one or more memory read or write operations and [ii] to control the dynamic random access memory elements in accordance with the address and command signals,
15.g	wherein the module controller in the first operation is further configured to output to the memory controller a signal indicating a parity error having occurred in the memory module; and
15.h	wherein the memory module in the second operation is configured to be trained with one or more training sequences while the first edge connections are not active, and
15.i	wherein the module controller in the second operation is configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output of the module controller.
16	16. The memory module of claim 15, wherein the module controller comprises an integrated circuit.

17	17. The memory module of claim 15, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.
18	18. The memory module of claim 17, wherein the notification circuit is configured to generate the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
19	19. The memory module of claim 18, wherein the notification circuit is configured to drive the signal indicating the parity error by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.
20.	20. The memory module of claim 18, wherein the notification circuit is configured to drive the notification signal using one or more OR logic elements.
21	21. The memory module of claim 15, wherein the memory module is configured to perform the second operation in response to a command from the memory controller.

22	22. The memory module of claim 15, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences.
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F. Construction of Terms Used in the 218 Patent Claims

94. I understand that claim terms should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. As detailed in my analysis and set forth below, I have used what I believe to be the ordinary and accustomed meaning of the claim terms as understood by one of ordinary skill in the art in view of the 218 Patent and its file history.

1. “memory read or write operations”

95. It is my opinion that a Skilled Artisan would understand the ordinary meaning of “*memory read and write operations*” to be operations used to communicate data between the memory module and the memory controller in response to commands from the memory controller.

96. In the claims, “*memory read and write operations*” refers to operations used to read or write DRAMs in response to address and control signals received from the system memory controller. EX1001, 16:37-46. For example, claim 1 requires:

wherein the module controller is configured to **receive via the second edge connections the address and command signals** associated with the **one or more memory read or write operations** and to control the dynamic random access memory elements in accordance with the address and command signals, and wherein the module controller is further configured to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the second mode

EX1001, 14:63-15:6 (emphasis added).

97. Similarly, the 218 Patent specification explains that “[d]uring the read/write operations, the memory module **communicates data** with the memory controller via the data signal pins **in response to second memory commands received via the address and control signal pins.**” EX1001, 1:52-56 (emphasis added). It further states that, during such operations, the module controller will transmit the command and address signals received from the system memory controller to the memory devices. EX1001, 5:40-47. The intrinsic record therefore confirms that this phrase refers to operations used to read from or write to memory devices in response to commands from the memory controller.

2. “mode”

98. It is my understanding that a Skilled Artisan would give “mode” its plain and ordinary meaning after reviewing the 218 Patent and its prosecution history.

99. The 218 Patent uses the term “mode” in accordance with the plain and ordinary meaning. EX1001, Abstract, 1:38-3:10, 4:24-37, 5:61-6:9, 6:41-52. I understand that during the 837 Patent IPR, Patent Owner sought to have the term “mode” interpreted to mean “a distinct behavioral state that a system may be switched to.” EX1035, 7.

100. In addition, based on the word “distinct” Patent Owner argued that that different “modes” must necessarily include mutually exclusive operations. EX1041, 6. However, this is inconsistent with the disclosure of the 837 Patent, and of the 218 Patent, that the disclosed memory operations may be used in both an operational mode and in an initialization mode. EX1001, 6:46-52.

For example, the system memory controller 14 may cause the memory module 10 to perform standard operations such as memory read/write, pre-charge, refresh, etc., while **in operational mode**, although it will be appreciated that one or more of these operations can also be performed by the memory module 10 while **in initialization mode** in certain embodiments.

EX1001, 6: 46-52 (emphasis added).

101. I also understand that in IPR2017-00548 the Board declined to construe the word “*mode*.” EX1035, 7. As the intrinsic record here never defines the term “*mode*” or uses it in any special sense, the Board should take the same approach here.

102. Finally, should a construction be necessary, as I explained in the 623 patent IPR, I agree that the word “state” – when understood without all of the implicit limitations Patent Owner sought to have read into the claims in the 837 Patent IPR – is a synonym for “mode” in the context of the 218 Patent. For instance, a “second mode” in which the module “perform[s] operations related to one or more training sequences” is a “state” of the module in which operations related to one or more training sequences are performed. That word “state” is consistent with the disclosures of the 218 Patent and the dictionary Patent Owner has provided in the IPR for the parent 837 Patent. While Patent Owner’s dictionary uses the phrase “operational state,” Ex. 1047, 3, it is using “operational” more broadly than the 218 Patent, since the patent explicitly equates the disclosed “operational mode” with normal memory operations and the dictionary includes no such limitation. EX1001, 6:41-46; Ex. 1047, 3. Construing “mode” to mean “state” therefore captures the ordinary meaning of “mode” and avoids any confusion from the inconsistent use of the word “operational.” To be clear, I do not believe interpreting “mode” to mean “state” alters the analysis set forth in my

declaration, since in my view the two words mean the same thing to a person of skill in the context of the 218 patent.

3. “training sequence”

103. It is my opinion that a Skilled Artisan would understand the ordinary meaning of “*training sequence*” to be a set of operations occurring in a particular order and used for training.

104. Generally, a “sequence” is “a set of related events, movements, or things that follow each other in a particular order.” EX1042, 1.

105. Further, the 218 Patent provides very few details concerning the disclosed “*training sequences*.” What is shown is only that (1) the “*training sequences*” are controlled by the memory module, EX1001, 3:28-31 (“the MCH according to such a scheme may give control to the local memory controller of a memory subsystem (*e.g.*, memory module) for execution of a training sequence.”), (2) that a module may carry out more than one, and (3) that they may be part of an “initialization sequence.” *Id.*, 6:16-19 (“the memory controller 14 issues a first command to the memory module 10, and, in response, the memory module 10 executes an initialization sequence (*e.g.*, one or more training sequences)”).

106. During IPR2018-00303, relating to the 623 Patent (which as noted above shares a specification with the 218 Patent and includes similar claims), the Board found that Buchmann’s TS3 training operations satisfied the “*training*

sequence” claimed in the 623 Patent. EX1034, 11-12. The TS3 operations are a set of operations carried out in a particular order to perform upstream lane training and repair. EX1016, 5:40-44. Indeed, Buchmann explicitly describes his different sets of training operations as “training sequences.” EX1016, 3:49-52, 14:38-41.

107. Thus, “*training sequence*” should be construed to mean a set of operations occurring in a particular order and used for training.

IV. OVERVIEW OF THE PRIOR ART

A. Prior Art

1. U.S. Patent Publication No. 2008/0098277 to Hazelzet (Ex. 1014)

108. U.S. Patent Publication No. 2008/0098277 to Hazelzet (“Hazelzet”) (Ex. 1014) was filed on October 23, 2006 and published on April 24, 2008. I understand that Hazelzet is prior art to the 218 Patent. Hazelzet is entitled “High Density High Reliability Memory Module With Power Gating and a Fault Tolerant Address and Command Bus” and discloses such functionality. Ex. 1014 (Hazelzet) at Title.

109. Hazelzet discloses memory modules that can operate in an “ECC mode” or a “parity mode.” Ex. 1014 (Hazelzet) at ¶¶[0064],[0069]-[0070]; *see also id.* at FIG. 8, ¶¶[0020], [0022], [0049], [0059]-[0062], [0072], [0075], [0081], [0101]-[0103], [0106]-[0107], [0109].



FIG. 8

110. Hazelzet explains that the “ECC mode” is a mode that allows the host system to detect and/or correct “correctable errors” or “uncorrectable errors” (*e.g.*, “double bit error”). Ex. 1014 (Hazelzet) at ¶[0069] (“This ECC logic will ... correct all single bit errors and detect all double bit errors present on the twenty-two chip select gated data inputs.”) In the “ECC mode,” the detected correctable errors would be output through an “/Error (CE)” output pin and any uncorrectable errors (*e.g.*, double bit errors) would be reported through an “/Error (UE)” output pin. Ex. 1014 (Hazelzet) at ¶[0069]. Hazelzet explains that these two outputs (*i.e.*, CE and UE) are “open-drain outputs.” Ex. 1014 (Hazelzet) at ¶¶[0072], [0109].

111. Hazelzet further explains that the “parity operating mode” is a mode that allows the host system to “interrogate the device to determine the error

condition” of the memory module. Ex. 1014 (Hazelzet) at ¶[0064] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”).

Hazelzet further explains that such “error condition” in the “parity mode” is also reported to the host “via the Uncorrectable Error (UE) line” when the memory module is in the “parity mode,” Ex. 1014 (Hazelzet) at ¶[0070], which is the open-drain output that is used to report the uncorrectable errors in the “ECC mode.” Ex. 1014 (Hazelzet) at ¶¶[0072], [0109].

112. Hazelzet further explains that its memory module is in the “ECC mode” when the “/ECC Mode” signal becomes “low,” Ex. 1014 (Hazelzet) at ¶[0069], and that the memory module switches to the “parity mode” when the “/ECC Mode” signal becomes “high.” Ex. 1014 (Hazelzet) at ¶[0070].

2. JEDEC LRDIMM Proposal (EX1015)

113. JEDEC discloses a proposed modification to the Memory Buffer (“*module controller*”) functionality of a DDR3 LRDIMM memory module, the standards for which were under development at that time, to add training modes that included training sequences and the ability to output notification signals providing the status of those sequences. I understand that JEDEC is prior art to the 218 Patent. The training modes included, among others, MB-DRAM Training that entailed training sequences Write Leveling Training and Read Enable Training

between the Memory Buffer and the DRAMs of the module. EX1015, 8. JEDEC also states that “[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete....” *Id.*

114. In the same description of MB-DRAM Training, JEDEC states that “training completion can be signaled by the assertion of ERROUT#.” *Id.*, 3, 8. A Skilled Artisan would understand that “ERROUT#” refers to the parity error out pin on a JEDEC standard LRDIMM module of the time. Specifically, a Skilled Artisan would have understood there were other JEDEC documents defining other aspects of DDR3 LRDIMM at that time, such as EX1036, 1, which is a ballot for the “DDR3 LRDIMM Design Specification Body.” Much like Hazelzet’s disclosed memory modules, the DDR3 LRDIMM memory modules at the time of the alleged invention were disclosed to include a PCB with various edge connections for data signals, address and command signals and an ErrOut_n pin that, during normal operation, was used to notify the memory controller of parity errors through the use of an open-drain output, a register/Memory Buffer/”module controller” (that, unlike Hazelzet, buffers address and command signals *and* data signals), and DRAMs. EX1036, 4 (“Product Description”), 8 (penultimate entry in table on page re ErrOut_n). A Skilled Artisan would have understood that the LRDIMM Design Specification’s ErrOut_n and JEDEC’s ERROUT# referred to

the same output/pin on the DDR3 LRDIMMs of the time. *See also* EX1044, 1 (October 2008 TI DDR3 buffer datasheet that discloses ERROROUT# open drain parity error signal).

115. JEDEC therefore discloses a training mode in which the memory module can be made to perform operations related to various training sequences, which does not include any memory read or write operations in response to memory controller commands, and which outputs a notification signal indicating status (*e.g.*, completion) of the training sequences over the same open drain output used to report parity errors in a normal mode of operation.

3. U.S. Patent No. 8,139,430 to Buchmann (Ex. 1016)

116. U.S. Patent No. 8,139,430 to Buchmann et al. (“Buchmann”), the application for which was filed on July 1, 2008, issued on March 20, 2012. I understand that Buchmann is prior art to the 218 Patent. Buchmann is entitled “Power-On Initialization and Test for a Cascade Interconnect Memory System” and discloses, among other things, such functionality. Ex. 1016 (Buchmann) at Title.

117. Buchmann discloses two modes of operation (*i.e.*, “SBC mode” and “high-speed mode”), Ex. 1016 (Buchmann) at Abstract, 1:39-44. The “high-speed mode” is a mode of operation “at a high nominal speed.” Ex. 1016 (Buchmann) at 14:67-15:2. On the other hand, the “SBC mode” is a mode of operation “at a

reduced rate” of communication. Ex. 1016 (Buchmann) at 14:65-67. According to Buchmann, before the high-speed bus between the memory controller and the memory module (*e.g.*, downstream bus 110 and upstream bus 112 in FIG. 1) can be used reliably to communicate with the memory modules, the memory module operates in the SBC mode to train the high-speed bus. Ex. 1016 (Buchmann) at 14:5-8, 3:52-54, 3:64-67; *see also id.* at FIG. 1, 4:11-14.

118. In particular, Buchmann discloses executing training and/or initialization sequences in its “SBC mode,” which is also referred to as an “error correcting code protected quasi-static bit communication” mode. Ex. 1016 (Buchmann) at 14:1-15:15; *see also id.* at 3:52-54, 5:6-22, 4:51-12:59. For example, the training and/or initialization sequences taught by Buchmann include “TS0-clock detection, test and repair; TS1-static configuration and calibration; TS2-downstream lane training and repair; TS3-upstream lane training and repair; TS4 packet training; TS5-initiate valid packets; TS6-frame lock; and TS7-read data latency calculation and inter-channel de-skew,” Ex. 1016 (Buchmann) at 5:40-46, FIG. 3.

119. As an example, training sequence TS0 involves “clock detection and repair,” Ex. 1016 (Buchmann) at 5:51-53, which is a training of the clock signal in the SBC mode. Ex. 1016 (Buchmann) at 5:66-6:22. In particular, the memory buffer MB (*i.e.*, “module controller,” as claimed) enters the TS0 state and initiates

the training sequence TS0 of Buchmann (*i.e.*, an example of a “training sequence” in the “second mode”) after receiving the SBC command “TS0_pdsck” from the host. Ex. 1016 (Buchmann) at 6:1-50 (Table 1 and Table 2, explaining that the “TS0_pdsck” command “causes the downstream receiver logic to enter the TS0 state, reset its memory channel PLLs and select the PDSCK clock as the MB reference clock” and that the “Host/MB drives downstream bus clock on SDSCK lane and issues TS0_pdsck SBC.”). Further, during the TS0 training sequence, the memory module generates and outputs various notification signals providing information about the training sequence to the memory controller of the host system, including the status of the TS0 training sequence (*e.g.*, “TS_done,” which notifies the host that the TS0 training is “done.”). Ex. 1016 (Buchmann) at FIG. 4, 5:51-7:2 & Tables 1-2.

120. As another example, training sequence TS3 involves “upstream lane training” and is “used to perform upstream data lane training,” Ex. 1016 (Buchmann) at 8:24-26, in the SBC mode, Ex. 1016 (Buchmann) at 8:27-47 (showing the SBC commands used during TS3 in Table 5). In particular, the memory buffer MB (*i.e.*, “module controller,” as claimed) initiates the “upstream lane training” TS3 of Buchmann (*i.e.*, another example of a “training sequence” in the “second mode”) after correction/forwarding of the SBC command “TS3_annnc” (*i.e.*, “TS3a announcement SBC”) from the host. Ex. 1016 (Buchmann) at 8:24-27

(“TS3 ... immediately follows TS2 with the host responsible for sending the TS3a announcement SBC.”), Table 5 (“TS3_annnc: This command announces the beginning of TS3a. This SBC is corrected and forwarded by MBs in the memory channel.”). Further, during the “upstream lane training” sequence TS3, the memory module generates and outputs various notification signals providing information about the training schemes to the memory controller of the host system, including the status of the TS3 training sequence, such as “TS3_ack,” which indicates that all downstream MBs have returned the TS3a_ack SBC, and “TS_done,” which notifies the host that the TS3 training sequence is “done.” EX1016, FIG. 6, 8:24-9:18 & Tables 5-6.

121. Buchmann discloses that his training operations may be initiated by power on, reset or initial program load operations, and “may be entered at different states,” which a person of ordinary skill would understand to mean that the his system was configurable to carry out some or all of the disclosed training. EX1016, 3:67-4:5, 4:51-5:12, FIG. 3. Moreover, Buchmann does not disclose the use of memory read and write operations during his TS0 and TS3 sequences during initialization/power-on. Buchmann therefore discloses a training mode (“*first mode*”) in which the memory module can be made to perform operations related to various training sequences and which does not include any memory read and write operations in response to memory controller commands.

122. Buchmann's implementation involves a daisy chain arrangement among the various modules of his system, resulting in signals from the memory module to the host indicating completion of a training sequence reaching the host only after all modules had completed the sequence. *See, e.g.*, Ex. 1016 (Buchmann) at 3:49-52; 14:41-43; 16:47-50; 28:23-26. However, Buchmann also explains that "one or more other bus structure(s) or a combination of bus structures" may be used, including "point-to-point bus(es)," "multi-drop bus(es)," and/or "other shared or parallel bus(es)." *Id.* at 28:26-31.

4. U.S. Patent No. 8,359,521 to Kim (Ex. 1017)

123. United States Patent No. 8,359,521 to Kim et al. ("Kim") was filed on January 22, 2008, the underlying application was published July 23, 2009, and the patent issued January 22, 2013. I understand that Kim is prior art to the 218 Patent. Kim is entitled "Providing a Memory Device Having a Shared Error Feedback Pin" and discloses such functionality. Ex. 1017 (Kim) at Title.

124. Kim discloses a "system and method for providing a memory device having a shared error feedback pin." Ex. 1017 (Kim) at Abstract. Kim discloses that sharing functionality with an error pin is desirable in order maximize use of available bandwidth, simplify the memory controller, Ex. 1017 (Kim) at 4:40-49, "mak[e] use of unused circuits within the subsystem," Ex. 1017 (Kim) at 11:31-34, and enable compatibility with standard memory modules, Ex. 1017 (Kim) at 5:49-

57. Kim teaches that this shared error feedback pin can be used to provide information such as status and error conditions and information related to initialization. Ex. 1017 (Kim) at 12:18-26. Kim further teaches how this shared error pin can be implemented using an open drain configuration and/or an OR-gate. Ex. 1017 (Kim) at 5:49-57; *see also id.* at 4:40-48; 6:1-16; FIG. 4, FIG. 5.

B. Background Technology

1. Shared Pins

125. By the effective filing date of the 218 Patent, a Skilled Artisan would have known that it was common to design the pins within a memory module, such that a single pin is shared for various types of signals for different purposes due to the limited number of pins within the memory module. *See, e.g.*, EX1026 (JESD82-20A) at page 18 (“The data mask signals share pins with the DQS[16:9] pins. ... The following table shows the mapping between DQS pins and data mask pins.”); EX1017 (Kim) at FIG. 5 (showing that the pins related to the open drain transistor (on the right) is shared between the “parity check” circuitry and the “CRC check” circuitry (on the left)).

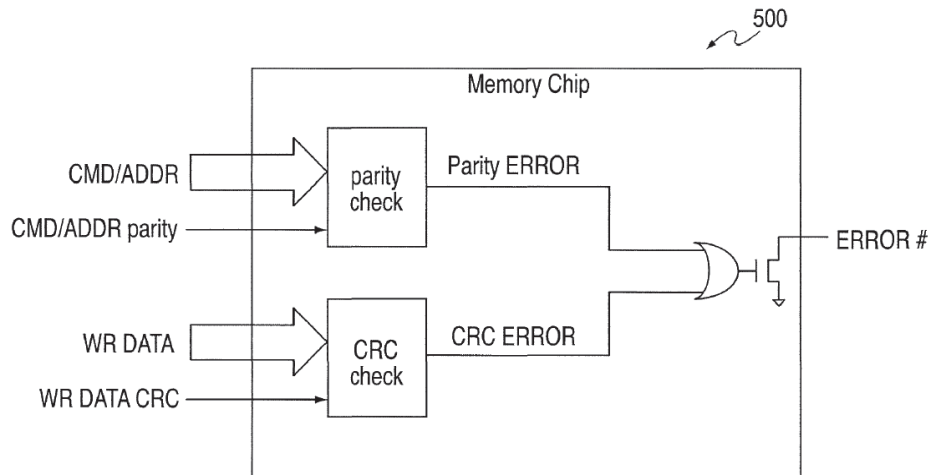


FIG. 5

126. As an example, Kim explains that its “pin... for reporting CRC errors ... could also be merged with an existing error pin available on many industry standard modules for the reporting of address/command errors.” EX1017 (Kim) at 5:49-55; *see also id.*, 6:13-18 (“In alternate exemplary embodiments, other functions also share the error feedback pin (*e.g.*, parity or CRC error(s) on command and address information).”).

127. A Skilled Artisan also knew that it was customary to use a logic OR circuit, as shown in FIG. 5 of Kim, to implement the shared pin. *See, e.g.*, EX1017 (Kim) at FIG. 5 (showing a logic OR circuit coupled to the gate of the open drain transistor), 6:13-16 (“FIG. 5 is a block diagram of a memory device 500 that shares an error feedback pin between data CRC and address parity in accordance with an exemplary embodiment of the present invention.”); *see also* EX1023, US 20080155378 (Amidi) at FIG. 2, FIG. 4, ¶[0018] (“An output device 120

functioning as a logic OR ties the output ends of the error detection module 158 and the transmission memory 156 together such that the error detection module 158 and the transmission memory 156 share the output terminal error-out 168 to transmit signals to the memory controller 110. The output device 120 can be implemented as an OR gate, a wired-OR gate, an open collector, or other device functioning as a logic OR.”); *see also id.*, FIG. 2 (showing that the “error out” signal is output from a “logic OR” element), FIG. 4, claim 17 (“The buffer device of claim 16 wherein the output terminals from the error detection module and the transmission memory are tied using a device functional as a logic OR before being applied to the output terminal for sending the error signal.”).

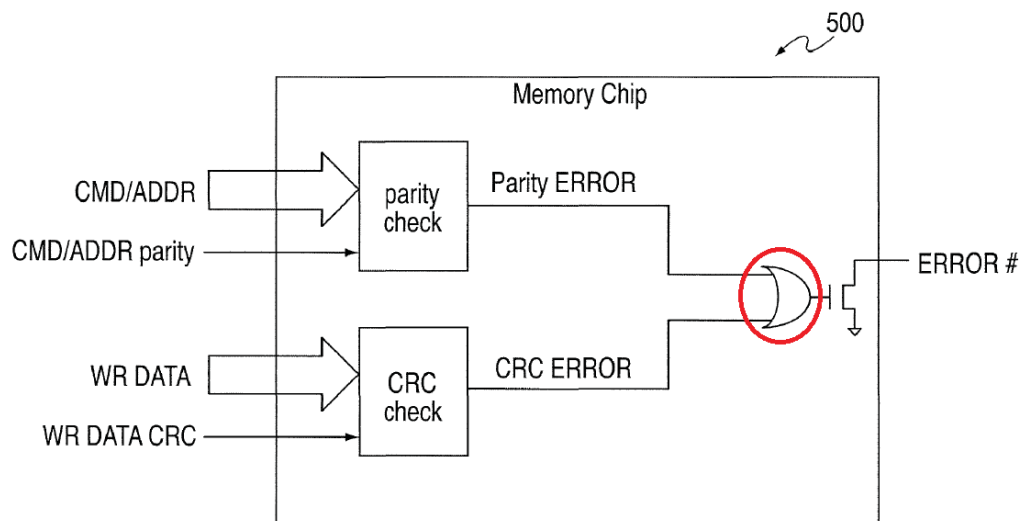


FIG. 5

[FIG. 5 of Kim]

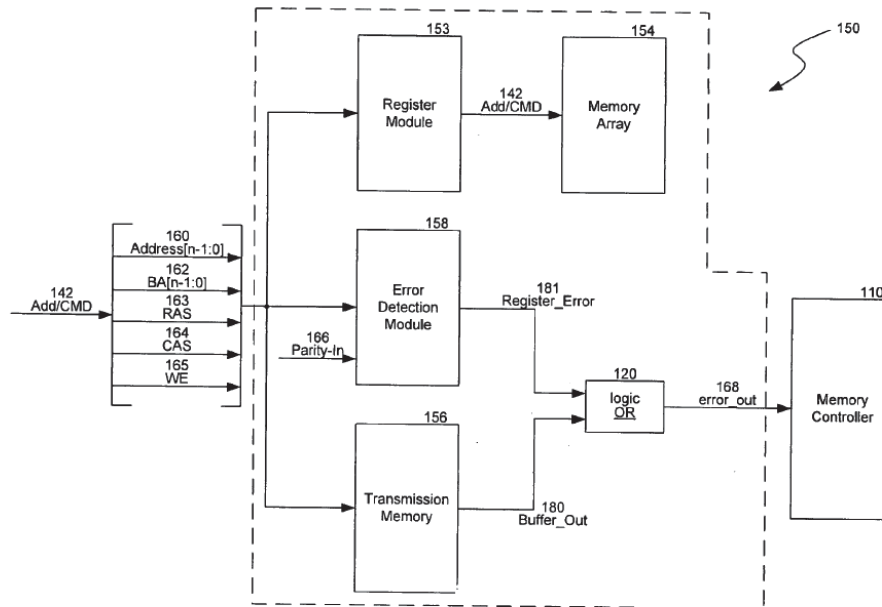


FIG. 2

[FIG. 2 of Amidi]

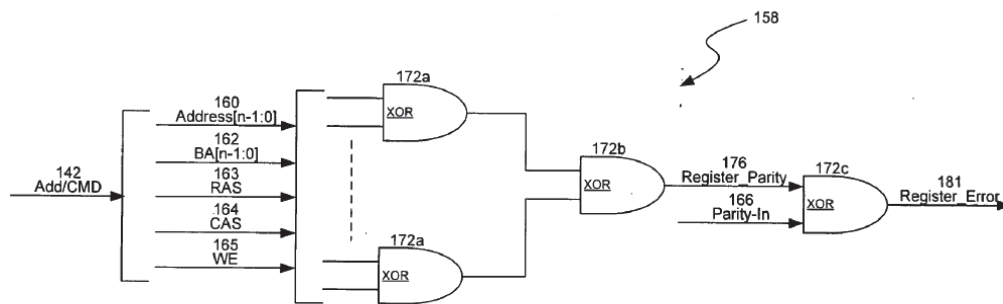


FIG. 4

[FIG. 4 of Amidi]

2. Open-Drain Output

128. By the effective filing date of the 218 Patent, a Skilled Artisan understood that it was common to use an “open drain output” in a memory module to send error signals to the host memory controller. *See, e.g.,* EX1017 (Kim) at

FIG. 4 (reproduced below), 4:40-48; 6:1-16; EX1014 (Hazelzet) at ¶¶[0072], [0109].

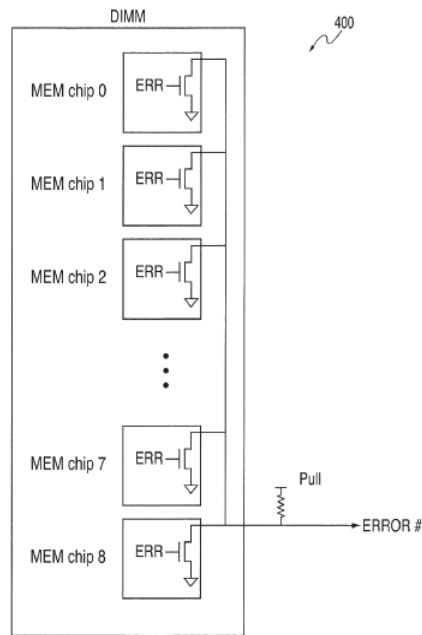


FIG. 4

129. An “open drain output” is an output pin coupled to the drain of a field effect transistor, which includes three ports (*i.e.*, a gate, source, and a drain). See, *e.g.*, EX1017 (Kim) at FIG. 4. As an example, FIG. 4 of Kim shows an open drain output that is coupled to a pull-up resistor (*i.e.*, connected to a high voltage via a pull-up resistor). FIG. 4 of Kim also shows that the source of the transistor is coupled to ground. Because the source of the transistor is coupled to ground (as opposed to Vdd), a positive voltage at the gate (*i.e.*, ERR in FIG. 4 of Kim) would turn on the transistor. Based on this bias condition, a Skilled Artisan would have understood that Kim’s transistor is an NMOS (*i.e.*, n-channel Metal Oxide

Semiconductor) transistor, as opposed to a PMOS (*i.e.*, p-channel Metal Oxide Semiconductor). *See, e.g.*, EX1017 (Kim) at FIG. 4. This is also clear from the symbol. A PMOS transistor would use a symbol with a bubble at the gate. *Id.*

130. A Skilled Artisan would have understood that such open drain outputs (*e.g.*, ERROR# in FIG. 4 of Kim) would be pulled to a high logic level (*i.e.*, the supply voltage connected to the resistor) through the resistor when the gate of the transistor is low, because the transistor would be off. *See, e.g.*, EX1017 (Kim) at FIG. 4. The output would therefore be in an un-driven, high impedance, state. Ex. 1014 (Hazelzet) at ¶[0099]. On the other hand, the open drain output would switch to a low logic level (*e.g.*, ground) when the gate of the transistor is high, because the transistor would be on. *Id.*

C. The Combinations Relied on Here

131. The combinations analyzed here – Hazelzet/JEDEC and Hazelzet/Buchmann – are straightforward. In each, Hazelzet's memory module would be modified to add a training mode ("*first mode*") into which the module could be switched and which includes training sequences and which reports completion of those training sequences by a notification/status signal output over an open drain output (*e.g.*, UE 121) of Hazelzet.

132. In the JEDEC combination, the training sequences would be like those described as MB-DRAM Training in JEDEC (*e.g.*, Write Leveling and Read

Enable Training), EX1015, 8, and the open drain output signal would be similar to the signal output on the ERROUT# pin as described in JEDEC, *id.* at 8; *see also* EX1036, 8 (penultimate entry in table on page re ErrOut_n – is an open drain output for parity errors during normal operation). During those training sequences, the memory controller communicates no data with the module and performs no operations to read or write to the memory devices; the training is carried out by memory buffer (module controller) itself. EX1015, 8.

133. In the Buchmann combination, the training sequences would be like those described as TS0, EX1016 (Buchmann) at FIG. 4, 5:51-7:2 & Tables 1-2, or alternatively, like those described as TS3, EX1016 (Buchmann) at FIG. 6, 8:24-9:18 & Tables 5-6. The open drain output signals would be TS0_done, in the former case, EX1016 (Buchmann) at FIG. 4, 5:51-7:2 & Tables 1-2, and TS3_ack or TS3_done, in the latter case, EX1016 (Buchmann) at FIG. 6, 8:24-9:18 & Tables 5-6. Buchmann does not disclose the memory controller communicating any data with the module or performing operations to read or write to the memory devices during either TS0 or TS3 sequences during initialization/power-on.

134. In either combination, the circuitry of Hazelzet's module, in particular the ECC/Parity register, would be modified to implement the training as part of an additional mode to run, for example, at initialization with Hazelzet's other disclosed initialization operations and to use an open drain output of Hazelzet to

communicate the new notification signals. EX1014 (Hazelzet) at ¶[0123] (initialization operations); EX1015, 3 (training occurs during initialization); EX1016 (Buchmann) at 3:49-60 (same). As explained in more detail below, Hazelzet already uses his UE 121 open drain output for two different signals in two different modes. Thus, this ECC/Parity register necessarily includes circuitry for receiving inputs for each of those signals, and selecting which one to drive on the UE 121 output depending on the mode of the module. It was well within the level of ordinary skill to modify such circuitry such that it accepted three different inputs for three different modes and would select among them depending on the mode, and a Skilled Artisan could have made that modification without undue experimentation and with a reasonable expectation of success.

135. Finally, these combinations would employ known open drain signaling circuitry, which necessarily included a transistor having its source coupled to ground and its drain as the output. That is what a Skilled Artisan would understand the phrase “open drain” to mean. EX1017, FIGs 4&5. A Skilled Artisan would have also known that in order to use open drain signaling to indicate training completion among multiple modules, as here, the open drain output would have to be configured such that the transistor output is driven low (ground) while training is still occurring and driven high upon training completion. This is because, with an open drain configuration shared by multiple modules, any module

can individually drive the output low, but it takes the collective action of all connected modules to drive the output high. Moreover, a Skilled Artisan would also understand that to drive the output low (which would be a low impedance state), the gate of the transistor must be high, causing the transistor to conduct and connect the drain to ground. Conversely, to drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off. This is how an open drain output works. EX1014, ¶¶[0099]; EX1017, FIGs. 4-5, 5:65-6:18.

D. Reasons to Combine

136. All of the prior art relied on in this declaration to combine Hazelzet and JEDEC or Buchmann are analogous art to the 218 Patent because all are in the same field of invention – memory module design, including error detection and correction, initialization, training and the use of pins/paths for multiple purposes during different operations/modes, EX1001(218 Patent) at Abstract, 5:66-6:14;8:4-48 (purported invention is memory module with an operating mode during which parity checking occurs and another mode during which initialization/training occur, and the same errout pin is used to provide notification signals indicating status to the memory controller during both modes, either regarding parity or initialization/training); EX1014(Hazelzet) at Abstract, ¶¶[0007],[0069]-[0070],[0123] (explaining that invention relates to memory modules, with, among

other things, two operating modes – ECC mode and parity mode, in which the two modes share a signal pin for notifying the memory controller of errors – and initialization operations/modes); EX1015, 1, 3, 8 (noting document is JEDEC ballot for “LRDIMM DDR3 Memory Initialization Chapter Proposal”, that includes various training during initialization, including that utilizes the parity ERROUT# pin for multiple purposes including training notifications of status); EX1016, 1:7-9;3:49-60;4:51-5:50;12:60-13:41;14:1-63;20:20-21:19;33:45-67 (explaining that invention relates to memory modules, with, among other things, an SBC mode and a “high-speed” or “functional” mode, wherein the SBC mode combines initialization/training and ECC that runs at power-on initialization and can also be entered from normal (i.e., “high-speed” or “functional”) operation for ECC without full re-initialization/training); EX1022, ¶¶[0004]-[0005],[0032]-[0033],[0052] (explaining that invention relates to memory modules, with, among other things, two modes – “a normal operation mode and a configuration and test mode” (a part of which is called “training mode”) – and, during “training mode,” the “CRC signal path” (normally used for “error detection” and “correct[ion]”) is used to “loop back” “training patterns” sent on the “BCMD signal path” (a command signal) to train the BCMD signal path); EX1025, 15-18 (JEDEC memory module standard for FBDIMM, specifying, in addition to various operating modes, initialization sequences that “must sequence the AMB devices

through the Disable, Calibrate, (back to Disable), *Training*, Testing, and Polling states in order to transition the AMBs into the active channel L0 state” (e.g., operating modes)); EX1027, 1:61-2:19;6:24-25;10:24-45 (discussing importance of training, including for memory modules, and disclosing, in addition to a “standard operating mode,” a “training mode” that occurs before “standard operating mode”); EX1017 (Kim) at 1:16-22;5:49-57;6:8-18;11:20-34;12:36-53(explaining that invention relates to memory modules, with, among other things, two operating modes – ECC mode and parity mode, in which the two modes share a signal pin for notifying the memory controller of errors – and initialization operations/modes that includes “completing a training process to establish reliable communication”, and further teaching that “initialization circuitry” “may reside local to the” memory module and that, by doing so, “added performance may be obtained as related to the specific function, often while making use of unused circuits within the subsystem,” and further teaching that, in addition to sharing ECC and parity on the error out pin, “[i]n alternate exemplary embodiments, other functions also share the error feedback pin”), and each is reasonably pertinent to the problem addressed by that patent – increasing memory module capacity, performance, and/or reliability by sharing an output pin/path to perform multiple functions during multiple operations/modes, including initialization/training, EX1001(218 Patent) at Abstract, 5:66-6:14;8:4-48; EX1014 (Hazelzet) at Abstract, ¶¶[0007],[0069]-

[0070],[0123]; EX1015, 1, 3, 8; EX1016 (Buchmann) at 1:7-9;3:49-60;4:51-5:50;12:60-13:41;14:1-63;20:20-21:19;33:45-67; EX1022 (Talbot) at ¶¶[0004]-[0005],[0032]-[0033],[0052]; EX1025, 15-18; EX1027, 1:61-2:19;6:24-25;10:24-45; EX1017(Kim) at 1:16-22;5:49-57;6:8-18;11:20-34;12:36-53.

137. Also, one skilled in the art would have considered each of the combinations analyzed here to be merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement. Each of Hazelzet, JEDEC, Buchmann and Kim, for example, is a prior art disclosure employing known signaling and training techniques. Many prior art systems had similarly included such techniques. Combining them as described here would therefore have been well within the level of ordinary skill in the art, would not have resulted in any unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success.

138. A Skilled Artisan would have been motivated to make these combinations for at least the following reasons.

1. Motivation to Add Training

139. A Skilled Artisan would have been motivated to add training to the system of Hazelzet. For example, Hazelzet emphasizes the need for “improved overall system reliability.” EX1014 (Hazelzet) at ¶[0003] (“Thus the emphasis and

need for improved overall system reliability is increasing dramatically and requires a comprehensive system solution that includes both a high degree of fault tolerance and overall reliability.”); *see also id.* at ¶[0042] (“The ECC/Parity buffer chips 21 on DIMM 20 include unique error correction code (ECC) circuitry that is coupled to the memory interface chip 18 via line 25 to provide even greater significant reliability enhancement to such servers. The inclusion of this new, improved error correction code (ECC) circuitry results in a significant reduction in interconnect failure.”), ¶[0044] (“The novel ECC/ Parity buffer 21 on DIMM 20 thus provides leading-edge performance and reliability and key operational features different from and unavailable from the prior art while retaining timing requirements generally consistent with devices such as the JEDEC 14 bit 1:2 DDR II register.”), Abstract (“A high density high reliability memory module with power gating and a fault tolerant address and command bus.”), ¶[0001] (“This invention relates generally to a high-density, high-reliability memory module with a fault tolerant address and command bus for use as a main memory that will achieve the degree of fault-tolerance and self-healing necessary for autonomic computing systems.”), ¶[0004] (“The present invention provides such a comprehensive system solution that includes the capability of high memory density and a high degree of fault tolerance and the overall differentiated system reliability long desired in the server market.”), ¶[0007] (“The present invention is directed to a high density high

reliability memory controller/interface module, provided with a high degree of compatibility with industry standard solutions, capable of meeting the desired density, performance and reliability requirements and interfacing with the presently available memory modules, as well as with existing or enhanced support devices. The present invention accomplishes all these ends, resulting in a high density and enhanced reliability memory solution at low cost.”). Given Hazelzet’s emphasis on the need for “improved overall system reliability,” one skilled in the art would have been motivated to add training to Hazelzet because it was known that training improved the reliability of a memory module’s operations. EX1027, 1:35-2:12 (discussing importance of training, including for DIMMs, given advent of DDR memory devices and increasing frequencies, and stating “During a training stage, such a memory controller may write certain data to and read certain data from a memory device, for example a DRAM, and shift the data signal in respect to the clock signal within the time domain, such that the data signal arrives at the memory device with a well-defined synchronization to the clock signal. The memory controller may vary this time shift until a written value corresponds to a read value, which indicates that timing is correct. *In this way, a reliable, fast, and efficient exchange of information is enabled.*”); EX1025, 15-18 (“FBDIMM Architecture and Protocol” standard, specifying initialization sequences that “must sequence the AMB devices through the Disable, Calibrate, (back to Disable),

Training, Testing, and Polling states in order to transition the AMBs into the active channel L0 state” and, for training, noting that, “[b]efore the channel is initialized the bit lanes are not aligned to a frame boundary, thus preventing Channel and DRAM commands from being communicated to the AMBs” such that training is required). This is particularly true given the emerging DDR3 applications in the 2009-10 time-frame and their increased speeds. EX1045, 22-24 (2008 Micron technical note explaining need for training for reads and writes). Indeed, Hazelzet discloses that “[i]nitialization of the memory subsystem” should occur, it just does not address training as part of that initialization or provide any details regarding how to go about that aspect of initialization. EX1014, ¶[0123]; EX1017, 12:36-53.

140. Further, JEDEC includes a portion of the draft standard for DDR3 LRDIMMs being voted upon by JEDEC members that specifically addresses “power-up initialization,” requires various training including “MB-DRAM Training” and explains that, during that training, “[t]he MB performs ‘Write Leveling’ to the DRAMs **to ensure successful writes**, and ‘Read Enable Training’ **to ensure it can capture read data from the DRAMs correctly**, as part of the DRAM interface training,” and further teaches that “MB DRAM interface training must be completed before any MB host interface read or write training **to ensure that the MB DRAM interface is configured optimally for DRAM reads and**

writes.” EX1015, 3,8-9. These statements would have motivated a person of ordinary skill to add training to other systems, such as that of Hazelzet.

141. Also, Buchmann’s “SBC mode” is a mode of operation where “error correcting code” is provided, EX1016 (Buchmann) at 14:25-32, as well as a “training phase that allows more flexibility and improved control data exchange during start-up,” *id.*, 3:64-67, to establish “reliable communication” on the bus, *id.* at 14:28-35 (“Quasi-static bit communication, also referred to as ‘static bit communication’ or ‘SBC’, can be used to control the sequence of link initialization and training phases to establish reliable communication on the high-speed bus. When error correction of an SBC sample is performed prior to checking for a static pattern, the error correction may be able to repair errors that would otherwise prevent the pattern from being static over a period of time.”); *see also id.* at 14:5-8. Thus, one skilled in the art would have been motivated by Hazelzet’s desire to improve reliability to look to systems such as JEDEC’s and Buchman’s that were designed to do just that.

2. Motivation to Add Training As A Mode Separate from Normal Operations

142. One skilled in the art would also have been motivated to combine Hazelzet and JEDEC or Buchmann by adding training in a mode separate from normal operations because she would have known that memory systems are typically and most efficiently initialized/trained before normal operations occur.

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For example, it was well-known that training/initialization of a memory module before normal operation was necessary to minimize errors, by “ensur[ing] successful writes,” and “ensur[ing] [the register on the DIMM] can capture read data from the DRAMs correctly.” EX1015, 8. Indeed, JEDEC’s training is taught to be completed as part of “power-up initialization,” before moving to “Normal Operation.” *Id.* at 3 (listing eight steps, including various training, as part of initialization before listing “Normal Operation” as step 9); *see also* EX1025, 15-18 (“FBDIMM Architecture and Protocol” standard, specifying initialization sequences that “must sequence the AMB devices through the Disable, Calibrate, (back to Disable), *Training*, Testing, and Polling states in order to transition the AMBs into the active channel L0 state” and, for training, noting that, “[b]efore the channel is initialized the bit lanes are not aligned to a frame boundary, thus preventing Channel and DRAM commands from being communicated to the AMBs” such that training sequences are required); EX1022, Fig. 4, ¶¶[0032], [0052],[0088-89]; EX1056, 18, 22, 25-26, 42-44, EX1057, Fig. 5, Abstract, 2:13-34, 2:60-3:3, 9:11-10:44. Likewise, Buchmann’s invention is an “initialization training sequence” completed at “power-on,” EX1016 (Buchmann) at Abstract (explaining that its “memory buffer includes logic for executing a power-on and initialization training sequence initiated by the memory controller.”), which would also suggest to a Skilled Artisan that training before normal operation is important.

143. Because the memory system in Hazelzet would be initialized upon power-on, see, e.g., EX1014 (Hazelzet) at ¶[0123] (“Initialization of the memory subsystem may be completed via one or more methods, based on the available interface busses, the desired initialization speed, available space, cost/complexity objectives, subsystem interconnect structures, the use of alternate processors (such as a service processor) which may be used for this and other purposes, etc.”); see also EX1025, 15-18 (JEDEC memory module standard for FBDIMM, specifying initialization sequences that “must sequence the AMB devices through the Disable, Calibrate, (back to Disable), *Training*, Testing, and Polling states in order to transition the AMBs into the active channel L0 state” (e.g., operating modes)); EX1027, 1:61-2:19; 6:24-25; 10:24-45 (discussing importance of training, including for memory modules, and disclosing, in addition to a “standard operating mode,” a “training mode” that occurs before “standard operating mode”), JEDEC’s and Buchmann’s training (that is disclosed in each to occur at initialization) would have complemented that power-up process as part of Hazelzet’s initialization, and one skilled in the art would have therefore been motivated to combine Hazelzet and JEDEC or Buchmann in a training mode occurring before, and separate from, other, normal operating modes.

3. Motivation to Use Hazelzet’s Open Drain Signaling for

Training Notifications

144. In the obvious combination of Hazelzet and JEDEC or Buchmann analyzed here it would have been further obvious to employ the open-drain parity and ECC signal connections and techniques of Hazelzet to communicate the status of the JEDEC or Buchmann training sequences, any of which satisfies the claimed “notification signal associated with the one or more training sequences,” since they each indicate some status of the related training operation.

145. To be clear, as to JEDEC, it is my opinion that a Skilled Artisan would have found it obvious to communicate that the MB-DRAM training was completed using the open drain output (*e.g.*, UE 121) of Hazelzet, and, as to Buchmann, it is my opinion that a Skilled Artisan would have found it obvious to communicate that the TS_done signal of Buchmann for TS0 training, and also obvious to communicate the TS3_ack and/or TS_done signals of Buchmann for TS3 training, using the open drain output (*e.g.*, UE 121) of Hazelzet, for the reasons set forth below.

146. For example, Hazelzet’s “ECC mode” is a mode where a notification signal indicating an “uncorrectable error” (*i.e.*, “UE”) can be output to the memory controller through the open-drain output line and 121 (*i.e.*, output for uncorrectable error “UE”). EX1014 (Hazelzet) at FIG. 4B, ¶¶[0044],[0049],[0059],[0064],[0069],[0072],[0109]. The open-drain output line 121 (or “/Error (UE)” 121) is the

same open drain output that is used for the parity error signal. EX1014 (Hazelzet) at FIG. 4B, ¶¶[0044],[0049],[0059],[0064],[0070],[0109]. The open-drain output line 121 is coupled to the memory controller of the host system using error edge connection number 142. EX1014 (Hazelzet) at FIG. 7A (indicating “UE” is pin 142). As such, Hazelzet’s implementation involves using the same open drain output (“/Error (UE)” 121), in two different modes, to output both a parity error notification signal and an ECC notification signal, depending on which mode the memory module is in. EX1014 (Hazelzet) at FIG. 4B, ¶¶[0044],[0049],[0059],[0064],[0069-70],[0072],[0109]. Hazelzet’s use of the same output in two different modes would have suggested to, and motivated a person of ordinary skill in the art to use that same output in the added training mode, particularly when the training mode was implemented separate from, and before, the parity and ECC modes of Hazelzet, as here. In such a system, those modes, which include normal memory operations, would therefore not be using the open drain outputs while the training mode was running during initialization.

147. Similarly, JEDEC employs this same technique, using the same open drain output to communicate parity error and training completion in different modes. Thus, a Skilled Artisan would have viewed JEDEC’s technique as a natural fit in the system of Hazelzet, and JEDEC’s disclosure would have motivated the use of that technique in other systems, such as with Buchmann.

148. Further, a person of ordinary skill in the art would have been motivated to use the same output to notify error signals and training status because such multiple use of a pin was known, and would have been considered an efficient use of the limited number of output pins on integrated circuits. For instance, Kim, EX1017, is a patent assigned to IBM that shares with Hazelzet a substantial overlap in their disclosures, particularly in the disclosures of open-drain shared outputs and in the latter halves of their specifications. Kim was filed approximately a year and a half after Hazelzet and discloses additional details regarding the use of an open-drain output on a memory module to notify the memory controller of errors during a parity normal operating mode and during an ECC normal operating mode. EX1017 (Kim) at 1:16-22; 5:49-57; 6:8-16. Kim further teaches initialization operations (initialization/training modes) that include “completing a training process to establish reliable communication,” *id.* at 12:36-53, teaches that “initialization circuitry” “may reside local to the” memory module and that, by doing so, “added performance may be obtained as related to the specific function, often while making use of unused circuits within the subsystem,” *id.* at 11:20-34, and further teaching that, in addition to sharing ECC and parity on the error out pin, “[i]n alternate exemplary embodiments, other functions also share the error feedback pin,” *id.* at 6:16-18. Such disclosures would have motivated a Skilled Artisan to use Hazelzet’s “/Error (UE)” 121 open-drain output

(corresponding to Kim's "error feedback pin") to notify the memory controller that the training was in progress or done.

149. As another example, Talbot discloses memory modules, with, among other things, two modes – "a normal operation mode and a configuration and test mode" (a part of which is called "training mode"). EX1022 (Talbot) at ¶¶[0004]-[0005],[0032]-[0033],[0052]. Talbot further discloses that, during the "training mode," the "CRC signal path" (normally used for "error detection" and "correct[ion]", *id.* at [0033]) is used to "loop[] back" "training patterns" sent on the "BCMD signal path" (a command signal) to train the BCMD signal path, *id.* at [0052]. Thus, Talbot discloses using a CRC (i.e. ECC) signal path to return signals relating to training during the training mode when the CRC functionality is off. *Id.* at [0033],[0052]. Such disclosures would have motivated a Skilled Artisan to use Hazelzet's "/Error (UE)" 121 open-drain output (corresponding to Talbot's "CRC signal path") to notify the memory controller that the training was in progress or done.

150. Moreover, a Skilled Artisan would have been motivated to arrange the modified Hazelzet to communicate a signal indicating completion of training only when all memory modules have completed that training, in order to ensure that the entire memory system had been trained before proceeding to normal operation. This would permit training to be completed in an orderly and systematic manner,

thereby limiting the complexity of the control circuitry needed to implement the training. EX1043, 7:30-51. Use of an open drain signal in this manner was a known, efficient way to communicate information about multiple circuits because it effectively OR'd the inputs into a single output. EX1017 (Kim) at FIG. 4; 5:65-6:12 (illustrating and describing just such a system); *see also* EX1014 (Hazelzet) at [0018] (“After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules.”), [0109] (“The error reporting circuitry, of the present invention is included to permit external monitoring of device operation. Two open-drain outputs are available to permit multiple modules to share a common signal pin for reporting an error that occurred during a valid command (any /CS low) cycle (consistent with the re-driven signals).”).

151. In addition, a Skilled Artisan would have been further motivated to modify Hazelzet as described above, because Hazelzet's memory system includes multiple memory modules in need of training. In other words, there would be a motivation to delay transitioning to a normal mode of operations until all memory modules had signaled the completion of training. EX1014 (Hazelzet) at [0018] (“After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance)

thus allowing this line to be shared by multiple modules.”), [0109] (“The error reporting circuitry, of the present invention is included to permit external monitoring of device operation. Two open-drain outputs are available to permit multiple modules to share a common signal pin for reporting an error that occurred during a valid command (any /CS low) cycle (consistent with the re-driven signals).”); *see also* EX1017 (Kim) at FIG. 4; 5:65-6:12; EX1043, 7:30-51. In particular, a Skilled Artisan would have been motivated to use Hazelzet’s open-drain output to notify the host of training status because that technique allows any module in the system to pull the open drain pin to “low” (i.e. to ground) if it is still executing its training sequence, regardless of whether other modules in the system have completed training and are no longer pulling that pin low. *Id.* As I demonstrate above, an open drain was a known way to signal when multiple circuits were, or were not all, finished performing some operation. *See* ¶¶125-130.

V. COMPARISON OF THE PRIOR ART TO THE CLAIMS OF THE 218 PATENT

152. My analysis is based on my understanding of the law as set forth above and the ordinary and accustomed meaning of the claim terms as understood by one of ordinary skill in the art in view of the 218 Patent and its file history, including the constructions I presented for three of the claim terms. *See* ¶¶ 94-107.

A. Claims 1-22 Are Unpatentable Over Hazelzet and JEDEC

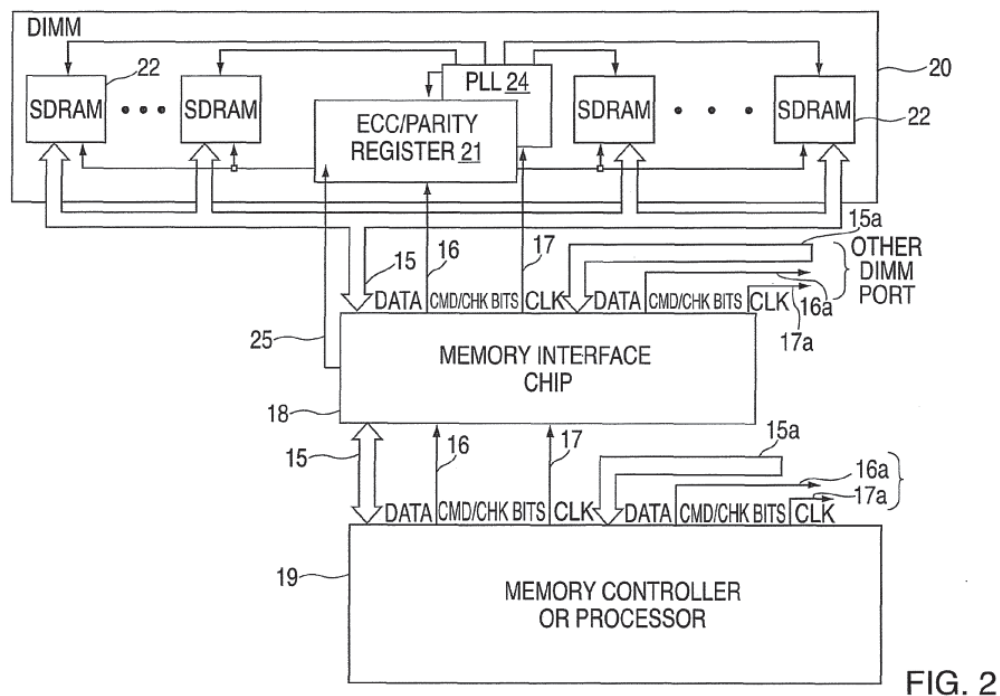
or **Buchmann**, with or without **Kim** for Certain Claims

1. **Claim 1 is Unpatentable**

a) *[1.a] Preamble*

153. The preamble of claim 1 requires “[a] memory module operable with a memory controller of a host system, comprising.”

154. Hazelzet discloses dual inline memory modules 20 (i.e., “DIMMs”) that are configured to operate with the “memory controller” 19 of the host system. Ex. 1014 (Hazelzet) at FIGs. 2, 3A-3D, ¶¶[0037], [0038], [0039]; see also Ex. 1014 (Hazelzet) at ¶[0036] (referring to DIMMs as “dual inline memory modules”).



155. Accordingly, Hazelzet satisfies “[a] memory module operable with a memory controller of a host system.”

b) [1.b] Printed Circuit Board Having Edge Connections

156. Claim 1 requires “a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections.”

157. Hazelzet explains that the “DIMM of the present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface,” EX1014, ¶[0015], examples of which are shown in FIGS. 2, 3A, 3B, 3C, and 3D. See EX1014, FIGS. 2, 3A-3D; see also *id.* at ¶[0037] (“Turning now to FIGS. 2, 3A, 3B, 3C, 3D, 4A, 4B, 5, 8, 9, 10 and 11, the enhanced server memory arrangement of the present invention will be described.”), ¶[0039], Abstract (“The memory module includes a rectangular printed circuit board having a first side and a second side, a length of between 149 and 153 millimeters and first and second ends having a width smaller than said length.”).

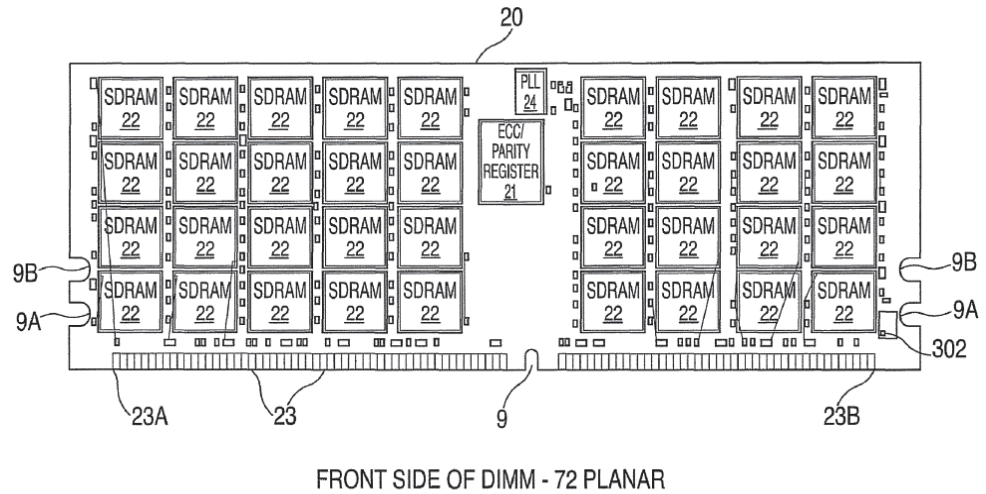


FIG. 3A

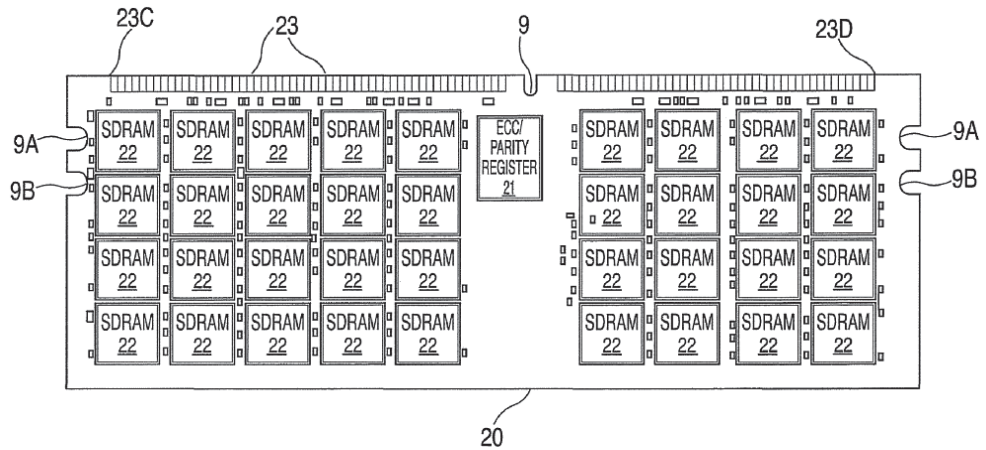


FIG. 3B

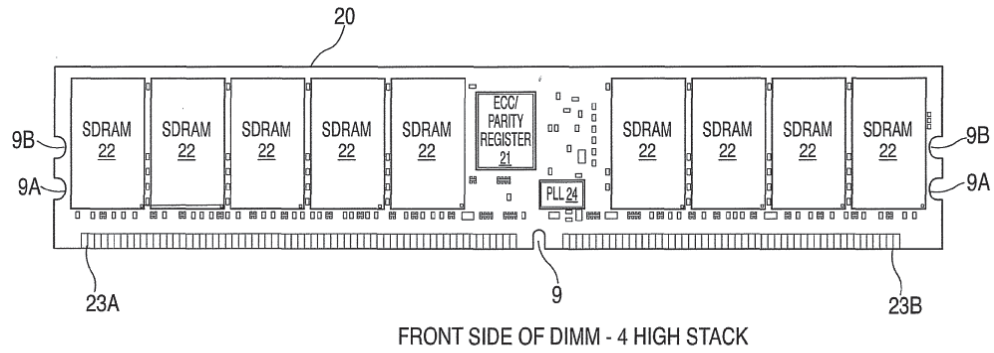


FIG. 3C

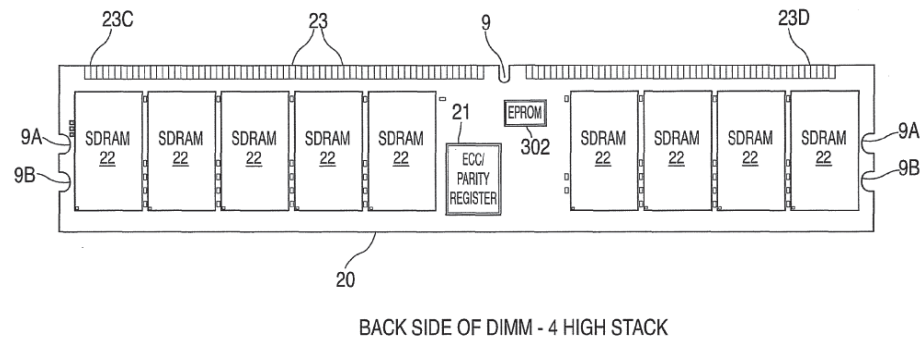
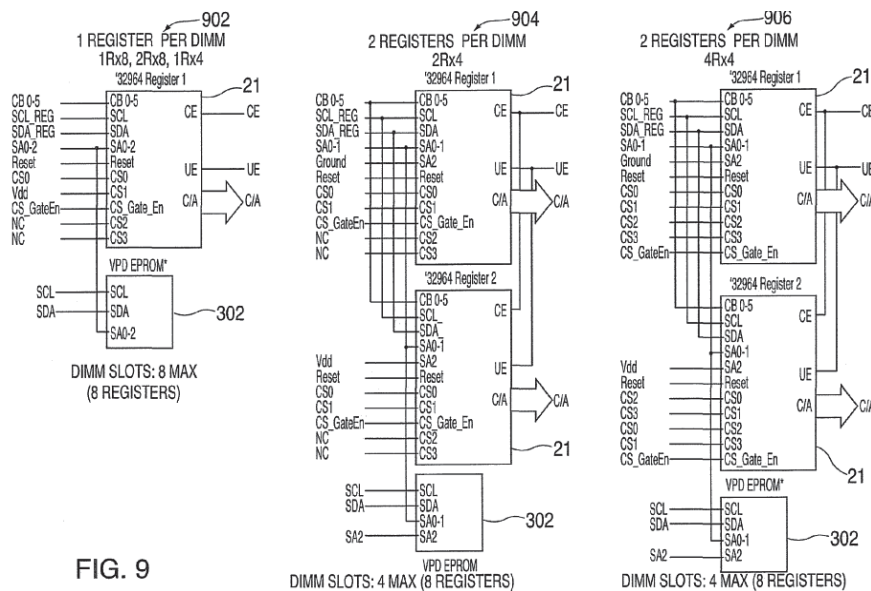


FIG. 3D

158. Hazelzet further explains that its memory modules include “connectors 23 along the edge of both the back and front sides” of the printed circuit board, Ex. 1014 (Hazelzet) at ¶[0039] (“Generally speaking DIMMs are printed circuit cards designed to carry a plurality of DRAMs 22 thereon and the DRAM output pins (not shown) are connected via the printed circuit to selected connectors 23 along the edge of both the back and front sides of the card and are often provided with a single indexing key or notch 9 on the connector edge.”), which are provided to form connections to the memory controller of the host system when the memory module is inserted into a corresponding “slot” of the host

system. Ex. 1014 (Hazelzet) at ¶[0097] (“Referring to FIG. 11, column 1102 is the slot in the memory system being occupied by the memory module. ... For memory modules having one buffer chip 21, the IIC address correlates to the slot being occupied by the memory module as shown in column 1106”); *see also id.* at ¶[0032], FIG. 11, FIG. 9 (showing the maximum number of “DIMM slots” for “1, 2, and 4 rank DIMMs.”).



159. Hazelzet therefore discloses “a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller.”

160. Hazelzet further discloses that the printed circuit board has a first set of edge connections for communicating data signals between the memory module and the memory controller of the host system, Ex. 1014 (Hazelzet) at FIGs 7A-7C

(showing data edge connections including pins 11, 12, 17, 18, 22, 23, 31, 32, 37, 38), while the memory module is in either the “parity mode” or the “ECC mode,” *id.* at FIG. 8 (showing “Data In” and “Data Out” in both the “parity mode” and the “ECC mode.”) , ¶¶[0015],[0035], [0038],[0041].

161. Hazelzet further discloses that the printed circuit board has a second set of edge connections for communicating address and control signals from the memory controller of the host system. Ex. 1014 (Hazelzet) at FIGs 7A-7C (showing address edge connections including pins 67, 70, 72-75, 82, 205-207, 210-213, 220, 277 and command edge connections including pins 86, 89, 91, 93), ¶[0072] (referring to “/CS” as commands), ¶[0068] (listing various control signals including “chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE)” signals); *see also* Ex. 1014 (Hazelzet) at ¶[0038] (“The memory interface chip 18 then sends and receives data, via line 15, to the memory devices or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16 and check bits for error correction purposes to the ECC/ Parity register chip 21 via line 25.”), FIG. 2 (showing address and command line 16), ¶¶[0015],[0035],[0041].

162. Hazelzet further explains that the printed circuit board has an error edge connection coupled to the open drain output of the module controller. Ex. 1014 (Hazelzet) at FIGs 7A (showing an uncorrectable error pin UE (142) of the

memory module that is coupled to the open drain output “/Error (UE)” 121); *see also id.* at FIG. 4B, ¶¶[0072], [0109].

163. Accordingly, Hazelzet discloses “*the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections.*”

c) [1.c] Dynamic Random Access Memory Elements

164. Claim 1 requires “*dynamic random access memory elements on the printed circuit board.*”

165. Hazelzet explains that its memory module (DIMM) includes a plurality of “synchronous dynamic random access memories (SDRAMs)” / “DRAMs” on the “printed circuit board,” Ex. 1014 (Hazelzet) at ¶[0015] (“The DIMM of the present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface.”), examples of which are shown in FIGS. 2, 3A, 3B, 3C, and 3D. *See* Ex. 1014 (Hazelzet) at FIGs. 2, 3A-3D; *see also id.* at ¶[0037], ¶[0039].

166. Accordingly, Hazelzet discloses “*dynamic random access memory elements on the printed circuit board.*”

d) [1.d] Module Controller ... Having An Open Drain

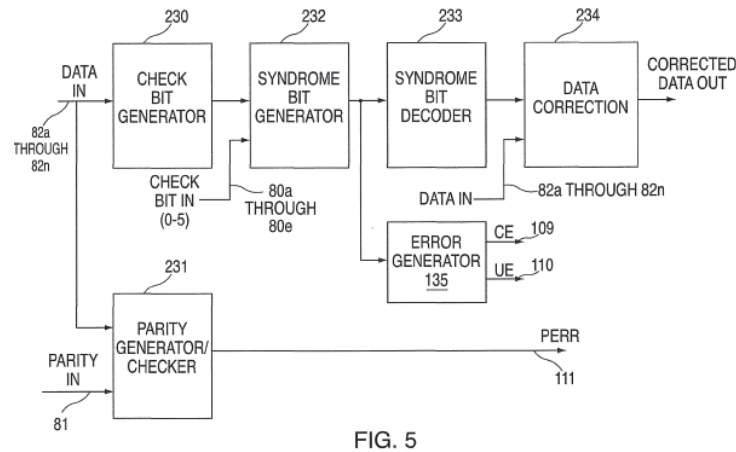
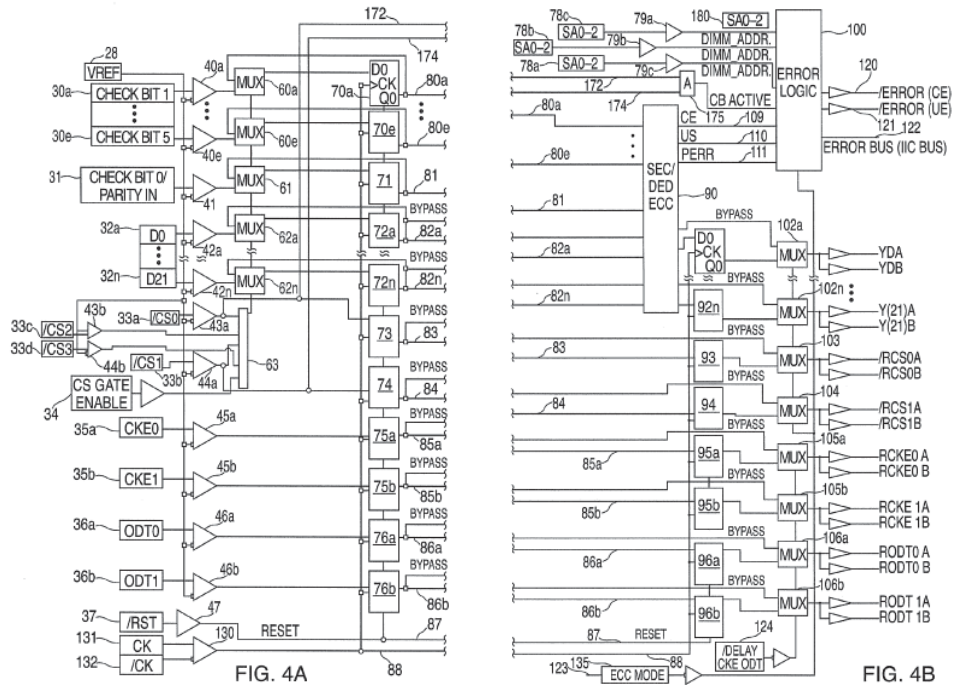
Output

167. Claim 1 requires “*a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection*”

168. Hazelzet discloses an “ECC/Parity register,” which is the claimed “*module controller*,” having an output for uncorrectable errors (shown in FIG. 4B as “/ERROR (UE) 121”), which is the claimed “*open drain output*.” Ex. 1014 (Hazelzet) at FIGS. 3A-3D, 4A, 4B, 5, ¶¶[0044], [0059], [0072]. As shown in FIGs. 3A, 3B, 3C, and 3D, the “ECC/Parity register” is on the “printed circuit board” and coupled to the “synchronous dynamic random access memories (SDRAMs).” Ex. 1014 (Hazelzet) at FIGs. 3A-3D, ¶[0015] (“The DIMM of the present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface.”), ¶[0039] (“Further, as shown in FIG. 3A on the front of each DIMM 20, in addition to the DRAMs, there is positioned a phase locked loop (PLL) chip 24 and the novel ECC/Parity Buffer chip 21 of the present invention.”), ¶[0042].

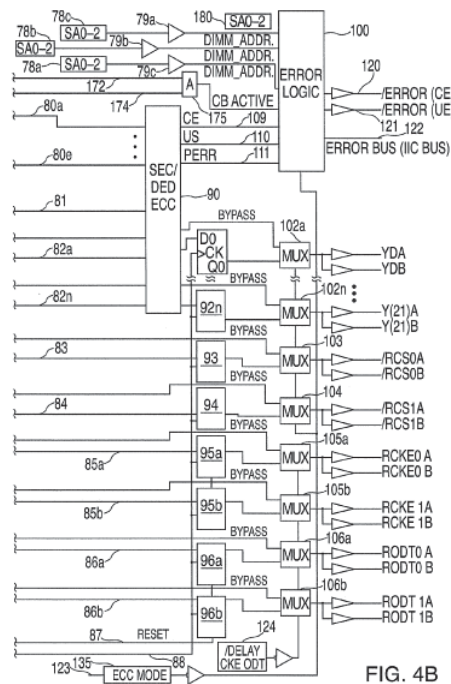
169. FIGS. 4A and 4B of Hazelzet show the “ECC/Parity register” of FIGS. 3A-3D in greater detail, and FIG. 5 of Hazelzet shows the “single error

correction / double error detection error correction code (SEC/DED ECC) circuit
of FIG. 4B.” Ex. 1014 (Hazelzet) at ¶¶[0027], [0028].



170. As shown in FIG. 4B, the “SEC/DED ECC” circuit is coupled to an
“ERROR LOGIC” 100, both of which being part of the “ECC/Parity register” (*i.e.*,

“*module controller*,” as claimed). The “ERROR LOGIC” of the “ECC/Parity register” (*i.e.*, “*module controller*,” as claimed) is coupled to an “error reporting circuitry” with two “open drain outputs,” one for correctable errors “CE” (120 of FIG. 4B) and another for uncorrectable errors “UE” (121 of FIG. 4B). Ex. 1014 (Hazelzet) at FIG. 4B, ¶[0072] (“Error reporting circuitry is included to permit external monitoring of DIMM operation. Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of /Error (UE) is different in parity mode vs. ECC mode.”). The output for uncorrectable errors (shown in FIG. 4B as “/ERROR (UE) 121”) is the “*open drain output*,” as claimed.



171. As explained in claim element [1.b.], the error edge connection is coupled to the open drain output of the module controller. Ex. 1014 (Hazelzet) at FIGs 7A (showing an uncorrectable error pin UE (142) of the memory module that is coupled to the open drain output “/Error (UE)” 121); *see also id.* at FIG. 4B, ¶¶[0059],[0072].

172. Accordingly, Hazelzet discloses “a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection.”

e) [1.e] First Wherein Clause

173. Claim 1 requires “*wherein the memory module is operable in at least a first mode and a second mode, wherein the memory module in the first mode is configured to be trained with one or more training sequences.*”

(1) [1.e.1] Two Modes

174. Hazelzet explains that its memory modules are configurable to operate in (1) a “parity mode,” which is the claimed “*second mode*,” and (2) an “ECC mode.” Ex. 1014 (Hazelzet) at FIG. 8; *see also id.* at ¶¶[0020], [0022], [0049], [0059]-[0062], [0064], [0069]-[0070], [0072], [0075]. Hazelzet uses the term “mode” in accordance with the plain and ordinary meaning, Ex. 1014 at FIG. 8, ¶¶[0044], [0049], [0059]-[0065], [0069]-[0072], [0075], and therefore its “parity mode” satisfies the plain and ordinary meaning of the claim term “*mode*.” The combination of Hazelzet and Buchmann or, alternatively, Hazelzet and JEDEC, would add a “*first mode*” as claimed to the module. The combined module would therefore be configurable to operate in either mode, as it would enter either mode when instructed to do so by the appropriate control inputs. *See* ¶¶131-135.

(2) [1.e.ii] Training Sequences

175. As explained above, *see* ¶¶131-135, the combinations analyzed here includes a separate training mode into which the module can be placed and in which the module can implement various training sequences (*e.g.*, Write Leveling

and Read Enable Training per JEDEC/TS0 and TS3 per Buchmann) (“*configured to be trained with one or more training sequences*”). Each of those operations includes a set of operations occurring in a particular order, used for training a memory module. For instance, a Skilled Artisan would understand “‘Write Leveling’ to the DRAMs to ensure successful writes, and ‘Read Enable Training’ to ensure it can capture read data from the DRAMs correctly,” as each including a set of operations occurring in a particular order to train the memory module. EX1015 at 8; EX1040, 14:1-15:3; EX1018, Fig. 4. For example, a Skilled Artisan would understand operations described on page 8 of EX1039 to be operations performed in a particular order during MB-DRAM Training’s “‘Write Leveling,’” and the operations described on page 9 of EX1039 to be operations performed in a particular order during MB-DRAM Training’s “‘Read Enable Training.’” Likewise, a Skilled Artisan would understand the various operations set forth in Buchmann as performed during the TS0 and TS3 operations as each including a set of operations occurring in a particular order to train the memory module. EX1016, FIGs. 4,6, 5:51-7:2,8:24-9:18. See for example the operations described in Table 1 of Buchmann, for TS0, and in Table 5 of Buchmann, for TS3. The combinations therefore satisfy this claim element.

f) [1.f] Second Wherein Clause

176. Claim 1 requires “*wherein the memory module in the second mode is configured to perform one or more memory read or write operations not associated with the one or more training sequences by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections.*”

177. Hazelzet discloses that “as shown in this FIG. 2, the memory interface chip 18 sends and receives data from the DIMMs via the data line 15 and sends address and commands via line 16.” EX1014, ¶[0038]; FIG. 2. The figure shows line 15 coupling the memory controller and the DRAMs, and line 16 coupling the memory controller and the register 21. *Id.* A Skilled Artisan would also understand from Figure 2 that lines 15 and 16 are coupled to edge connectors for data and address/control, respectively, since those lines coupled the DIMM to the memory controller. EX1014, FIGs. 2, 7A-7B, ¶¶[0015], [0035], [0038], [0041]. Hazelzet therefore discloses that the module is configurable to receive address and control signal via the edge connections included on the module for that purpose.

178. A Skilled Artisan would understand that such operations – communicating data with DRAMs while communicating address and command information with the register – to constitute “*memory read or write operations*” because they follow the standard configuration for such operations with a JEDEC

compliant device, EX1014, ¶[0044], including sending address and control to the register and data to the DRAMs. EX1024, 1, 14, 16.

179. Hazelzet additionally explains that its “parity mode” is an “operating mode” with “no correction of errors.” Ex. 1014 (Hazelzet) at ¶[0064] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”), ¶[0103] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”); *see also id.* at ¶[0020] (“Still further the present invention permits operation of the memory module in parity mode, such that unused ECC check bit inputs are held at a low level thus ensuring that these inputs are at a known and quiescent state.”); ¶[0072] (“Error reporting circuitry is included to permit external monitoring of DIMM operation.”); ¶[0070] (“In addition to the above ECC mode, the same twenty two chip select gated data signals can be operated in []parity mode (/ECC Mode high), whereby the signal received on CHK0/Parity in line is received as parity to the register one clock pulse later than the chip select gated data inputs. The received parity bit is then compared to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. ... No correction of errors will be completed in this mode.”). A Skilled Artisan would understand the phrase

“operating mode” to refer to a mode in which the memory operations are employed to store data in or read data from the DRAMs of the module.

180. Hazelzet states that “[i]n Parity Mode, the memory interface chip or controller would generate a single parity bit **in conjunction with providing the full address and command field to the module.** The module would re-drive the address and command bits, to the DRAMs, in the next cycle-rather than adding the additional cycle required in ECC mode. Any error on the address and command bus would be reported to the system at a later time, and the potential for recovery from the fail would be small hence this option is undesirable for many applications. The last mode would be to simply operate the memory in a mode with no parity bits and no ECC bits, with neither the added delay due to ECC nor any means to detect a fault on the address/command bus as per the prior art convention now used for these modules.” Ex. 1014 (Hazelzet) at ¶[0075]. (emphasis added). A Skilled Artisan would understand “the full address and command field” in this context to refer to the signals sent to a memory module during a read or write operation. *See, e.g.*, Ex. 1024, JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) (“JESD79”) at page 14 (“The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai (where i = 7 for x16, 8 for x8 or 9 for x4) selects the starting column

location. ... The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai (where i = 7 for x16, 8 for x8 or 9 for x4) selects the starting column location.”), *see also* page 16. Such operations include the reception at the module of address and control signals via their respective edge connections, and in response the communication of data signals between the system memory controller and the module DRAMs, which a Skilled Artisan would understand to occur over the data edge connections of the module, with the DRAM being controlled by the module controller. EX1014, ¶[0038]; EX1024, 1.

181. Moreover, I note that Figure 8 of Hazelzet depicts a timing diagram used with his invention and explicitly discloses “Data In” and “Data Out” in parity mode. A Skilled Artisan would understand such movement of data to occur in the context of read and write operations. Ex. 1014 (Hazelzet) at FIG. 8.

182. Hazelzet therefore discloses that the address and control signals received by the module over the address/control edge connections are associated with “*memory read or write operations.*”

183. Moreover, Hazelzet relates this configuration to both his ECC and parity mode, EX1014, ¶[0038], so a Skilled Artisan would understand these operations occur in parity mode (*i.e.*, “*second mode,*” as claimed).

184. Accordingly, one skilled in the art would have understood Hazelzet's parity mode to be a normal operating mode in which the module can be made, via the appropriate signaling, to perform "*one or more memory read or write operations*," which include the communication of data with the memory controller (over edge connections provided for that purpose) and in response to address and control signals (received over edge connections provided for that purpose).

185. Further, FIG. 2 of Hazelzet discloses that address and command bits are driven to the DRAMs from the memory interface chip through the "ECC/Parity register" (*i.e.*, "*module controller*," as claimed) using the address and command line (*i.e.*, "add/cmd line 16") regardless of which mode the memory module is in (*i.e.*, including the "parity mode"). Ex. 1014 (Hazelzet) at ¶[0038], FIG. 2, FIGs 7A-7C (showing address edge connections including pins 67, 70, 72-75, 82, 205-207, 210-213, 220, 277 and command edge connections including pins 86, 89, 91, 93), ¶[0072] (referring to "/CS" as commands), ¶[0068] (listing various control signals including "chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE)" signals); Ex. 1024 (JESD79) at page 13 (TRUTH TABLE 1a).

186. Accordingly, Hazelzet discloses "*wherein the memory module in the second mode is configured to perform one or more memory read or write operations...by communicating data signals via the first edge connections in*

response to address and command signals received via the second edge connections.”

187. To the extent one might argue that Hazelzet does not sufficiently disclose this wherein clause, it would have been obvious to include those claim requirements in the system of Hazelzet. In fact, Hazelzet describes how its “parity mode” is an “operating mode” with “no correction of errors.” Ex. 1014 (Hazelzet) at ¶[0064], [0070]. In addition, Hazelzet states that “[i]n Parity Mode, the memory interface chip or controller would generate a single parity bit in conjunction with providing the full address and command field to the module.” Ex. 1014 (Hazelzet) at ¶[0075]. Read and write operations were known in the prior art. EX1024, 14, 16. Based on these disclosures, a Skilled Artisan would have at least found it obvious to modify Hazelzet’s “parity mode” into the claimed “*second mode*” involving a read or write operation over the claimed edge connections because to do so would have permitted memory operations, the ultimate purpose of any memory module, using the existing and therefore convenient connections disclosed in Hazelzet and because it would have been common sense to do so. See, e.g., Ex. 1024 (JESD79) at page 14, page 16. This is confirmed by the passage’s reference to a third mode without ECC or parity where the register would simply be “operat[ing] the memory,” which a Skilled Artisan would also understand to refer to the usual memory operations such as reading and writing. Ex. 1014 (Hazelzet)

at ¶¶[0075]; *see also id.* at FIG. 8 (depicting a timing diagram used with his invention and explicitly discloses “Data In” and “Data Out” in parity mode).

188. Accordingly, the “*wherein the memory module in the second mode is configured to perform one or more memory read or write operations...by communicating data signals via the first edge connections in response to address and command signals received via the second edge connections*” limitation would have been obvious in view of Hazelzet.

189. As for the “ECC mode,” while the memory module is in the “ECC mode,” the “ECC/Parity register” (i.e., “*module controller*,” as claimed) generates a notification signal that is “low, for two clocks,” and outputs the notification signal to the memory controller of the host system through the “/Error (UE)” 121 pin if/when an uncorrectable error is detected. Ex. 1014 (Hazelzet) at ¶[0059] (“When either [correctable] error line (CE) 109 or uncorrectable error line (UE) 110 is low this indicates that an error was identified as being associated with the address and/or command inputs (either correctable or uncorrectable). The error lines 120,121 will be active, i.e., low, for two clock cycles simultaneous with the re-driven address/command data when operating in ECC mode or delayed by two clock cycles when operating in parity mode.”), ¶[0072] (“Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle

(consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of /Error (UE) is different in parity mode vs. ECC mode.”), FIG. 2, FIG. 4B, FIG. 7A (showing that the UE pin of the memory module is coupled to the memory controller of the host system using pin number 142).

190. Hazelzet’s notification signal from the “ECC/Parity register” (*i.e.*, “buffer chip”) indicates the status of the error correction sequence when the memory module is in the “ECC mode,” by indicating (1) whether “an error was identified” and (2) whether the error from the memory module is an “uncorrectable error.” Ex. 1014 (Hazelzet) at ¶¶[0059] (“When either [correctable] error line (CE) 109 or uncorrectable error line (UE) 110 is low this indicates that an error was identified as being associated with the address and/or command inputs (either correctable or uncorrectable). The error lines 120,121 will be active, *i.e.*, low, for two clock cycles simultaneous with the re-driven address/command data when operating in ECC mode or delayed by two clock cycles when operating in parity mode.”), [0069], [0072], FIG. 2, FIG. 4B, FIG. 7A; *see also id.*, at ¶¶[0092] (“As shown in configuration 902, outputs from the buffer chip 21 include an indication

of whether the error is a correctable error (CE) or an uncorrectable error (UE) as well as the corrected (if error is correctable) command and address information, which connect to memory devices 22.”).

191. This claim element also requires “*wherein the memory module in the second mode is configured to perform one or more memory read or write operations not associated with the one or more training sequences.*” As noted above, the combinations analyzed here include JEDEC or Buchmann training sequences in a training mode wholly separate from any mode that includes memory operations in response to memory controller commands and it would have been obvious to make the combinations in that manner. See ¶¶131-135. Moreover, I note that neither Hazelzet, JEDEC, nor Buchmann disclose memory read or write operations in response to memory controller commands occurring in a training mode of the proposed combinations. The combinations therefore satisfy this claim language.

*g) [1.g] Third Wherein Clause: Operation Of Module
Controller In the Second Mode*

192. Claim 1 requires “*wherein the module controller is configured to receive via the second edge connections the address and command signals associated with the one or more memory read or write operations and to control the dynamic random access memory elements in accordance with the address and command signals, and wherein the module controller is further configured to*

output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the second mode.”

(1) [1.g.i] Receiving for Read/Write

193. As explained in claim elements [1.b] and [1.e.i], Hazelzet’s module can be placed into a parity mode, which is a normal operating mode in which the module is provided, over the edge connections identified for that purpose, address and control signals for performing “one or more memory read or write operations.” EX1014 (Hazelzet) at FIGs. 2, 7A-7B, ¶¶[0015],[0035],[0038],[0041],[0064], [0070]; see also EX1024 (JESD79) at page 14, page 16. For example, Hazelzet discloses providing “the full address and command field to the module” during parity mode, which a Skilled Artisan would understand to refer to the normal signaling that implements a memory read or write from a memory controller. EX1014, ¶[0075]. In addition, as further explained in claim element [1.f.], FIG. 2 of Hazelzet discloses that address and command bits are driven to the DRAMs from the memory interface chip through the “ECC/Parity register” (i.e., “module controller,” as claimed) using the address and command line (i.e., “add/cmd line 16”) in the “parity mode.” EX1014 (Hazelzet) at ¶[0038] (“The memory interface chip 18 then sends and receives data, via line 15, to the memory devices or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16 and check bits for error correction purposes to

the ECC/ Parity register chip 21 via line 25.”), FIG. 2; *see also id.* at FIGs 7A-7C (showing address edge connections including pins 67, 70, 72-75, 82, 205-207, 210-213, 220, 277 and command edge connections including pins 86, 89, 91, 93), ¶[0072] (referring to “/CS” as commands), ¶[0068] (listing various control signals including “chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE)” signals). Given that the “write enable (WE)” is an exemplary control signal “*associated with the one or more memory read or write operations,*” *id.*; EX1024 (JESD79) at page 13 (TRUTH TABLE 1a), Hazelzet satisfies the “*wherein the module controller is configured to receive via the second edge connections the address and command signals associated with the one or more memory read or write operations*” limitation.

(2) [1.g.ii] Control the DRAM

194. Moreover, as explained in claim elements [1.b.] and [1.f.], Hazelzet discloses that the printed circuit board has a first set of edge connections for communicating data signals between the dynamic random access memory elements (within the memory module) and the memory controller of the host system, EX1014 (Hazelzet) at FIGs 7A-7C (showing data edge connections including pins 11, 12, 17, 18, 22, 23, 31, 32, 37, 38), while the memory module is in the “parity mode,” *id.* at FIG. 8 (showing “Data In” and “Data Out” in both the “parity mode” and the “ECC mode.”); *see also id.* at FIGs. 3A-3D, ¶[0015] (“The DIMM of the

present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface.”), ¶¶[0035],[0038],[0041]. Further, as explained in claim element [1.e.], data communication between the memory module and the memory controller is “*in accordance with the address and control signals.*” See, e.g., Ex. 1014 (Hazelzet) at FIGs 2,8, ¶¶[0015],[0035],[0038], [0041],[0064],[0070]; Ex. 1024 (JESD79) at page 13 (TRUTH TABLE 1a). Accordingly, Hazelzet satisfies the “*to control the dynamic random access memory elements in accordance with the address and command signals*” limitation.

h) [1.h] Fourth Wherein Clause: Parity Error

195. Claim 1 requires “*wherein the module controller is further configured to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the second mode.*”

196. As explained in claim elements [1.b.] and [1.d.], the error edge connection is coupled to the open drain output of the module controller. Ex. 1014 (Hazelzet) at FIGs 7A (showing an uncorrectable error pin UE (142) of the memory module that is coupled to the open drain output “/Error (UE)” 121); see also *id.* at FIG. 4B, ¶¶[0059],[0072].

197. In particular, Hazelzet's "ECC/Parity register" (*i.e.*, "*module controller*," as claimed) includes an "SEC/DED ECC" 90. EX1014 (Hazelzet) at FIG. 4B. FIG. 5 of Hazelzet, which is a block diagram of the "SEC/DED ECC" 90 in FIG. 4B, includes a "parity generator/checker circuit 231." EX1014 (Hazelzet) at ¶¶[0028], [0076], FIG. 5.

198. When the memory module is in the "parity mode" (*i.e.*, "*second mode*," as claimed), the "parity generator/checker circuit 231" generates and sends the "parity error signal (PERR)" to the "error logic circuit" 100. EX1014 (Hazelzet) at ¶[0076] ("FIG. 5 is a block diagram of the SEC/DED ECC circuit of FIG. 4B. ... The parity generator/checker circuit 231 further has a second input coupled to the parity in signal source 31 via primary latch 71 and output line 81 and depending on the state of the parity input signal on input 31 sends a parity error signal (PERR) on output line 111 to the error logic circuit 100."), FIG. 5; see also EX1014 (Hazelzet) at ¶[0070] ("In addition to the above ECC mode, the same twenty two chip select gated data signals can be operated in 'parity mode (/ECC Mode high)', whereby the signal received on CHK0/Parity in line is received as parity to the register one clock pulse later than the chip select gated data inputs. The received parity bit is then compared to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. The twenty two chip select gated data signals will be latched and re-

driven on the first clock pulse and any error will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses) and in the Error Bus Registers. No correction of errors will be completed in this mode. The convention of parity, in this application, is odd parity (odd numbers of 1s [*sic*] across data and parity inputs equals valid parity).”), FIG. 4B.

199. In the “parity mode” (*i.e.*, “*second mode*,” as claimed), the “parity error signal (PERR)” 111 that is fed into the “error logic circuit” 100 is used to drive the open-drain transistor in “error logic circuit” 100, which outputs to the memory controller through the output line 121 (*i.e.*, output for uncorrectable error “UE”). EX1014 (Hazelzet) at ¶[0059] (“This SEC/DED ECC circuit 90 provides three outputs 109, 110, and 111 to the error logic circuit 100. These outputs are: a correctable error (CE) line 109, an uncorrectable error (UE) line 110 and a parity error bit line 111 fed to the error logic circuit 100 which provides outputs regarding correctable and uncorrectable errors on output lines 120 and 121. When either [correctable] error line (CE) 109 or uncorrectable error line (UE) 110 is low this indicates that an error was identified as being associated with the address and/or command inputs (either correctable or uncorrectable). The error lines 120,121 will be active, *i.e.*, low, for two clock cycles simultaneous with the re-driven address/command data when operating in ECC mode or delayed by two clock cycles when operating in parity mode.”).

200. As explained above, the output line 121 (“UE”) is an open-drain output, EX1014 (Hazelzet) at ¶¶[0072], which is coupled to the memory controller of the host system using pin number 142. EX1014 (Hazelzet) at FIG. 7A (showing that the “Server PIN Number 142” corresponds to “DIMM PIN Name UE”), FIG. 2 (showing how the “DIMM 20” is coupled to the “Memory Controller or Processor 19”); *see also id.* at ¶¶[0016] (“More particularly the server of the present invention comprises a novel DIMM provided with a new and unique ECC/ Parity Register that is operable with 1 to 4 memory ranks, coupled to a memory interface chip which is in turn coupled to a memory controller or processor such that the memory controller sends address and command information to the buffer (or register) via address/command lines together with check bits for error correction purposes to the ECC/ Parity register.”), ¶¶[0038] (“In this FIG. 2 the server comprises a novel DIMM 20 provided with a novel ECC/Parity Buffer chip 21 (also referred to as a ‘buffer device’) coupled to the memory interface chip 18 which is in turn coupled to the memory controller or processor 19. ... In this configuration, the check bits and/or parity bits associated with the ECC/Parity register chip 21 are developed in the memory interface chip 18, although in other embodiments these bits could be developed in the memory controller or processor 19, be communicated to the memory interface chip as a subset of the information

on line 16 and the memory interface would then re-drive this information to the memory module on line 25”).

SERVER DIMM PIN NUMBER	PIN NAME	SERVER DIMM PIN NUMBER	PIN NAME
1	Vref	139	Vref
2	SCL	140	SCL
3	SDA	141	SDA
4	UE	142	UE
5	CE	143	CE
6	VDD	144	VDD
7	ECCMODE	145	ECCMODE
8	DLY CKE/ODT	146	DLY CKE/ODT
9	CS GATE EN	147	CS GATE EN
10	GND	148	GND
11	DQ0	149	DQ4
12	DQ1	150	DQ5
13	GND	151	GND
14	DQS0*	152	DQS9
15	DQS0	153	DQS9*
16	GND	154	GND
17	DQ2	155	DQ6
18	DQ3	156	DQ7
19	GND	157	GND
20	VDD	158	VDD
21	GND	159	GND
22	DQ8	160	DQ12
23	DQ9	161	DQ13
24	GND	162	GND
25	DQS1*	163	DQS10
26	DQS1	164	DQS10*
27	GND	165	GND
28	DQ10	166	DQ14
29	DQ11	167	DQ15
30	GND	168	GND
31	DQ16	169	DQ20
32	DQ17	170	DQ21
33	GND	171	GND
34	DQS2*	172	DQS11
35	DQS2	173	DQS11*
36	GND	174	GND
37	DQ18	175	DQ22
38	DQ19	176	DQ23
39	GND	177	GND
40	RESET	178	RESET
41	VDD	179	VDD
42	GND	180	GND
43	DQ24	181	DQ28
44	DQ25	182	DQ29
45	GND	183	GND
46	DQS3*	184	DQS12
47	DQS3	185	DQS12*
48	GND	186	GND
49	DQ26	187	DQ30
50	DQ27	188	DQ31
51	GND	189	GND
52	CB0	190	CB4

FIG. 7A

201. Hazelzet explains that the generated parity error signal is driven to the memory controller of the host system. EX1014 (Hazelzet) at ¶[0044], FIG. 2 (showing that the signals generated by the “DIMM 20” is driven to the “Memory Controller or Processor 19” through data paths 15 and 15a), ¶[0036] (“Each DRAM 11 on the DIMM 10 has a plurality of input/output pins that are coupled, via the printed circuitry on the DIMM 10 to the contacts on the DIMM 10 and theses contacts are further coupled, via a data line 15, to a memory interface chip

18 and to a memory controller or processor 19.”); *see also id.* at ¶[0072] (“Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of /Error (UE) is different in parity mode vs. ECC mode.”).

202. Hazelzet explains that the “parity operating mode” is a mode that allows the host system to “determine the error condition” of the memory module. EX1014 (Hazelzet) at ¶[0064] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”). Hazelzet further explains that such “error condition” is reported to the host “via the Uncorrectable Error (UE) line” when the memory module is in the “parity mode.” EX1014 (Hazelzet) at ¶[0070] (“In addition to the above ECC mode, the same twenty two chip select gated data signals can be operated in 'parity mode (/ECC Mode high)', whereby the signal received on CHK0/Parity in line is received as parity to the register one clock pulse later than the chip select gated data inputs. The received parity bit is then compared

to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. The twenty two chip select gated data signals will be latched and re-driven on the first clock pulse and any error will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses) and in the Error Bus Registers. No correction of errors will be completed in this mode. The convention of parity, in this application, is odd parity (odd numbers of 1s [sic] across data and parity inputs equals valid parity).”). Hazelzet further explains that the error line is driven “low, i.e., ‘0’,” when “an error is detected.” EX1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.”), ¶[0018] (“Still another object of the invention is to provide for Parity error reporting in which the parity signal is delivered one cycle after the address and command to which it applies, and the error line be driven low two clocks after the address and command bits are driven to the DRAMs from the

register on the DIMM.”), FIG. 8 (explaining that UE is driven low “if an error occurs” in the “parity mode”).

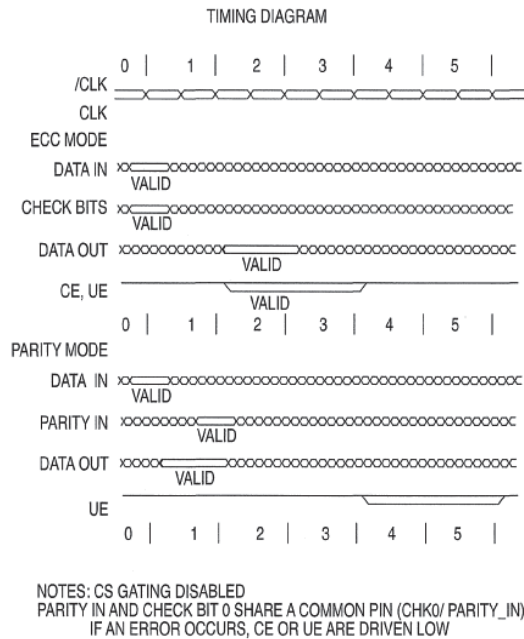


FIG. 8

203. Accordingly, Hazelzet discloses “wherein the module controller is further configured to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the second mode.”

i) [1.i] Fifth Wherein Clause: Notification Signal

204. Claim 1 requires “wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output while the memory module is in the first mode.”

205. As demonstrated above, ¶¶131-135, in the combinations analyzed here, the Hazelzet module would be modified to be configurable to enter a training mode and output JEDEC or Buchmann training status signals to the system memory controller via the open drain output UE 121. *Id.* Each of the status signals analyzed above (ERROUT#, TS0_done, TS3_ack, TS3_done) represent “a *notification signal associated with the one or more training sequences*” because each provides status about the related sequences, such as whether it has been completed or whether all memory buffers have returned an acknowledgement. *Id.* Each of these combinations therefore alternatively satisfies “*wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences.*”

206. Moreover, Hazelzet’s memory system involves sharing the open drain output so that the memory controller of the host system can receive parity error signals/notification signals from multiple memory modules using the open drain output. See, e.g., EX1014 (Hazelzet) at ¶¶[0018] (“After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules.”), [0072] (“Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred

during a valid command (/CS=low) cycle (consistent with the re-driven signals).”), [0099], [0109]; *see also* ¶¶125-130, *above*.

207. As noted above, in the combinations analyzed here, the training status signals would be at a low logic level (because the gate signals of the transistors in the open drain circuits in all the modules in which the training is ongoing are high) over an open drain output of Hazelzet until such time as the operations they related to completed for all modules of the system and the gate signals to the transistors of all the open drain circuits in all the modules are low, at which time the signals would be at a high impedance state, indicating completion. EX1017, FIG. 4; 5:65-6:12 (illustrating and describing how such a system as is in Hazelzet operates); EX1001, 9:47-10:50 (explaining in same way as Kim functioning of open-drain outputs in memory systems). As I note above, ¶¶131-135, it would have been obvious to use Hazelzet’s open drain signaling for these particular training signals because each indicates when operations carried out by multiple modules have completed. The high and low gate signals to the transistors represent “*driv[ing] a notification signal...to the error edge connection via the open drain output while the memory module is in the first mode,*” respectively or vice versa.

208. A Skilled Artisan would understand that, in the obvious combinations analyzed here, such open drain signals would be changed from a high impedance state to a low state as the gate of the transistor changes from a low to a high to

indicate the related training operations were in progress, and changed from a low state to a high impedance state as the gate of the transistor driving the signal changes from a high to a low to indicate when the related operations completed in each memory module. EX1014 (Hazelzet) at ¶¶ [0059], [0070], [0072], FIG. 4B; EX1017, FIGs. 4-5; 5:65-6:18 (teaching how a shared error pin can be implemented using an open drain configuration and/or an OR-gate); EX1015 (JEDEC), 8; EX1016 (Buchmann) at 5:51-7:2, Table 1, Table 2, FIG. 4, 8:24-9:18, Table 5, Table 6, FIG. 6, 8:24-9:17, 3:52-54, 27:18-21, 26:30-32; *see also* ¶¶ 125-130.

2. Claim 2 is Unpatentable

209. Claim 2 requires “[t]he memory module of claim 1, wherein the module controller comprises an integrated circuit.”

210. Hazelzet’s “ECC/Parity register” (*i.e.*, “module controller,” as claimed) is also referred to as a “buffer device” or a “buffer chip.” EX1014 (Hazelzet) at ¶[0038]. Hazelzet further explains that the module support devices, including “buffers” (*i.e.*, “module controller,” as claimed), “registers,” and “PLL” may be comprised of “multiple separate chips” or may be “combined onto a single package or even integrated onto a single device.” EX1014 (Hazelzet) at ¶[0115]; *see also id.* at FIG. 3A-3D, ¶[0039] (“It should be understood that the PLL chip 24 can be eliminated if its circuitry is provided on the buffer chip 21 or within the

same package as the buffer chip 21.”), ¶[0042]. Accordingly, Hazelzet discloses that “*the module controller comprises an integrated circuit,*” as claimed.

211. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy the “*wherein the module controller comprises an integrated circuit*” limitation.

3. Claim 3 is Unpatentable

212. Claim 3 requires “[t]he memory module of claim 1, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.”

213. As explained in claim element [1.d.], Hazelzet discloses that the “ECC/Parity register” (i.e., “*module controller,*” as claimed) has “open drain outputs].” Hazelzet further explains that the “ECC/Parity register” has an “error correction code circuit ECC segment 21b,” which is a “*notification circuit,*” as claimed, because it outputs signals notifying the system memory controller of correctable, uncorrectable, and parity errors. EX1014 (Hazelzet) at ¶[0044] (explaining that the “error correction code circuit ECC segment 21b” is within the “ECC/Parity buffer chip 21,” i.e., “ECC/Parity register”). Such “error correction code circuit ECC segment 21b” (within the “ECC/Parity register”) includes the circuitry for determining whether the errors occurred, SEC/DED ECC circuit 90, and error logic circuit 100 that receives error signals from SEC/DED ECC circuit

90, such as UE 110 and PERR 111, and provides the above-mentioned “open-drain output(s),” such as UE 121. EX1014 (Hazelzet) at FIG 4B, ¶¶[0059],[0072] (“Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of /Error (UE) is different in parity mode vs. ECC mode.”).

214. Hazelzet discloses that those “open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error,” and further discloses that the “outputs are driven low for two clocks to allow the memory controller time to sense the error. ... /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error.”). Further, Hazelzet explains that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” EX1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present

invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.”).

215. As noted above, the combinations analyzed here include a field effect transistor. Indeed, a Skilled Artisan would have understood the phrase “open drain” in the context of Hazelzet’s disclosures to necessarily mean the output is driven by a field effect transistor (as opposed to an open collector configuration), and that field effect transistors have three terminals, i.e., gate, source, and drain, that the drain would be connected to a pull-up resistor, the source to ground and the gate to an OR logic element that OR’ed the UE 110 and PERR 111 error signals to drive the gate, as depicted in Figure 5 of Kim. EX1017, FIGs. 4-5, 5:65-6:18; *see also generally* EX1020, U.S. 3,414,781 to Dill (“Dill”), entitled “Field Effect Transistor Having Interdigitated Source And Drain And Overlying, Insulated Gate.” A Skilled Artisan would have thus understood that the disclosed “open drain” output is the output of “*one or more transistors each having an open drain coupled to the open drain output.*” *See* ¶¶ 125-130; *see also* EX1017 (Kim)

at FIG. 4, 5:49-57, 4:40-48; 6:1-16. Furthermore, even if not inherently disclosed, it would have been obvious to a Skilled Artisan to implement in this fashion given the knowledge of a Skilled Artisan regarding open drain outputs. See ¶¶ 125-130.

216. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy “*the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output*” limitation.

217. To the extent one might argue otherwise, claim 3 would have been obvious in view of Hazelzet, JEDEC or Buchmann, and Kim. Kim discloses an “open drain output” that is an output pin coupled to the drain of a transistor, which includes three ports (*i.e.*, a gate, source, and a drain). See, *e.g.*, EX1017 (Kim) at FIG. 4. In particular, FIG. 4 of Kim shows an open drain output that is coupled to a pull-up resistor (*i.e.*, connected to a high voltage via a pull-up resistor). FIG. 4 of Kim also shows that the source of the transistor is coupled to ground and that the gate of the transistor is coupled to “ERR.”

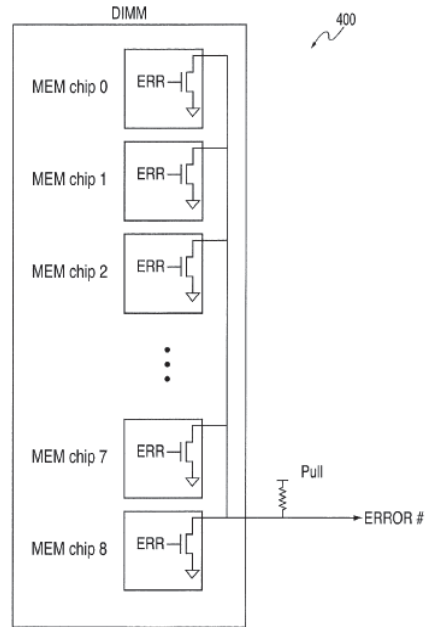


FIG. 4

218. Kim also discloses in Figure 5 the use of a logic element (an OR gate) such that multiple error signals could drive the gate of the open-drain transistor. EX1017, FIG. 5, 6:13-6:18.

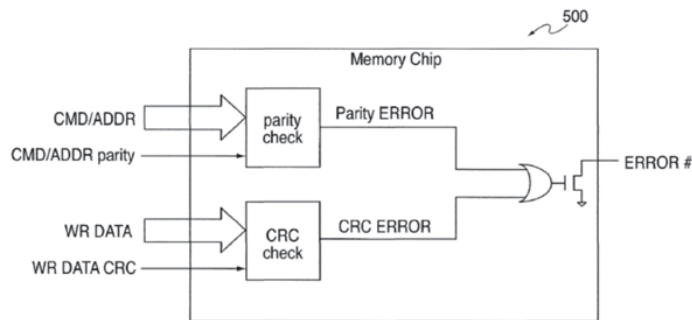
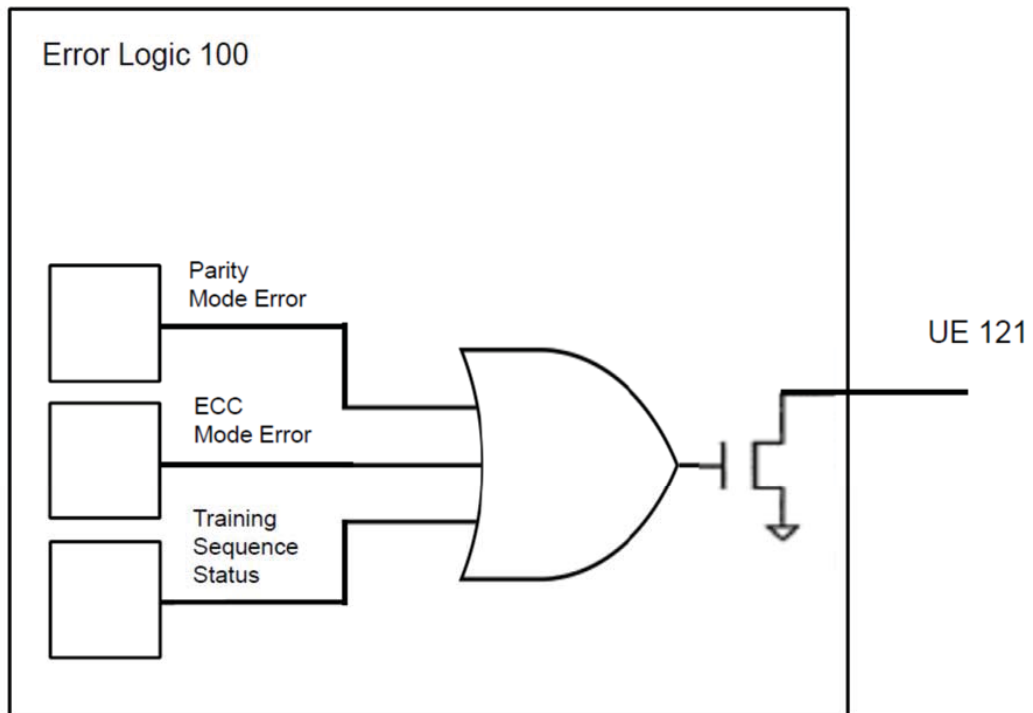


FIG. 5

219. In the combinations analyzed here, Kim's open drain transistor configuration would be included within Hazelzet's error logic 100 (which is part of the ECC segment 21b – a “notification circuit” as claimed) such that signals

indicating parity mode error, ECC mode error and training status would be provided to a logic gate, such as an OR gate, as in Kim, which would select among them based on the mode of the module, as in Hazelzet. The output of the OR gate would be coupled to, and would drive, the gate of an open drain transistor, which itself drives UE 121, as shown in the annotation below:



220. As in Hazelzet, UE 121 is coupled to an error edge connector.

221. As I note above, Hazelzet discloses that UE 121 is used in both Parity Mode and ECC Mode, so there is necessarily logic circuitry within Error Logic 100 for selecting which signal to use to drive the open drain output. Kim uses an OR gate for that function, as in this combination, but a multiplexor would have

also worked. It would have been obvious and common sense to use a three input OR gate here, since there are three modes in the modified version of Hazelzet.

222. A Skilled Artisan would understand that, in this combination, each signal input the OR gate would remain low when the module was not in its associated mode, and the signal whose mode was active could be high to indicate the occurrence of the event to be signaled (error in Parity Mode or ECC Mode; ongoing training in Training Mode), or low to indicate that the event is not occurring (Parity/ECC) or acknowledge/completed (training). The signal whose mode was active would then be passed through the OR gate to drive the gate of the transistor.

223. I note this is how both Hazelzet and JEDEC employ open drain signaling. For example, Hazelzet discloses that the “ECC/Parity register” (*i.e.*, “*module controller*,” as claimed) has “open drain output[s].” EX1014 (Hazelzet) at ¶[0072]. Hazelzet further explains that the “ECC/Parity register” has an “error correction code circuit ECC segment 21b,” which is a “*notification circuit*,” as claimed, because it outputs signals notifying the system memory controller of correctable, uncorrectable, and parity errors. EX1014 (Hazelzet) at ¶[0044]. Such “error correction code circuit ECC segment 21b” (within the “ECC/Parity register”) includes the circuitry for determining whether the errors occurred, SEC/DED ECC circuit 90, and error logic circuit 100 that receives error signals

from SEC/DED ECC circuit 90, such as UE 110 and PERR 111, and provides the above-mentioned “open-drain output(s),” such as UE 121. EX1014 (Hazelzet) at FIG 4B, ¶¶[0059],[0072]. Hazelzet discloses that those “open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error,” and further discloses that the “outputs are driven low for two clocks to allow the memory controller time to sense the error. ... /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error.”). Further, Hazelzet explains that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” EX1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.”).

224. Based upon these disclosures, a Skilled Artisan would have understood Hazelzet's open drain outputs to necessarily driven by a field effect transistor (as opposed to an open collector configuration), that field effect transistors have three terminals, *i.e.*, gate, source, and drain, that the drain would be connected to a pull-up resistor, the source to ground and the gate to an OR logic element that OR'ed the UE 110 and PERR 111 error signals to drive the gate, as depicted in Figure 5 of Kim. EX1017, FIGs. 4-5, 5:65-6:18.

225. Also, as explained above, *see* ¶¶128-130, a Skilled Artisan would have understood that an open drain output as set forth in the figure above would be pulled to a high logic level when the gate of the transistor is low, because the transistor would be off. *See, e.g.*, EX1017 (Kim) at FIG. 4. The output would then be in an un-driven, high impedance, state. EX1014 (Hazelzet) at ¶[0099]. On the other hand, the open drain output would switch to a low logic level (*e.g.*, ground), and be put in a low impedance state, when the gate of the transistor is high, because the transistor would be on. *Id.*

226. In this combination, as shown in the annotated figure above, the module controller would therefore include “*a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.*”

227. A Skilled Artisan would have been motivated to combine Kim into the obviousness combination of Hazelzet and JEDEC or Buchmann for various

reasons. Kim was filed approximately a year and a half after Hazelzet and includes some of the same disclosures. It discloses additional details regarding the use of an open-drain output on a memory module to notify the memory controller of errors during a parity normal operating mode and during an ECC normal operating mode. EX1017(Kim) at 1:16-22;5:49-57;6:8-16. To use the output-pin scheme of Kim in the system of Hazelzet would therefore have been only the use of known techniques for their known purposes to achieve predictable results, *i.e.*, using an open-drain output to provide error or status information from multiple components.

228. Kim and Hazelzet/JEDEC/Buchmann are analogous art to the 218 Patent because each is directed to the field of memory module design, including error detection and correction, initialization, training and the use of pins/paths for multiple purposes during different operations/modes, EX1001, Abstract, 5:66-6:14;8:4-48; EX1014, Abstract, ¶¶[0007],[0069]-[0070],[0123]; EX1015, 1, 3, 8; EX1016, 1:7-9;3:49-60;4:51-5:50;12:60-13:41;14:1-63;20:20-21:19;33:45-67; EX1017, 1:16-22;5:49-57;6:8-18;11:20-34;12:36-53, and also because Kim and Hazelzet/JEDEC/Buchmann are reasonably pertinent to the particular problem the inventor of the 218 Patent was trying to solve, increasing memory module capacity, performance, and/or reliability by sharing an output pin/path to perform multiple functions during multiple operations/modes, including initialization/training, EX1001, Abstract, 5:66-6:14;8:4-48; EX1014, Abstract,

¶¶[0007],[0069]-[0070],[0123]; EX1015, 1, 3, 8; EX1016, 1:7-9;3:49-60;4:51-5:50;12:60-13:41;14:1-63;20:20-21:19;33:45-67; EX1017, 1:16-22;5:49-57;6:8-18;11:20-34;12:36-53.

229. Moreover, a person of ordinary skill in the art would have been motivated to use the open-drain output pin reporting technique of Kim in the combined scheme of Hazelzet and JEDEC or Buchmann because it represented a well-known (and therefore reliable) and simple technique to provide error and/or status information from a number of memory components. See, e.g., EX1014 (Hazelzet) at ¶[0072], ¶[0122]; EX1017, FIGs. 4-5, 5:65-6:18, 12:18-23. The open-drain interrupt reporting technique of Kim permitted a single signal line with an “OR logic element” to indicate error or status information, thus simplifying the design of the system and saving pins on the various integrated circuits connected to the bus, which necessarily can have only a finite number of pins. Thus, a person of ordinary skill in the art could readily have modified Hazelzet’s open-drain output with the teachings of Kim and would have been motivated to do so.

230. Accordingly, claim 3 would have been obvious in view of Hazelzet, JEDEC or Buchmann, with or without Kim.

231. This same analysis applies to further combining Hazelzet and JEDEC or Buchmann, with Kim to satisfy the elements of claims 4-6, 10-12, or 17-20, each of which adds limitations going to details of the implementation of the open-

drain output disclosed by Hazelzet, details that Kim explicitly discloses are included as part of an open-drain output circuit. I thus cross-reference this analysis for each of those claims.

4. Claim 4 is Unpatentable

232. Claim 4 requires “[t]he memory module of claim 3, wherein the notification circuit is configured to drive the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.”

233. As demonstrated above, in the combinations analyzed here the open drain output is configured such that the transistor output is driven low (ground) while training is still occurring and driven high upon completion, thereby outputting “notification signals.” Moreover, to drive the output low (i.e., ground, i.e., “provide a low impedance path”), the gate of the transistor must be high, causing the transistor to conduct and connect the drain to ground. Conversely, to drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off. See ¶65.

234. Similarly Hazelzet explains that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” EX1014 (Hazelzet) at

¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.”). Accordingly, a Skilled Artisan would have understood that the known open-drain output for such a system, such as disclosed in Kim, was used in Hazelzet, see ¶¶128-130, *above*, and that Hazelzet’s open drain output would be left floating (*i.e.*, high impedance state) when the gate of the transistor is low, because the transistor would be off. EX1014 (Hazelzet) at ¶[0099]; see ¶¶128-130, *above* ; EX1017 (Kim) at FIG. 4. On the other hand, Hazelzet’s open drain output would switch to a low logic level (*e.g.*, ground) when the gate of the transistor is high, because the transistor would be on. *Id.* See ¶¶125-130.

235. Accordingly, one skilled in the art would have known that the open drain output along with the edge connection connected to the open drain output would both be driven to ground when the gate is driven high. See analysis in claim element [1.i.] and claim 3; EX1014 (Hazelzet) at ¶[0099]; see ¶¶125-130; see also EX1017 (Kim) at FIGs. 4-5, 5:65-6:18. Likewise, one skilled in the art knew that

the open drain output along with the edge connection connected to the open drain output would both be driven to a high impedance state (through the pull up resistor) when the gate is driven low. *Id.*

236. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy “*the notification circuit is configured to drive the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground*” limitation.

237. To the extent one might argue otherwise, the module controller of the obvious combination of Hazelzet, JEDEC or Buchmann, and Kim, described above, includes a notification circuit configured to “*drive the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground*” for the reasons set forth in ¶¶222-225 above.

5. Claim 5 is Unpatentable

238. Claim 5 requires “[t]he memory module of claim 4, wherein the notification circuit is configured to drive the parity error signal by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.

239. As explained in claim element [1.h.], see ¶¶197-202, *above*, Hazelzet explains that its “ECC/Parity register” (*i.e.*, “*module controller*”) has “open-drain output[s]” (*i.e.*, “Uncorrectable Error (UE) line[s]”) capable of utilizing “parity error signals” (PERR) to output signal UE 121 to the host indicating a parity error. See analysis in claim element [1.f.]; EX1014, ¶¶[0059],[0070],[0072], [0076]. Further, as explained in claim element [1.h.], when the memory module is in the “parity mode” (*i.e.*, “*second mode*,” as claimed), the “parity generator/checker circuit 231” (within SEC/DED ECC circuit 90) generates and sends the “parity error signal (PERR)” to the “error logic circuit” 100 (all part of the “*notification circuit*”). EX1014 (Hazelzet) at FIGs. 4B-5, ¶¶[0059],[0070],[0072],[0076] (“FIG. 5 is a block diagram of the SEC/DED ECC circuit of FIG. 4B. ... The parity generator/checker circuit 231 further has a second input coupled to the parity in signal source 31 via primary latch 71 and output line 81 and depending on the state of the parity input signal on input 31 sends a parity error signal (PERR) on output line 111 to the error logic circuit 100.”).

240. In particular, Hazelzet explains that in the “parity mode,” the parity error “will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses).” EX1014 (Hazelzet) at ¶[0070]; *see also id.* at [0018] (“After holding the error line low for only 2 clock cycles, the driver can be

disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules.”).

241. Further, as explained in claim 4, see ¶233, above, Hazelzet discloses that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” EX1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.”).

242. Accordingly, Hazelzet discloses that the open-drain output (UE 121) in each memory module is configured to “*drive the parity error signal by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.*” See also analysis in claim 4; EX1017, FIGs. 4-5, 5:65-6:18; see ¶¶125-130, above.

243. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy the “*wherein the notification circuit is configured to drive the parity error signal by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground*” limitation.

244. To the extent one might argue otherwise, the module controller of the obvious combination of Hazelzet, JEDEC or Buchmann, and Kim, described above, includes a memory module configured to “*drive the parity error signal by driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.*,” for the reasons set forth in ¶¶222-225 above. In particular, the module is “*configured*” to output the parity error as claimed because it can be configured to be in the Parity Mode.

6. Claim 6 is Unpatentable

245. Claim 6 requires: “*The memory module of claim 4, wherein the notification circuit is configured to drive the notification signal using one or more OR logic elements.*”

246. As explained in claim 3, Hazelzet’s “error correction code circuit ECC segment 21b” (within the “ECC/Parity register”) is the “*notification circuit*,” as claimed. See ¶213, above.

247. FIG. 4B of Hazelzet shows the “error correction code circuit segment 21b.” EX1014 (Hazelzet) at ¶¶[0044],[0059], FIG. 4B. Within Hazelzet’s error correction code circuit ECC segment 21b is “Error Logic 100.” *Id.* Hazelzet discloses that Error Logic 100 receives the “US [sic] 110” signal and the “PERR 111” signal, and outputs one of these signals to the same “/ERROR (UE)” pin depending on which mode the memory module is in. See EX1014 (Hazelzet) at FIG. 4B (showing an open-drain output “/ERROR (UE) 121” for uncorrectable error or parity error, depending on the mode of operation), ¶¶[0072] (explaining that “/Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error.”), ¶¶[0044],[0059],[0069-71]. As set forth above, see ¶¶131-135, in the combinations analyzed here, that circuitry would be modified to implement the additional training mode, in which the UE 121 open drain output would, when the module is in the training mode, be used to send the notification/status signals identified above.

248. Hazelzet also discloses that UE 121 is an open drain output, EX1014, [0072], which a Skilled Artisan would necessarily understand is driven by a transistor in an open drain configuration. EX1017, FIGs. 4-5, 5:65-6:18 (depicting in FIG. 5 OR logic gate used for such purpose); see ¶¶125-130, *above*. A Skilled

Artisan would understand that such a transistor necessarily has “a *gate*” that can be driven to assert the open drain output. *Id.*

249. Because in the combinations analyzed here, Error Logic 100 receives both “US [sic] 110” signal and the “PERR 111” signal and the training mode notification signals, but uses only one such signal to drive the UE 121 output, depending on mode, a Skilled Artisan would understand that Error Logic 100 would necessarily include “one or more OR logic elements,” such as a three-input OR gate, to determine which signal should be used to drive the transistor, thus the circuit would be “*configured to drive the notification signal using one or more OR logic elements.*” EX1017, FIGs. 4-5, 5:65-6:18 (depicting in FIG. 5 OR logic gate used for such purpose); see ¶¶ 125-130, *above*. Moreover, the signal driving that gate is necessarily related to one of the signals input to Error Logic 100 (*e.g.*, “PERR 111” (“*first signal*”) or the training notification signals (“*notification signal*”), depending on mode, so it is “*configured to drive the notification signal using one or more OR logic elements.*”

250. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy the “*wherein the notification circuit is configured to drive the notification signal using one or more OR logic elements.*” limitation.

251. To the extent one might argue otherwise, the notification circuit of the obvious combination of Hazelzet, JEDEC or Buchmann, and Kim, described

above, includes “*driv[ing] the notification signal using one or more OR logic elements,*” for the reasons set forth in ¶¶219-225 above. In particular, the circuit is “*configured*” in this manner because it be placed in either the Parity Mode or the Training Mode.

7. Claim 7 is Unpatentable

252. Claim 7 requires “[t]he memory module of claim 1, wherein the first edge connections are not active when the memory module is in the first mode and configured to be trained with the one or more training sequences.”

253. As explained in claim element [1.b.], Hazelzet discloses a second set of edge connections for communicating address and control signals from the memory controller of the host system. EX1014 (Hazelzet) at FIGs 7A-7C (showing address edge connections including pins 67, 70, 72-75, 82, 205-207, 210-213, 220, 277 and command edge connections including pins 86, 89, 91, 93), ¶[0072] (referring to “/CS” as commands), ¶[0068] (listing various control signals including “chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE)” signals); *see also* EX1014 (Hazelzet) at ¶[0038] (“The memory interface chip 18 then sends and receives data, via line 15, to the memory devices or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16 and check bits for error

correction purposes to the ECC/ Parity register chip 21 via line 25.”), FIG. 2 (showing address and command line 16); see ¶¶157-162, *above*.

254. In the JEDEC combination analyzed here, JEDEC discloses that during the MB-DRAM training (i.e., the mode that is added to Hazelzet here), “[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low.” EX1015, 8. A Skilled Artisan would understand from this that during such training the address/control pins would remain inactive as those are pins used to provide “DRAM commands or control word writes,” and no data signals would be communicated on the data pins (“*first edge connections*”), so they would be inactive as well. *Id.*

255. Similarly, in a Buchmann combination analyzed here, in which only the TS0 training operations are carried out in the training mode (“*first mode*”), the address/control and data pins (data pins are the “*first edge connections*”) of the module edge connections would not be active during that training because TS0 training involves training of the “clock” itself, and no address/control or data signals are transmitted between the host and the memory module during such training. EX1016 (Buchmann) at 5:51-7:2.

256. To the extent Patent Owner argues otherwise, a Skilled Artisan would have found it obvious at least not to send any data, control or address signals while the clock is being trained for the same reasons set forth above. For example, a Skilled Artisan would have been motivated to keep the pin(s) for address, control and data inactive to conserve power and/or avoid unreliable operation during periods that the clock may be unstable.

257. Moreover, I understand that a negative limitation is satisfied by silence in the prior art. *Süd-Chemie, Inc. v. Multisorb Technologies, Inc.*, 554 F.3d 1001, 1004-05 (Fed. Cir. 2009). I understand that this claim includes a negative limitation, because it requires “*not active*.” Neither Hazelzet nor JEDEC or Buchmann disclose pins (much less all pins) in the first edge connections being inactive while the memory module is in the training modes.

258. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy the “*wherein the first edge connections are not active when the memory module is in the first mode and configured to be trained with one or more training sequences*” limitation.

8. Claim 8 is Unpatentable

259. Claim 8 requires “*The memory module of claim 1, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences.*”

260. As demonstrated above, ¶¶131-135, in the combinations analyzed here, the Hazelzet module would be modified to be configurable to enter a training mode and output JEDEC or Buchmann training status signals (“*notification signals*”) to the system memory controller via open drain output UE 121. *Id.* Each of the status signals analyzed above (ERROUT#, TS0_done, TS3_ack, TS3_done) “*indicate a status of the one or more training sequences*” because each provides status about the related sequences, such as whether it has been completed or whether all memory buffers have returned an acknowledgement. *Id.* Each of these combinations therefore alternatively satisfies “*wherein the module controller is configured to drive a notification signal indicating status of the one or more training sequences.*”

261. Accordingly, the obvious combinations of Hazelzet and JEDEC or Buchmann satisfy the “*wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences*” limitation.

9. Claim 9 is Unpatentable

a) [9.a] Preamble

262. The preamble of claim 9 requires “[a] *method performed by a memory module operating with a memory controller of the host system.*”

263. This limitation is satisfied, because Hazelzet and JEDEC or Buchmann disclose corresponding methods in connection with the operation of the apparatus (analyzed in connection with claim 1).

b) [9.b] DRAMs

264. Claim 9 recites “*the memory module including dynamic random access memory elements on a printed circuit board.*”

265. The claim element is satisfied for the same reasons as set forth for claim element [1.c].

c) [9.c] Printed Circuit Board

266. Claim 9 recites “*the printed circuit board having edge connections that fit into a corresponding slot of a host system, the edge connections including first edge connections via which the dynamic random access memory devices communicate data with the memory controller, second edge connections via which the memory module receives address and command signals from the memory controller, and an error edge connection in addition to the first edge connections and the second edge connections.*”

267. The claim element is satisfied for the same reasons as set forth for claim elements [1.b] (identifying PCB and edge connections) and [1.f] (explaining coupling of edge connections to DRAMs and module controller).

d) [9.d] Receiving Signals Associated with Read or

Write Operations

268. Claim 9 recites “*receiving from the memory controller address and command signals associated with one or more memory read or write operations.*”

269. This limitation is satisfied for the reasons set forth for claim element [1.g]. Specifically, Hazelzet discloses memory operations that entail the module receiving address and control signals from a system memory controller via the respective address and control edge connections.

e) [9.e] Controlling the DRAM Elements

270. Claim 9 recites “*controlling the dynamic random access memory elements in accordance with the address and command signals*”

271. This limitation is satisfied for the reasons set forth for claim element [1.g]. Specifically, Hazelzet discloses memory operations that entail the module receiving address and control signals from a system memory controller via the respective address and control edge connections, and in response communicating data between the system memory controller and the module DRAMs via the data edge connections under the control of the module controller.

f) [9.f] Outputting a Parity Error Signal

272. Claim 9 recites “*outputting to the memory controller via an open-drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module*”

273. This limitation is satisfied for the reasons set forth for claim element [1.h]. Hazelzet discloses the module outputting, in the “*second mode*,” a parity error signal via an open drain output (UE 121) in connection with memory read and write operations accessing the module.

g) [9.g] Training with One or More Training Sequences

274. Claim 9 recites “*training with one or more training sequences while the first edge connections are not active*”

275. This limitation is satisfied for the same reasons set for in claim elements [1.e.] (explaining training that occurs) and claim 7 (explaining that “first edge connections are not active” during that training).

h) [9.h] Driving a Notification Signal

276. Claim 9 recites “*driving a notification signal associated with the one or more training sequences to the memory controller via the open drain output and the error edge connection.*”

277. This limitation is satisfied for the same reasons set forth in claim element [1.g]. Specifically, as demonstrated above, ¶¶131-135, the combinations analyzed here include a module that performs training sequence operations and outputs to the system memory controller training notification signals (*e.g.*, ERRROUT#, TS0_done, TS3_ack, TS3_done) via an open drain output (UE 121).

10. Claim 10 is Unpatentable

278. Claim 10 recites “[t]he method of claim 9, wherein driving the notification signal comprises driving a gate of each of one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground, the one or more transistors each having an open drain coupled to the open drain output.”

279. This claim is satisfied for the same reasons set for in claims 3 and 4. Specifically, the analysis above for claim 3 satisfies “wherein driving the notification signal comprises driving ... one or more transistors ... the one or more transistors each having an open drain coupled to the open drain output.” The analysis above for claim 4 satisfies “driving a gate of each of [the] one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground.”

280. To the extent one might argue otherwise, the module controller of the obvious combination of Hazelzet, JEDEC or Buchmann, and Kim, described above, includes a memory module configurable “driving a gate of each of one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground, the one or more transistors each having an open drain coupled to the open drain output” for the reasons set forth in ¶¶222-225 above.

11. Claim 11 is Unpatentable

281. Claim 11 requires “[t]he method of claim 10, wherein driving the signal indicating the parity error comprises driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path from the open drain output to ground.”

282. This claim is satisfied for the same reasons as set forth for claim 5.
See ¶¶209-211, above.

12. Claim 12 is Unpatentable

283. Claim 12 requires “[t]he method of claim 10, wherein driving the notification signal comprises using one or more OR logic elements.”

284. This claim is satisfied for the same reasons as set forth for claim 6.
See ¶213, above.

13. Claim 13 is Unpatentable

285. Claim 13 requires “[t]he method of claim 9, wherein the memory module is configured to be trained with the one or more training sequences in response to a request by the memory controller.”

286. In the combinations analyzed here, ¶¶131-135, it would have been obvious to train the memory module with one or more training sequences that initiates in response to a request by the memory controller, given that JEDEC explains that, for MB-DRAM training, “the host triggers the DRAM interface training by setting the control bit DA4 in F0RC12,” EX1015, 8, and that

Buchmann explains that “[t]he memory system includes a memory controller that includes logic for initiating ... initialization training sequence for the memory system.” EX1016 (Buchmann) at 1:56-59. Buchman further explains that “the memory buffer [in the memory module] includes logic for executing a power-on and initialization training sequence initiated by the memory controller.” EX1016 (Buchmann) at 1:46-48; *see also id.*, 6:51-7:2 (for the TS0 training sequence), 8:24-29 (for the TS3 training sequence); EX1015, 3 (noting it provides “an overview of the power-up initialization of the Memory Buffer”).

287. Accordingly, the obvious combinations of Hazelzet and JEDEC or Buchmann satisfy the “*wherein the memory module is configured to be trained with the one or more training sequences in response to a request by the memory controller*” limitation.

14. Claim 14 is Unpatentable

288. Claim 14 requires “[t]he method of claim 9, wherein the notification signal indicates a status of the one or more training sequences.”

289. This claim is satisfied for the same reasons as set forth for claim 6. See ¶¶245-251, above.

15. Claim 15 is Unpatentable

a) [15.a] Preamble

290. Claim 15 requires “[a] memory module operable with a memory controller of a host system, comprising.”

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291. This claim element is satisfied for the same reasons as set forth for claim element [1.a].

b) [15.b] Printed Circuit Board

292. Claim 15 recites “*a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and command signals, and an error edge connection in addition to the first edge connections and the second edge connections.*”

293. This limitation is satisfied for the reasons set forth for claim elements [1.b] (identifying PCB and edge connections) and [1.f] (explaining coupling of edge connections to DRAMs and module controller).

c) [15.c] DRAMs

294. Claim 15 recites “*dynamic random access memory elements on the printed circuit board and configurable to communicate data signals with the memory controller via the first edge connections*”

295. This limitation is satisfied for the reasons set forth in claim elements [1.c.] (identifying DRAMs on PCB) and [1.f.] (explaining coupling of edge connections to DRAMs).

d) [15.d] Module Controller

296. Claim 15 recites “*a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection.*”

297. This limitation is satisfied for the reasons set forth in claim element [1.d.].

e) [15.e] A First Operation And A Second Operation

298. Claim 15 recites “*wherein the memory module is configurable to perform at least a first operation and a second operation*”

299. This limitation is satisfied for the reasons set forth in claim elements [1.e.i]. The claimed “*first operation*” corresponds to the “*second mode*” of claim 1 and the claimed “*second operation*” corresponds to the “*first mode*” of claim 1.

f) [15.f] First Wherein Clause

(1) [15.f.i] Receive Via Second Edge Connections

300. Claim 15 recites “*wherein the module controller in the first operation is configured to receive via the second edge connections address and command signals associated with one or more memory read or write operations.*”

301. This limitation is satisfied for the reasons set forth for claim element [1.g]. Specifically, Hazelzet discloses memory operations that entail the module receiving address and control signals from a system memory controller via the respective address and control edge connections.

(2) [15.f.ii] *Control the DRAM*

302. Claim 15 recites “*to control the dynamic random access memory elements in accordance with the address and command signals*”

303. This limitation is satisfied for the reasons set forth for claim element [1.g]. Specifically, Hazelzet discloses memory operations that entail the module receiving address and control signals from a system memory controller via the respective address and control edge connections, and in response communicating data between the system memory controller and the module DRAMs via the data edge connections under the control of the module controller.

g) [15.g] *Second Wherein Clause: Output a Parity Signal*

304. Claim 15 recites “*wherein the module controller in the first operation is further configured to output to the memory controller a signal indicating a parity error having occurred in the memory module*”

305. This limitation is satisfied for the reasons set forth for claim element [1.h]. Hazelzet discloses the module outputting, in the “*second mode*,” corresponding to the “*first operation*” in this claim, a parity error signal via an open drain output (UE 121) in connection with memory read and write operations accessing the module.

h) [15.h] Third Wherein Clause: Trained

306. Claim 15 recites “*wherein the memory module in the second operation is configured to be trained with one or more training sequences while the first edge connections are not active.*”

307. This limitation is satisfied for the same reasons set for in claim elements [1.e.] (explaining training that occurs) and claim 7 (explaining that “first edge connections are not active” during that training.

i) [15.i] Fourth Wherein Clause: Drive a Notification Signal

308. Claim 15 recites “*wherein the module controller in the second operation is configured to drive a notification signal associated with the one or more training sequences to the error edge connection via the open drain output of the module controller.*”

309. This limitation is satisfied for the same reasons set forth in claim element [1.g]. Specifically, as demonstrated above, ¶¶131-135, the combinations analyzed here include a module that performs training sequence operations and outputs to the system memory controller training notification signals (*e.g.*, ERROUT#, TS0_done, TS3_ack, TS3_done, TS3_ack) via an open drain output (UE 121) of the module controller.

16. Claim 16 is Unpatentable

310. Claim 16 requires “[t]he memory module of claim 15, wherein the module controller comprises an integrated circuit.

311. This claim is satisfied for the same reasons set forth for claim 2. See ¶¶210-211, above.

17. Claim 17 is Unpatentable

312. Claim 17 recites “[t]he memory module of claim 15, wherein the module controller includes a notification circuit comprising one or more transistors each having an open drain coupled to the open drain output.”

313. The claim is satisfied for the same reasons set forth for claim 3. See ¶¶212-231, above.

18. Claim 18 is Unpatentable

314. Claim 18 requires “[t]he memory module of claim 17, wherein the notification circuit is configured to generate the notification signal by driving a gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.”

315. The claim is satisfied for the same reasons set forth for claim 4. See ¶¶232-237, above.

19. Claim 19 is Unpatentable

316. Claim 19 requires “The memory module of claim 18, wherein the notification circuit is configured to drive the signal indicating the parity error by

driving the gate of each of the one or more transistors to a logic high level to provide a low impedance path between the open drain output to ground.”

317. This claim is satisfied for the same reasons set forth for claim 5. See ¶¶238-244, above.

20. Claim 20 is Unpatentable

318. Claim 20 requires “[t]he memory module of claim 18, wherein the notification circuit is configured to drive the notification signal using one or more OR logic elements.”

319. The claim is satisfied for the same reasons as set forth for claim 6. See ¶¶245-251, above.

21. Claim 21 is Unpatentable

320. Claim 21 recites “[t]he memory module of claim 15, wherein the memory module is configured to perform the second operation in response to a command from the memory controller.”

321. The claim is satisfied for the same reasons as set forth for claim 13. See ¶¶285-287, above.

22. Claim 22 is Unpatentable

322. Claim 22 requires “[t]he memory module of claim 15, wherein the module controller is configured to drive the notification signal to indicate a status of the one or more training sequences.”

Declaration of Dr. Donald Alpert Regarding U.S. Patent No. 9,858,218

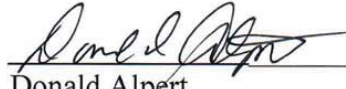
323. This claim is satisfied for the same reasons as set forth for claim 8.

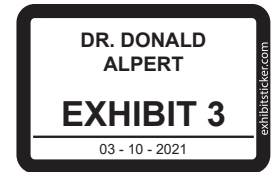
See ¶¶259-261, *above*.

* * *

I, Donald Alpert, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

Executed on: June 8, 2020


Donald Alpert



UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC. and SK HYNIX AMERICA INC.,
Petitioners,

v.

NETLIST, INC.
Patent Owner

Patent No. 10,474,595

Issued: November 12, 2019

Filed: December 28, 2017

Inventors: Hyun Lee

Title: Memory Module Having An Open-Drain Output Pin For Parity Error
In a First Mode and For Training Sequences In A Second Mode

Inter Partes Review No. IPR2020-01042

**DECLARATION OF DR. DONALD ALPERT REGARDING U.S. PATENT
NO. 10,474,595**

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1003, Cover

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I. INTRODUCTION

A. Engagement

1. I have been retained by counsel for SK hynix as an expert witness in the above-captioned proceeding. I have been asked to provide my opinion about the state of the art of the technology described in U.S. Patent No. 10,474,595 (“the 595 Patent”) (Ex. 1001) and on the patentability of the claims of this patent. The following is my written declaration on these topics.

B. Background and Qualifications

2. I am an independent consultant with Camelback Computer Architecture, LLC. My residence and place of business is at 2020 21st Street, Sacramento, CA 95818. I am over the age of eighteen, and I am a citizen of the United States.

3. I have 45 years of academic and industrial experience in applying, designing, studying, teaching, and writing about microprocessors and computer systems. I received an Electrical Engineering Ph.D. degree in 1984 from Stanford University. I earlier received an Electrical Engineering B.S. degree from MIT in 1973 and an Electrical Engineering M.S. degree from Stanford University in 1978. I have taught classes in computer architecture at Stanford, Tel Aviv, and Arizona State Universities.

4. From 1976 to 1977, I worked at Burroughs Corporation, where I designed peripheral interface controllers, including those for serial data

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communications based on Intel 8080 microprocessor components. From 1980 to 1989, I was the lead architect for the design of three high-performance microprocessors at Zilog and National Semiconductor. Later, at Intel, I was the lead architect of the Pentium® Processor from 1989 to 1992 and of the 815 chipset from 1999 to 2000, both of which became the most widely used PC components of their time. The 815 chipset comprised two components: (1) a memory controller hub (MCH) that included a graphics controller and memory controller with interfaces to the CPU, 133 MHz SDRAM system memory modules, an optional, external graphics controller and (2) an I/O controller hub (ICH) that included various I/O controllers (*e.g.*, network, hard drive, USB) for system peripheral devices. Additionally, I served as co-manager for the Itanium processor design from 1993-1997.

5. I am a Senior Member of the Institute of Electrical and Electronics Engineers (IEEE), and served as the chair of the IEEE Technical Committee on Microprocessors and Microcomputers from 1999 to 2000. I was the keynote speaker at the first Cool Chips conference, dedicated to the study of low-power microprocessors and systems. I have given invited lectures at several universities, and published ten papers in various professional journals and conference proceedings. My paper entitled “Architecture of the Pentium Processor,” was selected as best paper in IEEE Micro for 1993. I am a named inventor on over 30

U.S. patents that pertain to microprocessors, computer systems, and related technology.

6. I have reviewed the 595 Patent, and I am familiar with the patent's subject matter, which is within the scope of my education and professional experience. Based at least on my background in academia, industry, and consulting, I am familiar with the issues and technology relating to processors, chipsets, memory, and peripheral devices for computer systems. I have personally analyzed, developed, and tested such computer components and systems. More specifically, the Pentium® Processor and 815 chipset for which I was the lead architect at Intel implemented various features for initializing, calibrating, and testing the memory system, which comprised cache memory, a memory controller, and standard SDRAM modules.

7. My Curriculum Vitae, including my publications and patents, is submitted herewith as Ex. 1004.

C. Compensation and Prior Testimony

8. I am being compensated at a rate of \$550.00 per hour for my study and testimony in this matter. I am also being reimbursed for reasonable and customary expenses associated with my work and testimony in this investigation. My compensation is not contingent on the outcome of this matter or the specifics of my testimony.

9. I have previously submitted declarations in six IPR proceedings, namely IPR2014-00970, IPR2014-00971, IPR2015-00148, IPR2015-00191, IPR2017-00548, and IPR2018-00303. Additionally I have testified as an expert witness in Federal Court and the ITC, as summarized in Exhibit 1004 at 6-7.

D. Information Considered

10. My opinions are based on my years of education, research and experience, as well as my investigation and study of relevant materials. In forming my opinions, I have considered the materials I identify in this report and those listed in the Petition's Attachment B.

11. I may rely upon these materials and/or additional materials to respond to arguments raised by the Patent Owner. I may also consider additional documents and information in forming any necessary opinions — including documents that may not yet have been provided to me.

12. My analysis of the materials produced in this investigation is ongoing and I will continue to review any new material as it is provided. This report represents only those opinions I have formed to date. I reserve the right to revise, supplement, and/or amend my opinions stated herein based on new information and on my continuing analysis of the materials already provided.

II. LEGAL STANDARDS FOR PATENTABILITY

13. In expressing my opinions and considering the subject matter of the claims of the 595 Patent, I am relying upon certain basic legal principles that have been explained to me.

14. First, I understand that for an invention claimed in a patent to be found patentable, it must be, among other things, new and not obvious from what was known before the invention was made.

15. I understand the information that is used to evaluate whether an invention is new and not obvious is generally referred to as “prior art” and generally includes patents and printed publications (*e.g.*, books, journal publications, articles on websites, product manuals, *etc.*).

16. I understand that in this proceeding the Petitioner has the burden of proving that the claims of the 595 Patent are anticipated by or obvious from the prior art by a preponderance of the evidence. I understand that “a preponderance of the evidence” is evidence sufficient to show that a fact is more likely true than it is not.

17. I understand that in this proceeding, the claims should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. The claims after being construed in this manner are then to be compared to the information in the prior art.

18. I understand that in this proceeding, the information that may be evaluated is limited to patents and printed publications. My analysis below compares the claims to patents and printed publications that are prior art to the claims.

19. I understand that there are various ways in which prior art may render a patent claim unpatentable. First, the prior art can be shown to “anticipate” the claim. Second, the prior art can be shown to have made the claim “obvious” to a person of ordinary skill in the art. Third, I understand that a patent claim may be invalid where the specification of the patent fails to provide a written description adequate to support the claim. Fourth, I understand that a patent claim may be invalid when the claim fails to particularly point out and distinctly claim the subject matter of what the inventor regards as the invention. My understanding of the legal standards is set forth below.

A. Anticipation

20. I understand that the following standards govern the determination of whether a patent claim is “anticipated” by the prior art.

21. I have applied these standards in my evaluation of whether the claims of the 595 Patent would have been anticipated by the prior art.

22. I understand that the “prior art” includes patents and printed publications that existed before the earliest filing date (the “effective filing date”)

of the claim in the patent. I also understand that a patent will be prior art if it was filed before the effective filing date of the claimed invention, while a printed publication will be prior art if it was publicly available before that date.

23. I understand that, for a patent claim to be “anticipated” by the prior art, each and every requirement of the claim must be found, expressly or inherently, in a single prior art reference as recited in the claim. I understand that claim limitations that are not expressly described in a prior art reference may still be there if they are “inherent” to the thing or process being described in the prior art. For example, an indication in a prior art reference that a particular process complies with a published standard would indicate that the process must inherently perform certain steps or use certain data structures that are necessary to comply with the published standard.

24. I understand that if a reference incorporates other documents by reference, the incorporating reference and the incorporated reference(s) should be treated as a single prior art reference for purposes of analyzing anticipation.

25. I understand that it is acceptable to consider evidence other than the information in a particular prior art document to determine if a feature is necessarily present in or inherently described by that reference.

B. Obviousness

26. I understand that a claimed invention is not patentable if it would have been obvious to a person of ordinary skill in the field of the invention at the time the invention was made.

27. I understand that the obviousness standard is defined in the patent statute (35 U.S.C. § 103(a)) as follows:

28. A patent may not be obtained although the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be denied by the manner in which the invention was made.

29. I understand that the following standards govern the determination of whether a claim in a patent is obvious. I have applied these standards in my evaluation of whether the asserted claims of the 595 Patent would have been considered obvious as of the priority date of the patent.

30. I understand that to find a claim in a patent obvious, one must make certain findings regarding the claimed invention and the prior art. Specifically, I

understand that the obviousness question requires consideration of four factors (although not necessarily in the following order):

- The scope and content of the prior art;
- The differences between the prior art and the claims at issue;
- The knowledge of a person of ordinary skill in the pertinent art; and
- Whatever objective factors indicating obviousness or non-obviousness may be present in any particular case.

31. In addition, I understand that the obviousness inquiry should not be done in hindsight, but must be done using the perspective of a person of ordinary skill in the relevant art as of the effective filing date of the patent claim.

32. I understand the objective factors indicating obviousness or non-obviousness may include: commercial success of products covered by the patent claims; a long-felt need for the invention; failed attempts by others to make the invention; copying of the invention by others in the field; unexpected results achieved by the invention; praise of the invention by those in the field; the taking of licenses under the patent by others; expressions of surprise by experts and those skilled in the art at the making of the invention; and the patentee proceeded contrary to the accepted wisdom of the prior art. I also understand that any of this evidence must be specifically connected to the invention rather than being associated with the prior art or with marketing or other efforts to promote an invention. I am not presently aware of any evidence of “objective factors”

suggesting the claimed methods are not obvious, and reserve my right to address any such evidence if it is identified in the future.

33. I understand the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. I also understand that an example of a solution in one field of endeavor may make that solution obvious in another related field. I also understand that market demands or design considerations may prompt variations of a prior art system or process, either in the same field or a different one, and that these variations will ordinarily be considered obvious variations of what has been described in the prior art.

34. I also understand that if a person of ordinary skill can implement a predictable variation, that variation would have been considered obvious. I understand that for similar reasons, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using that technique to improve the other device would have been obvious unless its actual application yields unexpected results or challenges in implementation.

35. I understand that the obviousness analysis need not seek out precise teachings directed to the specific subject matter of the challenged claim, but instead can take account of the “ordinary innovation” and experimentation that

does no more than yield predictable results, which are inferences and creative steps that a person of ordinary skill in the art would employ.

36. I understand that sometimes it will be necessary to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art. I understand that all these issues may be considered to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue.

37. I understand that the obviousness analysis cannot be confined by a formalistic conception of the words “teaching, suggestion, and motivation.” I understand that in 2007, the Supreme Court issued its decision in *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 418 (2007), where the Court rejected the previous requirement of a “teaching, suggestion, or motivation to combine” known elements of prior art for purposes of an obviousness analysis as a precondition for finding obviousness. It is my understanding that *KSR* confirms that any motivation that would have been known to a person of skill in the art, including common sense, or derived from the nature of the problem to be solved, is sufficient to explain why references would have been combined.

38. I understand that a person of ordinary skill attempting to solve a problem will not be led only to those elements of prior art designed to solve the

same problem. I understand that under the *KSR* standard, steps suggested by common sense are important and should be considered. Common sense teaches that familiar items may have obvious uses beyond the particular application being described in a reference, that if something can be done once it is obvious to do it multiple times, and in many cases a person of ordinary skill will be able to fit the teachings of multiple patents together like pieces of a puzzle. As such, the prior art considered can be directed to any need or problem known in the field of endeavor and can provide a reason for combining the elements of the prior art in the manner claimed. In other words, the prior art does not need to be directed towards solving the same problem that is addressed in the patent. Further, the individual prior art references themselves need not all be directed towards solving the same problem.

39. I understand that obviousness does not require that the features of a secondary reference be bodily incorporated into the structure of the primary reference. Rather, the test is what the combined teachings of those references would have suggested to a Skilled Artisan. The disclosures of the prior art references need not be physically combinable. Combining the teachings of references should be the focus of the analysis.

40. I understand that an invention that might be considered an obvious variation or modification of the prior art may be considered non-obvious if one or more prior art references discourages or lead away from the line of inquiry

disclosed in the reference(s). A reference does not “teach away” from an invention simply because the reference suggests that another embodiment of the invention is better or preferred. My understanding of the doctrine of teaching away requires a clear indication that the combination should not be attempted (*e.g.*, because it would not work or explicit statements saying the combination should not be made).

41. I understand that a person of ordinary skill is also a person of ordinary creativity.

42. I further understand that in many fields, it may be that there is little discussion of obvious techniques or combination, and it often may be the case that market demand, rather than scientific literature or knowledge, will drive design trends. When there is such a design need or market pressure to solve a problem and there are a finite number of identified, predictable solutions, a person of ordinary skill has good reason to pursue the known options within their technical grasp. If this leads to the anticipated success, it is likely the product not of innovation but of ordinary skill and common sense. In that instance the fact that a combination was obvious to try might show that it was obvious. The fact that a particular combination of prior art elements was “obvious to try” may indicate that the combination was obvious even if no one attempted the combination. If the combination was obvious to try (regardless of whether it was actually tried) or

leads to anticipated success, then it is likely the result of ordinary skill and common sense rather than innovation.

III. THE 595 PATENT

A. Effective Filing Date of the 595 Patent

43. The 595 Patent is a continuation of, inter alia, a utility application filed June 14, 2010, and also claims priority to U.S. Provisional Application No. 61/186,799 (EX1008), filed June 12, 2009. EX1001, Face. I have been asked to give my opinion as to whether, from the perspective of a Skilled Artisan, the provisional application shows that the inventor actually invented what is claimed in each of the claims of the 595 patent, and possessed the claimed subject matter, as of the provisional filing date. When considering that question, I have considered whether the provisional explicitly or inherently discloses the elements of the claims. To determine whether the provisional inherently discloses an element, I considered whether any element not explicitly disclosed would be necessarily comprehended in the description provided by a Skilled Artisan. I conclude that certain elements of some claims are not adequately disclosed in the provisional.

1. Unsupported Negative Limitation

44. Each independent claim of the 595 Patent requires the negative limitation that the memory controller not access the module for memory read and write operations in a recited training mode (in some claims referred to as the “second mode”). *E.g.*, EX1001, 14:63-65 (claim 1: “wherein the memory module

in the second mode is not accessed by the memory controller for normal memory read or write operations”), *see also id.*, 16:14-22 (claim 10: “wherein the memory module is operable in at least ... a second mode in which the memory module is not accessed by the memory controller for memory read or write operations”), 17:41-44 (claim 17: “performing operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations”), 18:42-46 (claim 21: “wherein the memory module is configurable to perform operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations”).

45. The provisional says nothing about the memory controller not accessing the module for read and write operations in a training mode. Indeed, it mentions the word “training” in only one sentence fragment in a legend to a figure, never explains that such training may occur in its own mode, never uses the word “mode” at all, and never says anything about what operations may or may not occur in the training mode. Moreover, it does say: “This method allows the MCH to execute independent commands while it is waiting for a notification signaling for the memory subsystem controller.” EX1008, 22. If anything, this suggests read and write operations very much may be occurring during the disclosed “MB training.”

46. My opinion is that the negative limitation is not “necessarily comprehended” in the provisional’s disclosure. The 595 Patent itself states that both system memory controller memory operations and training sequences can occur during an initialization mode, confirming that both can occur during the same mode. EX1001, 6:26-30, 6:45-56

47. As noted above, the provisional uses the word “training” in only one sentence fragment, as follows: “Error-Out pin: Low during MB training (high signal indicates that training is done).” EX1008, 25 (Fig. 3 description). To the extent a Skilled Artisan would understand “MB training” as anything more than a generic reference to “training” in the context of memory buffers (and that is all I believe a Skilled Artisan would understand), a Skilled Artisan would, at most, understand “MB training” in this context (where the provisional refers to the then current LRDIMMs under development/ standardization, DDR3 LRDIMM) to refer to training of interfaces to/from and/or operations of a Memory Buffer – a type of register/buffer in DDR3 LRDIMMs that buffered both address and data signals. EX1036, 4 (“Product Description”).

48. It was well-known, however, that some types of memory buffers employed normal memory read and write operations instituted by the system memory controller during the training mode. For instance, JEDEC, a ballot on a draft DDR3 LRDIMM standard discloses training modes for the MB that both

employ normal memory read and write operations instituted by the system memory controller during the training mode and do not. EX1015, 8-9 (“Host-MB Training” employing normal memory read and write operations), 8 (“MB-DRAM Training” not employing normal memory read or write operations); *see also* EX1039, 7-9, 11 (presentation dated June 4, 2009 disclosing “Host-MB Training” and “MB-DRAM Training” before June 12, 2009 provisional filing date); *see also* EX1046, 1-2, 21 (June 4, 2009 meeting minutes noting EX1045 presentation discussed). I note that, in MB-DRAM Training, at least one JEDEC document (EX1039, 7-9) at the time suggests the memory buffer performs operations such as pre-charge, but those would not be considered “memory read or write operations” (or “normal memory read or write operations”) per the claims because they are not performed by the system memory controller (rather the memory buffer performed them). As another example, Talbot discloses that during normal operations normal read and writes are stored in FIFO 220 in the buffer, and are then passed on to DRAM. EX1022, ¶¶ [0039], [0043]. Additionally, during training, the controller may write data, which is also stored in FIFO 220; however, in this case, the data is not passed to DRAM. EX1022, ¶[0053]. Based on this disclosure a Skilled Artisan would conclude that the memory controller is using the same normal write operation in both modes.

2. “One or More” Training “Sequences”

49. Each independent claim of the 595 Patent requires the ability to “perform operations related to one or more training sequences.” *E.g.*, EX1001, 14:65-67 (claim 1: “wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences”), *see also id.*, 16:22-25 (claim 10), 17:41-42 (claim 17), 18:42-43 (claim 21).

50. The provisional, however, only discloses a single “MB training”, that a Skilled Artisan would understand as a generic disclosure of “training” a memory buffer in some way. It does not disclose any training “sequences,” and particularly not “one or more” training sequences. Indeed, the phrases “train sequence” and “training sequences” are completely absent from the provisional. A Skilled Artisan would not “necessarily comprehend” “one or more training sequences” from the bare disclosure of “MB training” as of June 12, 2009.

3. “one or more N-bit-wide data signals”

51. Claim 21 requires “wherein the dynamic random access memory elements are configurable to communicate one or more N-bit-wide data signals with the memory controller via the first edge connections in response to the set of address and control signals, where N is at least 32.” EX1001, 18:31-35. However, dynamic random access memory or DRAM is mentioned just once in the provisional, in the following sentence: “This method allows the MCH to work

with a non-homogenous memory subsystem, such as mixing of DIMMs with different DIMM density, ranks, DRAM density, speed, DRAM configuration, etc.”

EX1008, 23. And the terms “data signal,” “bit,” “width,” and “32” are found nowhere in the provisional, much less the concept of data signals of a certain width, particularly “at least 32.” There is no support for this limitation of this claim in the provisional. Nor would a Skilled Artisan “necessarily comprehend” such a disclosure from what is included in the provisional.

4. “one or more pins that are not active”

52. Claims 8, 15, 16, 18, and 19 require that “the second edge connections include one or more pins that are not active while the memory module is in the second mode,” or a substantially similar “not active” limitation. EX1001, 15:51-53; *see also id.* at 17:7-13 (claims 15-16), 17:49-56 (claims 18-19). However, the terms “edge,” “edge connection[s],” “mode” and “active” appear nowhere in the provisional, much less the concept that certain pins on an edge connection are not active during certain modes. There is simply no support whatsoever for these claims in the provisional. Nor would a Skilled Artisan “necessarily comprehend” such a disclosure from what is included in the provisional.

B. Person Of Ordinary Skill in the Art

53. Based on my experience and the prior art I discuss herein, I believe a person of ordinary skill in the art in the field of the 595 Patent would be someone

who was familiar with computer memory systems and basic CPU architecture documented in the computer/memory architecture literature and generally available in commercial systems as of 2009-10. Such literature and commercial systems would have included techniques related to how computer components access a computer's memory, including the role of a memory controller, the basic operation of memory modules and devices, and the techniques used to couple memory devices to the other components of the computer system. They would also include schemes for initialization of computer systems, including initialization/training of memory components. Such a person would also have been familiar with the standards that govern the operation of memory devices. The person of ordinary skill in the art would have had a bachelor's degree in computer engineering, or a related field, and several years of additional experience working with computer memory systems. Alternatively, such a person could have had equivalent combinations with more or less education and less or more experience.

C. Overview of The 595 Patent

54. The 595 Patent states that it describes “a method of establishing a handshake mechanism based on notification signaling.” EX1001, 4:5-7. The 595 Patent explains that “this [handshake] mechanism can be implemented by adding a new interface (notifying) signal between the MCH [i.e., system memory controller] and the memory subsystem controller, or by adding an additional functionality to

an existing, non-timing critical signal without altering the memory subsystem hardware.” EX1001, 4:7-12. The 595 Patent further explains that this interface “can be an open drain signaling from the memory subsystem controller to the MCH [i.e., system memory controller].” EX 1001, 4:12-16.

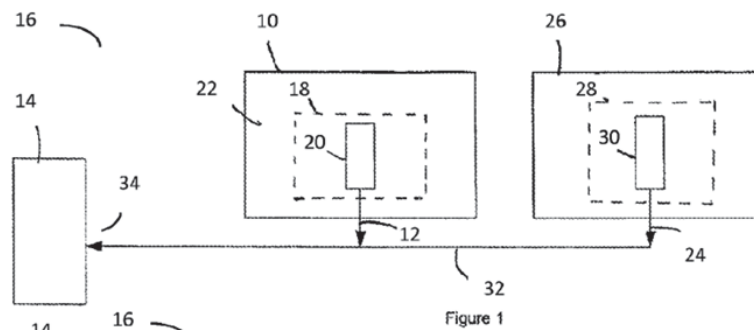
55. According to the 595 Patent, before the patent “[i]n general, there [was] *no existing method of handshaking* between the MCH (*e.g.*, system memory controller) and a memory subsystem (*e.g.*, memory module) during initialization.” Ex. 1001 (595 Patent) at 2:64-67 (emphasis added). The patent states that “in conventional systems, the system memory controller does not monitor the error-out signal from the memory subsystem.” *Id.* at 2:67-3:2. The 595 Patent states that “typical” servers of the prior art would instead, after commencing an initialization function in a memory module, simply wait a predetermined amount of time and then assume the memory subsystem had completed initialization. EX1001, 3:3-22.

56. The 595 Patent suggests that use of “handshaking” between memory controller and memory module (i.e., exchanging information about the completion of the initialization procedure) would be a better idea. EX1001, 2:58-63. It states that, generally, “handshaking can be implemented in at least two ways; polling and notifying.” EX1001, 3:43-44. The 595 Patent claims that polling is “generally inefficient because the system memory controller does not know exactly when the memory subsystem will have completed the required or requested operation,” thus

causing the controller to “wait longer than necessary to poll the memory subsystem, thereby delaying the overall initialization process.” EX1001, 3:48-54.

It further states that “the notifying method is an advantageous handshaking method between the MCH and the memory subsystem controller.” EX1001, 3:63-65.

57. The 595 Patent provides only limited detail on what it purports to be the inventive system. Figure 1, for example (below), depicts an embodiment. That figure shows a computer system including memory module 10 coupled to a memory controller 14 via “output 12” which is driven by notification circuit 20 of controller circuit 18.



Ex. 1001 (595 Patent) at 4:24-42, FIG. 1. Memory module 26 is also shown, and has essentially in the same structure as module 14, having “output 24” driven by notification circuit 30 of controller circuit 28. *Id.* at 6:23-44.

58. In one specific example of handshaking described in the 595 Patent, the interface between the memory controller (MCH) and memory subsystem controller (of the memory module) is implemented using a technique called open

drain signaling. EX1001, 4:12-16; *see also id.* at 9:47-53, FIGs. 2-3. Specifically, output 12 of module 10 and output 24 of module 26 are both tied to the same bus 32 using an open drain configured transistor. Ex. 1001 (595 Patent) at 4:12-23, 9:51-67, FIGs. 2-3.

59. In that configuration, when starting an initialization procedure, each memory module will drive high the gate of the transistor with the open drain output, placing a logic level low (low impedance) signal on bus 32. When the initialization is complete, the memory module can drive low the gate of the transistor with the open drain output, placing a logic level high (high impedance) signal on bus 32. However, because all of the outputs of multiple memory modules are tied to the same bus 32 in an open drain configuration, the state of bus 32 will remain logic level low (low impedance) until each memory module drives low the gate of the transistor of its open drain output, placing a logic level high (high impedance) on its output, which then allows “the bus 32 [to] be pulled high by the internal pull-up configuration 40 of the system memory controller 14.” Ex. 1001 (595 Patent) at 9:47-10:50. In this manner, the system memory controller may be provided the status of an initialization procedure (*e.g.*, either that it is currently executing or complete) using only a single bus line from multiple memory modules. *Id.* The 595 Patent further states that bus 32 could be tied to a

standard-defined (such as JEDEC) error output pin that is not required by the standard to be used during initialization. EX1001, 8:4-33.

60. The patent further states that output 12 can be operatively coupled to the error-out pin of the memory module 10, which is connected to a multiplexor 42 driving the transistor 36 with either of a task_in_progress signal 44 or an error signal 46 (*e.g.*, parity error signal). Ex. 1001 (595 Patent) at 11:19-23, FIG. 3. According to the 595 Patent, “the memory module 10 can be advantageously configured to both perform the standard (*e.g.*, JEDEC-specified) error reporting functionality via the error-out pin during the operational mode and provide the status notification functionality during the system initialization mode.” Ex. 1001 (595 Patent) at 11:29-34.

D. The Prosecution History of The 595 Patent

1. 553 Application (The 595 Patent)

61. The 595 Patent issued from U.S. Patent Application Serial No. 15/857,553 (“553 Application”), which is a continuation of U.S. Patent Application Serial No. 15/088,115 (“115 Application”), filed on April 1, 2016, now U.S. Patent No. 9,858,218 (“218 Patent”), which is a continuation of U.S. Patent Application Serial No. 13/942,721 (“721 Application”), filed on July 16, 2013, now U.S. Patent No. 9,311,116, which is a continuation of U.S. Patent Application Serial No. 12/815,339 (“339 Application”), filed on June 14, 2010,

Declaration of Dr. Donald Alpert Regarding U.S. Patent No. 10,474,595

which is now U.S. Patent No. 8,489,837 (“837 Patent”), which in turn claims priority to U.S. Provisional Application 61/186,799 filed June 12, 2009. Ex. 1001 (595 Patent) at 1-2.

62. The 553 Application presented 7 claims. Ex. 1002 (595 Patent File History) at 32-33. On August 28, 2018, the examiner rejected claims 1-7 on the ground of “nonstatutory double patenting as being unpatentable over claims 1-18 of U.S. Patent No. 8489837; claims 1-20 of U.S. Patent No. 9311116; and claims 1-22 of U.S. Patent No. 9858218.” Ex. 1002 (595 Patent File History) at 83. The examiner found:

Although the claims at issue are not identical, they are not patentably distinct from each other because the pending claims make obvious the claims of the issued patents and vice versa.

EX1002, 83, ¶3.

63. In response, the applicants of the 553 Application filed a terminal disclaimer on November 28, 2018. Ex. 1002 (595 Patent File History) at 106-107. The applicants further amended claims 4, 5, and 7 and added claims 8-20. Ex. 1002 (595 Patent File History) at 104.

64. On February 6, 2019, the examiner issued a notice of allowance. Ex. 1002 (595 Patent File History) at 121-122.

65. On March 1, 2019, the applicants of the 553 Application filed a Request for Continued Examination along with an Amendment. Ex. 1002 (595

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Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1003, p. 25

Patent File History) at 145-154. In the Amendment, the applicants amended the claims to remove the term “handshake” from all claims and add other terms. *See, e.g.*, Ex. 1002 (595 Patent File History) at 149, 151.

66. On March 21, 2019, The Board’s final decision in IPR2018-00303 was disclosed in a filed IDS. EX1002, 175.

67. On March 29, 2019, the examiner issued a second notice of allowance. EX1002, 182-183. The Examiner did not cite the March 21 IDS, citing, instead, a March 1 IDS. EX1002, 186. Similarly, the list of references considered by the examiner issued with that Notice of Allowance does not list the final written decision in IPR2018-00303. *See id.*, 194-201

68. On July 1, 2019, the applicants of the 553 Application filed another Request for Continued Examination along with an Amendment. Ex. 1002 (595 Patent File History) at 222-233. In the Amendment, the applicants amended claims 1, 3-8, 10, 12-15, 17-18, 20, and added new claims 21-24. *Id.* at 224-233.

69. On August 9, 2019, the examiner issued a third notice of allowance. EX1002, 243-244.

70. On September 15, 2019, the Examiner filed an IDS with a list of references considered, including, for the first time, the final decision in IPR2018-00303. EX1002, 265.

2. 115 Application (The 218 Patent)

71. The 218 Patent issued from the 115 Application. The 115 Application presented 20 claims, 1-20. Ex. 1005 (115 Application File History) at 30-33 (Application at 20-23). On May 20, 2016, the examiner rejected claims 1-20 on the ground of nonstatutory double patenting as being unpatentable over claims 1-20 of U.S. Patent No. 9,311,116 and claims 1-18 of U.S. Patent No. 8,489,837. Ex. 1005 (115 Application File History) at 49-57. Claims 1-20 were rejected also under 35 U.S.C. 103(a) as being unpatentable over Tanguay (Ex. 1009, US 2010/0042778) in view of Roohparvar (Ex. 1010, US 2003/0115427). *Id.*

72. In response, the applicants of the 115 Application cancelled claims 1-20, and added new claims 21-42. Ex. 1005 at 68-81. The applicants also filed a terminal disclaimer to overcome the nonstatutory double patenting rejections. *Id.*

73. On November 25, 2016, the examiner rejected claims 21-42 as being unpatentable over Moshayedi (Ex. 1011, U.S. 2010/0202240) in view of Fahr (Ex. 1012, U.S. 2008/0256281). Ex. 1005 (115 Application File History) at 100-107.

74. On April 25, 2017, the applicants of the 115 Application filed a Response. Ex. 1005 (115 Application File History) at 132-144. In the Response, the applicants amended claims 21 and 35 to “address issues with antecedent basis and for better clarity.” *Id.* at 138.

75. The applicants further argued that the Applicant is left to guess what the Examiner's rationale is in rejecting the claims under Moshayedi in view of Fahr, because Moshayedi shows several outputs including "CACHE_DIRTY, DRAM_AVAILABLE, NVDIMM_READY, TEST_TX, and VBACK_RESET," that cannot be "an open drain output" outputting "a signal indicating a parity error." Ex. 1005 at 139-141. The applicants further argue that Moshayedi fails to disclose "configured to receive from the memory controller via the second edge connections address and command signals associated with one or more memory read, write, pre-charge, or refresh operations and to control the memory elements in accordance with the address and command signals," *id.* at 142, and "wherein the module controller is further configured to process one or more training sequences unrelated to any memory read, write, pre-charge, or refresh operation, and wherein the module controller is further configured to drive a notification signal associated with the one or more training sequences to the memory controller via the open drain output of the module controller and the error edge connection." *Id.* at 143.

76. The applicants further argued that Fahr does not make up for the deficiency of Moshayedi, because the Fahr describes "two open-drain outputs for two different error signals, /Error (CE) 120 and /Error (UE) 121, respectively," while the claim requires "that the module controller 'outputs to the memory controller a signal indicating a parity error' AND 'is further configured to drive a

notification signal associated with the one or more training sequences to the memory controller’ **via the same open-drain output.**” Ex. 1005 (115 Application File History) at 143. (emphasis in original).

77. On May 25, 2017, the applicants of the 115 Application further filed an Amendment, amending claims 21, 22, 28-29, 34-36, and 42, responding to the Final Office Action dated November 25, 2016. Ex. 1005 (115 Application File History) at 167-179. In this Amendment, the applicants made similar arguments as in its April 25, 2017 Response. *Id.*

78. On May 31, 2017, the applicants of the 115 Application conducted an interview with the Examiner, discussing “the AFCP 2.0 filed 04/25/17 and potential claim amendments to overcome the art of record.” Ex. 1005 (115 Application File History) at 182.

79. On June 16, 2017, the examiner rejected claims 21-42. Ex. 1005 (115 Application File History) at 184-191. In particular, the examiner rejected claims 21-42 under 35 U.S.C. 112(a), as failing to comply with the written description requirement, because the newly added limitations to claims 21, 29, and 35 (*i.e.*, “‘wherein the one or more training sequences are not associated with any memory read or write operation,’ ‘while the memory module is not performing any memory read or write operation,’ ‘while the memory module is not performing any memory read or write operation,’” respectively”) are not supported by the original

disclosure and constitute new matter. Ex. 1005 (115 Application File History) at 186-187. The examiner further rejected claims 21-42 as being unpatentable over Moshayedi (Ex. 1011, U.S. 2010/0202240) in view of Fahr (Ex. 1012, U.S. 2008/0256281) and Goishi (Ex. 1013, U.S. 2010/0142383). Ex. 1005 (115 Application File History) at 188-190.

80. On July 14, 2017, the applicants of the 115 Application conducted an interview with the Examiner, discussing “the rejection of claims 21-42 under 35 USC 112 first paragraph and 35 USC 103 over Moshayedi (20100202240), Fahr (20080256281), and Goishi (20100142383), as well as potential claim amendments to overcome the pending rejections.” Ex. 1005 (115 Application File History) at 201.

81. On September 18, 2017, the applicants of the 115 Application filed an Amendment, amending claims 21, 27-29, 33-35, and 41-42, responding to the Non-Final Office Action dated June 16, 2017. Ex. 1005 (115 Application File History) at 203-216. In this Amendment, the applicants made similar arguments as in its April 25, 2017 Response with respect to Mosheyedi and Fahr. Ex. 1005 (115 Application File History) at 210-216. The applicants further argued that Goishi does not make up for the deficiencies of Moshayedi and Fahr without any substance. Ex. 1005 (115 Application File History) at 216.

82. On October 12, 2017, the examiner issued a notice of allowance, allowing claims 21-42 of the 115 Application. Ex. 1005 (115 Application File History) at 228-232.

3. 745 Application (The 623 Patent)

83. The 623 Patent issued from U.S. Patent Application 15/169,745. The 745 application presented 37 claims. The 745 application was accorded a filing date of June 6, 2016.

84. On July 29, 2016, the claims were rejected “on the ground of nonstatutory double patenting as being unpatentable over claims 1-20” of the 116 Patent, requiring Patent Owner to file a terminal disclaimer to overcome the rejection:

Although the claims at issue are not identical, they are not patentably distinct from each other because the claims ... make obvious the claims of the issued patent and vice versa.

EX1038, 57, ¶3. Patent Owner likewise had to file a terminal disclaimer over the 837 Patent when prosecuting the application that became the 623 Patent. EX1038, 79 (disclaiming over application that issued as ‘218 patent, which disclaims over the ‘837 patent); EX1005, 61.

4. 721 Application (The 116 Patent)

85. The 116 Patent issued from the 721 Application. The 721 Application presented 15 claims, 1-15 (Application at 21-23) Ex. 1006 (721 Application File History) at 27-29.

86. On August 5, 2014, the applicants of the 721 Application filed a Preliminary Amendment amending claims 1 and 11-15, canceling claims 4 and 8-10, and adding new claims 16-24. Ex. 1006 (721 Application File History) at 54-60.

87. On May 22, 2015, the examiner rejected claims 1-7 and 11-24 on the ground of nonstatutory double patenting as being unpatentable over claims 1-18 of U.S. Patent No. 8,489,837 (Ex. 1019). Ex. 1006 (721 Application File History) at 64-69.

88. On August 24, 2015, the applicants of the 721 Application filed a terminal disclaimer to overcome the double patenting rejection. Ex. 1006 (721 Application File History) at 74-80, 86.

89. On November 16, 2015, the examiner issued a Final Office Action maintaining the double patenting rejection noting that “the person who signed the terminal disclaimer is not an attorney or agent of record, is not recognized as an officer of the assignee, and has not been established as being authorized to act on behalf of the assignee.” Ex. 1006 (721 Application File History) at 92.

90. On January 21, 2016, the applicants of the 721 Application filed a “properly signed terminal disclaimer” to overcome the double patenting rejection. Ex. 1006 (721 Application File History) at 97, 99-104.

91. On February 24, 2016, the examiner issued a Notice of Allowance, allowing claims 1-3, 5-7, and 11-24 of the 721 Application. Ex. 1006 (721 Application File History) at 115-119.

5. 339 Application (The 837 Patent)

92. The 623 Patent issued from the 339 Application. The 339 Application presented 20 claims, 1-20. Ex. 1007 (339 Application File History) at 28-31. On September 14, 2012, the examiner rejected claims 1-3, 5, 7, 11, 14, and 19, and allowed claims 4, 6, 8-10, 12, 13, 15-18, and 20. Claims 5 and 11 were rejected under 35 U.S.C. 112, first paragraph. Ex. 1007 (339 Application File History) at 60-61. Claims 1-3, 5, 7, 11, 14, and 19 were rejected under 35 U.S.C. 103(a) as being unpatentable over Tanguay (Ex. 1009, US 2010/0042778) in view of Roohparvar (Ex. 1010, US 2003/0115427). Ex. 1007 (339 Application File History) at 61-67.

93. In response, the applicants of the 339 Application noted that the examiner’s 112 rejection must have referred to claims 5 and 14 not 5 and 11, and cancelled claims 5 and 14. EX1007, 90.

94. The applicants of the 339 Application also amended claims 1, 4, 11, and 19. Claim 1 was amended to add “wherein the at least one notification signal triggers the memory controller to execute an interrupt routine,” claim 4 was amended to remove “and the memory controller is responsive the at least one notification signal indicating completion of the at least one initialization sequence by triggering execution of an interrupt routine by the memory controller.” Ex. 1007 at 85. According to the applicants, the amendment to claim 1 rendered claims 1-3 patentable over Tanguay in view of Roohparvar. EX1007, 91.

95. On April 29, 2013, the examiner issued a notice of allowance, allowing claims 1-4, 6-13, and 15-20 of the 339 Application. EX1007, 121.

6. IPR2018-00303

96. U.S. Patent No. 9,535,623 (“623 Patent”) is related to the 595 Patent. Both the 623 Patent and the 595 Patent claims priority to and share the specification of the same parents (*e.g.*, 218 Patent and 837 Patent). The claims of both 595 Patent and 623 Patent are strikingly similar. Just by way of example, claim 1 of both patents arise directed to a memory module on a printed circuit board having various edge connections, including an error edge connection. Ex. 1001 at claim 1; Ex. 1031 at claim 1. Both require that the module operate in two modes, one for normal operation and one for training. *Id.* And both require an

open drain output that is used both for parity error during normal operation and for a notification signal during training. *Id.*

97. SK hynix filed a petition for inter partes review of the 623 Patent based primarily on US Patent Publication 2008/0098277, dated April 24, 2008 (“Hazelzet”) combined separately with several different references, most important for purposes of my analysis here US Patent 8,139,430, issued March 20, 2012 (“Buchmann”). Ex. 1032 (623 IPR Petition) at 61-67.

98. SK hynix’s petition also relied on my analysis and testimony concerning the obvious combination of Hazelzet and Buchman. In particular, I demonstrated in my direct testimony that Hazelzet, Buchmann and the 623 Patent were analogous art, Ex. 1033 (623 Patent IPR Declaration) at ¶172, and that Hazelzet and Buchman could be combined such that the same open drain output of Hazelzet could be used for a parity error signal during normal operations, as disclosed in Hazelzet, and also for a training sequence notification signal, such as “TS0_done,” “TS3_ack,” and “TS3_done,” as disclosed in Buchmann, Ex. 1033 (623 Patent IPR Declaration) at ¶¶167, 170; *see also id.* at ¶¶164-174.

99. I further demonstrated that a person of ordinary skill in the art would have been motivated to make this combination because, among other things, it would have improved overall system reliability, EX1033, ¶173, would have complemented Hazelzet’s existing initialization sequence, *id.* at ¶174, and “would

have been merely a use of prior art techniques for prior art purposes with only expected results,” *id.* at ¶175.

100. The Board issued a Final Written Decision in IPR2018-00303 on March 21, 2019, finding all claims of the 623 Patent unpatentable based on, among other grounds, the obvious combination of Hazelzet and Buchmann. Ex. 1034 (623 Patent IPR, Final Written Decision) at 21. In coming to that conclusion, the Board stated that “we agree with Petitioner’s showing that the combination of Hazelzet and any one of Buchmann or Talbot teaches every limitation of claims 1, 12, and 21 of the ’623 patent and that a person of ordinary skill in the art would have had reason, with rational underpinning, to combine the references.” Ex. 1034 (623 Patent IPR, Final Written Decision) at 13. In support of that conclusion, the Board stated “[f]urther, we credit Dr. Alpert’s supporting testimony (Ex. 1003 ¶¶ 121–150, 158–186), as it is consistent with the prior art disclosures.” Ex. 1034 (623 Patent IPR, Final Written Decision) at 13.

101. The Board’s Final Written Decision in IPR2018-00303 was provided to the examiner of the 595 Patent, and the examiner indicated that the Final Written Decision was considered. Ex. 1002 (595 Patent File History) at 265. However, no analysis or comments were made by the examiner explaining why the examiner departed from the Board’s conclusion.

102. I have been asked to consider whether the examiner erred in a manner material to the patentability of claims challenged here. In my opinion, the examiner of the 595 Patent erred in permitting the 595 Patent to issue. In particular, the examiner failed to give any reason why he departed from the Board's conclusion that the 623 Patent claims were obvious in view of Hazelzet and Buchmann, as explained in the Final Written Decision of IPR2018-00303. This is remarkable, given that the claims of both 595 Patent and 623 Patent are strikingly similar. The only arguable distinction is that the 623 Patent requires "a notification signal indicating ... status of one or more training sequences" while the 595 Patent requires "information related to one or more training sequences." Ex. 1001 at claim 1; Ex. 1031 at claim 1. However, that distinction cannot justify the examiner's decision to allow the 595 Patent, because "*a notification signal indicating ... status of one or more training sequences*" is within the scope of "*information related to one or more training sequences.*"

103. Below, in § V, I repeat my analysis demonstrating that a Skilled Artisan would have found the combination of Hazelzet and Buchmann to be obvious, and motivated by the prior art knowledge of such a person, as evidence by numerous exhibits not discussed by the examiner of the 595 Patent. I also point out that the Board has already found such evidence to be credible during the IPR on the 623 Patent.

E. Challenged Claims of the 595 Patent

104. This declaration relates to claims 1-24 of the 595 Patent. Those claims read as follows:

Claim	Claim Language
1.a	1. A memory module operable with a memory controller of a host system, comprising:
1.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;
1.c	dynamic random access memory elements on the printed circuit board;
1.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection; and

Claim	Claim Language
1.e	[i] wherein the memory module is configurable to operate in any of at least a first mode and a second mode; [ii] wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, [iii] wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and [iv] wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences;
1.f	[i] wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, [ii] wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller

Claim	Claim Language
	via the first edge connections in accordance with the address and control signals, and [iii] wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode;
1.g	wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.
2	2. The memory module of claim 1, wherein the module controller comprises an integrated circuit.
3	3. The memory module of claim 1, wherein the module controller includes a notification circuit comprising a transistor having an open drain coupled to the open drain output and source coupled to the ground.

Claim	Claim Language
4	4. The memory module of claim 3, wherein the module controller is configurable to drive a gate of the transistor high so as to drive open drain output and the error edge connection to ground, or to drive the gate of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state.
5	5. The memory module of claim 4, wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground.
6	6. The memory module of claim 3, wherein the notification circuit further includes a multiplexor or a logic circuit having a output coupled to a gate of the transistor and configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.
7	7. The memory module of claim 3, wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state.

Claim	Claim Language
8	8. The memory module of claim 1, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.
9	9. The memory module of claim 1, wherein the memory module in the second mode is configurable to perform the operations related to the one or more training sequences without communicating data signals via the first edge connections while the memory module is in the second mode.
10.a	10. A memory module operable with a memory controller of a host system, comprising:
10.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections;

Claim	Claim Language
10.c	dynamic random access memory elements on the printed circuit board;
10.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state; and
10.e	wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections;

Claim	Claim Language
10.f	wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode;
10.g	wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode.
11	11. The memory module of claim 10, wherein the module controller comprises an integrated circuit.
12.a	12. The memory module of claim 10, wherein the module controller includes a notification circuit having a transistor with an

Claim	Claim Language
	open drain coupled to the open drain output and a source coupled to the ground,
12.b	wherein the module controller is configurable to output to the memory controller the open-drain signals related to the one or more training sequences by driving a gate of the transistor high so as to drive the open drain output and the error edge connection to ground, and by driving the gate of the transistor low as to drive the open drain output and the error edge connection to the high impedance state,
12.c	and wherein the notification circuit is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground.
13	13. The memory module of claim 12, wherein the notification circuit further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor and configurable to drive the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.

Claim	Claim Language
14	14. The memory module of claim 10, wherein the module controller is configurable to output the open-drain signals related to the one or more training sequences by driving the open drain output from the high impedance state to the low logic level or from the low logic level to the high impedance state.
15	15. The memory module of claim 10, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.
16	16. The memory module of claim 10, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is in the second mode.
17.a	17. A method, comprising:
17.b	at a memory module coupled with a memory controller of a host system, the memory module including a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge

Claim	Claim Language
	connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections, the memory module further including dynamic random access memory elements on the printed circuit board;
17.c	receiving via the second edge connections address and control signals associated with one or more memory read or write operations; controlling the dynamic random access memory elements to communicate data signals corresponding to the one or more memory read or write operations via the first edge connections in response to the address and control signals; outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is being accessed by the memory controller for a memory read or write operation;
17.d	performing operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and outputting to the memory

Claim	Claim Language
	controller via the open drain output and the error edge connection open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation.
18	18. The method of claim 17, wherein the second edge connections include one or more pins that are not active while the memory module is trained with the one or more training sequences.
19	19. The method of claim 18, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is trained with the one or more training sequences.
20.a	20. The method of claim 17, wherein the memory module includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to ground,
20.b	wherein outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module comprises driving a gate of the transistor high to provide a low impedance path between the open drain output and ground, and

Claim	Claim Language
20.c	wherein outputting the open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation comprises driving the gate of the transistor to drive the open drain output from a high impedance state to ground and from ground to the high impedance state.
21.a	21. A memory module operable with a memory controller of a host system, comprising:
21.b	a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections;
21.c	dynamic random access memory elements on the printed circuit board; and
21.d	a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller including a transistor having a gate and an open drain output coupled to the error edge connection; wherein the module controller is

Claim	Claim Language
	configurable to drive the gate of the transistor so as to drive the open drain output to a first state or a second state, the first state being a low logic level and the second state being a high impedance state;
21.e	[i] wherein the module controller is configurable to receive via the second edge connections memory commands associated with normal memory read or write operations and to output a set of address and control signals for each of the normal memory read or write operations; [ii] wherein the dynamic random access memory elements are configurable to communicate one or more N-bit-wide data signals with the memory controller via the first edge connections in response to the set of address and control signals, where N is at least 32; [iii] wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred during any of the memory read or write operations by driving the open drain output and the error edge connection to the first state;
21.f	wherein the memory module is configurable to perform operations related to one or more training sequences while the memory

Claim	Claim Language
	module is not accessed by the memory controller for memory read or write operations; and wherein the module controller is configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection from one of the first state and the second state to the other one of the first state and the second state.
22	22. The memory module of claim 21, wherein the module controller further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor, and wherein the module controller is configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.
23.a	23. The memory module of claim 22, wherein the transistor has a source coupled to ground,
23.b	wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground, and

Claim	Claim Language
23.c	wherein the module controller is configurable to provide the information related to the one or more training sequences by driving the open drain output from a high impedance state to ground or from ground to the high impedance state.
24	24. The memory module of claim 21, wherein the memory module is configurable to perform the operations related to the one or more training sequences while the memory module is not communicating signals via the first edge connections.

F. Construction of Terms Used in the 595 Patent Claims

105. I understand that claim terms should be given their ordinary and accustomed meaning as understood by one of ordinary skill in the art in view of the patent and its file history. As detailed in my analysis and set forth below, I have used what I believe to be the ordinary and accustomed meaning of the claim terms as understood by one of ordinary skill in the art in view of the 595 Patent and its file history.

1. “memory read or write operations”

106. It is my opinion that a Skilled Artisan would understand the ordinary meaning of “*memory read and write operations*” to be operations used to communicate data between the memory module and the memory controller in response to commands from the memory controller.

107. In the claims, “*memory read and write operations*” refers to operations used to read or write DRAMs in response to address and control signals received from the system memory controller. EX1001, 16:26-33. For example, claim 10 requires:

the module controller in the first mode is configurable to receive via the second edge connections the **address and control signals** associated with the **one or more memory read or write operations**, wherein the dynamic random access memory elements are configurable to communicate data signals with **the memory controller** via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode

EX1001, 26-38. (emphasis added).

108. Similarly, the 595 Patent specification explains that “[d]uring the read/write operations, the memory module **communicates data** with the memory

controller via the data signal pins **in response to second memory commands received via the address and control signal pins.** EX1001, 1:57-61. (emphasis added).

109. Thus, during read/write operations, the module controller will transmit the command and address signals received from the system memory controller to the memory devices. EX1001, 5:45-52 (“For example, the controller circuit 18 may receive and process address and command signals (*e.g.*, read, write commands) from the system memory controller 14 and transmit appropriate address and commands to the memory elements in response”). (emphasis added). The intrinsic record therefore confirms that “*memory read and write operations*” refers to operations used to communicate data between the memory module and the memory controller in response to commands from the memory controller.

2. **“normal memory read and write operations”**

110. It is my opinion that a Skilled Artisan would understand the ordinary meaning of “*normal memory read and write operations*” to be the same as “*memory read and write operations.*”

111. The original application from which the 595 Patent issued does not use the phrase “normal.” Nevertheless, the original claims consistently used the phrase “*memory read and write operations.*” On July 2019, the Abstract and some

of the pending claims where amended to include “normal memory read and write operations.” EX1002, 224, 240.

wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and ~~control~~ ~~command~~ signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is ~~configurable to undergo training with~~ configurable to perform operations related to one or more training sequences ~~while the first edge connections are not active;~~

wherein the module controller is configurable to receive via the second edge connections the address and ~~command~~ ~~control~~ signals associated with the one or more normal memory read or write operations ~~and to control,~~ wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge

EX1002, 224 (annotated).

112. When making these amendments, the patent applicant explained that “[n]o new matter has been added.” *id.*, 233.

Support for the amendments can be found throughout the specification and drawings of the application as filed (e.g., paragraphs [0016], [0018], [0019], [0035]-[0037], and [0040]). No new matter has been added.

EX1002, 233 (annotated). (emphasis added).

113. Alternatively, “normal memory read and write operations” should be construed to mean standard operations used by the memory controller to read from or write to memory devices, whether or not they occur in a normal operating mode of a module. For example, the patent states:

For example, the system memory controller 14 may cause the memory module 10 to perform **standard operations such as memory**

read/write, pre-charge, refresh, etc., while in operational mode, although it will be appreciated that one or more of **these operations** **can** also be performed by the memory module 10 while **in initialization mode** in certain embodiments.

EX1001, 6:50-56. (emphasis added).

114. This passage is part of the patent’s description of a “normal” “operational mode.” EX1001, 6:45-50. It explains that “the **normal** mode of the memory module 10 ... [during which] ... the memory module 10 is generally accessed by the system memory controller 14 of the host computer 16 during standard computer operation not associated with initialization.” EX1001, 6:45-50. (emphasis added).

115. Thus, the specification includes an example of memory read and write operations used by the system memory controller to read from or write to memory devices during standard computer operation. However, this part of the specification also explains that “it will be appreciated that **one or more of these operations** can also be **performed** by the memory module 10 while **in initialization mode.**” EX1001, 6:53-56. (emphasis added). The 595 Patent therefore states that the disclosed standard memory operations can also be used in non-normal modes, for example, during initialization.

116. As another example, claim limitation [1.e.ii] requires that “normal memory read or write operations” occur in the “first mode,” while claim limitation

[1.e.iii] requires that “normal memory read or write operations” not occur in the “second mode” during which “training sequences” occur. If “normal memory read or write operations” were construed to be limited to memory read or write operations only in the “first” (normal) mode, then limitation [1.e.iii] would be meaningless because by construction “normal memory read or write operations” could never occur in the “second” training mode or any other non-normal mode.

117. Likewise, the prosecution history confirms that “*normal memory read and write operations*” can be used during initialization. The 595 patent claims to be a continuation of U.S. Patent No. 8,489,837 (the “837 Patent”), which was the subject of IPR2017-00548. I understand that the proceedings of that IPR are part of the prosecution history of the 595 Patent and of the intrinsic record for purposes of claim construction. Likewise, the record in IPR2017-00548 was provided to the examiner of the 595 Patent, so it is part of the intrinsic record for that reason as well

118. In IPR2017-00548, Patent Owner’s expert was questioned about the passage block quoted above (EX1001, 6:50-56), which appears in identical form in the 837 Patent. The expert agreed that a Skilled Artisan would have understood the quote to be accurate, EX1021, 24:8-23, and conceded that the referenced memory commands (*i.e.*, the ones that can be used during initialization) would be considered “normal memory commands that a memory controller or processor

would issue to read and write data out into main memory under standard or regular use of a computer[.]” EX1021, 24:24-25:18. The expert also testified that, aside from initialization, “normal read and writes” can be used in other non-normal modes, such as boot-down sequences. EX1021, 17:24-18:11. I agree with these conclusions of Patent Owner’s expert.

119. Thus, the specification and prosecution history of the 595 Patent confirm that “*normal memory read and write operations*” are not limited to operations actually used during standard computer operation or in any particular mode. But that, this phrase should be construed to have the same meaning as “*memory read and write operations*” or, in the alternative, to mean standard operations used to read from or write to memory devices and initiated by the system memory controller, and should explicitly be construed as not limited to occurring only in any normal operating mode of a module.

3. “mode”

120. It is my understanding that a Skilled Artisan would give “mode” it’s plain and ordinary meaning after reviewing the 595 Patent and its prosecution history.

121. The 595 Patent uses the term “mode” in accordance with the plain and ordinary meaning. EX1001, Abstract, 1:43-3:15, 4:29-42, 5:66-6:14, 6:45-6:56. I understand that in the course of IPR2017-00548, Patent Owner sought to have the

term “*mode*” interpreted to mean “a distinct behavioral state that a system may be switched to.” EX1035, 7.

122. In addition, based on the word “distinct” Patent Owner argued that that different “modes” must necessarily include mutually exclusive operations. EX1041, 6. However, this is inconsistent with the disclosure of the 837 Patent, and of the 595 Patent, that the disclosed memory operations may be used in both an operational mode and in an initialization mode. EX1001, 6:50-56.

For example, the system memory controller 14 may cause the memory module 10 to perform standard operations such as memory read/write, pre-charge, refresh, etc., while **in operational mode**, although it will be appreciated that one or more of these operations can also be performed by the memory module 10 while **in initialization mode** in certain embodiments.

EX1001, 6:50-56. (emphasis added).

123. I also understand that in IPR2017-00548 the Board declined to construe the word “*mode*.” EX1035, 7. As the intrinsic record here never defines the term “*mode*” or uses it in any special sense, the Board should take the same approach here.

124. Finally, should a construction be necessary, as I explained in the 623 patent IPR, I agree that the word “state” – when understood without all of the implicit limitations Patent Owner sought to have read into the claims in the 837

Patent IPR – is a synonym for “mode” in the context of the 595 Patent. For instance, a “second mode” in which the module “perform[s] operations related to one or more training sequences” is a “state” of the module in which operations related to one or more training sequences are performed. That word “state” is consistent with the disclosures of the 595 Patent and the dictionary Patent Owner has provided in the IPR for the parent 837 Patent. While Patent Owner’s dictionary uses the phrase “operational state,” Ex. 1047, 3, it is using “operational” more broadly than the 595 Patent, since the patent explicitly equates the disclosed “operational mode” with normal memory operations and the dictionary includes no such limitation. EX1001, 6:45-50; Ex. 1047, 3. Construing “mode” to mean “state” therefore captures the ordinary meaning of “mode” and avoids any confusion from the inconsistent use of the word “operational.” To be clear, I do not believe interpreting “mode” to mean “state” alters the analysis set forth in my declaration, since in my view the two words mean the same thing to a person of skill in the context of the 595 patent.

4. “training sequence”

125. It is my opinion that a Skilled Artisan would understand the ordinary meaning of “*training sequence*” to be a set of operations occurring in a particular order and used for training.

126. Generally, a “sequence” is “a set of related events, movements, or things that follow each other in a particular order.” EX1042, 1.

127. Further, the 595 Patent provides very few details concerning the disclosed “*training sequences*.” What is shown is only that (1) the “*training sequences*” are controlled by the memory module, EX1001, 3:32-35 (“the MCH according to such a scheme may give control to the local memory controller of a memory subsystem (*e.g.*, memory module) for execution of a training sequence.”), (2) that a module may carry out more than one, and (3) that they may be part of an “initialization sequence.” *Id.*, 6:19-23 (“the memory controller 14 issues a first command to the memory module 10, and, in response, the memory module 10 executes an initialization sequence (*e.g.*, one or more training sequences)”).

128. During IPR2018-00303, relating to the 623 Patent (which as noted above shares a specification with the 595 Patent and includes similar claims), the Board found that Buchmann’s TS3 training operations satisfied the “*training sequence*” claimed in the 623 Patent. EX1034, 11-12. The TS3 operations are a set of operations carried out in a particular order to perform upstream lane training and repair. EX1016, 5:40-44. Indeed, Buchmann explicitly describes his different sets of training operations as “training sequences.” EX1016, 3:49-52, 14:38-41.

129. Thus, “*training sequence*” should be construed to mean a set of operations occurring in a particular order and used for training.

IV. OVERVIEW OF THE PRIOR ART

A. Prior Art

1. U.S. Patent Publication No. 2008/0098277 to Hazelzet (Ex. 1014)

130. U.S. Patent Publication No. 2008/0098277 to Hazelzet (“Hazelzet”) (Ex. 1014) was filed on October 23, 2006 and published on April 24, 2008. I understand that Hazelzet is prior art to the 595 Patent. Hazelzet is entitled “High Density High Reliability Memory Module With Power Gating and a Fault Tolerant Address and Command Bus” and discloses such functionality. Ex. 1014 (Hazelzet) at Title.

131. Hazelzet discloses memory modules that can operate in an “ECC mode” or a “parity mode.” Ex. 1014 (Hazelzet) at ¶¶[0064],[0069]-[0070]; *see also id.* at FIG. 8, ¶¶[0020], [0022], [0049], [0059]-[0062], [0072], [0075], [0081], [0101]-[0103], [0106]-[0107], [0109].



FIG. 8

132. Hazelzet explains that the “ECC mode” is a mode that allows the host system to detect and/or correct “correctable errors” or “uncorrectable errors” (*e.g.*, “double bit error”). Ex. 1014 (Hazelzet) at ¶[0069] (“This ECC logic will ... correct all single bit errors and detect all double bit errors present on the twenty-two chip select gated data inputs.”) In the “ECC mode,” the detected correctable errors would be output through an “/Error (CE)” output pin and any uncorrectable errors (*e.g.*, double bit errors) would be reported through an “/Error (UE)” output pin. Ex. 1014 (Hazelzet) at ¶[0069]. Hazelzet explains that these two outputs (*i.e.*, CE and UE) are “open-drain outputs.” Ex. 1014 (Hazelzet) at ¶¶[0072], [0109].

133. Hazelzet further explains that the “parity operating mode” is a mode that allows the host system to “interrogate the device to determine the error

condition” of the memory module. Ex. 1014 (Hazelzet) at ¶[0064] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”).

Hazelzet further explains that such “error condition” in the “parity mode” is also reported to the host “via the Uncorrectable Error (UE) line” when the memory module is in the “parity mode,” Ex. 1014 (Hazelzet) at ¶[0070], which is the open-drain output that is used to report the uncorrectable errors in the “ECC mode.” Ex. 1014 (Hazelzet) at ¶¶[0072], [0109].

134. Hazelzet further explains that its memory module is in the “ECC mode” when the “/ECC Mode” signal becomes “low,” Ex. 1014 (Hazelzet) at ¶[0069], and that the memory module switches to the “parity mode” when the “/ECC Mode” signal becomes “high.” Ex. 1014 (Hazelzet) at ¶[0070].

2. JEDEC LRDIMM Proposal (EX1015)

135. JEDEC discloses a proposed modification to the Memory Buffer (“*module controller*”) functionality of a DDR3 LRDIMM memory module, the standards for which were under development at that time, to add training modes that included training sequences and the ability to output notification signals providing the status of those sequences. I understand that JEDEC is prior art to the 595 Patent. The training modes included, among others, MB-DRAM Training that entailed training sequences Write Leveling Training and Read Enable Training

between the Memory Buffer and the DRAMs of the module. EX1015, 8. JEDEC also states that “[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete....” *Id.*

136. In the same description of MB-DRAM Training, JEDEC states that “training completion can be signaled by the assertion of ERROUT#.” *Id.*, 8. A Skilled Artisan would understand that “ERROUT#” refers to the parity error out pin on a JEDEC standard LRDIMM module of the time. Specifically, a Skilled Artisan would have understood there were other JEDEC documents defining other aspects of DDR3 LRDIMM at that time, such as EX1036, 1, which is a ballot for the “DDR3 SDRAM LRDIMM Design Specification.” Much like Hazelzet’s disclosed memory modules, the DDR3 LRDIMM memory modules at the time of the alleged invention were disclosed to include a PCB with various edge connections for data signals, address and command signals and an ErrOut_n pin that, during normal operation, was used to notify the memory controller of parity errors through the use of an open-drain output, a register/Memory Buffer/”module controller” (that, unlike Hazelzet, buffers address and command signals *and* data signals), and DRAMs. EX1036, 4 (“Product Description”), 8 (penultimate entry in table on page re ErrOut_n). A Skilled Artisan would have understood that the LRDIMM Design Specification’s ErrOut_n and JEDEC’s ERROUT# referred to

the same output/pin on the DDR3 LRDIMMs of the time. *See also* EX1044, 1 (October 2008 TI DDR3 buffer datasheet that discloses ERROROUT# open drain parity error signal).

137. JEDEC therefore discloses a training mode in which the memory module can be made to perform operations related to various training sequences, which does not include any memory read or write operations in response to memory controller commands, and which outputs a notification signal indicating status (*e.g.*, completion) of the training sequences over the same open drain output used to report parity errors in a normal mode of operation.

3. U.S. Patent No. 8,139,430 to Buchmann (Ex. 1016)

138. U.S. Patent No. 8,139,430 to Buchmann et al. (“Buchmann”), the application for which was filed on July 1, 2008, issued on March 20, 2012. I understand that Buchmann is prior art to the 595 Patent. Buchmann is entitled “Power-On Initialization and Test for a Cascade Interconnect Memory System” and discloses, among other things, such functionality. Ex. 1016 (Buchmann) at Title.

139. Buchmann discloses two modes of operation (*i.e.*, “SBC mode” and “high-speed mode”), Ex. 1016 (Buchmann) at Abstract, 1:39-44. The “high-speed mode” is a mode of operation “at a high nominal speed.” Ex. 1016 (Buchmann) at 14:67-15:2. On the other hand, the “SBC mode” is a mode of operation “at a

reduced rate” of communication. Ex. 1016 (Buchmann) at 14:65-67. According to Buchmann, before the high-speed bus between the memory controller and the memory module (*e.g.*, downstream bus 110 and upstream bus 112 in FIG. 1) can be used reliably to communicate with the memory modules, the memory module operates in the SBC mode to train the high-speed bus. Ex. 1016 (Buchmann) at 14:5-8, 3:52-54, 3:64-67; *see also id.* at FIG. 1, 4:11-14.

140. In particular, Buchmann discloses executing training and/or initialization sequences in its “SBC mode,” which is also referred to as an “error correcting code protected quasi-static bit communication” mode. Ex. 1016 (Buchmann) at 14:1-15:15; *see also id.* at 3:52-54, 5:6-22, 4:51-12:59. For example, the training and/or initialization sequences taught by Buchmann include “TS0-clock detection, test and repair; TS1-static configuration and calibration; TS2-downstream lane training and repair; TS3-upstream lane training and repair; TS4 packet training; TS5-initiate valid packets; TS6-frame lock; and TS7-read data latency calculation and inter-channel de-skew,” Ex. 1016 (Buchmann) at 5:40-46, FIG. 3.

141. As an example, training sequence TS0 involves “clock detection and repair,” Ex. 1016 (Buchmann) at 5:51-53, which is a training of the clock signal in the SBC mode. Ex. 1016 (Buchmann) at 5:66-6:22. In particular, the memory buffer MB (*i.e.*, “module controller,” as claimed) enters the TS0 state and initiates

the training sequence TS0 of Buchmann (*i.e.*, an example of a “training sequence” in the “second mode”) after receiving the SBC command “TS0_pdsck” from the host. Ex. 1016 (Buchmann) at 6:1-50 (Table 1 and Table 2, explaining that the “TS0_pdsck” command “causes the downstream receiver logic to enter the TS0 state, reset its memory channel PLLs and select the PDSCK clock as the MB reference clock” and that the “Host/MB drives downstream bus clock on SDSCK lane and issues TS0_pdsck SBC.”). Further, during the TS0 training sequence, the memory module generates and outputs various notification signals providing information about the training sequence to the memory controller of the host system, including the status of the TS0 training sequence (*e.g.*, “TS_done,” which notifies the host that the TS0 training is “done.”). Ex. 1016 (Buchmann) at FIG. 4, 5:51-7:2 & Tables 1-2.

142. As another example, training sequence TS3 involves “upstream lane training” and is “used to perform upstream data lane training,” Ex. 1016 (Buchmann) at 8:24-26, in the SBC mode, Ex. 1016 (Buchmann) at 8:27-47 (showing the SBC commands used during TS3 in Table 5). In particular, the memory buffer MB (*i.e.*, “module controller,” as claimed) initiates the “upstream lane training” TS3 of Buchmann (*i.e.*, another example of a “training sequence” in the “second mode”) after correction/forwarding of the SBC command “TS3_annnc” (*i.e.*, “TS3a announcement SBC”) from the host. Ex. 1016 (Buchmann) at 8:24-27

(“TS3 ... immediately follows TS2 with the host responsible for sending the TS3a announcement SBC.”), Table 5 (“TS3_annnc: This command announces the beginning of TS3a. This SBC is corrected and forwarded by MBs in the memory channel.”). Further, during the “upstream lane training” sequence TS3, the memory module generates and outputs various notification signals providing information about the training schemes to the memory controller of the host system, including the status of the TS3 training sequence, such as “TS3_ack,” which indicates that all downstream MBs have returned the TS3a_ack SBC, and “TS_done,” which notifies the host that the TS3 training sequence is “done.” EX1016, FIG. 6, 8:24-9:18 & Tables 5-6.

143. Buchmann discloses that his training operations may be initiated by power on, reset or initial program load operations, and “may be entered at different states,” which a person of ordinary skill would understand to mean that the his system was configurable to carry out some or all of the disclosed training. EX1016, 3:67-4:4, 4:51-5:12, FIG. 3. Moreover, Buchmann does not disclose the use of memory read and write operations during his TS0 and TS3 sequences during initialization/power-on. Buchmann therefore discloses a training mode (“*second mode*”) in which the memory module can be made to perform operations related to various training sequences and which does not include any memory read and write operations in response to memory controller commands.

144. Buchmann's implementation involves a daisy chain arrangement among the various modules of his system, resulting in signals from the memory module to the host indicating completion of a training sequence reaching the host only after all modules had completed the sequence. *See, e.g.*, Ex.

1016(Buchmann) at 3:49-52;14:41-43;16:47-50;28:23-26. However, Buchmann also explains that "one or more other bus structure(s) or a combination of bus structures" may be used, including "point-to-point bus(es)," "multi-drop bus(es)," and/or "other shared or parallel bus(es)." *Id.* at 28:26-31.

4. U.S. Patent No. 8,359,521 to Kim (Ex. 1017)

145. United States Patent No. 8,359,521 to Kim et al. ("Kim") was filed on January 22, 2008, the underlying application was published July 23, 2009, and the patent issued January 22, 2013. I understand that Kim is prior art to the 595 Patent. Kim is entitled "Providing a Memory Device Having a Shared Error Feedback Pin" and discloses such functionality. Ex. 1017 (Kim) at Title.

146. Kim discloses a "system and method for providing a memory device having a shared error feedback pin." Ex. 1017 (Kim) at Abstract. Kim discloses that sharing functionality with an error pin is desirable in order maximize use of available bandwidth, simplify the memory controller, Ex. 1017 (Kim) at 4:40-49, "mak[e] use of unused circuits within the subsystem," Ex. 1017 (Kim) at 11:31-34, and enable compatibility with standard memory modules, Ex. 1017 (Kim) at 5:49-

57. Kim teaches that this shared error feedback pin can be used to provide information such as status and error conditions and information related to initialization. Ex. 1017 (Kim) at 12:18-26. Kim further teaches how this shared error pin can be implemented using an open drain configuration and/or an OR-gate. Ex. 1017 (Kim) at 5:49-57; *see also id.* at 4:40-48; 6:1-16; FIG. 4, FIG. 5.

B. Background Technology

1. Shared Pins

147. By the effective filing date of the 595 Patent, a Skilled Artisan would have known that it was common to design the pins within a memory module such that a single pin is shared for various types of signals for different purposes due to the limited number of pins within the memory module. *See, e.g.*, Ex. 1026 (JESD82-20A) at page 18 (“The data mask signals share pins with the DQS[16:9] pins. ... The following table shows the mapping between DQS pins and data mask pins.”); Ex. 1017 (Kim) at FIG. 5 (showing that the pins related to the open drain transistor (on the right) is shared between the “parity check” circuitry and the “CRC check” circuitry (on the left)).

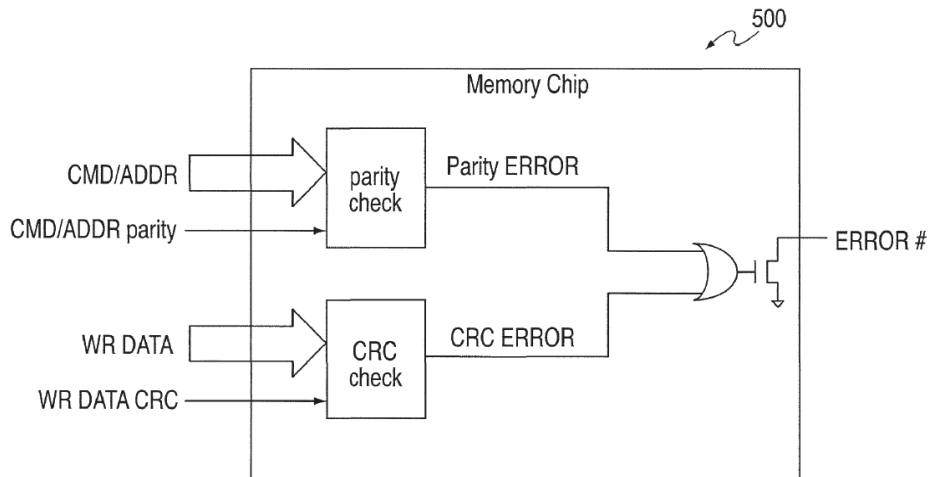


FIG. 5

148. As an example, Kim explains that its “pin [for] reporting CRC errors ... could also be merged with an existing error pin available on many industry standard modules for the reporting of address/command errors.” Ex. 1017 (Kim) at 5:49-55; *see also id.* at 6:13-18 (“In alternate exemplary embodiments, other functions also share the error feedback pin (*e.g.*, parity or CRC error(s) on command and address information).”).

149. A Skilled Artisan also knew that it was customary to use a logic OR circuit, as shown in FIG. 5 of Kim, to implement the shared pin. *See, e.g.*, Ex. 1017 (Kim) at FIG. 5 (showing a logic OR circuit coupled to the gate of the open drain transistor). *See* Ex. 1017 (Kim) at FIG. 5 (annotated to show the logic OR circuit in red), 6:13-16 (“FIG. 5 is a block diagram of a memory device 500 that shares an error feedback pin between data CRC and address parity in accordance with an exemplary embodiment of the present invention.”); *see also* Ex. 1023, US

20080155378 (Amidi) at FIG. 2, FIG. 4, ¶[0018] (“An output device 120 functioning as a logic OR ties the output ends of the error detection module 158 and the transmission memory 156 together such that the error detection module 158 and the transmission memory 156 share the output terminal error-out 168 to transmit signals to the memory controller 110. The output device 120 can be implemented as an OR gate, a wired-OR gate, an open collector, or other device functioning as a logic OR.”); *see also id.* at FIG. 2 (showing that the “error out” signal is output from a “logic OR” element), FIG. 4, claim 17 (“The buffer device of claim 16 wherein the output terminals from the error detection module and the transmission memory are tied using a device functional as a logic OR before being applied to the output terminal for sending the error signal.”).

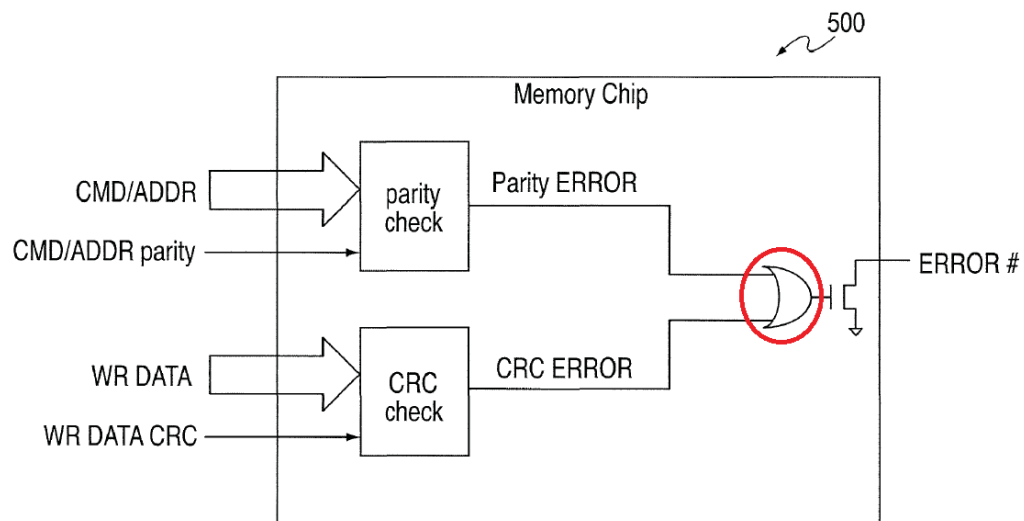


FIG. 5

[FIG. 5 of Kim]

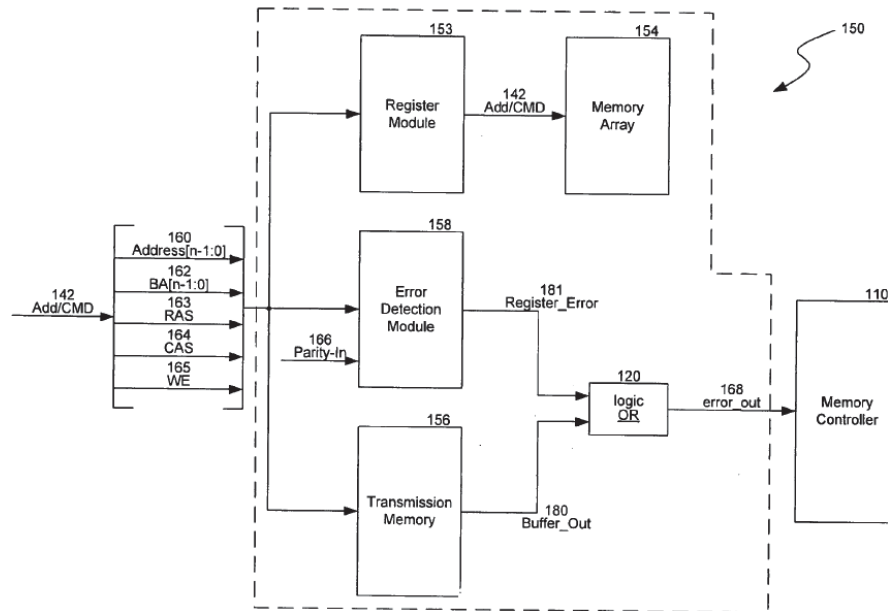


FIG. 2

[FIG. 2 of Amidi]

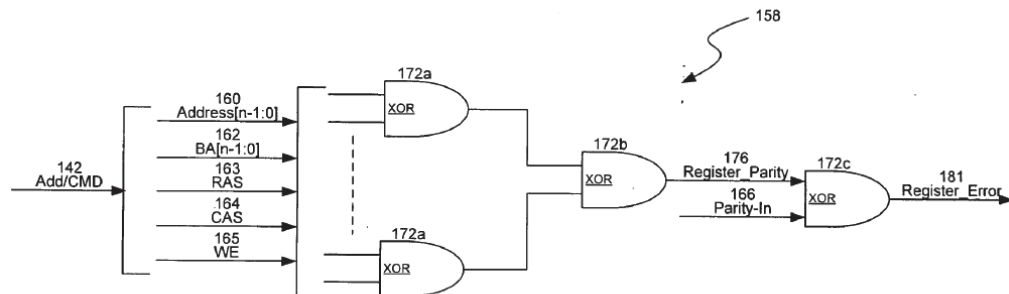


FIG. 4

[FIG. 4 of Amidi]

2. Open-Drain Output

150. By the effective filing date of the 595 Patent, a Skilled Artisan understood that it was common to use an “open drain output” in a memory module

to send error signals to the host memory controller. *See, e.g.*, US 8,359,521 to Ex. 1017 (Kim) at FIG. 4 (reproduced below), 4:40-48; 6:1-16; Ex. 1014 (Hazelzet) at ¶¶[0072], [0109].

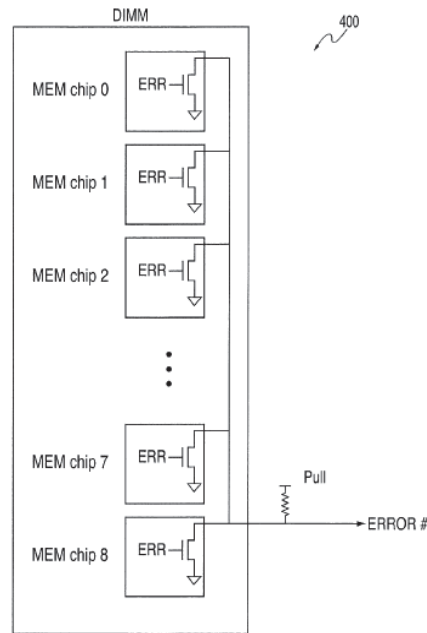


FIG. 4

151. An “open drain output” is an output pin coupled to the drain of a field effect transistor, which includes three ports (*i.e.*, a gate, a source, and a drain). *See, e.g.*, Ex. 1017 (Kim) at FIG. 4. As an example, FIG. 4 of Kim shows an open drain output that is coupled to a pull-up resistor (*i.e.*, connected to a high voltage via a pull-up resistor). FIG. 4 of Kim also shows that the source of the transistor is coupled to ground. Because the source of the transistor is coupled to ground (as opposed to Vdd), a positive voltage at the gate (*i.e.*, ERR in FIG. 4 of Kim) would turn on the transistor. Based on this bias condition, a Skilled Artisan would have

understood that Kim's transistor is an NMOS (*i.e.*, n-channel Metal Oxide Semiconductor) transistor, as opposed to a PMOS (*i.e.*, p-channel Metal Oxide Semiconductor). *See, e.g.*, Ex. 1017 (Kim) at FIG. 4. This is also clear from the symbol. A PMOS transistor would use a symbol with a bubble at the gate. *Id.*

152. A Skilled Artisan would have understood that such open drain outputs (*e.g.*, ERROR# in FIG. 4 of Kim) would be pulled to a high logic level (*i.e.*, the supply voltage connected to the resistor) through the resistor when the gate of the transistor is low, because the transistor would be off. *See, e.g.*, Ex. 1017 (Kim) at FIG. 4. The output would therefore be in an un-driven, high impedance, state. Ex. 1014 (Hazelzet) at ¶[0099]. On the other hand, the open drain output would switch to a low logic level (*e.g.*, ground) when the gate of the transistor is high, because the transistor would be on. *Id.*

C. The Combinations Relied on Here

153. The combinations analyzed here – Hazelzet/JEDEC and Hazelzet/Buchmann – are straightforward. In each, Hazelzet's memory module would be modified to add a training mode ("*second mode*") into which the module could be switched and which includes training sequences and which reports completion of those training sequences by a notification/status signal output over an open drain output (*e.g.*, UE 121) of Hazelzet.

154. In the JEDEC combination, the training sequences would be like those described as MB-DRAM Training in JEDEC (*e.g.*, Write Leveling and Read Enable Training), EX1015, 8, and the open drain output signal would be similar to the signal output on the ERROUT# pin as described in JEDEC, *id.* at 8; *see also* EX1036, 8 (penultimate entry in table on page re ErrOut_n – is an open drain output for parity errors during normal operation). During those training sequences, the memory controller communicates no data with the module and performs no operations to read or write to the memory devices; the training is carried out by memory buffer (module controller) itself. EX1015, 8.

155. In the Buchmann combination, the training sequences would be like those described as TS0, EX1016(Buchmann) at FIG. 4, 5:51-7:2 & Tables 1-2, or alternatively, like those described as TS3, EX1016(Buchmann) at FIG. 6, 8:24-9:18 & Tables 5-6. The open drain output signals would be TS0_done, in the former case, EX1016(Buchmann) at FIG. 4, 5:51-7:2 & Tables 1-2, and TS3_ack or TS3_done, in the latter case, EX1016(Buchmann) at FIG. 6, 8:24-9:18 & Tables 5-6. Buchmann does not disclose the memory controller communicating any data with the module or performing operations to read or write to the memory devices during either TS0 or TS3 sequences during initialization/power-on.

156. In either combination, the circuitry of Hazelzet's module, in particular the ECC/Parity register, would be modified to implement the training as part of an

additional mode to run, for example, at initialization with Hazelzet's other disclosed initialization operations and to use an open drain output of Hazelzet to communicate the new notification signals. EX1014(Hazelzet) at ¶[0123] (initialization operations); EX1015, 3 (training occurs during initialization); EX1016(Buchmann) at 3:49-60 (same). As explained in more detail below, Hazelzet already uses his UE 121 open drain output for two different signals in two different modes. Thus, this ECC/Parity register necessarily includes circuitry for receiving inputs for each of those signals, and selecting which one to drive on the UE 121 output depending on the mode of the module. It was well within the level of ordinary skill to modify such circuitry such that it accepted three different inputs for three different modes and would select among them depending on the mode, and a Skilled Artisan could have made that modification without undue experimentation and with a reasonable expectation of success.

157. Finally, these combinations would employ known open drain signaling circuitry, which necessarily included a transistor having its source coupled to ground and its drain as the output. That is what a Skilled Artisan would understand the phrase "open drain" to mean. EX1017, FIGs 4&5. A Skilled Artisan would have also known that in order to use open drain signaling to indicate training completion among multiple modules, as here, the open drain output would have to be configured such that the transistor output is driven low (ground) while

training is still occurring and driven high upon training completion. This is because, with an open drain configuration shared by multiple modules, any module can individually drive the output low, but it takes the collective action of all connected modules to drive the output high. Moreover, a Skilled Artisan would also understand that to drive the output low (which would be a low impedance state), the gate of the transistor must be high, causing the transistor to conduct and connect the drain to ground. Conversely, to drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off. This is how an open drain output works. EX1014, ¶[0099]; EX1017, FIGs. 4-5, 5:65-6:18.

D. Reasons to Combine

158. All of the prior art relied on in this declaration to combine Hazelzet and JEDEC or Buchmann are analogous art to the 595 Patent because all are in the same field of invention – memory module design, including error detection and correction, initialization, training and the use of pins/paths for multiple purposes during different operations/modes, EX1001(595 Patent) at Abstract, 5:66-6:14;8:4-48 (purported invention is memory module with an operating mode during which parity checking occurs and another mode during which initialization/training occur, and the same errout pin is used to provide notification signals indicating status to the memory controller during both modes, either regarding parity or

initialization/training); EX1014(Hazelzet) at Abstract, ¶¶[0007],[0069]-[0070],[0123] (explaining that invention relates to memory modules, with, among other things, two operating modes – ECC mode and parity mode, in which the two modes share a signal pin for notifying the memory controller of errors – and initialization operations/modes); EX1015, 1, 3, 8 (noting document is JEDEC ballot for “LRDIMM DDR3 Memory Initialization Chapter Proposal”, that includes various training during initialization, including that utilizes the parity ERROUT# pin for multiple purposes including training notifications of status); EX1016, 1:7-9;3:49-60;4:51-5:50;12:60-13:41;14:1-63;20:20-21:19;33:45-67 (explaining that invention relates to memory modules, with, among other things, an SBC mode and a “high-speed” or “functional” mode, wherein the SBC mode combines initialization/training and ECC that runs at power-on initialization and can also be entered from normal (i.e., “high-speed” or “functional”) operation for ECC without full re-initialization/training); EX1022, ¶¶[0004]-[0005],[0032]-[0033],[0052] (explaining that invention relates to memory modules, with, among other things, two modes – “a normal operation mode and a configuration and test mode” (a part of which is called “training mode”) – and, during “training mode,” the “CRC signal path” (normally used for “error detection” and “correct[ion]”) is used to “loop back” “training patterns” sent on the “BCMD signal path” (a command signal) to train the BCMD signal path); EX1025, 15-18 (JEDEC

memory module standard for FBDIMM, specifying, in addition to various operating modes, initialization sequences that “must sequence the AMB devices through the Disable, Calibrate, (back to Disable), *Training*, Testing, and Polling states in order to transition the AMBs into the active channel L0 state” (e.g., operating modes)); EX1027, 1:61-2:19;6:24-25;10:24-45 (discussing importance of training, including for memory modules, and disclosing, in addition to a “standard operating mode,” a “training mode” that occurs before “standard operating mode”); EX1017(Kim) at 1:16-22;5:49-57;6:8-18;11:20-34;12:36-53(explaining that invention relates to memory modules, with, among other things, two operating modes – ECC mode and parity mode, in which the two modes share a signal pin for notifying the memory controller of errors – and initialization operations/modes that includes “completing a training process to establish reliable communication”, and further teaching that “initialization circuitry” “may reside local to the” memory module and that, by doing so, “added performance may be obtained as related to the specific function, often while making use of unused circuits within the subsystem,” and further teaching that, in addition to sharing ECC and parity on the error out pin, “[i]n alternate exemplary embodiments, other functions also share the error feedback pin”), and each is reasonably pertinent to the problem addressed by that patent – increasing memory module capacity, performance, and/or reliability by sharing an output pin/path to perform multiple functions during multiple

operations/modes, including initialization/training, EX1001(595 Patent) at Abstract, 5:66-6:14;8:4-48; EX1014(Hazelzet) at Abstract, ¶¶[0007],[0069]-[0070],[0123]; EX1015, 1, 3, 8; EX1016(Buchmann) at 1:7-9;3:49-60;4:51-5:50;12:60-13:41;14:1-63;20:20-21:19;33:45-67; EX1022(Talbot) at ¶¶[0004]-[0005],[0032]-[0033],[0052]; EX1025, 15-18; EX1027, 1:61-2:19;6:24-25;10:24-45; EX1017(Kim) at 1:16-22;5:49-57;6:8-18;11:20-34;12:36-53.

159. Also, one skilled in the art would have considered each of the combinations analyzed here to be merely an arrangement of old elements with each performing the same function it had been known to perform and yielding no more than what one would expect from such an arrangement. Each of Hazelzet, JEDEC, Buchmann and Kim, for example, is a prior art disclosure employing known signaling and training techniques. Many prior art systems had similarly included such techniques. Combining them as described here would therefore have been well within the level of ordinary skill in the art, would not have resulted in any unpredictable results and could have been readily accomplished without undue experimentation and with a reasonable expectation of success.

160. A Skilled Artisan would have been motivated to make these combinations for at least the following reasons.

1. Motivation to Add Training

161. A Skilled Artisan would have been motivated to add training to the system of Hazelzet. For example, Hazelzet emphasizes the need for “improved overall system reliability.” EX1014(Hazelzet) at ¶[0003] (“Thus the emphasis and need for improved overall system reliability is increasing dramatically and requires a comprehensive system solution that includes both a high degree of fault tolerance and overall reliability.”); *see also id.* at ¶[0042] (“The ECC/Parity buffer chips 21 on DIMM 20 include unique error correction code (ECC) circuitry that is coupled to the memory interface chip 18 via line 25 to provide even greater significant reliability enhancement to such servers. The inclusion of this new, improved error correction code (ECC) circuitry results in a significant reduction in interconnect failure.”), ¶[0044] (“The novel ECC/ Parity buffer 21 on DIMM 20 thus provides leading-edge performance and reliability and key operational features different from and unavailable from the prior art while retaining timing requirements generally consistent with devices such as the JEDEC 14 bit 1:2 DDR II register.”), Abstract (“A high density high reliability memory module with power gating and a fault tolerant address and command bus.”), ¶[0001] (“This invention relates generally to a high-density, high-reliability memory module with a fault tolerant address and command bus for use as a main memory that will achieve the degree of fault-tolerance and self-healing necessary for autonomic computing systems.”),

¶[0004] (“The present invention provides such a comprehensive system solution that includes the capability of high memory density and a high degree of fault tolerance and the overall differentiated system reliability long desired in the server market.”), ¶[0007] (“The present invention is directed to a high density high reliability memory controller/interface module, provided with a high degree of compatibility with industry standard solutions, capable of meeting the desired density, performance and reliability requirements and interfacing with the presently available memory modules, as well as with existing or enhanced support devices. The present invention accomplishes all these ends, resulting in a high density and enhanced reliability memory solution at low cost.”). Given Hazelzet’s emphasis on the need for “improved overall system reliability,” one skilled in the art would have been motivated to add training to Hazelzet because it was known that training improved the reliability of a memory module’s operations. EX1027, 1:35-2:12 (discussing importance of training, including for DIMMs, given advent of DDR memory devices and increasing frequencies, and stating “During a training stage, such a memory controller may write certain data to and read certain data from a memory device, for example a DRAM, and shift the data signal in respect to the clock signal within the time domain, such that the data signal arrives at the memory device with a well-defined synchronization to the clock signal. The memory controller may vary this time shift until a written value corresponds to a

read value, which indicates that timing is correct. *In this way, a reliable, fast, and efficient exchange of information is enabled.*” (emphasis added)); EX1025, 15-18 (“FBDIMM Architecture and Protocol” standard, specifying initialization sequences that “must sequence the AMB devices through the Disable, Calibrate, (back to Disable), *Training*, Testing, and Polling states in order to transition the AMBs into the active channel L0 state” and, for training, noting that, “[b]efore the channel is initialized the bit lanes are not aligned to a frame boundary, thus preventing Channel and DRAM commands from being communicated to the AMBs” such that training is required). This is particularly true given the emerging DDR3 applications in the 2009-10 time-frame and their increased speeds. EX1045, 22-24 (2008 Micron technical note explaining need for training for reads and writes). Indeed, Hazelzet discloses that “[i]nitialization of the memory subsystem” should occur, it just does not address training as part of that initialization or provide any details regarding how to go about that aspect of initialization. EX1014, ¶[0123]; EX1017, 12:36-53.

162. Further, JEDEC includes a portion of the draft standard for DDR3 LRDIMMs being voted upon by JEDEC members that specifically addresses “power-up initialization,” requires various training including “MB-DRAM Training” and explains that, during that training, “[t]he MB performs ‘Write Leveling’ to the DRAMs **to ensure successful writes**, and ‘Read Enable Training’

to ensure it can capture read data from the DRAMs correctly, as part of the DRAM interface training,” and further teaches that “MB DRAM interface training must be completed before any MB host interface read or write training **to ensure that the MB DRAM interface is configured optimally for DRAM reads and writes.**” EX1015, 3,8-9 (emphasis added). These statements would have motivated a person of ordinary skill to add training to other systems, such as that of Hazelzet.

163. Also, Buchmann’s “SBC mode” is a mode of operation where “error correcting code” is provided, EX1016 (Buchmann) at 14:25-32, as well as a “training phase that allows more flexibility and improved control data exchange during start-up,” *id.*, 3:64-67, to establish “reliable communication” on the bus, *id.* at 14:28-35 (“Quasi-static bit communication, also referred to as ‘static bit communication’ or ‘SBC’, can be used to control the sequence of link initialization and training phases to establish reliable communication on the high-speed bus. When error correction of an SBC sample is performed prior to checking for a static pattern, the error correction may be able to repair errors that would otherwise prevent the pattern from being static over a period of time.”); *see also id.* at 14:5-8. Thus, one skilled in the art would have been motivated by Hazelzet’s desire to improve reliability to look to systems such as JEDEC’s and Buchman’s that were designed to do just that.

2. Motivation to Add Training As A Mode Separate from Normal Operations

164. One skilled in the art would also have been motivated to combine Hazelzet and JEDEC or Buchmann by adding training in a mode separate from normal operations because she would have known that memory systems are typically and most efficiently initialized/trained before normal operations occur. For example, it was well-known that training/initialization of a memory module before normal operation was necessary to minimize errors, by “ensur[ing] successful writes,” and “ensur[ing] [the register on the DIMM] can capture read data from the DRAMs correctly.” EX1015, 8. Indeed, JEDEC’s training is taught to be completed as part of “power-up initialization,” before moving to “Normal Operation.” *Id.* at 3 (listing eight steps, including various training, as part of initialization before listing “Normal Operation” as step 9); *see also* EX1025, 15-18 (“FBDIMM Architecture and Protocol” standard, specifying initialization sequences that “must sequence the AMB devices through the Disable, Calibrate, (back to Disable), *Training*, Testing, and Polling states in order to transition the AMBs into the active channel L0 state” and, for training, noting that, “[b]efore the channel is initialized the bit lanes are not aligned to a frame boundary, thus preventing Channel and DRAM commands from being communicated to the AMBs” such that training sequences are required); EX1022, Fig. 4, ¶¶[0032], [0052],[0088-89]; EX1056, 18, 22, 25-26, 42-44, EX1057, Fig. 5, Abstract, 2:13-

34, 2:60-3:3, 9:11-10:44. Likewise, Buchmann's invention is an "initialization training sequence" completed at "power-on," EX1016(Buchmann) at Abstract (explaining that its "memory buffer includes logic for executing a power-on and initialization training sequence initiated by the memory controller."), which would also suggest to a Skilled Artisan that training before normal operation is important.

165. Because the memory system in Hazelzet would be initialized upon power-on, *see, e.g.*, EX1014(Hazelzet) at ¶[0123] ("Initialization of the memory subsystem may be completed via one or more methods, based on the available interface busses, the desired initialization speed, available space, cost/complexity objectives, subsystem interconnect structures, the use of alternate processors (such as a service processor) which may be used for this and other purposes, etc."); *see also* EX1025, 15-18 (JEDEC memory module standard for FBDIMM, specifying initialization sequences that "must sequence the AMB devices through the Disable, Calibrate, (back to Disable), *Training*, Testing, and Polling states in order to transition the AMBs into the active channel L0 state" (*e.g.*, operating modes)); EX1027, 1:61-2:19; 6:24-25; 10:24-45 (discussing importance of training, including for memory modules, and disclosing, in addition to a "standard operating mode," a "training mode" that occurs before "standard operating mode"), JEDEC's and Buchmann's training (that is disclosed in each to occur at initialization) would have complemented that power-up process as part of Hazelzet's initialization, and

one skilled in the art would have therefore been motivated to combine Hazelzet and JEDEC or Buchmann in a training mode occurring before, and separate from, other, normal operating modes.

3. Motivation to Use Hazelzet's Open Drain Signaling for Training Notifications

166. In the obvious combination of Hazelzet and JEDEC or Buchmann analyzed here it would have been further obvious to employ the open-drain parity and ECC signal connections and techniques of Hazelzet to communicate the status of the JEDEC or Buchmann training sequences, any of which satisfies the claimed “*information related to the one or more training sequences*,” since they each indicate some status of the related training operation.

167. To be clear, as to JEDEC, it is my opinion that a Skilled Artisan would have found it obvious to communicate that the MB-DRAM training was completed using the open drain output (*e.g.*, UE 121) of Hazelzet, and, as to Buchmann, it is my opinion that a Skilled Artisan would have found it obvious to communicate that the TS_done signal of Buchmann for TS0 training, and also obvious to communicate the TS3_ack and/or TS_done signals of Buchmann for TS3 training, using the open drain output (*e.g.*, UE 121) of Hazelzet, for the reasons set forth below.

168. For example, Hazelzet's “ECC mode” is a mode where a notification signal indicating an “uncorrectable error” (*i.e.*, “UE”) can be output to the memory

controller through the open-drain output line and 121 (*i.e.*, output for uncorrectable error “UE”). EX1014(Hazelzet) at FIG. 4B, ¶¶[0044],[0049],[0059],[0064],[0069],[0072],[0109]. The open-drain output line 121 (or “/Error (UE)” 121) is the same open drain output that is used for the parity error signal. EX1014 (Hazelzet) at FIG. 4B, ¶¶[0044],[0049],[0059], [0064],[0070],[0109]. The open-drain output line 121 is coupled to the memory controller of the host system using error edge connection number 142. EX1014(Hazelzet) at FIG. 7A (indicating “UE” is pin 142). As such, Hazelzet’s implementation involves using the same open drain output (“/Error (UE)” 121), in two different modes, to output both a parity error notification signal and an ECC notification signal, depending on which mode the memory module is in. EX1014(Hazelzet) at FIG. 4B, ¶¶[0044],[0049],[0059],[0064],[0069-70],[0072],[0109]. Hazelzet’s use of the same output in two different modes would have suggested to, and motivated a person of ordinary skill in the art to use that same output in the added training mode, particularly when the training mode was implemented separate from, and before, the parity and ECC modes of Hazelzet, as here. In such a system, those modes, which include normal memory operations, would therefore not be using the open drain outputs while the training mode was running during initialization.

169. Similarly, JEDEC employs this same technique, using the same open drain output to communicate parity error and training completion in different

modes. Thus, a Skilled Artisan would have viewed JEDEC's technique as a natural fit in the system of Hazelzet, and JEDEC's disclosure would have motivated the use of that technique in other systems, such as with Buchmann.

170. Further, a person of ordinary skill in the art would have been motivated to use the same output to notify error signals and training status because such multiple use of a pin was known, and would have been considered an efficient use of the limited number of output pins on integrated circuits. For instance, Kim, EX1017, is a patent assigned to IBM that shares with Hazelzet a substantial overlap in their disclosures, particularly in the disclosures of open-drain shared outputs and in the latter halves of their specifications. Kim was filed approximately a year and a half after Hazelzet and discloses additional details regarding the use of an open-drain output on a memory module to notify the memory controller of errors during a parity normal operating mode and during an ECC normal operating mode. EX1017(Kim) at 1:16-22;5:49-57;6:8-16. Kim further teaches initialization operations (initialization/training modes) that include “completing a training process to establish reliable communication,” *id.* at 12:36-53, teaches that “initialization circuitry” “may reside local to the” memory module and that, by doing so, “added performance may be obtained as related to the specific function, often while making use of unused circuits within the subsystem,” *id.* at 11:20-34, and further teaching that, in addition to sharing ECC and parity on

the error out pin, “[i]n alternate exemplary embodiments, other functions also share the error feedback pin,” *id.* at 6:16-18. Such disclosures would have motivated a Skilled Artisan to use Hazelzet’s “/Error (UE)” 121 open-drain output (corresponding to Kim’s “error feedback pin”) to notify the memory controller that the training was in progress or done.

171. As another example, Talbot discloses memory modules, with, among other things, two modes – “a normal operation mode and a configuration and test mode” (a part of which is called “training mode”). EX1022(Talbot) at ¶¶[0004]-[0005],[0032]-[0033],[0052]. Talbot further discloses that, during the “training mode,” the “CRC signal path” (normally used for “error detection” and “correct[ion]”, *id.* at [0033]) is used to “loop[] back” “training patterns” sent on the “BCMD signal path” (a command signal) to train the BCMD signal path, *id.* at [0052]. Thus, Talbot discloses using a CRC (i.e. ECC) signal path to return signals relating to training during the training mode when the CRC functionality is off. *Id.* at [0033],[0052]. Such disclosures would have motivated a Skilled Artisan to use Hazelzet’s “/Error (UE)” 121 open-drain output (corresponding to Talbot’s “CRC signal path”) to notify the memory controller that the training was in progress or done.

172. Moreover, a Skilled Artisan would have been motivated to arrange the modified Hazelzet to communicate a signal indicating completion of training only

when all memory modules have completed that training, in order to ensure that the entire memory system had been trained before proceeding to normal operation.

This would permit training to be completed in an orderly and systematic manner, thereby limiting the complexity of the control circuitry needed to implement the training. EX1043, 7:30-51. Use of an open drain signal in this manner was a known, efficient way to communicate information about multiple circuits because it effectively OR'd the inputs into a single output. EX1017(Kim) at FIG. 4; 5:65-6:12 (illustrating and describing just such a system); *see also* EX1014(Hazelzet) at [0018] (“After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules.”), [0109] (“The error reporting circuitry, of the present invention is included to permit external monitoring of device operation. Two open-drain outputs are available to permit multiple modules to share a common signal pin for reporting an error that occurred during a valid command (any /CS low) cycle (consistent with the re-driven signals).”).

173. In addition, a Skilled Artisan would have been further motivated to modify Hazelzet as described above, because Hazelzet's memory system includes multiple memory modules in need of training. In other words, there would be a motivation to delay transitioning to a normal mode of operations until all memory

modules had signaled the completion of training. EX1014(Hazelzet) at [0018] (“After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules.”), [0109] (“The error reporting circuitry, of the present invention is included to permit external monitoring of device operation. Two open-drain outputs are available to permit multiple modules to share a common signal pin for reporting an error that occurred during a valid command (any /CS low) cycle (consistent with the re-driven signals).”); *see also* EX1017(Kim) at FIG. 4; 5:65-6:12; EX1043, 7:30-51. In particular, a Skilled Artisan would have been motivated to use Hazelzet’s open-drain output to notify the host of training status because that technique allows any module in the system to pull the open drain pin to “low” (i.e. to ground) if it is still executing its training sequence, regardless of whether other modules in the system have completed training and are no longer pulling that pin low. *Id.* As I demonstrate above, an open drain was a known way to signal when multiple circuits were, or were not all, finished performing some operation. *See* ¶¶147-152.

V. COMPARISON OF THE PRIOR ART TO THE CLAIMS OF THE 595 PATENT

174. My analysis is based on my understanding of the law as set forth above and the ordinary and accustomed meaning of the claim terms as understood

by one of ordinary skill in the art in view of the 595 Patent and its file history, including the constructions I presented for four of the claim terms. See ¶¶105-129.

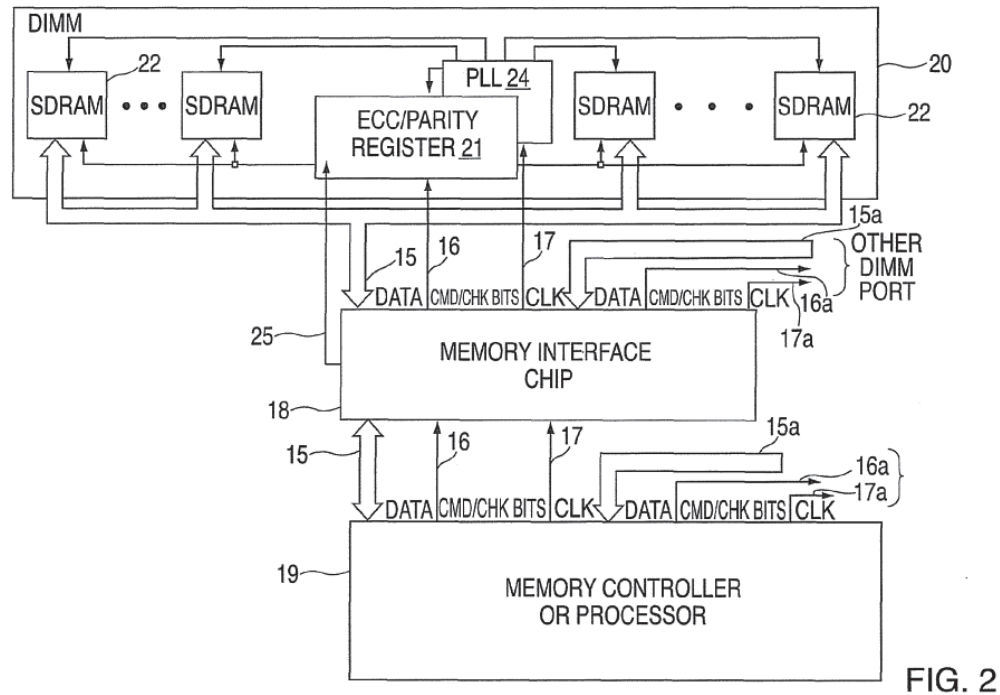
A. Claims 1-24 Are Unpatentable Over Hazelzet and JEDEC or Buchmann, with or without Kim for Certain Claims

1. Claim 1 is Unpatentable

a) [1.a] Preamble

175. The preamble of claim 1 requires “[a] memory module operable with a memory controller of a host system, comprising.”

176. Hazelzet discloses dual inline memory modules 20 (i.e., “DIMMs”) that are configured to operate with the “memory controller” 19 of the host system. Ex. 1014 (Hazelzet) at FIGs. 2, 3A-3D, ¶¶[0037], [0038], [0039]; see also Ex. 1014 (Hazelzet) at ¶[0036] (referring to DIMMs as “dual inline memory modules”).

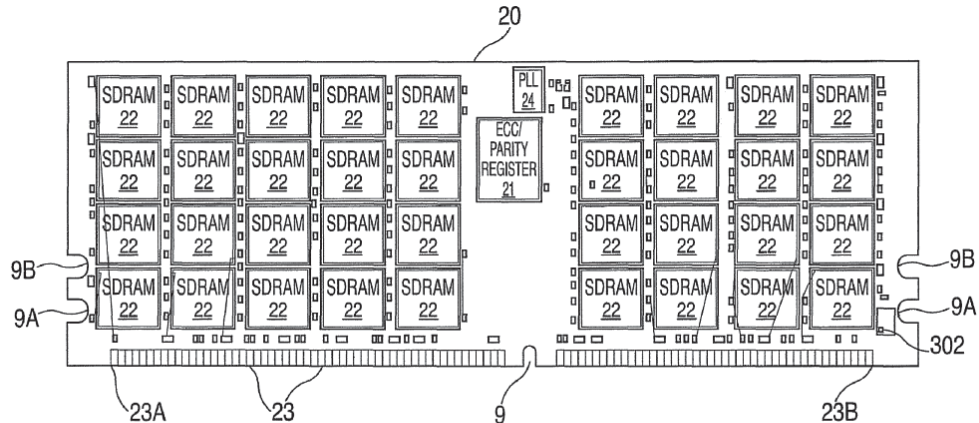


177. Accordingly, Hazelzet satisfies “[a] memory module operable with a memory controller of a host system.”

b) [1.b] Printed Circuit Board Having Edge Connections

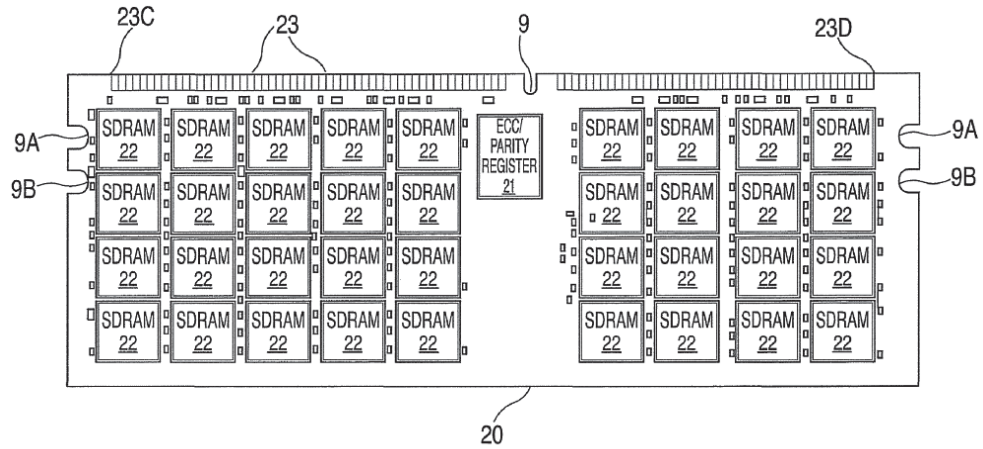
178. Claim 1 requires “a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections.”

179. Hazelzet explains that the “DIMM of the present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface,” EX1014, ¶[0015], examples of which are shown in FIGS. 2, 3A, 3B, 3C, and 3D. See EX1014, FIGS. 2, 3A-3D; see also *id.* at ¶[0037] (“Turning now to FIGS. 2, 3A, 3B, 3C, 3D, 4A, 4B, 5, 8, 9, 10 and 11, the enhanced server memory arrangement of the present invention will be described.”), ¶[0039], Abstract (“The memory module includes a rectangular printed circuit board having a first side and a second side, a length of between 149 and 153 millimeters and first and second ends having a width smaller than said length.”).



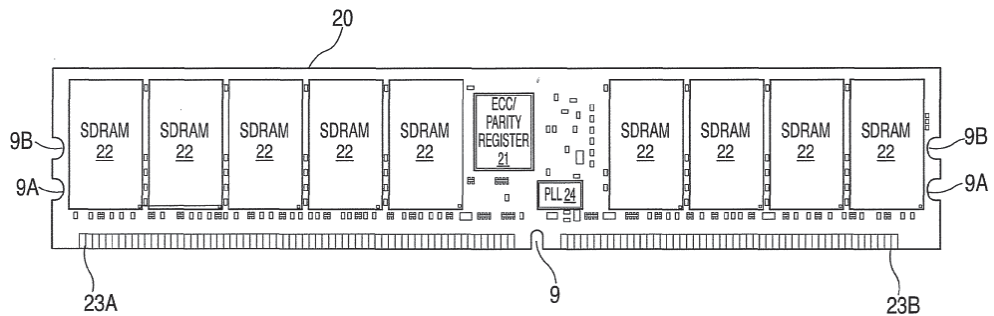
FRONT SIDE OF DIMM - 72 PLANAR

FIG. 3A



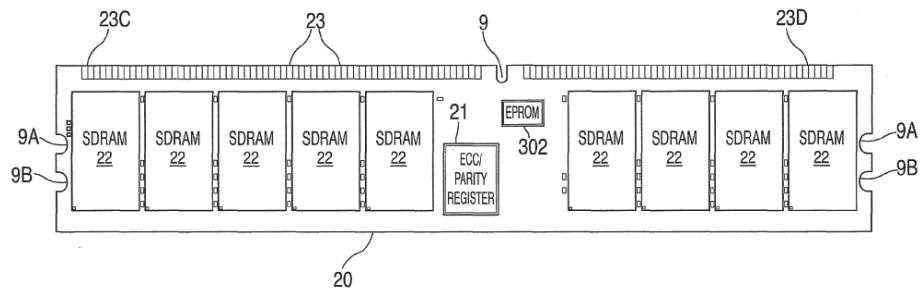
BACK SIDE OF DIMM - 72 PLANAR

FIG. 3B



FRONT SIDE OF DIMM - 4 HIGH STACK

FIG. 3C



BACK SIDE OF DIMM - 4 HIGH STACK

FIG. 3D

180. Hazelzet further explains that its memory modules include “connectors 23 along the edge of both the back and front sides” of the printed circuit board, Ex. 1014 (Hazelzet) at ¶[0039] (“Generally speaking DIMMs are printed circuit cards designed to carry a plurality of DRAMs 22 thereon and the DRAM output pins (not shown) are connected via the printed circuit to selected connectors 23 along the edge of both the back and front sides of the card and are often provided with a single indexing key or notch 9 on the connector edge.”), which are provided to form connections to the memory controller of the host system when the memory module is inserted into a corresponding “slot” of the host system. Ex. 1014 (Hazelzet) at ¶[0097] (“Referring to FIG. 11, column 1102 is the slot in the memory system being occupied by the memory module. ... For memory modules having one buffer chip 21, the IIC address correlates to the slot being occupied by the memory module as shown in column 1106”); *see also id.* at ¶[0032], FIG. 11, FIG. 9 (showing the maximum number of “DIMM slots” for “1, 2, and 4 rank DIMMs.”).

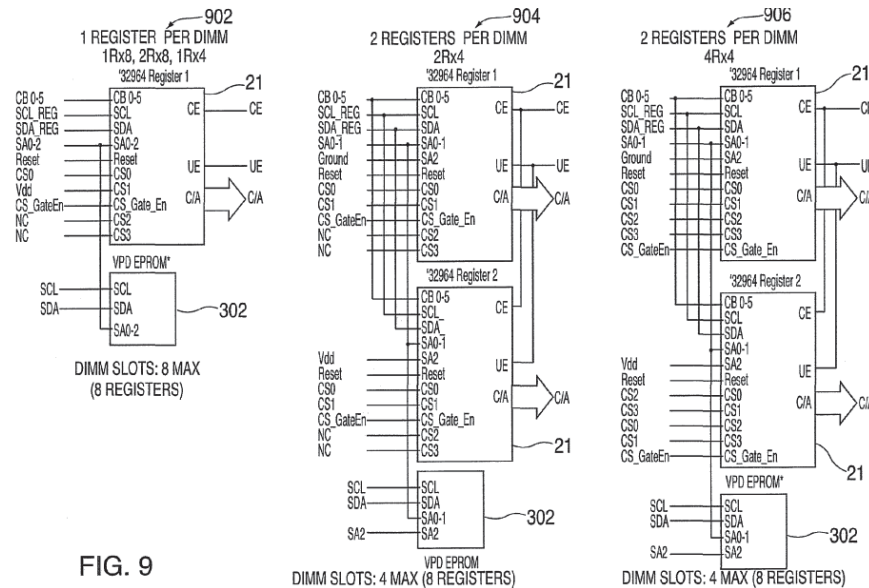


FIG. 9

181. Hazelzet therefore discloses “a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller.”

182. Hazelzet further discloses that the printed circuit board has a first set of edge connections for communicating data signals between the memory module and the memory controller of the host system, Ex. 1014 (Hazelzet) at FIGs 7A-7C (showing data edge connections including pins 11, 12, 17, 18, 22, 23, 31, 32, 37, 38), while the memory module is in either the “parity mode” or the “ECC mode,” *id.* at FIG. 8 (showing “Data In” and “Data Out” in both the “parity mode” and the “ECC mode.”), ¶¶[0015],[0035],[0038],[0041].

183. Hazelzet further discloses that the printed circuit board has a second set of edge connections for communicating address and control signals from the

memory controller of the host system. Ex. 1014 (Hazelzet) at FIGs 7A-7C (showing address edge connections including pins 67, 70, 72-75, 82, 205-207, 210-213, 220, 227 and command edge connections including pins 86, 89, 91, 93), ¶¶[0072] (referring to “/CS” as commands), ¶¶[0068] (listing various control signals including “chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE)” signals); *see also* Ex. 1014 (Hazelzet) at ¶¶[0038] (“The memory interface chip 18 then sends and receives data, via line 15, to the memory devices or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16 and check bits for error correction purposes to the ECC/ Parity register chip 21 via line 25.”), FIG. 2 (showing address and command line 16), ¶¶[0015],[0035],[0041].

184. Hazelzet further explains that the printed circuit board has an error edge connection coupled to the open drain output of the module controller. Ex. 1014 (Hazelzet) at FIGs 7A (showing an uncorrectable error pin UE (142) of the memory module that is coupled to the open drain output “/Error (UE)” 121); *see also id.* at FIG. 4B, ¶¶[0072], [0109].

185. Accordingly, Hazelzet discloses “*the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and*

control signals, and an error edge connection in addition to the first edge connections and the second edge connections.”

c) [1.c] Dynamic Random Access Memory Elements

186. Claim 1 requires “*dynamic random access memory elements on the printed circuit board.*”

187. Hazelzet explains that its memory module (DIMM) includes a plurality of “synchronous dynamic random access memories (SDRAMs)” / “DRAMs” on the “printed circuit board,” Ex. 1014 (Hazelzet) at ¶[0015] (“The DIMM of the present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface.”), examples of which are shown in FIGS. 2, 3A, 3B, 3C, and 3D. See Ex. 1014 (Hazelzet) at FIGs. 2, 3A-3D; see also *id.* at ¶[0037], ¶[0039].

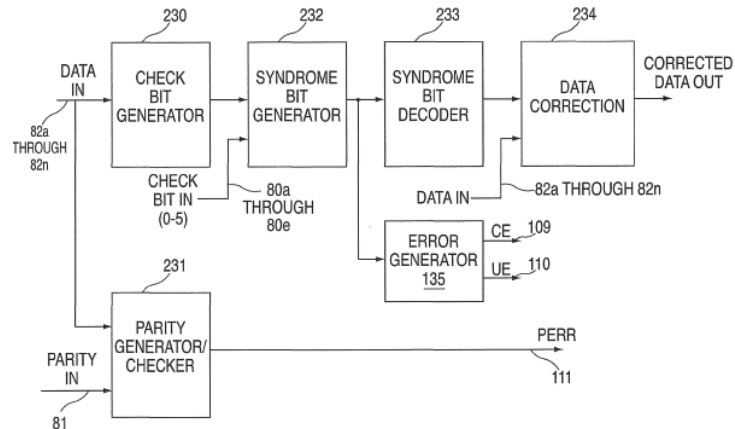
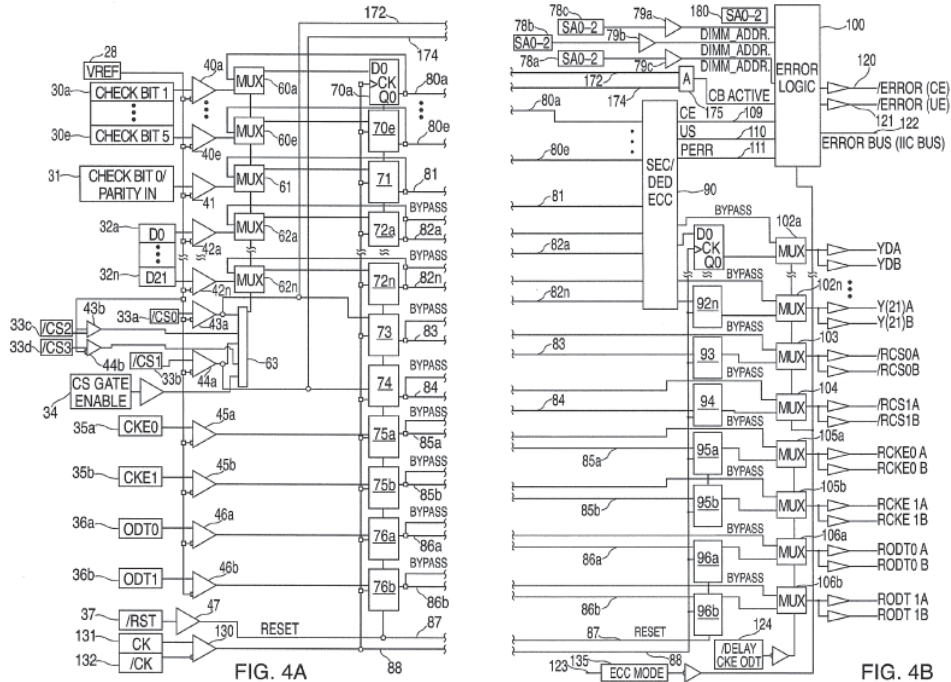
188. Accordingly, Hazelzet discloses “*dynamic random access memory elements on the printed circuit board.*”

d) [1.d] Module Controller ... Having An Open Drain Output

189. Claim 1 requires “*a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection.*”

190. Hazelzet discloses an “ECC/Parity register,” which is the claimed “*module controller*,”⁹ having an output for uncorrectable errors (shown in FIG. 4B as “/ERROR (UE) 121”), which is the claimed “*open drain output*.” Ex. 1014 (Hazelzet) at FIGS. 3A-3D, 4A, 4B, 5, ¶¶[0044], [0059], [0072]. As shown in FIGs. 3A, 3B, 3C, and 3D, the “ECC/Parity register” is on the “printed circuit board” and coupled to the “synchronous dynamic random access memories (SDRAMs).” Ex. 1014 (Hazelzet) at FIGs. 3A-3D, ¶[0015] (“The DIMM of the present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface.”), ¶[0039] (“Further, as shown in FIG. 3A on the front of each DIMM 20, in addition to the DRAMs, there is positioned a phase locked loop (PLL) chip 24 and the novel ECC/Parity Buffer chip 21 of the present invention.”), ¶[0042].

191. FIGS. 4A and 4B of Hazelzet show the “ECC/Parity register” of FIGS. 3A-3D in greater detail, and FIG. 5 of Hazelzet shows the “single error correction / double error detection error correction code (SEC/DED ECC) circuit of FIG. 4B.” Ex. 1014 (Hazelzet) at ¶¶[0027], [0028].



192. As shown in FIG. 4B, the “SEC/DED ECC” circuit is coupled to an “ERROR LOGIC” 100, both of which being part of the “ECC/Parity register” (*i.e.*, “*module controller*,” as claimed). The “ERROR LOGIC” of the “ECC/Parity register” (*i.e.*, “*module controller*,” as claimed) is coupled to an “error reporting

circuitry” with two “open drain outputs,” one for correctable errors “CE” (120 of FIG. 4B) and another for uncorrectable errors “UE” (121 of FIG. 4B). Ex. 1014 (Hazelzet) at FIG. 4B, ¶[0072] (“Error reporting circuitry is included to permit external monitoring of DIMM operation. Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of /Error (UE) is different in parity mode vs. ECC mode.”). The output for uncorrectable errors (shown in FIG. 4B as “/ERROR (UE) 121”) is the “*open drain output*,” as claimed.

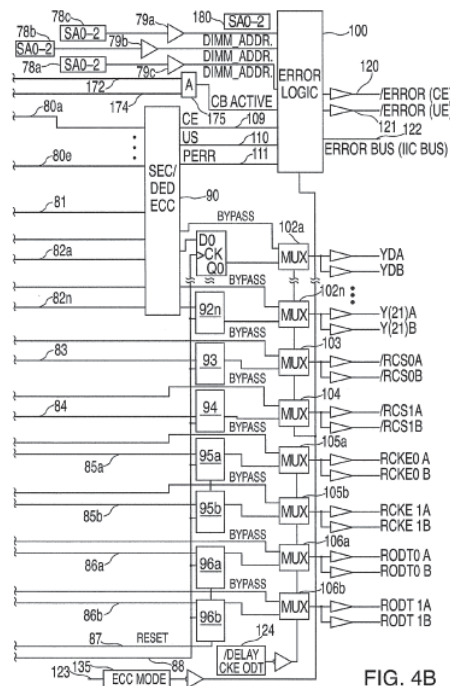


FIG. 4B

193. As explained in claim element [1.b.], the error edge connection is coupled to the open drain output of the module controller. Ex. 1014 (Hazelzet) at FIGs 7A (showing an uncorrectable error pin UE (142) of the memory module that is coupled to the open drain output “/Error (UE)” 121); *see also id.* at FIG. 4B, ¶¶[0059],[0072].

194. Accordingly, Hazelzet discloses *a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection.*”

e) [1.e] Wherein Clauses

195. Claim 1 requires “*wherein the memory module is configurable to operate in any of at least a first mode and a second mode; wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences.*”

(1) [1.e.i] Two Modes

196. Hazelzet explains that its memory modules are configurable to operate in (1) a “parity mode,” which is the claimed “*first mode*,” and (2) an “ECC mode.” Ex. 1014 (Hazelzet) at FIG. 8; see also *id.* at ¶¶[0020], [0022], [0049], [0059]-[0062], [0064], [0069]-[0070], [0072], [0075]. Hazelzet uses the term “mode” in accordance with the plain and ordinary meaning, Ex. 1014 at FIG. 8, ¶¶[0044], [0049], [0059]-[0065], [0069]-[0072], [0075], and therefore its “parity mode” satisfies the plain and ordinary meaning of the claim term “*mode*.” The combination of Hazelzet and Buchmann or, alternatively, Hazelzet and JEDEC DDR3, would add a “*second mode*” as claimed to the module. The combined

module would therefore be configurable to operate in either mode, as it would enter either mode when instructed to do so by the appropriate control inputs. See ¶¶153-156.

(2) [1.e.ii] Normal Reads and Writes

197. Hazelzet discloses that “as shown in this FIG. 2, the memory interface chip 18 sends and receives data from the DIMMs via the data line 15 and sends address and commands via line 16.” EX1014, ¶[0038]; FIG. 2. The figure shows line 15 coupling the memory controller and the DRAMs, and line 16 coupling the memory controller and the register 21. *Id.* A Skilled Artisan would also understand from Figure 2 that lines 15 and 16 are coupled to edge connectors for data and address/control, respectively, since those lines coupled the DIMM to the memory controller. EX1014, FIGs. 2, 7A-7B, ¶¶[0015],[0035], [0038],[0041]. Hazelzet therefore discloses that the module is configurable to receive address and control signal via the edge connections included on the module for that purpose.

198. A Skilled Artisan would understand that such operations – communicating data with DRAMs while communicating address and command information with the register – to constitute “*normal memory read or write operations*” because they follow the standard configuration for such operations with a JEDEC compliant device, EX1014, ¶[0044, including sending address and control to the register and data to the DRAMs. EX1024, 1, 14, 16.

199. Hazelzet additionally explains that its “parity mode” is an “operating mode” with “no correction of errors.” Ex. 1014 (Hazelzet) at ¶[0064] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”), ¶[0103] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”); *see also id.* at ¶[0020] (“Still further the present invention permits operation of the memory module in parity mode, such that unused ECC check bit inputs are held at a low level thus ensuring that these inputs are at a known and quiescent state.”); ¶[0072] (“Error reporting circuitry is included to permit external monitoring of DIMM operation.”); ¶[0070] (“In addition to the above ECC mode, the same twenty two chip select gated data signals can be operated in ‘parity mode (/ECC Mode high), whereby the signal received on CHK0/Parity in line is received as parity to the register one clock pulse later than the chip select gated data inputs. The received parity bit is then compared to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. ... No correction of errors will be completed in this mode.”). A Skilled Artisan would understand the phrase “operating mode” to refer to a mode in which the normal memory operations are employed to store data in or read data from the DRAMs of the module.

200. Hazelzet states that “[i]n Parity Mode, the memory interface chip or controller would generate a single parity bit **in conjunction with providing the full address and command field to the module.** The module would re-drive the address and command bits, to the DRAMs, in the next cycle-rather than adding the additional cycle required in ECC mode. Any error on the address and command bus would be reported to the system at a later time, and the potential for recovery from the fail would be small hence this option is undesirable for many applications. The last mode would be to simply operate the memory in a mode with no parity bits and no ECC bits, with neither the added delay due to ECC nor any means to detect a fault on the address/command bus as per the prior art convention now used for these modules.” Ex. 1014 (Hazelzet) at ¶[0075]. A Skilled Artisan would understand “the full address and command field” in this context to refer to the signals sent to a memory module during a normal read or write operation. See, e.g., Ex. 1024, JEDEC Standard, Double Data Rate (DDR) SDRAM Specification, JESD79 (June 2000) (“JESD79”) at page 14 (“The READ command is used to initiate a burst read access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on inputs A0–Ai (where i = 7 for x16, 8 for x8 or 9 for x4) selects the starting column location.” “The WRITE command is used to initiate a burst write access to an active row. The value on the BA0, BA1 inputs selects the bank, and the address provided on

inputs A0–Ai (where i = 7 for x16, 8 for x8 or 9 for x4) selects the starting column location.”), page 16. Such operations include the reception at the module of address and control signals via their respective edge connections, and in response the communication of data signals between the system memory controller and the module DRAMs, which a Skilled Artisan would understand to occur over the data edge connections of the module, with the DRAM being controlled by the module controller. EX1014, ¶[0038]; EX1024, 1.

201. Moreover, I note that Figure 8 of Hazelzet depicts a timing diagram used with his invention and explicitly discloses “Data In” and “Data Out” in parity mode. A Skilled Artisan would understand such movement of data to occur in the context of normal read and write operations. Ex. 1014 (Hazelzet) at FIG. 8.

202. Hazelzet therefore discloses that the address and control signals received by the module over the address/control edge connections are associated with “*normal memory read or write operations.*”

203. Moreover, Hazelzet relates this configuration to both his ECC and parity mode, EX1014, ¶[0038], so a Skilled Artisan would understand these operations occur in parity mode (*i.e.*, “*first mode,*” as claimed).

204. Accordingly, one skilled in the art would have understood Hazelzet’s parity mode to be a normal operating mode in which the module can be made, via the appropriate signaling, to perform “*one or more normal memory read or write*

operations,” which include the communication of data with the memory controller (over edge connections provided for that purpose) and in response to address and control signals (received over edge connections provided for that purpose).

205. Further, FIG. 2 of Hazelzet discloses that address and command bits are driven to the DRAMs from the memory interface chip through the “ECC/Parity register” (*i.e.*, “*module controller*,” as claimed) using the address and command line (*i.e.*, “add/cmd line 16”) regardless of which mode the memory module is in (*i.e.*, including the “parity mode”). Ex. 1014 (Hazelzet) at ¶[0038], FIG. 2, FIGs 7A-7C (showing address edge connections including pins 67, 70, 72-75, 82, 205-207, 210-213, 220, 227 and command edge connections including pins 86, 89, 91, 93), ¶[0072] (referring to “/CS” as commands), ¶[0068] (listing various control signals including “chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE)” signals); Ex. 1024 (JESD79) at page 13 (TRUTH TABLE 1a).

206. Accordingly, Hazelzet discloses “*wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections.*”

207. To the extent one might argue that Hazelzet does not sufficiently disclose this wherein clause, it would have been obvious to include those claim requirements in the system of Hazelzet. In fact, Hazelzet describes how its “parity mode” is an “operating mode” with “no correction of errors.” Ex. 1014 (Hazelzet) at ¶¶[0064], [0070]. In addition, Hazelzet states that “[i]n Parity Mode, the memory interface chip or controller would generate a single parity bit in conjunction with providing the full address and command field to the module.” Ex. 1014 (Hazelzet) at ¶¶[0075]. Normal read and write operations were known in the prior art. EX1024, 14, 16. Based on these disclosures, a Skilled Artisan would have at least found it obvious to modify Hazelzet’s “parity mode” into the claimed “*first mode*” involving a normal read or write operation over the claimed edge connections because to do so would have permitted normal memory operations, the ultimate purpose of any memory module, using the existing and therefore convenient connections disclosed in Hazelzet and because it would have been common sense to do so. See, e.g., Ex. 1024 (JESD79) at page 14, page 16. This is confirmed by the passage’s reference to a third mode without ECC or parity where the register would simply be “operat[ing] the memory,” which a Skilled Artisan would also understand to refer to the usual memory operations such as reading and writing. Ex. 1014 (Hazelzet) at ¶¶[0075]; see also *id.* at FIG. 8 (depicting a timing diagram

used with his invention and explicitly discloses “Data In” and “Data Out” in parity mode).

208. Accordingly, the “*wherein the memory module in the first mode is configurable to perform one or more normal memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections*” limitation would have been obvious in view of Hazelzet.

209. On the other hand, while the memory module is in the “ECC mode,” the “ECC/Parity register” (i.e., “*module controller*,” as claimed) generates a notification signal that is “low, for two clocks,” and outputs the notification signal to the memory controller of the host system through the “/Error (UE)” 121 pin if/when an uncorrectable error is detected. Ex. 1014 (Hazelzet) at ¶[0059] (“When either [correctable] error line (CE) 109 or uncorrectable error line (UE) 110 is low this indicates that an error was identified as being associated with the address and/or command inputs (either correctable or uncorrectable). The error lines 120,121 will be active, i.e., low, for two clock cycles simultaneous with the re-driven address/command data when operating in ECC mode or delayed by two clock cycles when operating in parity mode.”), ¶[0072] (“Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle

(consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of /Error (UE) is different in parity mode vs. ECC mode.”), FIG. 2, FIG. 4B, FIG. 7A (showing that the UE pin of the memory module is coupled to the memory controller of the host system using pin number 142).

210. Hazelzet’s notification signal from the “ECC/Parity register” (*i.e.*, “buffer chip”) indicates the status of the error correction sequence when the memory module is in the “ECC mode,” by indicating (1) whether “an error was identified” and (2) whether the error from the memory module is an “uncorrectable error.” Ex. 1014 (Hazelzet) at ¶¶[0059] (“When either [correctable] error line (CE) 109 or uncorrectable error line (UE) 110 is low this indicates that an error was identified as being associated with the address and/or command inputs (either correctable or uncorrectable). The error lines 120,121 will be active, *i.e.*, low, for two clock cycles simultaneous with the re-driven address/command data when operating in ECC mode or delayed by two clock cycles when operating in parity mode.”), [0069], [0072], FIG. 2, FIG. 4B, FIG. 7A; *see also id.*, at ¶[0092] (“As shown in configuration 902, outputs from the buffer chip 21 include an indication

of whether the error is a correctable error (CE) or an uncorrectable error (UE) as well as the corrected (if error is correctable) command and address information, which connect to memory devices 22.”).

(3) [1.e.iii] Not Accessed

211. This claim also requires “wherein the memory module in the second mode is not accessed by the memory controller for normal memory read or write operations.” As noted above, the combinations analyzed here include JEDEC or Buchmann training sequences in a training mode wholly separate from any mode that includes normal memory operations in response to memory controller commands and it would have been obvious to make the combinations in that manner. See ¶¶153-156. Moreover, I note that neither Hazelzet, JEDEC, nor Buchmann disclose normal memory read or write operations in response to memory controller commands occurring in a training mode of the combinations analyzed. The combination therefore satisfies this claim language.

(4) [1.e.iv] Training Sequences

212. As explained above, see ¶¶153-156, the combinations analyzed here includes a separate training mode into which the module can be placed and in which the module can implement various training sequences (*e.g.*, Write Leveling and Read Enable Training per JEDEC/TS0 and TS3 per Buchmann) (“*operations related to one or more training sequences*”). Each of those operations includes a

set of operations occurring in a particular order, used for training a memory module. For instance, a Skilled Artisan would understand “‘Write Leveling’ to the DRAMs to ensure successful writes, and ‘Read Enable Training’ to ensure it can capture read data from the DRAMs correctly,” as each including a set of operations occurring in a particular order to train the memory module. EX1015 at 8; EX1040, 14:1-15:3; EX1018, Fig. 4. For example, a Skilled Artisan would understand operations described on page 8 of EX1039 to be operations performed in a particular order during MB-DRAM Training’s “‘Write Leveling,’” and the operations described on page 9 of EX1039 to be operations performed in a particular order during MB-DRAM Training’s “‘Read Enable Training.’” Likewise, a Skilled Artisan would understand the various operations set forth in Buchmann as performed during the TS0 and TS3 operations as each including a set of operations occurring in a particular order to train the memory module. EX1016, FIGs. 4,6, 5:51-7:2,8:24-9:18. See for example the operations described in Table 1 of Buchmann, for TS0, and in Table 5 of Buchmann, for TS3. The combinations therefore satisfy this claim element.

f) [1.f] Operation Of Module Controller In the First Mode

213. Claim 1 requires “*wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations, wherein the*

dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode.”

214. As explained in claim elements [1.b] and [1.e.], Hazelzet’s module can be placed into a parity mode, which is a normal operating mode in which the module is provided, over the edge connections identified for that purpose, address and control signals for performing “*one or more normal memory read or write operations.*” Ex. 1014 (Hazelzet) at FIGs. 2, 7A-7B, ¶¶[0015],[0035],[0038],[0041],[0064], [0070]; *see also* Ex. 1024 (JESD79) at page 14, page 16. For example, Hazelzet discloses providing “the full address and command field to the module” during parity mode, which a Skilled Artisan would understand to refer to the normal signaling that implements a memory read or write from a memory controller. EX1014, ¶[0075]. In addition, as further explained in claim element [1.e.], FIG. 2 of Hazelzet discloses that address and command bits are driven to the DRAMs from the memory interface chip through the “ECC/Parity register” (*i.e.*, “*module controller,*” as claimed) using the address and command line (*i.e.*, “add/cmd line 16”) in the “parity mode.” Ex. 1014 (Hazelzet) at ¶[0038]

(“The memory interface chip 18 then sends and receives data, via line 15, to the memory devices, or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16 and check bits for error correction purposes to the ECC/ Parity register chip 21 via line 25.”), FIG. 2; *see also id.* at FIGs 7A-7C (showing address edge connections including pins 67, 70, 72-75, 82, 205-207, 210-213, 220, 227 and command edge connections including pins 86, 89, 91, 93), ¶[0072] (referring to “/CS” as commands), ¶[0068] (listing various control signals including “chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE)” signals). Given that the “write enable (WE)” is an exemplary control signal “*associated with the one or more normal memory read or write operations,*” *id.*; Ex. 1024 (JESD79) at page 13 (TRUTH TABLE 1a), Hazelzet satisfies the “*wherein the module controller is configurable to receive via the second edge connections the address and control signals associated with the one or more normal memory read or write operations*” limitation.

215. Moreover, as explained in claim elements [1.b.] and [1.e.], Hazelzet discloses that the printed circuit board has a first set of edge connections for communicating data signals between the dynamic random access memory elements (within the memory module) and the memory controller of the host system, Ex. 1014 (Hazelzet) at FIGs 7A-7C (showing data edge connections including pins 11,

12, 17, 18, 22, 23, 31, 32, 37, 38), while the memory module is in the “parity mode,” *id.* at FIG. 8 (showing “Data In” and “Data Out” in both the “parity mode” and the “ECC mode.”); *see also id.* at FIGs. 3A-3D, ¶[0015] (“The DIMM of the present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface.”), ¶[0035],[0038],[0041]. Further, as explained in claim element [1.e.], data communication between the memory module and the memory controller is “*in accordance with the address and control signals.*” *See, e.g.,* Ex. 1014 (Hazelzet) at FIGs 2,8, ¶¶[0015],[0035],[0038], [0041],[0064],[0070]; Ex. 1024 (JESD79) at page 13 (TRUTH TABLE 1a). Accordingly, Hazelzet satisfies the “*wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals*” limitation.

216. As explained in claim elements [1.b.] and [1.d.], the error edge connection is coupled to the open drain output of the module controller. Ex. 1014 (Hazelzet) at FIGs 7A (showing an uncorrectable error pin UE (142) of the memory module that is coupled to the open drain output “/Error (UE)” 121); *see also id.* at FIG. 4B, ¶¶[0059],[0072].

217. In particular, Hazelzet's "ECC/Parity register" (*i.e.*, "*module controller*," as claimed) includes an "SEC/DED ECC" 90. Ex. 1014 (Hazelzet) at FIG. 4B. FIG. 5 of Hazelzet, which is a block diagram of the "SEC/DED ECC" 90 in FIG. 4B, includes a "parity generator/checker circuit 231." Ex. 1014 (Hazelzet) at ¶¶[0028], [0076], FIG. 5.

218. When the memory module is in the "parity mode" (*i.e.*, "*first mode*," as claimed), the "parity generator/checker circuit 231" generates and sends the "parity error signal (PERR)" to the "error logic circuit" 100. Ex. 1014 (Hazelzet) at ¶[0076] ("FIG. 5 is a block diagram of the SEC/DED ECC circuit of FIG. 4B. ... The parity generator/checker circuit 231 further has a second input coupled to the parity in signal source 31 via primary latch 71 and output line 81 and depending on the state of the parity input signal on input 31 sends a parity error signal (PERR) on output line 111 to the error logic circuit 100."), FIG. 5; *see also* Ex. 1014 (Hazelzet) at ¶[0070] ("In addition to the above ECC mode, the same twenty two chip select gated data signals can be operated in 'parity mode (/ECC Mode high)', whereby the signal received on CHK0/Parity in line is received as parity to the register one clock pulse later than the chip select gated data inputs. The received parity bit is then compared to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. The twenty two chip select gated data signals will be latched and re-driven on the first

clock pulse and any error will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses) and in the Error Bus Registers. No correction of errors will be completed in this mode. The convention of parity, in this application, is odd parity (odd numbers of 1s [*sic*] across data and parity inputs equals valid parity).”), FIG. 4B.

219. In the “parity mode” (*i.e.*, “*first mode*,” as claimed), the “parity error signal (PERR)” 111 that is fed into the “error logic circuit” 100 is used to drive the open-drain transistor in “error logic circuit” 100, which outputs to the memory controller through the output line 121 (*i.e.*, output for uncorrectable error “UE”). Ex. 1014 (Hazelzet) at ¶[0059] (“This SEC/DED ECC circuit 90 provides three outputs 109, 110, and 111 to the error logic circuit 100. These outputs are: a correctable error (CE) line 109, an uncorrectable error (UE) line 110 and a parity error bit line 111 fed to the error logic circuit 100 which provides outputs regarding correctable and uncorrectable errors on output lines 120 and 121. When either [correctable] error line (CE) 109 or uncorrectable error line (UE) 110 is low this indicates that an error was identified as being associated with the address and/or command inputs (either correctable or uncorrectable). The error lines 120,121 will be active, *i.e.*, low, for two clock cycles simultaneous with the re-driven address/command data when operating in ECC mode or delayed by two clock cycles when operating in parity mode.”).

220. As explained above, the output line 121 (“UE”) is an open-drain output, Ex. 1014 (Hazelzet) at ¶¶[0072], which is coupled to the memory controller of the host system using pin number 142. Ex. 1014 (Hazelzet) at FIG. 7A (showing that the “Server PIN Number 142” corresponds to “DIMM PIN Name UE”), FIG. 2 (showing how the “DIMM 20” is coupled to the “Memory Controller or Processor 19”); *see also id.* at ¶[0016] (“More particularly the server of the present invention comprises a novel DIMM provided with a new and unique ECC/ Parity Register that is operable with 1 to 4 memory ranks, coupled to a memory interface chip which is in turn coupled to a memory controller or processor such that the memory controller sends address and command information to the buffer (or register) via address/command lines together with check bits for error correction purposes to the ECC/ Parity register.”), ¶[0038] (“In this FIG. 2 the server comprises a novel DIMM 20 provided with a novel ECC/Parity Buffer chip 21 (also referred to as a ‘buffer device’) coupled to the memory interface chip 18 which is in turn coupled to the memory controller or processor 19.” “In this configuration, the check bits and/or parity bits associated with the ECC/Parity register chip 21 are developed in the memory interface chip 18, although in other embodiments these bits could be developed in the memory controller or processor 19, be communicated to the memory interface chip as a subset of the information

on line 16 and the memory interface would then re-drive this information to the memory module on line 25”).

SERVER DIMM PIN NUMBER	PIN NAME	SERVER DIMM PIN NUMBER	PIN NAME
1	Vref	139	Vref
2	SCL	140	SCL
3	SDA	141	SDA
4	UE	142	UE
5	CE	143	CE
6	VDD	144	VDD
7	ECCMODE	145	ECCMODE
8	DLY CKE/ODT	146	DLY CKE/ODT
9	CS GATE EN	147	CS GATE EN
10	GND	148	GND
11	DQ0	149	DQ4
12	DQ1	150	DQ5
13	GND	151	GND
14	DQS0*	152	DQS9
15	DQS0	153	DQS9*
16	GND	154	GND
17	DQ2	155	DQ6
18	DQ3	156	DQ7
19	GND	157	GND
20	VDD	158	VDD
21	GND	159	GND
22	DQ8	160	DQ12
23	DQ9	161	DQ13
24	GND	162	GND
25	DQS1*	163	DQS10
26	DQS1	164	DQS10*
27	GND	165	GND
28	DQ10	166	DQ14
29	DQ11	167	DQ15
30	GND	168	GND
31	DQ16	169	DQ20
32	DQ17	170	DQ21
33	GND	171	GND
34	DQS2*	172	DQS11
35	DQS2	173	DQS11*
36	GND	174	GND
37	DQ18	175	DQ22
38	DQ19	176	DQ23
39	GND	177	GND
40	RESET	178	RESET
41	VDD	179	VDD
42	GND	180	GND
43	DQ24	181	DQ28
44	DQ25	182	DQ29
45	GND	183	GND
46	DQS3*	184	DQS12
47	DQS3	185	DQS12*
48	GND	186	GND
49	DQ26	187	DQ30
50	DQ27	188	DQ31
51	GND	189	GND
52	CB0	190	CB4

FIG. 7A

221. Hazelzet explains that the generated parity error signal is driven to the memory controller of the host system. Ex. 1014 (Hazelzet) at ¶[0044], FIG. 2 (showing that the signals generated by the “DIMM 20” is driven to the “Memory Controller or Processor 19” through data paths 15 and 15a), ¶[0036] (“Each DRAM 11 on the DIMM 10 has a plurality of input/output pins that are coupled, via the printed circuitry on the DIMM 10 to the contacts on the DIMM 10 and theses contacts are further coupled, via a data line 15, to a memory interface chip

18 and to a memory controller or processor 19.”); *see also id.* at ¶[0072] (“Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of /Error (UE) is different in parity mode vs. ECC mode.”).

222. Hazelzet explains that the “parity operating mode” is a mode that allows the host system to “determine the error condition” of the memory module. Ex. 1014 (Hazelzet) at ¶[0064] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”). Hazelzet further explains that such “error condition” is reported to the host “via the Uncorrectable Error (UE) line” when the memory module is in the “parity mode.” Ex. 1014 (Hazelzet) at ¶[0070] (“In addition to the above ECC mode, the same twenty two chip select gated data signals can be operated in 'parity mode (/ECC Mode high)', whereby the signal received on CHK0/Parity in line is received as parity to the register one clock pulse later than the chip select gated data inputs. The received parity bit is then compared

to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. The twenty two chip select gated data signals will be latched and re-driven on the first clock pulse and any error will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses) and in the Error Bus Registers. No correction of errors will be completed in this mode. The convention of parity, in this application, is odd parity (odd numbers of 1s [sic] across data and parity inputs equals valid parity).”). Hazelzet further explains that the error line is driven “low, i.e., ‘0’,” when “an error is detected.” Ex. 1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.”), ¶[0018] (“Still another object of the invention is to provide for Parity error reporting in which the parity signal is delivered one cycle after the address and command to which it applies, and the error line be driven low two clocks after the address and command bits are driven to the DRAMs from the

register on the DIMM.”), FIG. 8 (explaining that UE is driven low “if an error occurs” in the “parity mode”).

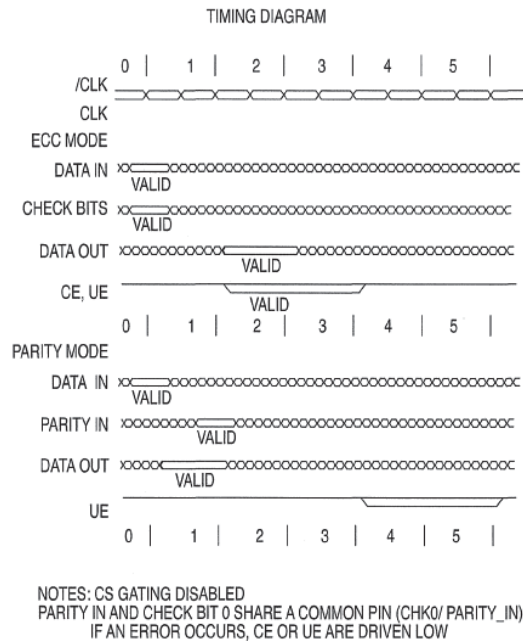


FIG. 8

223. Accordingly, Hazelzet discloses “wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred while the memory module is in the first mode.”

g) [1.g] Operation Of Module Controller In The Second Mode

224. Claim 1 requires “wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection to a first

state or to a second state, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.”

225. As demonstrated above, ¶¶153-156, in the combinations analyzed here, the Hazelzet module would be modified to be configurable to enter a training mode and output JEDEC or Buchmann training status signals to the system memory controller via the open drain output UE 121. *Id.* Each of the status signals analyzed above (ERROUT#, TS0_done, TS3_ack, TS3_done) represent “*information related to the one or more training sequences*” because each provides status about the related sequences, such as whether it has been completed or whether all memory buffers have returned an acknowledgement. *Id.* Each of these combinations therefore alternatively satisfies “*wherein the module controller in the second mode is further configurable to provide information related to the one or more training sequences.*”

226. Moreover, Hazelzet’s memory system involves sharing the open drain output so that the memory controller of the host system can receive parity error signals/notification signals from multiple memory modules using the open drain output. *See, e.g.,* Ex. 1014 (Hazelzet) at ¶¶[0018] (“After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared

by multiple modules.”), [0072] (“Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals).”), [0099], [0109]; *see also* ¶¶ 147-152, *above*.

227. As noted above, in the combinations analyzed here, the training status signals would be at a low logic level (because the gate signals of the transistors in the open drain circuits in all the modules in which the training is ongoing are high) over an open drain output of Hazelzet until such time as the operations they related to completed for all modules of the system and the gate signals to the transistors of all the open drain circuits in all the modules are low, at which time the signals would be at a high impedance state, indicating completion. EX1017, FIG. 4; 5:65-6:12 (illustrating and describing how such a system as is in Hazelzet operates); EX1001, 9:47-10:50 (explaining in same way as Kim functioning of open-drain outputs in memory systems). As I note above, ¶¶ 153-156, it would have been obvious to use Hazelzet’s open drain signaling for these particular training signals because each indicates when operations carried out by multiple modules have completed. The high and low gate signals to the transistors represent “*driving the open drain output and the error edge connection to a first state or to a second state*,” respectively or vice versa.

228. A Skilled Artisan would understand that, in the obvious combinations analyzed here, such open drain signals would be changed from a high impedance state to a low state as the gate of the transistor changes from a low to a high to indicate the related training operations were in progress, and changed from a low state to a high impedance state as the gate of the transistor driving the signal changes from a high to a low to indicate when the related operations completed in each memory module. Ex. 1014 (Hazelzet) at ¶¶ [0059], [0070], [0072], FIG. 4B; EX1017, FIGs. 4-5; 5:65-6:18 (teaching how a shared error pin can be implemented using an open drain configuration and/or an OR-gate); EX1015 (JEDEC), 8; Ex. 1016 (Buchmann) at 5:51-7:2, Table 1, Table 2, FIG. 4, 8:24-9:18, Table 5, Table 6, FIG. 6, 8:24-9:17, 3:52-54, 27:18-21, 26:30-32; *see also* ¶¶ 147-152.

229. Each combination therefore alternatively satisfies “*one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state.*”

2. Claim 2 is Unpatentable

230. Claim 2 requires “[t]he memory module of claim 1, wherein the module controller comprises an integrated circuit.”

231. Hazelzet’s “ECC/Parity register” (i.e., “module controller,” as claimed) is also referred to as a “buffer device” or a “buffer chip.” Ex. 1014

(Hazelzet) at ¶[0038]. Hazelzet further explains that the module support devices, including “buffers” (i.e., “*module controller*,” as claimed), “registers,” and “PLL” may be comprised of “multiple separate chips” or may be “combined onto a single package or even integrated onto a single device.” Ex. 1014 (Hazelzet) at ¶[0115]; *see also id.* at FIG. 3A-3D, ¶[0039] (“It should be understood that the PLL chip 24 can be eliminated if its circuitry is provided on the buffer chip 21 or within the same package as the buffer chip 21.”), ¶[0042]. Accordingly, Hazelzet discloses that “*the module controller comprises an integrated circuit*,” as claimed.

232. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy the “*wherein the module controller comprises an integrated circuit*” limitation.

3. Claim 3 is Unpatentable

233. Claim 3 requires “[t]he memory module of claim 1, wherein the module controller includes a notification circuit comprising a transistor having an open drain coupled to the open drain output and source coupled to the ground.”

234. As explained in claim element [1.d.], Hazelzet discloses that the “ECC/Parity register” (i.e., “*module controller*,” as claimed) has “open drain output[s].” Hazelzet further explains that the “ECC/Parity register” has an “error correction code circuit ECC segment 21b,” which is a “*notification circuit*,” as claimed, because it outputs signals notifying the system memory controller of

correctable, uncorrectable, and parity errors. Ex. 1014 (Hazelzet) at ¶[0044] (explaining that the “error correction code circuit ECC segment 21b” is within the “ECC/Parity buffer chip 21,” i.e., “ECC/Parity register”). Such “error correction code circuit ECC segment 21b” (within the “ECC/Parity register”) includes the circuitry for determining whether the errors occurred, SEC/DED ECC circuit 90, and error logic circuit 100 that receives error signals from SEC/DED ECC circuit 90, such as UE 110 and PERR 111, and provides the above-mentioned “open-drain output(s),” such as UE 121. Ex. 1014 (Hazelzet) at FIG 4B, ¶¶[0059],[0072] (“Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of /Error (UE) is different in parity mode vs. ECC mode.”).

235. Hazelzet discloses that those “open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error,” and further discloses that the “outputs are driven low for two clocks to allow the memory controller time to sense the error. ... /Error (UE) indicates that an

uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error.”). Further, Hazelzet explains that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” Ex. 1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.”).

236. As noted above, the combinations analyzed here include a field effect transistor. Indeed, a Skilled Artisan would have understood the phrase “open drain” in the context of Hazelzet’s disclosures to necessarily mean the output is driven by a field effect transistor (as opposed to an open collector configuration), and that field effect transistors have three terminals, i.e., gate, source, and drain, that the drain would be connected to a pull-up resistor, the source to ground and the gate to an OR logic element that OR’ed the UE 110 and PERR 111 error

signals to drive the gate, as depicted in Figure 5 of Kim. EX1017, FIGs. 4-5, 5:65-6:18; *see also generally* Ex. 1020, U.S. 3,414,781 to Dill (“Dill”), entitled “Field Effect Transistor Having Interdigitated Source And Drain And Overlying, Insulated Gate.” A Skilled Artisan would have thus understood that the disclosed “open drain” output is the output of “*a transistor having an open drain*” while the “source” of that transistor is “*coupled to the ground*.” See ¶¶ 147-152; *see also* EX1017 (Kim) at FIG. 4, 5:49-57, 4:40-48; 6:1-16. Furthermore, even if not inherently disclosed, it would have been obvious to a Skilled Artisan to implement in this fashion given the knowledge of a Skilled Artisan regarding open drain outputs. See ¶¶ 147-152.

237. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy “*the module controller includes a notification circuit comprising a transistor having an open drain coupled to the open drain output and source coupled to the ground*” limitation.

238. To the extent one might argue otherwise, claim 3 would have been obvious in view of Hazelzet, JEDEC or Buchmann, and Kim. Kim discloses an “open drain output” that is an output pin coupled to the drain of a transistor, which includes three ports (*i.e.*, a gate, source, and a drain). *See, e.g.*, Ex. 1017 (Kim) at FIG. 4. In particular, FIG. 4 of Kim shows an open drain output that is coupled to a pull-up resistor (*i.e.*, connected to a high voltage via a pull-up resistor). FIG. 4 of

Kim also shows that the source of the transistor is coupled to ground and that the gate of the transistor is coupled to “ERR.”

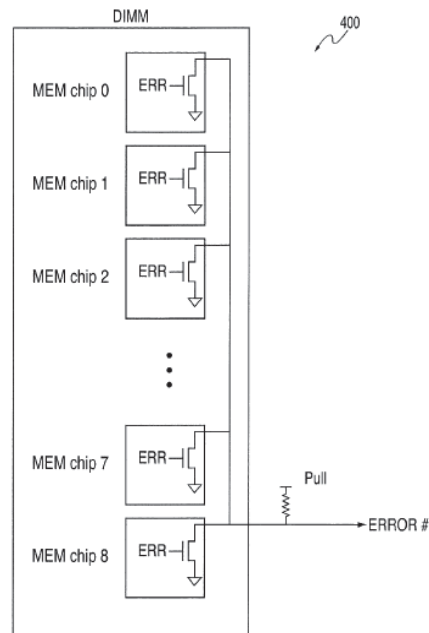


FIG. 4

239. Kim also discloses in Figure 5 the use of a logic element (an OR gate) such that multiple error signals could drive the gate of the open-drain transistor.

EX1017, FIG. 5, 6:13-6:18.

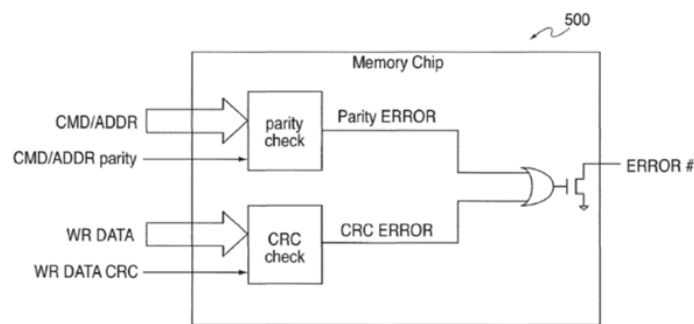
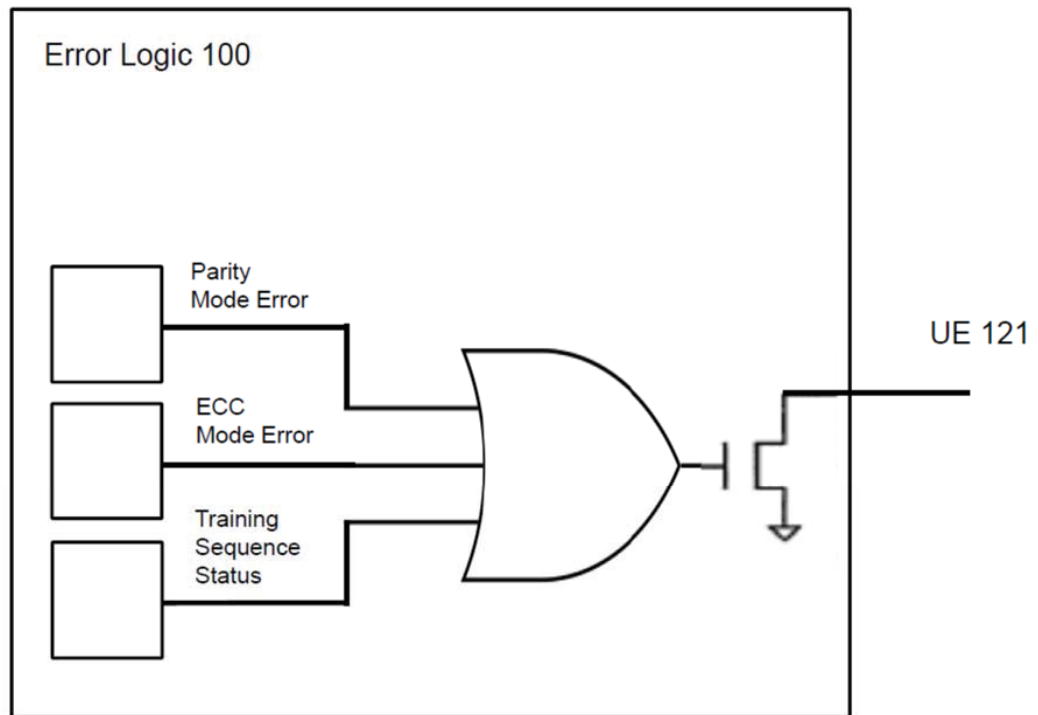


FIG. 5

240. In the combinations analyzed here, Kim's open drain transistor configuration would be included within Hazelzet's error logic 100 (which is part of the ECC segment 21b – a “*notification circuit*” as claimed) such that signals indicating parity mode error, ECC mode error and training status would be provided to a logic gate, such as an OR gate, as in Kim, which would select among them based on the mode of the module, as in Hazelzet. The output of the OR gate would be coupled to, and would drive, the gate of an open drain transistor, which itself drives UE 121, as shown in the annotation below:



241. As in Hazelzet, UE 121 is coupled to an error edge connector.

242. As I note above, Hazelzet discloses that UE 121 is used in both Parity Mode and ECC Mode, so there is necessarily logic circuitry within Error Logic 100 for selecting which signal to use to drive the open drain output. Kim uses an OR gate for that function, as in this combination, but a multiplexor would have also worked. It would have been obvious and common sense to use a three input OR gate here, since there are three modes in the modified version of Hazelzet.

243. A Skilled Artisan would understand that, in this combination, each signal input the OR gate would remain low when the module was not in its associated mode, and the signal whose mode was active could be high to indicate the occurrence of the event to be signaled (error in Parity Mode or ECC Mode; ongoing training in Training Mode), or low to indicate that the event is not occurring (Parity/ECC) or acknowledge/completed (training). The signal whose mode was active would then be passed through the OR gate to drive the gate of the transistor.

244. I note this is how both Hazelzet and JEDEC employ open drain signaling. For example, Hazelzet discloses that the “ECC/Parity register” (i.e., “*module controller*,” as claimed) has “open drain output[s].” Ex. 1014 (Hazelzet) at ¶[0072]. Hazelzet further explains that the “ECC/Parity register” has an “error correction code circuit ECC segment 21b,” which is a “*notification circuit*,” as claimed, because it outputs signals notifying the system memory controller of

correctable, uncorrectable, and parity errors. Ex. 1014 (Hazelzet) at ¶[0044]. Such “error correction code circuit ECC segment 21b” (within the “ECC/Parity register”) includes the circuitry for determining whether the errors occurred, SEC/DED ECC circuit 90, and error logic circuit 100 that receives error signals from SEC/DED ECC circuit 90, such as UE 110 and PERR 111, and provides the above-mentioned “open-drain output(s),” such as UE 121. Ex. 1014 (Hazelzet) at FIG 4B, ¶¶[0059],[0072]. Hazelzet discloses that those “open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error,” and further discloses that the “outputs are driven low for two clocks to allow the memory controller time to sense the error. ... /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error.”). Further, Hazelzet explains that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” Ex. 1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for

only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.”).

245. Based upon these disclosures, a Skilled Artisan would have understood Hazelzet’s open drain outputs to necessarily driven by a field effect transistor (as opposed to an open collector configuration), that field effect transistors have three terminals, *i.e.*, gate, source, and drain, that the drain would be connected to a pull-up resistor, the source to ground and the gate to an OR logic element that OR’ed the UE 110 and PERR 111 error signals to drive the gate, as depicted in Figure 5 of Kim. EX1017, FIGs. 4-5, 5:65-6:18.

246. Also, as explained above, see ¶152, a Skilled Artisan would have understood that an open drain output as set forth in the figure above would be pulled to a high logic level when the gate of the transistor is low, because the transistor would be off. *See, e.g.*, Ex. 1017 (Kim) at FIG. 4. The output would then be in an un-driven, high impedance, state. Ex. 1014 (Hazelzet) at ¶[0099]. On the other hand, the open drain output would switch to a low logic level (*e.g.*, ground), and be put in a low impedance state, when the gate of the transistor is high, because the transistor would be on. *Id.*

247. In this combination, as shown in the annotated figure above, the module controller would therefore include “*a notification circuit comprising a*

transistor having an open drain coupled to the open drain output and source coupled to the ground.”

248. A Skilled Artisan would have been motivated to combine Kim into the obviousness combination of Hazelzet and JEDEC or Buchmann for various reasons. Kim was filed approximately a year and a half after Hazelzet and includes some of the same disclosures. It discloses additional details regarding the use of an open-drain output on a memory module to notify the memory controller of errors during a parity normal operating mode and during an ECC normal operating mode. EX1017(Kim) at 1:16-22;5:49-57;6:8-16. To use the output-pin scheme of Kim in the system of Hazelzet would therefore have been only the use of known techniques for their known purposes to achieve predictable results, *i.e.*, using an open-drain output to provide error or status information from multiple components.

249. Kim and Hazelzet/JEDEC/Buchmann are analogous art to the 595 Patent because each is directed to the field of memory module design, including error detection and correction, initialization, training and the use of pins/paths for multiple purposes during different operations/modes, EX1001, Abstract, 5:66-6:14;8:4-48; EX1014, Abstract, ¶¶[0007],[0069]-[0070],[0123]; EX1015, 1, 3, 8; EX1016, 1:7-9;3:49-60;4:51-5:50;12:60-13:41;14:1-63;20:20-21:19;33:45-67; EX1017, 1:16-22;5:49-57;6:8-18;11:20-34;12:36-53, and also because Kim and Hazelzet/JEDEC/Buchmann are reasonably pertinent to the particular problem the

inventor of the 595 Patent was trying to solve, increasing memory module capacity, performance, and/or reliability by sharing an output pin/path to perform multiple functions during multiple operations/modes, including initialization/training, EX1001, Abstract, 5:66-6:14;8:4-48; EX1014, Abstract, ¶¶[0007],[0069]-[0070],[0123]; EX1015, 1, 3, 8; EX1016, 1:7-9;3:49-60;4:51-5:50;12:60-13:41;14:1-63;20:20-21:19;33:45-67; EX1017, 1:16-22;5:49-57;6:8-18;11:20-34;12:36-53.

250. Moreover, a person of ordinary skill in the art would have been motivated to use the open-drain output pin reporting technique of Kim in the combined scheme of Hazelzet and JEDEC or Buchmann because it represented a well-known (and therefore reliable) and simple technique to provide error and/or status information from a number of memory components. *See, e.g.*, Ex. 1014 (Hazelzet) at ¶[0072], ¶[0122]; EX1017, FIGs. 4-5, 5:65-6:18, 12:18-23. The open-drain interrupt reporting technique of Kim permitted a single signal line with an “*OR logic element*” to indicate error or status information, thus simplifying the design of the system and saving pins on the various integrated circuits connected to the bus, which necessarily can have only a finite number of pins. Thus, a person of ordinary skill in the art could readily have modified Hazelzet’s open-drain output with the teachings of Kim and would have been motivated to do so.

251. Accordingly, claim 3 would have been obvious in view of Hazelzet, JEDEC or Buchmann, with or without Kim.

252. This same analysis applies to further combining Hazelzet and JEDEC or Buchmann, with Kim to satisfy the elements of claims 4-7, 12-14, 20, 22, or 23, each of which adds limitations going to details of the implementation of the open-drain output disclosed by Hazelzet, details that Kim explicitly discloses are included as part of an open-drain output circuit. I thus cross-reference this analysis for each of those claims.

4. Claim 4 is Unpatentable

253. Claim 4 requires “[t]he memory module of claim 3, wherein the module controller is configurable to drive a gate of the transistor high so as to drive open drain output and the error edge connection to ground, or to drive the gate of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state.”

254. As demonstrated above, in the combinations analyzed here the open drain output is configured such that the transistor output is driven low (ground) while training is still occurring and driven high upon completion. Moreover, to drive the output low (i.e., ground), the gate of the transistor must be high, causing the transistor to conduct and connect the drain to ground. Conversely, to drive the

output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off. See ¶157.

255. Similarly Hazelzet explains that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” Ex. 1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.”). Accordingly, a Skilled Artisan would have understood that the known open-drain output for such a system, such as disclosed in Kim, was used in Hazelzet, see ¶¶150-152, *above*, and that Hazelzet’s open drain output would be left floating (i.e., high impedance state) when the gate of the transistor is low, because the transistor would be off. Ex. 1014 (Hazelzet) at ¶[0099]; see ¶¶150-152, *above* ; Ex. 1017 (Kim) at FIG. 4. On the other hand, Hazelzet’s open drain output would switch to a low logic level

(e.g., ground) when the gate of the transistor is high, because the transistor would be on. *Id.* See ¶¶ 147-152.

256. Accordingly, one skilled in the art would have known that the open drain output along with the edge connection connected to the open drain output would both be driven to ground when the gate is driven high. See analysis in claim element [1.g.] and claim 3; Ex. 1014 (Hazelzet) at ¶[0099]; see ¶¶147-152; see also Ex. 1017 (Kim) at FIGs. 4-5, 5:65-6:18. Likewise, one skilled in the art knew that the open drain output along with the edge connection connected to the open drain output would both be driven to a high impedance state (through the pull up resistor) when the gate is driven low. *Id.*

257. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy “*the module controller is configurable to drive a gate of the transistor high so as to drive open drain output and the error edge connection to ground, or to drive the gate of the transistor low so as to drive the open drain output and the error edge connection to the high impedance state*” limitation.

258. To the extent one might argue otherwise, the module controller of the obvious combination of Hazelzet, JEDEC or Buchmann, and Kim, described above, includes a memory module configurable “*to drive a gate of the transistor high so as to drive open drain output and the error edge connection to ground, or to drive the gate of the transistor low so as to drive the open drain output and the*

error edge connection to the high impedance state” for the reasons set forth in ¶¶243-246 above.

5. Claim 5 is Unpatentable

259. Claim 5 requires “[t]he memory module of claim 4, wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground.”

260. As explained in claim element [1.f.], see ¶¶217-222, above, Hazelzet explains that its “ECC/Parity register” (i.e., “module controller”) has “open-drain output[s]” (i.e., Uncorrectable Error (UE) line[s])” capable of utilizing “parity error signals” (PERR) to output signal UE 121 to the host indicating a parity error. See analysis in claim element [1.f.]; EX1014, ¶¶[0059],[0070],[0072], [0076]. Further, as explained in claim element [1.f.], when the memory module is in the “parity mode” (i.e., “first mode,” as claimed), the “parity generator/checker circuit 231” (within SEC/DED ECC circuit 90) generates and sends the “parity error signal (PERR)” to the “error logic circuit” 100. Ex. 1014 (Hazelzet) at FIGs. 4B-5, ¶¶[0059],[0070],[0072],[0076] (“FIG. 5 is a block diagram of the SEC/DED ECC circuit of FIG. 4B. ... The parity generator/checker circuit 231 further has a second input coupled to the parity in signal source 31 via primary latch 71 and output line

81 and depending on the state of the parity input signal on input 31 sends a parity error signal (PERR) on output line 111 to the error logic circuit 100.”).

261. In particular, Hazelzet explains that in the “parity mode,” the parity error “will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses).” Ex. 1014 (Hazelzet) at ¶[0070]; *see also id.* at [0018] (“After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules.”).

262. Further, as explained in claim 4, *see* ¶254, *above*, Hazelzet discloses that its open-drain output is driven “low” (i.e., to ground) when the driver is enabled (i.e., gate receives a high voltage), and further explains that the open-drain “output [is] permitted to return to an un-driven state (high impedance)” when the “driver [is] disabled.” Ex. 1014 (Hazelzet) at ¶[0099] (“Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., ‘0’ two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.”).

263. Accordingly, Hazelzet discloses that the open-drain output (UE 121) in each memory module is configured to “*output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground.*” See also analysis in claim 4; EX1017, FIGs. 4-5, 5:65-6:18; see ¶¶ 147-152, above.

264. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy the “*wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground*” limitation.

265. To the extent one might argue otherwise, the module controller of the obvious combination of Hazelzet, JEDEC or Buchmann, and Kim, described above, includes a memory module configurable “*to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and the ground,*” for the reasons set forth in ¶¶243-246 above. In particular, the module is “*configurable*” to output the parity error as claimed because it can be configured to be in the Parity Mode.

6. Claim 6 is Unpatentable

266. Claim 6 requires “[t]he memory module of claim 3, wherein the notification circuit further includes a multiplexor or a logic circuit having a output coupled to a gate of the transistor and configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.”

267. As explained in claim 3, Hazelzet’s “error correction code circuit ECC segment 21b” (within the “ECC/Parity register”) is the “notification circuit,” as claimed. See ¶234, above.

268. FIG. 4B of Hazelzet shows the “error correction code circuit segment 21b.” Ex. 1014 (Hazelzet) at ¶[0044],[0059], FIG. 4B. Within Hazelzet’s error correction code circuit ECC segment 21b is “Error Logic 100.” *Id.* Hazelzet discloses that Error Logic 100 receives the “US [sic] 110” signal and the “PERR 111” signal, and outputs one of these signals to the same “/ERROR (UE)” pin depending on which mode the memory module is in. See Ex. 1014 (Hazelzet) at FIG. 4B (showing an open-drain output “/ERROR (UE) 121” for uncorrectable error or parity error, depending on the mode of operation), ¶¶[0072] (explaining that “/Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error.”), ¶¶[0044],[0059],[0069-71]. As set forth above, see ¶¶151, 156, in the

combinations analyzed here, that circuitry would be modified to implement the additional training mode, in which the UE 121 open drain output would, when the module is in the training mode, be used to send the notification/status signals identified above.

269. Hazelzet also discloses that UE 121 is an open drain output, EX1014, [0072], which a Skilled Artisan would necessarily understand is driven by a transistor in an open drain configuration. EX1017, FIGs. 4-5, 5:65-6:18 (depicting in FIG. 5 OR logic gate used for such purpose); see ¶¶ 147-152, *above*. A Skilled Artisan would understand that such a transistor necessarily has “a *gate*” that can be driven to assert the open drain output. *Id.*

270. Because in the combinations analyzed here, Error Logic 100 receives both “US [sic] 110” signal and the “PERR 111” signal and the training mode notification signals, but uses only one such signal to drive the UE 121 output, depending on mode, a Skilled Artisan would understand that Error Logic 100 would necessarily include logic circuitry (in addition to the open drain transistor) to determine which signal should be used to drive the transistor. EX1017, FIGs. 4-5, 5:65-6:18 (depicting in FIG. 5 OR logic gate used for such purpose). That additional logic circuitry is the “*logic circuit*,” and necessarily has “*an output coupled to a gate of the transistor*” because that is how a transistor in an open drain configuration is driven (*i.e.*, by a signal driving the gate, see EX1017, FIGs.

4-5, 5:65-6:18 (depicting in FIG. 5 OR logic gate used for such purpose); see ¶¶ 147-152, *above*. Moreover, the signal driving that gate is necessarily related to one of the signals input to Error Logic 100 (e.g., “PERR 111” (“*first signal*”) or the training notification signals (“*second signal*”), depending on mode, so the additional logic circuitry is “*configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.*”

271. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy the “*wherein the notification circuit further includes a multiplexor or a logic circuit having a output coupled to a gate of the transistor and configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences*” limitation.

272. To the extent one might argue otherwise, the notification circuit of the obvious combination of Hazelzet, JEDEC or Buchmann, and Kim, described above, includes “*a multiplexor or a logic circuit having a output coupled to a gate of the transistor and configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences,*” for the reasons set forth in ¶¶ 240-246 above. In particular,

the circuit is “*configurable*” in this manner because it be placed in either the Parity Mode or the Training Mode.

7. **Claim 7 is Unpatentable**

273. Claim 7 requires “[t]he memory module of claim 3, wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state.”

274. As demonstrated above, in the combinations analyzed here the open drain output is configured such that the transistor output is driven low (ground) while training is still occurring and driven high upon completion. Moreover, to drive the output low (i.e., ground), the signal at the gate of the transistor (“*the second signal*” when the system is in training mode) must be high, causing the transistor to conduct and connect the drain to ground. On the other hand, to drive the output high (which would be a high impedance state), the gate of the transistor must be low, turning the transistor off. EX1003, ¶¶157,254-256.

275. As explained in claim element [1.g.] and claims 4-6, in either obvious combination of Hazelzet and JEDEC or Buchmann, the open drain signals would be low logic levels (i.e., the logic levels of the open drain output driven low, because the logic level of the gate would be driven high) in the second mode to

indicate the training operations (*e.g.*, MB-DRAM/TS0 or TS3) was in progress, and at a high impedance (*i.e.*, the logic level of the open drain output driven high, because the logic level of the gate would be driven low) when that operations completed in each memory module. See ¶¶ 228, 256, 263, 270, 147-149, *above*.

276. The application of a high signal to the gate of the transistor (which indicates that the training sequence is in progress) is the claimed “*second signal so as to drive the open drain output from the high impedance state to ground*” (*i.e.*, a low logic level). *Id.* The application of a low signal to the gate of the transistor (which indicates the completion of the training sequence) is the claimed “*second signal so as to drive the open drain output ... from ground to the high impedance state.*” *Id.*

277. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy the “*wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the transistor with the second signal so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state*” limitation.

278. To the extent one might argue otherwise, the notification circuit of the obvious combination of Hazelzet, JEDEC or Buchmann, and Kim, described above, includes “*wherein the module controller is configurable to provide the information related to the one or more training sequences by driving a gate of the*

transistor with the second signal so as to drive the open drain output from the high impedance state to ground or from ground to the high impedance state,” for the reasons set forth in ¶¶240-246 above. In particular, the circuit is “configurable” in this manner because it can be placed in the Training Mode, and thereby drive the gate of the transistor with the training status signal.

8. Claim 8 is Unpatentable

279. Claim 8 requires “[t]he memory module of claim 1, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.”

280. As explained in claim element [1.b.], Hazelzet discloses a second set of edge connections for communicating address and control signals from the memory controller of the host system. Ex. 1014 (Hazelzet) at FIGs 7A-7C (showing address edge connections including pins 67, 70, 72-75, 82, 205-207, 210-213, 220, 227 and command edge connections including pins 86, 89, 91, 93), ¶[0072] (referring to “/CS” as commands), ¶[0068] (listing various control signals including “chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE)” signals); *see also* Ex. 1014 (Hazelzet) at ¶[0038] (“The memory interface chip 18 then sends and receives data, via line 15, to the memory devices or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16 and check bits

for error correction purposes to the ECC/ Parity register chip 21 via line 25.”), FIG. 2 (showing address and command line 16); see ¶¶179-184, *above*.

281. In the JEDEC combination analyzed here, JEDEC discloses that during the MB-DRAM training (i.e., the mode that is added to Hazelzet here), “[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low.” EX1015, 8. A Skilled Artisan would understand from this that during such training the address/control pins (including the high order address/control pins) would remain inactive as those are pins used to provide “DRAM commands or control word writes,” and no data signals would be communicated on the data pins. *Id.*

282. Similarly, in a Buchmann combination analyzed here, in which only the TS0 training operations are carried out in the training mode (“*second mode*”), one or more of the pins of these edge connections would not be active during that training because TS0 training involves training of the “clock” itself, so a Skilled Artisan would have understood that no “address” or control signals (including to/from the high order address/control pins) are transmitted between the host and the memory module during TS0 training. Ex. 1016 (Buchmann) at 5:51-7:2.

283. To the extent Patent Owner argues otherwise, a Skilled Artisan would have found it obvious at least not to send any data, control or address signals while the clock is being trained for the same reasons set forth above. For example, a Skilled Artisan would have been motivated to keep the pin(s) for address, control and data inactive to conserve power and/or avoid unreliable operation during periods that the clock may be unstable.

284. Moreover, I understand that a negative limitation is satisfied by silence in the prior art. *Süd-Chemie, Inc. v. Multisorb Technologies, Inc.*, 554 F.3d 1001, 1004-05 (Fed. Cir. 2009). I understand that this claim includes a negative limitation, because it requires “*not active.*” Neither Hazelzet nor JEDEC or Buchmann disclose pins in the second edge connections being inactive while the memory module is in the training modes during initialization/power-on.

285. The obvious combinations of Hazelzet and JEDEC or Buchmann therefore satisfy the “*wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode*” limitation.

9. Claim 9 is Unpatentable

286. Claim 9 requires “[t]he memory module of claim 1, wherein the memory module in the second mode is configurable to perform the operations

related to the one or more training sequences without communicating data signals via the first edge connections while the memory module is in the second mode.”

287. According to claim element [1.b.], the “*first edge connections*” are connections “*via which the memory module receives or outputs data signals*” from/to the host. See ¶182, above.

288. In the JEDEC combination analyzed here, JEDEC discloses that during the MB-DRAM training (i.e., the mode that is added to Hazelzet here), “[n]o DRAM commands or control word writes (either over the Command/Address and Control buses or via SMBus) can be issued to the MB until the MB-DRAM Interface training is complete and the DODTn inputs must be kept low.” EX1015, 8. A Skilled Artisan would understand from this that during such training the address/control pins (including the high order address/control pins) would remain inactive as those are pins used to provide “DRAM commands or control word writes,” and no data signals would be communicated on the data pins. *Id.*

289. Similarly, in the obvious combination of Hazelzet and Buchmann, the memory module can execute a training sequence (e.g., TS0 training, which involves training of the “clock”) in the SBC mode. Ex. 1016 (Buchmann) at 5:51-7:2; see also analysis in claim 1. Because this training involves training of the “clock” itself, a Skilled Artisan would have understood that there are no “data”

signals being transmitted between the host and the memory module during the TS0 training.

290. To the extent Patent Owner argues otherwise, a Skilled Artisan would have found it at least obvious not to send any data, control or address signals while the clock is being trained for the same reasons set forth above. For example, a Skilled Artisan would have been motivated to keep the pin(s) for address, control and data inactive to conserve power and/or avoid unreliable operation during periods that the clock may be unstable.

291. Moreover, I understand that a negative limitation is satisfied by silence in the prior art. *Süd-Chemie, Inc. v. Multisorb Technologies, Inc.*, 554 F.3d 1001, 1004-05 (Fed. Cir. 2009). I understand that this claim includes a negative limitation, because it requires “*without communicating data signals.*” Neither Hazelzet nor JEDEC or Buchmann disclose communicating data signals while the memory module is in the training mode for the MB-DRAM or TS0 training during initialization/power-on.

292. Accordingly, the obvious combinations of Hazelzet and JEDEC or Buchmann satisfy the “*wherein the memory module in the second mode is configurable to perform the operations related to the one or more training sequences without communicating data signals via the first edge connections while the memory module is in the second mode*” limitation.

10. Claim 10 is Unpatentable

a) [10.a] Preamble

293. The preamble of claim 10 requires “[a] memory module operable with a memory controller of a host system, comprising.”

294. This limitation is satisfied for the same reasons set forth for claim element [1.a.]. See ¶¶175-177, above.

b) [10.b] Printed Circuit Board Having Edge Connections

295. Claim 10 requires “a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections.”

296. This limitation is satisfied for the same reasons set forth for claim element [1.b.]. See ¶¶178-185, above.

c) [10.c] Dynamic Random Access Memory Elements

297. Claim 10 requires “dynamic random access memory elements on the printed circuit board.”

298. This limitation is satisfied for the same reasons set forth for claim element [1.c.]. See ¶¶186-188, *above*.

d) [10.d] Module Controller ... Having An Open Drain Output

299. Claim 10 requires “*a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller having an open drain output coupled to the error edge connection and configurable to drive the open drain output from a first state to a second state and from the second state to the first state, one of the first state and the second state being a low logic level, and the other one of the first state and the second state being a high impedance state.*”

300. This limitation is satisfied for the same reasons set forth for claim elements [1.d.] and [1.g.]. See ¶¶189-194, 224-229, *above*.

301. While claim element [1.g.] requires the module controller to be “configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection **to a first state or to a second state**, one of the first state and the second state being a low logic level and the other one of the first state and the second state being a high impedance state,” claim element [10.d.] requires the module controller to be “configurable to drive the open drain output **from a first state to a second state and from the second state to the first state**, one of the first state and the second state being a

low logic level, and the other one of the first state and the second state being a high impedance state.”

302. This additional language in claim element [10.d.] is similar to claim 7 and satisfied in the obvious combinations of Hazelzet and JEDEC or Buchmann for similar reasons. In particular, as explained in claim element [1.g.] and claim 7, in either obvious combination of Hazelzet and JEDEC or Buchmann, the open drain signals would be low logic levels (*i.e.*, the logic levels of the open drain output changes from a high impedance state to a low state, because the gate of the transistor changes from a low to a high) to indicate the training sequence (*e.g.*, MB-DRAM/TS0 or TS3) was in progress. On the other hand, the open drain signals would be at a high-impedance (*i.e.*, the logic level of the open drain output changes from a low state to a high impedance state, because the gate of the transistor changes from a high to a low) when that sequence completed in all memory modules. EX1014, FIGs. 4B-5, ¶¶[0059],[0070], [0072],[0076]; EX1017, FIGs. 4-5, 5:65-6:18; Ex. 1016 (Buchmann) at 5:51-7:2, Table 1, Table 2, FIG. 4, 8:24-9:18, Table 5, Table 6, FIG. 6, 8:24-9:17, 3:52-54, 27:18-21, 26:30-32; *see also* ¶¶147-152, *above*.

e) [10.e] Operable In At Least A First Mode And A Second Mode

303. Claim 10 requires “*wherein the memory module is operable in at least a first mode in which the memory module is configurable to perform one or more*

memory read or write operations by communicating data signals via the first edge connections in response to address and control signals received via the second edge connections, and a second mode in which the memory module is not accessed by the memory controller for memory read or write operations, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences without communicating data signals via the first edge connections.”

304. This limitation is satisfied for the same reasons set forth for claim element [1.e.] and claim 9. See ¶¶195-212, 286-292, *above*.

305. While claim element [1.e.] requires that “the memory module in the second mode is not accessed by the memory controller for **normal memory read or write operations**, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences” and claim 9 requires a “second mode [that] is configurable to perform the operations related to the one or more training sequences **without communicating data signals via the first edge connections** while the memory module is in the second mode,” claim element [10.e.] requires “a second mode in which the memory module is not accessed by the memory controller for **memory read or write operations**, and wherein the memory module in the second mode is configurable to perform operations related to one or more training sequences **without**

communicating data signals via the first edge connections.” As demonstrated above, ¶¶106-119, those phrases should be interpreted to mean the same thing and, regardless, in the combinations analyzed, the “memory module is not accessed **by the memory controller** for memory read or write operations” during MB-DRAM Training, TS0 training or TS3 training because in none of those sequences does the memory controller communicate data with the module or seek to read or write to the memory devices. The analysis of claim element [1.e.] and claim 9 therefore satisfies this claim element.

f) [10.f] Operation Of Module Controller In The First Mode

306. Claim 10 requires “*wherein the module controller in the first mode is configurable to receive via the second edge connections the address and control signals associated with the one or more memory read or write operations, wherein the dynamic random access memory elements are configurable to communicate data signals with the memory controller via the first edge connections in accordance with the address and control signals, and wherein the module controller in the first mode is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is in the first mode.*”

307. This limitation is satisfied for the same reasons set for in claim element [1.f.]. See ¶¶213-223, above.

g) [10.g] Operation Of Module Controller In The Second Mode

308. Claim 10 requires “*wherein the module controller in the second mode is further configurable to output to the memory controller open-drain signals related to the one or more training sequences via the open drain output and the error edge connection while the memory module is in the second mode.*”

309. This limitation is satisfied for the same reasons set for in claim element [1.g.]. See ¶¶224-229, *above*.

11. Claim 11 is Unpatentable

310. Claim 11 requires “[t]he memory module of claim 10, wherein the module controller comprises an integrated circuit.”

311. This claim is satisfied for the same reasons set for in claim 2. See ¶¶230-232, *above*.

12. Claim 12 is Unpatentable

312. Claim 12 requires “[t]he memory module of claim 10, wherein the module controller includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to the ground, wherein the module controller is configurable to output to the memory controller the open-drain signals related to the one or more training sequences by driving a gate of the transistor high so as to drive the open drain output and the error edge connection to ground, and by driving the gate of the transistor low as to drive the

open drain output and the error edge connection to the high impedance state, and wherein the notification circuit is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the open drain output and ground.”

313. This claim is satisfied for the same reasons set forth for claims 3, 4 and 5. In particular, the analysis for claim 3 satisfies claim element [12.a.], see ¶¶233-252, *above*, the analysis for claim 4 satisfies claim element [12.b.], see ¶¶253-257, and the analysis for claim 5 satisfies claim element [12.c.]. See ¶¶259-264. In an abundance of caution, I note that this includes the alternative obviousness combinations of Hazelzet and JEDEC or Buchmann, in further view of Kim, as explained in Section V.A.3 above, ¶¶238-252.

13. Claim 13 is Unpatentable

314. Claim 13 requires “[t]he memory module of claim 12, wherein the notification circuit further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor and configurable to drive the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.”

315. This claim is satisfied or rendered obvious in further combination with Kim for the same reasons set forth for claims 3 and 6. See ¶¶233-252, 266-271, *above*. In an abundance of caution, I note that this includes the alternative

obviousness combinations of Hazelzet and JEDEC or Buchmann, in further view of Kim, as explained in Section V.A.3 above, ¶¶238-252.

14. Claim 14 is Unpatentable

316. Claim 14 requires “[t]he memory module of claim 10, wherein the module controller is configurable to output the open-drain signals related to the one or more training sequences by driving the open drain output from the high impedance state to the low logic level or from the low logic level to the high impedance state.”

317. This claim is satisfied or rendered obvious in further combination with Kim for the same reasons set forth for claims 3 and 7. See ¶¶233-252, 273-277, above. In an abundance of caution, I note that this includes the alternative obviousness combinations of Hazelzet and JEDEC or Buchmann, in further view of Kim, as explained in Section V.A.3 above, ¶¶238-252.

15. Claim 15 is Unpatentable

318. Claim 15 requires “[t]he memory module of claim 10, wherein the second edge connections include one or more pins that are not active while the memory module is in the second mode.”

319. This claim is satisfied for the same reasons set forth for claim 8. See ¶¶279-285, above.

16. Claim 16 is Unpatentable

320. Claim 16 requires “[t]he memory module of claim 10, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is in the second mode.”

321. This claim element is satisfied for the same reasons I set forth above for claim 8 where I addressed the additional limitation regarding “one or more high-order address pins that are not active” when conducting my claim 8 analysis. See ¶¶279-285, above.

17. Claim 17 is Unpatentable

a) [17.a] Preamble

322. The preamble of claim 17 requires “[a] method, comprising”:

323. This limitation is satisfied, because Hazelzet and JEDEC or Buchmann disclose corresponding methods in connection with the operation of the apparatus (analyzed in connection with claim 1). See ¶¶175-177, above.

b) [17.b] Printed Circuit Board Having Edge Connections & Dynamic Random Access Memory Elements

324. Claim 17 requires “at a memory module coupled with a memory controller of a host system, the memory module including a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections via which the memory module

receives or outputs data signals, second edge connections via which the memory module receives address and control signals, and an error edge connection in addition to the first edge connections and the second edge connections, the memory module further including dynamic random access memory elements on the printed circuit board.”

325. This limitation is satisfied for the same reasons set forth for claim elements [1.a.], [1.b.] and [1.c.]. See ¶¶175-188, *above*.

c) [17.c] Memory Read or Write Operations

326. Claim 17 requires “*receiving via the second edge connections address and control signals associated with one or more memory read or write operations; controlling the dynamic random access memory elements to communicate data signals corresponding to the one or more memory read or write operations via the first edge connections in response to the address and control signals; outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module while the memory module is being accessed by the memory controller for a memory read or write operation.*”

327. This limitation is satisfied for the same reasons set forth for claim elements [1.e.] and [1.f.]. Specifically, as explained there, Hazelzet discloses normal memory operations that were known to entail the module receiving address and control signals from a system memory controller via the respective address and

control edge connections, and in response communicating data between the system memory controller and the module DRAMs via the data edge connections and under the control of the module controller. See ¶197, *above*. Also as explained above, Hazelzet discloses the module outputting, in the “*first mode*,” a parity error signal via an open drain output (UE 121) in connection with memory read and write operations accessing the module. See ¶¶195-223, *above*.

d) [17.d] Operations Related To Training Sequences

328. Claim 17 requires “*performing operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and outputting to the memory controller via the open drain output and the error edge connection open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation.*”

329. This limitation is satisfied for the same reasons set forth for claim elements [1.e.] and [1.g.]. Specifically, as demonstrated above, the combinations analyzed here includes a module that performs training sequence operations unrelated to memory read or write operations in response to commands from the memory controller. See ¶¶213-223 *above*. Similarly, as explained in claim elements [1.e] and [1.g.], the module of the combined system outputs to the system memory controller training notification signals (*e.g.*, ERROUT#, TS0_done,

TS3_ack, TS3_done) via an open drain output (UE 121), see ¶¶224, above, which notification signals are related solely to the JEDEC or Buchmann training sequences (respectively) and not to any memory controller operations that seek to communicate data with the module or seek to read or write to the memory devices, see ¶¶153,164,211 , above.

18. Claim 18 is Unpatentable

330. Claim 18 requires “[t]he method of claim 17, wherein the second edge connections include one or more pins that are not active while the memory module is trained with the one or more training sequences.”

331. This claim is satisfied for the same reasons set forth for claims 1 and 8. See ¶¶ 224-229, 279-285, above.

19. Claim 19 is Unpatentable

332. Claim 19 requires “[t]he method of claim 18, wherein the second edge connections include one or more high-order address pins that are not active while the memory module is trained with the one or more training sequences.”

333. This claim is satisfied for the same reasons set forth for claims 1, 10, and 16. See ¶¶224-229, 309, 321, above.

20. Claim 20 is Unpatentable

334. Claim 20 requires “[t]he method of claim 17, wherein the memory module includes a notification circuit having a transistor with an open drain coupled to the open drain output and a source coupled to ground, wherein

outputting via an open drain output coupled to the error edge connection a signal indicating a parity error having occurred in the memory module comprises driving a gate of the transistor high to provide a low impedance path between the open drain output and ground, and wherein outputting the open-drain signals related to the one or more training sequences and unrelated to any memory read or write operation comprises driving the gate of the transistor to drive the open drain output from a high impedance state to ground and from ground to the high impedance state.”

335. This claim is satisfied for the same reasons set forth for claims 3, 4, 5. The analysis for claim 3 satisfies claim element [20.a.], the analysis for claim 5 satisfies claim element [20.b.], and the analysis for claim 4 satisfies claim element [20.c.]. Moreover, as demonstrated above for claim element [1.g], in the combinations analyzed here, the open drain signals relating to the training sequences (*e.g.*, ERROUT#, TS0_done, TS3_ack, TS3_done) are “*unrelated to any memory read or write operation*” because they are related solely to the JEDEC or Buchmann training sequences and not to any memory read or write operations, including because there are no memory read or write operations in response to commands from the memory controller during the training mode analyzed here. See 233-237, 254-256 -257, 260-264, *above*. In an abundance of caution, I note that this includes the alternative obviousness combinations of Hazelzet and JEDEC

or Buchmann, in further view of Kim, as explained in Section V.A.3 above, ¶¶238-252.

21. Claim 21 is Unpatentable

a) [21.a] Preamble

336. The preamble of claim 21 requires “[a] memory module operable with a memory controller of a host system, comprising.”

337. This limitation is satisfied for the same reasons set forth for claim element [1.a.]. See ¶¶175-177, above.

b) [21.b] Printed Circuit Board Having Edge Connections

338. Claim 21 requires “a printed circuit board having edge connections that fit into a corresponding slot of the host system so as to be in electrical communication with the memory controller, the edge connections including first edge connections, second edge connections, and an error edge connection in addition to the first edge connections and the second edge connections.”

339. This limitation is satisfied for the same reasons set forth for claim element [1.b.]. See ¶¶178-185, above.

c) [21.c] Dynamic Random Access Memory Elements

340. Claim 21 requires “dynamic random access memory elements on the printed circuit board.”

341. This limitation is satisfied for the same reasons set forth for claim element [1.c.]. See ¶¶186-188, *above*.

d) [21.d] Module Controller Including A Transistor Having A Gate And An Open Drain Output

342. Claim 21 requires “*a module controller on the printed circuit board and coupled to the dynamic random access memory elements, the module controller including a transistor having a gate and an open drain output coupled to the error edge connection; wherein the module controller is configurable to drive the gate of the transistor so as to drive the open drain output to a first state or a second state, the first state being a low logic level and the second state being a high impedance state.*”

343. This limitation is satisfied for the same reasons set forth for claim elements [1.d.], and claims 3 and 4. Specifically, the combinations analyzed here satisfies “*a module controller on the printed circuit board and coupled to the dynamic random access memory elements*” for the reasons set forth for claim element [1.d.]. See ¶¶189 *above*. It satisfies “*the module controller including a transistor having a gate and an open drain output coupled to the error edge connection*” for the reasons set forth for claim 3. See ¶¶233-252 *above*. And it satisfies “*wherein the module controller is configurable to drive the gate of the transistor so as to drive the open drain output to a first state or a second state, the*

first state being a low logic level [e.g., ground] and the second state being a high impedance state” for the reasons set forth for claim 4. See ¶¶253-257 above.

e) [21.e] Normal Memory Read or Write Operations

344. Claim 21 requires “*wherein the module controller is configurable to receive via the second edge connections memory commands associated with normal memory read or write operations and to output a set of address and control signals for each of the normal memory read or write operations; wherein the dynamic random access memory elements are configurable to communicate one or more N-bit-wide data signals with the memory controller via the first edge connections in response to the set of address and control signals, where N is at least 32; wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred during any of the memory read or write operations by driving the open drain output and the error edge connection to the first state.*”

345. This limitation is satisfied for the same reasons set forth for claim elements [1.f.i-iii], with the following additional analysis. See ¶¶213-223, *above*.

346. As demonstrated above, Hazelzet discloses that the ECC/Parity register is configurable (*e.g.*, when placed in parity mode) to receive address command signals that a Skilled Artisan would understand to be associated with normal memory read and write operations (“*memory commands associated with*

*normal memory read or write operations”). See ¶¶197 above; see also EX1014, FIGs. 2, 7A-7B, ¶¶[0015],[0035],[0038], [0041],[0064],[0070]. Hazelzet further discloses that, in response to such commands, the ECC/Parity register outputs associated address and control signals to the DRAMs of the module. EX1014, [0042],[0075]. Hazelzet therefore discloses “*wherein the module controller is configurable to receive via the second edge connections memory commands associated with normal memory read or write operations and to output a set of address and control signals for each of the normal memory read or write operations.*”*

347. To the extent one might argue that Hazelzet does not sufficiently disclose this claim element, it would have been obvious to include it in the combined system. In particular, Hazelzet discloses the ECC/Parity register receiving address and command information associated with memory commands. EX1014, FIGs. 2, 7A-7B, ¶¶[0015],[0038],[0041-42],[0064], [0070],[0075]. A Skilled Artisan would have been motivated to configure the register to correspondingly output associated address and control signals to the DRAMs, and it would have been common sense to do so, because that would be necessary to carry out the memory operations and access the DRAMs.

348. As demonstrated above, Hazelzet discloses that the DRAMs of his module are configurable (*i.e.*, when connected to the address. control, data and

PLL lines of the module, as described in Hazelzet, see EX1014, Fig. 2, to communicate data signals with the system memory controller over the disclosed edge connections in response to address and control signals. Moreover, Hazelzet discloses pinout information for one embodiment of his module, which includes 64 data lines (DQ0-DQ63), EX1014, FIGs. 7A-7C, which a Skilled Artisan would understand can communicate a 64-bit wide data signal. Alternatively, Hazelzet discloses a 72 bit wide (*i.e.*, $9 \times 8 = 72$) memory module Ex. 1014 (Hazelzet) at ¶[0092] (disclosing “an exemplary memory module having 9 eight bit wide or 18 four or eight bit wide memory devices and a single 4-rank enabled buffer chip 21.”). Hazelzet therefore discloses “*wherein the dynamic random access memory elements are configurable to communicate one or more N-bit-wide data signals with the memory controller via the first edge connections in response to the set of address and control signals, where N is at least 32.*”

349. To the extent Patent Owner argues that a single “dynamic random access memory element” must be able to “*communicate one or more N-bit-wide data signals ... where N is at least 32,*” to satisfy the limitation in claim element [21.e.], this limitation would nevertheless have been obvious in the obvious combination of Hazelzet and Buchmann. In particular, while Hazelzet discloses using a memory module having “9 eight bit wide ... memory devices” as an example, Ex. 1014 (Hazelzet) at ¶[0092] (disclosing “an exemplary memory

module having 9 eight bit wide or 18 four or eight bit wide memory devices and a single 4-rank enabled buffer chip 21.”), a Skilled Artisan would have understood that modifying the memory system to use SDRAMs with higher bit widths (*e.g.*, 32 bit wide) was not only known (or at least obvious), but also well within the skill of a Skilled Artisan by the effective filing date of the 595 Patent. *See, e.g.*, Ex. 1024 (JESD79) at page i. (“This comprehensive standard defines all required aspects of 64M x4/x8/x16 DDR SDRAMs, including features, functionality, AC and DC parametrics, packages and pin assignments. This scope will subsequently be expanded to formally apply to x32 devices, and higher density devices as well.”); Ex. 1029 (JESD209) at page 1 (demonstrating the prevalence of “x16 and x32 Low Power Double Data Rate SDRAM devices” by 2007); *see also* Ex. 1014 (Hazelzet) at ¶[0113] (disclosing embodiments with “LP RAM (Low Power DRAMs which are often based on the fundamental functions, features and/or interfaces found on related DRAMs.”).

350. Finally, as demonstrated above, the combinations analyzed here discloses “*wherein the module controller is further configurable to output via the open drain output and the error edge connection a signal indicating a parity error having occurred during any of the memory read or write operations by driving the open drain output and the error edge connection to the first state*” for the reasons set forth above for claim element [1.f.iii]. *See* ¶¶213-223, above. Additionally, as

explained in claim element [1.e.], one skilled in the art would have understood Hazelzet's parity mode to be a normal operating mode during which “*one or more normal memory read or write operations*” is/are performed. Ex. 1014 (Hazelzet) at ¶[0064] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”), ¶[0103] (“A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.”); *see also id.* at ¶[0020] (“Still further the present invention permits operation of the memory module in parity mode, such that unused ECC check bit inputs are held at a low level thus ensuring that these inputs are at a known and quiescent state.”); ¶[0072] (“Error reporting circuitry is included to permit external monitoring of DIMM operation.”); ¶[0070] (“In addition to the above ECC mode, the same twenty two chip select gated data signals can be operated in parity mode (/ECC Mode high), whereby the signal received on CHK0/Parity in line is received as parity to the register one clock pulse later than the chip select gated data inputs. The received parity bit is then compared to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. ... No correction of errors will be completed in this mode.”); *see also* claim element [1.e.]. Accordingly, a Skilled Artisan would have understood that the parity error signal, would have indicated “a

parity error having occurred during any of the memory read or write operations by driving the open drain output and the error edge connection to the first state,” as required by the claims. Id.

f) [21.f] Operations Related To Training Sequences

351. Claim 21 requires “*wherein the memory module is configurable to perform operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations; and wherein the module controller is configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection from one of the first state and the second state to the other one of the first state and the second state.*”

352. This limitation is satisfied for the same reasons set forth for claim elements [1.e.], [1.g.] and [10.e.]. Like claim element [10.e.], this element recites “*memory read or write operations,*” rather than “***normal*** *memory read or write operations*” like claim element [1.e.], and is satisfied for those additional reasons.

Moreover, I note that the combinations analyzed here disclose “*wherein the memory module is configurable to perform operations related to one or more training sequences while the memory module is not accessed by the memory controller for memory read or write operations*” for the reasons set forth in ¶¶195-212, 225-229, 303-305 above. The combinations disclose “*wherein the module*

controller is configurable to provide information related to the one or more training sequences by driving the open drain output and the error edge connection from one of the first state and the second state to the other one of the first state and the second state” for the reasons set forth in ¶¶224-229 above.

22. Claim 22 is Unpatentable

353. Claim 22 requires “[t]he memory module of claim 21, wherein the module controller further includes a multiplexor or a logic circuit having an output coupled to the gate of the transistor, and wherein the module controller is configurable to drive the gate of the transistor with either a first signal related to the parity error or a second signal related to the one or more training sequences.”

354. This claim is satisfied or rendered obvious in further combination with Kim for the same reasons set forth for claims 1, 3, and 6. See ¶¶189-194, 233-252, 266-271, *above*. In an abundance of caution, I note that this includes the alternative obviousness combinations of Hazelzet and JEDEC or Buchmann, in further view of Kim, as explained in Section V.A.3 above, ¶¶238-252.

23. Claim 23 is Unpatentable

355. Claim 23 requires “[t]he memory module of claim 22, wherein the transistor has a source coupled to ground, wherein the module controller is configurable to output the signal indicating a parity error having occurred by driving the gate of the transistor high to provide a low impedance path between the

open drain output and ground, and wherein the module controller is configurable to provide the information related to the one or more training sequences by driving the open drain output from a high impedance state to ground or from ground to the high impedance state.”

356. This claim is satisfied for the same reasons set forth for claims 3, 4, 5.

The analysis in claim 3 satisfies claim element [23.a.], see ¶¶233-252, *above*, the analysis in claim 5 satisfies claim element [23.b.], see ¶¶259-264, *above*, and the analysis in claim 4 satisfies claim element [23.c.]. See ¶¶253-257, *above*.

Moreover, as demonstrated above for claim element [1.g], in the combinations analyzed here, the open drain signals relating to the training sequences (*e.g.*, ERROUT#, TS0_done, TS3_ack, TS3_done) are “*unrelated to any memory read or write operation*” because they are related solely to the JEDEC or Buchmann training sequences and not to any memory read or write operations, including because there are no memory read or write operations during the training mode analyzed here. In an abundance of caution, I note that this includes the alternative obviousness combinations of Hazelzet and JEDEC or Buchmann, in further view of Kim, as explained in Section V.A.3 above, ¶¶238-252.

24. Claim 24 is Unpatentable

357. Claim 24 requires “[t]he memory module of claim 21, wherein the memory module is configurable to perform the operations related to the one or

Declaration of Dr. Donald Alpert Regarding U.S. Patent No. 10,474,595

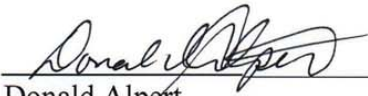
more training sequences while the memory module is not communicating signals via the first edge connections.”

358. This claim is satisfied for the same reasons set forth for claims 1 and 9. See ¶¶213-223, 286-292, *above*.

* * *

I, Donald Alpert, do hereby declare and state, that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, under Section 1001 of Title 18 of the United States Code.

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Donald Alpert



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Hazelzet (43) **Pub. Date: Apr. 24, 2008**

(54) **HIGH DENSITY HIGH RELIABILITY
MEMORY MODULE WITH POWER GATING
AND A FAULT TOLERANT ADDRESS AND
COMMAND BUS**

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(21) **Appl. No.:** **11/551,866**

(22) **Filed:** **Oct. 23, 2006**

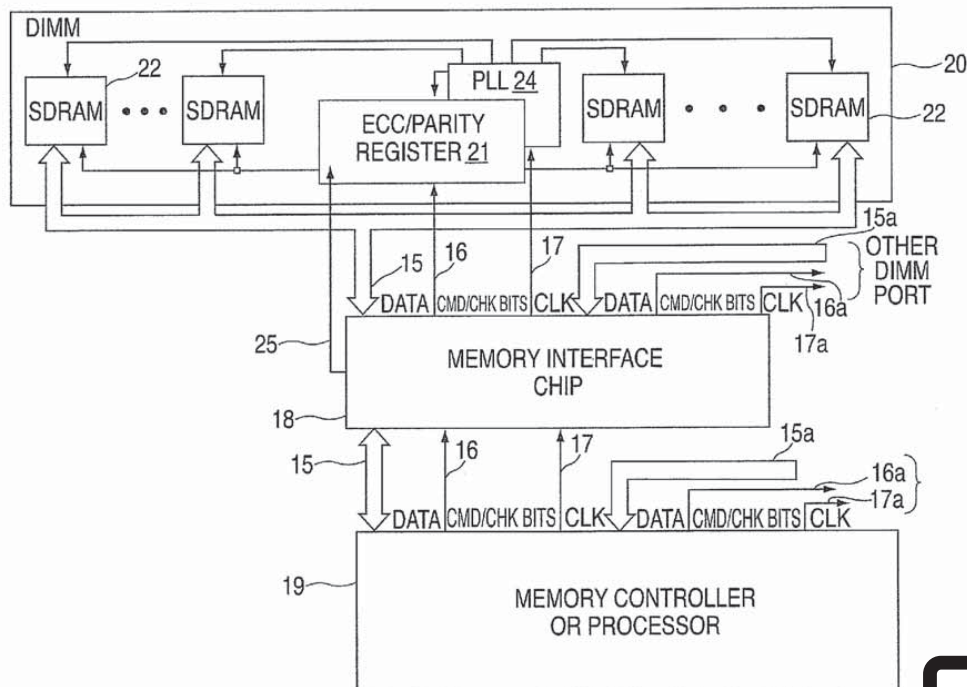
Publication Classification

(51) **Int. Cl.**
H03M 13/00 (2006.01)

(52) **U.S. Cl.** 714/753

(57) **ABSTRACT**

A high density high reliability memory module with power gating and a fault tolerant address and command bus. The memory module includes a rectangular printed circuit board having a first side and a second side, a length of between 149 and 153 millimeters and first and second ends having a width smaller than said length. The memory module also includes a first plurality of connector locations on the first side extending along a first edge of said board that extends the length of the board and a second plurality of connector locations on the second side extending on said first edge of said board. The memory module further includes a buffer device in communication with the circuit board for accessing up to four ranks of memory devices mounted on the first side and second side of the circuit board. In addition, a power savings means is included for causing all or a portion of the buffer device to be in an inactive mode in response to current activity at the memory module. The memory module also includes a locating key having its center positioned on said first edge and located between 82 mm and 86 mm from said first end of said card and located between 66 and 70 mm from said second end of said card.



**DR. DONALD
ALPERT**

EXHIBIT 4

03 - 10 - 2021

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1014, p. 1

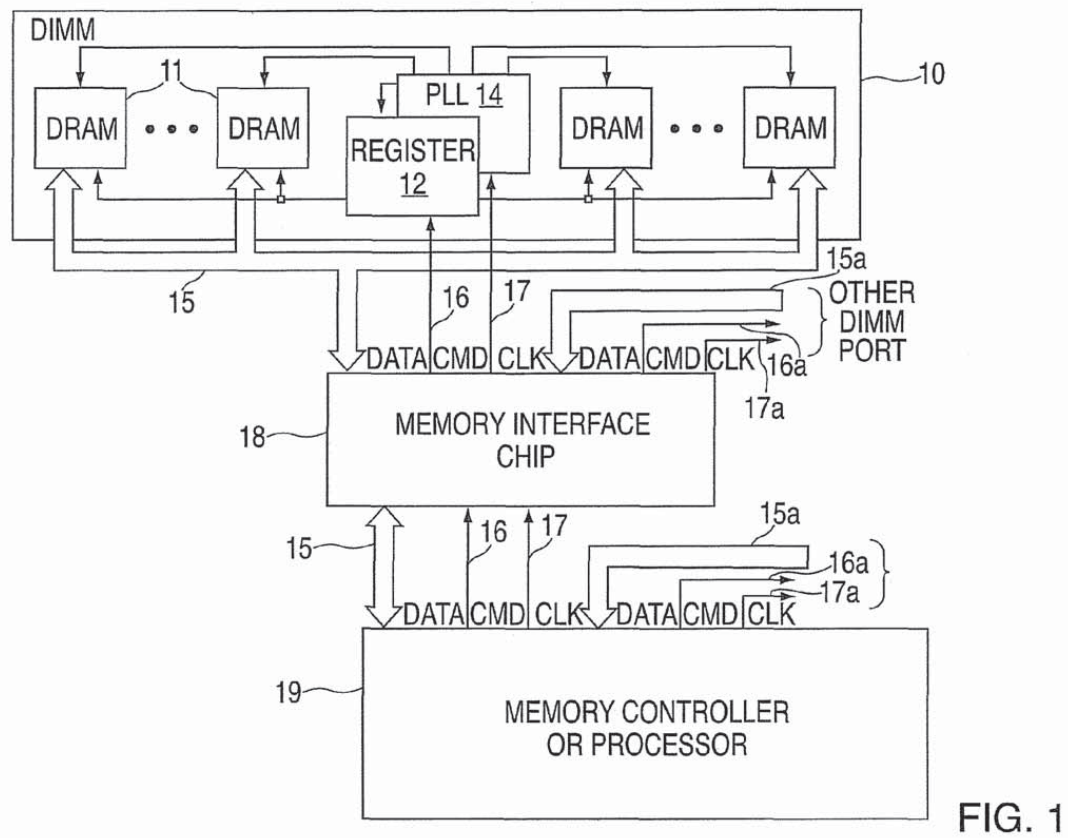
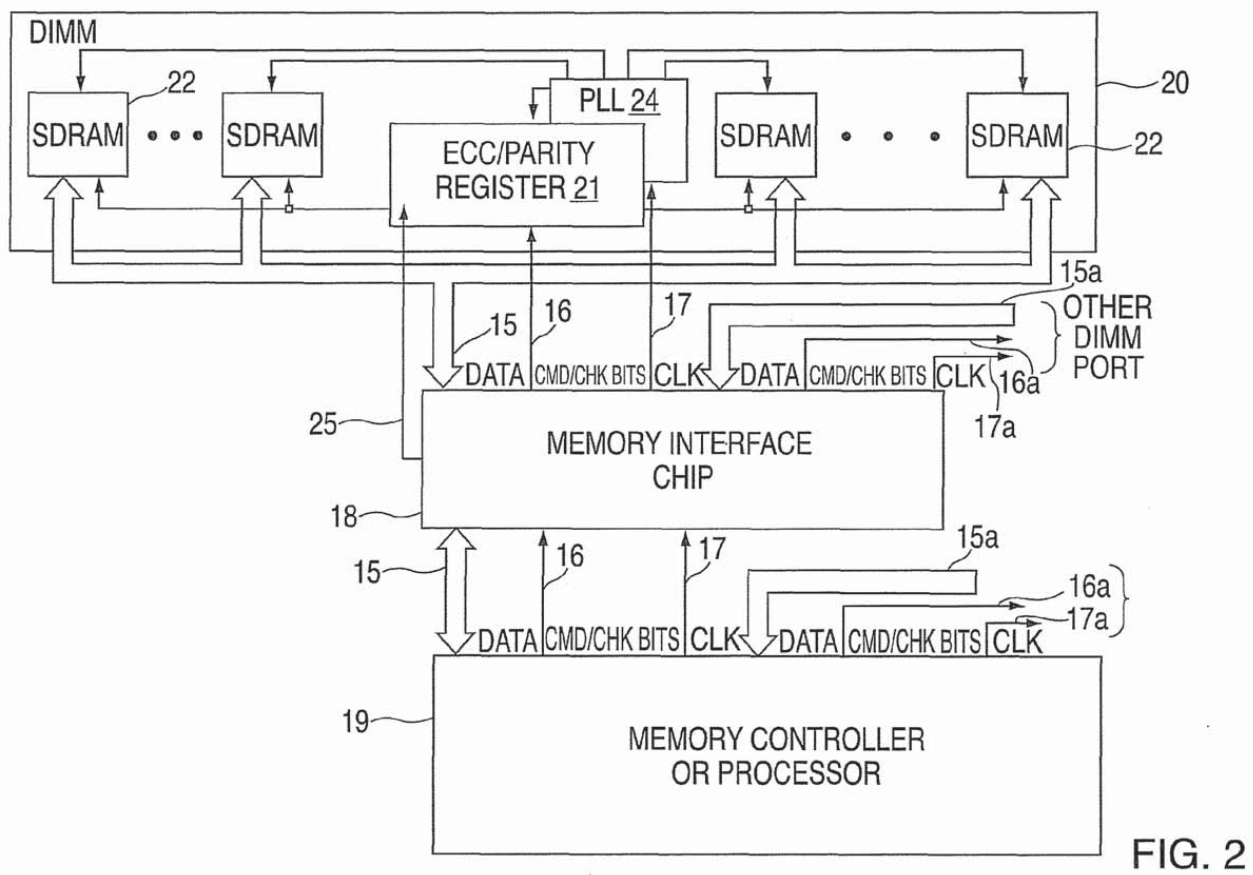
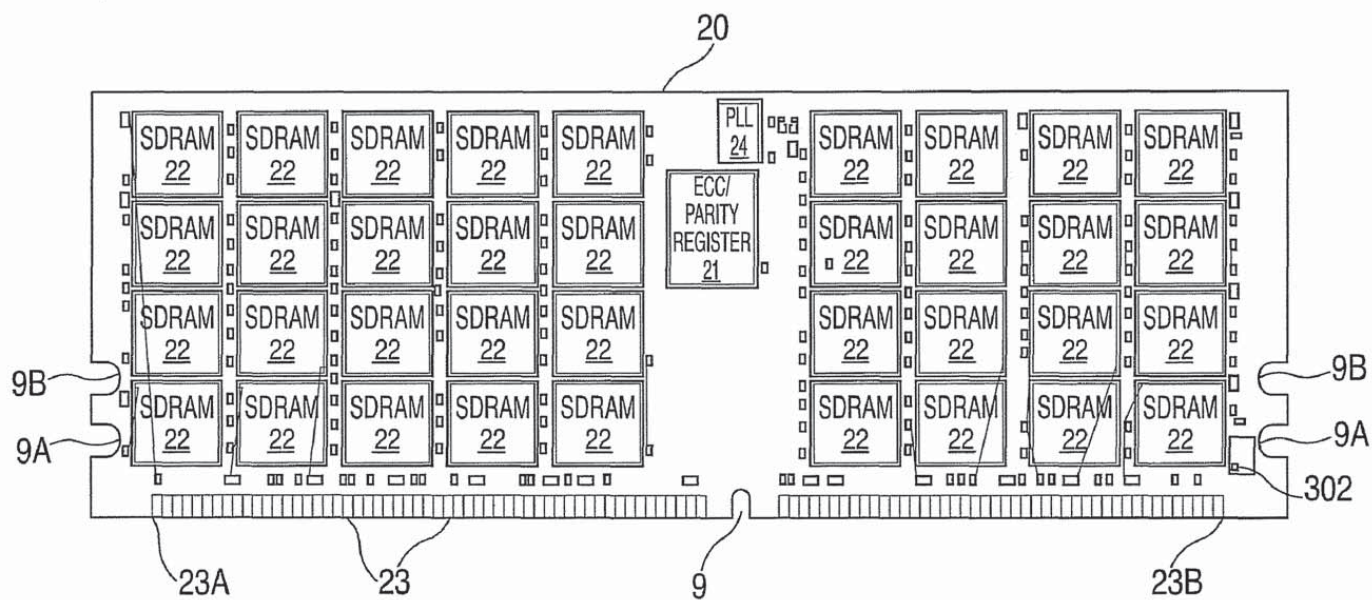


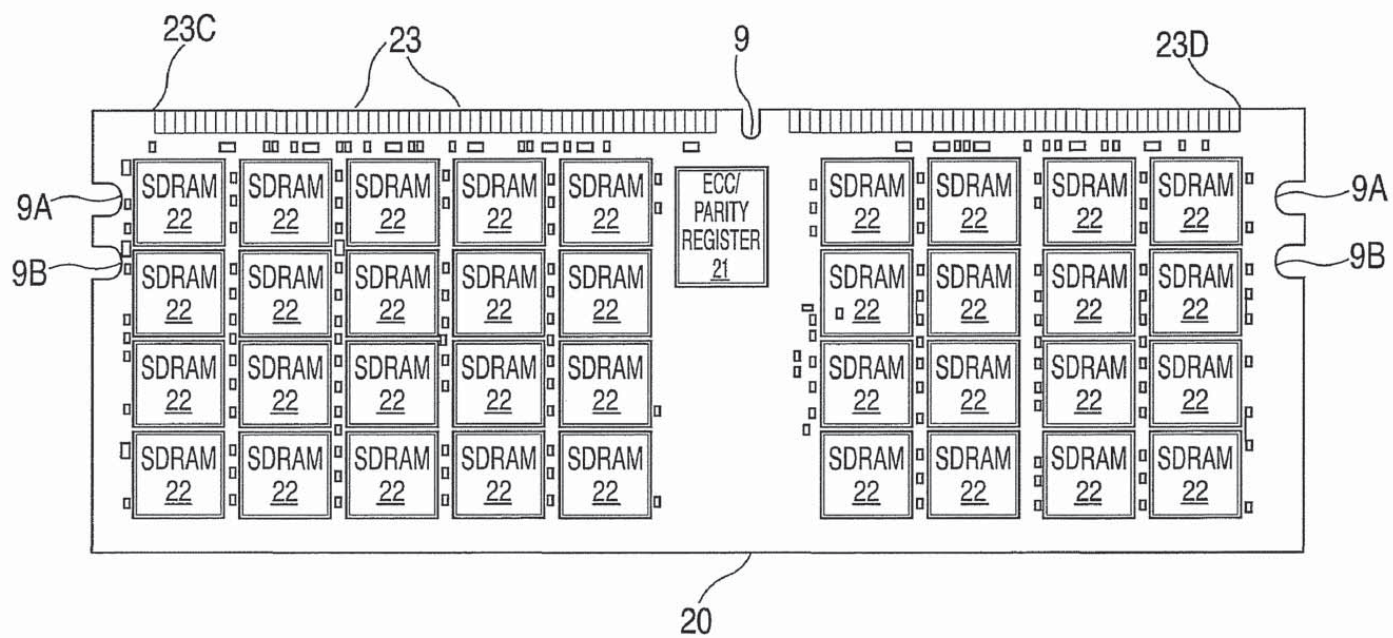
FIG. 1





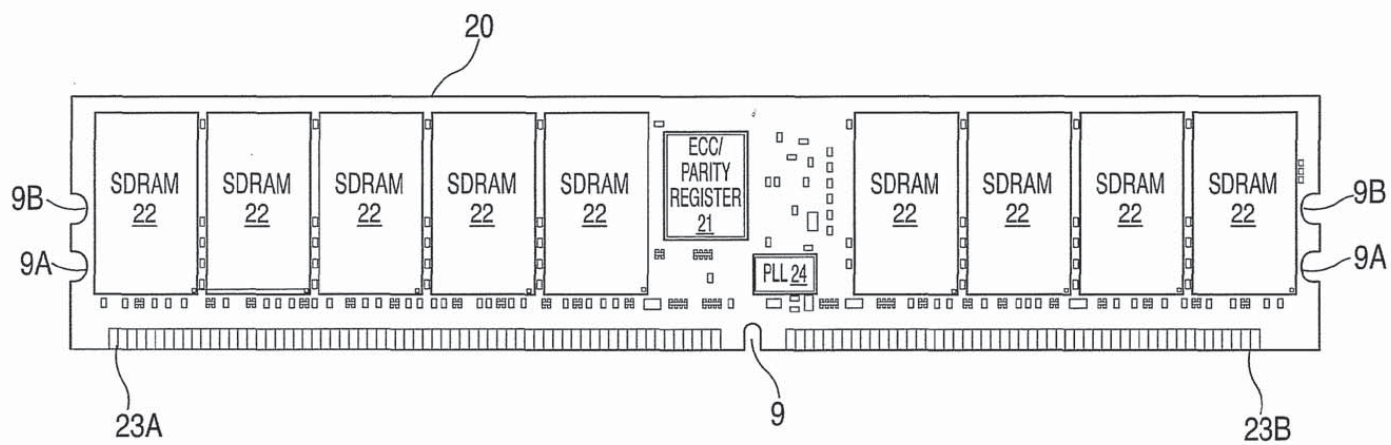
FRONT SIDE OF DIMM - 72 PLANAR

FIG. 3A



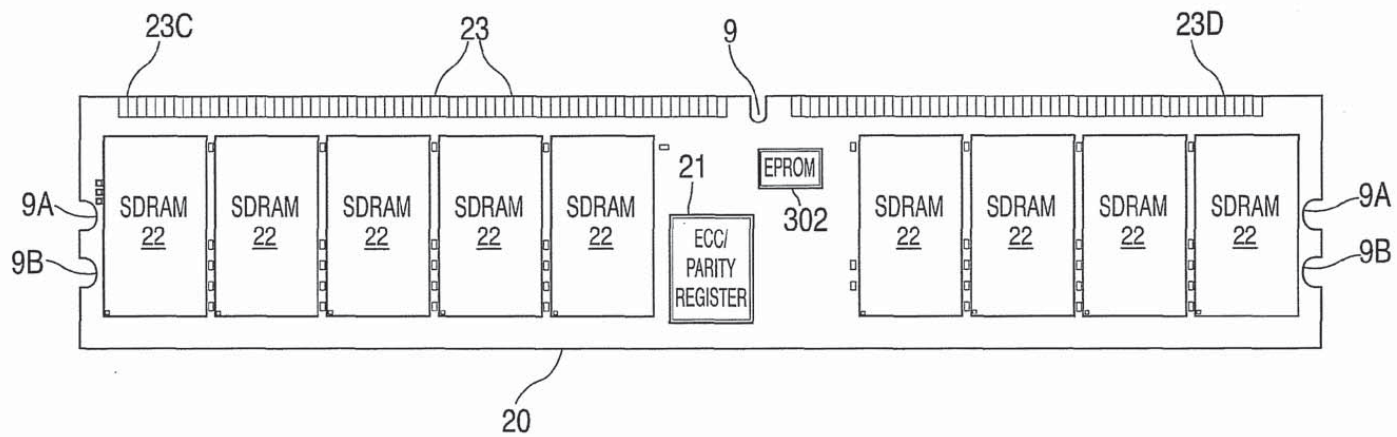
BACK SIDE OF DIMM - 72 PLANAR

FIG. 3B



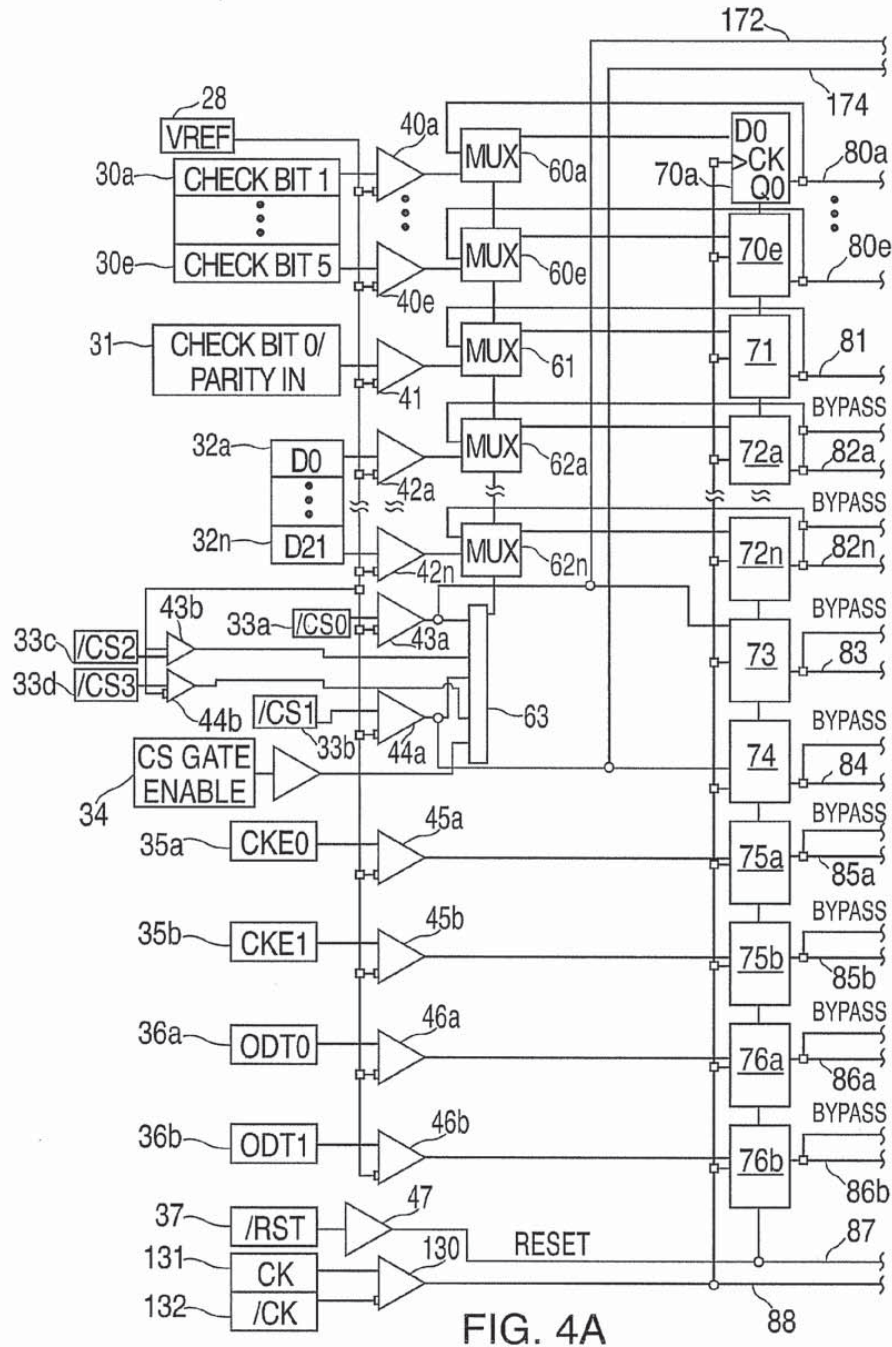
FRONT SIDE OF DIMM - 4 HIGH STACK

FIG. 3C



BACK SIDE OF DIMM - 4 HIGH STACK

FIG. 3D



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Ex. 1014, p. 8

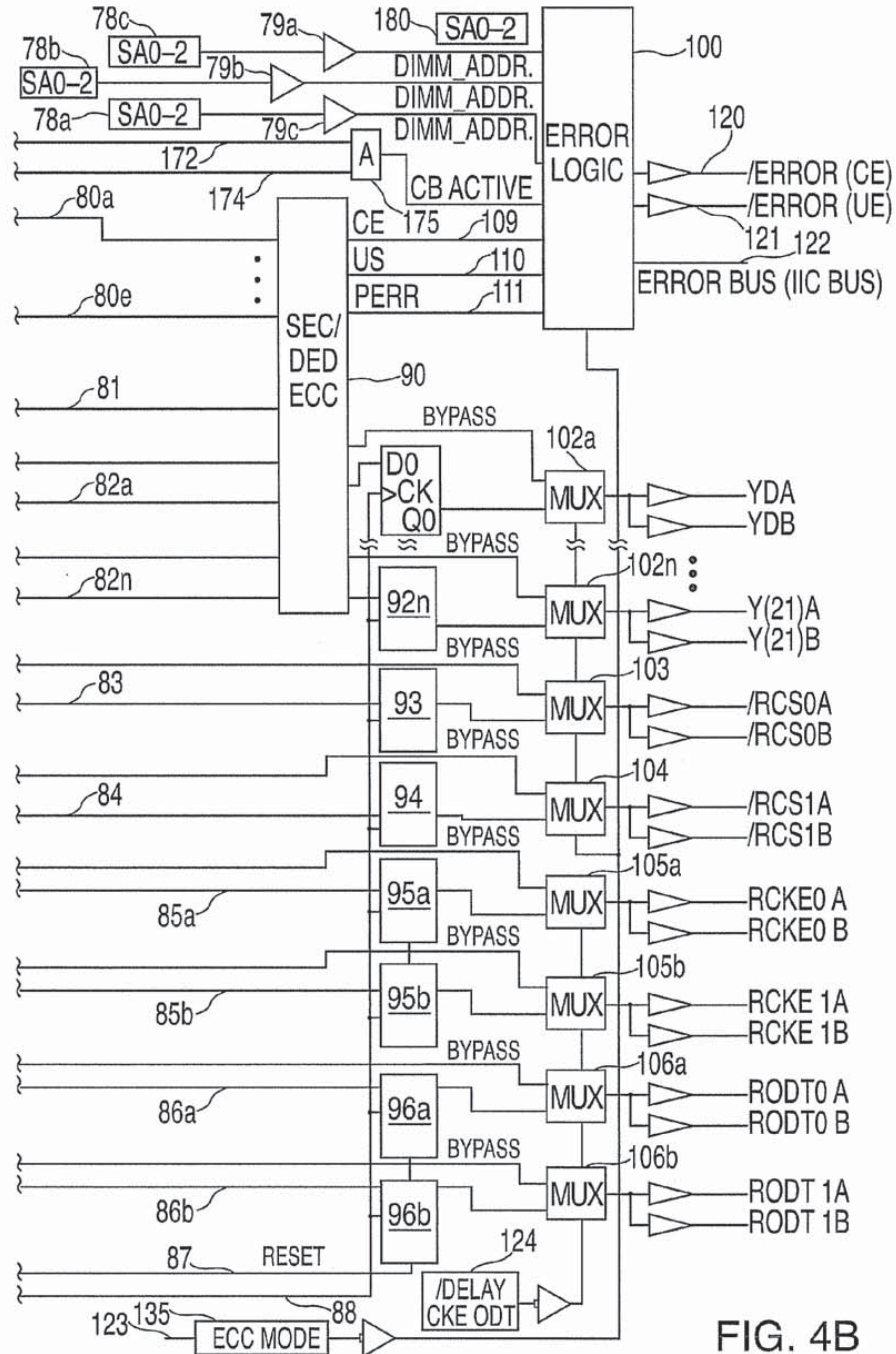


FIG. 4B

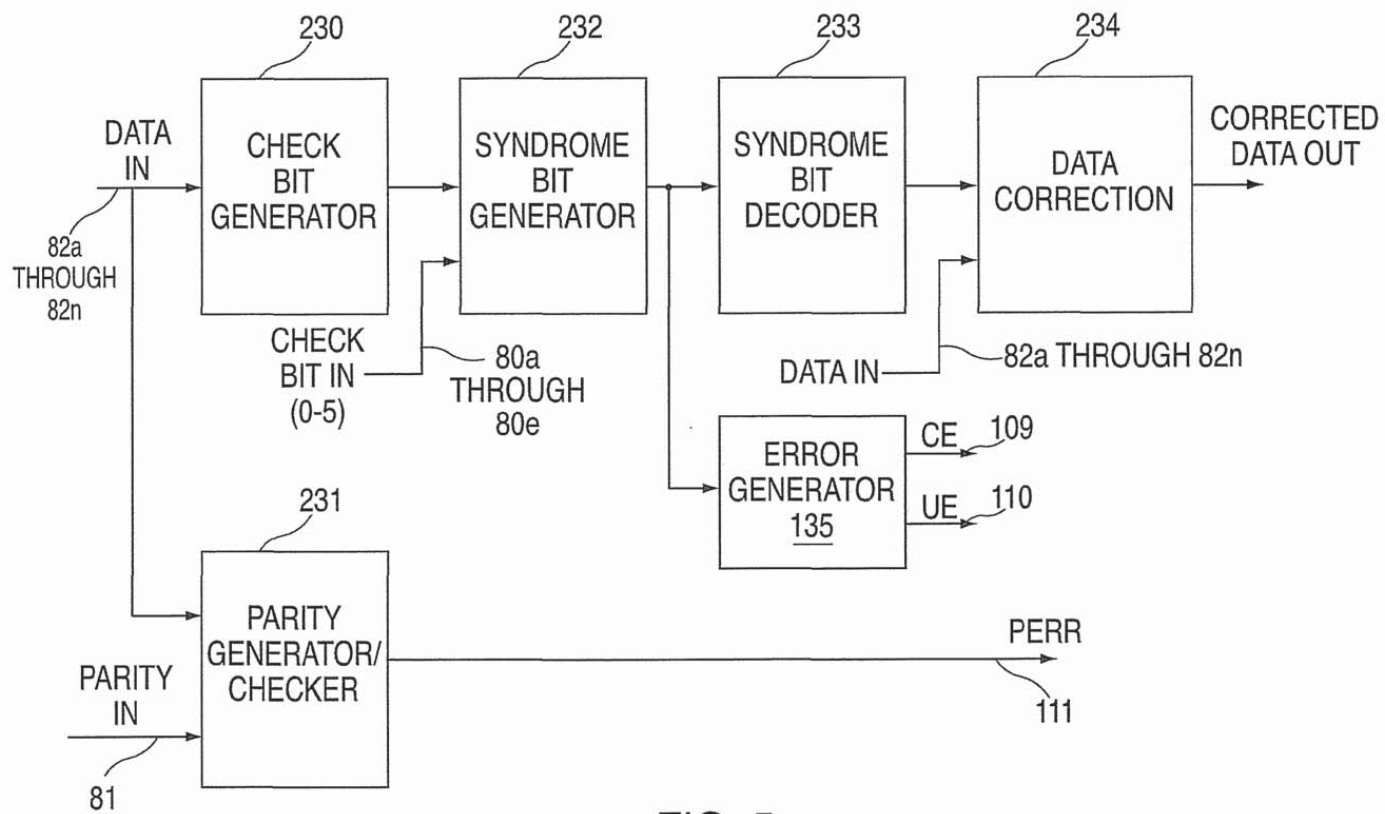


FIG. 5

	D0	D1	D2	D3	D4	D5	D6	D7	D8	D9	D10	D11	D12	D13	D14	D15	D16	D17	D18	D19	D20	D21	C0	C1	C2	C3	C4	C5
S0	1	1	1	0	0	1	1	0	1	0	0	0	0	1	1	0	0	1	0	1	0	1	1	0	0	0	0	0
S1	0	1	1	1	0	0	1	1	0	1	1	0	0	0	1	1	0	0	1	0	1	0	0	1	0	0	0	0
S2	0	0	1	1	1	1	0	1	1	0	1	1	0	0	0	0	1	0	0	1	1	1	0	0	1	0	0	0
S3	1	0	0	1	1	0	1	0	1	1	0	1	1	0	0	1	0	1	0	0	1	1	0	0	0	1	0	0
S4	1	1	0	0	1	1	0	1	0	1	0	0	1	1	0	0	1	0	1	0	1	1	0	0	0	0	1	0
S5	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	1

FIG. 6

SERVER DIMM PIN NUMBER	PIN NAME	SERVER DIMM PIN NUMBER	PIN NAME
1	Vref	139	Vref
2	SCL	140	SCL
3	SDA	141	SDA
4	UE	142	UE
5	CE	143	CE
6	VDD	144	VDD
7	ECCMODE	145	ECCMODE
8	DLY CKE/ODT	146	DLY CKE/ODT
9	CS GATE EN	147	CS GATE EN
10	GND	148	GND
11	DQ0	149	DQ4
12	DQ1	150	DQ5
13	GND	151	GND
14	DQS0*	152	DQS9
15	DQS0	153	DQS9*
16	GND	154	GND
17	DQ2	155	DQ6
18	DQ3	156	DQ7
19	GND	157	GND
20	VDD	158	VDD
21	GND	159	GND
22	DQ8	160	DQ12
23	DQ9	161	DQ13
24	GND	162	GND
25	DQS1*	163	DQS10
26	DQS1	164	DQS10*
27	GND	165	GND
28	DQ10	166	DQ14
29	DQ11	167	DQ15
30	GND	168	GND
31	DQ16	169	DQ20
32	DQ17	170	DQ21
33	GND	171	GND
34	DQS2*	172	DQS11
35	DQS2	173	DQS11*
36	GND	174	GND
37	DQ18	175	DQ22
38	DQ19	176	DQ23
39	GND	177	GND
40	RESET	178	RESET
41	VDD	179	VDD
42	GND	180	GND
43	DQ24	181	DQ28
44	DQ25	182	DQ29
45	GND	183	GND
46	DQS3*	184	DQS12
47	DQS3	185	DQS12*
48	GND	186	GND
49	DQ26	187	DQ30
50	DQ27	188	DQ31
51	GND	189	GND
52	CB0	190	CB4

FIG. 7A

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Ex. 1014, p. 12

53	CB1	191	CB5
54	GND	192	GND
55	DQS8*	193	DQS17
56	DQS8	194	DQS17*
57	GND	195	GND
58	CB2	196	CB6
59	CB3	197	CB7
60	GND	198	GND
61	VDD	199	VDD
62	CKE1	200	CKE1
63	CHKBT4	201	CHKBT1
64	CHKBT5	202	CHKBT3
65	CKE0	203	CKE0
66	VDD	204	VDD
67	A15	205	A14
68	BA2	206	A12
69	CHKBT0/PTY	207	A9
70	A11	208	CHKBT2
71	VDD	209	VDD
72	A7	210	A8
73	A5	211	A6
74	A4	212	A3
75	A2	213	A1
76	VDD	214	VDD
77	CK0	215	CK0
78	CK0B	216	CK0B
79	VDD	217	VDD
80	GND	218	GND
81	VDD	219	VDD
82	A10	220	A0
83	BA0	221	BA1
84	WE	222	RAS
85	VDD	223	VDD
86	CS0	224	CS0
87	CAS	225	CS3
88	ODT0	226	ODT0
89	CS3	227	A13
90	VDD	228	VDD
91	CS1	229	CS1
92	ODT1	230	ODT1
93	CS2	231	CS2
94	VDD	232	VDD
95	GND	233	GND
96	DQ32	234	DQ36
97	DQ33	235	DQ37
98	GND	236	GND
99	DQS4*	237	DQS13
100	DQS4	238	DQS13*
101	GND	239	GND
102	DQ34	240	DQ38

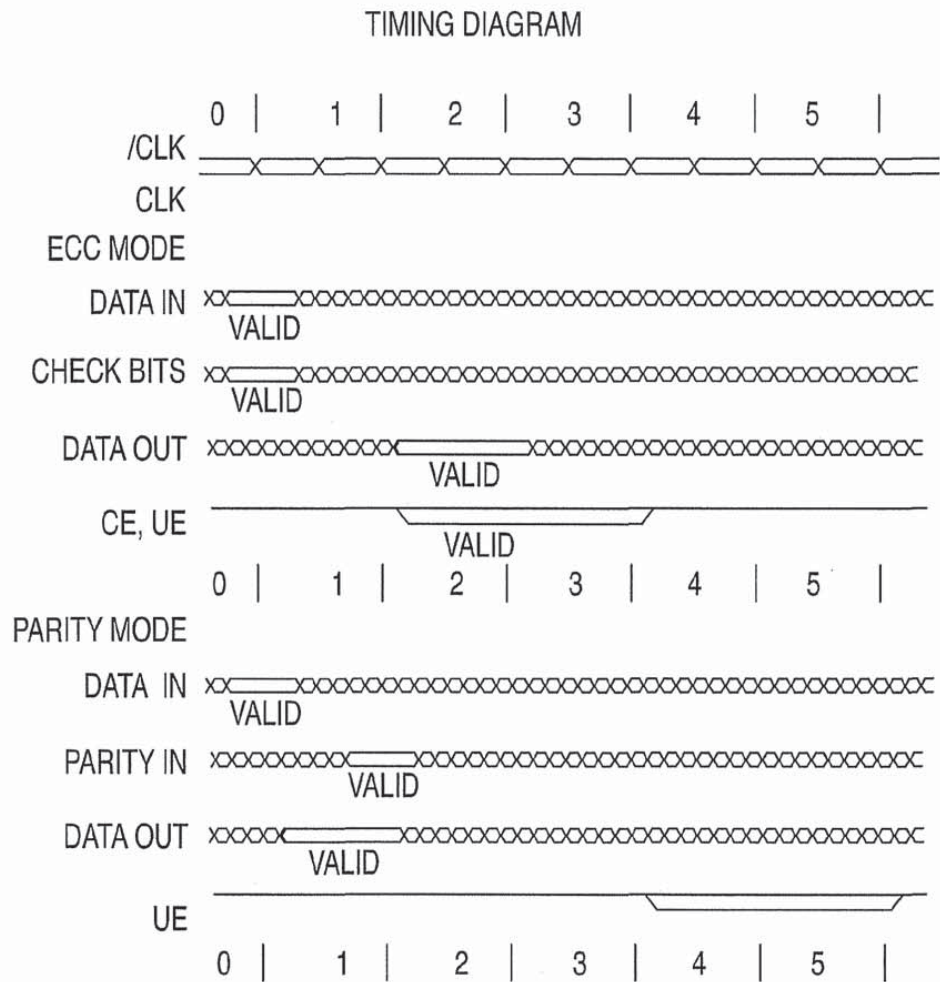
FIG. 7B

Petitioners SK hynix Inc., SK hynix America, Inc., and SK hynix memory solutions, Inc.
Ex. 1014, p. 13

103	DQ35	241	DQ39
104	GND	242	GND
105	DQ40	243	DQ44
106	DQ41	244	DQ45
107	GND	245	GND
108	DQS5*	246	DQS14
109	DQS5	247	DQS14*
110	GND	248	GND
111	DQ42	249	DQ46
112	DQ43	250	DQ47
113	GND	251	GND
114	DQ48	252	DQ52
115	DQ49	253	DQ53
116	GND	254	GND
117	DQS6*	255	DQS15
118	DQS6	256	DQS15*
119	GND	257	GND
120	DQ50	258	DQ54
121	DQ51	259	DQ55
122	GND	260	GND
123	DQ56	261	DQ60
124	DQ57	262	DQ61
125	GND	263	GND
126	DQS7*	264	DQS16
127	DQS7	265	DQS16*
128	GND	266	GND
129	DQ58	267	DQ62
130	DQ59	268	DQ63
131	GND	269	GND
132	VDD	270	VDD
133	SA2	271	SA2
134	VDDSPD	272	VDDSPD
135	SDA	273	SDA
136	SCL	274	SCL
137	SA0	275	SA0
138	SA1	276	SA1

FIG. 7C

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NOTES: CS GATING DISABLED
 PARITY IN AND CHECK BIT 0 SHARE A COMMON PIN (CHK0/ PARITY_IN)
 IF AN ERROR OCCURS, CE OR UE ARE DRIVEN LOW

FIG. 8

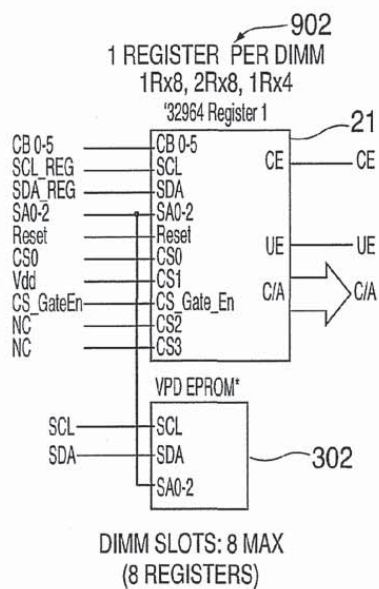
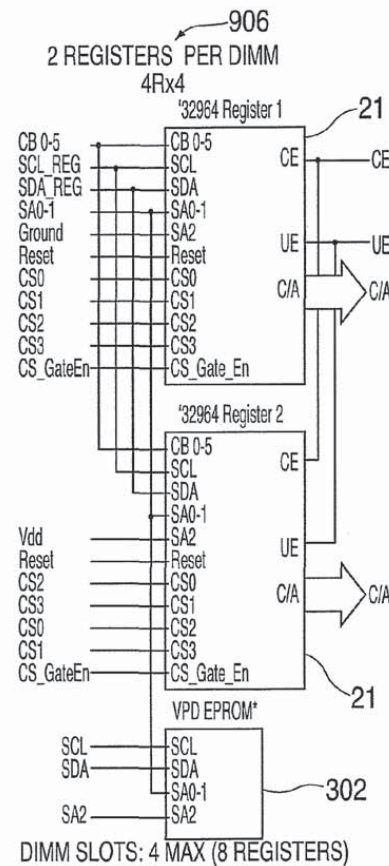
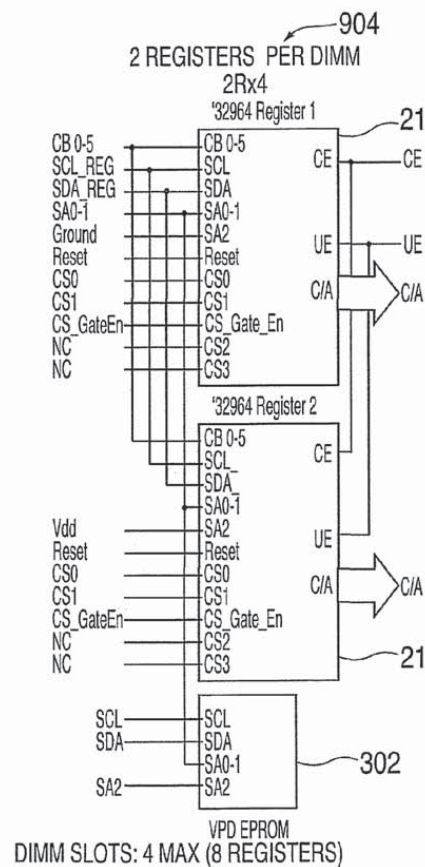


FIG. 9



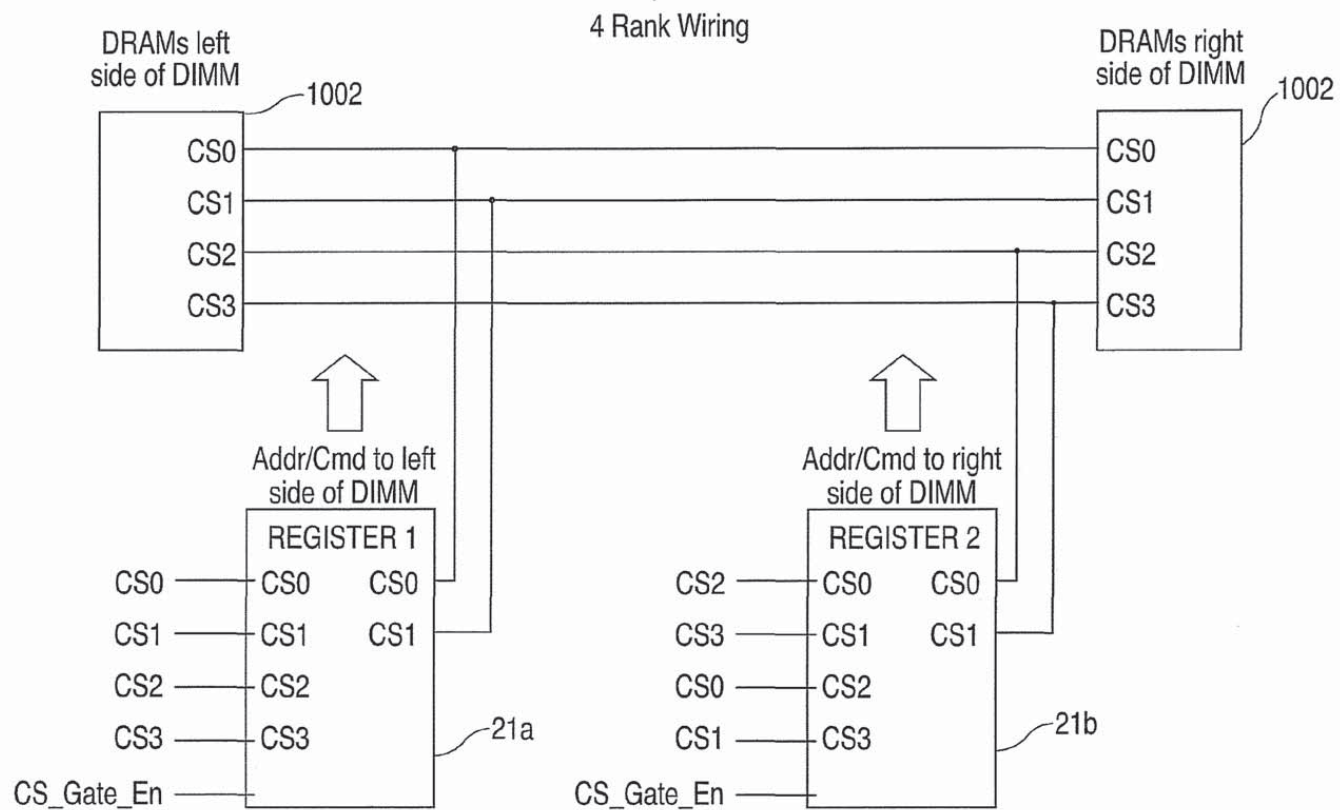


FIG. 10

DIMM SLOT	I2C ADDR	1 REGISTER I2C ADDR	2 REGISTERS I2C ADDR
1	0	0	0, 4
2	1	1	1, 5
3	2	2	2, 6
4	3	3	3, 7
5	4	4	-
6	5	5	-
7	6	6	-
8	7	7	-

FIG. 11

**HIGH DENSITY HIGH RELIABILITY
MEMORY MODULE WITH POWER GATING
AND A FAULT TOLERANT ADDRESS AND
COMMAND BUS**

BACKGROUND OF THE INVENTION

[0001] This invention relates generally to a high-density, high-reliability memory module with a fault tolerant address and command bus for use as a main memory that will achieve the degree of fault-tolerance and self-healing necessary for autonomic computing systems.

[0002] Memory modules are well known to the prior art and have been and are presently being used in practical applications such as in computers and other equipment using solid state memories.

[0003] Broadly speaking, currently available main memories offer bandwidths in the range of 1.6 to 2.6 GB/s, and although some memories provide for limited data path error correction most offer no means of any error correction targeting the interface between the memory controller and the memory subsystem. Furthermore, memory modules for server products and other higher-end computing systems usually include re-drive logic for address and command inputs, and clock re-synchronization and re-drive circuitry associated with the memory subsystems to permit these modules to contain higher memory device counts and to ensure accurate clock timings at each device on the memory assembly. Although these solutions provide systems with the ability to achieve the specified bandwidth objectives, the overall quantity and types of failures in the memory subsystem, outside the data path itself, has actually increased due to the added circuitry associated with each memory device. Simultaneously, as these computing systems are more widely utilized in business, many applications simply cannot accept periodic unplanned system outages caused by failed memory modules. Thus the emphasis and need for improved overall system reliability is increasing dramatically and requires a comprehensive system solution that includes both a high degree of fault tolerance and overall reliability. Further, a corresponding need for greater system memory density is also required to achieve the system performance and operation throughput required in modern business applications, as well as to maximize the return on investment by extending the utility of the system by offering memory density improvements.

[0004] The present invention provides such a comprehensive system solution that includes the capability of high memory density and a high degree of fault tolerance and the overall differentiated system reliability long desired in the server market.

[0005] Existing solutions have memory module density that is typically limited to 18 or 36 devices for each memory module—with this limit based on such elements as the memory device package size, the memory module physical dimensions, the re-drive capability of the buffer, re-drive or register device, the power dissipation of the completed memory subsystem and/or module, etc. Other possible fault-tolerant improvement methods such as memory mirroring, symbol slicing and extensive forms of fault rejection and redundancy, provide enhanced memory subsystem reliability, but, due to negative impacts such as increased cost, power, and reduced performance, have been considered only for niche applications where price is not of high importance as these subsystem quality enhancements are very expensive

to implement. Therefore solutions suitable for the low or midrange server markets have not been available.

[0006] Consequently the industry has long sought a simple, relatively inexpensive and reliable solution that provides high memory density with differentiated product quality, that provides an adequate level of asset-protection that does not endanger the reliability of the system through the use of reduced-function memory assemblies and yet is cost competitive.

BRIEF SUMMARY OF THE INVENTION

[0007] The present invention is directed to a high density high reliability memory controller/interface module, provided with a high degree of compatibility with industry-standard solutions, capable of meeting the desired density, performance and reliability requirements and interfacing with the presently available memory modules, as well as with existing or enhanced support devices. The present invention accomplishes all these ends, resulting in a high density and enhanced reliability memory solution at low cost.

[0008] An object of the present invention is to provide an enhanced 28 bit 1:2 register (also referred to herein as a "buffer") that supports 4 ranks of memory devices, intended for use with memory subsystems such as Dual Inline Memory Modules (DIMMs) having Dynamic Random Access Memory (DRAM) chips thereon. The register of the present invention has added thereto additional command inputs, error correction code (ECC) logic to identify and correct single bit errors on the command or address bus, and permit continuous memory operation independent of the existence of these errors.

[0009] Another object of the present invention is to include in such DIMMs error latches and an error reporting mode whereby the system may interrogate the device to determine the error condition thereby allowing accurate fault determination and preventive maintenance—thereby reducing unplanned system outages.

[0010] A further object of the present invention is to include redundant contacts on all connectors/DIMM interconnects that would otherwise be considered single points of failure whereby an intermittent or permanent contact failure would result in an unplanned system outage.

[0011] Still another object of the present invention is to provide the DIMM with key operational features such as chip select gating of key inputs and programmable delay for un-gated inputs, thereby reducing module power and offering increased operational flexibility.

[0012] A further object of the present invention is to provide a DIMM that can be readily utilized in presently available controllers in a manner most applicable to the market needs.

[0013] Another further object of the present invention is to have a DIMM that uses connectors similar to those presently in use so that prior art contacts, molds, handlers and related production tools can continue to be used such that the modules can be more cheaply produced with additional density while providing value-added reliability, and other value-add attributes, such as a higher memory packaging density with minimal additional production costs.

[0014] Another further object of the present invention is to have a buffer which is operable with up to 4 ranks of memory devices, that is also interchangeable with previously developed buffers limited to no more than 2 ranks of

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memory devices, and can be used as a direct replacement for said previously developed buffers on DIMMs that utilized said buffers—thereby eliminating the need to produce or procure two types of buffer devices or to re-design existing memory modules.

[0015] The DIMM of the present invention is comprised of a printed circuit board having a front side and a back side and a plurality of double data rate (DDR) DRAMs or synchronous dynamic random access memories (SDRAMs) affixed to both the front surface and the back surface. On a first edge of the front surface of said board there is provided one hundred and thirty eight (138) contacts for connecting circuitry, external to the card, to the SDRAMs and related devices on the DIMM and on the same first edge on the rear side of the card there is provided an additional one hundred and thirty eight (138) external circuitry connecting contacts so that the board has a total of two hundred and seventy six (276) external circuitry connecting contacts thereon. The contact means provided on the front and the back sides of the printed circuit card provide for electrically connecting the external circuitry to the SDRAMs in a direct or indirect manner.

[0016] Still another further object of the present invention is to provide a server memory structure having a dual inline memory module or DIMM provided with selective redundant contacts, a phase lock loop, 2 or 32K bit serial electrically erasable programmable read only memory (EEPROM) and a 28 bit, 1 to 2 register having error correction code (ECC), parity checking, a multi-byte fault reporting register, read via an independent bus, and real time error lines for both correctable errors and uncorrectable error conditions. More particularly the server of the present invention comprises a novel DIMM provided with a new and unique ECC/ Parity Register that is operable with 1 to 4 memory ranks, coupled to a memory interface chip which is in turn coupled to a memory controller or processor such that the memory controller sends address and command information to the buffer (or register) via address/command lines together with check bits for error correction purposes to the ECC/ Parity register.

[0017] Still another object of the invention is to provide for detecting if the module installed in the server can monitor the address and control bus integrity, correct errors on the address and control bus, report errors and log and counts errors.

[0018] Still another object of the invention is to provide for Parity error reporting in which the parity signal is delivered one cycle after the address and command to which it applies, and the error line be driven low two clocks after the address and command bits are driven to the DRAMs from the register on the DIMM. After holding the error line low for only 2 clock cycles, the driver can be disabled and the output permitted to return to an un-driven state (high impedance) thus allowing this line to be shared by multiple modules.

[0019] Still further the invention provides means for and a method for adjusting the propagation delay, for signals on the memory module that are not included in the ECC circuitry, such that the signals can be selectively re-driven by the buffer within one or two clock cycles.

[0020] Still further the present invention permits operation of the memory module in parity mode, such that unused ECC check bit inputs are held at a low level thus ensuring that these inputs are at a known and quiescent state.

[0021] Still further the present invention provides for reducing the probability of Single Point of Failures occurring by providing selected signals with redundant contacts directly on the opposite side of the DIMM from the original finction contact thereby reducing the probability of a contact failure resulting in an unplanned system outage.

[0022] Still further the present invention provides for operating a module of the present invention consistent with conventional non-ECC protected modules, by removing the secondary registers (post-ECC) from the delay path by setting the /ECC Mode control pin to a high level.

[0023] These objects, features and advantages of the present invention will be become further apparent to those skilled in the art from the following detailed description taken in conjunction with the accompanying drawings wherein:

BRIEF DESCRIPTION OF THE DRAWINGS

[0024] FIG. 1 is a block diagram of a typical server memory arrangement;

[0025] FIG. 2 is a block diagram of the enhanced server memory arrangement of the present invention;

[0026] FIGS. 3A and 3B are plan views respectively of the front and back of the two hundred and seventy six (276) pin dual inline memory module (DIMM) of the present invention that utilizes up to 72 planar DRAMS; and FIGS. 3C and 3D are plan views respectively of the front and back of the 276 pin DIMM of the present invention that utilizes up to eighteen four high DRAM stacks;

[0027] FIGS. 4A and 4B are schematic views of the ECC/ Parity register, shown in FIG. 3A;

[0028] FIG. 5 is a block diagram of the single error correction/ double error detection error correction code (SEC/DED ECC) circuit of FIG. 4B;

[0029] FIG. 6 describes, in H—matrix form, the preferred ECC code selected for the module of FIG. 3;

[0030] FIGS. 7A, 7B and 7C show the designated contacts or pin connections for the DIMM of FIGS. 3A and 3B;

[0031] FIG. 8 shows the timing diagram used with the present invention;

[0032] FIG. 9 shows the buffer connections and total number of buffers used in a system when the buffer of the present invention is used on 1, 2 and 4 rank DIMMs;

[0033] FIG. 10 shows the CS wiring between the buffers and the memory devices on the right and left side of the card, for a 4 rank DIMM of the present invention; and

[0034] FIG. 11 shows the IIC addresses that are utilized to access the error registers on the one or two buffers of the present invention.

DETAILED DESCRIPTION OF EXEMPLARY EMBODIMENTS

[0035] A full appreciation of the features and advantages of the present invention can best be gained by reference to the drawings and more particularly to the figures where: FIG. 1 is a block diagram of a typical server memory arrangement; FIG. 2 is a block diagram of the enhanced server memory arrangement of the present invention; FIGS. 3A and 3B are plan views respectively of the front and back of a 4 rank planar 276 contact dual inline memory module (DIMM) of the present invention; FIGS. 3C and 3D are plan views respectively of the front and back of a 4 rank four high stacked 276 contact DIMM of the present invention; FIGS.

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4A and 4B are schematic views of the 4 rank-optimized buffer/register, parity and error correction circuits shown in FIGS. 3A and 3B (and FIGS. 3C and 3D); FIG. 5 is a block diagram of the single error correction/double error detection error correction code (SEC/DED ECC) circuit of FIG. 4B; FIG. 6 describes, in H—matrix, form the preferred ECC code selected for the module of FIGS. 3A and 3C; FIGS. 7A, 7B and 7C show the designated pin connections for the DIMM of FIGS. 3A and 3B (and FIGS. 3C and 3D). FIG. 8 shows the timing diagram used with the present invention. FIG. 9 shows the buffer connections and total number of buffers used in a system when the buffer of the present invention is used on 1, 2 and 4 rank DIMMs; FIG. 10 shows the CS wiring between the buffers and the memory devices on the right and left side of the card, for a 4 rank DIMM of the present invention and FIG. 11 is a table showing the IIC addresses that would be used to access the error registers on the one or two buffers of the present invention.

[0036] In FIG. 1 there is illustrated, in schematic form, a block diagram of a typical server memory arrangement as might be found in any currently available server which can employ a plurality of memory subsystems, shown here in the form of dual inline memory modules (DIMMs). It should be understood that many such DIMMs would be used in actual practice but for ease of illustration only one prior art DIMM 10 is shown in FIG. 1. DIMM 10 is a printed circuit card on which there is provided a plurality of either synchronous dynamic random access memories or dynamic random access memories circuits 11, herein after collectively referred to herein as memory devices, or as DRAM(s). Each DRAM 11 on the DIMM 10 has a plurality of input/output pins that are coupled, via the printed circuitry on the DIMM 10 to the contacts on the DIMM 10 and these contacts are further coupled, via a data line 15, to a memory interface chip 18 and to a memory controller or processor 19. Each DRAM on the DIMM is further, coupled via such DIMM contacts, to a buffer/register 12 and to a phase locked loop circuit 14 on the DIMM. The phase locked loop 14 (PLL) is connected via clock line 17 to the memory interface chip 18. The register 12 is also coupled to the memory interface chip 18 via an address and command (CMD) bus 16. The memory interface chip 18 is coupled to the memory controller 19 via the data line 15, address and command line 16 and clock line 17. It should be understood that although only one such DIMM is shown in this figure that in actuality the server would contain many such DIMMs. Such other DIMMs would be coupled in a like manner to the memory interface chip 18 and memory controller 19 via data, address and command lines, and may be connected in a multi-drop, cascade interconnect or other connection method, depending on the system structure and buffer functionality. Since such servers and their operation are well known to those skilled in the art, further description of such servers and their operation is not deemed necessary.

[0037] Turning now to FIGS. 2, 3A, 3B, 3C, 3D, 4A, 4B, 5, 8, 9, 10 and 11 the enhanced server memory arrangement of the present invention will be described.

[0038] In FIG. 2 there is illustrated, in schematic form, a block diagram of a server memory arrangement employing the present invention. In this FIG. 2 the server comprises a novel DIMM 20 provided with a novel ECC/Parity Buffer chip 21 (also referred to as a “buffer device”) coupled to the memory interface chip 18 which is in turn coupled to the memory controller or processor 19. It should be understood

that the chip 21 need not include both the ECC function and the parity function. For example, the chip 21 could have just the 4 rank addressability alone, the ECC function alone or just the parity function alone and still operate in accordance with the present invention. More specifically, as shown in this FIG. 2, the memory interface chip 18 sends and receives data from the DIMMs via the data line 15 and sends address and commands via line 16. The memory interface chip 18 then sends and receives data, via line 15, to the memory devices, or DRAMs 22 and sends address and command information to the register chip 21 via add/cmd line 16 and check bits for error correction purposes to the ECC/Parity register chip 21 via line 25. In this configuration, the check bits and/or parity bits associated with the ECC/Parity register chip 21 are developed in the memory interface chip 18, although in other embodiments these bits could be developed in the memory controller or processor 19, be communicated to the memory interface chip as a subset of the information on line 16 and the memory interface would then re-drive this information to the memory module on line 25.

[0039] FIGS. 3A and 3B show respectively the front and back views of the novel 4 rank DIMM 20 of the present invention. Generally speaking DIMMs are printed circuit cards designed to carry a plurality of DRAMs 22 thereon and the DRAM output pins (not shown) are connected via the printed circuit to selected connectors 23 along the edge of both the back and front sides of the card and are often provided with a single indexing key or notch 9 on the connector edge. The use and manufacture of such DIMMs is well known and need not be further described herein. The DIMM 20 of the present invention however is novel and is designed to address the need for very high memory module density, as well as several of the most significant contributors to unplanned and often catastrophic system outages encountered in the prior art DIMMs. The improvements in the DIMM 20 of the present invention are realized especially by enlarging the length of DIMM 20 to between 149 mm and 153 mm. Nominally the DIMM 20 is 151.35 mm (5.97 inches) long and its width is 54.6 mm (2.16 inches). The width of the DIMM 20 is sufficient in width to accommodate the four rows of DRAMs 22 installed thereon, in addition to the two buffers 21 (one buffer is mounted on each side in the exemplary embodiment, as shown in FIGS. 3A and 3B), the PLL 24 and passive devices (not shown) such as resistors and capacitors, but must also be no wider than permitted by the available system physical dimensions for the module(s). The length of the DIMM 20 however must be such that the DIMM 20 can accommodate additional signal contacts, up to 138, as well as up to thirty-six planar DRAMs 26 having a nominal body size of up to 11.5 mm wide by 11 mm tall and have a locating key or notch 9 a distance of between 82.675 mm from one end of the DIMM 20 and 68.675 mm from the other end of the DIMM as shown. Again it should be understood that these dimensions are nominal and may vary plus or minus 3 mm in various implementations. The DIMM 20 can also be provided with additional notches 9a and 9b on each side, i.e., the shorter edges of the DIMM 20. These dimensions permit the DIMM, of the invention, to accommodate placing up to thirty-six planar DRAMs 22 on the front surface and up to an additional thirty-six such DRAMs 22 on the rear surface. Further, as shown in FIG. 3A, on the front of each DIMM 20, in addition to the DRAMs, there is positioned a phase locked loop (PLL) chip 24 and the novel ECC/Parity Buffer chip 21 of the present

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invention. This novel ECC/Parity Buffer chip 21 will be further described below and in detail in conjunction with FIGS. 4A and 4B. It should be understood that the PLL chip 24 can be eliminated if its circuitry is provided on the buffer chip 21 or within the same package as the buffer chip 21 (i.e. alongside the chip, above the chip, below the chip, etc). In exemplary embodiments, the DIMM 20 depicted in FIGS. 3A and 3B also includes an EPROM 302 which is used for the storage of memory module attribute information (commonly referred to as an SPD data, when associated with memory modules), with the EPROM's IIC interface also shared, in this module, with the novel ECC/Parity Buffer chip, enabling one means for accessing status registers on the buffer chip(s).

[0040] Alternate configurations of the 4 rank DIMM 20 may be implemented by exemplary embodiments. See, for examples FIGS. 3C and 3D which depict front and back plan views of a 4 rank four high stacked 276 contact DIMM 20 of the present invention. In the embodiment depicted in FIG. 3D, the DIMM 20 also includes an EPROM device 302 which has the same function as device 302 in FIG. 3A, which includes enabling one means for accessing status registers on the buffer chip(s). As will be evident to those skilled in the art, other configurations for providing up to 4 ranks of memory may also be implemented without departing from the scope of the invention. For example, a 4 rank two high, stacked 276 contact DIMM 20 may be implemented by exemplary embodiments.

[0041] This new, improved, larger sized DIMM 20, shown in these FIGS. 3A, 3B, 3C and 3D also achieves a further significant improvement in the interconnect failure rate for the larger size of the module permits the connector system to accommodate two hundred and seventy-six contacts or pins 23. These pins are numbered and coupled to respective inputs as shown in FIGS. 7a, 7b, and 7c. Contact or pin number one (1) is identified and shown in FIG. 3A as contact 23A and is on the left hand side of the front side of the DIMM 20 and is positioned approximately 5.175 mm from the left edge of the DIMM 20 and 77.5 mm from the center of the notch 9. Contact or pin number one hundred and thirty-eight (138) is identified and shown in FIG. 3A as contact 23B and is on the right hand side of the front side of the DIMM 20 and is positioned approximately 5.175 mm from the right edge of the DIMM 20 and approximately 63.5 mm from the center of the notch 9. Contact or pin number one hundred and thirty-nine (139) is identified and shown in FIG. 3B as contact 23C and is directly opposite contact number one 23A and is also positioned approximately 5.175 mm from the right edge of the back of DIMM 20 and is also 77.5 mm from the center of the notch 9. Contact or pin number two hundred and seventy-six (276) is identified in shown in FIG. 3B as contact 23D and is directly opposite contact number one hundred and thirty-eight 23B and is also positioned approximately 5.175 mm from the left edge of the back of DIMM 20 and 63.5 mm from the center of the notch 9. The greater size of this DIMM 20 also accommodates the inclusion of a new and larger ECC/Parity buffer chip 21 required by the present invention. Because the two hundred and seventy-six contacts or pins 23 on this larger DIMM 20 are more than sufficient to meet the needs of all the circuitry on the DIMM 20 this means that the DIMM 20 provides extra or redundant contacts. These extra or redundant contacts or pins 23 can now be used to provide additional protection for certain selected signal or voltage lines, for

which error correction is not possible. The present invention, by providing such redundant contacts, effectively eliminates concerns such as contact failures on clock inputs, CS, CKE, and ODT inputs, Vref inputs, and other signals not protected by ECC. Other benefits include the elimination or reduction of concerns regarding power supply noise and/or voltage drops due to scarcity of voltage (VDD) contacts in the data region as well providing additional ground pins in the address/control region on the DIMM 20. The larger contact count of the present invention also permits the DIMM 20 to be wired such that they are consistent with prior art DIMMs. The additional contacts 23 also permit the inclusion of ECC check bits, associated with address and command inputs, allowing for real-time system monitoring of faults associated with these inputs, as well as system interrogation of fault counts and attributes. These faults would result in catastrophic system outages in conventional prior art systems using the smaller prior art DIMMs.

[0042] It should be understood that although only one DIMM 10 and 20 is shown in the FIGS. 1 and 2 that, in actuality, the server would contain many such DIMMs. As noted above, the DIMM 20, of the present invention, is provided with a plurality of SDRAMs 22, a phase locked loop circuit 24 and the ECC/Parity buffer chips 21. The ECC/Parity buffer chips 21 on DIMM 20 include unique error correction code (ECC) circuitry that is coupled to the memory interface chip 18 via line 25 to provide even greater significant reliability enhancement to such servers. The inclusion of this new, improved error correction code (ECC) circuitry results in a significant reduction in interconnect failure. Memory interface chip 18 connects to both of the ECC/Parity buffer chips 21 through lines 25 and 16 and to PLL 24 through line (17). In exemplary embodiments, such as the one depicted in FIGS. 3A and 3B, one copy of the address and command outputs from buffer chip 21 located on the front of the DIMM 20 connect to the 20 (S)DRAMs to the left of the buffer chip 21 (10 DRAMs on the front and 10 DRAMs located behind said 10 DRAMs on the back of the DIMM), and the second copy connect to the 16 DRAMs to the right of the buffer (8 DRAMs on the front and 8 DRAMs located behind said 8 DRAMs on the back of the DIMM). The buffer chip 21 located on the back of the DIMM is wired in a similar manner, with one copy of the address and command outputs from the buffer connected to 20 DRAMs (10 on the front and 10 on the back) and a second copy connected to 16 DRAMs (8 on the front and 8 on the back). In exemplary embodiments, such as the one depicted in FIGS. 3C and 3D, one copy of the address and command outputs from buffer chip 21 located on the front of the DIMM 20 connect to the 20 DRAMs to the left of the buffer (2 DRAM stacks on the front and 3 DRAM stacks generally located behind said 2 DRAM stacks on the back of the DIMM), and the second copy connects to the 20 DRAMs to the left of the buffer (3 DRAM stacks on the front and to the right of the buffer and 2 DRAM stacks located generally behind said 3 DRAM stacks on the back of the DIMM). The buffer chip 21 located on the back of the DIMM is wired in a similar manner, with one copy of the address and command outputs from the buffer connected to 16 DRAMs to the right (2 DRAM stacks on the front and 2 DRAM stacks on the back) and a second copy connected to 16 DRAMs to the right (2 DRAM stacks on the front and 2 DRAM stacks on the back). PLL 24 connects to each of the SDRAMs 22.

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[0043] In an exemplary embodiment, a first set of buffer chip outputs connect to the SDRAM devices placed directly to the right of a buffer chip 21 on the front side of the DIMM 20 and to the memory devices on the backside of the DIMM 20 and on the same end of the DIMM 20 as the aforementioned memory devices, and a second set of buffer outputs connect to the devices to the left of the buffer on the front side of the DIMM 20 and to the memory devices, or SDRAMs 22, on the backside of the DIMM 20 and on the same end of the DIMM 20 as these memory devices. Alternate exemplary wiring embodiments may be used, while achieving the benefits described herein. For example, in FIGS. 3A-3D, address and command outputs from buffer 21, located on the front of the DIMM, may wire only to (S)DRAMs located on the front of the DIMM, while address and command outputs from buffer 21, located on the back of the DIMM, may wire only to (S)DRAMs located on the back of the DIMM. Other wiring methods may be used for address and command, while achieving many of the objectives cited in the teachings.

[0044] FIGS. 4A and 4B together comprise a schematic view of the novel ECC/Parity buffer chip 21 on DIMM 20 where, for clarity in description, it is shown as comprised of two distinct sections 21a and 21b. FIG. 4A shows the input portion of the enhanced function 4 rank-enabled 28 bit 1:2 buffer/register segment 21a of the present invention and FIG. 4B shows the output portion and error correction code circuit segment 21b. As depicted in FIGS. 4A and 4B, the buffer chip (also referred to herein as the buffer device) includes a plurality of buffer circuits (e.g., receivers, multiplexers, latches, etc.) for driving the address and command data. The error correction code circuit ECC segment 21b, shown in FIG. 4B, corrects for single bit errors and thus permits continuous memory operation independent of the existence of these errors. This ECC segment also includes a parity operating mode circuitry together and error reporting circuitry. The novel ECC/Parity buffer 21 on DIMM 20 thus provides leading-edge performance and reliability and key operational features different from and unavailable from the prior art while retaining timing requirements generally consistent with devices such as the JEDEC 14 bit 1:2 DDR II register.

[0045] More particularly, the register segment 21a contains a plurality of so called differential bit receivers 40a through 40e, 41, 42a through 42n, 43a, 43b, 44a, 44b, 45a, 45b, 46a and 46b and a single amplifier 47. Each of these differential receivers 40a through 40e, 41, 42a through 42n, 43a, 43b, 44a, 44b, 45a, 45b, 46a and 46b has two inputs and a single output. One of the inputs of each differential receiver 40a through 40e, 41, 42a through 42n, 43a, 43b, 44a, 44b, 45a, 45b, 46a and 46b is coupled to a reference voltage source 28. The second input of each of the differential receivers 40a through 40e, 41, 42a through 42n, 43a, 43b, 44a, 44b, 45a, 45b, 46a and 46b are coupled to respective inputs 30a through 30e, 31, 32a through 32n, 33a, 33b, 33c, 34, 35a, 35b, 36a and 36b.

[0046] Receiver set 40a through 40e is comprised of five receivers of which only the first and the last receivers 40a and 40e are shown. Receivers 40a through 40e have their second inputs respectively coupled to respective check bit lines 30a through 30e and their outputs connected through respective primary multiplexers 60a through 60e to the inputs of respective primary latches 70a through 70e. Typically the check bit lines are contained in a bus that contains

a set of five such check bit lines. However, for simplification of the drawing and ease of description only, FIG. 4A shows only the first and the last check bit lines 30a and 30e of the set and the first and last of the receivers 40a through 40e. It being understood that each receiver in the set 40a through 40e has one of its respective inputs coupled to a respective one of a set of check bit input lines 30a through 30e and its output to a respective one of a set of three input multiplexers and thence to a respective one of a set of three input primary latches.

[0047] The second input of the differential receiver 41 is coupled to a check bit 0/Parity_{in} in signal line 31.

[0048] Receiver set 42a through 42n is comprised of twenty-two receivers coupled to a data line bus typically containing twenty two data lines 32a through 32n. However, for simplification of the drawing and ease of description only, FIG. 4A shows only the first and the last data lines 32a and 32n of the set and the first and last of the receivers 42a through 42n are shown in the drawing. The first receiver 42a is shown as having its first input coupled to data bit line 32a and its output coupled to the first input of multiplexer 62a whose output is coupled to a first input of primary latch 72a and the last receiver 42n is shown as having its first input coupled to data bit line 32n and its output coupled to the first input of multiplexer 62n whose output is coupled to a first input of primary latch 72n. Each respective receiver in set 42a through 42n has an input coupled to a respective one of data lines in set 32a through 32n and their outputs connected through respective primary multiplexers 42a through 42n to the inputs of respective primary latches 62a through 62n. All the primary multiplexers and latches in the set 42a through 42n are identical to those shown connected to receivers 42a and 42n. Thus each receiver in the set has one of its respective inputs coupled to a respective one of a set of data bit input lines and its output to a respective one of a set of two input multiplexers and thence to a respective one of a set of primary latches. These signals are inputted from the memory interface chip 18 in FIG. 2 and are re-driven only when one or more of the inputs 33a, 33b, or 34 are low.

[0049] As previously noted, the second input of the differential receiver 41 is coupled to a check bit 0/Parity_{in} in signal line 31. The output of the differential receiver 41 is coupled to an input of multiplexer 61 whose output is coupled to a primary latch 71. The check bit 0/Parity_{in} in signal is interpreted as an ECC check bit from the memory controller or as a parity bit depending on the setting of ECC mode input 136 (FIG. 4B) Clock inputs 131 are fed to all the primary latches 70a through 70e, 71, 72a through 72n, 73, 74, 75a, 75b, 76a and 76b. The Check bits 1-5 at inputs 30a through 30e are in a don't care state when the register is being operated in parity mode and will be held low. When these inputs are operated in parity mode, a parity in signal will be provided on the Check bit 0/Parity_{in} in signal line 31 and maintain odd parity across the data inputs 32a through 32n, at the rising edge of the clock signal (CK) at input 131 that immediately follows the rising edge of clock 131 that occurred simultaneously with the associated data inputs 32a through 32n.

[0050] The second inputs of the differential receivers 43a, 43b, 44a and 44b are respectively coupled to chip select lines /CS0, /CS2, /CS1 and /CS3 and the outputs of the differential receivers 43a and 44a are coupled respectively to the first inputs of primary latches 73 and 74 as well as to the first and third inputs of a five input select NAND gate 63,

while the outputs of the differential receivers 43b and 44b are coupled only to the second and fourth inputs of the five input select NAND gate 63. The output of NAND gate 63 is coupled to the selection input of the multiplexers 60a through 60e, 61 and 62a through 62n. These lines initiate DRAM address/command decodes and as such at least one will be low when a valid address/command signal is present and the register can be programmed to re-drive all the data inputs when at least one chip select input (/CS0, /CS1, /CS2, /CS3) 33a, 33b, 33c, 33d is low. The fifth input of this NAND gate 63 is coupled to CS gate enable circuit 34 which can be set low to cause multiplexers 60a through 60e to pass signals from receivers 32a through 32n independent of the levels on inputs 33a, 33b, 33c and 33d.

[0051] The output of differential receivers 43a and 44a are also respectively coupled through the lines 172 and 174 and the AND gate 175 (FIG. 4B) whose output is coupled to the error logic circuit 100 also shown in FIG. 4b.

[0052] Receiver 45a has an input coupled to the clock enable signal source 35a (CKE0) and an output coupled to the primary latch 75a.

[0053] Receiver 45b has an input coupled to the clock enable signal source 35b (CKE1) and an output coupled to the primary latch 75b.

[0054] Receiver 46a has an input coupled to the on die termination line signal input line 36a (ODT0) and an output coupled to the primary latch 76a.

[0055] Receiver 46b has an input coupled to the on die termination line signal line 36b (ODT1) and an output coupled to the primary latch 76b.

[0056] Receiver 47 has an input coupled to the reset (/RST) signal line 37. The inputs 35a and 35b (CKE0, CKE1) 36a and 36b (ODT0, ODT1) are provided from the memory interface chip 18 and are not associated with the Chip Select (CS) inputs 33a, 33b, 33c and 33d, and the signal from source 37 (/RST) driving amplifier 47 is an asynchronous reset input and, when low, resets all the primary latches 70a through 70e, 71, 72a through 72n, 73, 74, 75a, 75b, 76a, 76b and all the secondary latches 92a through 92n, 93, 94, 95a, 95b, 96a and 96b thereby forcing the outputs low. This signal from source 37 (/RST) also resets the error bus registers and error lines from the error logic circuit 100.

[0057] Coupled to the above described register of FIG. 4A is the unique error correction code circuit arrangement of FIG. 4B.

[0058] In FIG. 4B, module location identification is provided to error logic circuit 100 which is more fully described in conjunction with FIG. 6 below. This module location identification is provided to error logic circuit 100 through receivers 79a, 79b, and 79c whose inputs are coupled to DIMM address input range sources (SA0, SA1, SA2) 78a, 78b and 78c and whose outputs are coupled to an error logic circuit 100. The signals from sources (SA0, SA1, SA2) 78a, 78b and 78c define the DIMM address which is then reported on the error bus when requested by the system. This error logic circuit 100 is controlled by a signal from the NAND gate 175 when either of the DRAM chip select signal sources (/CS0) 33a and (/CS1) 33b are active. The error logic circuit 100 further has a reset signal source 180 coupled thereto.

[0059] Also included in the error correction code circuit of FIG. 4B is a SEC/DED ECC circuit 90 which is more fully described in conjunction with FIG. 5 below. Coupled to this

SEC/DED ECC circuit are the outputs of primary latches 70a through 70e, 71 and 72a through 72n. This SEC/DED ECC circuit 90 provides three outputs 109, 110, and 111 to the error logic circuit 100. These outputs are: a correctable error (CE) line 109, an uncorrectable error (UE) line 110 and a parity error bit line 111 fed to the error logic circuit 100 which provides outputs regarding correctable and uncorrectable errors on output lines 120 and 121. When either error line (CE) 109 or uncorrectable error line (UE) 110 is low this indicates that an error was identified as being associated with the address and/or command inputs (either correctable or uncorrectable). The error lines 120, 121 will be active, i.e., low, for two clock cycles simultaneous with the re-driven address/command data when operating in ECC mode or delayed by two clock cycles when operating in parity mode. The logic error circuit 100 also provides an Error Bus (Inter Integrated Circuit or IIC) 122 for external collection of error information such as error type, DIMM address, error count and status of the 28 input and internally generated syndrome bits at the time of the first fail. The information remains latched until a reset command is written to bus 122 or /RST input 37 is switched low. The selected IIC protocol allows unique byte addressing of the ten registers, consistent with the present industry standard protocol for serial program decode electronic erasable programmable read only memory (SPD EPROM) and is well known to the art.

[0060] This SEC/DED ECC circuit 90 also has data bit outputs coupled through secondary latches 92a through 92n to a first input of all the output or secondary multiplexers 102a through 102n. The output of register latches 72a through 72n labeled BYPASS are directly connected to the second input of the output or secondary multiplexers 102a through 102n thereby allowing the SEC/DED ECC circuit 90 to be bypassed depending on the ECC mode input 123.

[0061] The output of the primary or register latches 73, 74, 75a, 75b, 76a and 76b are all coupled to a first input of secondary or output latches 93, 94, 95a, 95b, 96a and 96b and through these secondary latches 93, 94, 95a, 95b, 96a and 96b to a first input of output or secondary multiplexers 103, 104, 105a, 105b, 106a and 106b. The outputs of primary latches 73, 74, 75a, 75b, 76a and 76b are connected directly to a second input of output or secondary multiplexers 103, 104, 105a, 105b, 106a and 106b thereby allowing secondary latches 93, 94, 95a, 95b, 96a and 96b to be bypassed based on the /Delay CKE input 124 and /ECC mode input 123.

[0062] A control circuit comprised of a differential register 130 that has a first input coupled to a CK signal input 131, a second input coupled to a /CK signal input 132 and its output coupled to a second input all the primary latches 70a through 70e, 71, 72a through 72n, 73, 74, 75a, 75b, 76a and 76b and to the second input of all the output or secondary latches 92a through 92n, 93, 94, 95a, 95b, 96a and 96b and to the error logic circuit 100 via line 88. The /ECC mode signal source 135 is coupled to a selection third input of secondary multiplexers 102a through 102n, 103 and 104 and to the error logic circuit 100. The output or secondary multiplexers 105a, 105b, 106a and 106b have their selection inputs coupled to a source 124 of /Delay, CKE_ODT signals.

[0063] The ECC code selected for this module is a single error correction/double error detection (SEC/DED) code and is shown in the H-Matrix depicted in FIG. 6. The use of this SEC/DED code ensures that all single errors associated with the address and command bits are detected and corrected

and that all double bit errors are detected. It should be noted that interconnect failures almost exclusively begin as single point fails, with other failures possibly occurring over time dependent or independent of the root cause of the initial fail.

[0064] In summary, the present invention describes a unique DIMM having an enhanced 4 rank-enabled 28 bit 1:2 register with added error correction code logic (ECC) incorporated therein for correcting single bit errors while permitting continuous memory operation independent of the existence of these errors. A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.

[0065] The above described 28 bit 1:2 register of the present invention provides key operational features, which differ from existing register designs intended for memory module applications and includes: 4 rank operability; disabling of un-needed internal circuitry when the module is not selected; error detection and correction on key inputs; programmable delay for un-gated inputs; parity mode; reset circuitry; error reporting and identification and reporting of the DIMM address.

[0066] CS gating of key inputs, e.g., /CS0, /CS1, /CS2 and /CS3, is provided as a means of reducing device power for the internal latches which will only be updated and related internal circuitry utilized when one, two, three or all of the chip select CS inputs are active low (and chip select gate enable tied high) at the rising edge of the system clock. The twenty-two chip select-gated signals associated with this function include addresses continuously re-driven at the rising edge of every clock depending on the state of chip select. However, the chip select gating function can be disabled by tying the chip select gate enable input low thereby enabling all internal latches to be updated on every rising edge of clock.

[0067] In exemplary embodiments, the 4 rank circuitry in the enhanced 4-rank enabled ECC/parity buffer chip 21 is designed such that the enhanced 4-rank buffer device/chip 21 can be utilized as a direct replacement for earlier 2-rank enabled buffers, on one and two rank DIMMs, with no changes to the wiring of the assembly originally designed to use the earlier device. The inputs to differential receivers 43b and 44b are designed to float to a high level when not connected to an input source, the register pins assigned to inputs /CS2 33c and /CS3 33d were previously assigned to redundant VDD pins, and novel wiring on the 4 rank memory module depicted in FIGS. 3A-3D permit two of these buffers to be used on the 4-rank memory modules as shown in subsequent figures.

[0068] Programmable delay for un-gated inputs (/Delay CKE-ODT) associated with CKE and ODT (DRAM signals), the inputs will be latched and re-driven on each rising edge of the clock signal (CLK.) independent of the state of the chip select (CS) signals. However, since some controllers may be designed with limited flexibility regarding latency for these signals vs. chip select (CS), address (Addr), row address strobe (RAS), column address strobe (CAS) and write enable (WE), a delay block can be selected to re-align the timing relationships which are offset by 1 clock when the error correction code circuitry (ECC) is enabled.

[0069] ECC Mode (/ECC Mode low): For all inputs gated by CS, on-chip SEC/DED ECC logic is enabled and the signal received on CHK0/Parity in is received as check bit 0 when /ECC Mode input is low. This ECC logic will

operate across 28 inputs (22 'CS-gated inputs and the 6 check bits) and will correct all single bit errors and detect all double bit errors present on the twenty-two chip select gated data inputs. If a correctable error is detected, /Error (CE) will be driven low for two clocks and errors will be counted and latched in the error bus registers for the 28 inputs if this is the first error since a reset is issued. Any double bit error will also be detected (as well as many other errors that are not correctable), and will be reported on the /Error (UE) error line (driven low for two clocks) and in the error bus registers if this error is the first since a Reset is issued. Although /CS0, /CS1, /CS2 and /CS3 are not included in the ECC logic, the propagation delay of the CS output signals will track the signals included in the ECC logic (1 additional clock of latency).

[0070] In addition to the above ECC mode, the same twenty two chip select gated data signals can be operated in 'parity mode (/ECC Mode high), whereby the signal received on CHK0/Parity in line is received as parity to the register one clock pulse later than the chip select gated data inputs. The received parity bit is then compared to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. The twenty two chip select gated data signals will be latched and re-driven on the first clock pulse and any error will be reported two clock pulses later via the Uncorrectable Error (UE) line (driven low for two clock pulses) and in the Error Bus Registers. No correction of errors will be completed in this mode. The convention of parity, in this application, is odd parity (odd numbers of 1s across data and parity inputs equals valid parity).

[0071] The /RST signal input is used to clear all internal latches (including the error registers), and all outputs will be driven low quickly except the error lines which will be driven high.

[0072] Error reporting circuitry is included to permit external monitoring of DIMM operation. Two open-drain outputs are available to permit multiple modules to share a common signal line for reporting an error that occurred during a valid command (/CS=low) cycle (consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic, /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of /Error (UE) is different in parity mode vs. ECC mode.

[0073] In addition, an error bus (enabling access to 10 registers that can be read and reset via an IIC bus) is available to permit the device to be interrogated for additional error information, such as the error type (correctable, uncorrectable or parity error), error count and the memory card location (via the SA0-2 address pins which are conventionally wired only to the separate serial program decode (SPD) electronic erasable programmable read only memory (EE PROM). Other information is also available for diagnostics such as the signals received by the register (address/command, control signals, check bits, parity bit) when a chip select (CS) is active low and the associated syndrome bits so that they can be decoded to determine which of the 28 input signals (22 'CS-gated plus 6 check bits) or internal ECC logic failed, as well as an indication of the buffer type (1 to 2 rank enabled buffer or 1 to 4 rank enabled buffer), the

buffer die revision, an indication of the buffer vendor, the maximum buffer speed, the driver strength and whether ECC has been bypassed by the application or not. These registers will contain information about the first fail, and the error counter will continue to increment until it is reset or reaches the full count (64K). All registers can be reset by writing the reset error bus command on the IIC bus, or via the /RST pin.

[0074] In addition to the use of the ECC structure defined above (included in both the memory interface chip and the register on the DIMM), redundant contacts are included on the module pinout to effectively eliminate other possible SPOF (single-point-of-failure) contributors in the interconnect system. Contacts that cannot be protected by the ECC structure described above, for various reasons, include the following: voltage reference (Vref), Clocks, Chip Selects (CS), CKEs, ODTs, VSS /VDD contacts or pins, Error lines, data input on the IIC bus (SDA), data clock on the IIC bus (SCL) and related signals. In the present invention each of these contacts is provided with a first contact on a first side of the DIMM and a redundant contact directly opposite the first contact and/or offset by no more than two pins from the first contact on the opposite side of the DIMM. For example if the voltage reference source 28 is applied via contact or pin 1 on the front side of the DIMM it is also applied via contact or pin 139 on the back side of the DIMM with contact 1 being direct opposite contact 139. Similarly the SDA signal is applied via contact or pin 135 on the front side of the DIMM and also via the contact or pin 273 on the back side of the DIMM and the /CS3 signal is applied via contact or pin 89 on the front side of the DIMM and also via contact or pin 225 on the back side of the DIMM. A full description of the contact or pin assignment matrix for the present invention is shown in FIGS. 7A, 7B and 7C. The specific contact placement is selected to maximize fault tolerance. By providing such opposite redundant contacts, problems caused, for example, by a slight bowing of the DIMM will cause low contact pressure on a contact on one side of DIMM but high pressure on the opposing contact. In such cases good signal flow will always be assured when such redundant and opposing contacts, as discussed above, are used. These opposing and redundant contacts will also facilitate board wiring by minimizing wiring congestion for this solution also permits in-line wiring. The following chart is a listing of the DIMM locations of a few of these contacts.

Signal	Contact or PIN#	Side of DIMM	Nominal Distance from Key	Direction from Key
CS0	86	FRONT	11.495 mm	RIGHT
CS0	224	BACK	11.495 mm	LEFT
CS1	91	FRONT	16.495 mm	RIGHT
CS1	229	BACK	16.495 mm	LEFT
CKE0	65	FRONT	13.505 mm	LEFT
CKE0	203	BACK	13.505 mm	RIGHT
CKE1	62	FRONT	16.505 mm	LEFT
CKE1	200	BACK	16.505 mm	RIGHT
RAS	222	BACK	9.495 mm	LEFT
CAS	87	FRONT	12.495 mm	RIGHT
WE	84	FRONT	9.495 mm	RIGHT
CK0	77	FRONT	2.495 mm	RIGHT
CK0	215	BACK	2.495 mm	LEFT
CK0B	78	FRONT	3.495 mm	RIGHT
CK0B	216	BACK	3.495 mm	LEFT

[0075] The ECC function adds a single clock pulse delay (at planned operating frequencies) to the DIMM register performance, which may be of concern to some performance-optimized applications. As such, two additional modes are included on the module that permit the system user to tradeoff performance and reliability. In Parity Mode, the memory interface chip or controller would generate a single parity bit in conjunction with providing the full address and command field to the module. The module would re-drive the address and command bits, to the DRAMs, in the next cycle—rather than adding the additional cycle required in ECC mode. Any error on the address and command bus would be reported to the system at a later time, and the potential for recovery from the fail would be small hence this option is undesirable for many applications. The last mode would be to simply operate the memory in a mode with no parity bits and no ECC bits, with neither the added delay due to ECC nor any means to detect a fault on the address/command bus as per the prior art convention now used for these modules.

[0076] FIG. 5 is a block diagram of the SEC/DED ECC circuit of FIG. 4B. The twenty-two data inputs 32a through 32n via the twenty two latches 72a through 72n and lines 82a through 82n are fed both to a check bit generator circuit 230 and a first input of a parity generator/checker circuit 231. The parity generator/checker circuit 231 further has a second input coupled to the parity in signal source 31 via primary latch 71 and output line 81 and depending on the state of the parity input signal on input 31 sends a parity error signal (PERR) on output line 111 to the error logic circuit 100.

[0077] Meanwhile the check bit generator circuit 230 is transferring the twenty two inputted data signals to a first input of a syndrome bit generator 232 whose second input is coupled to the check bit inputs 30a through 30e through the lines 80a through 80e coming from the primary latches 70a through 70e.

[0078] The Syndrome bit generator 232 then transfers the twenty two data signals to a first input of a syndrome bit decoder and the six check bits to the error generator 235 which determines if there are either correctable or uncorrectable errors in the received data and provides the appropriate correctable error or uncorrectable error signal to the error logic circuit 100 via either line 109 or 110. The syndrome bit decoder now decodes the twenty-two data bits and transfers them to the data correction circuit 234. In the correction circuit the syndrome bits are selectively Xored with the data inputs consistent with the H-matrix, shown in FIG. 6, with any single bit errors in the data field inverted to correct the error.

[0079] The Error Logic block 100 consists of 3 major elements (not shown) which are an error counter, a status register block that contains a plurality of status registers, and an IIC logic block all of which are interconnected through common logic circuits. All of these blocks as well as the interconnecting logic circuits are common and readily available circuits known to those skilled in the art.

[0080] More specifically, the error counter is a 16-bit counter that increments as it receives errors inputs (CE, UE or Parity) from the SEC/DED ECC 90. This error counter continues to count errors (until it reaches its full count) even while the status registers are being read out on the IIC bus.

[0081] The status register block includes, in the present case, ten eight bit register sets (0-9) which contain infor-

mation on the data input (DO-21) signals, the check bit signals (CO-5 and Parity In) signals received from the memory controller 19, as well as signals from the memory module 20 (FCC/Parity Mode, SA0-2), the error count, and the syndrome bits (S0-5) which are calculated by the SEC/DED ECC 90. In addition, the ten eight bit registers include

All registers can be reset by writing the Reset Error Bus command on the IIC bus.

[0085] The Byte 0: Status Register is the general status bit register that can be read to determine the type of error, the mode and the address of the DIMM (same as the DIMM SPD address).

Byte 0: Status Register							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Extended Status Register (If 1, see Byte 9)	DIMM Address SA2	DIMM Address SA1	DIMM Address SA0	Mode 1=ECC 0=Pty	Parity Error 1=PERR	ECC error 1=UE	ECCerror 1=CE

an indication of the buffer type (1 to 2 rank enabled buffer or 1 to 4 rank enabled buffer), the buffer die revision, an indication of the buffer vendor, the maximum buffer speed, the driver strength and whether ECC has been bypassed by the application or not.

[0082] The IIC Logic block includes the necessary logic to support the "IIC Bus Specifications Version 2.1 January 2000 Standard". In this case the register is an IIC slave where the register is addressed by the DIMM address input range sources (SA0, SA1, SA2) 78a, 78b and 78c and responds to several IIC bus commands—reset, read from the ten (10) Status Registers and the test mode.

[0083] The miscellaneous logic circuits interconnecting the above described error counter, status register block and IIC logic block include logic circuits designed to reset the error counters and the ten (10) status registers from either the external reset signal (/RST) source 37 or an internal power-on reset, to load the contents of the ten status registers and logic (including a set of shadow registers) that the IIC logic will send out onto the IIC bus when a IIC bus read occurs, along with some control logic to drive the correctable error (CE) and uncorrectable error (UE) lines out if such an error occurs.

[0084] The error bus that provides access to the ten (10) internal status registers (that can be read and reset via an IIC bus) permits the device to be interrogated for additional error information, such as the error type (correctable, uncorrectable or parity error), error count and the memory card location (via the SA0-2 address pins, also shared by the separate SPD EPROM). Other information is also available for diagnostics such as the signals received by the register (address/command, control signals, check bits, parity bit) associated with a CS is active low and the syndrome bits so that they can be decoded to determine, in the case of a failure, which of the 28 input signals (22 'CS-gated plus 6 check bits) failed. The ten eight bit registers further include an indication of the buffer type (1 to 2 rank enabled buffer or 1 to 4 rank enabled buffer), the buffer die revision, an indication of the buffer vendor, the maximum buffer speed, the driver strength and whether ECC has been bypassed by the application or not. These registers will contain information about the first fail, and the error counter will continue to increment until it is reset or reaches the full count (64K).

[0086] Bytes 1 and 2: Error Counter. The 16 bit error counter will count up to 64K errors (FFFF hex) based on any error (CE, UE or Parity Error). Byte 1 is the LSB and byte 2 is the MSB of the error counter. Once the 16-bit counter has counted up to all ones, it will stay all 1s until the error bus is reset. The error counter register will not increment during a IIC read operation but will continue to count errors if they occur.

Byte 1 (LSB)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E7	E6	E5	E4	E3	E2	E1	E0
Byte 2 (MSB)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
E15	E14	E13	E12	E11	E10	E9	E8

[0087] Bytes 3-7 show the polarity of all 28 signals of the addresses and commands plus the check bits and parity bit that were received at the time of the first fail.

Byte 3: Data Register A (DO-7)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D7	D6	D5	D4	D3	D2	D1	D0
Byte 4: Data Register B (D8-15)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D15	D14	D13	D12	D11	D10	D9	D8
Byte 5: Data Register C (D16-21, CS0-1)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
CS1	CS0	D21	D20	D19	D18	D17	D16
Byte 6: Data Register D (CKE0-1, ODT0-1, CS2-3)							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	RFU	CS3	CS2	ODT1	ODT0	CKE1	CKE0
0	0	0	0				
Byte 7: Check Bit (CO-5) and Parity Register							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	RFU	Check	Check	Check	Check	Check	Check
0	0	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0/Pty In

[0088] Byte 8: Syndrome Register. Byte 8 shows the syndrome bits associated with the first error. These can be

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decoded to determine which of the 22 'CS-gated signals or 6 Check Bits caused the fail. Bytes 3-7 show the polarity of all input signals at the time of the fail. FIG. 8 shows the timing diagram used with the present invention.

Byte 8: Syndrome Bit (0-5) Register							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	RFU	Syndrome	Syndrome	Syndrome	Syndrome	Syndrome	Syndrome
0	0	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0

[0089] Byte 9 provides operational information such as bit 7, which indicates whether ECC checking is active and bit 6, which indicates the drive strength setting for the drivers, at the time the register contents are interrogated. In addition byte 9 provides useful information regarding the buffer device such as bit 5 (the maximum clock speed that the buffer is intended to operate at), the supplier (the exemplary embodiment allows two suppliers to be uniquely identified via a pre-defined bit assignment), although the use of bit 4 or an additional byte (i.e. byte 10) would permit the unique identification of 4 or more suppliers), and the supplier's die revision (the exemplary embodiment permits unique identification of up to 8 die revisions). Through the use of the contents of byte 9, further information can be obtained regarding the buffer settings at the time of failure, after power-up or at any other time during operation. In addition, systems using the enhanced 4-rank buffer device will be able to electronically detect the supplier code, die revision and speed sort of the buffer devices in the system, without the need to physically inspect the devices, by interrogating the installed memory subsystems containing the subject buffer devices.

This offers a significant advantage should it be necessary to identify installed buffers if issues arise regarding the viability of the devices in stalled in a system in regard to manufacturing, reliability or related concerns subsequent to the assembly of the memory subsystems.

Byte 9: Extended Status Register Description Bit (0-6) Register							
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ECC	DS	Speed	RFU	Supplier	Die	Die	Die
Bypass	1=Lo Drv	1=800		1=Supplier	Rev	Rev	Rev
1=Yes	0=Hi Drv	0=667		A			
0=No				0=Supplier B			

[0090] All the information necessary for one skilled in the art to design this error logic block 100 is included in the H-Matrix shown in FIG. 6 where D0 through D21 refer to the data bits, C0 through C5 refer to the check bits and S0 through S5 refer to the syndrome bits.

[0091] FIG. 9 depicts a variety of configurations that may be implemented using the enhanced 4-rank enabled buffer chip 21 described herein. As shown in FIG. 9, the buffer chip 21 may be utilized on existing memory modules that support one or two ranks of memory devices, thereby eliminating the need to upgrade to new memory modules to utilize the enhanced 4-rank enabled buffer chip 21. In addition, FIG. 9 depicts two of the enhanced 4-rank enabled buffer chips 21

being utilized on a high density 4 rank memory module to access the 4 ranks of memory devices.

[0092] A one buffer chip configuration 902 is depicted in FIG. 9 as an interconnect drawing showing the interconnec-

tions between the enhanced 4-rank enabled buffer chip 21 and the EPROM 302 (shown as VPD (Vital Product Data) but could also be used to contain SPD, or Serial Presence Detect information) on an exemplary memory module having 9 eight bit wide or 18 four or eight bit wide memory devices and a single 4-rank enabled buffer chip 21. As shown in configuration 902, outputs from the buffer chip 21 include an indication of whether the error is a correctable error (CE) or an uncorrectable error (UE) as well as the corrected (if error is correctable) command and address information, which connect to memory devices 22. The internal status registers (bytes 0 through 9) of the buffer chip 21 can be accessed via an IIC bus by operating the SCL and SDA pins that connect to the buffer (2, 140 and 2, 141 respectively) consistent with the IIC Bus Specification. At the SA0-2 input pins a memory card location is specified. The IIC data clock (SCL) and IIC data input (SDA) query the status registers on the buffer chip 21. As depicted in configuration 902, the CS2 and CS3 inputs are disconnected and thus, the enhanced 4-rank enabled buffer chip 21 can operate on a standard, prior art, one or two rank memory module without requiring a system upgrade.

[0093] A two buffer chip configuration 904 is depicted in FIG. 9 as an interconnect drawing showing the interconnections between the enhanced 4-rank enabled buffer chips 21 and the EPROM 302 on an exemplary memory module having 36 four bit wide memory devices and two 4-rank enabled buffer chips 21. The CS2 and CS3 inputs are disconnected, and thus, the enhanced 4-rank enabled buffer chip 21 can operate on a standard, prior art, one or two rank memory module without requiring a system upgrade. The status registers in buffer 1 can be separately accessed from the status registers in buffer 2 due to the fact that the SA2 pin on buffer 1 is tied to ground, whereas the SA2 pin on buffer 2 is tied to Vdd. The SA0 and SA1 inputs for both buffers are connected to the SA0 and SA1 pins on the module, resulting in the two buffers having unique addresses. Using this method, up to 4 modules, each with 2 buffers, can be installed in a system that permits independent addressing of the status registers in the 8 total buffer devices (using a unique SA0 and SA1 input combination for each of the four module positions in conjunction with the SA2 wiring shown).

[0094] A two buffer chip configuration 906 is depicted in FIG. 9 as an interconnect drawing showing the interconnections between the enhanced 4-rank enabled buffer chips 21 and the EPROM 302 on an exemplary memory module having 72 four bit wide memory devices and two 4-rank enabled buffer chips 21. As depicted in configuration 906, the buffer one has a CS0 signal connected to the CS0 pin and

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a CS1 signal connected to the CS1 pin, and register two has a CS2 signal connected to the CS0 pin and a CS3 signal connected to the CS1 pin.

[0095] As depicted in FIG. 9, the enhanced buffer chips 21 described herein may be utilized in a first mode with existing memory modules that support one or two ranks of memory devices and in a second mode with high density memory modules that support four ranks of memory devices with up to 72 memory devices. The second mode is executed when two buffer chips 21 are coupled together on a memory module with all four of the chip selects (CS0, CS1, CS2 and CS3) being utilized to access different ranks of memory devices. The enhanced buffer chips 21 include 2 additional chip select input lines, but continue to perform the same functions, have the same pin counts, and have the same outputs as prior art buffer devices, therefore, the enhanced buffer chips 21 can be interchanged with prior art buffer devices by disconnecting the 2 additional chip select input lines.

[0096] FIG. 10 is an interconnect drawing showing an exemplary embodiment of the chip select wiring at the inputs and outputs of the enhanced 4-rank buffer chip 21 when used on a memory module that supports up to four ranks of memory devices. Two buffer chips 21 are required in this exemplary embodiment to drive all of the DRAM devices at the intended operating frequencies. As depicted in FIG. 10, buffer chip 21a accesses the first and second rank (CS0 and CS1) of memory devices located on the left and right sides of the memory module and buffer chip 21b accesses the third and fourth rank (CS2 and CS3) of memory devices located on the left and right sides of the memory module. Although not shown in this figure, the exemplary buffer includes two copies of each chip select output, with one copy (e.g., CS0A) wiring to the first rank of DRAMs 1002 on the right side of the DIMM and the second copy (e.g., CS0B) wiring to the first rank of DRAMs 1002 on the left side of the DIMM. In the exemplary embodiment for the module shown in FIGS. 3A and 3B, the DRAMs 1002 are wired such that each of the two buffers drive one copy of each chip select (e.g., "/CSx") output to 10 DRAMs located to one side of the buffer and 8 DRAMs located to the other side of the buffer and on the same side of the buffer as the first DRAMs (18 DRAMs in total). In the exemplary embodiment for the module of FIGS. 3A and 3B, the buffer driving /CS2 and /CS3 is located on the front of the DIMM, and the buffer driving /CS0 and /CS1 is located on the back of the DIMM. Alternate exemplary embodiments may swap the location of the buffers, or may re-drive /CS0 and /CS2 in one buffer device and /CS1 and CS3 in a second buffer device, while not straying from the teachings described herein. Address and command wiring is fully described in the text associated with FIGS. 3A-3D. Note that in this exemplary embodiment, the wiring to the chip select inputs of buffer chip 21b is swapped between CS0/1 and CS2/3. As depicted in FIG. 10, the buffer chip 21 is operable with as few as one rank of memory devices (e.g., with only one chip select input line being selectable) and as many as four ranks of memory devices (e.g., with all four chip select input lines being selectable).

[0097] FIG. 11 is a table describing the IIC addressing associated with the one or more buffer chips 21 utilized in memory modules implementing exemplary embodiments, when either one or two registers, or buffer chips 21, are installed on a given memory module. In exemplary embodi-

ments, the SA2 is hard-wired on two and four rank memory modules so that the internal status registers can be read from each buffer chip 21, as previously described. Referring to FIG. 11, column 1102 is the slot in the memory system being occupied by the memory module and column 1104 is the binary IIC address associated with the memory module slot in column 1102. For memory modules having one buffer chip 21, the IIC address correlates to the slot being occupied by the memory module as shown in column 1106. For memory modules having two buffer chips and up to four ranks of memory devices, the IIC address is doubled up as shown in column 1108. The table in FIG. 11 shows the IIC addresses for four rank memory modules with two buffer chips 21. For a four rank memory module located in slot 1 of the memory system, IIC addresses 0 and 4 are utilized to uniquely access the two buffer chips 21, whereas IIC addresses 1 and 5 are utilized to uniquely access the two buffer chips 21 located on a memory module in slot 2 of the memory system, and so on. Therefore, only four DIMM slots can be utilized with 4 rank memory modules containing 2 buffer devices. However, twice the memory density (up to 72 memory devices per memory module) is being supported in the same four slots (before limit was up to 36 memory devices on each memory module). FIG. 11 shows that in exemplary embodiments, memory modules having one or two ranks of memory and a single buffer chip 21 can be installed in up to eight system module slots, whereas memory modules having up to four ranks of memory devices are limited to up to four memory system module slots, due to such factors as the bus loading on the data bus, overall system power, unique addressability of the internal registers of the buffer devices, etc. This limitation may not hold true in all applications, but is applicable in the exemplary embodiment described herein.

[0098] In order to detect if the module(s) installed in the server can properly function in the intended application, monitor the address and control bus integrity, correct errors on the address and control bus, report errors and log and counts errors it is necessary that the DIMM error bus be functional and correctly accessed using the industry IIC protocol and the SA 0-2 bits such that the DIMM can provide a byte of data which includes Byte 0 discussed above. This is achieved by reading the SA 0-2 bits on bits 4, 5, and 6 of the Byte 0 to verify that they match the address of the memory module being interrogated, verifying that bit 3 (the ECC flag bit) is a "1" or high level and verifying that bit 7 of Byte 9 is set to a "1" or high level while the module is programmed to operate with ECC enabled. This proves a unique signature that indicates that the buffer/module combination is intended for use with error checking and correction on the address and control bus. If the correct register values are not obtained, the module is incapable one or more of monitoring the address and control bus integrity, correcting errors on the address and control bus, reporting errors or logging and counting detected errors.

[0099] Parity error reporting in the present invention is realized by delivering the parity signal one cycle after the address and command to which it applies, and driving the error line low, i.e., "0" two clock cycles after the address and command bits are driven to the DRAMs from the memory interface chip if an error is detected. After holding the error line low for only 2 clock cycles, the driver will be disabled

and the output permitted to return to an un-driven state (high impedance) allowing this line to be shared by multiple modules.

[0100] The invention also provides a means for and a method for adjusting the propagation delay for signals on the memory module that are not included in the ECC circuitry such that the signals can be selectively re-driven within one or two clock cycles. This results in a significant increase in module operating speed.

[0101] Moreover by operating the memory module in parity mode, unused ECC check bit inputs can be held at a low level, i.e., "0" thus ensuring that these inputs are at a known and quiescent state.

[0102] Finally the module of the invention may be operated as if it were a conventional non-ECC protected module, by effectively removing the secondary registers (post-ECC) from the delay path by setting the /ECC Mode control pin to a high level, i.e. "1".

[0103] In summary, the present invention is an enhanced function 4 rank-enabled 28 bit 1:2 buffer/register, intended for use on main memory modules having one to four ranks of memory devices. The buffer, of the present invention, includes addressability for up to 4 ranks of memory devices and includes ECC logic to correct single bit errors and permit continuous memory operation independent of the existence of these errors. A parity operating mode is also provided, in conjunction with error reporting circuitry to permit the system to interrogate the device to determine the error condition.

[0104] The present invention also provides CS gating of key inputs through the use of CS0, CS1, CS2, CS3 and CS Gate Enable. As a means to reduce device power, the buffer's internal latches will only be updated when one or more of the CS inputs are active low (and CS Gate Enable at a high level) at the rising edge of clock. The 22 'CS-gated signals associated with this function include addresses (addr 0:15, BA 0:2), RAS, CAS, WE—with the remaining signals (CS, CKE, ODT) continuously re-driven at the rising edge of every clock as the re-drive of these inputs by the buffer does not require that one or more of the CS inputs to be at a low level. The CS gating function can be disabled by tying CS Gate Enable low enabling all internal latches to be updated on every rising edge of clock. This novel use of CS gating reduces the power dissipation of the buffer device and attached memory devices when any of the gated inputs (addr 0:15, BA 0:2) transition, as the transitions will not propagate through the buffer(s) to the memory device(s), thereby causing circuitry within the buffer and memory devices to switch, unless one or more of the CS inputs to the buffer(s) are at a low level (selecting the buffer and associated memory device(s)). As is well known in the art, overall power dissipation can be minimized by eliminating unnecessary transitions of circuitry that is not associated with an intended operation.

[0105] Programmable delay for un-gated inputs (/Delay CKE-ODT) is also provided. For the pins associated with CKE and ODT (DRAM signals), the inputs will be latched and re-driven on each rising edge of CLK, independent of the state of the chip select (CS). However, since some controllers may be designed with limited flexibility regarding latency for these signals vs CS, Addr, RAS, CAS and WE, a delay block can be selected to re-align the timing relationships which are offset by one clock cycle when the error correction code is enabled.

[0106] Also for all inputs gated by CS, the on-chip SEC/DED ECC logic is enabled and the signal received on CHK0/Parity In is received as check bit 0 via a programming pin (/ECC Mode low). This ECC logic will operate across 28 inputs (22 CS-gated inputs and the 6 check bits), and will correct all single bit errors present on the 22 CS-gated inputs. /Error (CE) will be driven low for two clocks and errors will be counted and latched in the Error Bus Registers for the 28 inputs. Any double bit error will also be detected (as well as any error that is not correctable), and will be reported on the /Error (UE) error line (driven low for two clocks) and in the Error Bus Registers. Although CS0-3 are not included in the ECC logic, the propagation delay of the CS output signals will track the signals included in the ECC logic (1 additional clock of latency).

[0107] In addition to the above ECC mode, the same 22 CS-gated signals can be operated in 'parity mode (/ECC Mode high), whereby the signal received on CHK0/Parity In is received as parity to the register 1 clock later than the 'CS-gated inputs. The received parity bit is then compared to the parity calculated across these same inputs by the register parity logic to verify that the information has not been corrupted. The 22 'CS-gated signals will be latched and re-driven on the first clock and any error will be reported two clocks later via the /Error (UE) line (driven low for two clocks) and in the Error Bus Registers. No correction of errors will be completed in this mode. The convention of parity is odd parity (odd numbers of 1's across data and parity inputs equals valid parity).

[0108] The /RST pin is used to clear all internal latches (including the error registers), and all outputs will be driven low quickly except the error lines which will be driven high.

[0109] The error reporting circuitry, of the present invention is included to permit external monitoring of device operation. Two open-drain outputs are available to permit multiple modules to share a common signal pin for reporting an error that occurred during a valid command (any /CS=low) cycle (consistent with the re-driven signals). These two outputs are driven low for two clocks to allow the memory controller time to sense the error. /Error (CE) indicates that a correctable error occurred and was corrected by the ECC logic. /Error (UE) indicates that an uncorrectable error occurred and depending on the mode selected is an uncorrectable ECC error or a parity error. Note that the timing of UE is different in parity mode vs ECC mode.

[0110] In addition, the error bus, (the ten registers discussed above that can be read and reset via an IIC bus) is available to permit the device to be interrogated for additional error information, such as the error type (correctable, uncorrectable or parity error), error count and the memory card location (via the SA0-2 address pins, also shared by the separate SPD EPROM). Other information is also available for diagnostics such as the signals received by the register (address/command, control signals, check bits, parity bit) when a CS is active low and the syndrome bits so that they can be decoded to determine which of the 28 input signals (22 CS-gated plus 6 check bits) failed. These registers will contain information about the first fail, and the error counter will continue to increment until it is reset or reaches the full count (64K). All registers can be reset by writing the Reset Error Bus command on the IIC bus.

[0111] In alternate exemplary embodiments, the memory controller(s) may be integrated together with one or more processor chips and supporting logic, packaged in a discrete

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chip (commonly called a “northbridge” chip), included in a multi-chip carrier with the one or more processors and/or supporting logic, or packaged in various alternative forms that best match the application/environment. Any of these solutions may or may not employ one or more narrow/high speed links to connect to one or more hub chips and/or memory devices.

[0112] The memory modules may be implemented by a variety of technology including a DIMM, a single in-line memory module (SIMM) and/or other memory module or card structures. In general, a DIMM refers to a small circuit board which is comprised primarily of random access memory (RAM) integrated circuits or die on one or both sides with signal and/or power pins on both sides of the board. This can be contrasted to a SIMM, which is a small circuit board or substrate composed primarily of RAM integrated circuits or die on one or both sides and single row of pins along one long edge. The DIMM depicted in FIG. 1 includes 276 pins in the exemplary embodiment, whereas DIMMs can be constructed with other pincounts while still retaining the same functionality as that described herein.

[0113] Memory devices are generally defined as integrated circuits that are composed primarily of memory (storage) cells, such as DRAMs (Dynamic Random Access Memories), SRAMs (Static Random Access Memories), FeRAMs (Ferro-Electric RAMs), MRAMs (Magnetic Random Access Memories), Flash Memory and other forms of random access and related memories that store information in the form of electrical, optical, magnetic, biological or other means. Dynamic memory device types may include asynchronous memory devices such as FPM DRAMs (Fast Page Mode Dynamic Random Access Memories), EDO (Extended Data Out) DRAMs, BEDO (Burst EDO) DRAMs, SDR (Single Data Rate) Synchronous DRAMs, DDR (Double Data Rate) Synchronous DRAMs or any of the expected follow-on devices such as DDR2, DDR3, DDR4 and related technologies such as Graphics RAMs, Video RAMs, LP RAM (Low Power DRAMs) which are often based on the fundamental functions, features and/or interfaces found on related DRAMs.

[0114] Memory devices may be utilized in the form of chips (die) and/or single or multi-chip packages of various types and configurations. In multi-chip packages, the memory devices may be packaged with other device types such as other memory devices, logic chips, analog devices and programmable devices, and may also include passive devices such as resistors, capacitors and inductors. These packages may include an integrated heat sink or other cooling enhancements, which may be further attached to the immediate carrier or another nearby carrier or heat removal system.

[0115] Module support devices (such as buffers, registers, PLL's, DLL's, non-volatile memory, etc) may be comprised of multiple separate chips and/or components, may be combined as multiple separate chips onto one or more substrates, may be combined onto a single package or even integrated onto a single device—based on technology, power, space, cost and other tradeoffs. In addition, one or more of the various passive devices such as resistors, capacitors may be integrated into the support chip packages, or into the substrate, board or raw card itself, based on technology, power, space, cost and other tradeoffs. These packages may include an integrated heat sink or other

cooling enhancements, which may be further attached to the immediate carrier or another nearby carrier or heat removal system.

[0116] Memory devices, buffers, registers, clock devices, passives and other memory support devices and/or components may be attached to the memory subsystem via various methods including solder interconnects, conductive adhesives, socket structures, pressure contacts and other methods which enable communication between the two or more devices via electrical, optical or alternate means.

[0117] The one or more memory modules (or memory subsystems) may be connected to the memory system, processor complex, computer system or other system environment via one or more methods such as soldered interconnects, connectors, pressure contacts, conductive adhesives, optical interconnects and other communication and power delivery methods. Connector systems may include mating connectors (male/female), conductive contacts and/or pins on one carrier mating with a male or female connector, optical connections, pressure contacts (often in conjunction with a retaining mechanism) and/or one or more of various other communication and power delivery methods. The interconnection(s) may be disposed along one or more edges of the memory assembly and/or placed a distance from an edge of the memory subsystem depending on such application requirements as ease-of-upgrade/repair, available space/volume, heat transfer, component size and shape and other related physical, electrical, optical, visual/physical access, etc.

[0118] As used herein, the term memory subsystem refers to, but is not limited to: one or more memory devices; one or more memory devices and associated interface and/or timing/control circuitry; and/or one or more memory devices in conjunction with a memory buffer, and/or switch. The term memory subsystem may also refer to one or more memory devices, in addition to any associated interface and/or timing/control circuitry and/or a memory buffer assembled into a substrate, a card, a module or related assembly, which may also include a connector or similar means of electrically attaching the memory subsystem with other circuitry. The memory modules described herein may also be referred to as memory subsystems because they include one or more memory devices and buffers.

[0119] Memory subsystem support device(s) may be directly attached to the same substrate or assembly onto which the memory device(s) are attached, or may be mounted to a separate interposer or substrate also produced using one or more of various plastic, silicon, ceramic or other materials which include electrical, optical or other communication paths to functionally interconnect the support device(s) to the memory device(s) and/or to other elements of the memory or computer system.

[0120] Information transfers along a bus, channel, link or other naming convention applied to an interconnection method may be completed using one or more of many signaling options. These signaling options may include such methods as single-ended, differential, optical or other approaches, with electrical signaling further including such methods as voltage or current signaling using either single or multi-level approaches. Signals may also be modulated using such methods as time or frequency, non-return to zero, phase shift keying, amplitude modulation and others. Voltage levels are expected to continue to decrease, with 1.5V, 1.2V, 1V and lower signal voltages expected consistent with

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(but often independent of) the reduced power supply voltages required for the operation of the associated integrated circuits themselves.

[0121] One or more clocking methods may be utilized within the memory subsystem and the memory system itself, including global clocking, source-synchronous clocking, encoded clocking or combinations of these and other methods. The clock signaling may be identical to that of the signal lines themselves, or may utilize one of the listed or alternate methods that is more conducive to the planned clock frequency(ies), and the number of clocks planned within the various subsystems. A single clock may be associated with all communication to and from the memory, as well as all clocked functions within the memory subsystem, or multiple clocks may be sourced using one or more methods such as those described earlier. When multiple clocks are used, the functions within the memory subsystem may be associated with a clock that is uniquely sourced to the subsystem, or may be based on a clock that is derived from the clock related to the information being transferred to and from the memory subsystem (such as that associated with an encoded clock). Alternately, a unique clock may be used for the information transferred to the memory subsystem, and a separate clock for information sourced from one (or more) of the memory subsystems. The clocks themselves may operate at the same or frequency multiple of the communication or functional frequency, and may be edge-aligned, center-aligned or placed in an alternate timing position relative to the data, command or address information.

[0122] Information passing to the memory subsystem(s) will generally be composed of address, command and data, as well as other signals generally associated with requesting or reporting status or error conditions, resetting the memory, completing memory or logic initialization and other functional, configuration or related information. Information passing from the memory subsystem(s) may include any or all of the information passing to the memory subsystem(s), however generally will not include address and command information.

[0123] Initialization of the memory subsystem may be completed via one or more methods, based on the available interface busses, the desired initialization speed, available space, cost/complexity objectives, subsystem interconnect structures, the use of alternate processors (such as a service processor) which may be used for this and other purposes, etc. In one embodiment, the high speed bus may be used to complete the initialization of the memory subsystem(s).

[0124] Another initialization method might utilize a distinct bus, such as a presence detect bus (such as the one defined in U.S. Pat. No. 5,513,135 to Dell et al., of common assignment herewith), an IIC bus (such as defined in published JEDEC standards such as the 168 Pin DIMM family in publication 21-C revision 7R8) and/or the SMBUS, which has been widely utilized and documented in computer systems using such memory modules. This bus might be connected to one or more modules within a memory system in a point-to-point, multi-drop, daisy chain/cascade interconnect or alternate structure, providing an independent means of interrogating memory subsystems, programming each of the one or more memory subsystems to operate within the overall system environment, and adjusting the operational characteristics at other times during the normal

system operation based on performance, thermal, configuration or other changes desired or detected in the system environment.

[0125] Other methods for initialization can also be used, in conjunction with or independent of those listed. The use of a separate bus, such as described in the embodiment above, also offers the advantage of providing an independent means for both initialization and uses other than initialization, such as described in U.S. Pat. No. 6,381,685 to Dell et al., of common assignment herewith, including changes to the subsystem operational characteristics on-the-fly and for the reporting of and response to operational subsystem information such as utilization, temperature data, failure information or other purposes.

[0126] With improvements in lithography, better process controls, the use of materials with lower resistance, increased field sizes and other semiconductor processing improvements, increased device circuit density (often in conjunction with increased die sizes) will help facilitate increased function on integrated devices as well as the integration of functions previously implemented on separate devices. This integration will serve to improve overall performance of the intended function, as well as promote increased storage density, reduced power, reduced space requirements, lower cost and other manufacturer and customer benefits. This integration is a natural evolutionary process, and may result in the need for structural changes to the fundamental building blocks associated with systems.

[0127] The integrity of the communication path, the data storage contents and all functional operations associated with each element of a memory system or subsystem can be assured, to a high degree, with the use of one or more fault detection and/or correction methods described herein. Any or all of the various elements may include error detection and/or correction methods such as CRC (Cyclic Redundancy Code), EDC (Error Detection and Correction), parity or other encoding/decoding methods suited for this purpose. Further reliability enhancements may include operation retry (to overcome intermittent faults such as those associated with the transfer of information), the use of one or more alternate or replacement communication paths to replace failing paths and/or lines, complement-re- complement techniques or alternate methods used in computer, communication and related systems.

[0128] The use of bus termination, on busses as simple as point-to-point links or as complex as multi-drop structures, is becoming more common consistent with increased performance demands. A wide variety of termination methods can be identified and/or considered, and include the use of such devices as resistors, capacitors, inductors or any combination thereof, with these devices connected between the signal line and a power supply voltage or ground, a termination voltage or another signal. The termination device(s) may be part of a passive or active termination structure, and may reside in one or more positions along one or more of the signal lines, and/or as part of the transmitter and/or receiving device(s). The terminator may be selected to match the impedance of the transmission line, or selected via an alternate approach to maximize the useable frequency, operating margins and related attributes within the cost, space, power and other constraints.

[0129] As described above, the embodiments of the invention may be embodied in the form of computer-implemented processes and apparatuses for practicing those processes.

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Embodiments of the invention may also be embodied in the form of computer program code containing instructions embodied in tangible media, such as floppy diskettes, CD-ROMs, hard drives, or any other computer-readable storage medium, wherein, when the computer program code is loaded into and executed by a computer, the computer becomes an apparatus for practicing the invention. The present invention can also be embodied in the form of computer program code, for example, whether stored in a storage medium, loaded into and/or executed by a computer, or transmitted over some transmission medium, such as over electrical wiring or cabling, through fiber optics, or via electromagnetic radiation, wherein, when the computer program code is loaded into and executed by a computer, the computer becomes an apparatus for practicing the invention. When implemented on a general-purpose microprocessor, the computer program code segments configure the microprocessor to create specific logic circuits.

[0130] While the invention has been described with reference to exemplary embodiments, it will be understood by those skilled in the art that various changes may be made and equivalents may be substituted for elements thereof without departing from the scope of the invention. In addition, many modifications may be made to adapt a particular situation or material to the teachings of the invention without departing from the essential scope thereof. Therefore, it is intended that the invention not be limited to the particular embodiment disclosed as the best mode contemplated for carrying out this invention, but that the invention will include all embodiments falling within the scope of the appended claims. Moreover, the use of the terms first, second, etc. do not denote any order or importance, but rather the terms first, second, etc. are used to distinguish one element from another.

[0131] This completes the description of the preferred embodiment of the invention. Since changes may be made in the above construction without departing from the scope of the invention described herein, it is intended that all the matter contained in the above description or shown in the accompanying drawings shall be interpreted in an illustrative and not in a limiting sense. Thus other alternatives and modifications will now become apparent to those skilled in the art without departing from the spirit and scope of the invention as set forth in the following claims.

What is claimed is:

1. An enhanced four rank enabled buffer device, the buffer device comprising:
 - input ports for receiving address and command data directed to one or more of up to four ranks of memory devices;
 - one or more buffer circuits for driving one or more of the address and command data;
 - four chip select input lines for selecting between the up to four ranks of memory devices;
 - two chip select output lines for accessing one or two of the up to four ranks of memory devices; and
 - a power savings means for causing one or more of the buffer circuits to be in an inactive mode when the chip select input lines are not active;
- said buffer device operable in a first mode to access the up to four ranks of memory devices when coupled to a second enhanced four rank enabled buffer device and said buffer device operable in a second mode to access

the one or two of the up to four ranks of memory devices when not coupled to the second buffer device.

2. The buffer device of claim 1 further comprising error correction code (ECC) logic to identify and correct errors in the input data.

3. The buffer device of claim 2 wherein the ECC identifies double bit errors and corrects single bit errors to permit continuous operation of the buffer device independent of the existence of single bit errors.

4. The buffer device of claim 1 further comprising:

- a status register block that includes a plurality of internal status registers; and

- an IIC logic block for transmitting contents of the status registers to an error bus.

5. The buffer device of claim 4 wherein contents of the internal status registers include operational information, supplier identification, and a supplier die revision identifier.

6. The buffer device of claim 1 further comprising a parity checking function applied to the address and command data received by the input ports.

7. The buffer device of claim 1 wherein the buffer device is located on a one or two rank memory module.

8. The buffer device of claim 1 wherein the buffer device is located on a four rank memory module.

9. A memory module comprising:

- a rectangular printed circuit board having a first side and a second side, a length of between 149 and 153 millimeters and first and second ends having a width smaller than said length;

- a first plurality of connector locations on said first side extending along a first edge of said board that extends the length of the board;

- a second plurality of connector locations on said second side extending on said first edge of said board;

- a buffer device in communication with the circuit board for accessing up to four ranks of memory devices mounted on the first side and second side of the circuit board;

- power savings means for causing all or a portion of the buffer device to be in an inactive mode in response to current activity at the memory module; and

- a locating key having its center positioned on said first edge and located between 82 mm and 86 mm from said first end of said card and located between 66 and 70 mm from said second end of said card.

10. The memory module of claim 9 wherein the buffer device includes four chip select input lines for selecting between the up to four ranks of memory devices, a first buffer device located on the first side for accessing one or more of the up to four ranks of memory devices and a second buffer device located on the second side for accessing one or more of the up to four ranks of the memory devices not accessed by the first buffer device.

11. The memory module of claim 10 wherein half of the memory devices are mounted on the first side of the circuit board and half of the memory devices are mounted on the second side of the circuit board.

12. The memory module of claim 10 wherein the first buffer device and the second buffer device each include an independently accessible status register block with a plurality of internal status registers and an IIC block for transmitting contents of the status registers to an error bus.

13. The memory module of claim 9 further comprising an error correction code (ECC) logic module mounted to the

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Ex. 1014, p. 33

circuit board to identify and correct errors in one or more of address and command data inputs received at the memory module.

14. The memory module of claim 13 further comprising a real time error line for reporting both correctable and uncorrectable errors identified by the ECC logic module.

15. The memory module of claim 9 wherein selected contacts on said first side are coupled to selected contacts on said second side to provide redundant contacts for selected signals sent to and received from one or more of the memory devices, the buffer device and the EPROM.

16. The memory module of claim 9 wherein the memory devices are mounted in one or more of a planar and a stacked fashion.

17. A memory module comprising:

- a rectangular printed circuit board having a first side and a second side, a length of between 149 and 153 millimeters and first and second ends having a width smaller than said length;
- a first plurality of connector locations on said first side extending along a first edge of said board that extends the length of the board;
- a second plurality of connector locations on said second side extending on said first edge of said board;
- a locating key having its center positioned on said first edge and located between 82 mm and 86 mm from said first end of said board and located between 66 and 70 mm from said second end of said board;
- a buffer device in communication with the circuit board for accessing up to four ranks of memory devices mounted on the first side and second side of the circuit board, the buffer device receiving input from:
- a first chip select input pin for specifying a first rank of memory devices, the pin located in one or more of the front side of the circuit board a nominal distance of 18.495 mm to the right of the locating key and the

backside of the circuit board a nominal distance of 18.495 mm to the left of the locating key; and
a second chip select input pin for specifying a second rank of memory devices, the pin located in one or more of the front side of the circuit board a nominal distance of 14.495 mm to the right of the locating key and on the backside of the circuit board a nominal distance of 12.495 mm to the left of the locating key; and

power savings means for causing all or a portion of the buffer device to be in an inactive mode in response to current activity at the memory module.

18. The memory module of claim 17 further comprising and error correction code (ECC) logic module mounted to the circuit board to identify and correct errors in one or more of address and command data inputs received at the memory module.

19. A high-reliability high density memory arrangement with a fault tolerant address and command bus for use as a main memory that will achieve the degree of fault-tolerance and self-healing necessary for autonomic computing systems comprising:

- a memory interface chip;
- a memory controller; and
- a memory module having up to four ranks of memory devices, a power savings means for causing all or a portion of the memory module to be in an inactive mode in response to current activity at the memory module, and a buffer device coupled to the memory interface chip and the memory controller via address and command lines such that the memory controller sends address and command information to the register via the address and command lines together with check bits for error correction purposes to the register.

20. The memory of claim 17 wherein said buffer device includes one or more of an ECC register and a parity register.

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