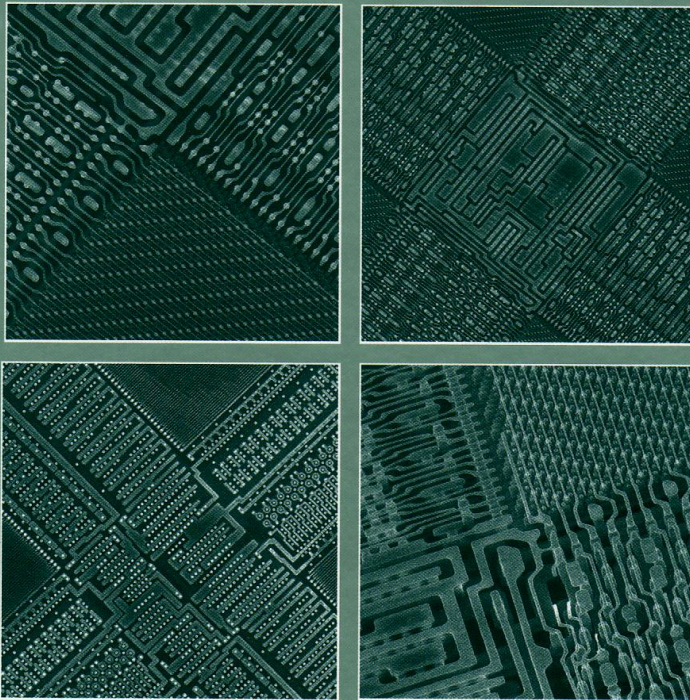


# DRAM

## CIRCUIT DESIGN

Fundamental and High-Speed Topics



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*To Susi, John, Katie, Gra  
To Julie, Kyri  
To Cassandra, Parker, S  
To Hui, Luan, a  
To Leah and M*

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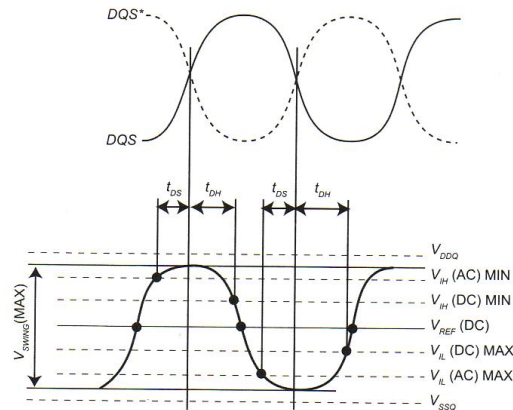


Figure 9.1 b) Setup and hold timing diagram for data.

Timing uncertainty is another challenge for data capture and processing. A clock path that runs between the clock (or strobe) pads and capture latches may include a clock receiver, timing adjust circuits, and a clock distribution network (or clock tree). Data and  $C/A$  paths, on the other hand, can be much shorter with only input buffers. With different electrical lengths, the input paths are no longer source synchronous internally. Furthermore, process, voltage, and temperature (PVT) variations introduce excessive jitter, and even post-production trimming may not be sufficient as the timing margin shrinks. One way to retain the clock and data relationship is by matched routing all the way from the pads to the capture points. On-chip, closed-loop synchronization or input path “de-skewing” is another approach. For instance, data training, either slaved to the host memory controller or conducted inside the DRAM itself, can greatly improve the capture timing and ensure reliable data capture over PVT variations. Timing alignment methods are addressed in Section 9.3 and Section 9.5.

Besides increasing  $I/O$  speed, prefetching multiple bits of data can improve memory throughput significantly without sacrificing internal array cycle time. A 4n- or 8n-Prefetch widens the internal bus compared to the external data bus. SIPO (series in parallel out) circuits and pipelines can cooperate with input circuits to tailor the incoming data into the internal buses based on the decoded commands and programmable Write latency. Control logic for the internal data path is discussed in Chapter 12. This chapter starts with input receiver design.

(Chapter 10), clock distribution networks, and one or more de-skewing circuits. Latency control (Chapter 12) and power delivery (Chapter 13) must also be considered when designing the timing circuits. Although high-speed circuit design for de-skewing is the focus of this chapter, each piece along the critical timing path inevitably interacts with the core sync circuits and contributes to the overall timing budget. Several critical timing specs, such as  $t_{AC}$ ,  $t_{DQSQ}$ ,  $t_{DQSS}$ ,  $CAS$  latency, data setup and hold, etc., can be determined through the analysis. Therefore, the design of clock synchronization circuits are integral to the overall system; design modifications and improvements are necessary to accommodate increasing clock speed.

So, how is the design of synchronization circuits impacted by increasing clock frequencies? First, the timing margins shrink with a shorter clock cycle time. In turn, the clock and data alignment must be more precise and tolerate less jitter. Because both the rising and falling edges are utilized, duty-cycle distortion jeopardizes the accuracy of data processing. Second, clock domain crossing becomes more of a problem due to timing uncertainty arising from clock skew and short cycle time. With the inherently slow transistors and minimum number of metal layers of a DRAM process, clock and power delivery is a challenge: ground bounce, voltage bumps, and noise from cross coupling degrade timing. Last but not least, impedance mismatch and inter-symbol interference (ISI) degrade signaling, which necessitates on-die calibration and training. Advanced packaging technology must be considered and modeled in the design flow to analyze timing and power delivery. Since cost remains the primary concern for DRAM manufacturers, design trade-offs must be made between cost and performance, simplicity, and scalability.

Historically, sync circuitry first appeared in DDR SDRAM, in which the clock frequency was approximately 66–133 MHz. A simple digital delay-locked loop was used to synchronize the clock with output data. High-performance GDDR4 DRAMs have pushed speeds up to multi-gigahertz range, while scaling cycle times down to less than 1 ns. Achieving such high speeds requires enormous complexity in the sync circuit and system design. However, variability in the lock time, tuning range, resolution, jitter, power, and layout can greatly impact overall system performance.

Based on various design choices, sync circuitry can be implemented using digital or analog, open or closed loop methodologies or any combination thereof. The two most common sync circuits in use today are the delay-locked loop (DLL) and the phase-locked loop (PLL). The DLL is widely used in memory interfaces for its simplicity and good jitter performance. An alternative approach is the PLL, which is usually found in communication systems and microprocessors for clock data recovery and frequency synthesis. Both the DLL and PLL are closed-loop systems with a reference and

feedback signal. The biggest difference between a DLL and a PLL is that a DLL merely passes the reference signal, while a PLL generates a new signal that is phase-locked to the reference signal.

Although both the DLL and PLL are used in high-speed DRAMs, the PLL is rarely used in high-speed DRAMs.

1. Increased complexity
2. Stability issues inherent in a high-speed PLL
3. Need for frequency locking
4. Longer lock time

Unlike the PLL, jitter in a DLL is not a problem because of the lack of jitter circulation, which occurs in a PLL. In a DLL, input jitter may directly pass to the output. However, with a low-jitter reference signal, a well-designed DLL can achieve performance as good as a PLL for clock synchronization.

An analog approach generally involves a voltage-controlled delay (VCDL) and a charge-pump phase detector. However, an all-digital DLL (ADDLL) is preferred for its scalability and portability across DRAM processes. The gate delay remains fairly constant as the technology scales, so an all-digital design can be reused with minimal modification for test and debug, an issue which can be a major concern in DRAM design. Good stability over process variations is another plus because it reduces the need for calibration. A register-controlled DLL [1], which is an ADDLL design, is addressed in detail in Section 11.2.

A higher performance DRAM design requires a sync circuit in power saving modes. To resume normal operation, the sync circuit must be relocked. The lock time of a sync circuit becomes a critical parameter. Implementations usually surpass analog open-loop architectures such as sync counter delay (RCD) can achieve, but they lack fine timing resolution. A charge-pump-controlled delay (MCD), has a faster lock time with a closed-loop architecture, but it has poor temperature tracking after initial lock. Voltage tracking is reduced by the power saving in DRAMs, which is needed for high-speed operation. Power consumption is traded for better overall timing performance.