

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

SK HYNIX INC., SK HYNIX AMERICA INC., and SK HYNIX
MEMORY SOLUTIONS INC.

Petitioners,

v.

NETLIST, INC.

Patent Owner.

Inter Partes Review No. IPR2018-00303

U.S. Patent 9,535,623

DEPOSITION OF DONALD ALPERT, Ph.D.

Washington, D.C.

July 20, 2018

9:58 a.m.

Job No. 43798

Reported by: Michele E. Eddy, RPR, CRR, CLR

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Netlist Exhibit 2031

SK hynix Inc., et al. v. Netlist, Inc.

IPR2020-01044

Page 1 of 218

1 Deposition of DONALD ALPERT, Ph.D.,
2 held at the offices of:

3 MORRISON & FOERSTER LLP
4 2000 Pennsylvania Avenue, Northwest
5 Suite 600
6 Washington, D.C. 20006
7 (202) 887-1500

8 Pursuant to Notice, before Michele E.
9 Eddy, Registered Professional Reporter, Certified
10 Realtime Reporter, and Notary Public in and for
11 the District of Columbia.
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A P P E A R A N C E S

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E X H I B I T S

(Previously marked and referred to)

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12	Exhibit 1001 U.S. Patent No. 9,535,623	11
13	Exhibit 1003 Declaration of Dr. Donald Alpert	7
14	Exhibit 1014 U.S. Patent Application No.	8
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16	Exhibit 1015 U.S. Patent Application No.	8
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18	Exhibit 1016 U.S. Patent Application No.	8
19	2008/0147897	
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1 P R O C E E D I N G S

2 Washington, D.C.

3 July 20, 2018

4 - - -

5 DONALD ALPERT, Ph.D.

6 having been duly sworn, testified as follows:

7 EXAMINATION BY COUNSEL FOR PATENT OWNER

8 BY MR. ARJOMAND:

9 Q Please state your name for the record.

10 A It's Donald Alpert, A-L, P like Peter,
11 E-R-T.

12 Q Good morning, Dr. Alpert. Is there any
13 reason why you can't testify truthfully today?

14 A No, there's no reason.

15 Q And there any reason why you can't
16 testify competently today?

17 A No, there is no reason of that.

18 Q Dr. Alpert, how many times have you been
19 deposed?

20 A To the, kind of, best of my general
21 recollection, I would say probably about 15 times,
22 maybe 15 to 20.

23 Q Okay. And do you recall how many of
24 those times were related to an IPR proceeding?

25 A Probably about -- I think about four,

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1 **maybe five previous ones.**

2 Q Okay, great.

3 So it appears that you may be familiar
4 with a deposition in an IPR proceeding, but let me
5 just go over a few ground rules.

6 I'm going to be asking a number of
7 questions today, and your answers will be recorded
8 by the court reporter here. I ask that you
9 respond to my questions with a verbal answer since
10 the court reporter can't record nodding of the
11 heads. Is that okay?

12 **A Yes, that's fine.**

13 Q You understand that you can't take a
14 break or consult with your counsel while a
15 question is pending unless it involves a question
16 of privilege?

17 **A Yes, that's my understanding.**

18 Q You understand that you cannot consult
19 with your counsel regarding your testimony during
20 any of the breaks today?

21 **A Yes, I understand that.**

22 Q Dr. Alpert, did you meet with counsel in
23 preparation for today's deposition?

24 **A Yes, I did.**

25 Q Whom did you meet with?

1 **A With Mr. Suh.**

2 Q And when did you meet with Mr. Suh?

3 **A Yesterday.**

4 Q For how many hours did you meet with
5 Mr. Suh?

6 **A It was about five hours.**

7 Q Okay. Did you spend any additional time
8 preparing for today's deposition beyond the five
9 hours that you met with Mr. Suh?

10 **A Yes, I did.**

11 Q How many hours did you spend preparing
12 for the deposition?

13 **A I would estimate about 10 to 15 hours.**

14 Q So would it be fair to say that you
15 spent roughly a total of 15 to 20 hours in
16 preparation for today's deposition?

17 MR. SUH: Objection to form.

18 **A That sounds like it would be fairly**
19 **accurate.**

20 Q Did you review any documents in
21 preparation for today's deposition?

22 MR. SUH: Objection to form.

23 **A Yes, I did.**

24 **(Exhibit 1003 was previously marked**
25 **and referred to.)**

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1 Q Did you review your declaration, Exhibit
2 1003, in preparation for today's deposition?

3 A Yes, I did.

4 (Exhibit 1014 was previously marked
5 and referred to.)

6 Q Did you review Exhibit 1014, the
7 Hazelzet reference, in preparation for today's
8 deposition?

9 A Yes, I did review that.

10 (Exhibit 1015 was previously marked
11 and referred to.)

12 Q Did you review Exhibit 1015, the Amidi
13 reference, in preparation for today's deposition?

14 A Yes, I did.

15 (Exhibit 1016 was previously marked
16 and referred to.)

17 Q Did you review Exhibit 1016, the Talbot
18 reference, in preparation for today's deposition?

19 A Yes, I did.

20 Q And did you review Exhibit 1017, the
21 Buchmann reference, in preparation for today's
22 deposition?

23 A Yes, I did review Buchmann.

24 Q Dr. Alpert, do you understand that this
25 inter partes review was instituted by the Board?

1 **A** Yes, it's my understanding there was a
2 decision issued. I think it's called an
3 institution decision. I believe that's probably
4 what you're referring to.

5 **Q** Correct.

6 And did you review the institution
7 decision in preparation for today's deposition?

8 **A** Yes, I did.

9 **Q** Were you aware that the patent owner
10 filed a preliminary response prior to the
11 institution decision?

12 **A** Yes, I have seen a document like that,
13 and it's my understanding that would have been
14 filed prior to the Patent Board's decision.

15 **Q** Were you -- strike that.

16 Did you review the patent owner's
17 preliminary response in preparation for today's
18 deposition?

19 **A** Yes, I did.

20 **Q** Did you review the petitioner's petition
21 in preparation for today's deposition?

22 **A** Yes, I also reviewed the petition.

23 **Q** Is there any other document that you
24 reviewed for preparation for today's deposition
25 that I have not referenced yet?

1 MR. SUH: Objection to form.

2 A Yes.

3 Q What are those documents?

4 A Off the top of my head, there were
5 several other exhibits that were filed with the
6 petition. I don't think I remember exactly which
7 ones I looked at, but they were not among the
8 particular references that you mentioned so far.

9 Q Do you recall their names?

10 A One I recall, I believe, was something
11 like Hutsell, I think H-U-T-S-E-L-L. There were
12 some exhibits that included file history
13 information about the -- I guess the '623 patent
14 is what we're talking about today. And I do
15 believe I reviewed deposition testimony that I
16 gave last year for -- I believe it was 837 IPR.

17 Q Okay.

18 Do you recall reviewing any other
19 documents beyond what I've asked you about and
20 your previous answer?

21 A I do generally recall reviewing -- I
22 believe I reviewed other documents from the
23 exhibit list, but I don't think I could identify
24 them specifically just sitting here right now.

25 Q Okay. Thank you.

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1 And do you recall reviewing any
2 documents outside of the exhibit list beyond what
3 you've testified today?

4 **A No, not that I recall.**

5 Q Dr. Alpert, are you aware that there's a
6 co-pending ITC proceeding with this inter partes
7 review proceeding?

8 **A Yes, I'm generally aware there is some**
9 **type of investigation, I guess it's called, by the**
10 **ITC.**

11 Q Did you review any documents associated
12 with that co-pending ITC proceeding in preparation
13 for today's deposition?

14 **A No.**

15 Q Dr. Alpert, we've been referring to this
16 as an IPR proceeding. To be specific, this IPR is
17 IPR number 2018-00303 for U.S. Patent Number
18 9,535,623. I am placing Exhibit 1001 from this
19 IPR in front of you. And this is the U.S. Patent
20 Number 9,535,623.

21 (Exhibit 1001 was previously marked and
22 referred to.)

23 Q I'm going to be referring to this patent
24 as the '623 patent. Is that okay?

25 **A Yes, that's fine.**

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1 Q I'll set forth some additional terms to
2 make this deposition go smoothly. I'll be
3 referring to a person of ordinary skill in the art
4 as a POSITA. Is that okay with you?

5 A **Yes, that's fine.**

6 Q Do you understand a person of ordinary
7 skill in the art to be the person of ordinary
8 skill in the art at the time of the invention?

9 A **Yes, that's my understanding.**

10 Q Let me place in front of you Exhibit
11 1003, your declaration in this IPR proceeding.

12 Dr. Alpert, I would like to direct you
13 to paragraph 42 of your declaration. Take a
14 moment to review that paragraph.

15 A **(Document review.)**

16 **All right. I've reviewed paragraph 42.**

17 Q Thank you.

18 Did you use June 12th, 2009, as set
19 forth in paragraph 42 of your declaration, as the
20 time of invention?

21 A **Yes, that was what I assumed.**

22 Q And from this point on, when I refer to
23 the time of invention, will you understand it is
24 as of June 2009?

25 A **Yes. I don't see any reason that any**

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1 question would come up about that. If there is
2 some reason that I wanted to clarify either the
3 question or something I was saying, I would raise
4 it at the time.

5 Q Thank you.

6 Please turn to paragraph 43 of your
7 declaration. And if you can take a moment to
8 review that paragraph.

9 A (Document review.)

10 Okay. I have reviewed that.

11 Q Great.

12 Dr. Alpert, how did you go about
13 determining the level of skill in the art as set
14 forth in paragraph 43 of your declaration?

15 A Well, I considered the field of the
16 technology and the specific characteristics of the
17 disclosed embodiments and the invention. And in
18 considering that, I also have been familiar with
19 the education of people studying electrical
20 engineering, computer systems that would have been
21 an appropriate background for this patent, and
22 based on -- as well as on my experience in
23 industry, I had some idea of about how much
24 experience -- practical experience I thought
25 someone would need to be able to understand this

1 **patent.**

2 Q Is there anything else beyond your
3 previous testimony that you relied upon to
4 determine the level of skill in the art as set
5 forth in paragraph 43 of your declaration?

6 A **No. I think that covers it.**

7 Q And are the conclusions that you have
8 reached in this declaration, Exhibit 1003, based
9 on the level of skill that you set forth in
10 paragraph 43 of your declaration?

11 MR. SUH: Objection to form.

12 A **Yes, what I've described in paragraph 43**
13 **is the level of skill that I assumed in my**
14 **analysis.**

15 Q In determining the level of ordinary
16 skill in the art, Dr. Alpert, did you consider
17 prior art solutions to the types of problems
18 encountered by a person of ordinary skill in the
19 art?

20 A **When you're asking about prior art**
21 **solutions, do you mean like specific references or**
22 **just general knowledge and experience that someone**
23 **might have?**

24 Q Well, let's break it up. Let's start
25 with specific references.

1 **A** **No, I don't recall considering any**
2 **specific references.**

3 **Q** And did you consider the experience that
4 someone might have in determining the level of
5 ordinary skill in the art in this proceeding?

6 **A** **Yes, I did consider what would have been**
7 **the general knowledge and experience that a person**
8 **would have to understand the patent. And as I**
9 **explained here, I believe the level that I**
10 **summarized would be appropriate.**

11 **Q** And what was the basis for you to
12 determine that general knowledge and experience?

13 **A** **Well, you know, I've had several decades**
14 **of experience in the industry, working on various**
15 **types of computer systems, projects, hiring,**
16 **supervising and training new college graduates and**
17 **kind of junior engineers, and I'm familiar with**
18 **the textbooks, both from teaching at universities**
19 **as well as from looking at newer textbooks from**
20 **time to time.**

21 **Q** When was the last time that you taught
22 at a university?

23 **A** **I believe it was around 2004.**

24 **Q** And when was the last time that you
25 performed a project in the computer industry,

1 specifically a paid project?

2 **A My belief is around 2008.**

3 Q Do you recall what that project was?

4 **A Yes.**

5 Q What was it?

6 **A I was retained as a consultant by a**
7 **company -- a start-up company called Montalvo**
8 **Systems, M-O-N-T-A-L-V-O.**

9 Q And was the start-up company project
10 pertaining to a memory module?

11 MR. SUH: Objection to form.

12 **A It was directed toward microprocessors**
13 **that would be used in conjunction with memory**
14 **modules.**

15 Q In determining the level of ordinary
16 skill in the art, did you consider the rapidity
17 with which inventions are made in this field?

18 **A I don't recall specifically considering**
19 **that, but I have been familiar through**
20 **conferences, through other work that I have done,**
21 **through textbooks, and understanding how the field**
22 **has advanced.**

23 Q Dr. Alpert, what do you believe to be
24 the field of the '623 patent?

25 **A Well, looking at the patent, in**

1 column 1, it looks like lines about 21 to 26, the
2 patent describes, it says, "The Field of the
3 Disclosure," and it says, "The present disclosure
4 relates to the operation of memory modules.
5 Specifically, the present disclosure relates to a
6 memory module capable of handshaking with a memory
7 controller of a host system." And I believe
8 that's a useful summary.

9 Q In determining the level of ordinary
10 skill in the art, did you consider the
11 sophistication of the technology at issue here?

12 A I considered the disclosure in the
13 claims. I don't know if that falls under the
14 scope of the technology at issue.

15 Q Well, I guess my question was more
16 directed to the sophistication of the technology
17 at issue. So let me maybe ask you this way.

18 Would you consider working on a
19 processor to be a more sophisticated technical
20 challenge than working on a memory module?

21 A You know, it's a very broad question. I
22 think it would depend on the nature of the work
23 that was being performed on. Sounds like two
24 different projects there.

25 Q But from your experience with processors

1 and your discussions in your declaration about
2 your experience with memory modules, which would
3 you say involves more sophisticated technology?

4 **A I don't think I would have a general**
5 **answer to that question.**

6 **Q** What do you think is the sophistication
7 level of memory module technology?

8 **MR. SUH:** Objection. Form.

9 **A Again, it's a very broad question. I**
10 **don't think I would have a single answer that**
11 **would characterize that.**

12 **Q** Let me ask you this. Does a person of
13 ordinary skill in the art need to have a Ph.D. to
14 understand the technology that's associated with a
15 memory module?

16 **A Well, I would say generally I don't**
17 **think a person needs to have -- you know, requires**
18 **a specific credential or degree in order to be**
19 **able to understand a particular technology or to**
20 **do productive work.**

21 **Q** So you think that a person without any
22 technical training could understand the operations
23 of a memory module?

24 **MR. SUH:** Objection. Mischaracterizes
25 testimony.

1 A No, I wasn't -- I didn't mean to say
2 that. I don't know if it sounded that way.

3 Q But it is your position that a person of
4 ordinary skill in the art would need technical
5 training to understand the operations of a memory
6 module. Correct?

7 A Yes. And, in particular, I documented
8 the level that I thought would be appropriate to
9 understand the '623 patent.

10 Q Do you believe that there are aspects of
11 memory module technology that are more complicated
12 than processor technology?

13 MR. SUH: Objection to form.

14 A I would say that there are certain
15 aspects of memory module technology that are more
16 complicated than certain aspects of -- processor
17 technology I believe was the question?

18 Q Correct.

19 What would those aspects be as you sit
20 here today?

21 MR. SUH: Objection to form.

22 A Well, one example that comes to mind is
23 just the physical aspects of designing the module
24 and particularly the issues of the signal
25 integrity that are involved in communicating

1 information throughout the module -- and, let's
2 say, for example, DRAM chips could be a module
3 with those types of chips -- is, in fact, quite
4 a -- quite a challenging problem, especially given
5 the kind of market-driven constraints, say, for
6 cost on that. In a processor, let's say one of
7 the simpler aspects might be just running and
8 analyzing the results of some, say, basic
9 instruction tests.

10 Q What's your understanding of signal
11 integrity in the context of memory module
12 technology?

13 A It's my general understanding that it's
14 one of the -- one of the significant technical
15 challenges of developing modules and,
16 particularly, being able to develop both the
17 components and standards for modules so they can
18 be widely produced using chips from different
19 vendors.

20 Q What is signal integrity?

21 A Signal integrity would involve the
22 reliable communication of information.

23 Q And is the issue of signal integrity for
24 a memory module related to the communication
25 between the memory controller and the memory

1 module?

2 A That would be one aspect, yes.

3 Q What would be other aspects?

4 A Within the module itself, the signals
5 need to be -- say, the command address and data
6 signals, clocks, need to arrive at all of the
7 memory chips that would be on a module.

8 Q Are there any other aspects beyond
9 signal integrity that are more complicated in
10 memory module technology than processor
11 technology?

12 MR. SUH: Objection. Form.

13 A Another example that comes to mind is
14 that it can affect -- be quite challenging to test
15 the memory module either at production or in a
16 system. And, again, I would say some aspects of
17 that issue of the testing are more complicated
18 than certain simpler aspects of processor
19 technology. Again, I would use the example of
20 just running some kind of straightforward
21 instruction tests on the processor just to check
22 the results.

23 Q I see.

24 What aspects of -- strike that.

25 What makes testing the memory module

1 challenging?

2 A Well, one characteristic would be the
3 nature of the faults that might arise. Some of
4 them might just be the metal on the connectors.
5 Others might relate internally to some errors that
6 might come about because of the circuits and the
7 physical structures that are used to implement the
8 memory and the circuits to access the memory. And
9 that can be, I think, quite a complex task to
10 analyze those issues. And then, of course, the
11 testing would need to be done efficiently. It can
12 take an excessive amount of time and incurs both
13 cost and potentially downtime of the system to do
14 the testing.

15 Q Going back to signal integrity, what
16 makes that challenging in the context of memory
17 modules?

18 A I would say primarily it's the speed at
19 which the signals are communicated.

20 Q Are there any other reasons that make
21 signal integrity challenging for a memory module?

22 A There can be issues involved with cross
23 talk or other type of interference between
24 different signals that would be routed on the
25 module. That's another example.

1 Q So when you refer to cross talk, is that
2 cross talk between memory devices on the memory
3 module?

4 A No. In this context I was talking about
5 cross talk between signals that are being routed,
6 for example, on different metal traces on the
7 memory module.

8 Q I see.

9 Could you explain to me what the issue
10 of cross talk is in that context.

11 A Well, a signal on -- that's being routed
12 on one metal trace may affect the integrity of a
13 signal on another metal trace that may cause it to
14 be either recognized incorrectly or to cause some
15 influence on a second signal that would affect
16 the -- either the value or the -- kind of noise
17 immunity, noise susceptibility on that second
18 signal.

19 Q Is that due to the fact that the lines
20 are in such close proximity to each other?

21 A It would be related to the proximity of
22 the lines as well as the speed.

23 Q I see.

24 Would it also be related to the length
25 of the traces or the lines?

1 A The issues of signal integrity are
2 related to the length. At the moment, sitting
3 here, I don't recall whether the length has
4 particularly an impact on the cross talk.

5 Q I see.

6 So, from your experience, typically what
7 are the measures that -- strike that.

8 From your experience what are the
9 measures that are typically taken to ensure signal
10 integrity in the context of memory modules?

11 MR. SUH: Objection to form.

12 A Well, one aspect is that there would be
13 extensive amounts of simulation and
14 characterization -- simulation of the design,
15 characterization of the prototypes. There would
16 also be some issues on the specification, for
17 example, to ensure that certain speeds were
18 satisfied. There would be issues of the so-called
19 termination of the signals to try to avoid
20 reflections, for example, that could be a problem.

21 And there can also be, say, adjustments
22 of the circuits that are used to interface the
23 signals, adjustments related to the drive
24 strength, for example.

25 Q Are those adjustments done in the design

1 phase, or are they done during the operation of
2 the memory module itself?

3 A Well, thinking back specifically, there
4 was -- I was the manager of architecture for a
5 project at Intel around the year 2000 that was a
6 chipset. It was called the 815. And, in
7 particular, that -- there's a memory controller
8 that's part of that chipset. And there was a new
9 interface being designed for that memory
10 controller to work with 133-megahertz memories.

11 And, as I recall, there were various
12 parameters that could be tuned. Particularly, I
13 remember some resistors that would be in the
14 drivers, and those -- that information was highly
15 simulated. And, as well, after the chips were
16 manufactured, the characteristics of those drivers
17 were measured both in electronic testers as well
18 as in systems. So the -- say a particular
19 resistor value could be selected. It could either
20 be kind of what they call like a burning a fuse at
21 the time of manufacturing or potentially be
22 adjusted based on the characterization in a
23 particular system.

24 Q Are there any actions taken by a memory
25 module during its operation to ensure signal

1 integrity?

2 MR. SUH: Objection. Form.

3 Q Maybe I can explain my question a little
4 better.

5 I feel from your previous answer that
6 most of the discussion was directed to actions
7 that designers take during the design of a memory
8 module to ensure that once the memory module is
9 utilized, it operates with good signal integrity.

10 Is there anything that is done, say, in
11 real time, when the memory module is operating, to
12 ensure good signal integrity?

13 MR. SUH: Same objection.

14 A Well, there is certain testing that
15 could be done when a system is first powered on as
16 well as during the operation of a system that
17 would relate, for example, to training and
18 calibrating some of the signals being communicated
19 within the module.

20 Q So can you explain what that testing is.

21 A There are tests -- just, for example,
22 what I -- what I recall were the -- say, for
23 example, a -- a clock signal may be adjusted in
24 such a way as ensuring that the data is -- data or
25 control information is received reliably at the --

1 say, for example, at a DRAM chip.

2 Q Could you explain a little bit more?

3 I'm not sure I'm following.

4 A Well, many of the chips in production
5 for the past ten years are synchronous, say
6 particularly for dynamic RAMS. So the information
7 that the chip receives, in particular, the, say,
8 address and commands, are received synchronously
9 with a clock. And depending on the differences in
10 routing of those signals, the clock versus the
11 address and command -- either on the module or
12 based on variations within the manufacturing and
13 temperature or current conditions of the chip --
14 in order to receive information reliably, it's
15 necessary that the clock be in the appropriate
16 phase with the information that's being received
17 so that it can be, say, for example, sampled in a
18 latch or flip-flop.

19 Q So upon power on, the memory module
20 tests the clock signal?

21 MR. SUH: Objection. Mischaracterizes
22 testimony. Outside the scope.

23 A Within the memory module, there would be
24 tests that were performed that would be used to
25 adjust the clock signal such that the information

1 would be communicated reliably with respect to --
2 to the clock that's being used to synchronize the
3 DRAM.

4 Q How would the memory module test to
5 adjust the clock signal?

6 MR. SUH: Objection. Outside the scope.
7 Mischaracterizes testimony.

8 A One way that I've seen is that there can
9 be information that's sent together with the
10 clock, and then the DRAM can report back whether
11 there are some errors associated. So what I've
12 seen is that, actually, first it will adjust the
13 clock to the point that there would be about
14 50 percent errors, and that's a way of determining
15 that the data is actually being received in the
16 middle of a clock phase or too close to the edge
17 and then the clock delay will be backed off such
18 that the information can be communicated reliably
19 with respect to the adjusted clock.

20 Q So is this test done by the memory
21 module -- strike that.

22 Is this test done by logic on the memory
23 module, or is it done by the memory controller in
24 communication with the memory module? Let me ask
25 that question again.

1 When you previously testified that there
2 can be information that's sent together with the
3 clock, who sends that information?

4 MR. FUSCHILLO: Objection. Outside the
5 scope. Calls for a legal conclusion.

6 A Well, if the information was, for
7 example, an address, then that would come from the
8 processor or another bus master. It could be
9 information that would be a command, such as a
10 precharging or opening a page in a DRAM device
11 that would come from the memory controller, and
12 it's possible to have a -- some type of a buffer
13 circuit on the module itself that would be used to
14 generate the signals that go to the DRAM.

15 Q I see.

16 So when you previously testified the
17 DRAM can report back whether there are some
18 errors, it would be either reporting back to such
19 a buffer device or to the memory controller?

20 A From my experience, yes, it could be
21 either.

22 Q We've been talking a little bit about
23 the clock. What else, in your experience, is
24 typically tested upon power-up or initialization
25 in a memory module?

1 A Well, we did talk about the clock and
2 how that might be adjusted, but, generally, that
3 would be related to reliable communication of
4 address commands and data to the memory chip. So
5 all of that communication would be tested. It's
6 also possible to test the reliability of the data
7 array itself.

8 Q So if the clock is not properly adjusted
9 upon power-on or initialization, what happens?

10 MR. SUH: Objection. Form.

11 A I'm not sure that I -- that I
12 understand. Do you mean what happens in a system,
13 what would happen if it weren't adjusted? Can you
14 be a little bit clearer?

15 Q Yes. Let me try to rephrase the
16 question.

17 So we've been discussing the importance
18 of ensuring that the clock is properly operating.
19 Do you recall that testimony?

20 A Yes.

21 Q And so if the clock is not properly
22 operating, what happens on the memory module?

23 MR. SUH: Same objection.

24 A Well, generally, if the clock were not
25 properly adjusted so that the information could be

1 communicated reliably, then there would be errors.
2 There would be accesses to the -- potentially, to
3 incorrect words or locations of the memory array,
4 or potentially the wrong data could be sent or
5 received to the memory chip and internally to the
6 array.

7 Q Are there any other errors, as you sit
8 here, that you believe could occur if the clock is
9 not properly functioning?

10 A Not that I can think of right at the
11 moment.

12 Q What would you call the error that is
13 associated with a clock that's not properly
14 functioning? Is there a term of art for that?

15 A At the moment nothing -- no specific
16 term comes to mind.

17 Q Would you call it a synchronization
18 error?

19 MR. SUH: Objection. Form. Calls for
20 speculation.

21 A I believe it might be called that. If
22 someone used that term, I would want to understand
23 more specifically what they meant by it.

24 Q What do you understand that term to
25 mean?

1 **A** Well, synchronization would generally
2 imply that two circuits are able to operate off of
3 a common clock and that information can be
4 communicated reliably; that the delays are such
5 that the clock can be effectively used to operate
6 the circuits together and at the same time.

7 **Q** Would there be a synchronization error
8 if signal integrity is not properly addressed on a
9 memory module?

10 MR. SUH: Objection. Form.

11 **A** I would say one type of error could be a
12 synchronization error.

13 **Q** Do you have the '623 patent in front of
14 you?

15 **A** Yes.

16 **Q** Have you read the '623 patent in its
17 entirety?

18 **A** Yes, I have.

19 **Q** And have you read its claims?

20 **A** Yes, I have.

21 **Q** Are you familiar with its prosecution
22 history?

23 **A** I am generally, yes.

24 **Q** Did you read the '623 patent's
25 prosecution history?

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1 A I have reviewed it. I wouldn't say I
2 necessarily read every word in it.

3 Q Fair enough.

4 MR. ARJOMAND: We've been going for
5 about an hour. I would like to get into a new
6 area right now. Would you like to take a break
7 before we do so?

8 THE WITNESS: Yes. If it's a good
9 breaking point, I think it would be good to do it
10 now.

11 MR. ARJOMAND: Great. Off the record.
12 Discussion off the record.

13 (A brief recess was taken.)

14 MR. ARJOMAND: Back on the record.

15 BY MR. ARJOMAND:

16 Q Dr. Alpert, I'm placing in front of you
17 Exhibit 1014, the Hazelzet reference.

18 So, what I would like to do is go
19 through the elements of claim 1 of the '623 patent
20 and ask you what you're pointing to in Hazelzet
21 set for meeting those elements. So if you would
22 like to open up the '623 patent, claim 1, which I
23 believe is in front of you.

24 Dr. Alpert, do you see that claim 1
25 recites a memory module?

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1 **A Yes.**

2 **Q What elements are you relying on in**
3 Hazelzet as meeting the claim element "memory
4 module"?

5 **A (Document review.)**

6 I was just consulting with the
7 declaration in order to refresh my memory, and I
8 don't know how much detail you wanted to go into,
9 but in paragraph 122 -- it's on page 52 -- it does
10 indicate that Hazelzet -- and I don't know if
11 that's the correct pronunciation, it's just a
12 habit I've developed -- discloses dual in-line
13 memory modules -- it's capital D, capital, I,
14 capital M, capital M -- configured to operate with
15 a memory controller. Then it lists certain
16 citations, and there's additional information in
17 the following paragraphs.

18 **Q But as you sit here today, is there --**
19 when we're looking -- strike that.

20 Can you turn to figure 2 of the Hazelzet
21 reference. Are you relying on element 20 in
22 figure 2 of the Hazelzet reference as meeting the
23 memory module recitation of claim 1 of the '623
24 patent?

25 **A (Document review.)**

1 So, yes, I was -- just to make sure I
2 get the right element number -- but in
3 paragraph 38 of Hazelzet, it does say, second
4 sentence, "In this figure 2, the server comprises
5 a novel DIMM," D-I-M-M, "20." And so element 20
6 from figure 2 is a memory module.

7 Q Thank you.

8 While we're here on figure 2, what is
9 your understanding of the memory interface chip
10 18?

11 A (Document review.)

12 The memory interface chip 18, I believe,
13 a person of ordinary skill in the art would
14 recognize that to be a chip that drives the
15 information between the controller and the DIMMs,
16 and, in particular, because there may be a large
17 number of DIMMs, it's important to provide that
18 electrical amplification.

19 Q So the memory controller 19 would be
20 unable to drive the DIMMs without the memory
21 interface chip 18?

22 A It would depend on the memory capacity
23 whether the -- whether it's necessary to have that
24 driving. It would also depend on the frequency of
25 operation, whether that was required.

1 Q Is there a certain capacity, from your
2 knowledge in the art, that, once met, requires a
3 chip-like memory interface chip 18?

4 A Well, just based on my recollection of
5 chipsets from Intel, I believe they -- that they
6 were commonly limited to four DIMMs before some
7 type of -- some type of interface chip performing
8 the function that I've mentioned would be
9 required.

10 Q So more than four DIMMs requires a
11 memory interface chip 18?

12 A That's my recollection of Intel
13 products. Again, that might depend on the
14 environment, you know, kind of the cost structure
15 and form factors associated with personal
16 computers as opposed to some other systems.

17 Q Are there four DIMMs shown in figure 2
18 of Hazelzet?

19 A (Document review.)

20 I just wanted to hear the question
21 again.

22 (Record read.)

23 A I don't see -- and I've looked briefly,
24 say, at paragraph 39, and I also don't see a
25 description that there are four DIMMs shown in

1 **figure 2.**

2 Q Okay. Thank you.

3 Still focusing here on figure 2 of
4 Hazelzet, what is 15 in figure 2?

5 A **In figure 2 there's two elements labeled**
6 **15 or, I should just say, at least two sets of**
7 **conductors that are for communicating data.**

8 Q And what is 16 in figure 2 of Hazelzet?

9 A **(Document review.)**

10 **Sorry, the question again.**

11 **(Record read.)**

12 A **16 is labeled that it's command and**
13 **check bits that are communicated.**

14 Q So, 16, between the memory controller
15 and the memory interface chip, is a conductor that
16 communicates command and check bits between those
17 two elements?

18 A **Sorry, between which elements again?**

19 Q Let me ask the question again.

20 So 16 is a conductor that communicates
21 command and check bits between the memory
22 controller and the memory interface chip?

23 A **Yes. And there's also a path for the**
24 **command and check bit 16 to arrive at the**
25 **ECC/Parity register 21.**

1 Q Is there a difference between the
2 conductor 16 -- strike that.

3 Is there a difference in conductor 16
4 between the memory interface chip and the memory
5 controller and conductor 16 between the memory
6 interface chip and the ECC/Parity register 21?

7 A **The information on those paths would be**
8 **the same. The memory interface chip would be --**
9 **would have stronger drivers to communicate that**
10 **information.**

11 Q So when you say that the memory
12 interface chip would have stronger drivers, is the
13 signal speed between memory interface chip and the
14 ECC/Parity register 21 higher than the signal
15 speed between the memory controller 19 and the
16 memory interface chip 18?

17 MR. SUH: Objection. Mischaracterizes
18 the testimony.

19 A **Yes, I'm not sure what you mean by**
20 **"speed." Can you help me understand?**

21 Q Well, what I'm trying to understand is,
22 does -- does the conductor 16 between the memory
23 interface chip 18 and the ECC/Parity register 21
24 operate at a higher bit rate than the conductor 16
25 between the memory controller 19 and the memory

1 interface chip 18?

2 A No. I believe a person of ordinary
3 skill in the art would understand that the
4 operating speed of communication would be the same
5 for those.

6 Just going back to a previous question,
7 I did notice -- in terms of whether there are
8 multiple DIMMs depicted, something that I noticed
9 is that on the right side of figure 2, it shows
10 another DIMM port. So it's like 15A and 16A,
11 we've been talking about.

12 So I believe a person of ordinary skill
13 in the art, looking at this figure, would
14 understand that there are more DIMMs present. And
15 also in paragraph 42 of Hazelzet the first
16 sentence says, "It should be understood that
17 although only one DIMM" -- it says 10 and 20 --
18 "is shown in figures 1 and 2, that in actuality
19 the server would contain many such DIMMs."

20 Q Thank you.

21 So turning back to conductor 15 in
22 figure 2, would the data rate between the memory
23 interface chip 18 and the ECC/Parity register 21
24 be different than the data rate between the memory
25 controller 19 and the memory interface chip 18 on

1 conductor 15?

2 **A** **No. I believe a person of ordinary**
3 **skill in the art would understand those to be the**
4 **same -- communicating information at the same**
5 **rate.**

6 **Q** And can you explain to me what element
7 17 is in figure 2 of Hazelzet?

8 **A** **So line 17 is a clock.**

9 **Q** And is there any difference between line
10 17 with respect to ECC/Parity register 21 and the
11 memory interface chip 18 on one hand and memory
12 controller 19 and the memory interface chip 18 on
13 the other hand?

14 MR. SUH: Objection to form.

15 **A** **Again, I believe a person of ordinary**
16 **skill in the art would understand that both of**
17 **those clock signals are operating at the same**
18 **frequency and are used synchronously.**

19 **Q** So, as you sit here today, would you say
20 that conductors 15, 16, and 17, between the
21 ECC/Parity register 21 and the memory interface
22 chip 18, are identical to conductors 15, 16, and
23 17 between memory controller 19 and the memory
24 interface chip 18?

25 **A** **Well, as I heard the question, I think**

1 you're asking whether -- that those would be
2 identical. And I don't believe a person of
3 ordinary skill in the art would understand that
4 there's a single metal trace, for example, that's
5 used for both kind of segments of communicating
6 that information.

7 Q Correct.

8 A I was just going to say, just for
9 example, you know, 15, between the memory
10 controller and the memory interface chip, would
11 not necessarily be the same as 15, you know, the
12 same metal, continuous metal line of trace between
13 the memory chip and the ECC/Parity register 21.

14 Q Well, what I'm trying to get at is,
15 maybe for the -- to make it simpler, let's call
16 15, 16, and 17 a link between the memory interface
17 chip 18 and memory controller 19. Do you
18 understand that? Just as a --

19 A I would say as I -- I think we can use
20 that as a code word, not implying any specific
21 technical content that might be associated with
22 any --

23 Q Yes, it's just for a naming -- just for
24 purposes of us to be able to communicate easily,
25 I'm just calling it a link. I'm calling 15, 16,

1 and 17, between memory interface chip 18 and
2 memory controller 19, a link, just for us to --

3 **A Okay. Well, I'll understand that when**
4 **you say "link," that that's what you're referring**
5 **to.**

6 **Q That's in the context of figure 2 here.**

7 **A Okay. Thank you.**

8 **Q Then let's also say that when I refer to**
9 **a link between the ECC/Parity register 21 and the**
10 **memory interface chip 18, I'm referring to**
11 **conductors 15 and 16 and 17 between those two**
12 **elements. Do you understand?**

13 **A Yes.**

14 **Q So are there any operational differences**
15 **between the link -- strike that.**

16 **Are there any operational differences on**
17 **one hand with respect to the link between the**
18 **ECC/Parity register 21 and the memory interface**
19 **chip 18 and on the other hand the link between the**
20 **memory controller 19 and the memory interface chip**
21 **18?**

22 **A You know, sitting here right now, I**
23 **don't remember anything described for the memory**
24 **interface chip that would indicate a difference in**
25 **how those two interfaces operate.**

1 Q Those two links?

2 A Yes, the two links coming -- both of
3 which are coupled to the memory interface chip.

4 Q I see.

5 So is truly the memory interface chip
6 designed to simply drive the signals harder? Is
7 that its sole purpose?

8 A Yes, I believe that's what a person of
9 ordinary skill in the art would understand.

10 Q And is it typically positioned off of
11 the memory module, as shown here in figure 2?

12 A Examples that I can think of would be on
13 the motherboard, so off of the memory module, yes.

14 Q And when we discuss -- strike that.

15 When we previously had discussed issues
16 related to signal integrity, would that apply with
17 regard to the distance between the memory
18 controller and the memory interface chip on the
19 motherboard?

20 A I don't remember exactly what we talked
21 about before, but just in this context, the signal
22 integrity for that what you've called a link would
23 be a concern, and that would be related, in part,
24 to the length of the traces that were between the
25 memory controller and the memory interface chip.

1 Q And would there be a similar concern
2 with regard to signal integrity between the memory
3 interface chip 18 and the ECC/Parity register 21
4 in figure 2 of Hazelzet?

5 A There would be a concern. Whether it's
6 similar or not, I haven't -- I haven't given that
7 much thought. There is also the data between the
8 module and the memory interface chip on 15 which
9 is shown as being communicated with the SDRAMs and
10 not the ECC/Parity register 21.

11 Q Correct.

12 When I try to use the naming convention
13 of a link to describe 15, 16, and 17 between
14 memory interface chip 18 and memory controller 19,
15 I sense that you paused a little bit. Is there a
16 technical understanding to the term "link"?

17 A There is a -- a usage in the field of
18 networking, at least, that I think has also been
19 used in computer systems. So that was what did
20 give me pause, whether or not, in fact, it would
21 be understood necessarily to be a link.

22 Q So you wouldn't collectively call
23 conductors 15, 16, and 17 between memory interface
24 chip 18 and memory controller 19 a link?

25 A Sitting here right now, I wouldn't, but

1 **if I went and perhaps looked at a dictionary or**
2 **some textbooks, I might find that appropriate.**

3 Q Is your answer the same with regard to
4 15, 16, and 17 between ECC/Parity register 21 and
5 the memory interface chip 18?

6 A **Yes, it would be the same.**

7 Q Let's turn back to the claim language of
8 claim 1 of the '623 patent. Do you see that it
9 recites a module controller?

10 A **I do see that, yes.**

11 Q On what element or elements in Hazelzet
12 are you relying to meet the claim language of a
13 module controller in claim 1 of the '623 patent?

14 A **Again, just referring to my report to**
15 **help my recollection and make sure I -- you know,**
16 **I answer as accurately as I can, in paragraph 127**
17 **the report says that Hazelzet discloses an -- and**
18 **it's in quotes here, "ECC/Parity register," which**
19 **is the claimed module controller.**

20 Q Okay. Continuing on with the claim
21 language, do you see that it recites a module
22 controller having an open drain output?

23 A **Yes, I do.**

24 Q And what element or elements of Hazelzet
25 are you relying upon to meet the claim language

1 "an open drain output" in claim 1 of the '623
2 patent?

3 THE WITNESS: Okay. Can I just hear
4 again, hear the question.

5 (Record read.)

6 A There is a signal -- I see it shown on
7 4B, figure 4B -- which is called a UE,
8 uncorrectable error. And that is the open drain
9 output that satisfies the other requirements --
10 well, it -- that I'm pointing to from the claim.

11 Q Are you relying upon the signal UE as
12 meeting the open drain output?

13 A I'm relying on that as being the parity
14 error signal that is driven by the module as an
15 open drain output.

16 Q So let me just ask the question again.
17 Are you relying on the UE signal as an open drain
18 output?

19 MR. SUH: Objection. Form.

20 A (Document review.)

21 Just looking at figure 7A, at least for
22 the example on the left, the UE output is
23 identified as being on the DIMM pin 4. So the UE
24 signal is driven by an open drain -- sorry, an
25 open drain driver from the module on, at least in

1 this example, pin 4. I don't know if all the
2 other examples line up to the same pin number.

3 Q Is there any other pin in figure 7A that
4 would output the UE signal?

5 A (Document review.)

6 It does show a pin number 142 in the
7 right-hand column as well, so either of those.

8 Q So is it your understanding that the UE
9 signal would be output onto pins in figure 7A?

10 A Yes, that's my understanding. There's
11 two signals -- two versions of that signal that
12 would be reflecting the configuration of the DIMM
13 where there were two of the buffer registers, one
14 on each side of the DIMM.

15 Q I see. So turning back to figure 2 of
16 Hazelzet, your understanding is that element 20
17 has an ECC/Parity register 21 on one side and an
18 ECC/Parity register 21 on its opposite side?

19 A (Document review.)

20 Okay. If I can hear the question again.

21 (Record read.)

22 A Okay. So it's my understanding that
23 Hazelzet discloses DIMMs that have either one or
24 two ECC/Parity register chips 21. And if I look
25 at paragraph 91, this is -- let's see where that

1 is. Well, paragraph 93 explains, it says, "A
2 two-buffer chip configuration 904 is depicted in
3 figure 9."

4 Q So is it your understanding that in that
5 configuration each ECC/Parity register would
6 utilize its own UE pin?

7 A Yes, that's my understanding. I mean,
8 specifically, I think you asked me whether -- in
9 figure 2, whether there are two buffers. I don't
10 think figure 2 gives information to indicate
11 whether there's one or two buffers on the
12 particular DIMM that's depicted there.

13 Q Okay, great. Thank you.

14 So since we are discussing the UE pin,
15 what is your understanding of UE in Hazelzet?

16 A Sorry, just going back to -- I believe
17 it was the previous question, I do see on
18 figure 9 -- I didn't see it in the text, but I do
19 see on figure 9 that when there are two buffer
20 registers, the UE outputs are tied together. You
21 can see that in the middle and the right-hand
22 figure. So I believe that's at least one
23 embodiment that's depicted by Hazelzet, and if the
24 figure 7 showed two pins carrying that, that could
25 well have been for reliability. They were

1 explanations within the spec, indicating that
2 there might be duplicate connector pins for
3 certain of the signals that could be used if one
4 trace on the edge connector had failed, for
5 example.

6 Okay. And I believe the question was
7 what's my understanding of the UE?

8 Q Yes.

9 A Well, the UE is an indication that
10 there's an uncorrectable error that has been
11 detected by the ECC/Parity register, could be
12 uncorrectable in parity mode, or it could be
13 uncorrectable in ECC mode.

14 Q When you say "the UE," are you referring
15 to the UE signal?

16 A Yes, that that's what the UE signal
17 indicates.

18 Q So there's a UE signal on a UE line?
19 Would that be fair?

20 A Yes. UE signal would be communicated
21 over a line or a trace.

22 Q Turning to figure 4B of Hazelzet, what
23 is the UE line that carries the UE signal?

24 A (Document review.)

25 Specifically, the UE line in paragraph

1 59 is identified, actually, to be an element 110
2 in figure 4B. So at least in terms of what is
3 called a UE line -- it says US there, but the
4 specification indicates that element 110 is the UE
5 line, and that's going between the SEC/DED -- SEC
6 slash DED ECC box 90 and the error logic 100 in
7 figure 4B.

8 Q So is it your understanding, as you sit
9 here today, that the UE line is line 110 in
10 figure 4B?

11 A That's what the patent refers to as the
12 UE line. In terms of -- I believe we got here
13 talking about which is the output, an open drain
14 output. And the open drain output of the module
15 controller and of the module would be the UE
16 signal that's driven on the right side by a
17 buffer 121.

18 Q So would it be fair to say that the UE
19 line in figure 4B is both line 110 and line 121?

20 MR. SUH: Objection. Form.

21 A If I referred earlier to a UE line, I
22 mean, before I pointed out what I'd read about
23 110, then in that previous context I was referring
24 to the output of buffer 121.

25 Q So I guess I want to be clear here. In

1 preparing your declaration, Exhibit 1003, what did
2 you rely upon for the UE line?

3 **A** So looking at paragraph 128, and it's
4 over to -- towards the top of page 59, it
5 indicates that the open drain outputs include the
6 uncorrectable errors UE, which is 121 in
7 figure 4B.

8 **Q** So would it be fair to say that you
9 relied upon UE line 121 in your declaration?

10 **A** Yes. Just to clarify, the 121 itself is
11 a buffer.

12 **Q** Oh, I'm sorry, yes.

13 **A** I think that's what it's pointing to,
14 the triangle shape there.

15 **Q** I guess, paragraph 59, that you were
16 referencing, refers to error lines 120 and 121.
17 So, once again, would it be fair to say that
18 you're relying on UE line 121 in your declaration?

19 **A** Yes. Line 121 --

20 **Q** Okay.

21 **A** -- is the uncorrectable error.

22 **Q** Line.

23 **A** Why is it --

24 **Q** No, it's the uncorrectable error line.

25 Correct?

1 **A Yes.**

2 Q Thank you.

3 And does uncorrectable error line 121
4 carry any address information?

5 **A It does not carry any addresses.**

6 Q Does it carry any command information?

7 **A No, it doesn't carry commands.**

8 Q And focusing on figure 4B of Hazelzet,
9 does UE line 121 go to memory cells?

10 **A I don't recall any disclosure that it**
11 **would go to the memory chips or the cells within**
12 **them.**

13 Q So would it be fair to say that UE line
14 121 doesn't carry data to memory cells?

15 MR. SUH: Objection. Form.

16 **A Yes. The UE line 121 doesn't carry data**
17 **to the -- I think you're referring probably to the**
18 **memory cells of the DRAM chips?**

19 Q That could be one, yes, but ...

20 **A And I don't see any other types of**
21 **latches or other types of memory that it carries.**

22 Q Thank you.

23 So, Dr. Alpert, what's an uncorrectable
24 error?

25 MR. SUH: Objection to form.

1 **A** Well, generally, errors that occur and
2 are detected can fall into either of two
3 categories. One is that the errors can be
4 corrected, and the second category is errors that
5 cannot be corrected.

6 **Q** And is that understanding of
7 uncorrectable error that you testified about --
8 strike that.

9 Is your definition of uncorrectable
10 error consistent with Hazelzet's discussion of
11 uncorrectable error?

12 **A** Yes, it is.

13 **Q** So how do uncorrectable errors arise in
14 the operation of a memory module?

15 MR. SUH: Objection to form.

16 **A** Is your question specifically focused on
17 Hazelzet, or is it broader?

18 **Q** Let's start broad, and then we can focus
19 on Hazelzet.

20 So how do uncorrectable errors arise in
21 the operation of memory modules?

22 **A** Well, there are various choices for the
23 type of circuitry and functions that can be used
24 for detecting and correcting errors. So I don't
25 know if you -- maybe you can ask a little more

1 specific question.

2 Q I'm just -- I'm just -- I would like to
3 get your understanding of how uncorrectable errors
4 arise in the operation of memory modules.

5 A Okay. Well, let me just give an
6 example. One that's sometimes used is that the
7 information, whether it be data or address and
8 commands, can be augmented with some additional
9 bits, sometimes called check bits. And there are
10 certain types of coding where that redundant
11 information can be used to determine whether an
12 error has occurred. And there are -- within that
13 class of coding, sometimes called hamming codes,
14 H-A-M-M-I-N-G, there are certain types of codes
15 where there's sufficient redundant information
16 that in the presence of an error, the correct
17 information can be recovered.

18 So, for example, in Hazelzet it shows a
19 block that's called a SEC/DED, and that would
20 indicate to a person of ordinary skill in the art
21 that it's using a code that's capable of
22 correcting single errors -- all single errors and
23 detecting all double errors.

24 Q Well, I guess my question is directed to
25 how do these errors arise that you would need

1 circuitry like 90 to address them?

2 A Well, some errors can occur as a result
3 of cosmic rays, particularly a concern for, say,
4 financial servers that might be located at high
5 altitudes. I know people go to Denver to conduct
6 a lot of experiments for that purpose. So that's
7 one example of what could cause an error to occur
8 in a bit of a memory chip.

9 Q So is the error that occurs related to
10 the transmission of address or command signals
11 from the memory controller to the memory module?

12 A No. That example I gave would be
13 related to changing the state of the DRAM cell
14 within the chip, the data value within the DRAM
15 cell.

16 Q Oh, the cosmic rays would specifically
17 impact the memory cell itself?

18 A Yes. That's at least the mode of
19 failure I'm familiar with. They're quite powerful
20 events. I would expect it's possible that it
21 could cause other types of failures, like you say,
22 address. But, of course, there's -- so much more
23 of the silicon area is devoted to the memory cells
24 that it's more likely to -- that a cosmic ray
25 would strike the cell array rather than some of

1 the peripheral circuitry.

2 Q I see.

3 So is your understanding of Hazelzet
4 that it's directed to addressing errors associated
5 with cosmic rays impacting the memory cells of the
6 DRAMs?

7 MR. SUH: Objection. Mischaracterizes
8 testimony.

9 A No. Hazelzet -- what's described in
10 Hazelzet is focused on the address and command
11 signals.

12 Q And so what -- strike that.

13 So how do the errors -- strike that.

14 How do uncorrectable errors arise with
15 respect to address and command signals?

16 A Well, errors in general -- I mean, the
17 question of whether they're correctable or not
18 depends on the number of them and the type of
19 coding scheme.

20 Q Right.

21 A Errors in general can occur from some
22 disturbance in the power, for example. Could be
23 the result of the temperature changing and
24 affecting the operation of the driving and
25 receiving circuitry. Voltage, temperature would

1 be a couple of examples that would commonly be
2 understood to occur in practice.

3 Q Are there any other examples beyond
4 voltage and temperature that you can think of as
5 you sit here today?

6 A Well, at any given time there could be
7 some noise in the system, maybe something that
8 would occur only rarely that could induce an error
9 that was uncorrectable. I say rarely because if
10 it were something systematic, it would -- you
11 know, it would be expect- -- it should show up in
12 testing. I mean, the testing should be thorough
13 enough to find anything that might be systematic.

14 Q Okay. So would it be fair to say that
15 Hazelzet is concerned with errors associated with
16 address and command signals arising from voltage
17 or temperature issues?

18 A Yes. I don't think it's limited to
19 that, but those would definitely be known
20 concerns.

21 Q Well, what other concerns do you think
22 Hazelzet is directed to with regard to errors that
23 arise from command and address signals?

24 A I think I just mentioned there could be
25 some noise that would affect the quality of the

1 **signals on the lines. There could also be a**
2 **failure of either the driver or receiver of the**
3 **signals.**

4 Q Anything else, as you sit here today?

5 A **Those are examples that come to my mind**
6 **that would have to be dealt with.**

7 Q And so are all those examples associated
8 with -- strike that.

9 Are all those examples -- strike that.

10 Do all those examples arise from the
11 communication between the memory controller and
12 the memory module -- well, let me -- maybe I can
13 ask that question more specifically.

14 So is Hazelzet concerned with, in your
15 opinion, errors that arise from transmitting
16 address and command signals between the memory
17 controller and the memory module due to
18 temperature, voltage, noise, and the other
19 examples that you referred to?

20 A **Yes. I believe what Hazelzet is**
21 **disclosing as being the novel part of the**
22 **invention is ways of protecting the address and**
23 **command. I think it's understood -- it might be**
24 **expressly in there, but I think it's understood**
25 **that the data would be protected as well. Just**

1 **that's been an issue that's been longer solved**
2 **than practiced.**

3 Q Let me direct you to figure 4A of
4 Hazelzet. Actually, let me direct you to both
5 figures 4A and 4B. You understand that figures 4A
6 and 4B are showing the ECC/Parity register 21 in
7 figure 2. Is that correct?

8 A **Yes, I was just checking, but it does**
9 **say -- paragraph 27 says it's a schematic view of**
10 **the ECC/Parity register.**

11 Q Great.

12 So, is it your understanding that the
13 ECC/Parity register 21 can operate in two modes?

14 A **I would say at least two modes, but**
15 **thinking specifically of a parity mode and an ECC**
16 **mode.**

17 Q When the ECC/Parity register 21 is
18 operating in the parity mode, what is it doing?

19 MR. SUH: Object to form.

20 A **Generally, it would be receiving address**
21 **and commands. Those would be identified as the**
22 **32A through 32N on the left side, and it would**
23 **receive a single bit of parity, which would be**
24 **shown as 31 on the left side. And that**
25 **information would be from the address and**

1 commands. The element 21 would generate a parity
2 based on what it received, compare that -- the
3 parity generated to the parity received, and if
4 they don't match, it will recognize -- it will
5 detect a parity error that will be signaled on the
6 UE, line 121.

7 Q So at the start of your answer, you
8 referred to lines 32A through 32N. Do you see
9 that?

10 A Yes.

11 Q So those are the address and command
12 signals -- strike that.

13 So those are the lines that receive the
14 address and command signals?

15 A (Document review.)

16 If I can hear that question again?

17 Q Let me just ask it again.

18 A Okay, sure.

19 Q Do lines 32A through 32N in figure 4A of
20 Hazelzet receive the address and command signals
21 from the memory controller?

22 A It's my understanding that they do. I
23 was trying to find a specific disclosure of that,
24 which, unfortunately, just looking by eye on the
25 fly I couldn't find that.

1 Q And is it your understanding that the
2 memory module in Hazelzet, figure 2, is operating
3 under a JEDEC standard?

4 MR. SUH: Objection. Calls for
5 speculation.

6 Q Let me see if I can ask the question in
7 a slightly different way.

8 What I'm trying to get at is, is it your
9 understanding that the address and command signals
10 that are received on lines 32A through 32N appear
11 regularly at every clock cycle during the
12 operation of the memory module?

13 MR. SUH: Objection to form.

14 A **Well, the address and command would have**
15 **a valid content in conjunction with a chip select,**
16 **for example. So it might not be on every clock**
17 **that the contents would have -- be valid or have a**
18 **meaning.**

19 Q Right. If the chip select, for example,
20 is 1, and let's say 1 is not active, you're saying
21 that the address and command signals would not
22 have meaning in that -- in that command.

23 A **Yes, that's correct.**

24 Q Is that your understanding?

25 But assuming that the chip select is

1 active low, would the signal lines 32A through
2 32N -- well, strike that.

3 Assuming that the memory module is
4 receiving active low chip selects, would data
5 lines 32A through 32N be receiving at every clock
6 cycle address and command signals that are valid?

7 **A They could be.**

8 Q When you say "they could be," why do you
9 say "they could be"?

10 **A Well, they could be a NOP, I think, is a**
11 **command, for example.**

12 Q Understood.

13 MR. ARJOMAND: Okay. Let's take a
14 break.

15 (A lunch recess was taken.)

16 BY MR. ARJOMAND:

17 Q Dr. Alpert, during the lunch break did
18 you discuss the substance of your testimony with
19 counsel here?

20 **A No, I don't.**

21 Q Thank you.

22 So, Dr. Alpert, let's turn back to
23 Hazelzet figures 4A and 4B. Do you have them in
24 front of you?

25 **A I do now, yes.**

1 Q Okay, great. Thank you.

2 So prior to the lunch break we were
3 discussing the parity mode. Is there another mode
4 that the ECC/Parity register 21 can enter into?

5 A Yes, there is.

6 Q What mode is?

7 A It's called ECC mode.

8 Q How does the ECC/Parity register 21 --
9 strike that.

10 How is -- how does the memory module
11 decide between the parity mode and the ECC mode?

12 A There's an input signal that would
13 select between -- I believe that's shown at the
14 bottom of figure 4B. It's labeled 123.

15 Q And what is the input to that signal
16 123, or that line, I should say, 123.

17 A If we refer to figure 7A again, there is
18 a pin on the module connector -- in this case pin
19 number 7, for example -- indicates ECC mode.

20 Q Does a human program the memory
21 controller to issue a signal that is asserted on
22 that pin to put the memory module into the ECC
23 mode in Hazelzet?

24 MR. SUH: Objection. Calls for
25 speculation.

1 A The patent does indicate that the mode
2 is programmable and explains that a different
3 app- -- applications could run in different modes,
4 but I don't recall that it said anything
5 specifically about a human being making that
6 decision.

7 Q But typically you would understand that
8 if something is programmable, then that could be
9 programmed by a human. Right?

10 A Yeah, I don't know if typically, but
11 that would be certainly one way of programming a
12 value that comes to mind.

13 Q So you would understand, by Hazelzet's
14 reference to programmability, that a person would
15 be able to set the memory module to operate in the
16 ECC mode or the parity mode?

17 A (Document review.)

18 I was looking for something I didn't
19 find immediately, but I generally recall that the
20 disclosure of Hazelzet indicates that certain
21 modules might, for example, be operated in only
22 one mode or the other. But, generally, the
23 disclosure does indicate that a mode can be -- you
24 know, for at least certain modules, that mode can
25 be programmed between ECC mode or parity mode.

1 Q And why is there an option to have both
2 modes for a memory module in Hazelzet?

3 A (Document review.)

4 Sorry, what I was looking for before at
5 paragraph 38, I did just find at the bottom left
6 of page 3. It does indicate, it says, "It should
7 be understood that the chip 21 need not include
8 both the ECC function and the parity function."

9 Q And so, just following up on my previous
10 question, why is there an option for a memory
11 module in Hazelzet to have both modes?

12 A (Document review.)

13 Well, again, without my going back and
14 reading the whole patent, I do recall that
15 Hazelzet indicates that there can be a trade-off
16 between the reliability of the coverage for errors
17 versus the performance, and the ECC mode would
18 give a better coverage for errors and the parity
19 could give better performance.

20 Q And how would the parity give better
21 performance?

22 A The parity mode does not provide the
23 capability of correcting errors, and so the memory
24 accesses proceed, and if there is an error that's
25 found, it's reported later, after the error might

1 **have had an effect on the system, but there was**
2 **basically no delays associated with the error**
3 **detection for parity.**

4 Q I see.

5 But there would be delays associated
6 with error correction in the ECC mode. Is that
7 correct?

8 A **There can be, particularly when an error**
9 **is detected and something may be -- an access may**
10 **be retried.**

11 Q Okay. Would you understand that in the
12 situation where a memory module has the option of
13 both being in the parity mode and the ECC mode
14 that it would be able to switch between those two
15 modes depending on the circumstances?

16 A **Yes, I believe that's possible.**

17 Q And so what would be the circumstances
18 that would arise for it to switch between one mode
19 to another mode?

20 MR. SUH: Objection. Calls for
21 speculation.

22 A **(Document review.)**

23 Well, I found one example of what I was
24 looking for. As I recall, there were several
25 statements like this. It's in paragraph 81. In

1 the last kind of phrase in the paragraph,
2 indicates that the "chip 21 will report
3 information indicating whether ECC has been
4 bypassed by the application or not," which I
5 believe is an indication that certain applications
6 running on the system may use the ECC mode and
7 certain may use the parity mode.

8 Q I see.

9 So your understanding is that when a
10 certain application is being run, the memory
11 controller would inform the memory module to be in
12 the ECC mode or in the parity mode?

13 A I believe that's consistent with the
14 disclosures here, yes.

15 Q And that may -- and the application --
16 strike that.

17 The memory controller may make that
18 decision based on the trade-off between coverage
19 for errors and performance for a given
20 application. Is that correct?

21 A Yes, that would be the trade-off.
22 Whether it's done by the memory controller or, for
23 example, the application developer or the OS
24 vendor, I don't believe it provides any guidance
25 on that, "it" meaning Hazelzet.

1 Q Since we're at paragraph 81 of Hazelzet,
2 let me ask you, at the start of that paragraph, it
3 refers to the "status register block, including
4 ten 8-bit register sets which contain informations
5 on the data input signals," and so forth.

6 What is that referring to?

7 A Well, there's various tables that follow
8 that paragraph -- I think they're on the next
9 couple pages -- that show the formats for
10 information that would be reported, indicating, I
11 guess, from byte zero up through byte 9 following
12 paragraph 89. So that would be -- I believe it
13 says "8-bit register sets." So I -- I understand
14 it's referring to the registers that are described
15 bit by bit in those tables.

16 Q Would that 8-bit reporting be done on
17 the UE line 121?

18 A So let me just ask, when you're saying
19 the "reporting," are you asking whether the
20 information that's shown in those tables can be
21 accessed using the UE line?

22 Q Well, if I understood your previous
23 answer correctly, is that 8 bits of information
24 are being provided, and those 8 bits provide
25 information as set forth in the tables on page 9

1 of Hazelzet. Is that correct?

2 A Yes, there's ten 8-bit registers, and
3 those are covered on pages 9 and 10.

4 Q Thank you for that clarification.

5 What I was trying to understand was
6 whether those 8- -- those ten 8-bit registers or
7 those ten 8 bits of information are expressed on
8 the UE line 121.

9 A Yeah, I don't see a disclosure that the
10 information of those registers can be accessed
11 through the UE line.

12 Q Turning back to figure 4B, is it your
13 understanding that the information on those
14 registers can be accessed through the I2C bus 122?

15 A Yes, that's my understanding. I mean, I
16 could look through here to find it in more detail,
17 but it's my understanding that's the way that
18 error information would be obtained, is with
19 the -- yes, the I2C bus.

20 Q So what is the difference between the UE
21 line 121 and the I2C bus 122 in figure 4B of
22 Hazelzet?

23 A Well, the UE line would indicate the
24 occurrence of an error associated with a memory
25 access, would indicate that back to the memory

1 controller. And the I2C bus is a serial bus that
2 can be accessed by either the central processor or
3 another kind of service or maintenance processor
4 in the system.

5 Q So when you say it's a serial bus, what
6 do you mean by that? Let me ask it more
7 carefully. When you say that the I2C bus 122 is a
8 serial bus, what do you mean by that?

9 A It has a -- I believe it's a clock and a
10 single data line -- I don't know if it has another
11 signal -- that's used to communicate information
12 between some type of a controller or master and
13 other devices that are connected to that serial
14 line. It's been around since about the 1980s.
15 Philips developed.

16 Q And is there a pin in figure 7A where
17 that information is output to?

18 A Based on my recollection of the bus --
19 I'm looking at figure 9, and there are some
20 signals labeled "SCL" and "SDA," which, to the
21 best of my recollection, are the signal names
22 associated with the clock and data line for the
23 I2C. Again, just looking at figure 7A, those are
24 the signal names associated with pins 2 and 3.

25 Q So is there a design reason for Hazelzet

1 to have an error bus 122 in figure 4B?

2 A Well, I believe a person of ordinary
3 skill in the art would understand it to be useful
4 to have access to the error information and
5 particularly to do it over a standard low-cost
6 serial bus like the I2C.

7 Q When you just testified that "a person
8 of ordinary skill in the art would understand it
9 to be useful to have access to error information,"
10 what do you mean by that?

11 A Well, as I recall, we've seen that there
12 are the ten 8-bit registers. As I recall, there's
13 multiple sets of those for storing the error
14 information associated with multiple errors.
15 There's also a counter that indicates the number
16 of errors that have occurred.

17 Q Just for my understanding, would this
18 register information that you're referring to be
19 asserted on the error bus 122 during either the
20 ECC mode or the parity mode?

21 A Well, it would be asserted on that bus
22 in response to a request from a bus master like a
23 service processor, and at that path, the I2C bus
24 could be used to access the error register
25 information in either mode, either parity or ECC

1 **mode.**

2 Q So in the case of a parity error when
3 the memory module of Hazelzet is in the parity
4 mode, what does line 121 provide and what does
5 error bus 122 provide in terms of information?

6 MR. SUH: Objection.

7 A Line 121, the UE line, provides an
8 indication of whether a parity error was detected.
9 In the parity mode all the parity errors would be
10 uncorrectable, so that would be the one line that
11 was used to report those errors.

12 And the error bus I2C bus would be used
13 to access information that's stored about the
14 error condition, such as shown in the registers
15 that we talked about previously.

16 Q So let me ask you that question in the
17 context of the ECC mode. So specifically in the
18 case of an uncorrectable error in the ECC mode,
19 what does line 121 provide and what does error bus
20 122 provide in terms of information?

21 A You know, I think my answer would be --
22 would be very similar. In the ECC mode, line 121,
23 the UE line provides an indication of whether the
24 memory access had an uncorrectable error that was
25 detected, and, similarly, the I2C bus could be

1 used by a master on that bus, such as a service
2 processor, to access the information that's stored
3 in those ten registers.

4 Q So stepping back and looking at figures
5 4A and 4B of Hazelzet, would it be fair to say
6 that in the parity mode, what drives whether there
7 is a signal on the UE line are the inputs 32A
8 through 32N and check bit 025?

9 MR. SUH: Objection to form.

10 A I don't think I see the latter check
11 bit.

12 Q Maybe I -- I may have gotten it ...

13 A (Document review.)

14 Q Well, let me ask you more broadly. What
15 do you think are the critical inputs in figures 4A
16 and 4B for having a signal be expressed on the UE
17 line 121 in the parity mode?

18 MR. SUH: Objection to the form.

19 A Yes, generally, in the parity mode, what
20 happens is that the signals received on 32A
21 through 32N are examined by -- I believe it's by
22 the so-called SEC/DED ECC block 90, which will
23 generate a signal indicating the parity of those
24 bits, and that generated parity will be compared
25 with the parity in, which is shown as 31 on the

1 left side of figure 4A. And if there's a mismatch
2 between the received parity and the generated
3 parity, then an uncorrectable error will be
4 signaled on line 121.

5 Q And in the ECC mode, what are the key
6 inputs for whether a signal is expressed on UE
7 line 121?

8 MR. SUH: Objection to form.

9 A So in the ECC mode, the signals
10 corresponding to the inputs 32A through 32N and,
11 it looks like, six check bits, 30A through 30E and
12 31, are considered to determine whether there's an
13 uncorrectable error, and if there is an
14 uncorrectable error, then that's indicated on line
15 121.

16 Q Thank you.

17 We've been referring to ECC. What is
18 your understanding of what ECC means?

19 A ECC stands for an error correcting code
20 or error correction code.

21 Q What does that mean to you, error
22 correction code?

23 A Well, generally, as we talked about
24 earlier, there are various ways of storing
25 redundant information with some data that's being

1 transmitted and to allow the extra redundant
2 information to be used in such a way that if one
3 or more errors occur in the information being
4 stored or communicated, that the correct value can
5 be recovered.

6 Q Let me direct you to figure 8 of
7 Hazelzet. Can you explain to me the top diagram
8 that's referred to as the ECC mode?

9 MR. SUH: Objection to form.

10 Q Let me address the objection.

11 So you are looking at figure 8.

12 Correct, Dr. Alpert?

13 A Yes, I am.

14 Q Would you say that it shows two timing
15 diagrams?

16 A Yes, that's what it's showing. Yes.

17 Q One timing diagram refers to the ECC
18 mode. Is that correct?

19 A Yes.

20 Q And another timing diagram refers to the
21 parity mode?

22 A Yes. The lower one is indicated as
23 parity mode.

24 Q So could you walk through the top timing
25 diagram, referred to as the ECC mode, for me.

1 A So in the ECC mode, we can see on the
2 left side, that on the clock edge between zero and
3 1, data in check bits are valid.

4 Q So just to stop you there, data in would
5 be the data that's going into lines 32A through
6 32N in figure 4A of Hazelzet?

7 MR. SUH: Objection. Calls for
8 speculation.

9 A Yes, that's what I believe it
10 represents.

11 Q Okay.

12 A And the check bits, so those are valid
13 on the clock edge shown between zero and 1.

14 Q Just to stop you there, so those check
15 bits would be the inputs that are coming in lines
16 30A through 30E and line 31?

17 A Yes, those are the check bits from
18 figure 4A.

19 Q Yes. Thank you.

20 A Okay.

21 And then at the clock boundary between 2
22 and 3, the data that's coming out, what's called
23 data out, is shown to be valid, meaning that it
24 would have been corrected if that were necessary
25 and possible, and also that the signals CE and UE

1 are also valid and remain so for two clocks.

2 Q So when you say that "the signals CE and
3 UE are valid," what do you mean by that?

4 A Well, the timing diagram indicates that
5 they are valid, and so they would, therefore, take
6 on a value of either -- representing either a zero
7 or 1 that corresponded to whether the information
8 that was received had an error that was corrected
9 or had an error that could not be corrected.

10 Q I see.

11 So it appears that there are two clock
12 cycles or so between the validity of the data in
13 and the check bits and the validity of the CE and
14 UE lines. Is that correct?

15 A Yes. That's what this diagram is
16 showing.

17 Q And is the reason for those two clock
18 cycles, is that element 90 in figure 4B of
19 Hazelzet has to do the mathematical operations to
20 determine whether there's a correctable error or
21 an uncorrectable error based on the data in and
22 the check bits that are received?

23 A Just based on my general knowledge and,
24 I believe, a person ordinary skill in the art
25 would understand that would be the primary source

1 **of delay.**

2 Q Do you know why the CE and UE lines are
3 valid across two cycles in figure 8 of Hazelzet?

4 MR. SUH: Objection. Relevance.

5 **A I don't recall why that is.**

6 Q All right. So now turning to the second
7 timing diagram in figure 8, which applies to the
8 parity mode, could you walk through that timing
9 diagram with me.

10 **A Okay. In the parity mode we can see**
11 **that the data in is valid at the same**
12 **corresponding time between clock zero -- the**
13 **clocks labeled zero and 1. The check information,**
14 **particularly the single bit of parity, is valid a**
15 **clock later, between clocks 1 and 2.**

16 Q So just to stop you there, the data in
17 in figure 8 would correspond to the data that's on
18 lines 32A through 32N in figure 4A of Hazelzet?

19 **A Yes, that's right.**

20 Q And the parity in in figure 8 of
21 Hazelzet would correspond to the parity signal
22 that's on line 31 in figure 4A of Hazelzet?

23 **A Yes, it's 31.**

24 Q And in the case of the ECC mode, the
25 data in and the check bits are valid in the same

1 clock cycle, but in the parity mode it appears
2 that the data in and the parity in are not valid
3 in the same clock cycle. Why is that?

4 A Generally, I would understand and I
5 believe a person of ordinary skill in the art
6 would understand, both from the disclosure here
7 and general knowledge, that for the ECC mode, the
8 memory controller would take the time to generate
9 the check bits before sending the data so they
10 would be sent at the same time and that the buffer
11 chip or whatever it is called, the 21, the
12 register chip 21, would have the information
13 necessary to determine whether a -- particularly
14 whether a correctable error had occurred.

15 In contrast, for the parity mode, what's
16 indicated is that the data is sent over to -- from
17 the memory controller over to the chip 21, and
18 then, in parallel with that, the memory controller
19 would be calculating the parity bit, which it
20 would then send a clock later. So that would be
21 part of the performance advantage associated with
22 parity mode.

23 Q Okay. So continuing on in the timing
24 diagram related to the parity mode, and you
25 discussed the data out and the UE line?

1 A Okay. So in parity mode the data out
2 would be valid between clock 1 and 2. So there
3 would not be any -- in this mode there would not
4 be any change or correction to the data so it
5 would be available sooner than in the ECC mode.
6 And then it looks like between clock 4 and 5 the
7 uncorrectable error signal would be valid,
8 indicating whether or not uncorrectable error,
9 basically, any parity, was detected.

10 Q And would it be fair to say that the
11 time between the parity in being valid and the UE
12 line being valid is about two clock cycles?

13 A As I'm looking at it, it looks like it
14 would be three clock cycles. I think the parity
15 in would be valid between clocks 1 and 2, and the
16 UE would be valid between clocks 4 and 5.

17 Q Okay. What is the reason for three
18 clock cycles being needed for the UE line to be
19 valid after the parity in line is valid?

20 MR. SUH: Objection. Relevance.

21 A I'm not sure that I understand.

22 Q Let me ask the question again.

23 Is the sort of the delay between the
24 parity in being valid and the UE line being valid
25 due to the mathematical operations that element 90

1 in figure 4B of Hazelzet has to perform?

2 MR. SUH: Same objection. I'll just
3 object to this line of questioning so that I don't
4 keep constantly objecting.

5 MR. ARJOMAND: Okay.

6 MR. SUH: And the basis is relevance.

7 MR. ARJOMAND: Okay.

8 A So there would be a delay for the parity
9 generation and checking by the block 90 that would
10 be in the timing path for generating the UE signal
11 121.

12 Q Okay. Thank you.

13 So stepping back and looking at both
14 timing diagrams for figure 8, so is it your
15 understanding that each time there is a data
16 transmission between the memory controller and the
17 memory module, whether the memory module is in the
18 ECC mode or the parity mode, the ECC/Parity
19 register bit performs the operations that are
20 shown in figure 8?

21 A I think you might have said "the
22 ECC/Parity bit performs"? I'm not sure if that's
23 what you meant to ask.

24 Q Let me -- maybe I mis- -- not bit. I
25 meant register. But let me ask the question

1 again.

2 So stepping back and looking at both
3 timing diagrams for figure 8, is it your
4 understanding that each time there's a data
5 transmission between the memory controller and the
6 memory module, whether the memory module is in ECC
7 mode or the parity mode, the ECC/Parity register
8 21 performs the operations that are shown in
9 figure 8?

10 A (Document review.)

11 Well, I found what I was looking for in
12 paragraph 75 so let me just summarize it. I don't
13 know how necessarily it relates in all aspects to
14 what you're asking, but paragraph 75 indicates
15 that there's an ECC mode, and I think it's the
16 second sentence that says, "As such, two
17 additional modes are included on the module that
18 permit the system user to trade off performance
19 and reliability." And then it talks about in
20 parity mode. So we've talked about both ECC mode
21 and parity mode with respect to figure 8.

22 And then at the bottom of that
23 paragraph, it indicates that potentially there
24 could be a third mode. The last mode would be to
25 simply operate the memory in a mode with no parity

1 bits and no ECC bits with neither the added delay
2 due to ECC nor any means to detect a fault on the
3 address command buses.

4 So in that regard, I believe that the
5 disclosure for Hazelzet is indicating that there
6 could be circumstances under which there would be
7 no parity, no parity or ECC checking performed.

8 Q Okay. But when we look at figure 8,
9 we're talking about the ECC mode and the parity
10 mode. Correct?

11 A Yes, that's what's shown in figure 8.

12 Q So let's just focus on the ECC mode for
13 a second here.

14 So is it your understanding that for
15 every data transfer from the memory controller to
16 the memory module, the ECC/Parity register
17 performs the operations that are shown in the top
18 timing diagram of figure 8?

19 MR. SUH: Objection. Form. Calls for
20 speculation.

21 A I don't recall any disclosure that would
22 indicate times that it was not performed.

23 Q So does that mean that you agree with
24 the question that I just answered? I'm sorry, so
25 does that mean that you agree with my question?

1 A No. I'm just saying that I know it's
2 sometimes performed. I don't recall whether it's
3 performed every time.

4 Q Okay. So as you sit here, you think
5 that there's a situation in Hazelzet during the
6 ECC mode where the data in and the check bits that
7 are received are not crunched by element 90 to
8 determine whether there should be a signal on the
9 CE or UE line?

10 A Well, as I recall, Hazelzet does talk
11 about needing the presence of a chip select, and
12 there's also this CS gate enable for the power
13 savings. So I believe there's some combination of
14 those inputs that would be required for the --
15 this whatever it is, chip 21, to respond to the
16 inputs in performing the checking calculations.

17 Q But assuming that the chip selects are
18 at a value that allows for the data in and the
19 check bits to be received and processed by the
20 ECC/Parity register 21, would it be your
21 understanding that in that situation, the element
22 90 would perform its mathematical analysis to
23 determine whether to express a signal on the CE or
24 UE line as shown in the timing diagram of
25 figure 8?

1 MR. SUH: Objection to form. Relevance.
2 Incomplete hypothetical.

3 A I would say yes, it's generally my
4 understanding that that function unit 90 would be
5 operating in the way that your question reflected.

6 Q In other words, that for each data
7 transfer coming in, it would -- "it" being element
8 90 -- would be operating to determine whether
9 there should be a signal on the CE or UE line in
10 the ECC mode?

11 MR. SUH: Same objection.

12 A I would say, yes, you know, as I'm
13 sitting here now, without going and reading all
14 the disclosures. Again, that's my understanding
15 sitting here now of what Hazelzet describes.

16 Q All right. Let me just turn quickly
17 back to figure 4B of Hazelzet.

18 So let me direct you to line 121 in
19 figure 4B. Could you explain to me what
20 information that line provides to the memory
21 controller in the ECC mode?

22 A In the ECC mode, line 121 indicates that
23 an error was detected that could not be corrected.
24 For example, if there are two errors, there's
25 indication that the algorithm that's used is

1 called a single-error correcting double-error
2 detecting. So the detection would indicate that
3 there were, say, two or more errors that were
4 detected and could not be corrected.

5 Q Would you characterize that information
6 provided by line 121 to the memory controller as
7 status information?

8 A I would say generally that I think a
9 person of ordinary skill in the art would consider
10 the error reporting information on 121 to be a
11 status.

12 Q Let me direct you back to the claim
13 language where we started this line of inquiry,
14 specifically claim 1 of the '623 patent. Can you
15 let me know what element or elements you're
16 relying upon to meet the claim limitation "first
17 mode" in claim 1 of the '623 patent?

18 A So in the declaration -- in my
19 declaration at paragraph 130, it indicates that
20 the claimed first mode is Hazelzet's parity mode.

21 Q Now turning to the claim element "parity
22 error" in claim 1 of the '623 patent, what element
23 or elements of Hazelzet are you relying upon to
24 meet that claim term?

25 A You're asking parity error signal?

1 Q Just parity error, I believe.

2 A Oh, it says -- the claim says, "the
3 parity error signal indicating a parity error" --

4 Q Correct.

5 A -- "having occurred in the memory
6 module"?

7 Q Yes. Not the signal, the parity error.

8 A So a parity error would be detected by
9 the block 90 when it generates a parity that does
10 not match the parity received from the memory
11 controller and then indicates that on line 111. I
12 believe that's also shown at the bottom of --
13 figure 5 separates out the parity generation and
14 checking path from the error correction path.

15 Q Thank you.

16 MR. ARJOMAND: We've been going for
17 about an hour, so it's a good time for a break.

18 THE WITNESS: Sure.

19 MR. ARJOMAND: Let's go off the record.

20 (A brief recess was taken.)

21 BY MR. ARJOMAND:

22 Q So before the break, Dr. Alpert, we were
23 talking about the claim elements of claim 1 of the
24 '623 patent and how they map to Hazelzet in your
25 view. So continuing with that, do you see the

1 term "second mode" in claim 1 of the '623 patent?

2 **A Yes.**

3 Q What element or elements are you relying
4 upon in Hazelzet for meeting that claim term?

5 **A Again, pointing to paragraph 130 in my**
6 **declaration, it says there that the second mode is**
7 **the ECC mode.**

8 Q Okay.

9 Now turning to the claim term
10 "notification signal" in claim 1 of the '623
11 patent, what element or elements of Hazelzet are
12 you relying upon to meet that claim term?

13 **A (Document review.)**

14 **So the notification signal is the signal**
15 **UE on line 121.**

16 Q And in what mode or modes would that be
17 in? Let me ask it better.

18 You're relying on the signal UE line --
19 strike that.

20 You're relying on the signal on UE line
21 121 of Hazelzet for meeting the notification
22 signal. And what mode or modes of Hazelzet are
23 you relying on for that analysis?

24 **A Well, the claim language, as I'm looking**
25 **at it, column 15, starting at line 39, says, "The**

1 **module controller generating a notification signal**
2 **indicating at least one status of one or more**
3 **training sequences while the memory module is in**
4 **the second mode." So the notification signal**
5 **would be in the second mode or the ECC mode.**

6 Q So your understanding of the
7 notification signal of claim 1 of the '623 patent
8 being met by the signal on UE line 121 in the ECC
9 mode? Is that correct?

10 A **Yes, UE line in the ECC mode.**

11 Q Okay. So continuing with the claim
12 language of claim 1 of the '623 patent, what
13 element or elements are you relying upon in
14 Hazelzet for meeting the claim language "status of
15 one or more training sequences"?

16 THE WITNESS: Can I just hear that one
17 back again.

18 (Record read.)

19 A **So the status would be the indication on**
20 **line 121 of whether an uncorrectable error**
21 **occurred. And a training sequence for Hazelzet**
22 **would be the sequence of retrying memory accesses**
23 **in the ECC mode.**

24 Q What do you mean by "retrying memory
25 accesses in the ECC mode"?

1 **A** (Document review.)

2 **Q** Dr. Alpert, let me see if I can shortcut
3 this.

4 **A** **Sure.**

5 **Q** So as we've been going through the claim
6 elements, you've been looking to paragraphs in
7 your declaration to see how the claim element is
8 mapped to Hazelzet. Is that correct?

9 **A** **Yes.**

10 **Q** So with regard to the term "status of
11 one or more training sequences," I believe it was
12 addressed with respect to Hazelzet in paragraph
13 148 of your declaration. Is that correct?

14 **A** (Document review.)

15 **Yes, that's an explanation of**
16 **notification signal indicating status.**

17 **Q** And so can you explain to me, based on
18 paragraph 148 of your declaration, how you believe
19 Hazelzet discloses a notification signal
20 indicating the status of one or more training
21 sequences?

22 **A** Well, the UE signal is a notification
23 signal indicating status of whether an error --
24 uncorrectable error was detected for memory
25 access, and I believe, looking at paragraphs 150

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1 and 151, that a person of ordinary skill in the
2 art would find it obvious from Hazelzet to use the
3 error correction mode as a -- recognize that it is
4 a training sequence.

5 Q So would it be fair to say, based on
6 your previous answer, that you do not believe
7 Hazelzet expressly discloses a signal that
8 indicates the status of one or more training
9 sequences?

10 MR. SUH: Objection. Mischaracterizes
11 testimony.

12 A So what I would say is it does disclose
13 the status of one or more training sequences. To
14 the extent that it doesn't, then Hazelzet as a
15 single reference makes obvious the status of the
16 training sequence.

17 Q So in the case of Hazelzet disclosing
18 the status -- strike that.

19 In the case of Hazelzet disclosing a
20 signal that indicates the status of one or more
21 training sequences, are you relying upon the
22 uncorrectable error as being the training
23 sequence?

24 A I'm regarding the accesses in the ECC
25 mode as being a training sequence. The status

1 **would be whether or not there was an uncorrectable**
2 **error.**

3 Q So, just so that I understand, in your
4 view Hazelzet discloses a information signal,
5 which is the signal on the UE line during an ECC
6 mode. Correct?

7 A **That's correct, yes.**

8 Q And the claim further says that the
9 notification signal indicates a status of one or
10 more training sequences. Correct?

11 A **Yes, that's what the claim says.**

12 Q And so for that, are you relying on the
13 signal that's on the UE line 121 during the ECC
14 mode?

15 A **Yes.**

16 Q How does that signal on the UE line 121
17 during the ECC mode indicate a status of one or
18 more training sequences?

19 A **It indicates whether particular memory**
20 **access, of which there would be a sequence of**
21 **accesses, would have -- would or would not have an**
22 **uncorrectable error.**

23 Q So is it your view that a sequence of
24 memory access is equivalent to a training
25 sequence?

1 MR. SUH: Objection. Mischaracterizes
2 testimony.

3 A In the ECC mode, yes, I believe a person
4 of ordinary skill in the art would understand that
5 to be a training sequence.

6 Q So if I am to understand your position,
7 in Hazelzet figures 4A and 4B, we talked about how
8 there was an input of signals onto lines 30A
9 through N. Correct?

10 A Yes.

11 Q And those signals could be address and
12 command signals associated with a memory access.
13 Correct?

14 A Yes, there were would be address and
15 command signals.

16 Q We discussed that in figures 4A and 4B,
17 those signals, the address and command signals,
18 combined with the check bits in the ECC mode would
19 be crunched by element 90 to determine whether
20 there's a correctable or uncorrectable error.
21 Correct?

22 A Yes, that's shown in -- what's shown in
23 figures 4A and 4B.

24 Q And if there's an uncorrectable error,
25 then there's a signal that's placed on line 121 in

1 figure 4B of Hazelzet?

2 **A Yes, 121 is for uncorrectable errors.**

3 Q So is it your view that the fact that
4 the memory access, based on the input address and
5 command signals has an uncorrectable error, is a
6 sequence of training?

7 **A What I would say, the sequence would be**
8 **a sequence of memory addresses, and when an error**
9 **is detected, an uncorrectable error in particular,**
10 **then that can be used to prevent future errors,**
11 **which would be the rationale for training.**

12 Q So when you say "a sequence of memory
13 addresses," do you mean like a sequence of reads?

14 **A That would be one example, yes.**

15 Q So, in your view, Hazelzet discloses one
16 or more training sequences by disclosing one or
17 more sequences of reads that have errors?

18 **A The sequence would -- some would have**
19 **errors, some would not, in the ECC mode.**

20 Q But, in your view, a sequence of reads
21 being input into the left side of figure 4A of
22 Hazelzet, some having errors, some not, would
23 correspond to one or more training sequences?

24 **A Yes, I believe a person of ordinary**
25 **skill in the art would understand that.**

1 Q Okay. And, in your view, would a
2 sequence of writes, some having errors, some not,
3 would correspond to one or more training
4 sequences?

5 MR. SUH: Objection. Incomplete
6 hypothetical.

7 A Yes, a person of ordinary skill in the
8 art would understand that that would be a training
9 sequence.

10 Q So turning back to paragraph 148 of your
11 declaration -- well, actually, strike that.

12 In paragraph 148 of your declaration, do
13 you refer to a sequence of reads or a sequence of
14 writes being a training sequence?

15 A I don't see that it's specifically
16 identified in that paragraph.

17 Q Well, let me just step back a little
18 bit. What aspects of a sequence of reads or
19 writes makes it training?

20 A In paragraph 151, I was identifying, I
21 think it's the second sentence, it says -- which
22 is talking about how it would be obvious to a
23 person of ordinary skill in the art based on
24 Hazelzet to consider the training sequence to be
25 -- have the purpose of avoiding errors during the

1 normal operation. And so, in that regard, by
2 having the memory accesses check and report that
3 uncorrectable errors have occurred, I believe a
4 person of ordinary skill in the art would
5 recognize that to be a training.

6 Q So you testified previously that "By
7 having the memory accesses check and report that
8 uncorrectable errors have occurred, I believe a
9 person of ordinary skill in the art would
10 recognize that to be training."

11 So is the memory accesses or are the
12 memory accesses the training or is it the check
13 and reporting that's the training?

14 A The memory accesses would be the
15 training.

16 Q Okay.

17 Thank you.

18 Let's turn to the next element in claim
19 1 of the '623 patent, printed circuit board.

20 A Okay. I haven't heard a question yet,
21 but I was finding where the analysis for that was
22 in the declaration.

23 Q Fair enough.

24 So what element or elements of Hazelzet
25 are you relying upon to meet the claim term

1 "printed circuit board" in claim 1 of the '623
2 patent?

3 **A So the DIMM that's disclosed, D-I-M-M,**
4 **that's disclosed by Hazelzet, is disclosed to be a**
5 **printed circuit board.**

6 **Q** Okay. And then moving on to the claim
7 term "error edge connection," what term or terms
8 -- strike that.

9 What element or elements of Hazelzet are
10 you relying upon to meet the claim term "error
11 edge connection" in claim 1 of the '623 patent?

12 **A The error edge -- what is it --**

13 **Q** To be specific, it's the claim term "an
14 error edge connection."

15 **A So, an error edge -- let me make sure I**
16 **read it -- so an error edge connection would be**
17 **the connection on the edge through a pin. And**
18 **we've seen earlier, figure 7A identifies that it's**
19 **the module pin, for example, 4 that is the --**
20 **carries the UE signal.**

21 **Q** Okay. Let me direct you to claim 12 of
22 the '623 patent.

23 **A Okay.**

24 **Q** What element or elements of Hazelzet are
25 you relying upon to meet the claim language

1 "notification circuit" in claim 12 of the '623
2 patent?

3 A (Document review.)

4 Okay. So the notification circuit would
5 be in figure 4B, and it would include the buffer
6 that's driving line 121.

7 Q Is that element 100?

8 A No, not directly. It appears to be a
9 triangle that would indicate the output of 100,
10 and it goes through a buffer driving 121.

11 Q I see.

12 So the element, the triangular element
13 right before the reference line to 121 is your
14 understanding of the notification signal at claim
15 12.

16 MR. SUH: Objection. Mischaracterizes
17 the testimony.

18 A I would say it includes that buffer. I
19 was just looking at figure, say, for example, 1
20 and 2 of the patent show that it's -- of the '623
21 patent are showing a notification circuit 20,
22 which is -- and in particular figure 2 showing --
23 merely being a signal line driving a wire or a
24 connection. Figure 3 indicates there can be some
25 logic before that, and so there would be some

1 logic in 100 that would, for example, select
2 between the PERR input 111 and the UE input 110 in
3 order to determine which of those two signals
4 would be selected as the output of 100, the input
5 to the buffer that drives line 121.

6 Q So as you sit here today, what element
7 or elements of Hazelzet are you relying upon to
8 meet the claim term "notification circuit" in
9 claim 12 of the '623 patent?

10 A I would say it's the portion of the
11 error logic that selects between inputs 110 and
12 111 and drives those out to the buffer, that is
13 what drives line 121, similar to figure 3 in the
14 '623 patent.

15 Q May I direct you to figure 6 of
16 Hazelzet. Strike that.

17 I'll place in front of you Exhibit 1017,
18 the Buchmann reference.

19 (Exhibit 1017 was previously marked
20 and referred to.)

21 Q I believe, Dr. Alpert, that you said you
22 reviewed this reference, the Buchmann reference in
23 preparation for today's deposition. Is that
24 correct?

25 A I did review it. I think you asked me

1 **and I said that, if I recall correctly.**

2 Q Let us turn to figure 6 of Buchmann.

3 So what is your understanding of what
4 figure 6 of Buchmann discloses?

5 MR. SUH: Objection, form.

6 Q Let me ask it this way, Dr. Alpert.
7 What does figure 6 of Buchmann disclose?

8 A Just looking at column 9 of Buchmann,
9 line 16, it says, "Figure 6 depicts a process flow
10 that may be implemented by TS3 (training sequence
11 3) in an exemplary embodiment."

12 Q So what is TS3a in figure 6 of Buchmann?

13 A Looking at column 8 of Buchmann around
14 line 24, it says TS3 is the upstream lane training
15 and repair. And in table 6 it discloses that the
16 TS3a is a substate of TS3. It's called an
17 announce state.

18 Q So in figure 6, do you understand that
19 TS3a is being sent from the memory controller to a
20 series of memory modules?

21 A (Document review.)

22 Yes, figure 6 is depicting the command
23 being sent to MBF, I believe stands for memory
24 buffer. And figure 2 shows the memory buffer is
25 an element of a dual in-line memory module that's

1 **used for communication.**

2 Q What is your understanding of HMC in
3 figure 6 of Buchmann?

4 A **HMC, if I recall, is the host memory**
5 **controller.**

6 Q Okay. So, just taking a look at the two
7 left vertical lines in figure 6, would you
8 understand that to be showing that the TS3a
9 command is being sent from the host memory
10 controller to memory buffer zero in Buchmann?

11 A **Yes, I believe that's what figure 6**
12 **would be showing.**

13 Q What do you understand to be the bit
14 size of TS3a command to be?

15 A **I don't think -- just sitting here at**
16 **the moment, I don't think I have an idea of what**
17 **the size would be.**

18 Q Would it help you if I direct you to
19 table 11 on column 19 of Buchmann?

20 A **I'll look and then I can answer that**
21 **question, whether it helps.**

22 (Document review.)

23 **Sorry, where did you say it was?**

24 Q Table 11 in column 19 of Buchmann.

25 MR. SUH: Objection, relevance.

1 A (Document review.)

2 So it looks as though, for at least the
3 embodiment in table 11, the training state 3
4 announce looks as though it's 6 bits.

5 Q Is there a reason that Buchmann utilizes
6 6 bits for all the training sequences that are --
7 strike that.

8 Is there a reason that Buchmann utilizes
9 6 bits for all the training command batch in table
10 11?

11 MR. SUH: Object to form.

12 A Well, I did just find a disclosure in
13 column 15 that I believe relates to that. At line
14 53, it says, "While the example depicted in figure
15 11 includes a 6-bit SBC, capital S, capital B,
16 capital C, commands and 15-bit values transmitted
17 from the transmitting circuitry 1102 to the
18 receiving circuitry 1104, it will be understood
19 that other bus widths, including SBC command and
20 ECC widths are included within the scope of the
21 invention."

22 So, I believe a person of ordinary skill
23 in the art would understand that the particular --
24 there is a particular embodiment that's disclosed,
25 described in table 11, but that Buchmann is

1 **teaching that the invention can be practiced with**
2 **other lengths or commands.**

3 Q Okay. Let me come back to that passage
4 that you just read, but for now focusing on table
5 11, is there a reason that Buchmann utilizes 6
6 bits for the training commands that are shown in
7 table 11?

8 MR. SUH: Objection. Relevance. Calls
9 for speculation.

10 A **I don't recall a particular significance**
11 **to the 6 bits for this embodiment.**

12 Q Would you understand that the use of 6
13 bits would allow for a wider range of
14 communication commands to be provided between the
15 memory controller and the memory buffer unit in
16 Buchmann?

17 MR. SUH: Same objection to this line of
18 questioning.

19 A **Larger than what? I think you said a**
20 **larger number?**

21 Q Well, than, let's say, 1 bit.

22 A **Well, 6 bits can represent more**
23 **possibilities than 1 bit. Six bits can also be**
24 **transmitted one bit at a time in a six time period**
25 **serially rather than necessarily six bits in**

1 **parallel.**

2 Q Okay. Well, let me -- on that basis,
3 let me just quickly direct you to figure 11 of
4 Buchmann.

5 Do you understand this figure to show
6 the transmission of the training commands in a
7 serial fashion?

8 MR. SUH: Objection to form.

9 A **As I recall from Buchmann, I don't**
10 **believe this would be showing a serial path for**
11 **transmitting the 6 bits of commands.**

12 Q Would there be any reason to have a
13 serial communication in the context of Buchmann's
14 invention?

15 MR. SUH: Objection. Relevance.

16 Q Strike that. Let me ask the question in
17 a different way.

18 So you had previously, you had referred
19 to the example depicted in figure 11 includes a
20 6-bit SBC commands and 15-bit values.

21 Do you understand the 6 bits to be
22 output from element 1182 to ECC encoder 120?

23 A **Yes, I believe that's what figure 11 is**
24 **showing.**

25 Q Do you understand that the ECC encoder

1 120 adds an additional 9 bits to those 6 bits to
2 be output to element 1108?

3 A That's generally what I recall, is that
4 there are 9 bits used for -- as redundant
5 information for error correction and detection.

6 Q Okay. So then those 15 bits are
7 transferred through the high-speed link to element
8 1128, the SBC receiving logic; is that correct?

9 A Yes, I believe this is showing an
10 embodiment where the 15 bits are transmitted over
11 to the receiver and they are sent to the --
12 whatever it is, I guess it's a block 1128.

13 Q Okay, great.

14 So then can you explain to me what
15 happens to those 15 bits when they're received at
16 element 1140.

17 A Well, 15 bits will be passed through
18 block 1142. It's an EEC decoder and syndrome
19 generator, and I believe -- let's see where that's
20 explained.

21 Yes, in column 15, looks like starting
22 at line 48, it's talking about the encoder on the
23 sending side, but it indicates that that is a
24 double error correcting, triple error detecting
25 encoding.

1 Q So is it your understanding that element
2 1142 on the receiving side is essentially
3 crunching the math based on those 9 bits that are
4 added to the SBC command?

5 A Yes, that would be generally the
6 function it's performing.

7 Q Okay. So then to the right of element
8 1142, there's an UE line and another line that
9 refers to 6 bits. Can you explain those two
10 lines.

11 A Looking at column 16 starting at what
12 looks like line 23, it says, "The ECC decoder and
13 syndrome generator 1142 may also provide the SBC
14 FSM/command decoding logic 1144 with error
15 information to assist in decoding the SBC command,
16 e.g., to prevent reliance on an uncorrectable
17 error (ULE) in the SBC command."

18 So with that in mind, maybe I could just
19 hear the specific question again.

20 Q Well, what does UE and 6 bits to the
21 right of element 1142 or the left of element 1144
22 refer to?

23 A The 6 bits coming out of 1142 would be
24 the 6-bit command, as that's been derived from the
25 15 bits sent over. And I don't see in the text

1 what is UE. The text talks about an uncorrectable
2 error. It says ULE. But I believe a person of
3 ordinary skill in the art would understand that UE
4 is likely referring to a signal line that
5 indicates whether the command being sent over on
6 the 6 bits is correct or not. In other words,
7 either it was -- didn't need to be corrected or it
8 was correctable, but in some situations, such as
9 triple errors, there could be a error detected but
10 not corrected, and that would be likely what the
11 use of the UE is for.

12 Q So is that UE line in figure 11 of
13 Buchmann analogous to the UE line in figure 4B of
14 Hazelzet?

15 MR. SUH: Objection. Relevance. Form.

16 A Generally I would say that it does
17 appear that they would both be used when there was
18 an error correcting code to indicate that an error
19 was detected but couldn't be corrected.

20 Q Right. Because in both cases, to the
21 left of the UE line there is some kind of logic or
22 element that's crunching the math to determine
23 whether the error is uncorrectable. Correct?

24 MR. SUH: Objection. Same objection to
25 the line of questioning.

1 A So Hazelzet in figure 4B, and this one,
2 Buchmann in figure 11, do both show a block that
3 has the function of checking and correcting some
4 received values, checking for errors and
5 correcting them when possible.

6 Q Turning your attention back to figure 11
7 of Buchmann, so the line to the right of element
8 1142 that has a slash with a 6, is that where TS
9 command would be provided on?

10 MR. SUH: Same objection.

11 A Yeah, I believe a person of ordinary
12 skill in the art would understand that on the
13 receiving side, that 6-bit -- that bus with six
14 lines would carry the SBC command.

15 Q And do you think that the signal on the
16 UE line to the right of element 1142 would be a
17 1-bit signal?

18 MR. SUH: Objection. Relevance.

19 A I believe that's likely what's
20 indicated, particularly on this diagram shows a
21 number of connections with kind of a slash and a
22 number next to it indicating that there's several
23 lines in parallel. And so since the line with the
24 arrow that's labeled UE doesn't have the slash or
25 any indication that there are multiple signal

1 **lines there, I believe it would be an indication**
2 **that there's a single line for the UE.**

3 Q Okay. Let me actually turn back for a
4 moment to Hazelzet since we've been discussing
5 Hazelzet a little bit here. I wanted to know, in
6 your opinion, as you sit here, what you believe
7 Hazelzet is directed to.

8 MR. SUH: Objection. Form.

9 A **(Document review.)**

10 Looking at the background of the
11 **invention, paragraph 1 in Hazelzet, it indicates**
12 **the invention relates generally to high density,**
13 **high reliability memory module with fault tolerant**
14 **address and command bus for use as a main memory.**

15 Q So that's what you believe Hazelzet is
16 directed to?

17 A **Yes.**

18 MR. ARJOMAND: Let's take a quick break.
19 Off the record.

20 (A brief recess was taken.)

21 BY MR. ARJOMAND:

22 Q Dr. Alpert, before the break, we were
23 talking about figure 11 of Buchmann. With respect
24 to figure 11, we were mentioning SBC commands. Do
25 you recall that?

1 **A Yes.**

2 **Q Would you understand TS3a to be a SBC**
3 **command?**

4 **A Yes, that's my understanding. I believe**
5 **table 11 is showing its -- about the middle**
6 **there's a training state 3 announce, and I believe**
7 **that's what we saw. I think that was the same**
8 **name that we saw earlier in a table that talked**
9 **about the TS3 states.**

10 **Q Would you generally understand -- strike**
11 **that.**

12 Would you understand that generally all
13 the TS3 commands are SBC commands?

14 MR. SUH: Objection, form.

15 **A I don't think that I've studied whether**
16 **all the commands are necessarily identified as SBC**
17 **commands.**

18 **Q Okay. So if I may direct you to figure**
19 **6 of Buchmann, would you understand that TS3**
20 **commands shown in figure 6 of Buchmann are SBC**
21 **commands?**

22 **A Sorry, which -- let me hear that again,**
23 **please, at least the first part.**

24 **Q Are you looking at figure 6 of Buchmann?**

25 **A Yes.**

1 Q Would you understand that the TS3
2 commands shown in figure 6 of Buchmann are SBC
3 commands?

4 A I see a number of commands. It looks
5 like it goes all the way "a" through "f". And I'm
6 just not aware whether all of those would be SBC
7 commands.

8 Q Okay. Would you understand that the
9 TS3a command is an SBC command?

10 A Sorry, that's TS3a?

11 Q Did I -- yes.

12 A Okay. That was one I saw in table 6
13 that does indicate that there's a TS3a state, the
14 announce state. And it's my understanding that
15 table 11 is showing that there's encoding for
16 training state 3 announce, which I believe would
17 correspond to that -- to the same description in
18 table 6.

19 Q Continuing on with the commands that are
20 shown in figure 6 of Buchmann, would you
21 understand the TS3b message to be an SBC command?

22 A Well, I see again looking at table 6 and
23 table 9 -- sorry, table 6 and table 11, I see a
24 training -- TS3b-acknowledge, which I believe
25 would correspond to the training state 3

1 **acknowledge in table 11. So generally that's my**
2 **understanding from seeing the same terminology**
3 **used.**

4 Q Well, now that you've taken a look at
5 table 6, which I think continues on to column 9?

6 A **Yes.**

7 Q Would you believe it fair to say that
8 messages TS3a through f in figure 6 are SBC
9 commands?

10 A **Again, just looking at the table 6 and**
11 **table 11 and what I recall from, it's a**
12 **substantial sized disclosure, I just don't**
13 **remember what, you know, TS3c and all the way**
14 **through TS3f mean, whether those mean commands or**
15 **it's just an indication that there's a certain**
16 **state for the training sequence.**

17 Q Okay. Let's focus on TS3b message. So
18 just to resummairize your testimony through the
19 past few questions and answers, you would agree
20 that the TS3 message is an SBC command, correct?

21 A **That's my understanding looking at,**
22 **particularly at table 11 and understanding that**
23 **TS3b is a training state 3 acknowledge.**

24 Q Okay. And so sometimes in the memory
25 module art, people refer to a read command or a

1 write command.

2 Would you understand that the TS3b
3 message is a read or write command?

4 A Looking at the description here in table
5 6, I don't believe that a TS3 announce command
6 would be a read or write command.

7 Q Okay. Let me direct you back to figure
8 11 of Hazelzet.

9 A I was just going to ask, before we move
10 off figure 6, I did want to make -- make an
11 observation because we did speak earlier about how
12 on the left side there's the host memory
13 controller, and that would be sending commands to
14 MB0, which would in turn forward those to MB1,
15 which would forward them to MB2 and MB3. And I
16 just want to point out that this particular
17 embodiment is an example where those memory
18 buffers are cascaded, so one communicating with
19 the next. And there's several disclosures, I
20 located one, that indicate that particular sort of
21 communication network is not the only one that's
22 envisioned by the patent. And if I look at --
23 let's see. I'm looking at column 28, line 23. I
24 do recall there's several other places that says
25 something like this in Buchmann. And it says, "In

1 exemplary embodiments, the memory system includes
2 one or more hub devices on one or more memory
3 modules connected to the memory controller via one
4 or more cascade interconnect memory buses.

5 However, one or more other bus structures or a
6 combination of bus structures may be implemented
7 to enable communication such as point-to-point
8 buses, multi-drop buses, or other shared or
9 parallel buses. They often allow various means of
10 communicating, including both high speed and low
11 speed communication means." It goes on to further
12 say that there would be some design trade-offs
13 based on the frequency performance, power, cost,
14 and so on.

15 But in particular, the disclosure here
16 does talk about what it calls multi-drop buses,
17 which would be a configuration where there would
18 be a memory controller talking to multiple memory
19 modules using the same signal lines.

20 Q Rather than in a cascade format as shown
21 in figure 6 of Buchmann?

22 A Yes, rather than a cascade format.

23 Q Okay. Let me turn you, since we're
24 still talking about Buchmann, let me turn you back
25 to figure 11 of Buchmann.

1 Are you looking at figure 11?

2 **A Yes, I am.**

3 **Q Great.**

4 Do you recall we were talking about UE
5 line and the line that is 6 bit to the left of
6 element 1142?

7 **A Yes. To the right.**

8 **Q Did I say left?**

9 **A Okay.**

10 **Q I apologize.**

11 Let me ask the question again so the
12 record is clear.

13 In figure 11 of Buchmann, to the right
14 of element 1142, there is a UE line and a line
15 that is indicated as having 6 bits. Do you see
16 those?

17 **A Yes.**

18 **Q And my question to you is, why are there**
19 **two lines there?**

20 **MR. SUH: Objection. Relevance.**

21 **A I think I know what you mean. Can you**
22 **clarify what the two lines are.**

23 **Q Yes, let me explain. I believe from**
24 **your previous testimony, you explained that the UE**
25 **line would have the UE signal on it, whereas the**

1 6-bit line would have the SBC command. And the
2 question that I have for you is, why does Buchmann
3 separate those two signals on to two different
4 lines?

5 MR. SUH: Objection, relevance.

6 A I don't think I have -- I don't think I
7 have an answer necessarily for why that's done.

8 Q As you sit here today?

9 A As I'm sitting here today here, yes. I
10 mean, it might have said something in the
11 disclosure, but I don't recall.

12 Q Okay. All right.

13 Dr. Alpert, would it be fair to say that
14 you're combining Hazelzet with Buchmann in your
15 declaration?

16 A There is a combination of the teachings
17 of those two references that is provided in
18 support of an obviousness opinion.

19 Q So in that combination, what are you
20 relying on Buchmann for with respect to claim 1 of
21 the '623 patent?

22 MR. SUH: Objection, form.

23 Q Maybe I should ask it more clearly.

24 So in the Hazelzet-Buchmann combination,
25 what are you relying upon for Buchmann with

1 respect to claim 1 of the '623 patent?

2 MR. SUH: Same objection.

3 **A So, in the combination, relying on the**
4 **teachings of Buchmann that relate to training**
5 **sequence, and I'm still just looking -- (document**
6 **review) -- and the notification signal indicating**
7 **a status of the training sequence.**

8 Q So would it be fair to say that in your
9 Hazelzet-Buchmann combination, you're relying on
10 Buchmann for meeting the element of a notification
11 signal indicating at least one status of one or
12 more training sequences?

13 A Yes, as I'm looking at the claim again,
14 I would say that's what Buchmann discloses that
15 would be a teaching that could be used to modify
16 Hazelzet notification signal indicating at least
17 one status of one or more training sequences.

18 Q And are you relying upon Buchmann's TS3b
19 message as being that notification signal
20 indicating at least one status of one or more
21 training sequences?

22 MR. SUH: Objection, form.

23 A **(Document review.)**

24 THE WITNESS: Okay, so can I hear that
25 again, please.

1 (Record read.)

2 **A That would be an example.**

3 Q Well, is there another TS3 message that
4 you're relying upon in Buchmann for meeting the
5 claim language of a notification signal indicating
6 at least one status of one or more training
7 sequences?

8 MR. SUH: Object to form.

9 **A I would say there's a large number of**
10 **training sequences, steps of training sequences**
11 **that are disclosed in Buchmann, and for many of**
12 **them Buchmann teaches that a status would be**
13 **reported back to the memory controller.**

14 Q But in paragraph 165 of your
15 declaration, you're pointing to the TS3b message,
16 right?

17 MR. SUH: Objection, relevance.

18 Q Or let me rephrase that.

19 In paragraphs 165 through 171, you're
20 referring to the TS3b message as meeting the
21 notification signal indicating the status of one
22 or more training sequences; is that correct?

23 MR. SUH: Same objection. Objection,
24 form, too.

25 **A Looking at paragraph 167, I see what I**

1 recalled, which looks like it might be the second
2 sentence. It says, as an example of notification
3 signals without polling, Buchmann explains that
4 during the upstream lane training TS3 memory --
5 the memory module generates and outputs various
6 notification signals indicating the status of the
7 TS3 training sequence to the memory controller of
8 the host system.

9 So that issue of the TS3_acknowledge is
10 pointed out here, and I meant that very
11 specifically as just one example of Buchmann's
12 disclosure.

13 Q Okay. But since you've specifically
14 identified the TS3b message, let's focus on that
15 for now.

16 How would you understand that that
17 message would be combined with Hazelzet?

18 A So I believe the teachings of Hazelzet
19 and Buchmann would be combined by having the
20 training sequences disclosed by Buchmann, at least
21 as examples to be communicated to the -- from the
22 memory controller to the memory module in Hazelzet
23 and then having a status for those training
24 sequences returned on the UE signal line we talked
25 about of Hazelzet.

1 Q Is it your understanding that in
2 Hazelzet -- strike that.

3 Is it your understanding -- do you have
4 Hazelzet?

5 A I think I might have put it over here.

6 No.

7 Actually, I believe this was just a
8 clean copy. I don't know if you have -- I don't
9 know if I want to refer to that one.

10 Q That's fine.

11 A Just because it's labeled here and
12 bound.

13 So the question is on?

14 Q Figure 2 of Hazelzet.

15 A Yes.

16 Q So is it your understanding that in your
17 combination of Hazelzet and Buchmann, that the
18 memory controller would issue some type of TS3
19 message, such as TS3a to the ECC/parity register
20 21, and that register would return another TS3
21 message, such as TS3b back to the memory
22 controller?

23 MR. SUH: Objection to form and
24 relevance.

25 A Okay. I kind of heard multiple aspects

1 of questions there. I don't know if you want to
2 break it apart. I think I focused on the first
3 part.

4 Q Why don't you try your best to answer
5 that question and we'll go from there.

6 A Okay. So, again, TS3 was an example
7 from Buchmann. That particular command might or
8 might not be used in the combination. It is
9 related to upstream lane training and repair,
10 which, compared to figure 2 in Hazelzet, it
11 wouldn't necessarily be a very appropriate command
12 given that Hazelzet is not showing at least --
13 this embodiment is not showing the kind of
14 cascaded connection that is shown in Buchmann's
15 embodiments. So instead what I would say is that
16 the memory controller in Hazelzet would be
17 modified to initiate training commands, training
18 sequences like Buchmann does, and that the success
19 or failure of those training sequences would be
20 indicated by a status on the UE signal line that
21 comes back from the module to the memory
22 controller in Hazelzet.

23 Q Well, Dr. Alpert, I would like to focus
24 on your declaration, which refers to TS3 messages,
25 if you will. I mean, you do rely upon the TS3

1 messages for your combination of Hazelzet and
2 Buchmann, correct?

3 **A** I rely on that as an example of a
4 training sequence disclosed by Buchmann along with
5 a notification that comes back. It is an example.

6 **Q** But putting aside that in your opinion
7 today you believe it's exemplary, in any event,
8 you do rely as an example on the TS3 messages in
9 Buchmann, correct?

10 **A** First of all, it's not just my opinion
11 today that it's an example. It says -- the plain
12 explanation in the declaration says, "As an
13 example, notification signals without polling."
14 So it was my opinion and I documented it clearly
15 at the time, I think back last December when this
16 declaration was submitted.

17 So TS3 is an example of a training
18 sequence, and the acknowledge is an example of a
19 notification from Buchmann.

20 **Q** Okay. So I understand your position
21 that you believe that your reference to TS3
22 messages was exemplary, but, nonetheless, you do
23 rely upon it in paragraphs 165 through 171 of your
24 declaration, correct?

25 **A** Yes, it does give that as an example.

1 Q So let's just focus on that example. So
2 what I want to understand from you is, in that
3 example, is it your understanding that the memory
4 controller 19 in figure 2 of Hazelzet would issue
5 a TS3a message and then the ECC/parity register 21
6 would issue a TS3e message in response?

7 MR. SUH: Objection, relevance.

8 A No. The memory controller would issue a
9 command which could be the command to enter TS3.
10 And the status that comes back, the notification,
11 would be an indication of whether or not that
12 command was completed successfully or not, and
13 that would come back on the UE, the line that goes
14 from the, whatever it is, chip 21 to the memory
15 controller from Hazelzet.

16 Q So I guess I'm a little bit confused by
17 your answer because I felt that you started with a
18 no, but the rest of your answer seemed to be
19 consistent with my question. So I would like to
20 ask it to you one more time.

21 Is it your understanding in your
22 Hazelzet-Buchmann combination relying on TS3
23 messages, that the memory controller 19 would
24 issue a TS3a message to the ECC/parity register
25 21?

1 MR. SUH: Same objection to the line of
2 questioning.

3 A I would say is that the memory
4 controller in the combined system would issue a
5 command. I wouldn't call it a message. I don't
6 know if message might have other meaning.

7 Q But it would be a TS3a message?

8 A That would be an example of what command
9 could be sent to the ECC/parity register 21 from
10 the memory controller 19.

11 Q And then in your Hazelzet-Buchmann
12 combination, based on the TS3 messages, the
13 ECC/parity register 21 would respond with a TS3b
14 message on UE line 121 of figure 4B of Hazelzet;
15 is that correct?

16 MR. SUH: Same objection.

17 A The UE would indicate that the command
18 was complete, the status of complete, not
19 necessarily the same as the message from Buchmann.

20 Q So in your Hazelzet-Buchmann
21 combination, that UE line would not carry
22 Buchmann's TS3b message?

23 A It would be an indication of whether the
24 command was complete or not. I don't remember
25 what -- whether that's all that's in the TS3b

1 **message.**

2 Q But my question to you is, would it
3 carry the message identified in figure 11 or table
4 11 of Buchmann that corresponds to
5 TS3b_acknowledge?

6 A (Document review.)

7 So looking at Buchmann in table 6, it
8 says the TS3b_acknowledge is an indication that
9 the last memory buffer in the memory channel sends
10 the TS3a_ack upon detecting the TS3a_announce.
11 TS3a_ack is decoded, corrected and forwarded back
12 to the host by the remaining memory buffers.

13 So to the extent that TS3b_acknowledge
14 is an indication that the TS3a_announce has been
15 completed, then that information would be
16 indicated by the UE signal.

17 Q So would that TS3b_acknowledge be what's
18 shown in table 11 of Buchmann?

19 A No. It would not be, for example, a
20 6-bit code that's shown there.

21 Q So it wouldn't be the code that's shown
22 as 001001 in your Hazelzet-Buchmann combination?

23 A That's correct. It wouldn't be that
24 code.

25 Q What code would it be?

1 **A** It would be an indication of the same
2 information, which is that the TS3a command has
3 completed.

4 **Q** So would that code be -- strike that.
5 So why wouldn't it be the code that's
6 shown in table 11 of Buchmann corresponding to
7 TS3b_acknowledge?

8 **A** Because in modifying Hazelzet, it
9 wouldn't be necessary or appropriate just to try
10 to drop the exact same implementation of Buchmann
11 into there and, instead, teachings of Buchmann
12 would be used by a person of ordinary skill in the
13 art to modify Hazelzet but not to incorporate
14 Buchmann wholesale.

15 **Q** But, in your opinion, one of ordinary
16 skill in the art could utilize the 6-bit message
17 that's shown in table 11 of Buchmann on the UE
18 line in Hazelzet's figure 4B?

19 **A** There are lots of ways, you know, that
20 these two references can be combined. Sitting
21 here right now, I don't see a reason why the UE
22 line couldn't be used for that purpose, for
23 example, if it were used to communicate those 6
24 bits serially.

25 **Q** Okay. So let me -- since we're talking

1 about the UE line 121, can I direct you to figures
2 4A and 4B of Hazelzet.

3 So we've been talking about where the
4 TS3b_acknowledge message would be in the figure 4B
5 of Hazelzet. Where would the TS3a message be
6 received in figure 4A of Hazelzet?

7 MR. SUH: Objection, relevance.

8 A One way to do that would be to send the
9 SBC commands, of which the TS3a was one example,
10 over the command lines to the register chip 21.

11 Q And those would be lines 32a through 32n
12 of figure 4A?

13 A That would be command and address, so
14 the command would be a subset of those.

15 Q Okay, understood.

16 Dr. Alpert, what would be the reason for
17 placing the TS3b message on UE line 121 in your
18 Hazelzet and Buchmann combination?

19 A Well, one example would be that both
20 Hazelzet and Buchmann are oriented to providing
21 error correction for the commands that are sent
22 from a memory controller to the memory module, and
23 so, therefore, the same logic that's used in
24 Hazelzet to detect, in this case correct or
25 indicate uncorrectable errors for the commands in

1 the first mode of operation, could be used in the
2 second mode, the ECC mode to detect whether there
3 have been errors in the commands for the training
4 sequence.

5 Q As you sit here today, are there any
6 other reasons that you can think of for placing
7 the TS3b message on UE line 121 in your Hazelzet
8 and Buchmann combination?

9 A I would say just, you know, that was
10 kind of a specific rationale. I would just say
11 generally that the UE is a signal line that
12 returns information from the memory module to the
13 memory controller and, as well, it's one that is a
14 wire or signal so it could be used -- be shared by
15 a number of memory modules at the same time. So,
16 therefore, that signal, you know, could be used
17 for other purposes besides just the indication of
18 uncorrectable errors in the communication between
19 the memory controller and the chip 21 of Hazelzet.

20 Q So, in your Hazelzet-Buchmann
21 combination, the TS3a message that is received
22 perhaps on the command lines in figure 4A of
23 Hazelzet, and then a TS3b message is expressed on
24 the UE line 121. Is that correct?

25 A That's one example of how that

1 **combination could operate.**

2 Q Okay. So when the TS3b message is
3 expressed on UE line 121, does that signify that
4 the TS3a message has been received?

5 MR. SUH: Objection, relevance.

6 Q Or let me phrase it this way.

7 Does the TS3b message on UE line 121 in
8 your Hazelzet-Buchmann combination indicate
9 successful transmission of the TS3a message
10 received in figure 4A of Hazelzet?

11 A **Yes, as I'm looking at table 6 in**
12 **Buchmann, that's how it describes the**
13 **TS3b_acknowledge.**

14 Q So the TS3b_acknowledge in your
15 Hazelzet-Buchmann combination doesn't relate to
16 the processing of that message between receipt and
17 output on UE line 121?

18 MR. SUH: Objection. Mischaracterizes
19 testimony.

20 A **As I understand what Buchmann is**
21 **disclosing, the TS3b_acknowledge is merely a**
22 **notification that the TS3a was successfully**
23 **received.**

24 MR. ARJOMAND: Okay. Thank you.

25 Let's take a really short break because

1 I'm at a point where I can move on to another
2 subject. Thank you.

3 (A brief recess was taken.)

4 MR. ARJOMAND: Let's go back on the
5 record.

6 BY MR. ARJOMAND:

7 Q Dr. Alpert, let me place in front of you
8 Exhibit 1016, the Talbot reference.

9 Dr. Alpert, let me direct you to figure
10 1 of Talbot. What is element 160A in figure 1 of
11 Talbot?

12 A The element 160A is a serial
13 interconnect between the memory controller and
14 whatever buffer unit 170.

15 Q Would it be fair to say that it's --
16 strike that.

17 Would it be fair to say that serial
18 interconnect 160A is between memory controller 100
19 and buffer units 170A and 170B as shown in figure
20 1?

21 A I believe looking at the figure, looking
22 at the disclosure briefly, I believe that the 160A
23 is between the memory controller and the 170A. I
24 believe it's a separate path between 170A and
25 170B.

1 Q Okay, thank you.

2 And is your understanding that 160B is
3 similar to 160A in that it is a serial
4 interconnect between memory controller 100 and
5 buffer unit 170A shown in figure 1 of Talbot?

6 MR. SUH: Objection, relevance.

7 A Yes, it's my understanding that it's --
8 that's another serial interconnect.

9 Q So just to make it simple, would it be
10 okay to refer to serial interconnect 160A and 160B
11 collectively as serial interconnect 160?

12 A Yes, I believe the patent does that as
13 well.

14 Q What is element 165 in figure 1 of
15 Talbot?

16 MR. SUH: Objection, relevance.

17 A 165 is a parallel interconnect between
18 -- well, let's just say to the memory modules 110.
19 No, it says memory units 110.

20 Q Okay. So is interconnect 160A -- strike
21 that.

22 Is interconnect 160 different from
23 interconnect 165 in that interconnect 160 is
24 serial while interconnect 165 is parallel?

25 MR. SUH: Objection, relevance.

1 **A** **Yes, that's -- that is one difference,**
2 **yes.**

3 **Q** Would another difference between
4 interconnect 160 and 165 be the data rates?

5 MR. SUH: Same objection.

6 **A** **Yes, I believe the data rate is**
7 **different.**

8 **Q** As you sit here today, are there any
9 other differences between interconnect 160 and
10 interconnect 165 in Talbot?

11 MR. SUH: Same objection to this line of
12 questioning.

13 **A** **One other difference I'm noticing is**
14 **that the address command and memory clock that**
15 **goes to what's called memory units 110, the**
16 **parallel interconnect 165 includes those signals,**
17 **whereas those signals are not a part of at least**
18 **what's circled here as 160A -- 160A or B, the**
19 **serial.**

20 **Q** Would another difference between serial
21 interconnect 160 and parallel interconnect 165 be
22 that serial interconnect has CRC data on it?

23 **A** **Yes, that would be a difference. I'm**
24 **looking at figure 2. That does appear to be a**
25 **difference.**

1 Q And what is your understanding of B CMD
2 in figure 1 of Talbot?

3 A **These are commands to the buffer 170**
4 **that come from the memory controller.**

5 Q And would you understand that to be a
6 difference between serial interconnect 160 and
7 parallel interconnect 165, specifically that
8 serial interconnect has these buffer commands?

9 A **Yes, that does appear to be a**
10 **difference, although I haven't searched through**
11 **the spec to indicate whether there might be some**
12 **overlap.**

13 Q What do you think is the problem that
14 Talbot is seeking to solve?

15 MR. SUH: Objection, form.

16 A **Well, I see based on what Talbot is**
17 **disclosing, that the problem is to be able to**
18 **provide a serial interconnection for the data**
19 **going to and from memory, serial interconnection 4**
20 **memory controller to the memory subsystem while**
21 **still using memory units, they're called, that**
22 **have parallel data bus.**

23 Q What do you believe is Talbot's solution
24 to that problem?

25 MR. SUH: Objection, form.

1 A The solution that Talbot provides is
2 primarily in the form of this memory buffer 170
3 that converts between the serial data
4 communication of the memory controller and the
5 parallel data communication of the memory modules.

6 Q Why is it important in Talbot for the
7 interconnect 160 between the memory controller and
8 the buffer units 170A to be a serial interconnect?

9 MR. SUH: Objection to form. Relevance.

10 A (Document review.)

11 One reason for having -- putting this
12 serial data buffer in between the memory
13 controller and the memory modules that a person of
14 ordinary skill in the art would be aware of is
15 that approach would allow the memory controller to
16 have fewer pin signals, either just to reduce the
17 number of pins or to provide, for example, for
18 multiple data paths with a comparable number of
19 pins.

20 Q Okay. Do you recall Talbot disclosing
21 asymmetric functionality?

22 A I don't recall those words.

23 Q Let me direct you to paragraph 35 of
24 Talbot, specifically right in the center of the
25 paragraph.

1 A Okay, I've read that portion.

2 Q What's your understanding of functional
3 asymmetry -- strike that.

4 What's your understanding of the
5 reference to functionality asymmetry in paragraph
6 35?

7 A Well --

8 MR. SUH: Objection, relevance.

9 A Yes, what it says is that, "However, it
10 is described in greater detail below, buffer unit
11 170 may be simplified, making this type of control
12 functionality asymmetric. As such, memory
13 controller may include control functionality that
14 may dynamically and adaptively adjust the signal
15 characteristics of transmitted write data to
16 enable buffer unit 170 to correctly read the data
17 based on information received from buffer unit
18 170."

19 Q So what does that mean to you?

20 A So what it means is that there is more
21 control of the signal characteristics that's
22 placed within the memory controller 100 than in
23 the buffer 170.

24 Q Okay. What is Talbot's training in your
25 opinion?

1 A There's several places it's described in
2 the specification. What I kind of went to was
3 paragraph 152, which says that "after reset or
4 power-on condition," it says "block 400" -- okay,
5 that's just walking through the figure 4 -- "in
6 one embodiment, control logic 255 causes the
7 buffer unit 170 to come out of reset in a training
8 mode. Upon entering the training state, all
9 bidirectional signal path drivers (DDQ, DQ, and
10 DQS) may be placed in a high-impedance state. In
11 the training mode," this particular training mode,
12 "the BCMD signal path, is looped back to the CRC
13 signal path during even MCLK cycles and a training
14 pattern (for example, 10101010) is output on the
15 CRC path during odd MCLK cycles. The memory
16 controller 100 drives a training pattern on the
17 BCMD signal path, which is returned on the CRC
18 path during even MCLK cycles. The memory
19 controller obtains bit-lock and byte-lock
20 receiving known data patterns on the CRC. In
21 addition, memory controller adjusts the phase of
22 the BCMD clock signal by adjusting a variable
23 phase unit so that the buffer unit may obtain
24 bit-lock (i.e., bit alignment) and byte-lock
25 (i.e., byte alignment) on the B command signal

1 **path."**

2 Q That passage that you just read is
3 Talbot's training in your opinion?

4 A **I think that's an example of the**
5 **training that occurs after power-on/reset.**

6 Q So is the nature of Talbot's training
7 initialization?

8 MR. SUH: Objection, form.

9 A **It also does indicate in paragraph 84,**
10 **it talks about during operation, memory**
11 **controller, in this case 800, may dynamically and**
12 **adaptively adjust the signal characteristics, for**
13 **example, the phase of transmitted write data and**
14 **received read data.**

15 And then at paragraph 88 it indicates
16 **that "At predetermined intervals during normal**
17 **operation (e.g. every 100 microseconds), memory**
18 **controller 800 may train the upstream and**
19 **downstream signal paths using a periodic training**
20 **mode."**

21 So there is a disclosure as well that
22 **the training would be done periodically after**
23 **initialization.**

24 Q Okay. But is it your understanding that
25 the nature of the training from your quotes on

1 paragraph 84 and 52, that it's associated with
2 alignment or synchronization?

3 MR. SUH: Objection, form. Asked and
4 answered.

5 A The example I see in a little bit more
6 details in paragraph 36, that it says, "More
7 particularly, at high data rates, the
8 uncertainties of delays in the transmission path
9 for different signals in a bus may require per bit
10 phase adjustment of a sample clock of a receiver
11 of those signals. To avoid employing this
12 circuitry in buffer unit 170, the memory
13 controller may adjust the phase of its transmitted
14 clock and data signals to avoid complex phase
15 shifting circuits in the slave."

16 So at least for that example that I've
17 seen here, it would relate to synchronizing the
18 data signals and the clock signal.

19 Q It appears that both paragraphs 36 and
20 84 you cite refer to phase adjustments. Is that
21 correct?

22 A Yes, that's what both of those
23 paragraphs refer to.

24 Q That would inform you on the nature of
25 initialization in Talbot -- I'm sorry, that would

1 inform you the nature of training in Talbot?

2 MR. SUH: Objection, form.

3 A Well, certainly those examples do refer
4 to the adjustment of the clock phase as well as
5 the data receivers and drivers. At the moment I
6 don't recall if there are other examples of
7 training that Talbot talks about.

8 Q Going back to paragraph -- I'm sorry,
9 going back to paragraph 52 that you initially
10 referenced, I see that it refers to the B CMD
11 signal path and a CRC path.

12 Those are on the serial interconnect 160
13 between the memory controller and the buffer unit
14 170A, correct?

15 MR. SUH: Objection, relevance.

16 A Yes, I think, for example, figure 2
17 shows those signals B CMD and CRC are shown along
18 what's indicated to be the serial interconnect
19 160.

20 Q Since we're talking a little bit about
21 training here with regard to Talbot, can we just
22 go back to Buchmann. Do you have that in front of
23 you? It's Exhibit 1017.

24 A Yes, I've been using this.

25 Q It's easier.

1 A Yes, but it took me a little while to
2 descramble the pages that weren't bound, but they
3 are -- I don't know if you need them or not,
4 because in the past I have gotten some exhibits
5 quite permuted.

6 Q Interleaved.

7 A Yes, something like that.

8 Q So we have been talking about Buchmann,
9 the TS3 training. Do you recall that?

10 A Yes.

11 Q And my recollection was that you had
12 pointed to column 8 of Buchmann, the reference to
13 TS3, specifically upstream lane and lane training
14 and repair.

15 A Yes, it looks like it's column 8, line
16 24.

17 Q Right.

18 What is your understanding of training
19 in Buchmann?

20 Let me ask you that differently. Based
21 on the disclosure of TS3 in column 8, what do you
22 believe to be the nature of training in Buchmann?

23 MR. SUH: Objection, form.

24 A Well, if we look at the bottom of column
25 8, it kind of describes what is the training that

1 occurs and it says, "Upon removal of TS3a_annnc,
2 MBs drive locally generated PRBS23 on upstream
3 transmitters. The host and MB US receivers
4 analyze received signal quality, identify broken
5 lanes, achieve bit lock, equalize receivers and
6 perform BER optimization." So that's at least
7 some description of what happens in --
8 specifically for training in the TS3.

9 Q Is that occurring -- strike that.
10 Are those -- strike that.
11 What you just referred to are actions
12 that are taken during initialization?

13 A Well, I've been looking at column 4 --
14 let's see, starting at line 51 is the paragraph
15 that refers to figure 3. And at least the
16 beginning of that sequence at figure 3 says that
17 it's for the states of the MB, the memory buffer,
18 during power-up and initialization in an exemplary
19 embodiment. So at least looking at that
20 disclosure would indicate that a power-on -- that
21 there would be initialization that would include
22 going through those training sequences. For
23 example, in figure 3, looks like the circle 316
24 would include a TS3 sequence. It says TS2 to 7,
25 which I believe would include the TS3 sequence

1 that we were looking at before. But with that
2 said, I haven't looked through to indicate whether
3 there might be other times when certain training
4 would be performed.

5 Q You pointed to some actions that are
6 taken at the bottom of column 8 of Buchmann. Do
7 you recall that?

8 A Yes.

9 Q So achieving bit-lock equalization, et
10 cetera, are those similar to the type of training
11 that is done in Talbot with regard to phase
12 adjustment and other aspects of Talbot that you
13 identified earlier?

14 MR. SUH: Objection. Form and
15 relevance.

16 A I say that at this -- up until now I
17 haven't tried to compare the operations and
18 sequencing between Talbot and Buchmann, and right
19 now just looking at it, it appears a disclosure
20 for Buchmann is more elaborate, but I don't know
21 what the differences might be.

22 Q But you would agree that Buchmann refers
23 to bit lock in the context of training at the
24 bottom of column 8, correct?

25 MR. SUH: Same objection.

1 **A Yes, at the bottom of column 8, it does**
2 **refer to train and test in the training state 3**
3 **that does involve bit lock.**

4 **Q I thought that you testified that Talbot**
5 **also addresses bit lock and its training. Did I**
6 **misunderstand you?**

7 **A I don't know. I don't remember. It**
8 **might have been only five minutes ago, but I don't**
9 **recall talking about it in Talbot.**

10 **Q I thought you discussed bit lock in the**
11 **context of Talbot. Maybe it was in the context of**
12 **paragraph 84 or in the context of paragraphs 35**
13 **and 36, paragraph 52? Yes, paragraph 52 refers to**
14 **bit lock.**

15 **A Okay, I see that from Talbot, and we did**
16 **talk about that.**

17 **Q So my recollection -- so let me ask you**
18 **the question now in a more clear fashion.**

19 **Is the bit lock that's performed in the**
20 **training of Buchmann at the bottom of Buchmann's**
21 **column 8 similar to the bit lock that's performed**
22 **during training in paragraph 52 of Talbot?**

23 **MR. SUH: Objection. Form. And**
24 **relevance. Asked and answered.**

25 **A I don't know how similar the bit-lock**

1 **training processes are for the two of them.**

2 Q Well, is there any reason for you to
3 doubt that they would be dissimilar?

4 MR. SUH: Same objection.

5 A I would expect the result to be similar,
6 but we do note that Talbot was emphasizing the
7 advantages of putting the complexity in the memory
8 controller, for example.

9 And so the particular steps that are
10 taken to achieve the bit lock might well be
11 different between Talbot where it's adjusting the
12 memory controller and at least the embodiment of
13 Buchmann that we looked at, figure 6, which would
14 need to do the buffers on each module as well.

15 Q But you would say -- strike that.

16 But would it be fair to say that in your
17 view both Talbot and Buchmann are directed to bit
18 lock in the context of training?

19 MR. SUH: Same objection.

20 A Yes, I think that's apparent from the
21 disclosure, that both aimed at achieving bit lock
22 during training.

23 MR. ARJOMAND: Let's take a short break.

24 THE WITNESS: Sure.

25 (A brief recess was taken.)

1 (Exhibit 1015 was previously marked
2 and referred to.)

3 BY MR. ARJOMAND:

4 Q Let me place in front of you Exhibit
5 1015, the Amidi reference. I know you already
6 have that in your binder, but let's be official
7 about it.

8 A And I did just want to add a point about
9 Talbot, if I may. I don't know if we're on the
10 record.

11 Q Well, with all due respect, Dr. Alpert,
12 I'm running low on time and I would like to
13 continue with my questions. If we have time at
14 the end, I'll make sure you have some time or
15 counsel here can redirect you.

16 A Okay.

17 Q So you stated at the start of the
18 deposition that you had reviewed the Amidi
19 reference in advance of this deposition; is that
20 correct?

21 A Yes, I have reviewed it.

22 Q So in your review, what is the training
23 in Amidi?

24 A Well, looking at the declaration in
25 paragraph 153, it does explain that the training

1 that Amidi teaches is that in response to an error
2 being detected, Amidi will try the reference
3 again, and based on whether an error is detected
4 again on the second -- on the retransmission, on
5 the second attempt, Amidi will either recognize
6 the error as being what is called a random error
7 or potentially a permanent error and take
8 corrective action in the latter case.

9 Q So if I can unpack that a little bit, in
10 Amidi, the memory module is operating in normal
11 operations, and it transmits address and command
12 signals, and there's an error. Is that correct?

13 MR. SUH: Objection.

14 A Yes, there would be an error.

15 Q Okay. And then what's the training at
16 that point in your opinion in Amidi? Or maybe I
17 should ask you, and then what happens next in
18 Amidi?

19 A Okay. So, in Amidi, the memory
20 controller will retransmit the address and command
21 signals. It will attempt the same access again,
22 and on that second access, looking at paragraph 26
23 now, Amidi says if no error is found during
24 retransmission, the memory controller 110 can
25 conclude that the error was random and resume

1 normal operation. If an error is again declared
2 during retransmission, the memory controller can,
3 for example, mark the transmitted address as a bad
4 memory location and reprocess the instruction from
5 the processor to derive and transmit a new set of
6 address command signals corresponding to a
7 different memory location to the memory module
8 150.

9 Q So then what is the specific act or acts
10 of training that you believe Amidi shows?

11 A Amidi shows training by performing the
12 access a second time, and if there's an error
13 that's declared on the second attempt, then Amidi
14 will mark that address as a bad memory location
15 and substitute a different address for that access
16 and for future reference.

17 Q Okay. So then in your Hazelzet and
18 Amidi combination, then the memory module is in
19 the parity mode; is that correct?

20 A Yes, it's in the parity mode.

21 Q And there is an address and command
22 signal that is sent from the memory controller to
23 the memory module, correct?

24 A Yes.

25 Q And Hazelzet figures 4A and 4B determine

1 that there is an error. Correct?

2 **A Yes, determines there's an error.**

3 Q So then how are you modifying Hazelzet
4 in view of Amidi's training from that point?

5 **A Okay. So at that point there's an error**
6 **detected under Hazelzet. Then following what**
7 **Amidi says, that access will be tried again and --**

8 Q In the parity mode?

9 **A No, it will be tried again in the ECC**
10 **mode. It will be retransmitted, tried again in**
11 **the ECC mode. And based on the result of that**
12 **second attempt, following the teachings of Amidi,**
13 **if the access continues to show errors, then the**
14 **memory location associated with that access will**
15 **be marked so it will not be used, and so that a**
16 **different memory address -- so that memory address**
17 **would map to a different location in the memory**
18 **system.**

19 Q Okay. Since you were in your -- since
20 you're referencing your declaration a few answers
21 ago, specifically paragraph 153, can I direct you
22 to paragraph 152 of your declaration?

23 **A Okay.**

24 Q So in paragraph 152 you state that you
25 believe that the claims would be obvious in view

1 of Hazelzet and Amidi under the broadest
2 reasonable construction of the term "train." Do
3 you see that?

4 **A Yes.**

5 **Q** Do you believe that the claims would be
6 obvious over Hazelzet and Amidi under a narrower
7 construction standard than the broadest reasonable
8 construction?

9 **A** Okay. So what I had in mind, the reason
10 that I wrote it in the way that you just read to
11 the record is an issue associated with the
12 interpretation of training, and that's covered
13 starting on page 39 of the declaration.

14 **Q** Page 49, not paragraph?

15 **A** Page 39. It's paragraph 91 of the
16 declaration.

17 **Q** I'm there.

18 **A** I understand there's been, for lack of a
19 better word, I'll call it a dispute or maybe at a
20 minimum some discussion about whether the claim
21 training needs to be training of a memory module,
22 meaning there's some adjustment made within the
23 memory module, or whether it's allowed that the
24 training would only affect differences within the
25 memory controller as long as the module

1 participated in the training.

2 So going back to your specific question
3 at 152, what I was referring to there is that the
4 training disclosed by Amidi is a training of the
5 memory controller such that it would know whether
6 a particular memory address should be marked as
7 being invalid and remapped to another location or
8 not. So that's what I meant, it's the memory
9 controller that is being trained with involvement
10 of the memory module, but no change is made in the
11 memory module as a result of the training.

12 Q So you don't believe that that mark
13 that's disclosed in paragraph 26 of Amidi relates
14 to the memory module?

15 MR. SUH: Objection, form.

16 A In general, it's not my understanding,
17 but I think even specifically looking at that
18 paragraph 26, it says, "If an error is again
19 declared during retransmission, the memory
20 controller can, for example, mark the transmitted
21 address location as a bad memory location."

22 So it is the memory controller that's
23 keeping track of that error condition --

24 Q I see.

25 A -- to avoid the same error in the

1 **future.**

2 Q So, then, is it your view that the
3 claims are obvious in view of Hazelzet and Amidi
4 only if training is read to encompass training of
5 the memory controller?

6 A Let me say that I haven't -- I haven't
7 considered whether -- whether it would be --
8 whether it would be obvious otherwise. I don't
9 think -- I don't think I'm prepared to offer an
10 opinion other than what I've written here, which
11 is that it would be obvious, particularly the
12 claim 1 here, talking about claim 1 would be
13 obvious over the combination of Hazelzet and Amidi
14 when the term "training" does include training of
15 the memory controller.

16 Q Well, since you directed us to page 39
17 of your declaration, let me direct you to page 40,
18 specifically paragraph 94 that spans from 40 to
19 41. Can you take a moment to read that.

20 A To read which?

21 Q Paragraph 94.

22 A 94. (Document review.)

23 Okay, I've read through that.

24 Q When I take a look at page 41,
25 specifically you state, "As discussed below,

1 Hazelzet in view of Talbot or Buchmann discloses
2 training under both the most reasonable
3 construction and the broadest reasonable
4 construction. On the other hand, Hazelzet in view
5 of Amidi discloses training under the broadest
6 reasonable construction."

7 Do you see that?

8 **A Yes, I see that.**

9 Q So when I look at that passage, it
10 suggests to me that you have considered whether
11 Hazelzet in view of Amidi discloses training under
12 the most reasonable construction, given the
13 phraseology.

14 A I might have missed something, but I
15 didn't hear a question.

16 Q Correct?

17 A I mean, that may have been your
18 interpretation. What I can tell you is that I was
19 limiting my opinion to training under the broadest
20 reasonable construction. Sitting here right now,
21 I don't see how that obviousness combination would
22 teach the training if the training had to involve
23 some changes within the memory module, but I don't
24 believe that I considered that in sufficient
25 detail to form an opinion that was documented

1 **here.**

2 Q Okay. So would it be fair to say that
3 in your declaration that accompanied the petition,
4 you didn't consider whether Hazelzet in view of
5 Amidi discloses training under the "most
6 reasonable construction"?

7 A I would say that I considered it, but I
8 don't recall that I offered an opinion. I don't
9 see that this is expressing an opinion about that.

10 Q Okay. Would you say that Amidi's
11 training involves -- strike that.

12 Would you say that Amidi's training
13 involves phase adjustment or bit-lock analysis
14 that we discussed with regard to Talbot and
15 Buchmann earlier in the day?

16 MR. SUH: Objection. Calls for
17 speculation. Relevance.

18 A I don't recall that this expressed
19 disclosure of those training techniques in Amidi.

20 Q Would you say that there's any
21 disclosure of phase adjustment, synchronization,
22 bit-lock alignment in Amidi?

23 A To the best of my recollection, I don't
24 recall that there was any.

25 Q Dr. Alpert, how did you come up with

1 your construction of training in paragraphs 91
2 through 94 of your declaration?

3 A Well, I understand that there's
4 different standards for interpreting claims in an
5 IPR such as this one compared to some other forms,
6 such as, I believe, the Federal Court and the ITC.
7 And so in coming up with the broadest reasonable
8 interpretation, I considered that one
9 interpretation would certainly be that the module
10 itself was trained. And then I understood as
11 summarized in paragraph 92, that the patent owner
12 had represented that the training sequence could
13 include the training of the memory controller.
14 And I thought that if that was what the patent
15 owner believed and represented, then such an
16 interpretation, you know, that I should conclude
17 and assume that the broadest reasonable
18 interpretation includes what the patent owner had
19 considered, I believe, reasonably in these other
20 forms.

21 Q Okay. Well, you certainly have
22 discussed related proceedings, but I believe that
23 you know that a claim construction analysis
24 includes consideration of their claim language,
25 correct?

1 **A Certainly, yes, that's where it would**
2 **start.**

3 Q Did you consider the claim language when
4 you construed training in paragraphs 91 through 94
5 of your declaration?

6 **A Yes, it would start with the claim**
7 **language and considered the broadest reasonable**
8 **interpretation in light of the specification.**

9 Q Did you consider the specification of
10 the '623 patent when you construed training in
11 paragraphs 91 through 94 of the declaration?

12 **A Yes, I did.**

13 Q Is there any reason why you don't
14 reference either of them in these paragraphs?

15 **A Well, it looks like in paragraph 93**
16 **there is a citation to column 4, lines 1 to 56 of**
17 **the '623 patent.**

18 Q But there's no discussion of the
19 specification in the sense that how it would
20 inform one of ordinary skill in the art what the
21 proper construction of training is, correct?

22 **A That's correct, there's not a discussion**
23 **there.**

24 Q And did you review or consider the '623
25 prosecution history to determine your construction

1 of training?

2 A I considered the prosecution history.
3 Sitting here right now I don't remember that there
4 was anything in particular that informed me about
5 interpretation of training.

6 Q But you don't specifically recall
7 reviewing the prosecution history of the '623
8 patent to determine what the proper construction
9 of training should be, correct?

10 A Sitting here right now, I don't recall
11 specifically, say, searching for training.
12 Certainly, as I reviewed portions of the patent
13 and particularly the correspondence that went back
14 and forth where there were rejections and both
15 remarks and amendments made, then I was looking to
16 inform myself generally of how certain claims --
17 certain claim terms might be interpreted.

18 Q Do you recall referring to any technical
19 dictionaries in reaching your construction of
20 training in paragraphs 91 through 94 of your
21 declaration?

22 A I don't recall looking at technical
23 dictionaries for that.

24 Q Dr. Alpert, do you have any direct
25 technical experience with designing the training

1 of a memory module?

2 MR. SUH: Objection to form. Relevance.

3 A No, not -- at least not that I can
4 recall.

5 Q Dr. Alpert, do you have any direct
6 technical experience with handling or implementing
7 memory modules training?

8 MR. SUH: Same objection.

9 A I don't recall having any direct
10 experience with that.

11 Q So we've discussed what you considered
12 to be training in Hazelzet, Buchmann, Talbot and
13 Amidi, correct?

14 A Yes, I think we've discussed for all of
15 those references.

16 Q So I would like to ask you, in the case
17 of Talbot and Buchmann, we discussed bit-lock
18 synchronization as an example of training in those
19 references, correct?

20 A Yes, that's what I recall was an
21 example.

22 Q Do you recall testifying earlier today
23 that the read and write commands would be an
24 example of training in Hazelzet?

25 A Yes.

1 Q So what I would like to understand from
2 you is based on those two examples from bit-lock
3 synchronization to read and write commands, what
4 do you understand training to be?

5 MR. SUH: Objection to form.

6 A **Generally I would say that training**
7 **would involve running certain operations in order**
8 **to determine whether the memory module is**
9 **operating correctly in the system and to make**
10 **certain adjustments or changes, whether in the**
11 **memory controller or in the memory module itself**
12 **to compensate for any deficiencies that are**
13 **identified.**

14 Q So you believe what's common among
15 Buchmann, Talbot and Hazelzet with regard to their
16 specific forms of training, be it bit-lock
17 synchronization or read/write commands, is that
18 they involve running certain operations in order
19 to determine whether the memory module is
20 operating correctly?

21 MR. SUH: Objection, form.

22 A **Yes, I believe that would be a common**
23 **characteristic of the training for each of those**
24 **references.**

25 MR. ARJOMAND: Okay. Let's take a quick

1 break. I'll take a look through the final pages
2 of my outline and we'll see if there are any
3 further questions to be asked.

4 MR. SUH: All right.

5 (A brief recess was taken.)

6 MR. ARJOMAND: Back on the record.

7 BY MR. ARJOMAND:

8 Q Dr. Alpert, do you recall when we were
9 discussing the Hazelzet-Buchmann combination, we
10 discussed in your view that one of ordinary skill
11 in the art could put a TS3 message on the UE line,
12 on Hazelzet?

13 A Generally I do recall some point like
14 that came up for discussion.

15 Q Turning to the Hazelzet-Talbot ground,
16 in your combination, what is being placed on the
17 UE line of Hazelzet?

18 MR. SUH: Object to form. Relevance.

19 A Okay, so the combination of Hazelzet and
20 Talbot, the UE signal can be used, for example, to
21 detect and to communicate that an error has
22 occurred in a training pattern, for example, a CRC
23 mismatch detected by the buffer.

24 Q So can you explain -- strike that.

25 Are you looking at a specific paragraph

1 in your declaration to assist you with that
2 testimony?

3 A No, I was just looking generally at what
4 was described in there, so I wasn't citing to a
5 particular paragraph.

6 Q What portion of your declaration were
7 you looking at generally?

8 A I was looking at I think probably the --
9 the closest point looks like it's paragraph 159.
10 It's on page 95. I think it carries over to
11 there.

12 About the middle of that paragraph, it's
13 a statement that explains, it says, "Further,
14 modifying Hazelzet's buffer device in view of
15 Talbot's buffer unit 170 would have rendered
16 obvious the claim even under the narrower
17 construction of training that is limited to
18 training of a memory module. Indeed, Hazelzet
19 explains that Talbot CRC is an example of its
20 error detection and/or correction methods," citing
21 to Hazelzet at paragraph 127, in quotations, "any
22 or all of the various elements may include error
23 detection and/or correction methods such as CRC
24 (Cyclic Redundancy Code), EDC (Error Detection and
25 Correction), parity or other encoding/decoding

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1 **methods suited for this purpose."**

2 Q Thank you for that testimony. It seems
3 to me that in your Hazelzet and Talbot
4 combination, it's the memory controller that's
5 being trained?

6 MR. SUH: Objection. Mischaracterizes
7 testimony.

8 MR. ARJOMAND: I'm just basing it on
9 that sentence he just read --

10 MR. SUH: Sorry.

11 MR. ARJOMAND: -- two minutes ago.

12 MR. SUH: Still, objection,
13 mischaracterizes testimony.

14 A **(Document review.)**

15 **So can I hear that question again.**

16 Q In your Hazelzet and Talbot combination,
17 is the memory controller being trained?

18 A **The memory controller is being trained.**
19 **And as I recall, there's also training in relation**
20 **to what's shown in figure 2, as the drivers from**
21 **the buffer 170 to the memory controller. There's**
22 **a buffer -- there's a driver 210 and a driver 211.**
23 **As I was looking through, I did not find the**
24 **specific citation to where it talks about how**
25 **those drivers are adjusted according to the**

1 **training sequence.**

2 Q Are you referring to figure 2 of Talbot?

3 A **Yes, figure 2 of Talbot.**

4 Q So as you sit here today, do you recall
5 any training of the memory module in your Hazelzet
6 and Talbot combination?

7 A **As I'm sitting here today, I don't
8 recall specifically what training might occur.**

9 Q Okay. Let's move on to your Hazelzet
10 and Amidi combination.

11 So what is placed on the UE line in that
12 combination?

13 MR. SUH: Objection, form. Relevance.

14 A **On the UE line would be an indication of
15 whether an uncorrectable error had been detected
16 based on the transmission and retransmission by
17 Amidi.**

18 Q Okay. What would be the signal on the
19 UE line in your Hazelzet and Talbot combination?

20 MR. SUH: Asked and answered.
21 Objection.

22 A **Well, there's a large number of ways in
23 which the teachings could be combined, but one
24 example in response to your question is that
25 Talbot could use the data received from the memory**

1 controller together with the CRC received by the
2 memory controller in order to report back if there
3 had been an error in the transmission.

4 Q So you're saying that the CRC signal
5 would be on the UE line in your Hazelzet-Talbot
6 combination?

7 A No, I'm saying that the memory buffer of
8 Talbot would perform a CRC check on the data it
9 receives from the memory controller and report
10 back on the UE line whether or not there had been
11 an error detected.

12 Q So there would be a UE signal on the UE
13 line in your Hazelzet-Talbot combination?

14 MR. SUH: Same objection.

15 A Yes. Yes, the CRC -- if there's an
16 error with the CRC, it would be uncorrectable.

17 Q But you're not putting the CRC signal on
18 the EU line in your Hazelzet-Talbot combination;
19 instead you're just putting a UE signal on the UE
20 line?

21 A It would be possible to put the entire
22 CRC on there, but I think it would work -- it
23 would be a useful combination that would reduce
24 the changes to Hazelzet if Hazelzet just reported
25 an indication that there would have been an error

1 in connection with the CRC.

2 Q I see.

3 So as you sit here today, in your
4 Hazelzet and Talbot combination, what's on the UE
5 line is a UE signal?

6 MR. SUH: Objection to form.
7 Mischaracterizes testimony.

8 A I'm not sure I understand the question.
9 I'm just saying that a UE signal would be on a UE
10 line. I mean, it's just a name, and that would be
11 connoted by calling it a UE line.

12 Q I'm just trying to understand what your
13 combination is between Hazelzet and Talbot that --
14 strike that.

15 So just to confirm, is it your testimony
16 that in your Hazelzet and Talbot combination,
17 there would be a UE signal on the UE line of
18 Hazelzet?

19 A Yes, that's certainly one combination
20 that I envisioned and I believe a person of
21 ordinary skill in the art would look at. The UE
22 signal in the combination with Talbot would be
23 indicating that there was a CRC error rather than
24 simply a parity error.

25 Q Just the same question with regard to

1 your Hazelzet and Amidi combination, would there
2 be a UE signal on the UE line 121 of Hazelzet?

3 MR. SUH: Objection. Asked and
4 answered. Relevance.

5 **A Yes, there would be a UE signal on the**
6 **UE line.**

7 Q Since you have your declaration in front
8 of you, can I -- strike that.

9 Just to clarify, would it be the ECC UE
10 signal on the UE line in your Hazelzet-Amidi
11 combination?

12 MR. SUH: Objection. Mischaracterizes
13 testimony.

14 **A Yes, just to understand a little bit**
15 **more context, are we talking about the status**
16 **signal in the second mode? I hope that's what**
17 **we've been talking about.**

18 Q In the ECC mode, there's a UE signal on
19 the UE line, correct?

20 **A In Hazelzet, yes.**

21 Q Right.

22 And so in your Hazelzet and Amidi
23 combination, would the signal be the ECC UE signal
24 on the UE signal line?

25 MR. SUH: Objection. Incomplete

1 hypothetical.

2 **A** Yes, a combination would tell when there
3 was training that was occurring, it would be in
4 the ECC mode, and the UE signal would indicate an
5 uncorrectable ECC error.

6 **Q** You just mentioned Talbot, but I believe
7 you meant Amidi?

8 **A** I think so, yes.

9 **Q** It's a little late in the day. All
10 right.

11 Let me just ask you a few questions
12 relating to your declaration. Can I direct you to
13 the last page of your declaration.

14 **A** I'm there.

15 **Q** Is that your signature, Dr. Alpert?

16 **A** Yes, it is.

17 **Q** Did you sign this declaration under the
18 penalty of perjury?

19 **A** Whatever it says here. I certainly
20 understood that there were potential penalties if
21 I had done anything incorrectly, and I have no
22 interest in doing anything other than stating the
23 truth as I understood it.

24 **Q** Okay.

25 Do you represent that the opinions

1 contained in your declaration, Exhibit 1003, are
2 your independent opinions?

3 **A Yes, I do.**

4 Q Do you recall what time you utilized or
5 needed to prepare your declaration?

6 MR. SUH: Objection, form.

7 Q Let me ask that question again.

8 Over what period of time did you prepare
9 your declaration?

10 MR. SUH: Objection. Calls for
11 speculation.

12 **A I generally recall that it was starting**
13 **in, let's just say, the first half of November of**
14 **2017 until the declaration was executed on**
15 **December 13th. I don't know when it was produced.**

16 Q So do you recall how many hours you
17 spent in preparing your declaration from November
18 of 2013 -- 2017 to December 13th, 2017, when you
19 signed your declaration?

20 MR. SUH: Same objection.

21 **A No, I don't have any recollection.**

22 Q Was it more than ten hours?

23 MR. SUH: Same objection.

24 **A Just generally I would say that it -- it**
25 **certainly would have been more than ten hours.**

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1 Q Would it be more than 50 hours?

2 MR. SUH: Same objection.

3 A I don't have a recollection.

4 Q Was it more than 100 hours?

5 MR. SUH: Same objection.

6 A I don't have any specific recollection,
7 but 100 hours seems like it probably would have
8 been -- it would have been less than that, but I
9 don't have a recollection.

10 Partly there was, I think we talked
11 before how it was just about the period I had been
12 moving to California. So a lot of things going on
13 besides just the work on this, so I just don't
14 recall with any more specificity.

15 Q Other than counsel, did anyone else
16 assist you in preparing this declaration?

17 A No.

18 Q At the time you prepared this
19 declaration, did you believe the statements made
20 in the declaration were true?

21 A Yes.

22 Q Are there any statements in your
23 declaration that you now believe are not true?

24 A No.

25 Q Does this declaration set forth all of

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1 your opinions in connection with claim
2 construction?

3 MR. SUH: Objection, form.

4 A I would say so other than I'm just
5 thinking here right now that, of course, there's
6 many of the terms from the claims are not listed
7 specifically here, in which case, my
8 understanding, they would be given the plain and
9 ordinary meaning.

10 Q Okay. And does this declaration set
11 forth all of your opinions in connection with the
12 validity of the claims at issue?

13 MR. SUH: Objection, form.

14 A Yes.

15 Q Are all the basis -- strike that.
16 Are all the bases for your opinions set
17 forth in your declaration, Exhibit 1003?

18 MR. SUH: Same objection.

19 A Yes, they are.

20 Q Dr. Alpert, you've been retained by
21 Hynix in this IPR proceeding, correct?

22 A Yes, sir, at least by the attorneys
23 representing Hynix.

24 Q You've been retained by Hynix or the
25 attorneys representing Hynix in four other IPR

1 proceedings; is that correct?

2 **A Did you say four other?**

3 Q (Nodding head.)

4 **A Not to the best of my recollection.**

5 Q Do you believe it's more than four?

6 **A No.**

7 Q Well, I have here a number of IPRs
8 listed where I believe you submitted a
9 declaration. Did you submit a declaration for
10 Hynix or its attorneys in IPR2014-00970?

11 MR. SUH: Objection. Calls for
12 speculation.

13 **A I don't remember the number. The one**
14 **other that I'm recalling is, I believe it was the**
15 **'837 patent, also to the same inventor, and we**
16 **were sitting here last August, I believe. That's**
17 **the only other one that I recall sitting here that**
18 **related to Hynix.**

19 Q Okay. So you haven't been hired by
20 Hynix or the attorneys for Hynix in any other IPR
21 beyond the IPR for the '837 patent and the IPR for
22 the '623 patent?

23 **A I don't recall any other matters like**
24 **that.**

25 Q Dr. Alpert, did you provide your rate

1 for providing expert services?

2 **A I believe so.**

3 **Yes, I'm just looking at paragraph 8**
4 **indicates the rate -- the compensation rate is**
5 **\$550 per hour.**

6 Q Now turning to paragraph 9, it states
7 that you previously submitted declaration in five
8 IPR proceedings. I certainly recognize the final
9 IPR, IPR2017-00548, as being the IPR in the '837
10 patent, for the '837 patent, I should say.

11 Do you recall if those other four IPRs
12 related to Hynix?

13 **A To the best of my recollection, they did**
14 **not relate to Hynix.**

15 MR. ARJOMAND: Let's take a quick
16 two-minute break and I'll come back.

17 (A brief recess was taken.)

18 MR. ARJOMAND: Back on the record.

19 BY MR. ARJOMAND:

20 Q Dr. Alpert, can I direct you to
21 paragraph 159 of your declaration.

22 **A Looks like a long one.**

23 Q I just want to understand, in this
24 paragraph you are referencing how Talbot meets the
25 element of a notification signal indicating the

1 status of one or more training sequences, correct?

2 **A Yes, that's what the first sentence of**
3 **the paragraph says.**

4 Q Okay. I wanted to direct you to page 93
5 of your declaration, which is the continuation of
6 paragraph 159. Do you see the sentence that says,
7 "During its training mode, Talbot explains that
8 the memory controller monitors the looped back
9 training pattern data (i.e., also referred to as
10 the CRC information) and shifts the training
11 pattern data in increments until the looped back
12 training pattern data is byte-locked (or
13 bit-locked)."

14 **A Okay, I do see that.**

15 Q My question to you, Dr. Alpert, is, do
16 you believe that this disclosure that I just read
17 of Talbot is what meets in your opinion the claim
18 language notification signal indicating the status
19 of one or more training sequences?

20 MR. SUH: Objection, form.
21 Mischaracterizes testimony.

22 **A (Document review.)**

23 **Yes, I believe it is a good description**
24 **of how Talbot discloses the notification signal.**

25 MR. ARJOMAND: Okay, thank you.

1 With that, I have no further questions.

2 EXAMINATION BY COUNSEL FOR PETITIONERS

3 BY MR. SUH:

4 Q So I have a couple of questions. Before
5 the earlier -- right after the earlier break, you
6 said you had something to add to -- regarding
7 Talbot, and counsel said I could redirect instead
8 because he was running low on time. Do you recall
9 that?

10 A I do.

11 Q So what was that about?

12 A Yes, what I noticed, I think we were
13 talking about paragraph 52, and I noticed that
14 paragraph 53 describes a -- one operation of
15 training for Talbot, and it talks about to train
16 the DDQ path, it indicates that the memory
17 controller will adjust the phase of the data to
18 obtain a bit error rate of substantially 50
19 percent. And then it says, "The 50 percent
20 transition error rate may be indicative that the
21 write data is being sampled near the edge so,
22 therefore, the memory controller adjusts the phase
23 of the write data back by," it says, "0.5 UI," so
24 0.5 clock cycles. And I was -- I did just want to
25 point that out because I believe very early on,

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1 **maybe even this morning, I had been asked some**
2 **questions about kind of examples of training**
3 **patterns, and I think that I gave this example. I**
4 **recall giving this example. At that time I didn't**
5 **recall that it had been documented in Talbot.**

6 Q I see. Thank you.

7 Okay. And before the break, counsel
8 directed you to paragraph 159 of your declaration
9 and asked you whether in your Hazelzet and Amidi
10 combination, whether it was the memory controller
11 that was being trained as opposed to the memory
12 module. I think your answer to that was the
13 memory controller. Do you recall that?

14 MR. ARJOMAND: Objection, form.
15 Objection, leading.

16 A **I believe I generally recall that.**

17 Q I recognize that paragraph 159 is very
18 long. It's four pages long. Can you read
19 paragraph 159 of your declaration again.

20 A **Actually let me just go back to clarify.**
21 **The question that you asked related to Amidi or**
22 **Talbot? And I might have heard it wrong.**

23 Q Maybe it was Talbot. Oh, maybe that was
24 why. So if it was Amidi -- so 159 is about
25 Talbot. Okay. So strike that.

1 So during the course of your testimony
2 today, you referenced your declaration at certain
3 points in time, right?

4 **A Yes, it did come up.**

5 Q If you forgot to mention some sections
6 of your declaration that may have been responsive
7 to the questions that you were asked today, did
8 you mean to take back anything you wrote in your
9 declaration?

10 MR. ARJOMAND: Objection, form.

11 Objection, leading.

12 **A No, I didn't mean to take back. It was**
13 **just a matter of trying to identify from the Table**
14 **of Contents and my recollection where the most**
15 **relevant information was responsive to the**
16 **questions.**

17 Q Was training a well understood term to a
18 POSITA by June of 2009?

19 **A Yes, it was. In fact, I had been --**
20 **there had been a kind of an everyday example or**
21 **kind of an antidote I remembered that wasn't in**
22 **here. I failed to bring it up earlier. I just**
23 **was remembering at Intel when we talk about**
24 **anybody learning a new skill, whatever it might**
25 **be, technical skill or management skill, then they**

1 would always talk about, you know, how to develop
2 a skill, you need some awareness, training and
3 then feedback. And so I think that training is
4 used in that same everyday sense here. You get a
5 chance to try something, then you get some
6 feedback, and based on that, able to improve the
7 quality of the operation, in this case from memory
8 modules.

9 Q And does the '623 patent give a special
10 definition of the term "training"?

11 MR. ARJOMAND: Objection. Leading.

12 A No, I don't believe within the patent
13 itself there's any special definition. It would
14 be the plain and ordinary meaning.

15 Q Does the '623 patent use the term
16 "training" in a plain and ordinary sense as
17 understood by a POSITA by June of 2009?

18 MR. ARJOMAND: Objection, leading.

19 A Yes, I believe it does.

20 Q Earlier in connection with your
21 testimony regarding how memory modules can be more
22 sophisticated compared to processors, you
23 mentioned a particular type of training that
24 involves the DRAM performing some test and
25 reporting back to either the buffer or memory

1 controller whether there are some errors. Do you
2 recall that?

3 MR. ARJOMAND: Objection, form.

4 A Generally I do.

5 Q And do you recall the name of the
6 training you were talking about then?

7 A I don't -- I don't know for certain
8 which I was talking about, but there is something
9 called a ZQ training. There's both a long and a
10 short version of it, and I believe that's the type
11 of training that I did have in mind at least in
12 response to one or more questions in that
13 sequence.

14 Q So you said a ZQ training. Was that
15 training known before June of 2009? Do you happen
16 to know?

17 A I believe that it was.

18 Q And do you know what a CA bus training
19 is?

20 MR. ARJOMAND: Objection, leading.

21 A No, I'm not familiar with the -- what
22 type of training that involves.

23 Q Would it be fair to say that you are not
24 testifying about the CA bus training at any point
25 in time of your deposition today, correct?

1 MR. ARJOMAND: Objection. Leading.

2 A I would say that's correct. I was not
3 testifying about the CA bus or CA bus training I
4 think you called it.

5 MR. SUH: I pass the witness.

6 MR. ARJOMAND: Let's take a quick break.
7 I'll consult here with my colleague and hopefully
8 we can end the deposition very soon.

9 (A brief recess was taken.)

10 MR. ARJOMAND: Back on the record. We
11 have no further questions.

12 MR. SUH: Okay. Thank you very much.

13

14 (Signature having not been waived, the
15 deposition of Donald Alpert, Ph.D. was concluded at
16 7:01 p.m.)

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1 CERTIFICATE OF SHORTHAND REPORTER

2 I, Michele E. Eddy, Registered Professional
3 Reporter, Certified Realtime Reporter, and Notary
4 Public in and for the District of Columbia, the
5 officer before whom the proceedings were taken, do
6 hereby certify that the foregoing transcript is a true
7 and accurate record of these proceedings; that said
8 proceedings were taken in Stenotype note by me on the
9 20th day of July, 2018, commencing at 10:00 a.m. and
10 ending at 7:01 p.m.

11 I further certify that present on behalf of
12 the Petitioner, Wonjoo Suh, Esquire, of Sidley Austin,
13 and on behalf of the Patent Owner, Mehran Arjomand,
14 Esquire, of Morrison Foerster.

15 I further certify that I am not related to,
16 nor associated with any of the parties or their
17 attorneys, nor do I have any disqualifying interest,
18 personal or financial in the actions within.

19 IN WITNESS WHEREOF, I have hereunto set my
20 hand and affixed my notarial seal this 22nd day of
21 July, 2018.

22 My commission expires July 14, 2022

23

24

25 MICHELE E. EDDY

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1 ACKNOWLEDGMENT OF DEPONENT

2

3 I, _____, do hereby
 4 acknowledge that I have read and examined the
 5 foregoing testimony, and the same is a true, correct
 6 and complete transcription of the testimony given by
 7 me, and any corrections appear on the attached Errata
 8 Sheet signed by me.

9

10 _____

11 (DATE)

(SIGNATURE)

12

13 NOTARIZATION (If Required)

14 State of _____

15 County of _____

16 Subscribed and sworn to (or affirmed) before me on
 17 this _____ day of _____, 20____, by
 18 _____, proved to me on the
 19 basis of satisfactory evidence to be the person who
 20 appeared before me.

21 Signature: _____

22 (Seal)

23

24

25

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ERRATA SHEET FOR THE TRANSCRIPT OF:

Caption: SK Hynix, Inc, et al. v. Netlist, Inc.

Deponent: Donald Alpert, Ph.D.

Dep. Date: July 20, 2018

I wish to make the following changes for the following reasons:

[illegible]

SIGNATURE OF THE WITNESS

this 25TH day of JULY, 2018.